SGM41285
70V, 300mW Step-Up Converter and Current Monitor for APD Bias Applications

GENERAL DESCRIPTION

SGM41285 constant frequency pulse width modulating (PWM) step-up DC/DC converter features an internal switch and a high-side current monitor with high speed adjustable current limiting. This device is capable of generating output voltages up to 70V and providing current monitoring up to 4mA. The SGM41285 operates from 2.8V to 5.5V.

The constant frequency (850kHz) current mode PWM architecture provides low noise output voltage that is easy to filter. A high voltage internal power MOSFET allows this device to boost output voltages up to 70V. Internal soft-start circuitry limits the input current when the boost converter starts. The SGM41285 features a shutdown mode to save power.

The SGM41285 includes a current monitor with more than three decades of dynamic range and monitors current ranging from 500nA to 4mA with high accuracy. Resistor-adjustable current limiting protects the APD from optical power transients. A clamp diode protects the monitor's output from overvoltage conditions. Other protection features include cycle-by-cycle current limiting of the boost converter switch, under-voltage lockout (UVLO), and thermal shutdown if the die temperature reaches +170℃.

The SGM41285 is available in a Green TQFN-3×3-16L package. It operates over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **Input Voltage Range: 2.8V to 5.5V**
- **Wide Output Voltage Range from (V_{IN} + 5V) to 70V**
- **Internal 0.6Ω (TYP) 72V MOSFET**
- **Boost Converter Output Power:**
  SGM41285A: 300mW
  SGM41285B: 200mW
- **High-side Current Monitor Ratios:**
  SGM41285A: 1:1
  SGM41285B: 5:1
- **Accurate ±5% (1:1 and 5:1) High-side Current Monitor**
- **Resistor-Adjustable Ultra-Fast APD Current Limit (1μs Response Time)**
- **Open-Drain Current-Limit Indicator Flag**
- **850kHz Fixed Switching Frequency**
- **Constant PWM Frequency Provides Easy Filtering in Low Noise Applications**
- **Internal Soft-Start Function**
- **Less than 1μA Shutdown Current**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TQFN-3×3-16L Package**

APPLICATIONS

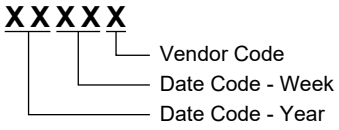
Avalanche Photodiode Biasing and Monitoring
PIN Diode Bias Supply
Low-Noise Varactor Diode Bias Supply
FBON Modules
GPON Modules

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41285A	TQFN-3×3-16L	-40℃ to +125℃	SGM41285AXTQ16G/TR	GMDTQ XXXXX	Tape and Reel, 4000
SGM41285B	TQFN-3×3-16L	-40℃ to +125℃	SGM41285BXTQ16G/TR	GMETQ XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, nSHDN, FB, nILIM, RLIM, CNTRL, CLAMP to SGND ..... -0.3V to 6V
SW to PGND ..... -0.3V to 76V
BIAS to SGND ..... -0.3V to 76V
APD, to SGND ..... -0.3V to (V_{BIAS} + 0.3V)
PGND to SGND ..... -0.3V to 0.3V
MOUT to SGND ..... -0.3V to (V_{CLAMP} + 0.3V)
Package Thermal Resistance
TQFN-3×3-16L, θ_{JA} ..... 45℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
MM 200V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 2.8V to 5.5V
Operating Ambient Temperature Range ..... -40℃ to +125℃
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

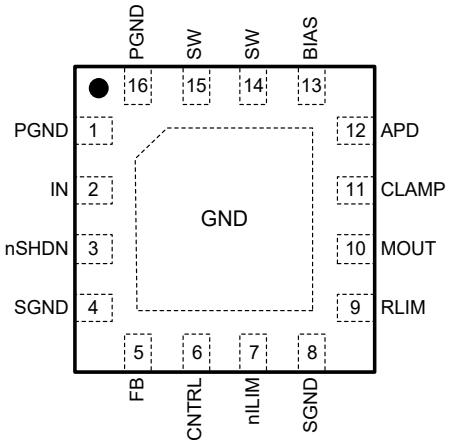
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3×3-16L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 16	PGND	Power Ground. Connect the negative terminals of the input and output capacitors to PGND. Connect PGND externally to SGND at a single point, typically at the return terminal of the output capacitor.
2	IN	Input Supply Voltage. Bypass IN to PGND with a ceramic capacitor of 1μF minimum value.
3	nSHDN	Active Low Shutdown Control Input. Apply a logic low voltage to nSHDN to shut down the device. Connect nSHDN to IN for normal operation. Ensure that V_{nSHDN} is not greater than the input voltage, V_{IN}. nSHDN is internally pulled low. The converter is disabled when nSHDN is left unconnected.
4, 8	SGND	Signal Ground. Connect directly to the local ground plane. Connect SGND to PGND at a single point, typically near the return terminal of the output capacitor.
5	FB	Feedback Regulation Input. Connect FB to the center tap of a resistive voltage-divider from the boost output to SGND to set the output voltage. The FB voltage regulates to 1.20V (TYP) when V_{CNTRL} is above 1.3V (TYP) and to V_{CNTRL} when V_{CNTRL} is below 1.2V (TYP).
6	CNTRL	Control Input for Boost Converter Output-Voltage Programmability. CNTRL allows the feedback set-point voltage to be set externally by CNTRL when V_{CNTRL} is less than 1.2V. Pull CNTRL above 1.3V (TYP) to use the internal 1.20V (TYP) feedback set-point voltage.
7	nILIM	Open-Drain Current-Limit Indicator. nILIM asserts low when the APD current limit has been exceeded.
9	RLIM	Current-Limit Resistor Connection. Connect a resistor from RLIM to SGND to program the APD current-limit threshold. When RLIM is connected to SGND, the current limit is set to 4.5mA.
10	MOUT	Current Monitor Output. For the SGM41285A, MOUT sources a current equal to I_{APD}. For the SGM41285B, MOUT sources a current equal to 1/5 of I_{APD}.
11	CLAMP	Clamp Voltage Input. CLAMP is the external potential used for voltage clamping of MOUT.
12	APD	Reference Current Output. APD provides the source current to the cathode of the photodiode.
13	BIAS	Bias Voltage Input. Connect BIAS to the boost converter output (V_{OUT}) either directly or through a low-pass filter for ripple attenuation. BIAS provides the voltage bias for the current monitor and is the current source for APD.
14, 15	SW	Drain of Internal 72V N-Channel DMOS. Connect inductor to SW. Minimize the trace area at SW to reduce switching-noise emission.
–	Exposed Pad	Exposed Pad. Connect to a large copper plane at the SGND and PGND potential to improve thermal dissipation. Do not use as the only ground connection.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{nSHDN} = V_{CNTRL} = 3.3V, V_{BIAS} = 40V, V_{MOUT} = 0V, V_{PGND} = V_{SGND} = 0V, C_{IN} = 1μF, SW = APD = CLAMP = nILIM = unconnected, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
INPUT SUPPLY								
Supply Voltage Range	V_{IN}			Full	2.8		5.5	V
Supply Current	I_{SUPPLY}	V_{FB} = 1.4V, no switching		Full		190	280	μA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising		Full	2.4	2.5	2.6	V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}			+25℃		200		mV
Shutdown Current	I_{SHDN}	V_{nSHDN} = 0V		Full		0.01	1	μA
Shutdown Bias Current	I_{BIAS_SHDN}	V_{BIAS} = 3.3V, V_{nSHDN} = 0V		Full		0.01	0.6	μA
BOOST CONVERTER								
Output-Voltage Adjustment Range				Full	V_{IN} + 5		70	V
Switching Frequency	f_{SW}			Full	750	850	950	kHz
Maximum Duty Cycle	D_{MAX}			+25℃	87.5	90	92.5	%
FB Set-Point Voltage	V_{FB_SET}			Full	1.175	1.20	1.225	V
FB Input-Bias Current	I_{FB}	V_{FB} = V_{FB_SET}		+25℃			400	nA
Internal Switch On-Resistance	R_{ON}	I_{SW} = 100mA		Full		0.6	1.2	Ω
Peak Switch Current Limit	I_{LIM_SW}			+25℃	0.9	1.1	1.35	A
Peak Current-Limit Response				+25℃		100		ns
Switch Leakage Current		V_{SW} = 72V		+25℃			1	μA
Line Regulation		2.8V ≤ V_{IN} ≤ 5.5V, I_{LOAD} = 4.5mA		+25℃		0.1		%
Load Regulation		0 ≤ I_{LOAD} ≤ 4.5mA		+25℃		0.05		%
Soft-Start Duration				+25℃		4		ms
CONTROL INPUT (CNTRL)								
Maximum Control Input Voltage		FB set point is controlled to V_{CNTRL}		+25℃		1.2		V
CNTRL-to-REF Transition Threshold		V_{FB} = V_{REF} above this voltage		+25℃		1.3		V
CNTRL Input-Bias Current		V_{CNTRL} = V_{FB_SET}		+25℃			400	nA
CURRENT MONITOR								
Bias Voltage Range	V_{BIAS}			Full	10		70	V
Bias Quiescent Current	I_{BIAS}	I_{APD} = 500nA	SGM41285A	Full		220	280	μA
			SGM41285B	Full		220	280	
		I_{APD} = 2mA	SGM41285A	Full		4	4.7	mA
			SGM41285B	Full		2	3	
Voltage Drop	V_{DROP}	I_{APD} = 2mA, V_{DROP} = V_{BIAS} - V_{APD}		Full		1.9	2.3	V
Dynamic Output Resistance at MOUT	R_{MOUT}	R_{MOUT} = $\Delta V_{MOUT}/\Delta I_{MOUT}$, I_{APD} = 2.5mA	SGM41285A	+25℃		5		GΩ
APD Current-Step Response		Step load on I_{APD} = 20μA to 1mA		+25℃		50		ns
MOUT Output Leakage		APD is unconnected		+25℃		1	400	nA
Output Clamp Voltage	V_{MOUT} - V_{CLAMP}	Forward diode current = 500μA		Full	0.8	0.95	1.1	V

ELECTRICAL CHARACTERISTICS (continued)

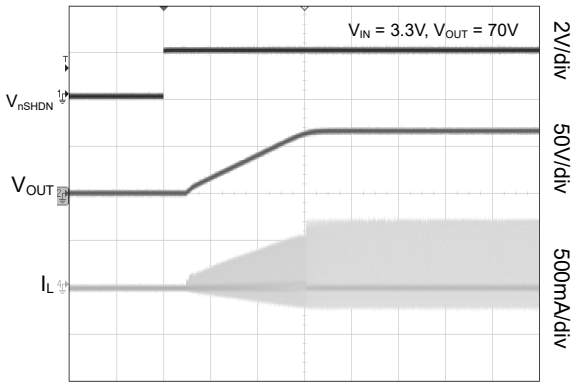
(V_{IN} = V_{nSHDN} = V_{CNTRL} = 3.3V, V_{BIAS} = 40V, V_{MOUT} = 0V, V_{PGND} = V_{SGND} = 0V, C_{IN} = 1μF, SW = APD = CLAMP = nILIM = unconnected, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Current Gain	I_{MOUT}/I_{APD}	I_{APD} = 500nA	SGM41285A	Full	0.965	1.05	1.170	mA/mA
			SGM41285B	Full	0.172	0.2	0.225	
		I_{APD} = 2mA	SGM41285A	Full	0.985	1	1.025	
			SGM41285B	Full	0.195	0.2	0.204	
Power-Supply Rejection Ratio	PSRR	$(\Delta I_{MOUT}/I_{MOUT})/\Delta V_{BIAS}$, V_{BIAS} = 10V to 70V and I_{APD} = 5μA to 1mA	SGM41285A	+25℃		30		ppm/V
			SGM41285B	+25℃		30		
APD Input Current Limit	I_{LIM_APD}			Full	3.95	4.5	5.05	mA
LOGIC I/O								
nSHDN Input Voltage Low	V_{IL}			Full			0.3	V
nSHDN Input Voltage High	V_{IH}			Full	1.5			V
nILIM Output Voltage Low	V_{OL}	I_{LIM} = 2mA		Full			200	mV
nILIM Output Leakage Current	I_{OH}			+25℃			1	μA
THERMAL PROTECTION								
Thermal Shutdown	T_{SHDN}					170		℃
Thermal Shutdown Hysteresis	T_{HYS}					20		℃

TYPICAL PERFORMANCE CHARACTERISTICS

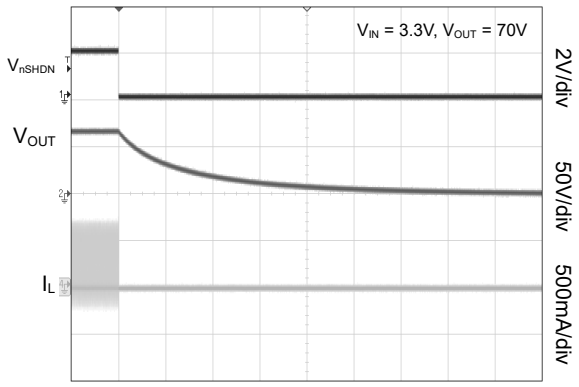
V_{IN} = 3.3V, V_{OUT} = 70V, T_A = +25℃, unless otherwise noted.

Exiting Shutdown



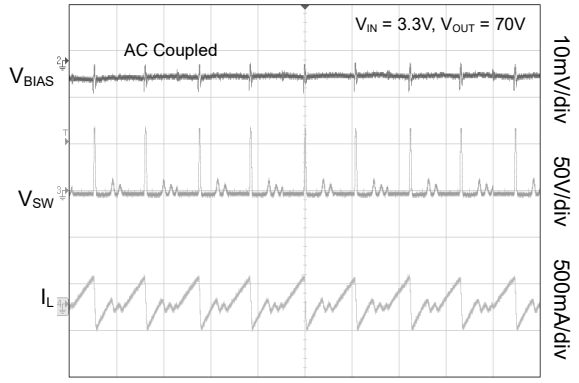
Time (2ms/div)

Entering Shutdown



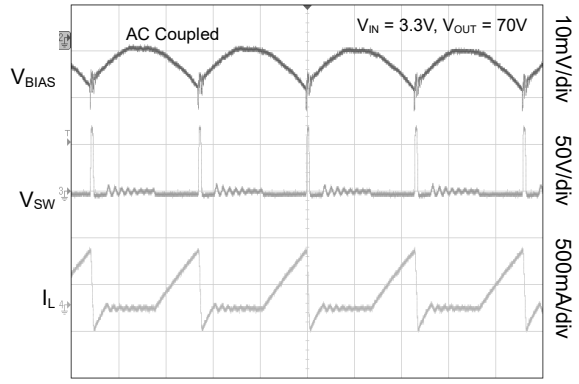
Time (20ms/div)

Light-Load Switching Waveforms with RC Filter



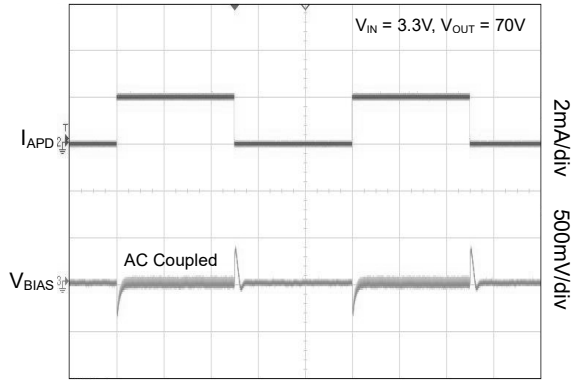
Time (1μs/div)

Heavy-Load Switching Waveforms with RC Filter



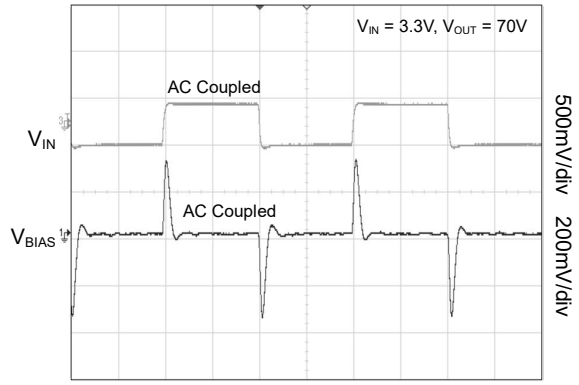
Time (1μs/div)

Load-Transient Response



Time (1ms/div)

Line-Transient Response

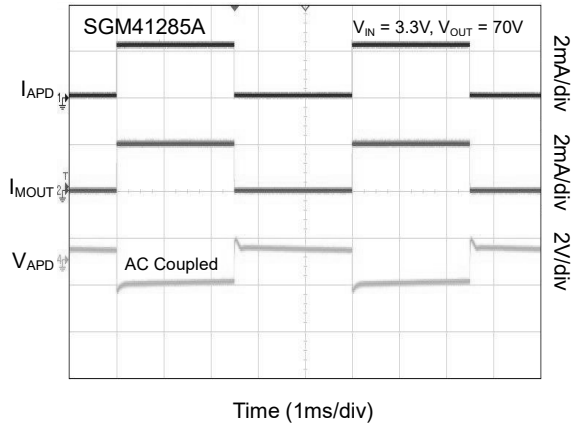


Time (1ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

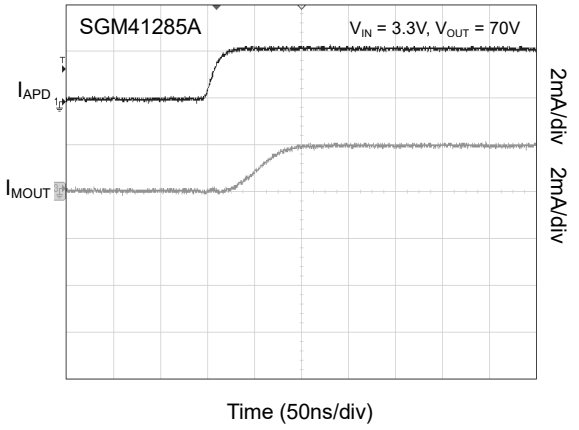
V_{IN} = 3.3V, V_{OUT} = 70V, T_A = +25℃, unless otherwise noted.

APD Transient Response



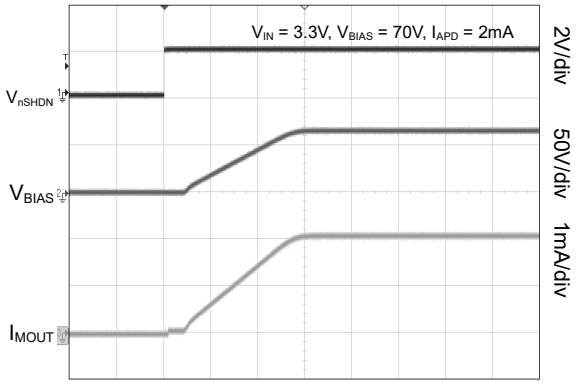
Time (1ms/div)

APD Transient Response



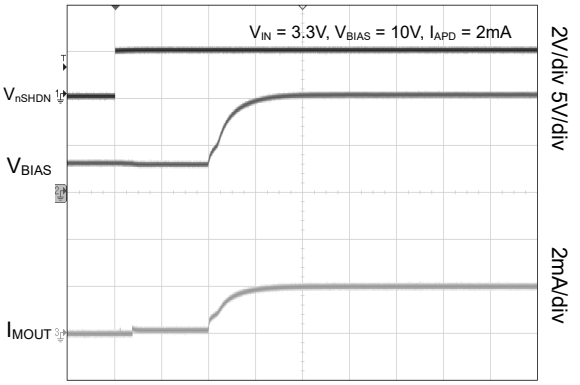
Time (50ns/div)

Startup Delay



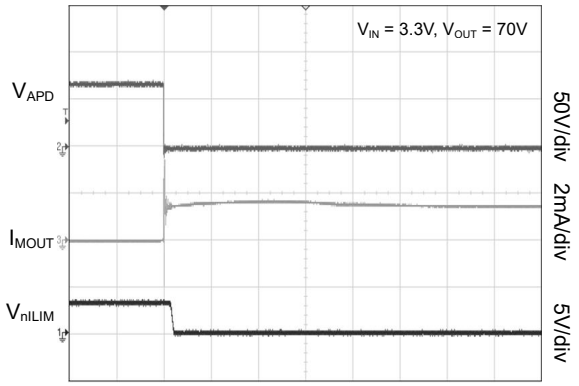
Time (2ms/div)

Startup Delay



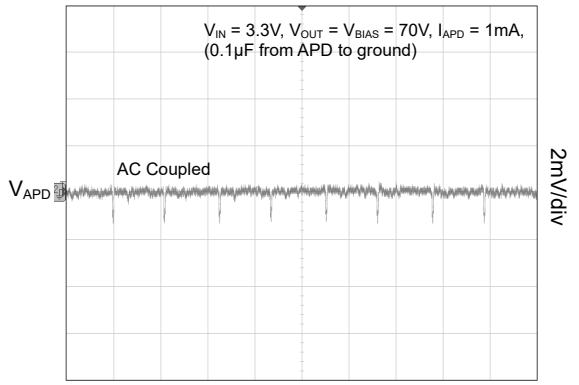
Time (500μs/div)

Short-Circuit Response



Time (2μs/div)

APD Output Ripple Voltage

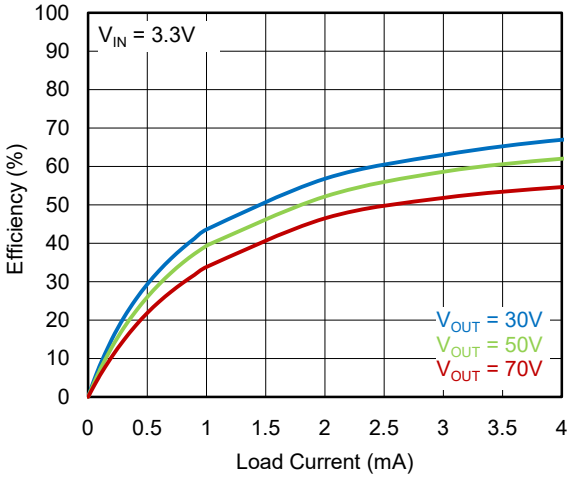


Time (1μs/div)

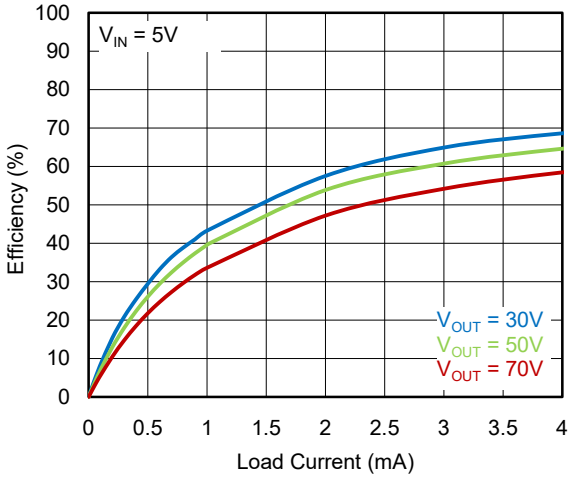
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.3V, V_{OUT} = 70V, T_A = +25℃, unless otherwise noted.

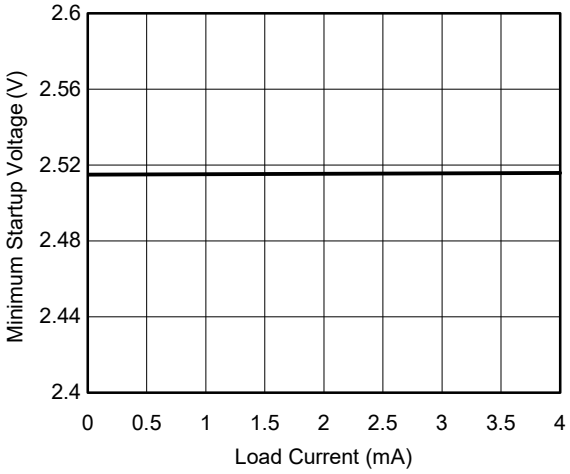
Efficiency vs. Load Current



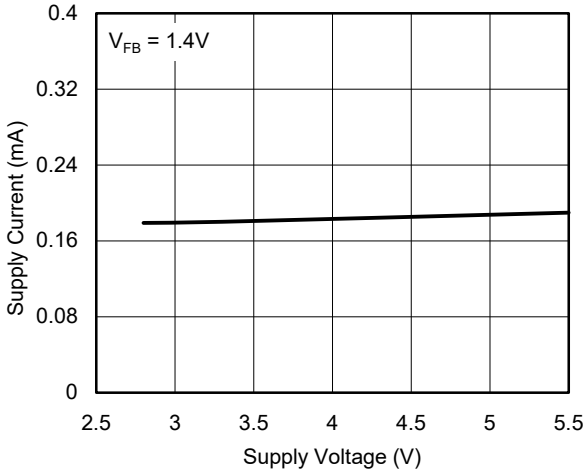
Efficiency vs. Load Current



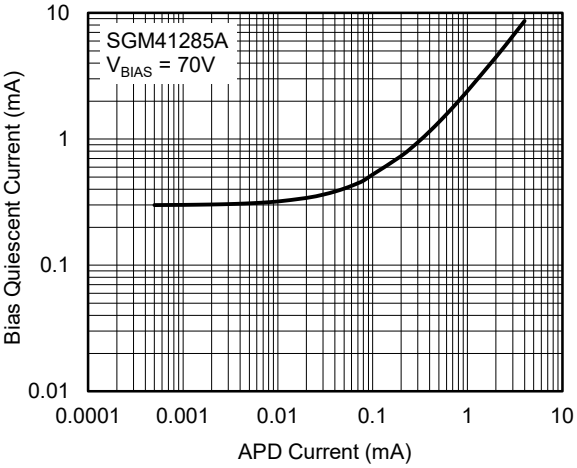
Minimum Startup Voltage vs. Load Current



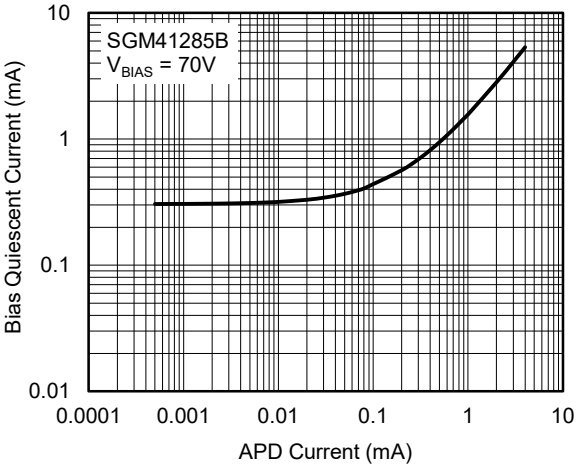
Supply Current vs. Supply Voltage



Bias Quiescent Current vs. APD Current



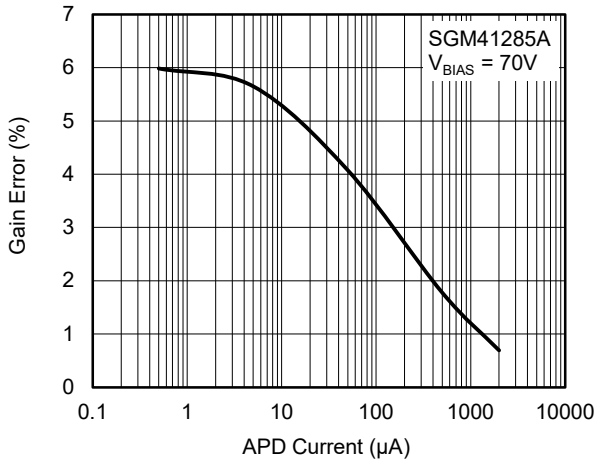
Bias Quiescent Current vs. APD Current



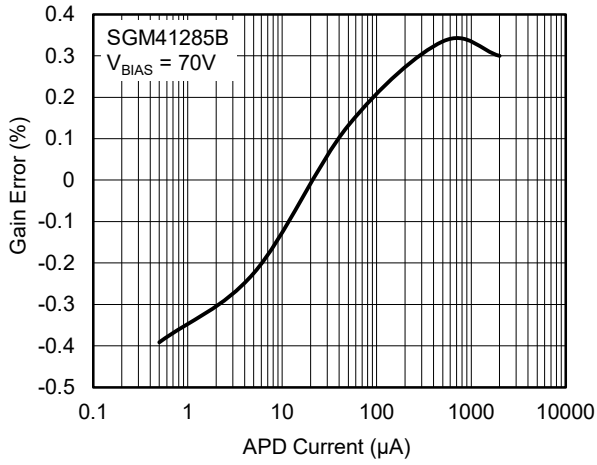
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.3V, V_{OUT} = 70V, T_A = +25℃, unless otherwise noted.

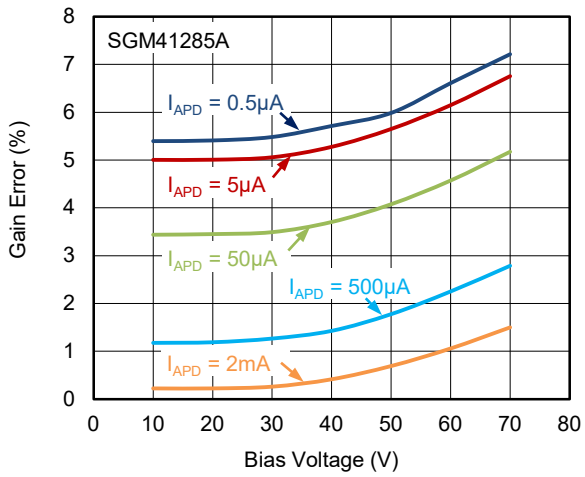
Gain Error vs. APD Current



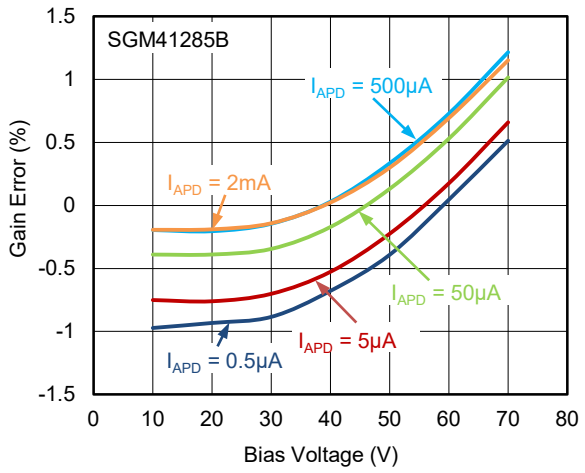
Gain Error vs. APD Current



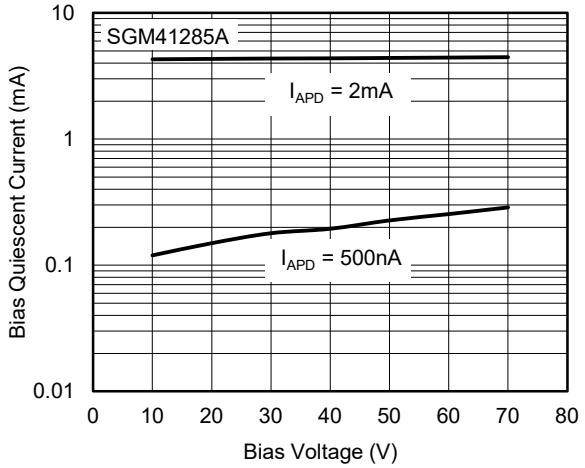
Gain Error vs. Bias Voltage



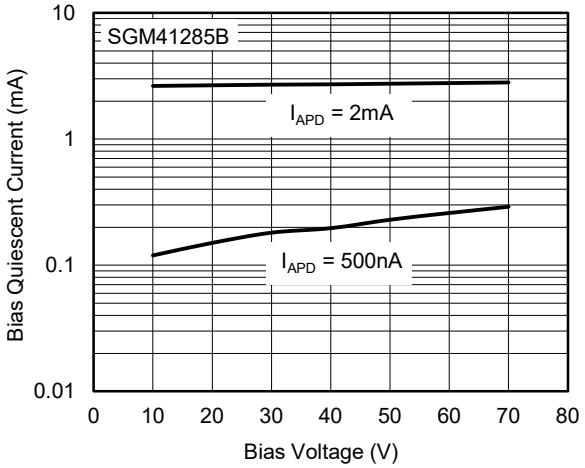
Gain Error vs. Bias Voltage



Bias Quiescent Current vs. Bias Voltage



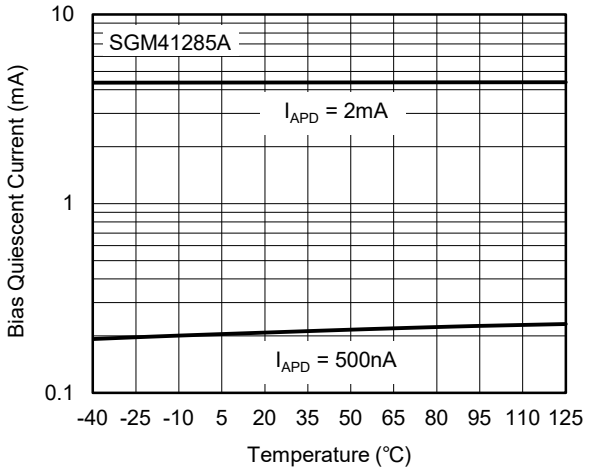
Bias Quiescent Current vs. Bias Voltage



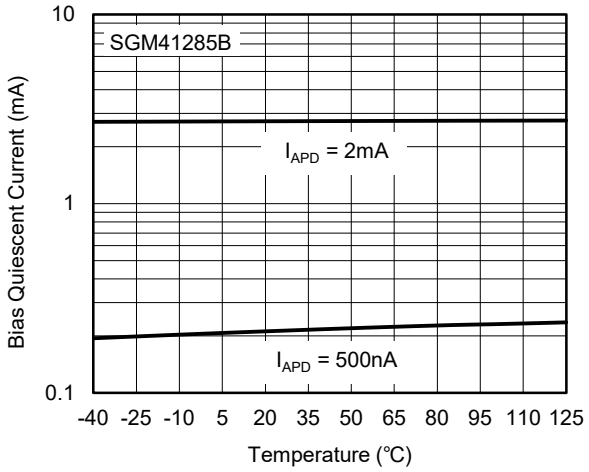
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.3V, V_{OUT} = 70V, T_A = +25℃, unless otherwise noted.

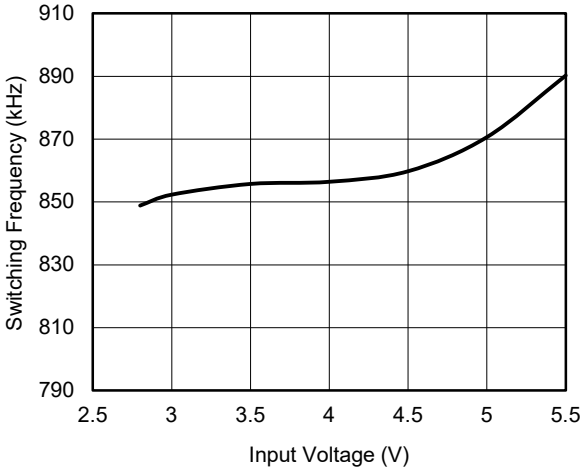
Bias Quiescent Current vs. Temperature



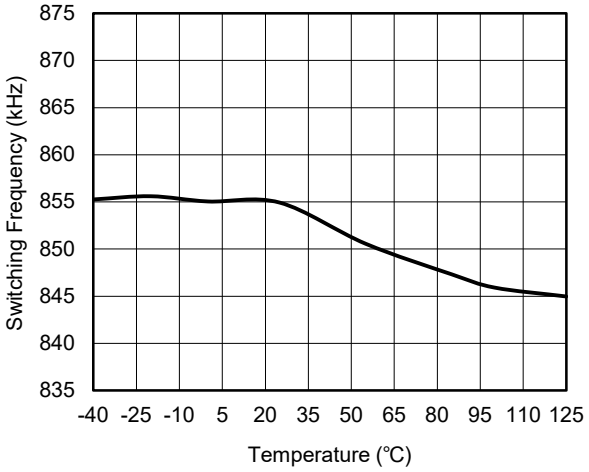
Bias Quiescent Current vs. Temperature



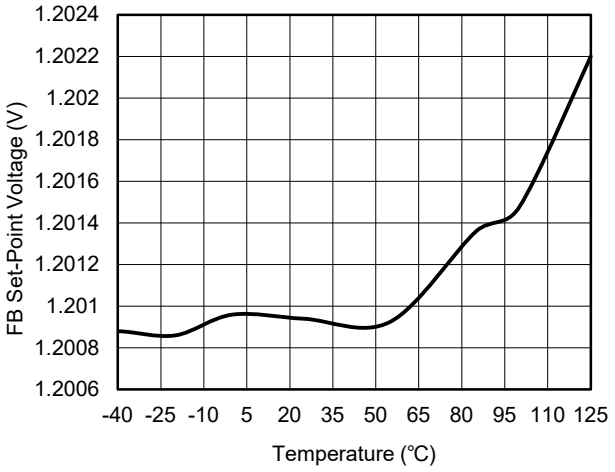
Switching Frequency vs. Input Voltage



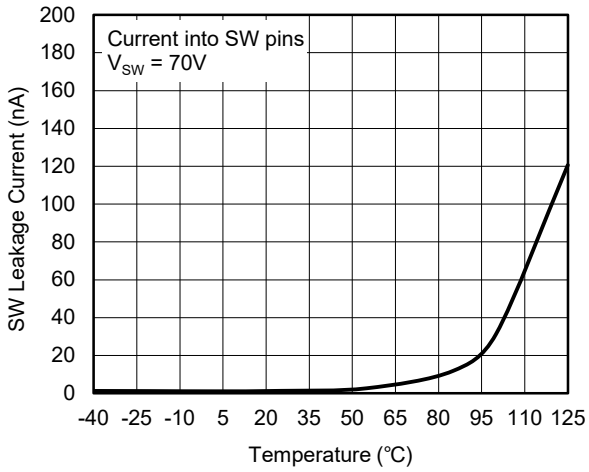
Switching Frequency vs. Temperature



FB Set-Point Voltage vs. Temperature

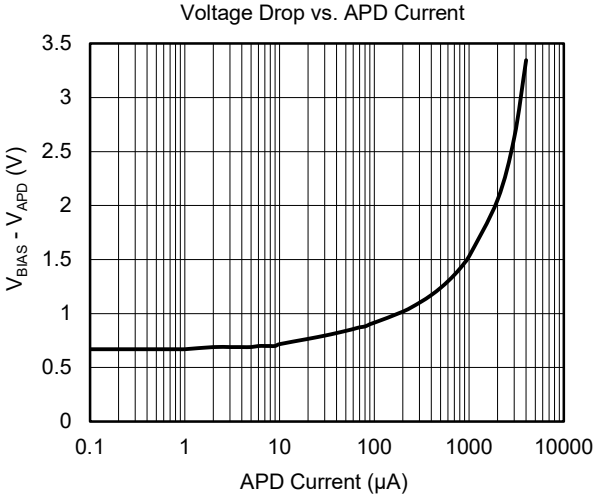


SW Leakage Current vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.3V, V_{OUT} = 70V, T_A = +25℃, unless otherwise noted.



TYPICAL APPLICATION

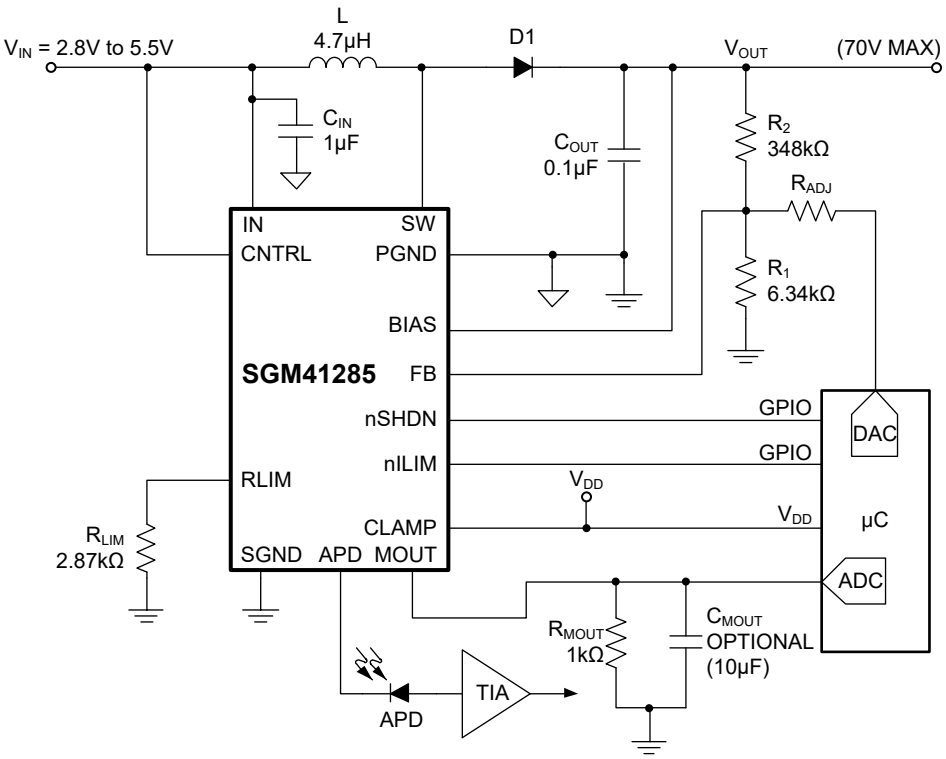


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

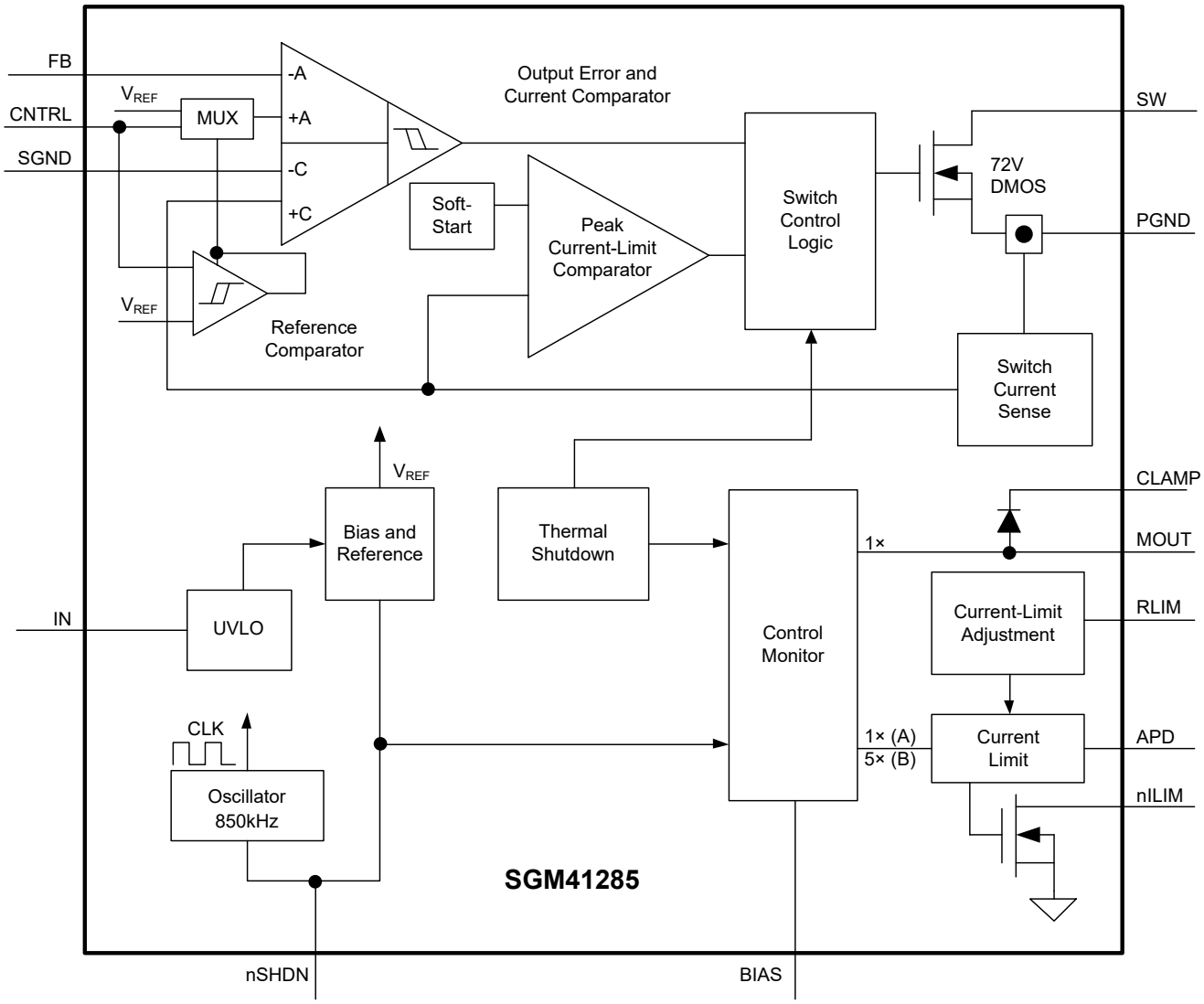


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM41285 constant frequency, current-mode, PWM boost converter is intended for low voltage systems that require a locally generated high voltage. This device is capable of generating a low noise, high output voltage required for PIN and varactor diode biasing. The SGM41285 operates from 2.8V to 5.5V.

The SGM41285 operates in discontinuous mode in order to reduce the switching noise caused by reverse recovery charge of the rectifier diode and eliminates the need for external compensation components. Other continuous-mode boost converters generate large voltage spikes at the output when the SW switch turns on because there is a conduction path between the output, diode, and switch to ground during the time needed for the diode to turn off and reverse its bias voltage. The constant frequency PWM architecture generates an output voltage ripple that is easy to filter. A 72V lateral DMOS device used as the internal power switch is ideal for boost converters with output voltages up to 70V.

The SGM41285 includes a versatile current monitor intended for monitoring the APD, PIN, or varactor diode DC current in fiber and other applications. The SGM41285 features more than three decades of dynamic current ranging from 500nA to 4mA and provides an output current accurately proportional to the APD current at MOUT. The SGM41285 also features a shutdown logic input to disable the device and reduce its standby current to 1μA (MAX).

SGM41285 operates in PWM mode using a fixed frequency, current-mode operation. The current-mode frequency loop regulates the peak inductor current as a function of the output voltage error signal.

The current-mode PWM controller is intended for DCM operation. No internal slope compensation is added to the current signal.

Current Limit

The current limit of the current monitor is programmable from 1mA to 4.5mA (TYP). Connect RLIM pin to SGND to get a default current-limit threshold of 4.5mA or connect a resistor from RLIM pin to SGND to program the current-limit threshold below the default setting of 4.5mA. Calculate the value of the external resistor, R_{LIM}, for a given current limit, I_{LIM}, using the following equation:

$$R_{LIM}\ [k\Omega] = \left[\left(\frac{1.20V}{I_{LIM}\ [mA]}\right) \times 10 - 2.67k\Omega\right] \quad (1)$$

Clamping the Monitor Output Voltage (MOUT)

CLAMP provides a means for diode clamping the voltage at MOUT; thus, V_{MOUT} is limited to (V_{CLAMP} + 0.9V). CLAMP pin can be connected to an external supply. Leave CLAMP unconnected if voltage clamping is not required.

Shutdown

The SGM41285 features an active-low shutdown input (nSHDN). Pull nSHDN low or leave it unconnected to enter shutdown. During shutdown, the supply current drops to less than 1μA when input voltage is lower than 5.0V, and the shutdown current may rise to about 50μA when input voltage is large than 5.0V. The output remains connected to the input through the inductor and output rectifier, holding the output voltage to one diode drop below IN when the SGM41285 is in shutdown. Connect nSHDN pin to IN for always-on operation.

Adjusting the Feedback Set-Point/ Reference Voltage

Apply a voltage to the CNTRL input to set the feedback set-point reference voltage, V_{REF} (see the Functional Diagram). For V_{CNTRL} > 1.3V, the internal 1.20V (TYP) reference voltage is used as the feedback set point and for V_{CNTRL} < 1.2V, the CNTRL voltage is used as the reference voltage (V_{FB} set equal to V_{CNTRL}).

DETAILED DESCRIPTION (continued)

Setting the Output Voltage

Set the SGM41285 output voltage by connecting a resistive divider from the output to FB to SGND (Figure 3). Select R_1 (FB to SGND resistor) between 5kΩ and 10kΩ. Calculate R_2 (V_{OUT} to FB resistor) using the following equation:

$$R_2 = R_1 \times \left[\left(\frac{V_{OUT}}{V_{REF}}\right) - 1\right] \quad (2)$$

where V_{OUT} can range from (V_{IN} + 5V) to 70V. Apply a voltage to the CNTRL input to set the feedback set-point reference voltage, V_{REF} (see the Functional Block Diagram).

For V_{CNTRL} > 1.3V, the internal 1.20V (TYP) reference voltage is used as the feedback set point and for V_{CNTRL} < 1.2V, $V_{FB} = V_{CNTRL}$. See the Adjusting the Feedback Set-Point/Reference Voltage section for more information on adjusting the feedback reference voltage, V_{REF}.

Determining Peak Inductor Current

If the boost converter remains in the discontinuous mode of operation, then the approximate peak inductor current, I_{LPEAK} (in A), is represented by the formula below:

$$I_{LPEAK} = \sqrt{\frac{2 \times t_S \times \left(V_{OUT} - V_{IN\_MIN}\right) \times I_{OUT\_MAX}}{\eta \times L}} \quad (3)$$

where t_S is the switching period in μs, V_{OUT} is the output voltage in volts, V_{IN_MIN} is the minimum input voltage in volts, I_{OUT_MAX} is the maximum output current in amps, L is the inductor value in μH, and η is the efficiency of the boost converter.

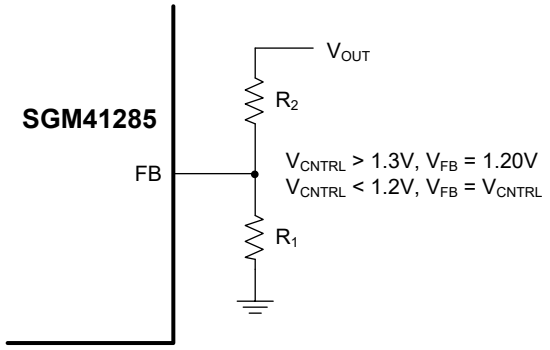


Figure 3. Adjustable Output Voltage

Determining the Inductor Value

Three key inductor parameters must be specified for operation with the SGM41285: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR). In general, the inductor should have a saturation current rating greater than the maximum peak switch current-limit value (I_{LIM_SW} = 1.1A). DCR should be low for reasonable efficiency.

Use the following formula to calculate the lower bound of the inductor value at different output voltages and output currents. This is the minimum inductance value for discontinuous mode operation for supplying full 300mW of output power:

$$I_{MIN}\ [\mu H] = \frac{2 \times t_S \times I_{OUT} \times \left(V_{OUT} - V_{IN\_MIN}\right)}{\eta \times I_{LIM\_SW}^2} \quad (4)$$

where V_{IN_MIN}, V_{OUT} (both in volts), and I_{OUT} (in amps) are typical values (so that efficiency is optimum for typical conditions), t_S (in μs) is the period, η is the efficiency, and I_{LIM_SW} is the peak switch current in amps (see the Electrical Characteristics table).

Calculate the optimum value of L ($L_{OPTIMUM}$) to ensure the full output power without reaching the boundary between continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM) using the following formula:

$$L_{OPTIMUM}\ [\mu H] = \frac{L_{MAX}\ [\mu H]}{2.25} \quad (5)$$

where:

$$I_{MAX}\ [\mu H] = \frac{V_{IN\_MIN}^2 \times \left(V_{OUT} - V_{IN\_MAX}\right) \times t_S \times \eta}{2 \times I_{OUT} \times V_{OUT}^2} \quad (6)$$

For a design in which V_{IN} = 3.3V, V_{OUT} = 70V, I_{OUT} = 3mA, η = 45%, I_{LIM_SW} = 1.1A, and t_S = 1.17μs: L_{MAX} = 13μH and L_{MIN} = 0.9μH.

For a worse-case scenario in which V_{IN} = 2.8V, V_{OUT} = 70V, I_{OUT} = 4mA, η = 43%, I_{LIM_SW} = 1.1A, and t_S = 1.17μs: L_{MAX} = 7μH and L_{MIN} = 1.2μH.

The choice of 4.7μH is reasonable given the worst-case scenario above. In general, the higher the inductance, the lower the switching noise. Load regulation is also better with higher inductance.

DETAILED DESCRIPTION (continued)

Diode Selection

The SGM41285's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward-voltage drop. Ensure that the diode's peak current rating is greater than the peak inductor current. Also, the diode breakdown voltage must be greater than V_{OUT}.

Output Filter Capacitor Selection

For most applications, use a small output capacitor of 0.1μF or greater. To achieve low output ripple, a capacitor with low ESR, low ESL, and high capacitance value should be selected. If tantalum or electrolytic capacitors are used to achieve high capacitance values, always add a smaller ceramic capacitor in parallel to bypass the high-frequency components of the diode current. The higher ESR and ESL of electrolytic capacitors increase the output ripple and peak-to-peak transient voltage. Assuming the contribution from the ESR and capacitor discharge equals 50% (proportions may vary), calculate the output capacitance and ESR required for a specified ripple using the following equations:

$$C_{OUT}\ [\mu F] = \frac{I_{OUT}}{0.5 \times \Delta V_{OUT}} \left[t_S - \frac{I_{PEAK} \times L_{OPTIMUM}}{V_{OUT} - V_{IN\_MIN}} \right] \quad (7)$$

$$ESR\ [m\Omega] = \frac{0.5 \times \Delta V_{OUT}}{I_{OUT}} \quad (8)$$

For very-low-output-ripple applications, the output of the boost converter can be followed by an RC filter to further reduce the ripple. Figure 4 shows a 100Ω, 0.1μF (R_F, C_F) filter used to reduce the switching output ripple. The output voltage regulation resistive divider must remain connected to the diode/output capacitor node.

Use X7R ceramic capacitors for more stability over the full temperature range.

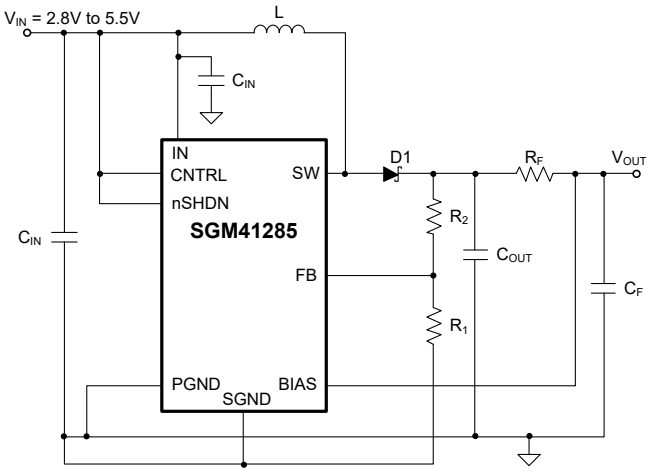


Figure 4. Typical Operating Circuit with RC Filter

Input Capacitor Selection

Bypass IN to PGND with a 1μF (MIN) ceramic capacitor. Depending on the supply source impedance, higher values may be needed. Make sure that the input capacitors are close enough to the IC to provide adequate decoupling at IN as well. If the layout cannot achieve this, add another 0.1μF ceramic capacitor between IN and PGND in the immediate vicinity of the IC. Bulk aluminum electrolytic capacitors may be needed to avoid chattering at low-input voltage. In case of aluminum electrolytic capacitors, calculate the capacitor value and ESR of the input capacitor using the following equations:

$$C_{IN}\ [\mu F] = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN\_MIN} \times 0.5 \times \Delta V_{IN}} \left[t_S - \frac{I_{PEAK} \times L_{OPTIMUM} \times V_{OUT}}{V_{IN\_MIN}\left(V_{OUT} - V_{IN\_MIN}\right)} \right] \quad (9)$$

$$ESR\ [m\Omega] = \frac{0.5 \times \Delta V_{IN} \times \eta \times V_{IN\_MIN}}{V_{OUT} \times I_{OUT}} \quad (10)$$

APPLICATION INFORMATION

When using the SGM41285 to monitor APD or PIN photodiode currents in fiber applications, several issues must be addressed. In applications where the photodiode must be fully depleted, keep track of voltages budgeted for each component with respect to the available supply voltage(s). The current monitors require as much as 1.9V between BIAS and APD, which must be considered part of the overall voltage budget.

Additional voltage margin can be created if a negative supply is used in place of a ground connection, as long as the overall voltage drop experienced by the SGM41285 is less than or equal to 70V. For this type of application, the SGM41285 is suggested so the output can be referenced to “true” ground and not the negative supply. The SGM41285’s output current can be referenced as desired with either a resistor to ground or a transimpedance amplifier. Take care to ensure that output voltage excursions do not interfere with the required margin between BIAS and MOUT. In many fiber applications, MOUT is connected directly to an ADC that operates from a supply voltage that is less than the voltage at BIAS. Connecting the SGM41285’s clamping diode output, CLAMP, to the ADC power supply helps avoid damage to the ADC. Without this protection, voltages can develop at MOUT that might destroy the ADC.

This protection is less critical when MOUT is connected directly to subsequent transimpedance amplifiers (linear or logarithmic) that have low-impedance, near-ground referenced inputs. If a transimpedance amp is used on the low side of the photodiode, its voltage drop must also be considered. Leakage from the clamping diode is most often insignificant over nominal operating conditions, but grows with temperature.

To maintain low levels of wideband noise, lowpass filtering the output signal is suggested in applications where only DC measurements are required. Connect the filter capacitor at MOUT. Determining the required filtering components is straightforward, as the SGM41285 exhibits a very high output impedance of 5GΩ.

In some applications where pilot tones are used to identify specific fiber channels, higher bandwidths are desired at MOUT to detect these tones. Consider the minimum and maximum currents to be detected, then consult the frequency response and noise typical operating curves. If the minimum current is too small, insufficient bandwidth could result, while too high a current could result in excessive noise across the desired bandwidth.

Layout Considerations

Careful PCB layout is critical to achieve low switching losses and clean and stable operation. Protect sensitive analog grounds by using a star ground configuration. Connect SGND and PGND together close to the device at the return terminal of the output bypass capacitor. Do not connect them together anywhere else. Keep all PCB traces as short as possible to reduce stray capacitance, trace resistance, and radiated noise. Ensure that the feedback connection to FB is short and direct. Route high-speed switching nodes away from the sensitive analog areas. Use an internal PCB layer for SGND as an EMI shield to keep radiated noise away from the device, feedback dividers, and analog bypass capacitors.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JANUARY 2019 – REV.A to REV.A.1

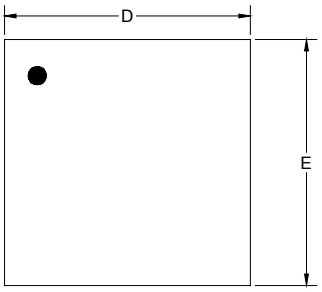
Updated operating temperature range and Electrical Characteristics	4-5

Changes from Original (DECEMBER 2018) to REV.A

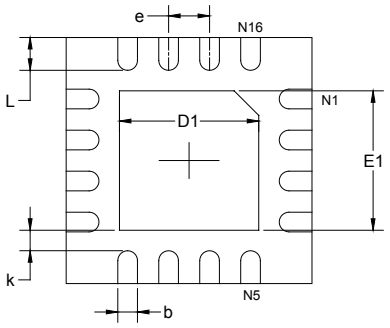
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

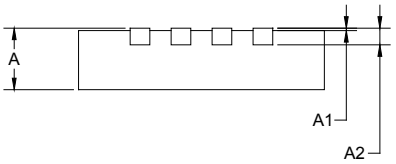
TQFN-3×3-16L



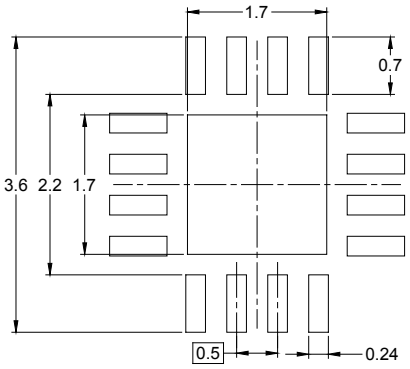
TOP VIEW



BOTTOM VIEW



SIDE VIEW

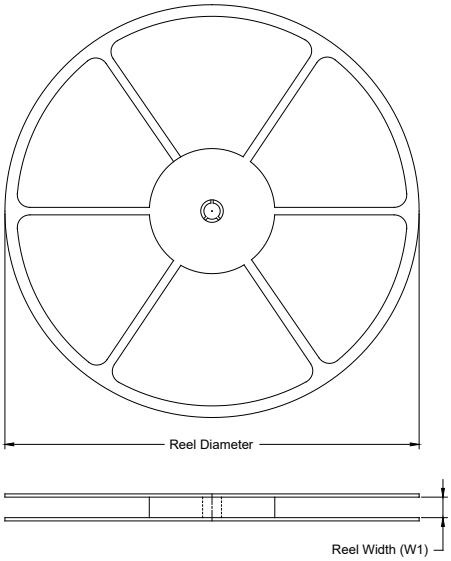


RECOMMENDED LAND PATTERN (Unit: mm)

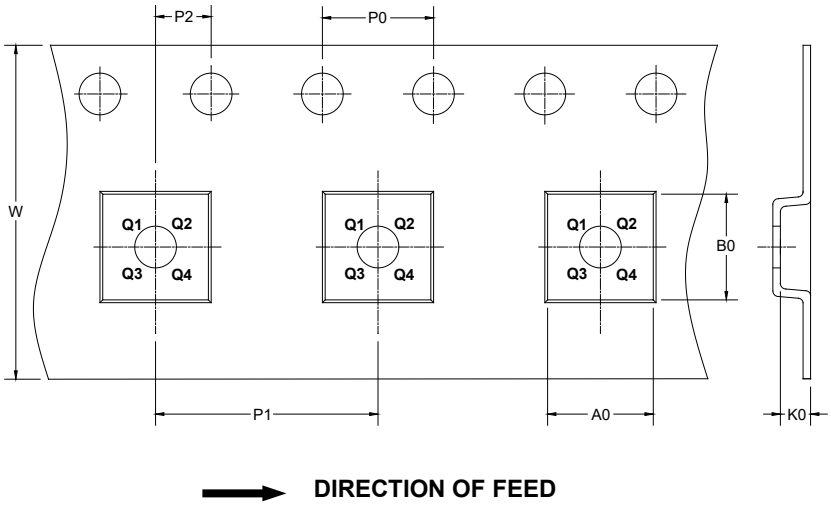
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



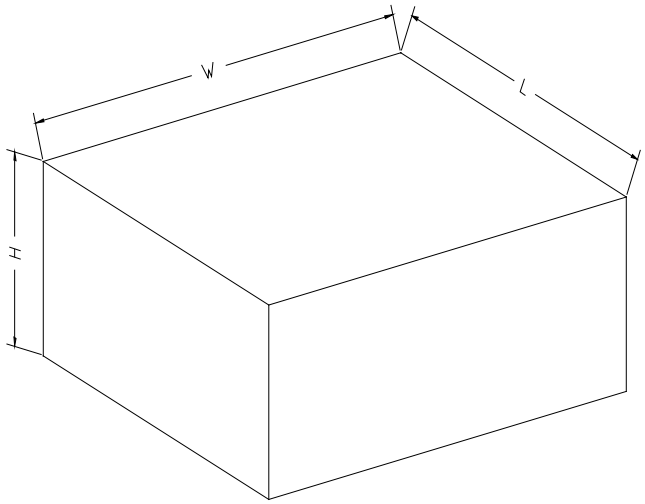
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×3-16L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002