Green-Mode PFC / Flyback-PWM Controller **SG6902**

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FEATURES

- Green-mode PFC and PWM operation
- No switching of PFC at light loads saves power
- Low start-up and operating current
- Innovative switching-charge multiplier-divider
- Multi-vector control for improved PFC output transient response
- Interleaved PFC/PWM switching
- Programmable two-level PFC output voltage
- Average-current-mode control for PFC
- Cycle-by-cycle current limiting for PFC/PWM
- PFC over-voltage and under-voltage protections
- PFC and PWM feedback open-loop protection
- Brownout protection
- Over-temperature protection

APPLICATIONS

- Switching Power Supplies with Active PFC
- High-Power Adaptors

DESCRIPTION

The highly integrated SG6902 is designed for power supplies with boost PFC and Flyback PWM. It requires very few external components to achieve green-mode operation and versatile protections. It is available in a 20-pin SOP package.

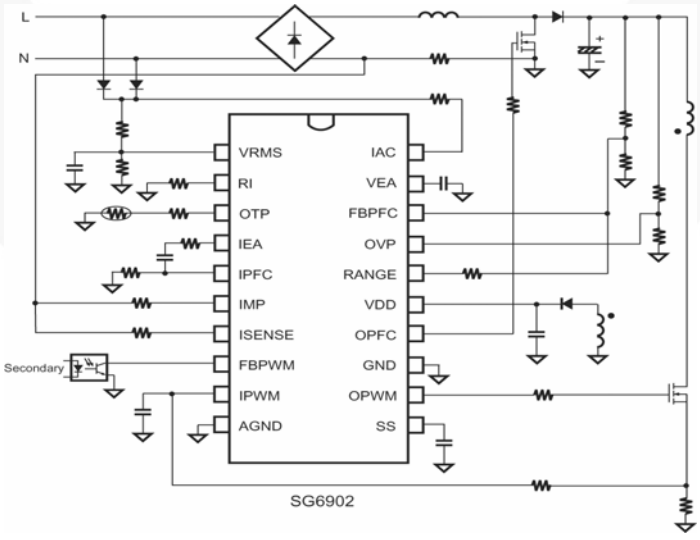
The patented interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light loads, the switching frequency is continuously decreased to reduce power consumption. If output loading is further reduced, the PFC stage is turned off to further reduce power consumption.

For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6902 shuts off PFC to prevent extra-high voltage on output. Programmable two-level output voltage control reduces the PFC output voltage at low line input to increase the efficiency of the power supply.

For the flyback PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-conduction-mode operation. Built-in line-voltage compensation maintains a constant output power limit. Hiccup operation during output overloading is also guaranteed.

In addition, SG6902 provides protection functions, such as brownout and RI pin open/short protections.

TYPICAL APPLICATION



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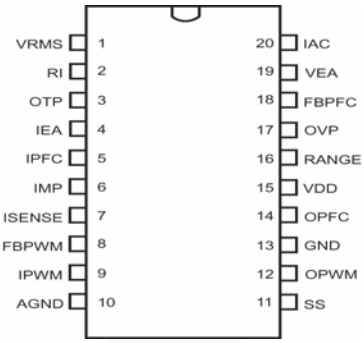
MARKING DIAGRAM

T: S=SOP
P : Z=Lead Free
+ ROHS Compatible
Null=regular package
XXXXXXXX: Wafer Lot
Y: Year; WW: Week
V: Assembly Location

PIN CONFIGURATION



ORDERING INFORMATION

Part Number	Pb-Free	Package
SG6902SZ		20-pin SOP

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PIN DESCIRPTIONS

Name	Pin No.	Type	Function
VRMS	1	Line Voltage Detection	Line voltage detection. The pin is used for PFC multiplier, RANGE control of PFC output voltage, and brownout protection. For brownout protection, the controller is disabled after a delay time when the V_{RMS} voltage drops below a threshold.
RI	2	Oscillator Setting	Reference setting. One resistor connected between RI and AGND determines the switching frequency. The switching frequency is equal to [1560 / RI] kHz, where RI is in kΩ. For example, if R_I is 24kΩ, the switching frequency is 65kHz.
OTP	3	Over-Temperature Protection	This pin supplies an over-temperature protection signal. A constant current is output from this pin. An external NTC thermistor must be connected from this pin to ground. The impedance of the NTC thermistor decreases whenever the temperature increases. Once the voltage of the OTP pin drops below the OTP threshold, the SG6902 is disabled.
IEA	4	Output for PFC Current Amplifier	This is the output of the PFC current error amplifier. The signal from this pin is compared with an internal sawtooth and determines the pulse width for PFC gate drive.
IPFC	5	Inverting Input for PFC Current Amplifier	The inverting input of the PFC current error amplifier. Proper external compensation circuits result in excellent input power factor via average-current-mode control.
IMP	6	Non-Inverting Input for PFC Current Amplifier	The non-inverting input of the PFC current amplifier and also the output of multiplier. Proper external compensation circuits will result in excellent input power factor via average-current-mode control.
ISENSE	7	Peak Current Limit Setting for PFC	The peak-current setting for PFC.
FBPWM	8	PWM Feedback Input	The control input for voltage-loop feedback of PWM stage. It is internally pulled high through a resistor. An external opto-coupler from secondary feedback circuit is usually connected to this pin.
IPWM	9	PWM Current Sense	The current-sense input for the flyback PWM. Via a current sense resistor, this pin provides the control input for peak-current-mode control and cycle-by-cycle current limiting.
AGND	10	Ground	Signal ground.
SS	11	PWM Soft-Start	During start-up, the SS pin charges an external capacitor with a 50μA (R_I=24kΩ) constant-current source. The voltage on FBPWM is clamped by SS during start-up. In the event of a protection condition occurring and/or PWM being disabled, the SS pin quickly discharges.
OPWM	12	PWM Gate Drive	The totem-pole output drive for the flyback PWM MOSFET. This pin is internally clamped under 18V to protect the MOSFET.
GND	13	Ground	Power ground.
OPFC	14	PFC Gate Drive	The totem-pole output drive for the PFC MOSFET. This pin is internally clamped under 18V to protect the MOSFET.
VDD	15	Supply	The power supply pin.
RANGE	16	PFC Output Voltage Control	Two-level output voltage setting for PFC. The PFC output voltage at low line can be reduced to improve efficiency. The RANGE pin is of high impedance while the V_{RMS} voltage is lower than a threshold.
OVP	17	PFC Over-Voltage Input	The PFC stage over-voltage input. The comparator disables the PFC output driver if the voltage at this input exceeds a threshold. This pin can be connected to FBPFC or it can be connected to the PFC boost output through a divider network.
FBPFC	18	Voltage Feedback Input for PFC	The feedback input for PFC voltage loop. The inverting input of PFC error amplifier. This pin is connected to the PFC output through a divider network.
VEA	19	Error Amplifier Output for PFC Voltage Feedback Loop	The error amplifier output for PFC voltage feedback loop. A compensation network (usually a capacitor) is connected between this pin and ground. A large capacitor value results in a narrow bandwidth and improves the power factor.
IAC	20	Input AC Current	Before start-up, this input is used to provide start-up current for V_{DD}. For normal operation, this input is used to provide current reference for the multiplier.

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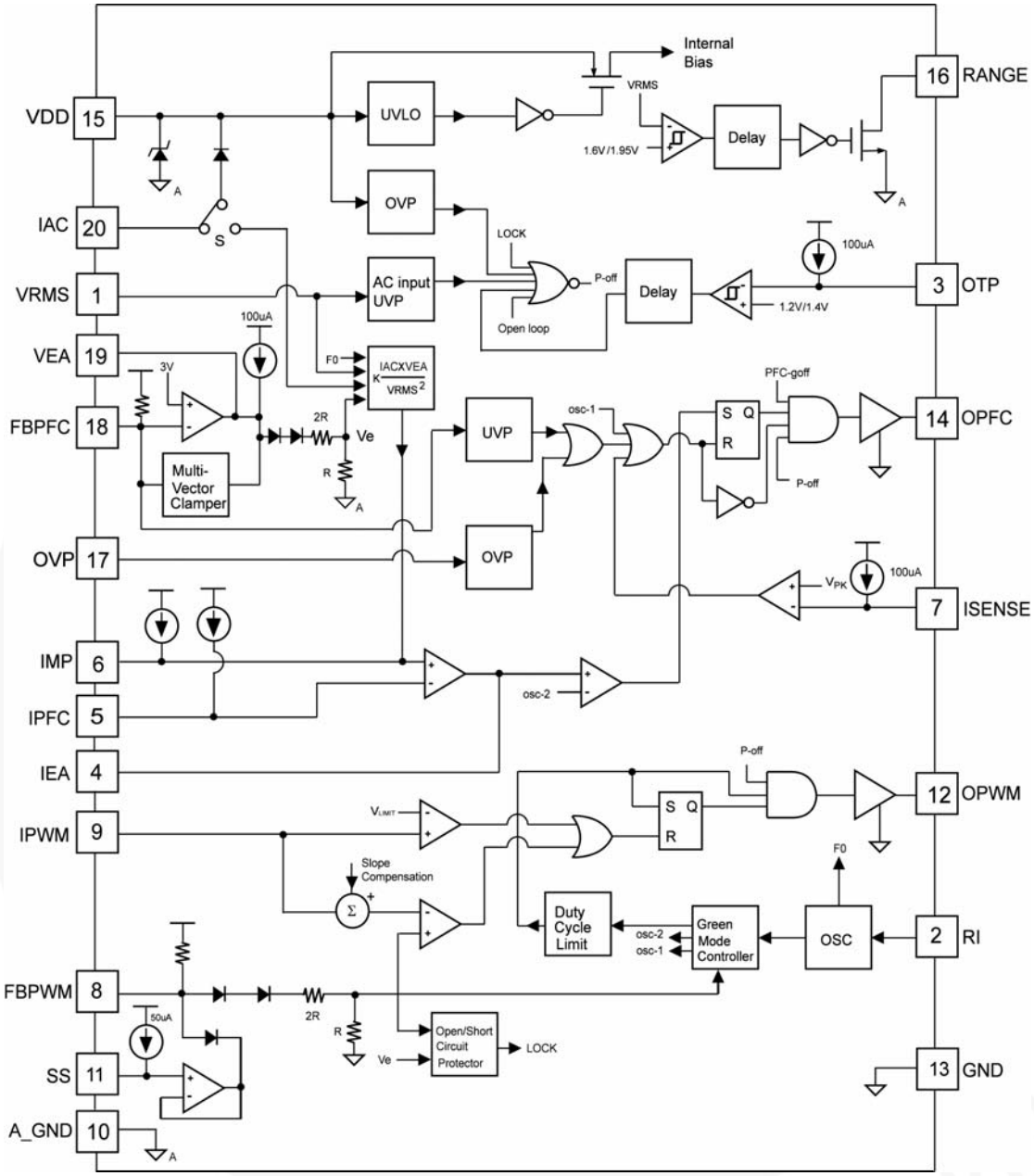
BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
V_{DD}	DC Supply Voltage*	25		V
I_{AC}	Input AC Current	2		mA
V_{HIGH}	OPWM, OPFC, IAC	-0.3 to +25.0		V
V_{LOW}	Others	-0.3 to +7.0		V
P_D	Power Dissipation at T_A < 50°C	SOP	1.15	W
T_J	Operating Junction Temperature	-40 to +125		°C
T_{STG}	Storage Temperature Range	-55 to +150		°C
$R_{\theta JC}$	Thermal Resistance (Junction-to-Case)	SOP	23.64	°C/W
T_L	Lead Temperature (Wave Soldering or Infrared, 10 Seconds)	260		°C
ESD	Electrostatic Discharge Capability, Human Body Model	4.5		KV
	Electrostatic Discharge Capability y, Machine Model	250		V

*All voltage values, except differential voltages, are given with respect to GND pin.

*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
T_A	Operating Ambient Temperature*	-30 to +85	°C

*For proper operation.

ELECTRICAL CHARACTERISTICS

V_{DD}=15V, T_A=25°C unless otherwise noted.

V_{DD} Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD-OP}	Continuously Operating Voltage				20	V
I_{DD-ST}	Start-up Current	V_{TH-ON} –0.16V		10	25	µA
I_{DD-OP}	Operating Current	OPFC, OPWM Open, R_i=24kΩ		6	10	mA
V_{TH-ON}	Start Threshold Voltage		15	16	17	V
V_{DD-MIN}	Minimum Operating Voltage		9	10	11	V
V_{DD-OVP}	V_{DD} OVP Threshold		23.5	24.5	25.5	V
$T_{VDD-OVP}$	Debounce Time of V_{DD} OVP	R_i=24kΩ	8		25	µs
$V_{DD-TH-G}$	V_{DD} Low-Threshold Voltage to Exit Green-off Mode		V_{DD-MIN} +0.9	V_{DD-MIN} +1.5	V_{DD-MIN} +2.1	V

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Oscillator & Green-Mode Operation

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RI}	RI Voltage		1.176	1.200	1.224	V
F_{OSC}	PWM Frequency	R_I=24kΩ	62	65	68	KHz
$F_{OSC-MINFREQ}$	Minimum Frequency in Green Mode	R_I=24kΩ	18.0	20.0	22.5	KHz
RI	RI Pin Resistance Range		15		47	KΩ
RI_{OPEN}	RI Pin Open Protection If RI> RI_{open} , SG6902 Turns Off			200		KΩ
RI_{SHORT}	RI Pin Short Protection If RI< RI_{short} , SG6902 Turns Off			2		KΩ

VRMS for UVP and RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{RMS-UVP-1}$	RMS AC Voltage Under-Voltage Protection Threshold (with T_{UVP} Delay)		0.75	0.80	0.85	V
$V_{RMS-UVP-2}$	Recovery Level on VRMS		$V_{RMS-UVP-1}$ +0.16V	$V_{RMS-UVP-1}$ +0.18V	$V_{RMS-UVP-1}$ +0.2V	V
T_{D-PWM}	When UVP Occurs, Interval from PFC Off to PWM Off	R_I=24kΩ	$T_{UVP-Min}$+ 9		$T_{UVP-Min}$+ 14	ms
T_{UVP}	Under-Voltage Protection Delay Time*	R_I=24kΩ	150	195	240	ms
V_{RMS-H}	High V_{RMS} Threshold for RANGE Comparator		1.90	1.95	2.00	V
V_{RMS-L}	Low V_{RMS} Threshold for RANGE Comparator		1.55	1.60	1.65	V
T_{RANGE}	Range Enable Delay Time	R_I=24kΩ	145	170	200	ms
V_{OL}	Output Low Voltage of RANGE Pin	I_o=1mA			0.5	V
I_{OH}	Output High Leakage Current of RANGE Pin	RANGE=5V			50	nA

* No delay for start-up.

PFC STAGE

Voltage Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{REF}	Reference Voltage		2.95	3.00	3.05	V
Av_{-PFC}*	Open-Loop Gain			60		dB
Z_O*	Output Impedance			110		KΩ
OVP_{PFC}	PFC Over Voltage Protection (OVP Pin)		3.20	3.25	3.30	V
$\triangle OVP_{PFC}$	PFC Feedback Voltage Protection Hysteresis		60	90	120	mV
$T_{OVP-PFC}$	Debounce Time of PFC OVP	R_I=24kΩ	40	70	120	µs
$V_{FBPFC-H}$	Clamp-High Feedback Voltage		3.10	3.15	3.20	V
$G_{FBPFC-H}$*	Clamp-High Gain			0.5		mA/V
$V_{FBPFC-L}$	Clamp-Low Feedback Voltage		2.75	2.85	2.90	V
$G_{FBPFC-L}$*	Clamp-Low Gain			6.5		mA/mV
$I_{FBPFC-L}$	Maximum Source Current		1.5	2.0		mA
$I_{FBPFC-H}$	Maximum Sink Current		70	110		µA
UVP_{FBPFC}	PFC Feedback Under-Voltage Protection		0.35	0.40	0.45	V
V_{FBHIGH}	FB Open Voltage		6	7	8	V
$T_{UVP-PFC}$	Debounce Time of PFC UVP	R_I=24kΩ	40	70	120	µs

* Not tested in production.

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Current Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OFFSET}	Input Offset Voltage			8		mV
A_I [*1]	Open-Loop Gain			60		dB
BW [*1]	Unit Gain Bandwidth			1.5		MHz
CMRR [*1]	Common Mode Rejection Ratio	V_{CM}=0 to +1.5V		70		dB
$V_{OUT-HIGH}$	Output High Voltage		3.2			V
$V_{OUT-LOW}$	Output Low Voltage				0.2	V
I_{MR1}, I_{MR2}	Reference Current Source	R_I=24kΩ (I_{MR}=20+I_{RI}•0.8)	50		70	μA
I_L	Maximum Source Current			3		mA
I_H	Maximum Sink Current			0.25		mA

Peak Current Limit

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_P	Constant Current Output	R_I=24kΩ	90	100	110	μA
V_{PK}	Peak Current Limit Threshold Voltage Cycle-by-Cycle Limit (V_{SENSE} < V_{PK})	V_{RMS}=1.05V	0.15	0.20	0.25	V
		V_{RMS}=3V	0.35	0.40	0.45	V
T_{PD-PFC}	Propagation Delay				200	ns
$T_{BNK-PFC}$	Leading-Edge Blanking Time		270	350	450	ns

Multiplier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AC}	Input AC Current	Multiplier Linear Range	0		360	μA
V_{DROP}	Voltage Drop from the IAC Pin to VDD	I_{AC}=240μA			3.5	V
I_{MO-MAX} [*1]	Maximum Multiplier Current Output	R_I=24 kΩ		250		μA
I_{MO-1}	Multiplier Current Output (Low-line, High-power)	V_{RMS}=1.05V; I_{AC}=90μA; V_{EA}=7.5V; R_I=24kΩ	200	250	280	μA
I_{MO-2}	Multiplier Current Output (High-line, High-power)	V_{RMS}=3V; I_{AC}=264μA; V_{EA}=7.5V; R_I=24kΩ	65	85		μA
V_{IMP}	Voltage of IMP Open		3.4	3.9	4.4	V

PFC Output Driver

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{Z-PFC}	Output Voltage Maximum (Clamp)	V_{DD}=20V		16	18	V
T_{PFC}	Interval OPFC Lags Behind OPWM at Start-up	R_I=24kΩ	9.0	11.5	14.0	ms
V_{OL-PFC}	Output Voltage Low	V_{DD}=15V; I_O=100mA			1.5	V
V_{OH-PFC}	Output Voltage High	V_{DD}=13V; I_O=100mA	8			V
T_{R-PFC}	Rising Time	V_{DD}=15V; C_L=5nF; OPFC=2V to 9V	40	70	120	ns
T_{F-PFC}	Falling Time	V_{DD}=15V; C_L=5nF; OPFC=9V to 2V	40	60	110	ns
$DC_{MAX-PFC}$	Maximum Duty Cycle		93		98	%

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PWM STAGE

FBPWM

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$A_{V\text{-}PWM}$	FB to Current Comparator Attenuation		2.5	3.1	3.5	V/V
Z_{FB}*	Input Impedance		4	5	7	KΩ
I_{FB}	Maximum Source Current		0.8	1.2	1.5	mA
$FB_{OPEN\text{-}LOOP}$	PWM Open-Loop Protection Threshold		4.2	4.5	4.8	V
$T_{OPEN\text{-}PWM}$	PWM Open-Loop Protection Delay Time	R_I=24kΩ	45	56	70	ms
$V_{PFC\text{-}OFF1}$	PFC Off Voltage at FBPWM	RANGE=Ground		V_G+0.2V		V
$V_{PFC\text{-}OFF2}$	PFC Off Voltage at FBPWM	RANGE=Open		V_G+0.2V		V
$T_{PFC\text{-}OFF}$	PFC Off Delay Time	R_I=24kΩ	500	650	800	ms
$V_{PFC\text{-}ON\ 1.6}$	PFC On Voltage at FBPWM	RANGE=Ground V_{RMS}=1.6V		V_G+0.35 V		V
$V_{PFC\text{-}ON\ 2.85}$	PFC On Voltage at FBPWM	RANGE=Ground V_{RMS}=2.85V		V_G+0.35 V		V
$V_{PFC\text{-}ON\ 0.8}$	PFC On Voltage at FBPWM	RANGE=Open V_{RMS}=0.8V		V_G+0.85 V		V
$V_{PFC\text{-}ON\ 1.95}$	PFC On Voltage at FBPWM	RANGE=Open V_{RMS}=1.95V		V_G+0.5V		V
V_N	Frequency Reduction Threshold on FBPWM	RANGE=Ground	1.9	2.1	2.3	V
S_G*1	Green-Mode Modulation Slope		60	75	90	Hz/V
V_G	Voltage on FBPWM at F_S=20KHz		1.35	1.60	1.75	V

* Not tested in production.

PWM-Current Sense

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$T_{PD\text{-}PWM}$	Propagation Delay to Output		60		120	ns
$V_{LIMIT\text{-}1}$	Peak Current Limit Threshold Voltage1	RANGE=Open	0.65	0.70	0.75	V
$V_{LIMIT\text{-}2}$	Peak Current Limit Threshold Voltage2	RANGE=Ground	0.60	0.65	0.70	V
$T_{BNK\text{-}PWM}$	Leading-Edge Blanking Time		270	350	450	ns
$\triangle V_{SLOPE}$	Slope Compensation	$\triangle V_S = \triangle V_{SLOPE}$ x (T_{on}/T) $\triangle V_S$: Compensation Voltage Added to Current Sense	0.45	0.50	0.55	V

PWM Output Driver

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{Z\text{-}PWM}$	Output Voltage Maximum (Clamp)	V_{DD}=20V		16	18	V
$V_{OL\text{-}PWM}$	Output Voltage Low	V_{DD}=15V; I_O=100mA			1.5	V
$V_{OH\text{-}PWM}$	Output Voltage High	V_{DD}=13V; I_O=100mA	8			V
$T_{R\text{-}PWM}$	Rising Time	V_{DD}=15V; C_L=5nF; OPWM=2V to 9V	30	60	120	ns
$T_{F\text{-}PWM}$	Falling Time	V_{DD}=15V; C_L=5nF; OPWM=9V to 2V	30	50	110	ns
$DC_{MAX\text{-}PWM}$	Maximum Duty Cycle		73	78	83	%

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OTP Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{OTP}	OTP Pin Output Current	R_I=24kΩ	90	100	11	μA
$V_{OTP-OFF}$	OTP Threshold Voltage		1.15	1.20	1.25	V
V_{OTP-ON}	Recovery Level on OTP		1.35	1.40	1.45	V
T_{OTP}	OTP Debounce Time	R_I=24kΩ	8		25	μs

Soft-Start Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SS}	Constant Current Output for Soft-Start	R_I=24kΩ	44	50	56	μA
R_D*	Discharge R_{DSON}			470		Ω

* Not tested in production.

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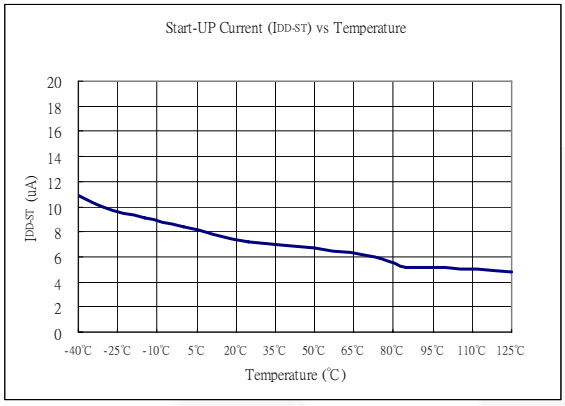
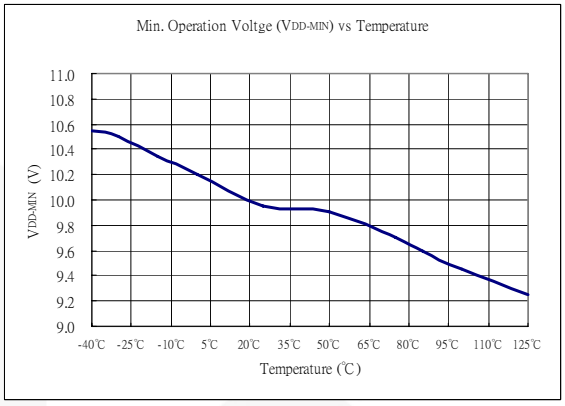
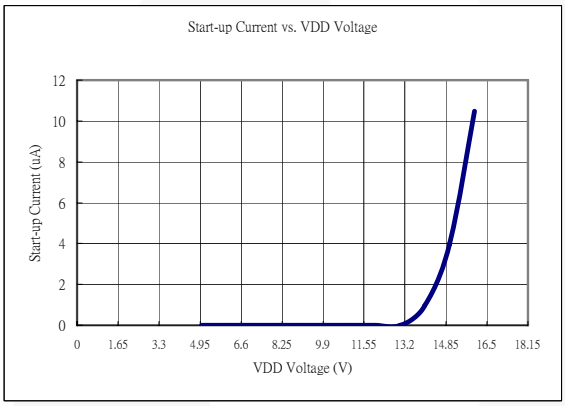
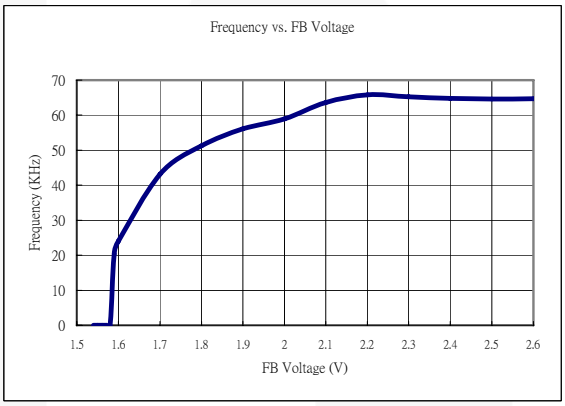
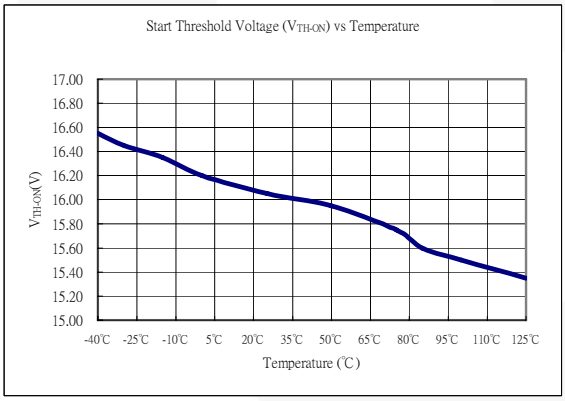
TYPICAL CHARACTERISTICS

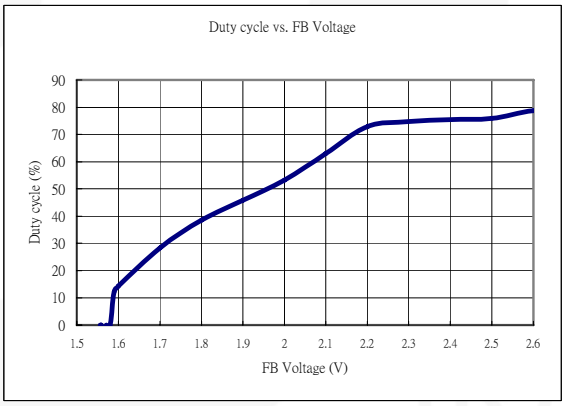












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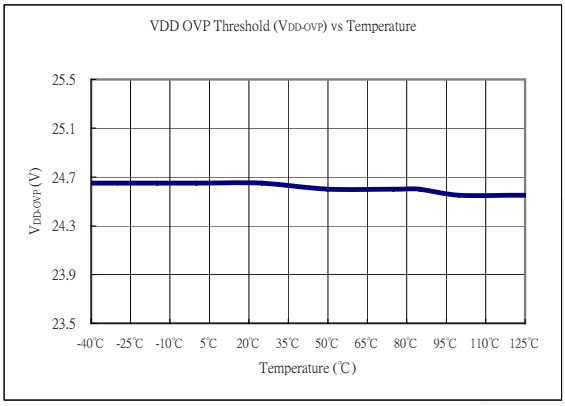

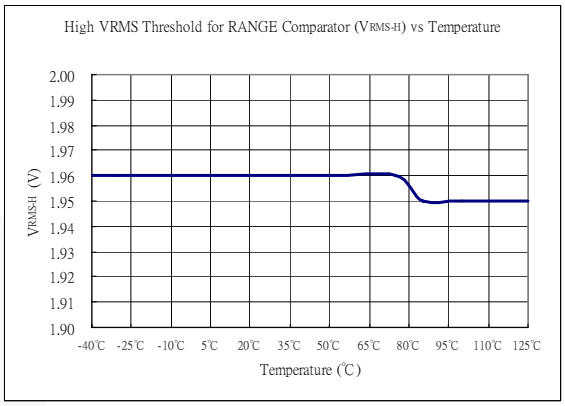

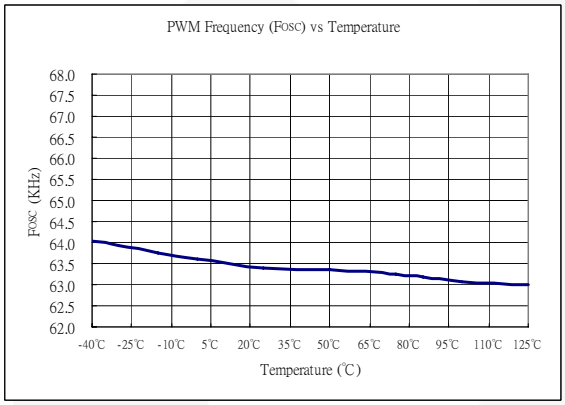

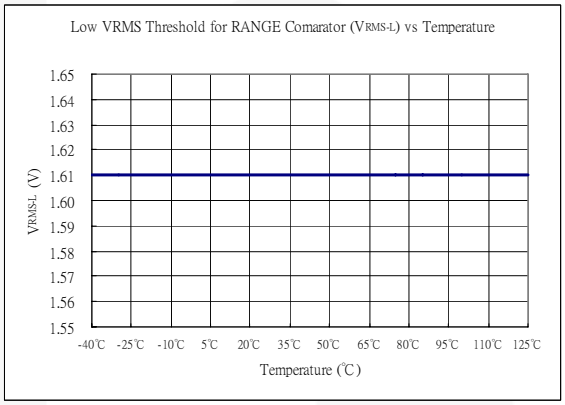

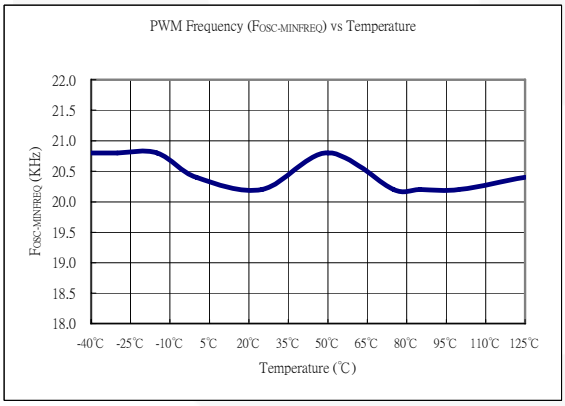

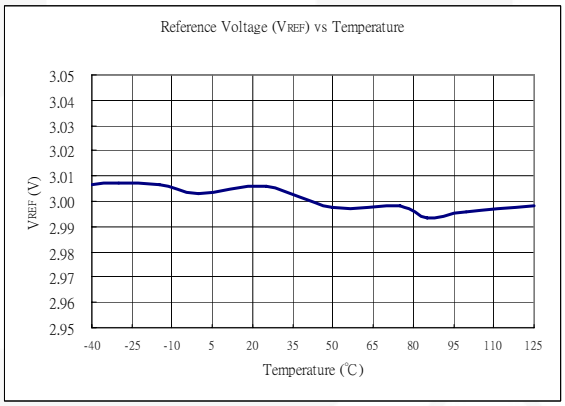

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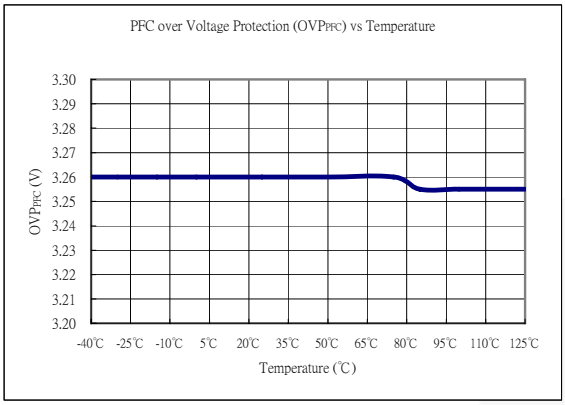

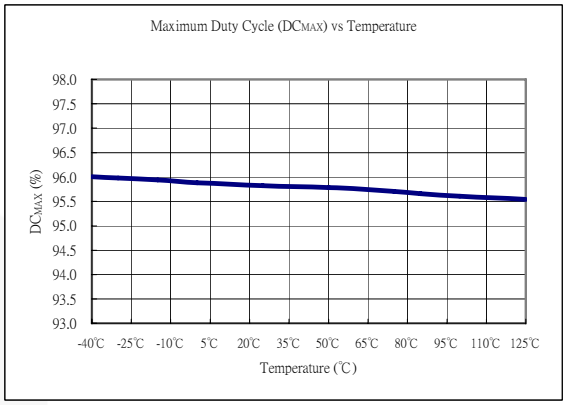

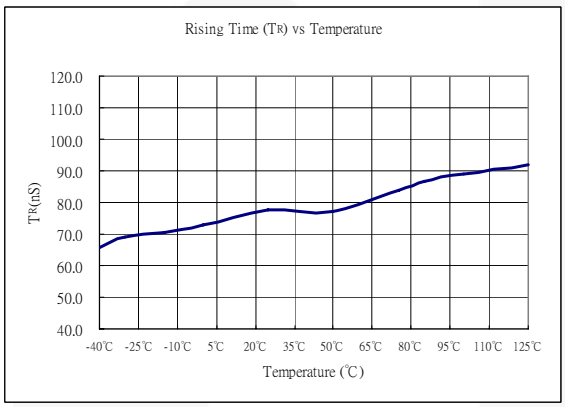

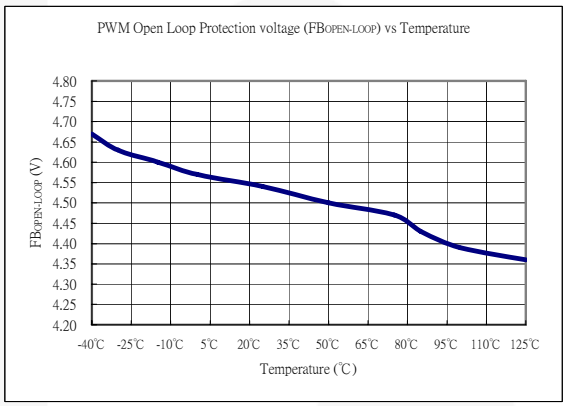

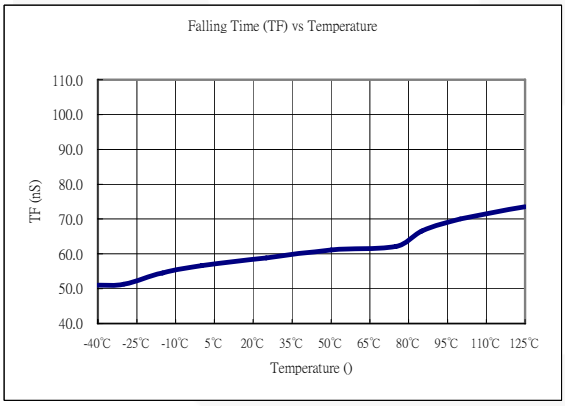

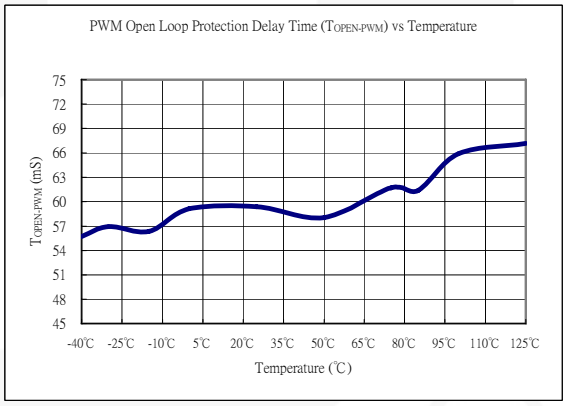

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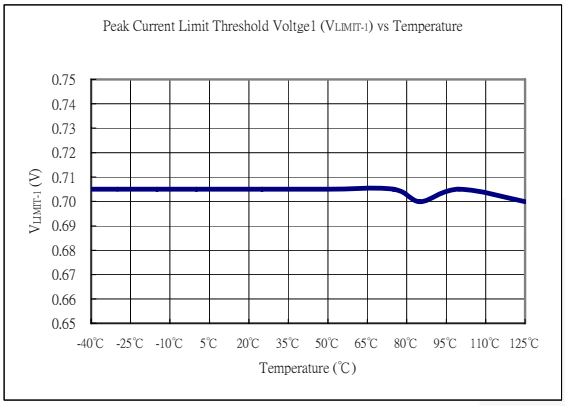

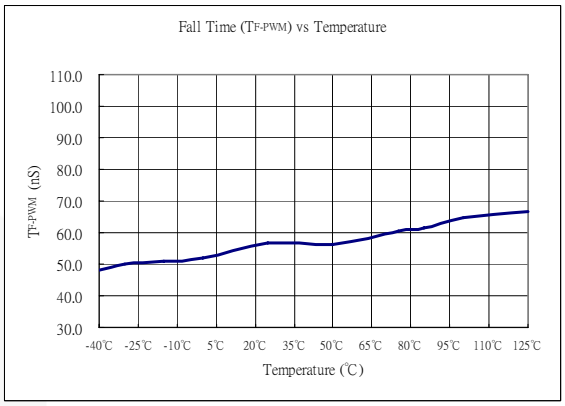

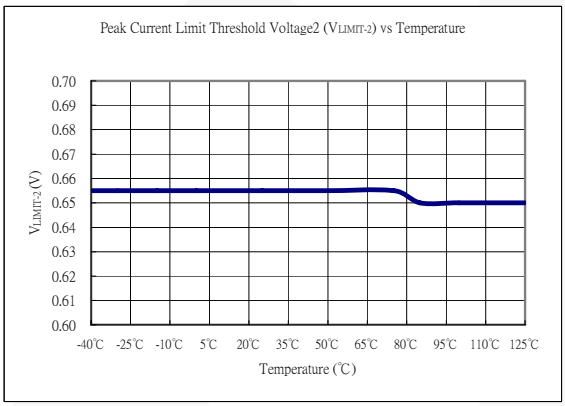

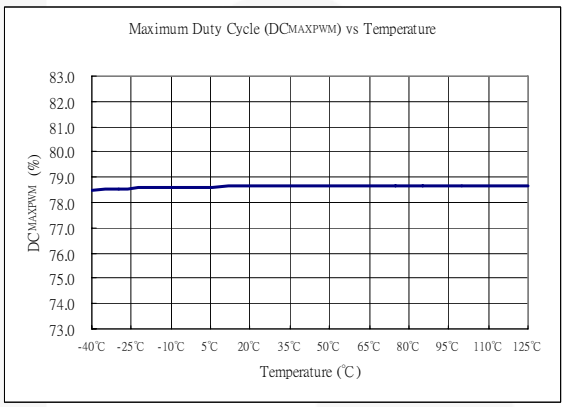

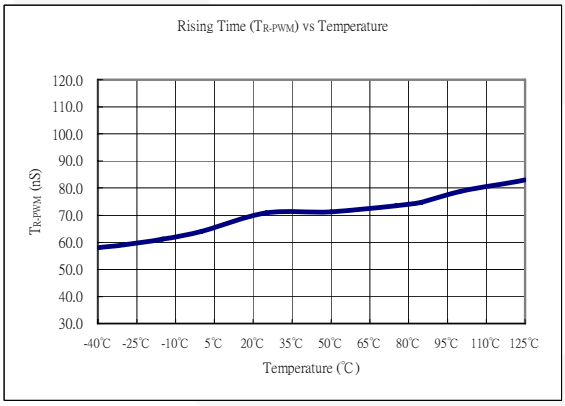

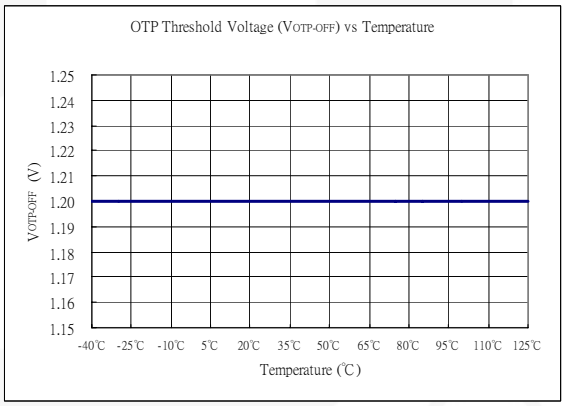

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OPERATION DESCRIPTION

The highly integrated SG6902 is designed for power supplies with boost PFC and flyback PWM. It requires very few external components to achieve green-mode operation and versatile protections / compensation.

The patented interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light loads, the switching frequency is continuously decreased to reduce power consumption. If output loading is reduced, the PFC stage is turned off to further reduce power consumption.

The PFC function is implemented by average-current-mode control. The patented switching charge multiplier-divider provides a high-degree noise immunity for the PFC circuit. The proprietary multi-vector output voltage control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6902 shuts off PFC to prevent extra-high voltage on output. Programmable two-level output voltage control reduces the PFC output voltage at low line input to increase the efficiency of the power supply.

For the flyback PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-mode operation. Built-in line-voltage compensation maintains constant output power limit. Hiccup operation during output overloading is also guaranteed. To prevent the power supply from drawing large current during start-up, the start-up for PFC stage is delayed 11.5ms after the operation of PWM stage.

In addition, SG6902 provides complete protection functions, such as brownout, over-voltage, and RI pin open/short protections.

Start-up

Figure 1 shows the start-up circuit of the SG6902. A resistor R_{AC} is utilized to charge V_{DD} capacitor through S1. The turn-on and turn-off thresholds are fixed internally at 16V/10V. During start-up, the hold-up capacitor must be charged to 16V through the start-up resistor to enable SG6902. The hold-up capacitor continues to supply V_{DD} before the energy can be delivered from auxiliary winding of the main transformer. V_{DD} must not drop below 10V during this start-up process. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply V_{DD} during start-up. Since SG6902 consumes less than 25μA start-up current, the value of R_{AC} can be large to reduce power consumption. One 10μF capacitor should hold enough energy for successful start-up. After start-up, S1 switches so that the current I_{AC} is the input for PFC multiplier. This helps reduce circuit complexity and power consumption.

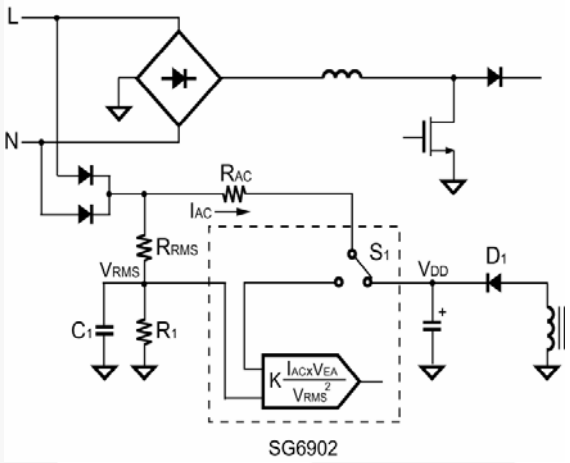

FIG.1 Start-up Circuit

Switching Frequency and Current Sources

The switching frequency can be programmed by resistor R_I connected between RI and GND. The relationship is:

$$F_{OSC} = \frac{1560}{R_I\ (k\Omega)}(kHz) \text{ ----------} \quad (1)$$

For example, a 24kΩ resistor for R_I results in a 65kHz switching frequency. Accordingly, a constant current, I_T, flows through R_I:

$$I_T = \frac{1.2V}{R_I\ (k\Omega)}(mA) \text{ ----------} \quad (2)$$

I_T is used to generate internal current reference.

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Line-Voltage Detection (VRMS)

Figure 2 shows a resistive divider with low-pass filtering for line-voltage detection on the VRMS pin. The V_{RMS} voltage is used for the PFC multiplier, brownout protection, and range control.

For brownout protection, the SG6902 is disabled with 195ms delay time if the voltage V_{RMS} drops below 0.8V.

For PFC multiplier and range control, refer to the sections below for details.

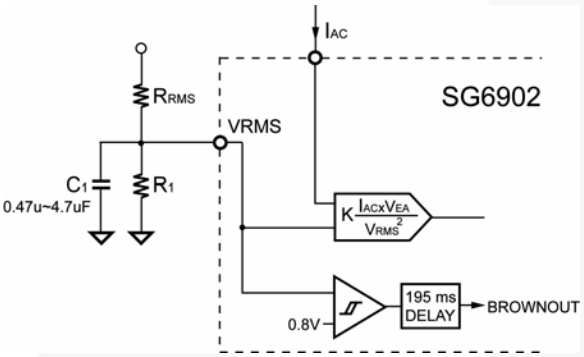

FIG.2 Line-Voltage Detection Circuit

PFC Output Voltage Control (RANGE)

For a universal input ($90V_{AC}$ ~ $264V_{AC}$) power supplies applying active boost PFC and flyback as a second stage, the output voltage of PFC is usually designed around 250V at low line and 390V at high line. This is to improve efficiency at low-line input. In SG6902, the RANGE pin (open-drain structure) is used for the two-level output voltage setting.

Figure 3 shows the RANGE output that programs the PFC output voltage. The RANGE output is shorted to ground if the V_{RMS} voltage exceeds 1.95V while high impedance (open) and the V_{RMS} voltage drops below 1.6V. The output voltages can be designed using below equations:

$$\text{Range} = \text{Open} \Rightarrow V_O = \frac{R_A + R_B}{R_B} \times 3V \quad \text{---- (3)}$$

$$\text{Range} = \text{Ground} \Rightarrow V_O = \frac{R_A + (R_B // R_C)}{(R_B // R_C)} \times 3V$$

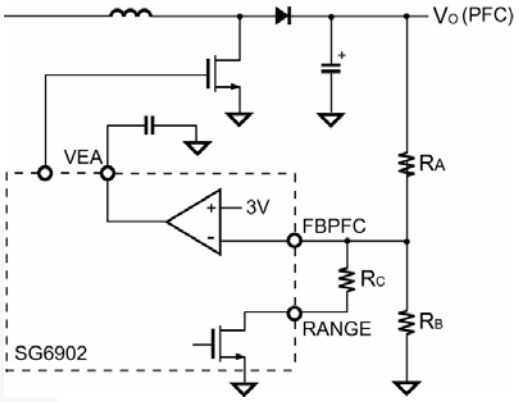

FIG.3 Range Control Two-Level Output Voltage

Interleave Switching and Green-Mode Operation

The SG6902 uses interleaved switching to synchronize the PFC and flyback stages, which reduces switching noise and spreads the EMI emissions. Figure 4 shows off-time, T_{OFF}, inserted between the turn-off of the PFC gate drive and the turn-on of the PWM.

The off-time T_{OFF} is increased in response to the decreasing of the voltage level of FBPWM. Therefore, the PWM switching frequency is continuously decreased to reduce switching losses. To further reduce power losses under extra light-load conditions, the PFC stage is turned off with a 650ms delay time.

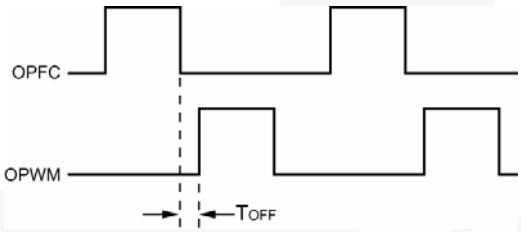

FIG.4 Interleaved Switching Pattern

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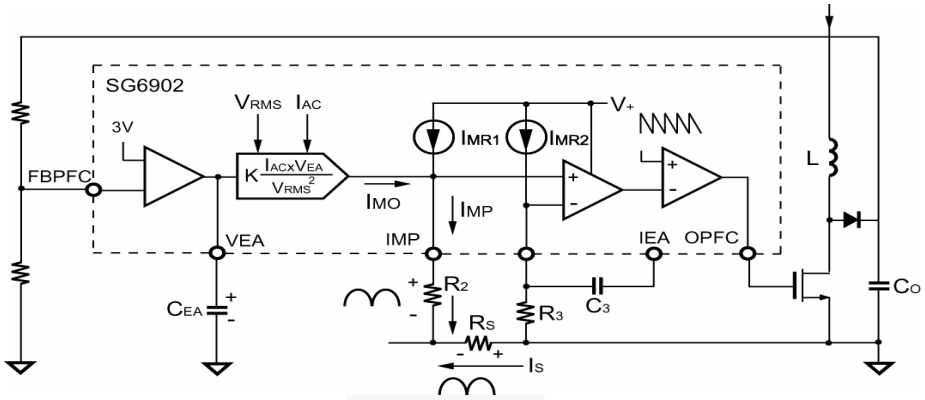

FIG.5 Average-Current-Mode Control Loop

PFC Operation

The purpose of a boost active power factor corrector (PFC) is to shape the input current of a power supply. The input current waveform and phase follow that of the input voltage. Average-current-mode control is utilized for continuous-current-mode operation for the PFC booster. With the innovative multi-vector control for voltage loop and switching charge multiplier-divider for current reference, excellent input power factor is achieved with good noise immunity and transient response. Figure 5 shows the total control loop for the average-current-mode control circuit of SG6902.

The current source output from the switching charge multiplier-divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} (\mu A) \quad \text{----------} \qquad (4)$$

I_{IMP}, the current output from the IMP pin, is the summation of I_{MO} and I_{MR1}. I_{MR1} and I_{MR2} are identical fixed-current sources. R_2 and R_3 are also identical. They are used to pull high the operating point of the IMP and IPFC pins since the voltage across R_S goes negative with respect to ground. The constant current sources I_{MR1} and I_{MR2} are typically 60μA.

Through the differential amplification of the signal across R_S, better noise immunity is achieved. The output of I_{EA} is compared with an internal sawtooth and the pulse width for PFC is determined. Through the average current-mode control loop, the input current, I_S, is proportional to I_{MO}:

$$I_{MO} \times R_2 = I_S \times R_S \quad \text{----------} \qquad (5)$$

According to Equation 5, the minimum value of R_2 and maximum of R_S can be determined, because I_{MO} should not exceed the specified maximum value.

There are different concerns in determining the value of the sense resistor R_S. The value of R_S should be small enough to reduce power consumption, but large enough to maintain the resolution. A current transformer (CT) can improve the efficiency of high-power converters.

To achieve good power factor, the voltage for V_{RMS} and V_{EA} should be kept as DC as possible, according to Equation 4. Good RC filtering for V_{RMS} and narrow bandwidth (lower than the line frequency) for voltage loop are suggested for better input current shaping. The transconductance error amplifier has output impedance Z_O (>90kΩ) and a capacitor C_{EA} (1μF ~ 10μF) that should be connected to ground (as shown in Figure 5). This establishes a dominant pole f1 for the voltage loop:

$$f_1 = \frac{1}{2\pi \times R_0 \times C_{EA}} \quad \text{----------} \qquad (6)$$

The average total input power can be expressed as:

$$\begin{aligned} Pin &= V_{IN(rms)} \times I_{IN(rms)} \\ &\propto V_{RMS} \times I_{MO} \\ &\propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} \quad \text{----------} \\ &\propto V_{RMS} \times \frac{\frac{Vin}{R_{AC}} \times V_{EA}}{V_{RMS}^2} \\ &= \sqrt{2} \times \frac{V_{EA}}{R_{AC}} \end{aligned} \qquad (7)$$

V_{EA}, the output of the voltage error amplifier, controls the total input power and the power delivered to the load.

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Multi-vector Error Amplifier

The voltage-loop error amplifier is transconductance, which has high output impedance (> 90kΩ). A capacitor C_{EA} (1μ ~ 10μF) connected from VEA to ground provides a dominant pole for the voltage loop. Although the PFC stage has a low bandwidth voltage loop for better input power factor, the innovative multi-vector error amplifier provides a fast transient response to clamp the overshoot and undershoot of the PFC output voltage.

Figure 6 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage exceeds ±5% of the reference voltage, the transconductance error amplifier adjusts its output impedance to increase the loop response. If R_A is opened, SG6902 shuts off immediately to prevent extra-high voltage on the output capacitor.

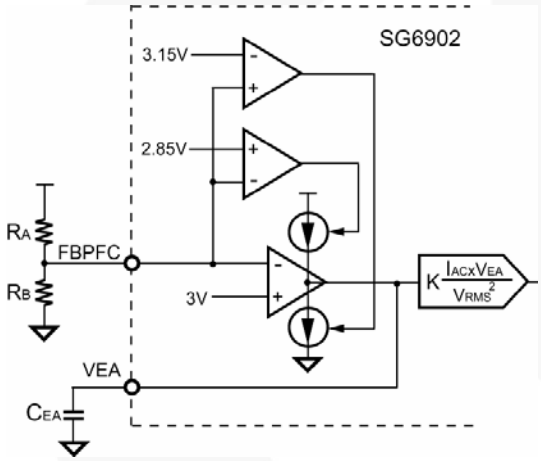

FIG.6 Multi-vector Error Amplifier

PFC Over-Voltage Protection (OVP)

When the OVP feedback voltage exceeds the over-voltage threshold, the SG6902 inhibits the PFC switching signal. This protection also prevents the PFC power converter from operating abnormally while the FBPFC pin is open.

Cycle-by-Cycle Current Limiting

SG6902 provides cycle-by-cycle current limiting for both PFC and PWM stages. Figure 7 shows the peak current limit for the PFC stage. The PFC gate drive is terminated once the voltage on the ISENSE pin goes below V_{PK}.

The voltage of V_{RMS} determines the voltage of V_{PK}. The relationship between V_{PK} and V_{RMS} is shown in Figure 7.

The amplitude of the constant current, I_P, is determined by the internal current reference, I_T, according to the following equation:

$$I_P = 2 \times I_T = 2 \times \frac{1.2V}{R_I} \quad \text{----------} \quad (8)$$

The peak current of the I_S is given by (V_{RMS}<1.05V):

$$I_{S\_peak} = \frac{(I_P \times R_P) - 0.2V}{R_S} \quad \text{----------} \quad (9)$$

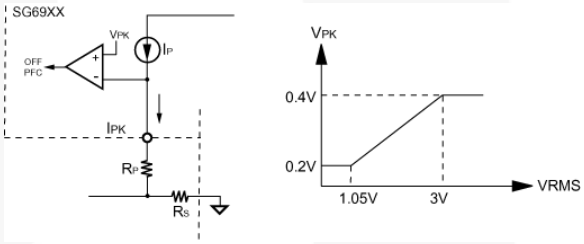

FIG.7 V_{RMS} Controlled Current Limiting

Flyback PWM and Slope Compensation

As shown in Figure 8, peak-current-mode control is utilized for flyback PWM. The SG6902 inserts a synchronized 0.5V ramp at the beginning of each switching cycle. This built-in slope compensation ensures stable operation for continuous-current-mode operation.

When the IPWM voltage, across the sense resistor, reaches the threshold voltage, 0.65V or 0.7V selected by RANGE, the OPWM is turned off after a small propagation delay, T_{PD-PWM}. This propagation delay introduces additional current, proportional to $T_{PD-PWM} \bullet V_{PFC}/L_p$, where V_{PFC} is the output voltage of PFC and L_p is the magnetized inductance of the flyback transformer. Since the propagation delay is nearly constant, higher V_{PFC} results in a larger additional current

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and the output power limit is higher than under low V_{PFC}. To compensate for this variation, the peak current threshold is modulated by the RANGE output. When RANGE is shorted to GND, the PFC output voltage is high and the corresponding threshold is 0.65V. When RANGE is opened, the PFC output voltage is low and the corresponding threshold is 0.7V.

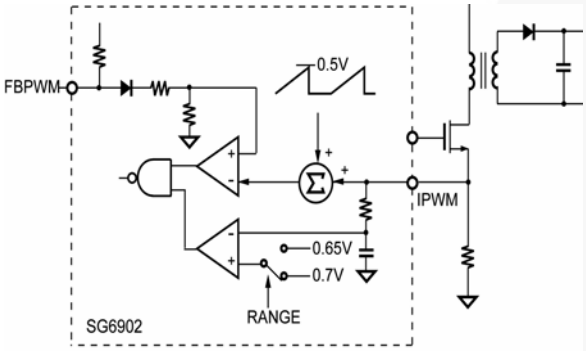

FIG.8 Peak Current Control Loop

Limited Power Control

Every time the output of power supply is shorted or overloaded, the FBPWM voltage increases. If the FB voltage is higher than a designed threshold, 4.5V, for longer than 56ms, the OPWM is turned off. As OPWM is turned off, the supply voltage V_{DD} begins decreasing.

When V_{DD} is lower than the turn-off threshold, such as 10V, SG6902 is totally shut down. Due to the start-up resistor, V_{DD} is charged up to the turn-on threshold voltage, 16V, until enabled again. If the overloading condition persists, the protection occurs repeatedly to prevent the power supply from being overheated during overloading condition.

Over-Temperature Protection (OTP)

SG6902 provides an OTP pin for over-temperature protection. A constant current is output from this pin. If R_I is equal to 24kΩ, the magnitude of the constant current is 100μA. An external NTC thermistor must be connected from this pin to ground, as shown as Figure 9. When the OTP voltage drops below 1.2V, SG6902 is disabled until the OTP voltage exceeds 1.4V.

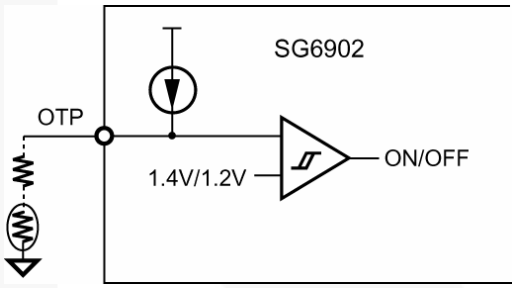

Fig.9 OTP Function

Soft-Start

During start-up of PWM stage, the SS pin charges an external capacitor with a constant current source. The voltage on FBPWM is clamped by SS voltage during start-up. In the event of a protection condition and/or PWM being disabled, the SS pin quickly discharges.

Gate Drivers

SG6902 output stage is a fast totem-pole gate driver. The output driver is clamped by an internal 18V Zener diode to protect the power MOSFET.

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PCB Layout

SG6902 has two ground pins. Good high-frequency or RF layout practices should be followed. Avoid long PCB traces and component leads. Locate decoupling capacitors near the SG6902. A resistor (5 ~ 20Ω) is recommended, connected in series from the OPFC and OPWM, to the gate of the MOSFET.

Isolating the interference between the PFC and PWM stages is also important. Figure 10 shows an example of the PCB layout. The *ground trace* connected from the AGND pin to the decoupling capacitor should be low impedance and as short as possible. The *ground trace 1* provides a signal ground and should be connected directly to the decoupling capacitor V_{DD} and/or to the AGND pin. The *ground trace* 2 shows that the AGND pins should connect to the PFC output capacitor C_O independently. The *ground trace 3* is independently tied from the PGND to the PFC output capacitor C_O. The ground in the output capacitor C_O is the major ground reference for power switching. To provide a good ground reference and reduce switching noise of both the PFC and PWM stages, the *ground traces 6 and 7* should be located very near and be low impedance.

The IPFC pin is connected directly to R_S through R_3 to improve noise immunity (do not incorrectly connect to ground trace 2). The IMP and ISENSE pins should be connected directly via the resistors R_2 and R_P to another terminal of R_S. Because the *ground trace 4 and 5* are PFC and PWM stages of the current loop, they should be as short as possible.

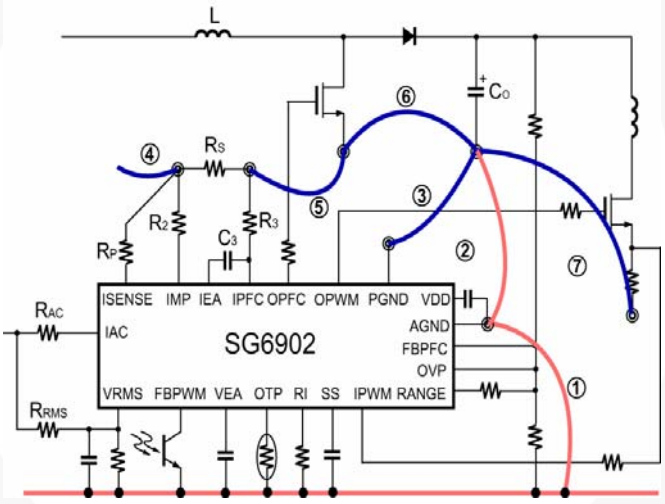

Fig.10 Layout Considerations

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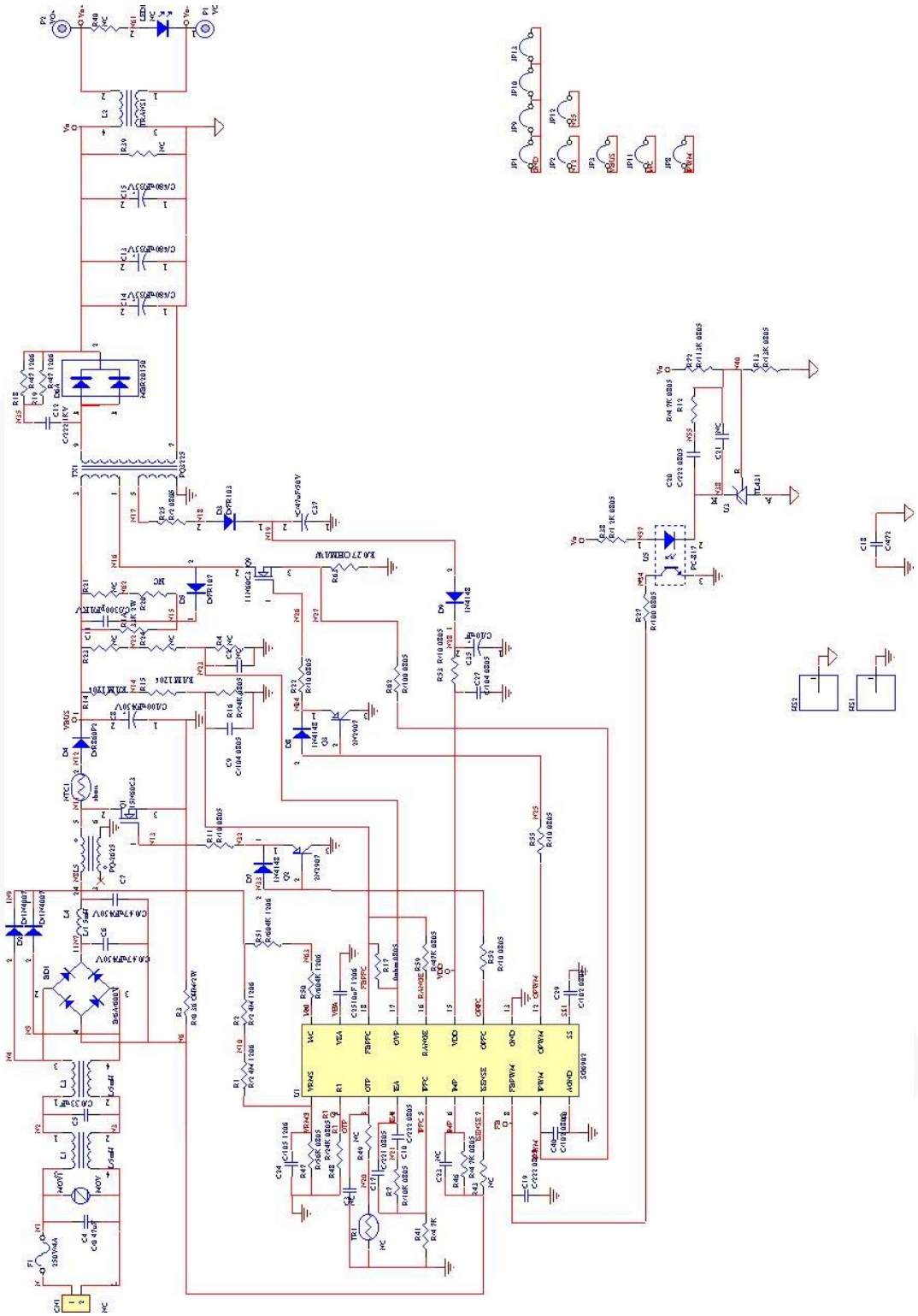
REFERENCE CIRCUIT



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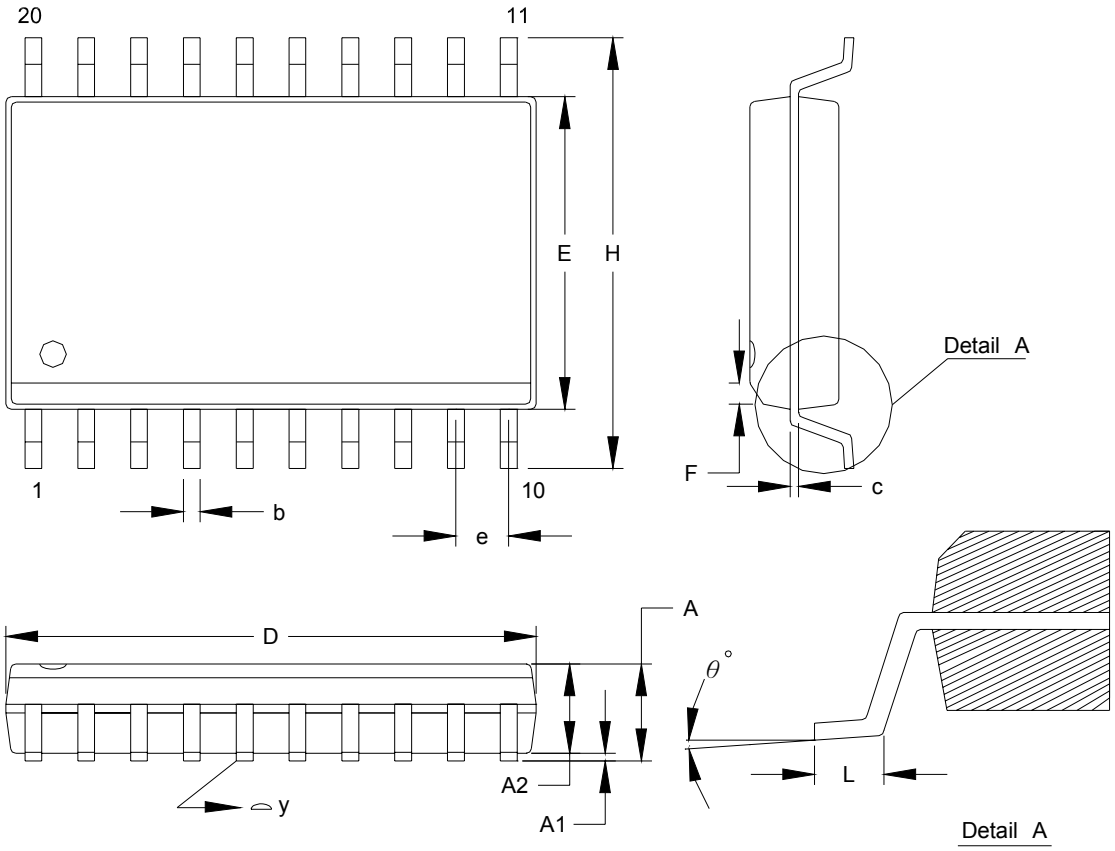
PACKAGE INFORMATION

20 PINS – PLASTIC SOP (S)



Dimensions:

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.362		2.642	0.093		0.104
A1	0.101		0.305	0.004		0.012
A2	2.260		2.337	0.089		0.092
b		0.406			0.016	
c		0.203			0.008	
D	12.598		12.903	0.496		0.508
E	7.391		7.595	0.291		0.299
e		1.270			0.050	
H	10.007		10.643	0.394		0.419
L	0.406		1.270	0.016		0.050
F		0.508X45°			0.020X45°	
y			0.101			0.004
θ°	0°		8°	0°		8°

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i-Lo™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
®
PDP-SPM™
Power220®
Power247®
POWEREDGE®
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

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