FAIRCHILD SEMICONDUCTOR®

SG5841J — Highly Integrated Green-Mode PWM Controller

Features

- Green-Mode PWM Controller
- Low Startup Current : 14μA
- Low Operating Current: 4mA
- Programmable PWM Frequency with Hopping
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Synchronized Slope Compensation
- Leading-Edge Blanking (LEB)
- Constant Output Power Limit
- Totem Pole Output with Soft Driving
- V_{DD} Over-Voltage Clamping
- Programmable Over-Temperature Protection (OTP)
- Internal Open-Loop Protection
- V_{DD} Under-Voltage Lockout (UVLO)
- GATE Output Maximum Voltage Clamp:18V

Applications

General-purpose, switch-mode, power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame SMPS

Description

The highly integrated SG5841/J series of PWM controllers provides several features to enhance the performance of flyback converters.

To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to continuously decrease the switching frequency at light-load conditions. This green-mode function enables the power supply to meet international power conservation requirements. To further reduce power consumption, SG5841/J is manufactured using the BiCMOS process. This allows a low startup current, around 14μA, and an operating current of only 4mA. As a result, a large startup resistance can be used.

The built-in synchronized slope compensation achieves stable peak-current-mode control. The proprietary internal sawtooth power-limiter ensures a constant output power limit over a wide range of AC input voltages, from $90V_{AC}$ to $264V_{AC}$.

SG5841/J provides many protections. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety should an open-loop or output-short-circuit failure occur. PWM output is disabled until V_{DD} drops below the UVLO lower limit, then the controller restarts. An external NTC thermistor can be applied for over-temperature protection.

SG5841/J is available in an 8-pin DIP or SOP package.

Ordering Information

Part Number	Ambient Operating Temperature Range	Frequency Hopping	Package
SG5841JSZ	-20 to +85°C	Yes	8-Pin Small Outline Package (SOP)
SG5841JSY	-20 to +85°C	Yes	8-Pin Small Outline Package (SOP)
SG5841SZ	-20 to +85°C	No	8-Pin Small Outline Package (SOP)
SG5841SY	-20 to +85°C	No	8-Pin Small Outline Package (SOP)

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Typical Application

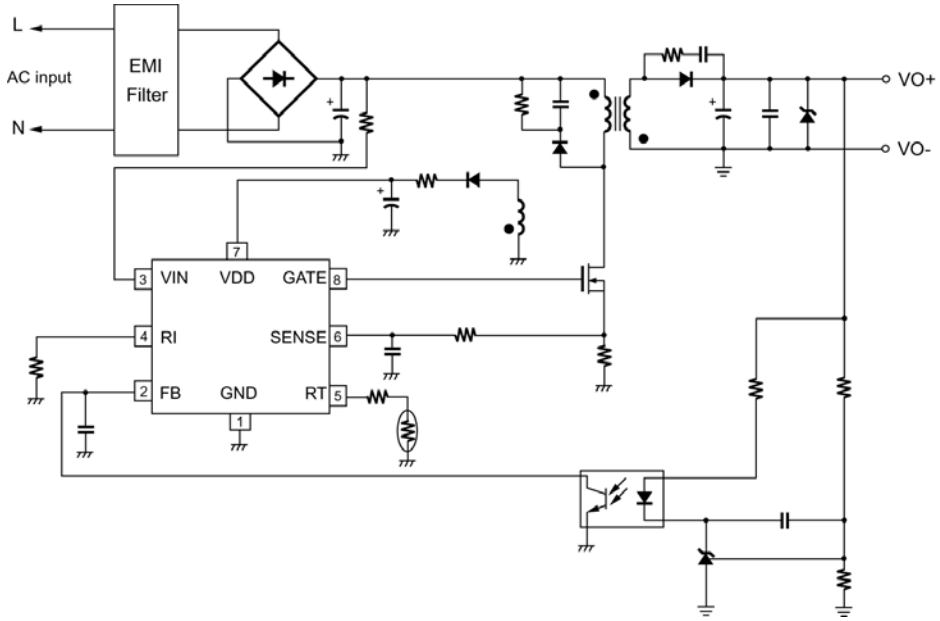


Figure 1. Application Diagram

Block Diagram

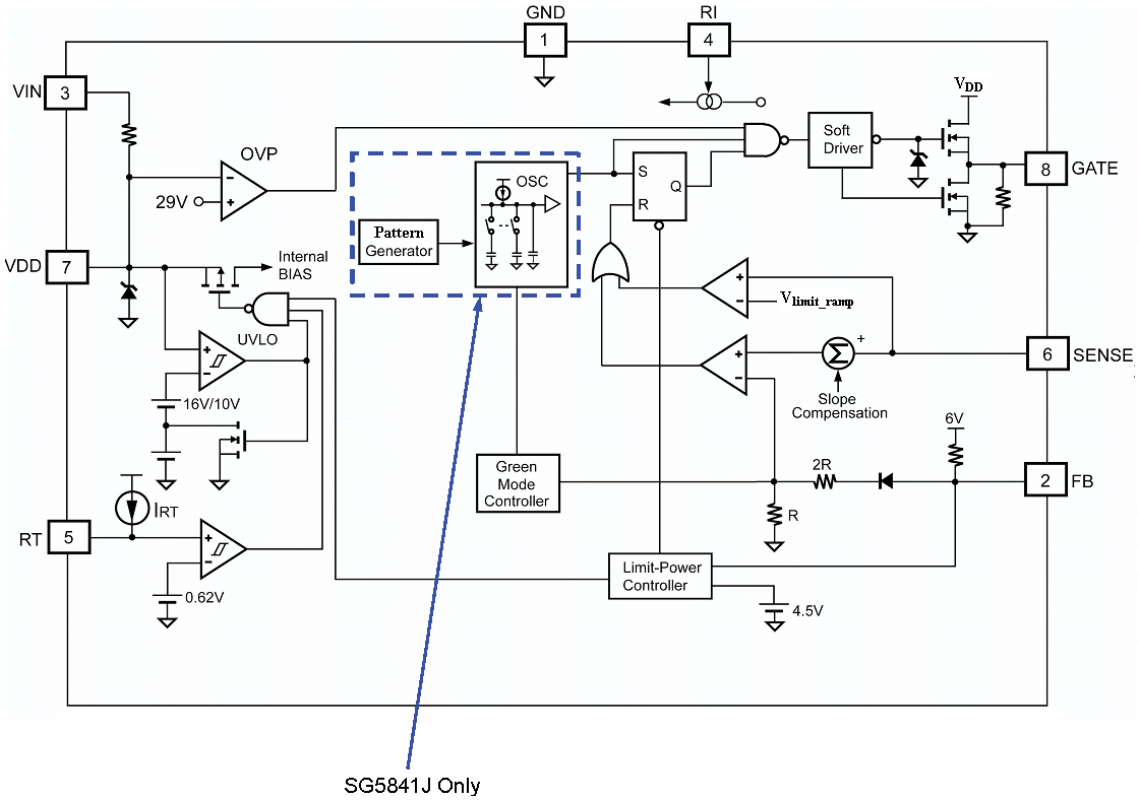
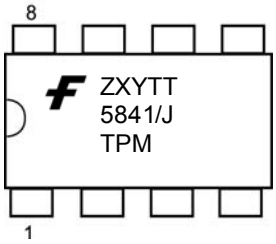


Figure 2. Block Diagram

Marking Information

marking for SG5841JSZ (pb-free)
marking for SG5841JDZ (pb-free)
marking for SG5841SZ (pb-free)
marking for SG5841DZ (pb-free)

H: J = with Frequency Hopping
Null = without Frequency Hopping
T: D = DIP, S = SOP
P: Z = Lead Free
Null = regular package
XXXXXXXX : Wafer Lot
Y: Year; WW: Week
V: Assembly Location



marking for SG5841JSY (green-compound)
marking for SG5841SY (green-compound)

F: Fairchild Logo
Z:Plant Code
X:1 Digit Year Code
Y:1 Digit Week Code
TT:2 Digit Die Run Code
T: Package Type (D:DIP, S:SOP)
P:Y = Green Package
M:Manufacturing Flow Code

Figure 3. Top Mark

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Pin Configuration

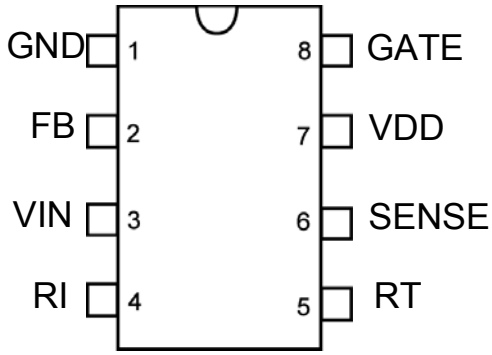

Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Function	Description
1	GND	Ground	Ground.
2	FB	Feedback	The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal from this pin and the current-sense signal from pin 6. If FB voltage exceeds the threshold, the internal protection circuit disables PWM output after a predetermined delay time.
3	VIN	Startup Input	For startup, this pin is pulled HIGH to the rectified line input via a resistor. Since the startup current requirement is very small, a large startup resistance is used to minimize power loss.
4	RI	Reference Setting	A resistor connected from the RI to GND provides a constant current source. This determines the center PWM frequency. Increasing the resistance reduces PWM frequency. Using a 26KΩ resistor results in a 65KHz center PWM frequency.
5	RT	Temperature Detection	For over-temperature protection. An external NTC thermistor is connected from this pin to the GND pin. The impedance of the NTC decreases at high temperatures. Once the voltage of the RT pin drops below a fixed limit, PWM output is disabled.
6	SENSE	Current Sense	Current sense. The sensed voltage is used for peak-current-mode control and cycle-by-cycle current limiting.
7	VDD	Power Supply	Power supply. If V_{DD} exceeds a threshold, the internal protection circuit disables PWM output.
8	GATE	Driver Output	The totem-pole output driver for the power MOSFET, which is internally clamped below 18V.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to GND pin.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	Supply Voltage			30	V
V_{IN}	Input Terminal			30	V
V_{FB}	Input Voltage to FB Pin		-0.3	7.0	V
V_{SENSE}	Input Voltage to SENSE Pin		-0.3	7.0	V
V_{RT}	Input Voltage to RT Pin		-0.3	7.0	V
V_{RI}	Input Voltage to RI Pin		-0.3	7.0	V
P_D	Power Dissipation (T_A < 50°C)	DIP		800	mW
		SOP		400	
Θ_{JA}	Thermal Resistance (Junction-to-Air)	DIP		82.5	°C/W
		SOP		141	
Θ_{JC}	Thermal Resistance (Junction-to-Case)	DIP		59.7	°C/W
		SOP		80.8	
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Wave Soldering or Infrared, 10 Seconds)			260	°C
ESD	Human Body Model, JESD22-A114			3	kV
	Charged Device Model, JESD22-C101			250	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperatures	-20	+85	°C

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Electrical Characteristics

V_{DD} = 15V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
V_{DD} Section							
V_{DD-OP}	Continuously Operating Voltage					24.7	V
V_{DD-ON}	Start Threshold Voltage			15	16	17	V
V_{DD-OFF}	Minimum Operating Voltage			9	10	11	V
I_{DD-ST}	Startup Current		V_{DD}=V_{DD-ON}–0.16V		14	30	µA
I_{DD-OP}	Operating Supply Current		V_{DD}=15V, R_I=26KΩ, GATE=OPEN		4	5	mA
$V_{DD-CLAMP}$	V_{DD} Over-Voltage-Clamping Level			28	29		V
$t_{D-VDDCLAMP}$	V_{DD} Over-Voltage-Clamping Debounce Time		R_I=26KΩ	50	100	200	µs
R_I Section							
RI_{NOR}	R_I Operating Range			15.5		36.0	KΩ
RI_{MAX}	Maximum R_I Value for Protection				230		KΩ
RI_{MIN}	Minimum R_I Value for Protection				10		KΩ
Oscillator Section							
f_{OSC}	Normal PWM Frequency	Center Frequency	R_I=26KΩ	62	65	68	KHz
		Hopping Range	R_I=26KΩ (SG5841J only)	±3.7	±4.2	±4.7	
t_{HOP}	Hopping Period		R_I=26KΩ (SG5841J only)	3.9	4.4	4.9	ms
f_{OSC-G}	Green-Mode Frequency		R_I=26KΩ	18	22	25	KHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation		V_{DD}=11.5V to 24.7V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation		T_A=-20 to +85°C			5	%
Feedback Input Section							
A_V	FB Input to Current Comparator Attenuation			1/3.75	1/3.20	1/2.75	V/V
Z_{FB}	Input Impedance			4		7	KΩ
$V_{FB-OPEN}$	FB Output High Voltage		FB pin open	5	6		V
V_{FB-OLP}	FB Open-Loop Trigger Level			4.2	4.5	4.8	V
t_{D-OLP}	Delay Time of FB Pin Open-Loop Protection		R_I=26KΩ	26	29	32	ms
V_{FB-N}	Green-Mode Entry FB Voltage		R_I=26KΩ	1.9	2.1	2.3	V
V_{FB-G}	Green-Mode Ending FB Voltage		R_I=26KΩ		V_{FB-N}-0.5		V

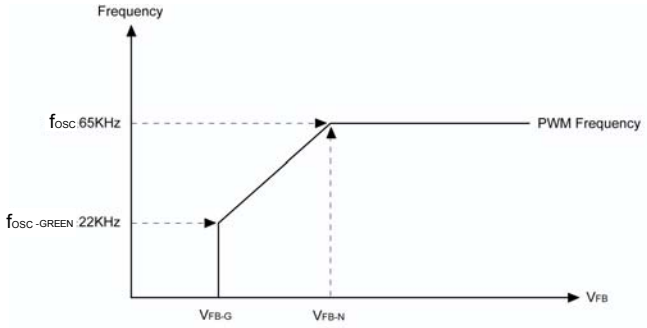

Figure 5. PWM Frequency

Electrical Characteristics (Continued)

V_{DD} = 15V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Current-Sense Section						
Z_{SENSE}	Input Impedance			12		KΩ
V_{STHFL}	Current Limit Flatten Threshold Voltage		0.85	0.90	0.95	V
V_{STHVA}	Current Limit Valley Threshold Voltage	V_{STHFL}–V_{STHVA}		0.22		V
t_{PD}	Propagation Delay to GATE Output	R_I=26KΩ		150	200	ns
t_{LEB}	Leading-Edge Blanking Time	R_I=26KΩ	200	270	350	ns
GATE Section						
DCY_{MAX}	Maximum Duty Cycle		60	65	70	%
V_{GATE-L}	Output Voltage Low	V_{DD}=15V, I_O=50mA			1.5	V
V_{GATE-H}	Output Voltage High	V_{DD}=12.5V, I_O=50mA	7.5			V
t_r	Rising Time	V_{DD}=15V, C_L=1nF	150	250	350	ns
t_f	Falling Time	V_{DD}=15V, C_L=1nF	30	50	90	ns
I_O	Peak Output Current	V_{DD}=15V, GATE=6V	230			mA
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=24.7V		18	19	V
RT Section						
I_{RT}	Output Current of RT Pin	R_I=26KΩ	92	100	108	μA
V_{RTTH}	Trigger Voltage for Over-Temperature Protection		0.585	0.620	0.655	V
V_{RT-RLS}	OTP Release Voltage			V_{RTTH} +0.03		V
t_{D-OTP}	Over-Temperature Debounce	R_I=26KΩ	60	100	140	μs

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Typical Performance Characteristics

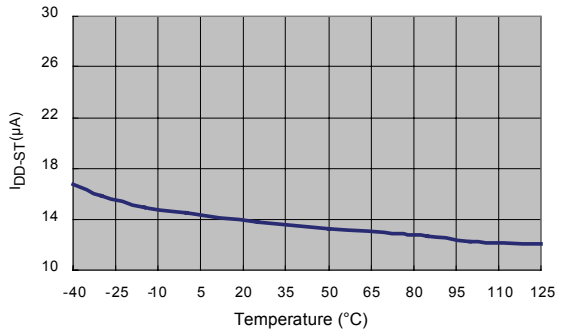

Figure 6. Startup Current (I_{DD-ST}) vs. Temperature

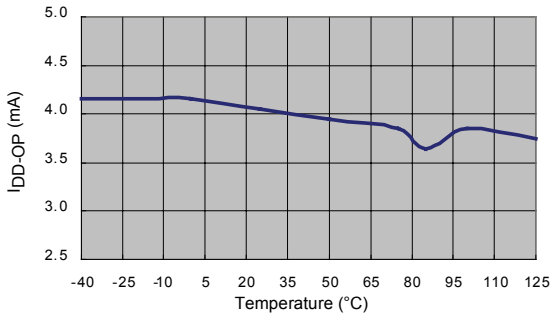

Figure 7. Operating Supply Current (I_{DD-OP}) vs. Temperature

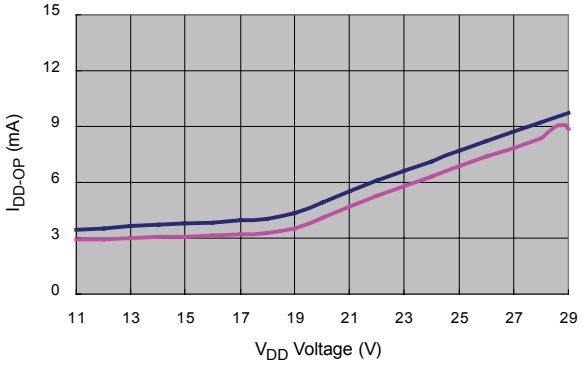

Figure 8. Operating Current (I_{DD-OP}) vs. V_{DD} Voltage

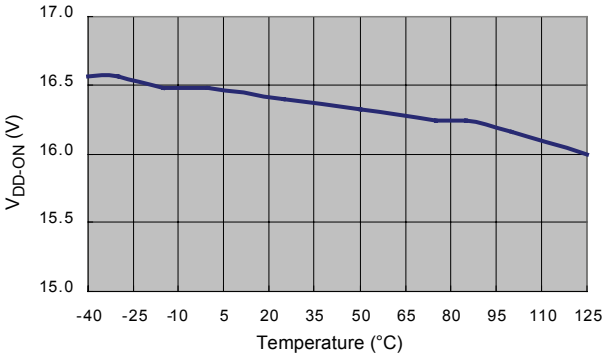

Figure 9. Start Threshold Voltage (V_{DD-ON}) vs. Temperature

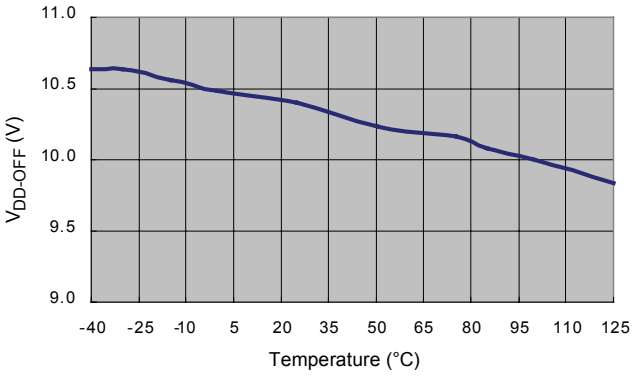

Figure 10. Minimum Operating Voltage (V_{DD-ON}) vs. Temperature

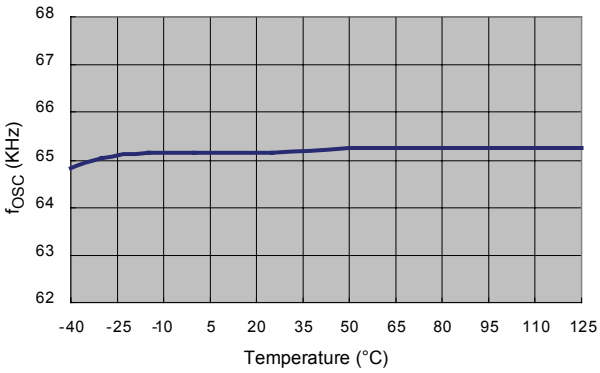

Figure 11. PWM Frequency (f_{OSC}) vs. Temperature

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Typical Performance Characteristics (Continued)

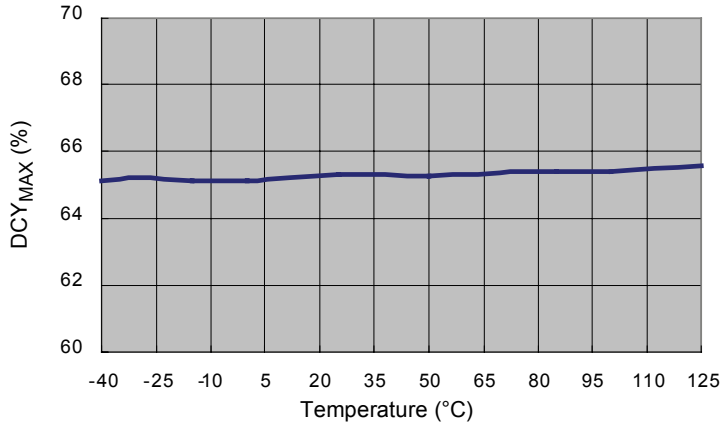

Figure 12. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

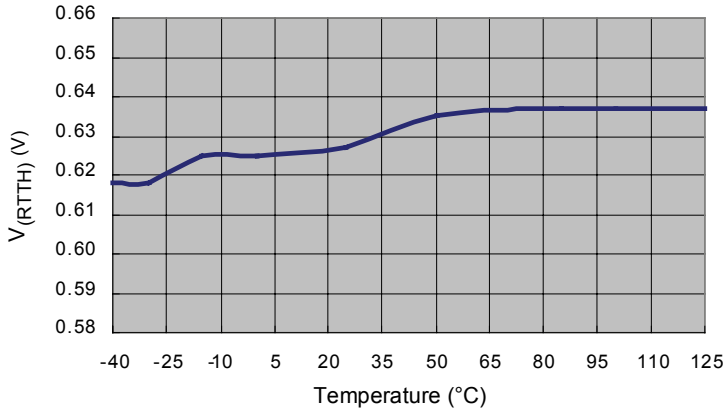

Figure 13. Trigger Voltage for Over-Temperature Protection V_{RTTH} vs. Temperature

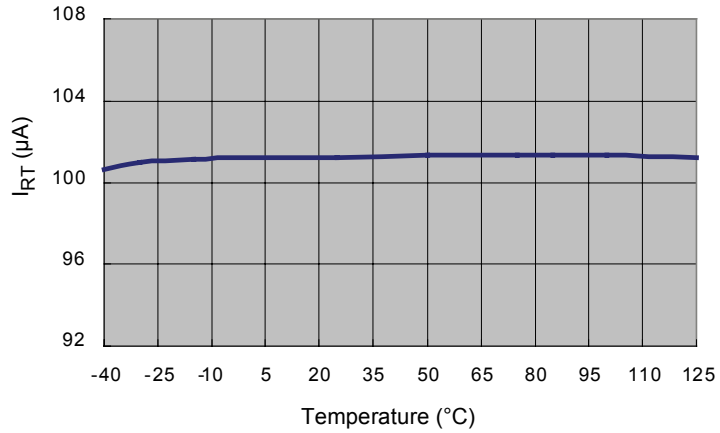

Figure 14. Output Current of RT Pin (I_{RT}) vs. Temperature

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Functional Description

Startup Current

Typical startup current is only 14μA, which allows a high-resistance and low-wattage startup resistor to minimize power loss. For an AC/DC adapter with universal input range, a 1.5MΩ, 0.25W startup resistor and a 10μF/25V V_{DD} hold-up capacitor are enough for this application.

Operating Current

Operating current is around 4mA. The low operating current enables better efficiency and reduces the requirement of V_{DD} hold-up capacitance.

Green-Mode Operation

The proprietary green-mode function provides off-time modulation to continuously decrease the PWM frequency under light-load conditions. To avoid acoustic noise problems, the minimum PWM frequency is set above 22KHz. Green mode dramatically reduces power consumption under light-load and zero-load conditions. Power supplies using a SG5841/J controller can meet restrictive international regulations regarding standby power consumption.

Oscillator Operation

A resistor connected from the RI pin to the GND pin generates a constant current source for the SG5841/J controller. This current is used to determine the center PWM frequency. Increasing the resistance reduces PWM frequency. Using a 26KΩ resistor, R_I, results in a corresponding 65KHz PWM frequency. The relationship between R_I and the switching frequency is:

$$f_{PWM} = \frac{1690}{R_I\ (K\Omega)}(KHz) \quad (1)$$

The range of the PWM oscillation frequency is designed as 47KHz ~ 109KHz.

SG5841J also integrates a frequency hopping function internally. The frequency variation ranges from around 62KHz to 68KHz for a center frequency of 65KHz. The frequency-hopping function helps reduce EMI emission of a power supply with minimum line filters.

Current Sensing / PWM Current Limiting

Peak-current-mode control is utilized in to regulate output voltage and provide pulse-by-pulse current limiting. The switch current is detected by a sense resistor into the SENSE pin. The PWM duty cycle is determined by this current-sense signal and the feedback voltage. When the voltage on the SENSE pin reaches around $V_{COMP} = (V_{FB}–1.0)/3.2$, a switch cycle is terminated immediately. V_{COMP} is internally clamped to a variable voltage around 0.85V for output power limit.

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs at the sense-resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate drive.

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16V and 10V. During startup, the hold-up capacitor must be charged to 16V through the startup resistor to enable the IC. The hold-up capacitor continues to supply V_{DD} before the energy can be delivered from auxiliary winding of the main transformer. V_{DD} must not drop below 10V during this startup process. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply V_{DD} during startup.

Gate Output / Soft Driving

The SG5841/J BiCMOS output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18V Zener diode to protect power MOSFET transistors against undesirable gate over-voltage. A soft driving waveform is implemented to minimize EMI.

Built-in Slope Compensation

The sensed voltage across the current-sense resistor is used for peak-current-mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability or prevents sub-harmonic oscillation. SG5841/J inserts a synchronized, positive-going ramp at every switching cycle.

Constant Output Power Limit

When the SENSE voltage across the sense resistor, R_S, reaches the threshold voltage, around 0.85V, the output GATE drive is turned off after delay, t_{PD}. This delay introduces additional current, proportional to $t_{PD} \cdot V_{IN} / L_P$. The delay is nearly constant, regardless of the input voltage V_{IN}. Higher input voltage results in larger additional current and the output power limit is higher than under low-input line voltage. To compensate this variation for a wide AC input range, a sawtooth power-limiter (saw limiter) is designed to solve the unequal power-limit problem. The saw limiter is designed as a positive ramp signal (V_{limit_ramp}) and fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs.

V_{DD} Over-Voltage Clamping

V_{DD} over-voltage clamping prevents damage due to abnormal conditions. If V_{DD} voltage is over the V_{DD} over-voltage clamping voltage ($V_{DD-CLAMP}$) and lasts for $t_{D-VDDCLAMP}$, the PWM pulses are disabled until the V_{DD} drops below the V_{DD} over-voltage clamping voltage.

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Thermal Protection

An NTC thermistor R_{NTC} in series with a resistor R_A can be connected from the RT pin to ground. A constant current I_{RT} is output from pin RT. The voltage on the RT pin can be expressed as $V_{RT} = I_{RT} \times (R_{NTC} + R_A)$, in which $I_{RT} = 2 \times (1.3V / R_I)$. At high ambient temperature, R_{NTC} is smaller, such that V_{RT} decreases. When V_{RT} is less than 0.62V, the PWM is completely turned off.

Limited Power Control

The FB voltage increases every time the output of the power supply is shorted or overloaded. If the FB voltage remains higher than a built-in threshold for longer than t_{D-OLP}, PWM output is turned off. As PWM output is turned off, the supply voltage V_{DD} begins decreasing.

$$t_{D-OLP\ (ms)} = 1.115 \times R_I(K\Omega) \quad (2)$$

When V_{DD} goes below the turn-off threshold (e.g. 10V) the controller totally shuts down. V_{DD} is charged up to the turn-on threshold voltage of 16V through the startup resistor until PWM output is restarted. This protection remains activated as long as the overloading condition persists. This prevents the power supply from overheating due to overloading conditions.

Noise Immunity

Noise on the current-sense or control signal may cause significant pulse-width jitter, particularly in the continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near SG5841/J, and increasing power MOS gate resistance improve performance.

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Reference Circuit

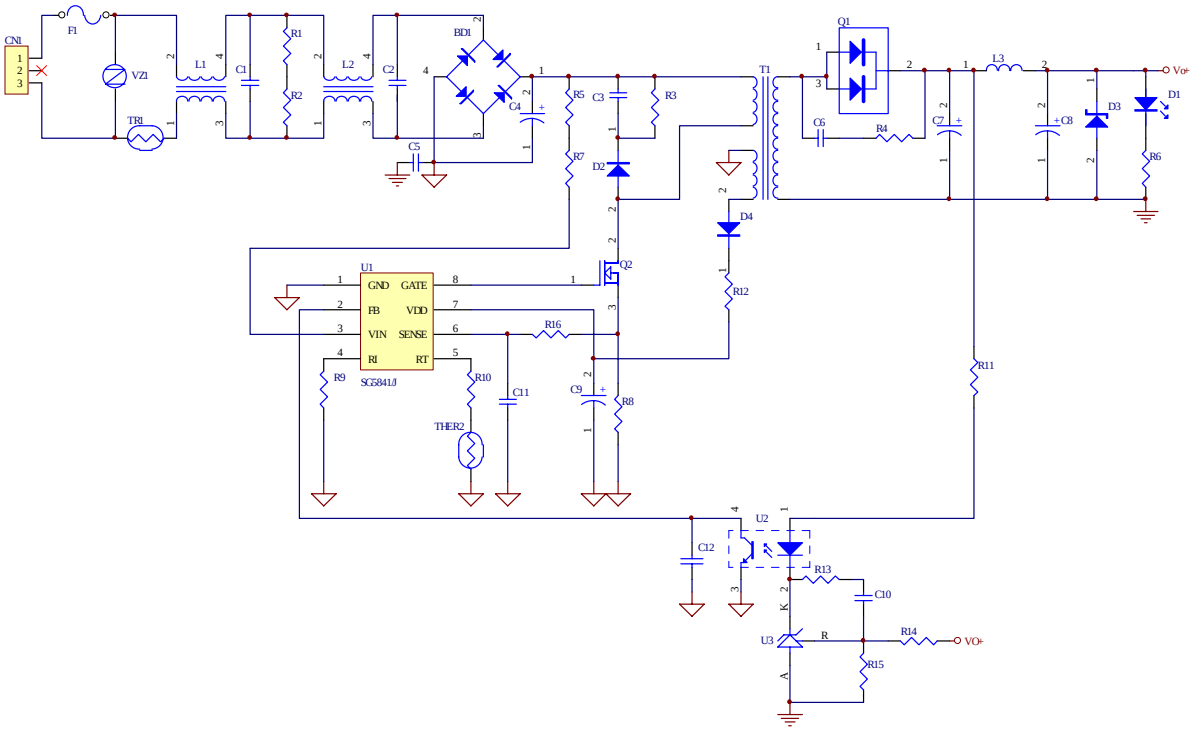

Figure 15. Reference Circuit

BOM

Reference	Component	Reference	Component
BD1	BD 4A/600V	Q2	MOS 7A/600V
C1	XC 0.68μF/300V	R1, R2	R 1MΩ 1/4W
C2	XC 0.1μF/300V	R3	R 100KW 1/2W
C3	CC 0.01μF/500V	R4	R 47Ω 1/4W
C4	EC 120μ/400V	R5, R7	R 750KΩ 1/4W
C5	YC 222p/250V	R6	R 2KΩ 1/8W
C6	CC 1000pF/100V	R8	R 0.3Ω 2W
C7	EC 1000μF/25V	R9	R 33KΩ 1/8W
C8	EC 470μF/25V	R10	R 4.7KΩ 1/8W 1%
C9	EC 10μF/50V	R11	R 470Ω 1/8W
C10	CC 222pF/50V	R12	R 0Ω 1/8W
C11	CC 470pF/50V	R13	R 4.7KΩ 1/8W
C12	CC 102pF/50V (Option)	R14	R 154KΩ 1/8W
D1	LED	R15	R 39KΩ 1/8W
D2	Diode BYV95C	R16	R 100Ω 1/8W
D3	TVS P6KE16A	THER2	Thermistor TTC104
D4	Diode FR103	T1	Transformer (600μH-PQ2620)
F1	FUSE 4A/250V	U1	IC SG5841/J
L1	Choke (900μH)	U2	IC PC817
L2	Choke (10mH)	U3	IC TL431
L3	Inductor (2μH)	VZ1	VZ 9G
Q1	Diode 20A/100V		

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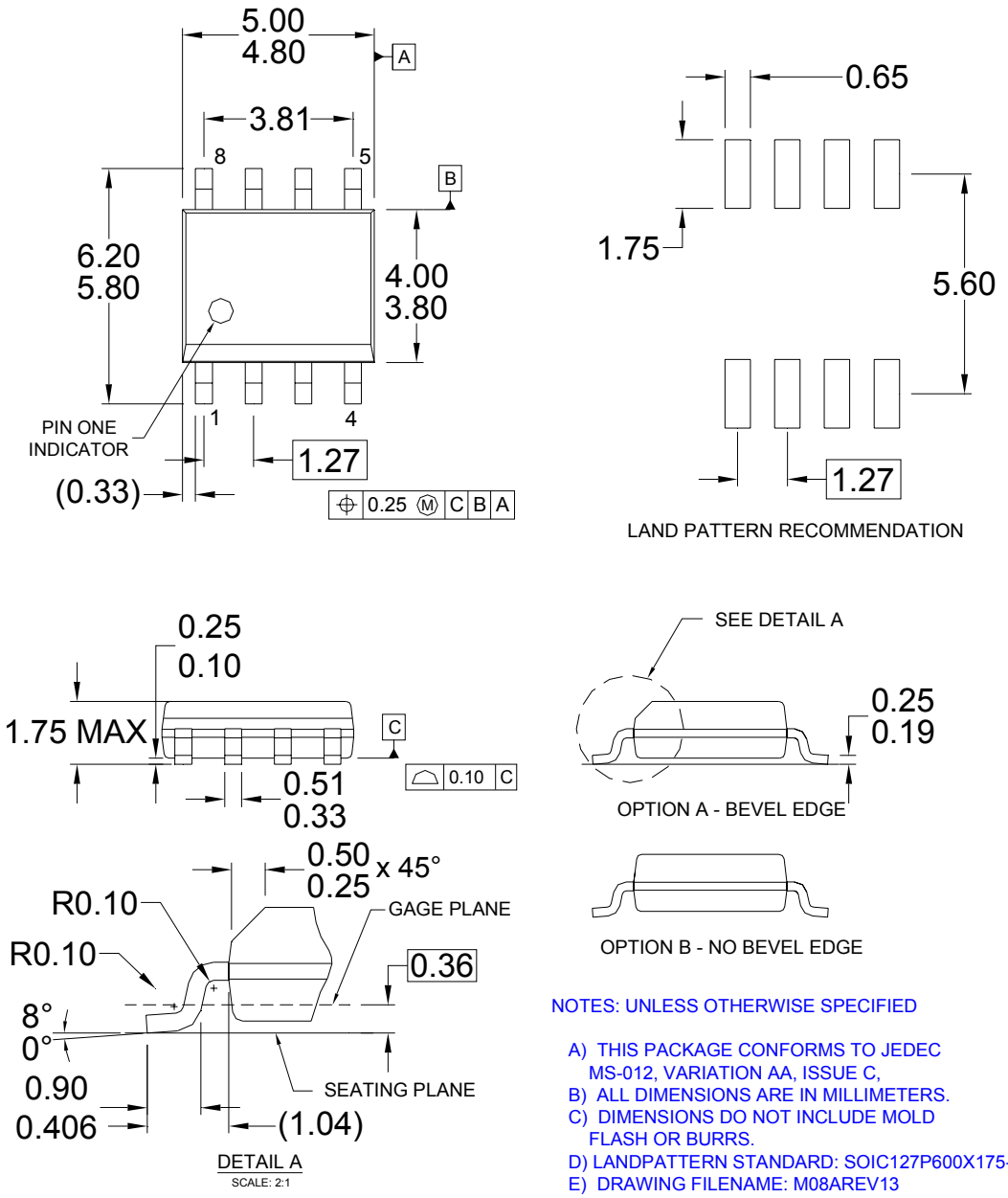
Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
E) DRAWING FILENAME: M08AREV13

Figure 16. 8-Pin Small Outline Package (SOP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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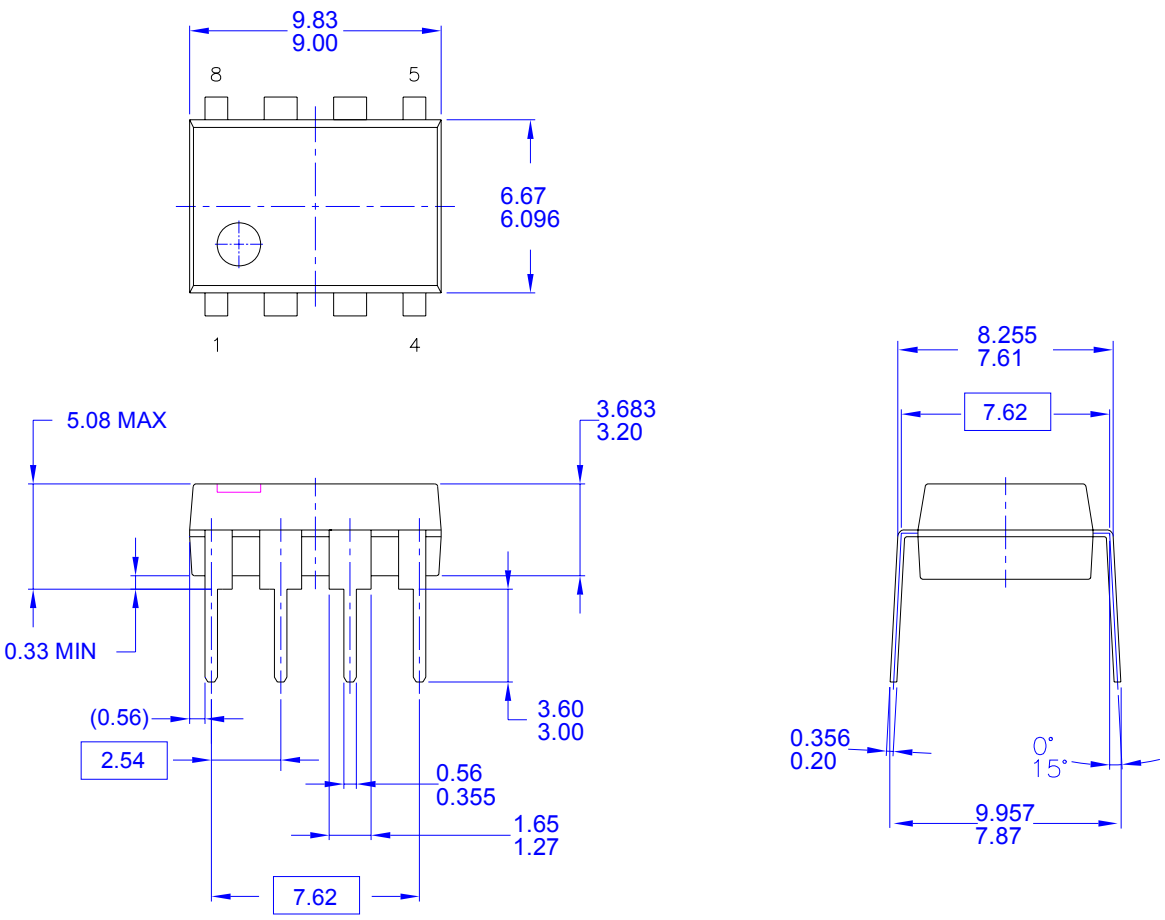
Physical Dimensions (Continued)



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

E) DRAWING FILENAME AND REVSION: MKT-N08FREV2.

Figure 17. 8-Pin Dual Inline Package (DIP)

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