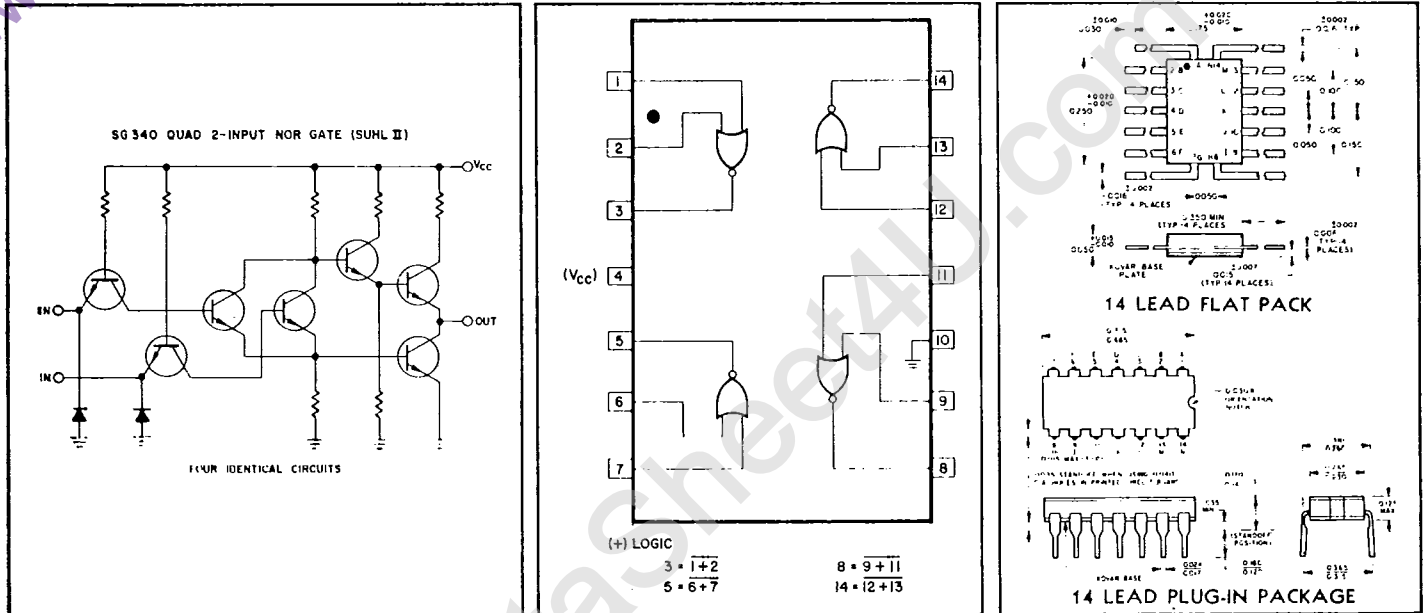


INTEGRATED CIRCUITS SUHL* II

NEW PRODUCT REPORT

Monolithic Silicon Epitaxial Circuit For Military Temp. Range -55°C to $+125^{\circ}\text{C}$ • Industrial 0°C to $+75^{\circ}\text{C}$

Quad 2-Input Nor/Nand Gate SG 340 Series



CIRCUIT DESCRIPTION

The SG340 series of gates are members of the SUHL II family of logic elements which is a monolithic, epitaxial, saturated high speed logic family. Each package contains four circuits. Each circuit consists of two input transistors which are OR'ed together and then inverted. Each input has a clamp diode to assist in reducing the effects of system ringing. The gate functions as a NOR element in positive logic, and a NAND element in negative logic. The circuit is designed for high speed operation over the military and industrial temperature range without sacrificing characteristics of fan out, logic swing, noise immunity and capacitance drive at low power.

This circuit requires a single power supply and has the following outstanding features:

CHARACTERISTIC SUMMARY

1. High fan out . . . 11 min. for SG340; 6 min. for SG341; 9 min. for SG342 and 5 min. for SG343.
2. High speed . . . designed to operate at 20 mc, propagation delay time is typically 6 nsec.
3. High noise immunity . . . ± 900 mV at 25°C and worst case fan out; ± 450 mV from -55°C to $+125^{\circ}\text{C}$ at worst case fan out; ± 600 mV from 0°C to $+75^{\circ}\text{C}$ at worst case fan out.
4. High capacitance drive . . . up to 600 pF.
5. High logic swing . . . Logic 0 is typically 0.26 volts; Logic 1 is typically 3.3 volts at 25°C .
6. Short circuit protection.
7. Low power . . . 22 mw average dissipation, per gate.
8. Low output impedance in the "0" and "1" level reduces noise pickup.
9. No complex loading rules since input and output are isolated.

These features offer the logic designer an integrated circuit with combined advantages of speed at low power, high reliability and a high degree of logic flexibility. The result is a digital element that facilitates system design when combined with other SUHL elements.

*Sylvania Universal High Level Logic

The purpose of this report is to provide tentative engineering data on Sylvania Integrated Circuits.

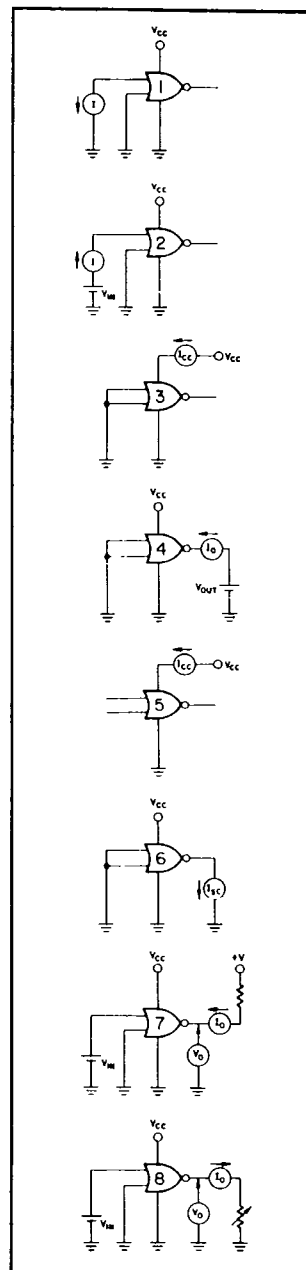
RATINGS

SG 340/341				SG 340/341			
VOLTAGE	Min.	Typ.	Max.	TEMPERATURE AND POWER	Min.	Typ.	Max.
Supply voltage (D.C.)			8.0 V	Operating	-55		+125°C
Supply voltage (surge, 1 sec)			12.0 V	Storage	-65		+200°C
Supply voltage (operating)	4.5	5.0	6.0 V	Thermal gradient, junction to air (θ_{ja}) (Flat Pack)			0.3°C/mW
Input voltage			5.5 V	Thermal gradient, junction to air (θ_{ja}) (Plug-in)			0.15°C/mW
Output voltage			5.5 V	Power Dissipation (50% Duty Cycle, $V_{CC} = +5v$)		22	mW/Circuit

ELECTRICAL SPECIFICATIONS

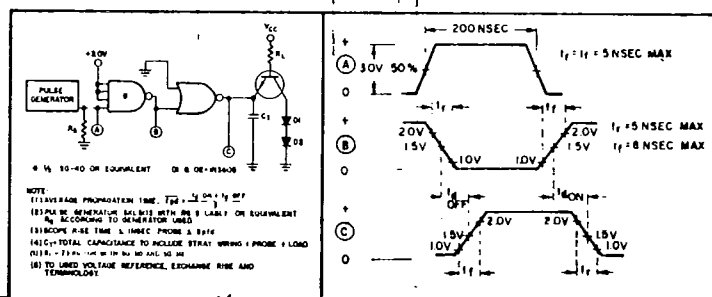
Values at Specified Temperatures						Fig. No.
Characteristics at $V_{CC} = +5.0V$	Symbol	-55°C	+25°C	+125°C	Units	
INPUT:						
Input Load Current @ $V_{IN} =$ Other Inputs	I_{IN}	2.0 0 0	2.0 0 0	2.0 0 0	mA Max. Volts Volts	1
Input Leakage Current @ $V_{IN} =$ Other Inputs	I_{IN}	0.1 4.5 0	0.1 4.5 0	0.1 4.5 0	mA Max. Volts Volts	2
Input (OFF Level) Breakdown Voltage $I_{IN} =$ Other Inputs	BV_{IN} "1"	5.5 1.0 0	5.5 1.0 0	5.5 1.0 0	Volts mA Max. Volts	2
Logic "1" Threshold Voltage $V_{OUT} =$ I_{OUT} (SG 340) I_{OUT} (SG 341)	V_{MIN} "1"	2.0 0.45 22 12	1.8 0.45 22 12	1.5 0.45 22 12	Volts Volts Max. mA mA	7
Logic "0" Threshold Voltage $V_{OUT} =$ I_{OUT} (SG 340) I_{OUT} (SG 341)	V_{MAX} "0"	0.9 2.5 2.2 1.2	1.1 2.4 2.2 1.2	0.9 2.5 2.2 1.2	Volts Volts Min. mA mA	8
OUTPUT:						
Output Leakage Current @ $V_{OUT} =$ Inputs	I_{OUT}	0.25 5.5 0	0.25 5.5 0	0.25 5.5 0	mA Max. Volts Volts	4
Output Short Circuit Current @ Input	I_{OUT}	25 100 0	25 100 0	25 100 0	mA Min. mA Max. Volts	6
Logic "0" Level @ $V_{IN} =$ I_{OUT} (SG 340) I_{OUT} (SG 341)	V_{OUT} "0"	0.40 2.7 22 12	0.40 2.7 22 12	0.45 2.7 22 12	Volts Max. Volts mA mA	7
Logic "1" Level @ $V_{IN} =$ I_{OUT} (SG 340) I_{OUT} (SG 341)	V_{OUT} "1"	2.8 0.45 2.2 1.2	3.1 0.45 2.2 1.2	3.15 0.45 2.2 1.2	Volts Min. Volts mA mA	8
POWER REQUIREMENTS:						
Breakdown Current @ $V_{CC} =$ @ $V_{IN} =$	I_{CC}		40.0 8.0 0		mA Max. Volts Volts	3
"ON" State Current Drain Inputs	I_{CC} "0"	36.0 Open	36.0 Open	36.0 Open	mA Max.	5
"OFF" State Current Drain Inputs	I_{CC} "1"	24.0 0	24.0 0	24.0 0	mA Max. Volts	3

TYPICAL TEST CONFIGURATION



SWITCHING SPECIFICATIONS

Switching Parameters	CONDITIONS				LIMITS	
	V_{CC} volts	T_A °C	Fanout		C_f pfd.	Time—nsec Max.
			SG340	SG341		
Turn On Delay	+5.0	+25	1	1	15	10
Turn Off Delay			1	1	15	10
Rise Time Note 6			1	1	15	2.5
Fall Time Note 6			1	1	15	4.0



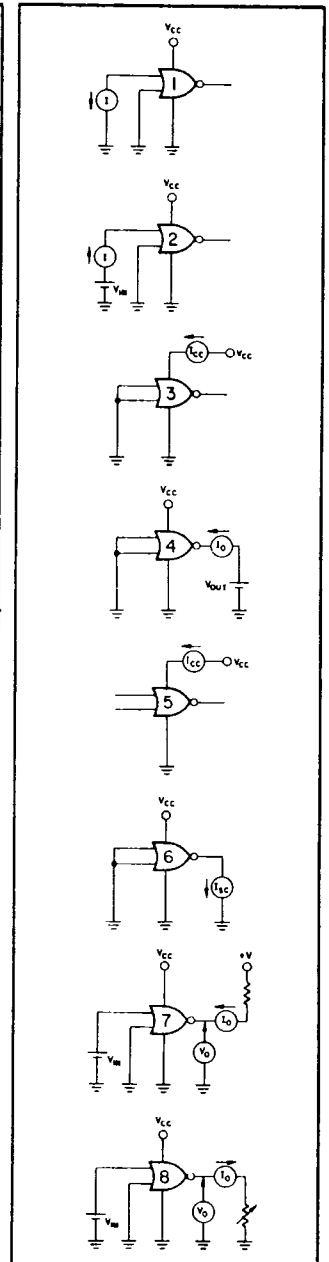
RATINGS

SG 342/343				SG 342/343			
VOLTAGE	Min.	Typ.	Max.	TEMPERATURE AND POWER	Min.	Typ.	Max.
Supply voltage (D.C.)			7.0 V	Operating	0		+75°C
Supply voltage (surge, 1 sec)			12.0 V	Storage	-65		+200°C
Supply voltage (operating)	4.5	5.0	6.0 V	Thermal gradient, junction to air (θ_{ja}) (Flat Pack)			0.3°C/mW
Input voltage			5.5 V	Thermal gradient, junction to air (θ_{ja}) (Plug-in)			0.15°C/mW
Output voltage			5.5 V	Power Dissipation (50% Duty Cycle, $V_{CC} = +5V$)	77		mW/Circuit

ELECTRICAL SPECIFICATIONS

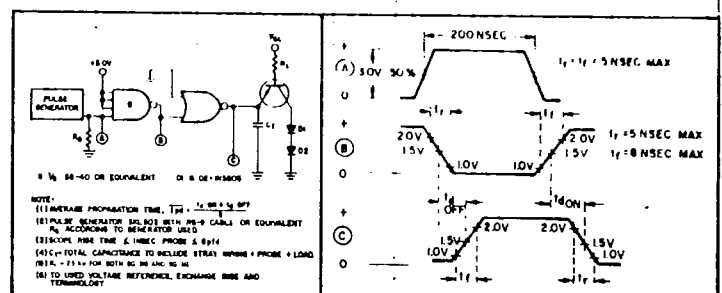
Values at Specified Temperatures						Fig. No.
Characteristics at $V_{CC} = +5.0 V$	Symbol	0°C	+25°C	+75°C	Units	
INPUT:						
Input Load Current @ $V_{IN} =$ Other Inputs	I_{IN}	2.5 0 0	2.5 0 0	2.5 0 0	mA Max. Volts Volts	1
Input Leakage Current @ $V_{IN} =$ Other Inputs	I_{IN}	0.1 4.5 0	0.1 4.5 0	0.1 4.5 0	mA Max. Volts Volts	2
Input (OFF Level) Breakdown Voltage $I_{IN} =$ Other Inputs	BV_{IN} "1"	5.5 1.0 0	5.5 1.0 0	5.5 1.0 0	Volts mA Max. Volts	2
Logic "1" Threshold Voltage $V_{OUT} =$ I_{OUT} (SG 342) I_{OUT} (SG 343)	V_{MIN} "1"	1.9 0.45 22.5 12.5	1.8 0.45 22.5 12.5	1.7 0.45 22.5 12.5	Volts Volts Max. mA mA	7
Logic "0" Threshold Voltage $V_{OUT} =$ I_{OUT} (SG 342) I_{OUT} (SG 343)	V_{MAX} "0"	1.0 2.5 1.8 1.0	1.1 2.4 1.8 1.0	1.0 2.5 1.8 1.0	Volts Volts Min. mA mA	8
OUTPUT:						
Output Leakage Current @ $V_{OUT} =$ Inputs	I_{OUT}	0.25 5.5 0	0.25 5.5 0	0.25 5.5 0	mA Max. Volts Volts	4
Output Short Circuit Current @ Input	I_{OUT}	25 100 0	25 100 0	25 100 0	mA Min. mA Max. Volts	6
Logic "0" Level @ $V_{IN} =$ I_{OUT} (SG 342) I_{OUT} (SG 343)	V_{OUT} "0"	0.40 2.9 22 12	0.40 2.9 22 12	0.45 2.9 22 12	Volts Max. Volts mA mA	7
Logic "1" Level @ $V_{IN} =$ I_{OUT} (SG 342) I_{OUT} (SG 343)	V_{OUT} "1"	2.9 0.45 1.8 1.0	3.0 0.45 1.8 1.0	3.0 0.45 1.8 1.0	Volts Min. Volts mA mA	8
POWER REQUIREMENTS:						
Breakdown Current @ $V_{CC} =$ @ $V_{IN} =$	I_{CC}		44.0 7.0 0		mA Max. Volts Volts	3
"ON" State Current Drain Inputs	I_{CC} "0"	48.0 Open	48.0 Open	48.0 Open	mA Max.	5
"OFF" State Current Drain Inputs	I_{CC} "1"	30.0 0	30.0 0	30.0 0	mA Max. Volts	3

TYPICAL TEST CONFIGURATION



SWITCHING SPECIFICATIONS

Switching Parameters	CONDITIONS				LIMITS	
	V_{CC} volts	T_A °C	Fanout		C_T pfd.	Time—nsec Max.
			SG342	SG343		
Turn On Delay	+5.0	+25	1	1	15	10
Turn Off Delay			1	1	15	10
Rise Time Note 6			1	1	15	2.5
Fall Time Note 6			1	1	15	4.0



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