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Record of Revision

Date	Revision No.	Summary
2013 03 05	1.0	Rev 1.0 was issued(update the temperature range)

1. Scope

This data sheet is to introduce the specification of SG1010AZG-T-1 active matrix TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC, Touch panel and a backlight unit. The 10.1″ display area contains 1024(RGB) x 600 pixels.

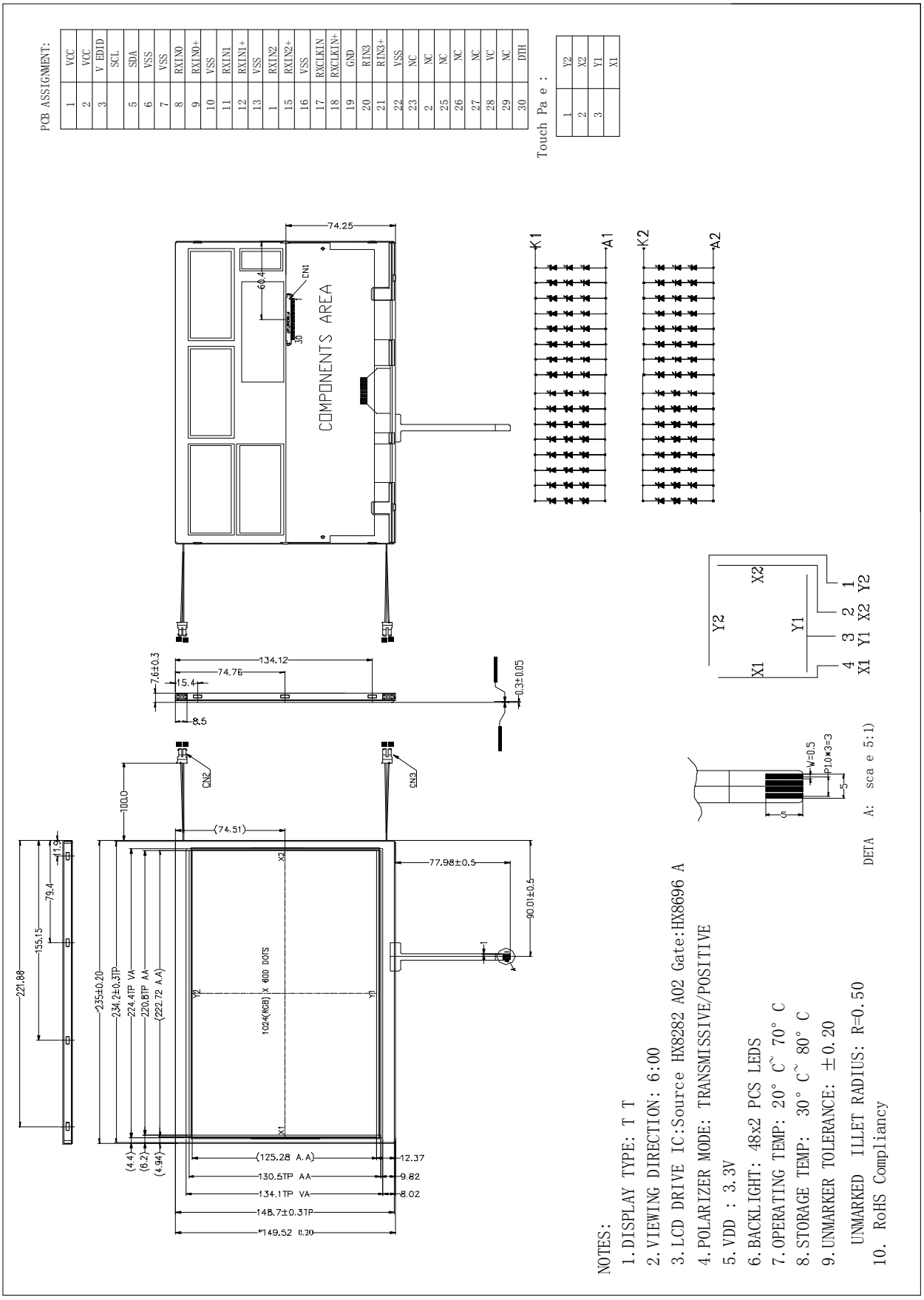
2. Application

Digital equipments which need color display,mobile navigator/video systems.

3. General Information

Item	Contents	Unit
Size	10.1	inch
Resolution	1024(RGB) x 600	/
Interface	LVDS	/
Technology type	a-Si TFT	/
Pixel pitch	0.0722X0.2192	mm
Pixel Configuration	RGB stripes	
Outline Dimension (W x H x D)	235.0 x 149.52 x 7.6	mm
Active Area	222.72 x 125.28	mm
Display Mode	Transmissive Normally White	/
Backlight Type	LED	/

4. Outline Drawing



5. Interface signals

Pin No.	Symbol	I/O	Description	Remark
1	VCC	P	POWER Supply	
2	VCC	P	POWER Supply	
3	V-EDID	P	Power Supply for EDID EEPROM(3.3V)	
4	SCL	I	EDID	
5	SDA	I	EDID	
6	VSS	P	Power	
7	VSS	P	Power	
8	RIN0-	I	- LVDS differential data input	
9	RIN0+	I	+LVDS differential data input	
10	VSS	P	Power	
11	RIN1-	I	- LVDS differential data input	
12	RIN1+	I	+LVDS differential data input	
13	VSS	P	Power	
14	RIN2-	I	- LVDS differential data input	
15	RIN2+	I	+LVDS differential data input	
16	VSS	P	Power	
17	RXCLKIN-	I	- LVDS differential clock input	
18	RXCLKIN+	I	+LVDS differential clock input	
19	VSS	P	Power	
20	RIN3-	I	- LVDS differential data input	
21	RIN3+	I	+LVDS differential data input	
22	VSS	P	Power	
23	NC	I	No connection	
24	NC	I	No connection	
25	NC	I	No connection	
26	NC	I	No connection	
27	NC	I	No connection	
28	NC	I	No connection	
29	NC	I	No connection	
30	DTH	-	Dithering function	

Note: 1、Recommend connector Part No: MDF76KBW-30S-1H or equivalent.
2、User's connector Part No.: MDF76-30P-1Cor equivalent

CN2/CN3 (LED connector)

Pin No.	Symbol	I/O	Description	Wire Color
1	A1/A2	P	LED Anode	red
2	K1/K2	P	LED Cathode	white

Note： Connector part NO is BHSR-02VS-1

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Item		Symbol	Min.	Max.	Unit	Remark
Supply Voltage for Source Driver	Analog	AVDD	-0.5	+13.5	V	-
	Digital	VCC	-0.5	+5.0		-
Supply Voltage for Gate Driver	Positive	VGH	-0.3	+40	V	-
	Negative	VGL	-20	+0.3		-
	-	VGH-VGL	-0.3	+40		-
Gamma Reference Voltage		V1~V7	0.4 AVDD	AVDD+0.3	-	-
		V8~V14	-0.3	0.6 AVDD	-	-
Analog Input Voltage		VIN	-0.3	AVDD +0.3	V	-

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	70	℃	
Storage Temperature	TSTG	-30	80	℃	

7. Electrical Specifications

7.1 Electrical characteristics

GND=0V, Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Digital Power Supply	VCC	3.1	3.3	3.5	V	-
Analog Power Supply	AVDD	6.5	10.5	13.5	V	-
Gate on Power	VGH	-	+21	-	V	-
Gate on Current	IVGH	-	-	100	μA	-
Gate off Power	VGL	-	-8	-	V	-
Gate off Current	IVGL	-	-	100	μA	-
Common Electrode Voltage	VCOM	-	+3.5	-	V	-
Frame Frequency	fFRAME	-	60	90	Hz	-

7.2 LED Backlight

Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Voltage	VL	9.0	9.6	10.2	V	-
LED Current	IL	-	640		mA	Note 7-1
Power Consumption	PLED	-	2.5	-	W	Note 7-2

Note :
7-1: The LED driving condition is 20mA for each LED;
7-2: PLED is a calculated reference value (IL × VL);

8. Command/AC Timing

8.1. Timing Conditions

8.1.1. Source Driver Timing Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK frequency	Fclk	-	40	45	MHz	EDGSL = '0'
	Fclk		20	22.5	MHz	EDGSL = '1'
CLK pulse width	Tcw	40%	-	60%	Tcph	
Data set-up time	Tsu	4	-	-	ns	D00 ~ D25, REV and DIO1/2 to CLK
Data hold time	Thd	2	-	-	ns	D00 ~ D25, REV and DIO1/2 to CLK
Propagation delay of DIO2/1	Tphl	6	10	15	ns	CL=25pF (Output)
Time that the last data to LD	Tld	1	-	-	Tcph	
Pulse width of LD	Twld	2	-	-	Tcph	
Time that LD to DIO1/2	Tlds	5	-	-	Tcph	
POL set-up time	Tpsu	6	-	-	ns	POL to LD
POL hold time	Tphd	6	-	-	ns	POL to LD
Output stable time	Tst	-	-	12	us	10% or 90% target voltage. CL=60pF, R=2K ohm

8.1.2. Gate Driver Timing Conditions

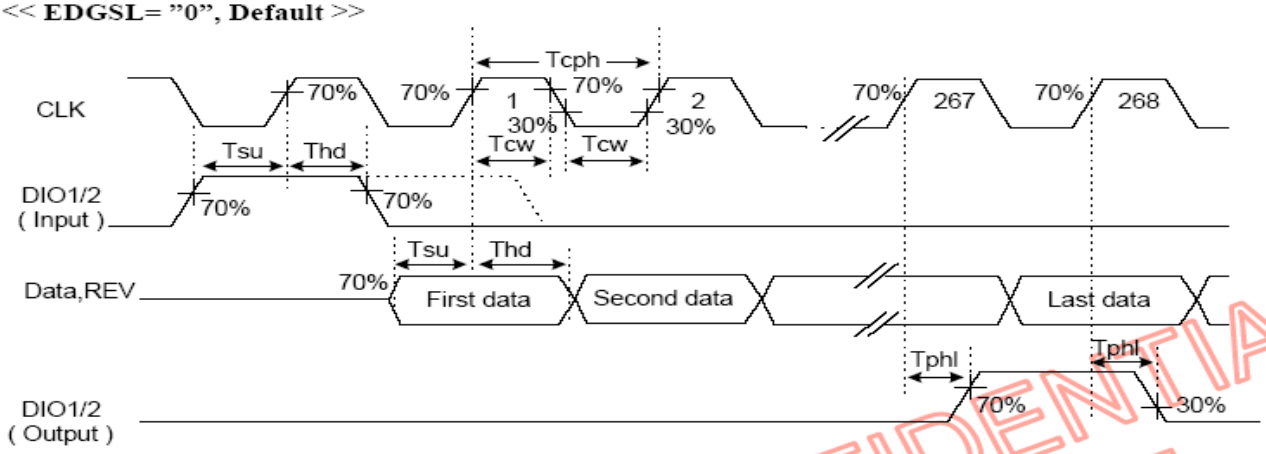
Symbol	Parameters	Min.	Typ.	Max.	Unit	Conditions
Tdt	STVD/STVU Delay Time	-	-	500	ns	CL = 20pF
Tdo	Driver Output Delay Time	-	-	900	ns	CL = 220pF
Tthl	Output Falling Time	-	400	800	ns	CL = 220pF, 90% to 10%
Ttlh	Output Rise Time	-	500	1000	ns	CL = 220pF, 10% to 90%
Txon	XON to Driver Output Delay Time	-	-	10	us	CL = 220pF
Toe	OEx to Driver Output Delay Time	-	-	900	ns	CL = 220pF
Fclk	Clock Frequency	-	-	200	KHz	In cascade connection
Trck	Clock Rise Time	-	-	100	ns	CL = 20pF
Tfck	Clock Falling Time	-	-	100	ns	CL = 20pF
PWCLK	Clock Pulse Width (High & Low)	500	-	-	ns	
Tsu	STVD/STVU Set-up Time	200	-	-	ns	
Thd	STVD/STVU Hold Time	300	-	-	ns	
Twcl	Output Enabled pulse width	1	-	-	us	

Note: Here OEx indicates OEV signal

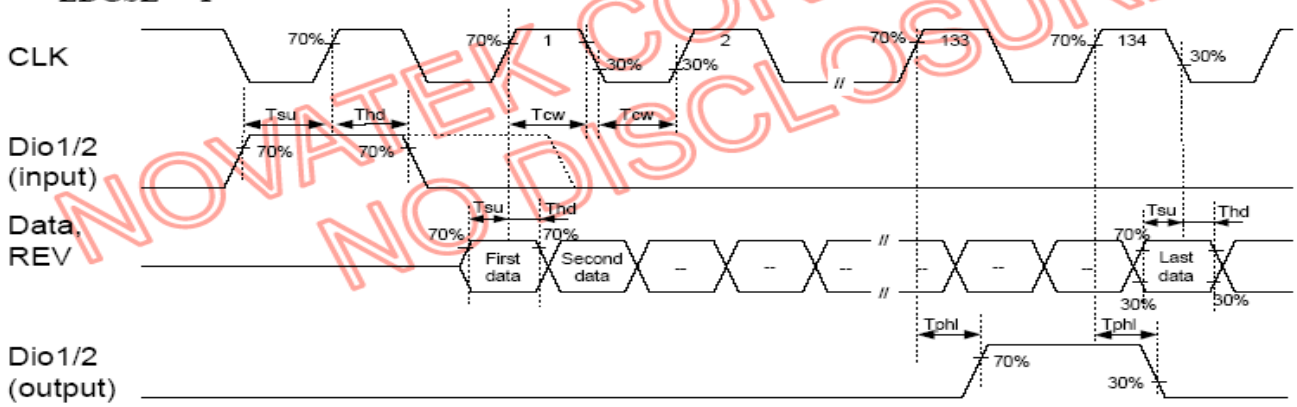
8.2. Timing Diagram

8.2.1 Source Driver Timing Diagram1 (CHNSL="11" ,CHDNS="0", Default)

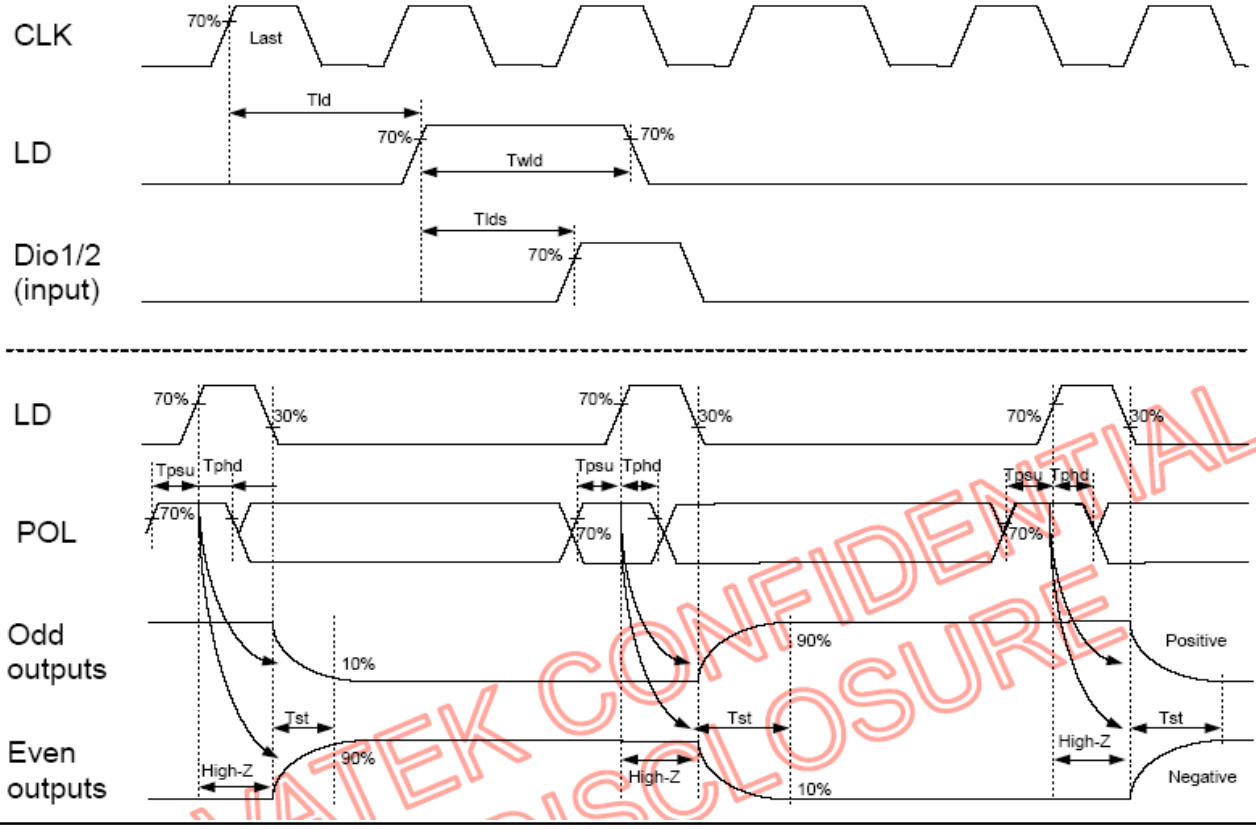
<< EDGSL= "0", Default >>



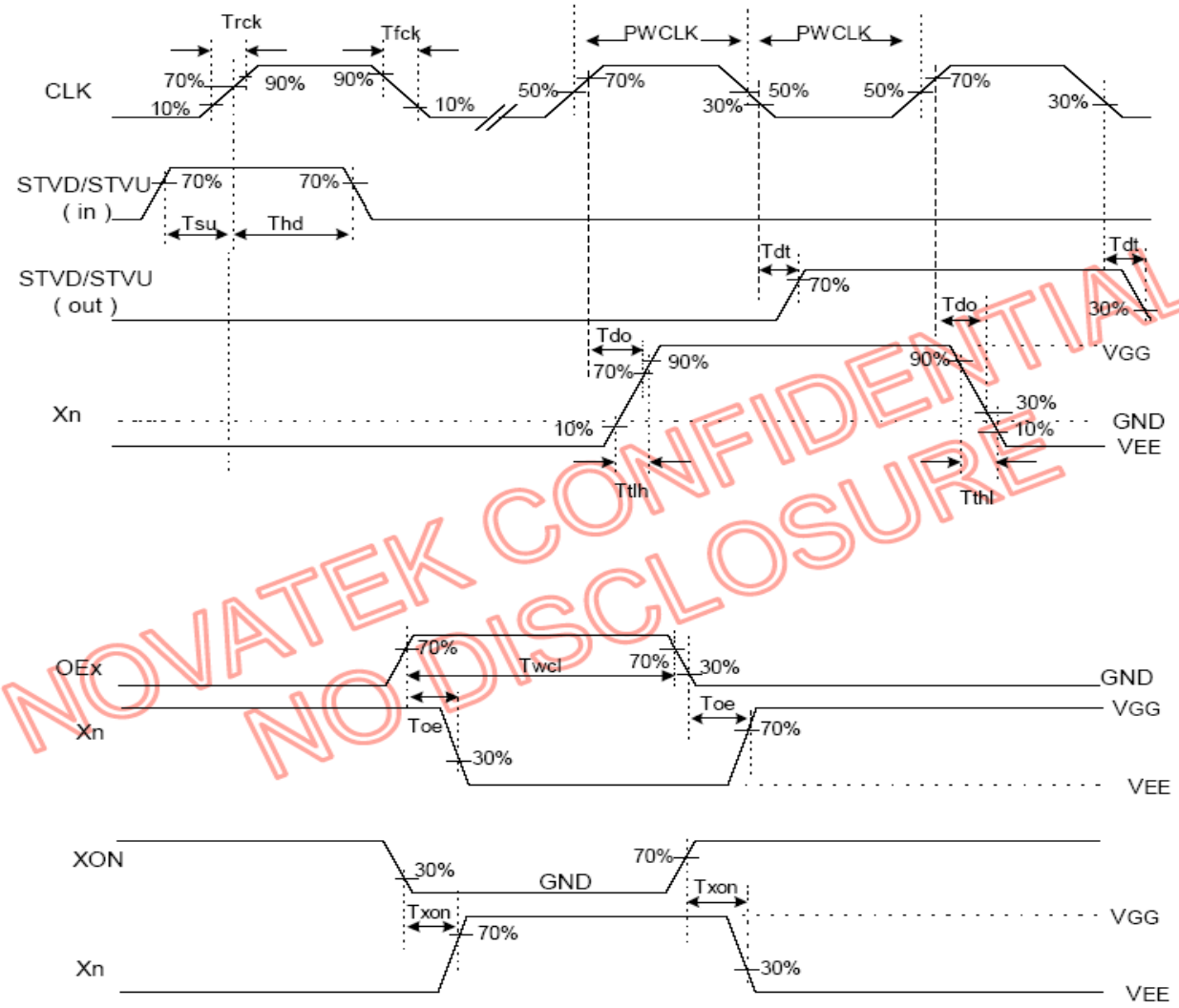
<< EDGSL= "1">>



8.2.2 Source Driver Timing Diagram2

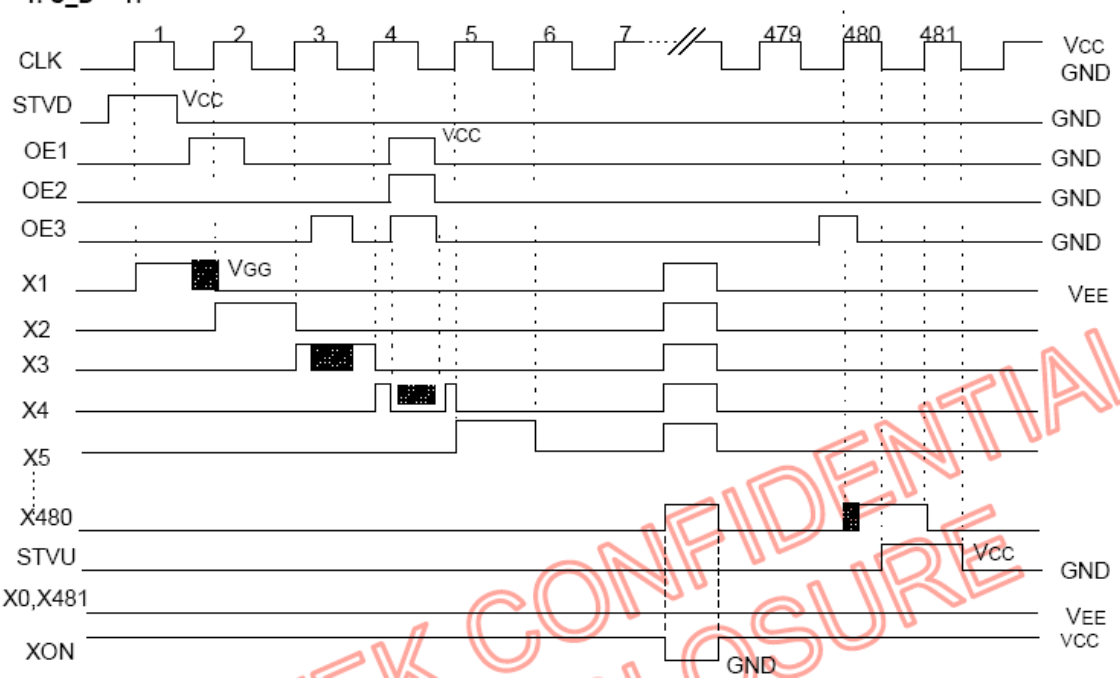


8.2.3 Gate Driver Timing Diagram



Note: Here Xn indicates driving LCD's gate signals

1. U_D = 'H'



Note: Here VEE indicates VGL signal, VGG indicates VGH signal;
OE1 OE2 OE3 connect together to OEV on the panel.

8.3. Power Sequence (Voltage Source)

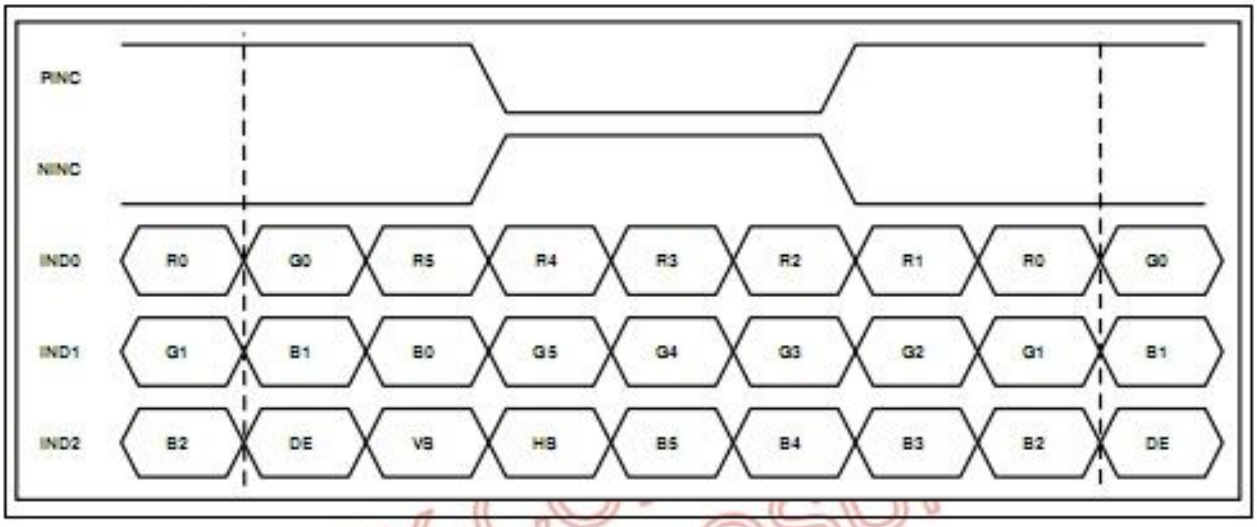
To prevent the device damage from latch up, the power ON/OFF sequence shown below must be followed:

When power on: VCC->VGL-> AVDD ->VGH

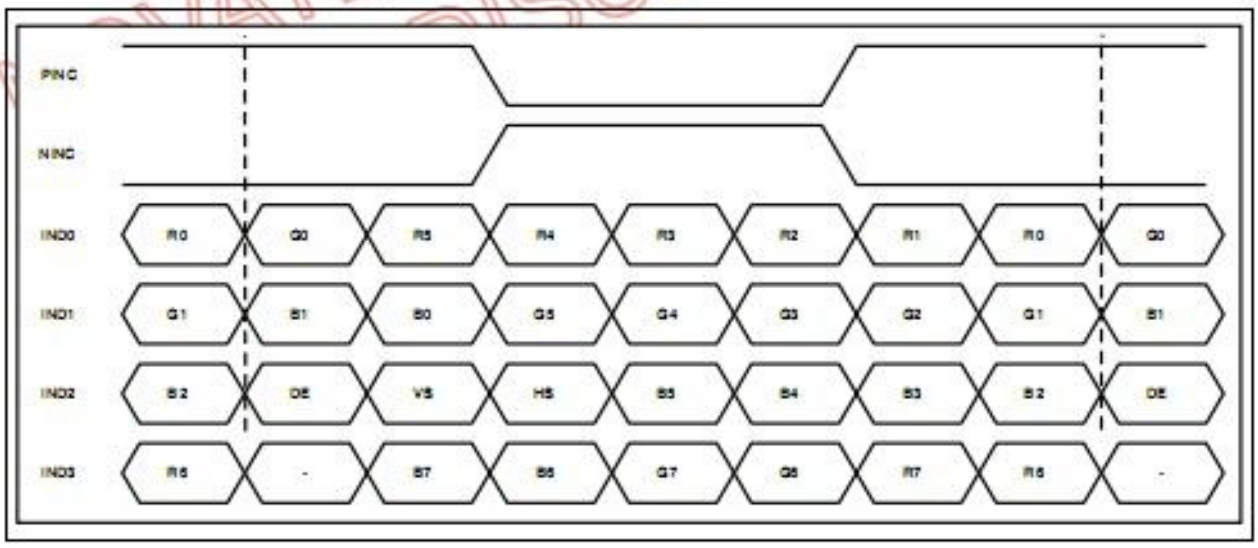
When power off: VGH-> AVDD ->VGL->VCC

8.3.1 Data input for LVDS

6bit LVDS input (HSD='H')

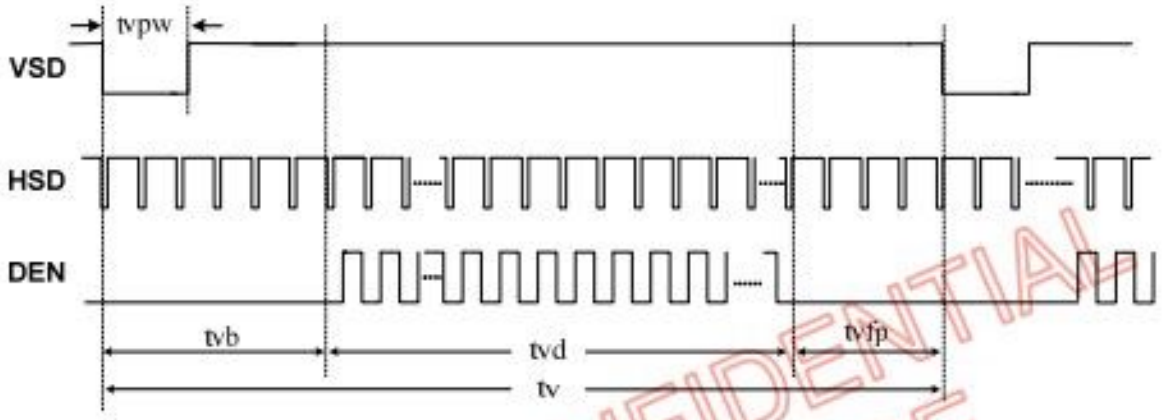


8-bit LVDS input (HSD='L')

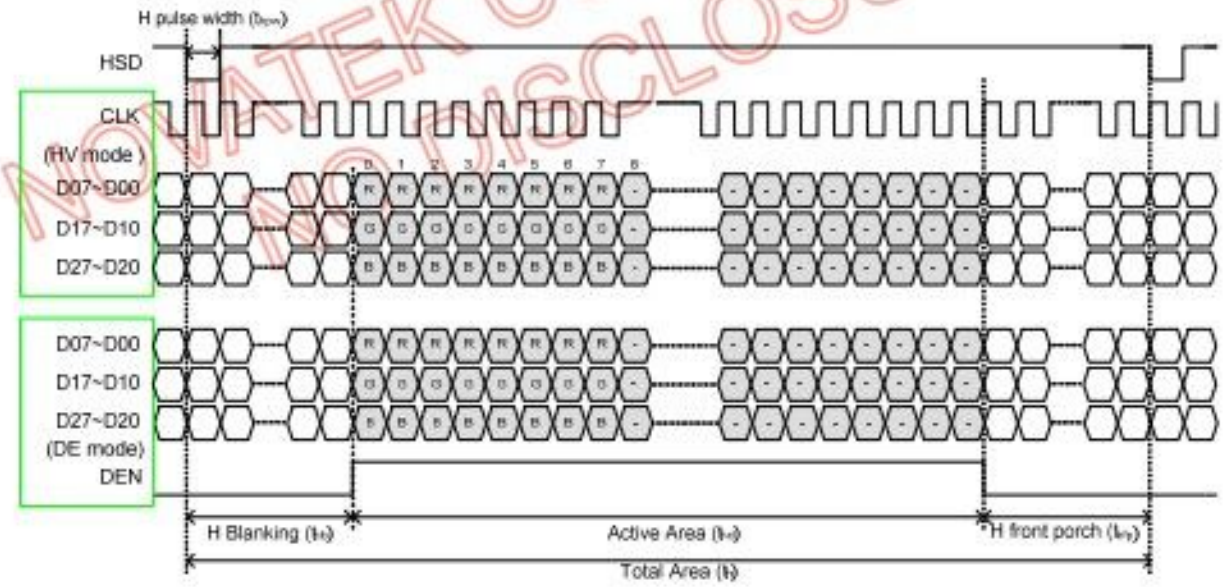


8.3.2 Data input for TTL

Vertical input timing



Horizontal input timing



For 1024x600 panel

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @ Frame rate = 60Hz	fclk	40.8	51.2	67.2	MHz
Horizontal display area	thd		1024		DCLK
HSYNC period time	th	1114	1344	1400	DCLK
HSYNC blanking	thb+thfp	90	320	376	DCLK
Vertical display area	tvd		600		H
VSYNC period time	tv	610	635	800	H
VSYNC blanking	tvb+tvfp	10	35	200	H

HV mode

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		1024		DCLK
DCLK frequency @ Frame rate = 60Hz		fclk	Min.	Typ.	Max.	
			44.9	51.2	63	MHz
1 Horizontal Line		th	1200	1344	1400	DCLK
HSYNC pulse width	Min.	thpw		1		
	Typ.			-		
	Max.			140		
HSYNC blanking		thb	160	160	160	
HSYNC front porch		thfp	16	160	216	

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		600		H
VSYNC period time	tv	624	635	750	H
VSYNC pulse width	tvpw	1	-	20	H
VSYNC Blanking (tvb)	tvb	23	23	23	H
VSYNC Front porch (tvfp)	tvfp	1	12	127	H

9 Optical Specification

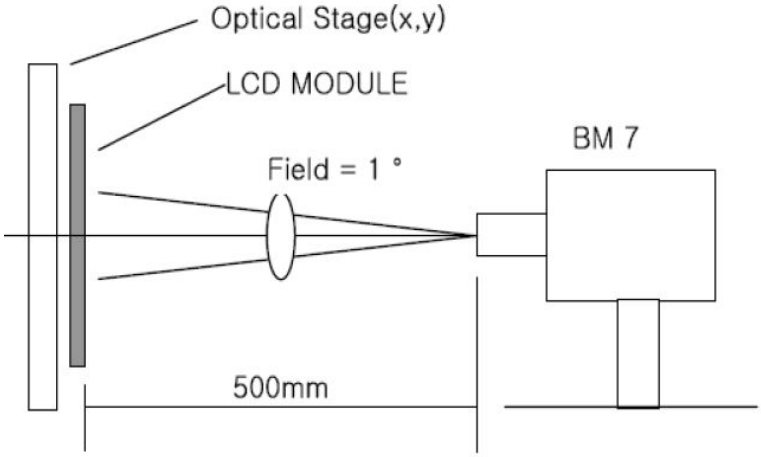
Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°		250			Note1 Note2
Response Time		Ton/ Toff	25℃				ms	Note1 Note3
View Angles		ΘT	CR≧10		85		Degree	Note 4
		ΘB			50			
		ΘL			85			
		θR			85			
Chromaticity	White	x	Brightness is on		TBD			Note5, Note1
		y			TBD			
Luminance		L			800		cd/m^2	Note1 Note6
Uniformity		U			80		%	Note1 Note7

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

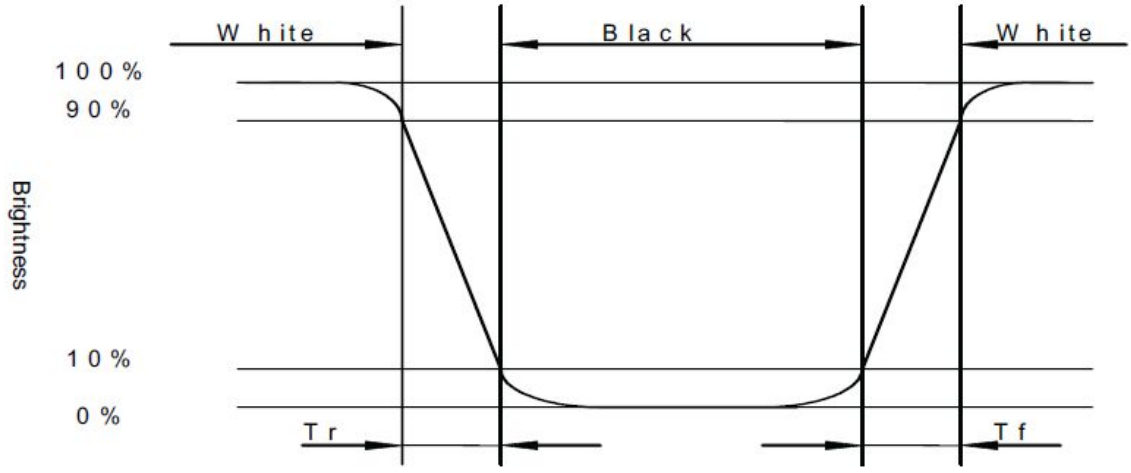


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

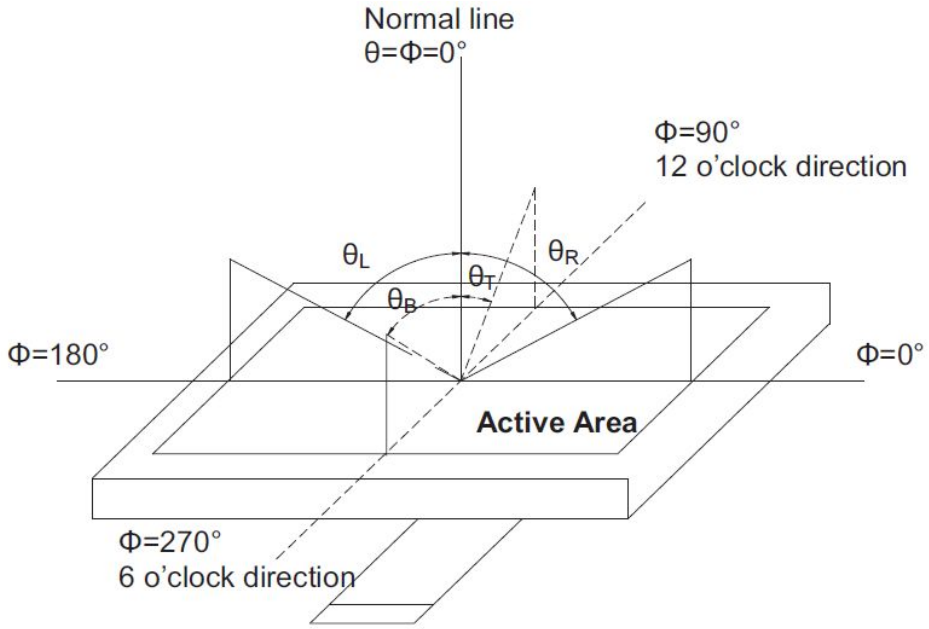
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



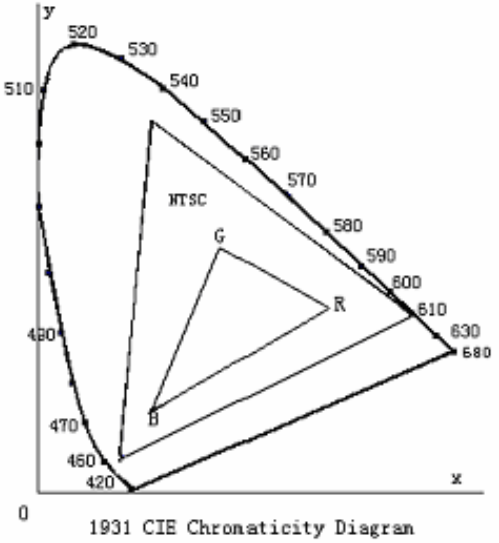
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



$$S \quad \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity (U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

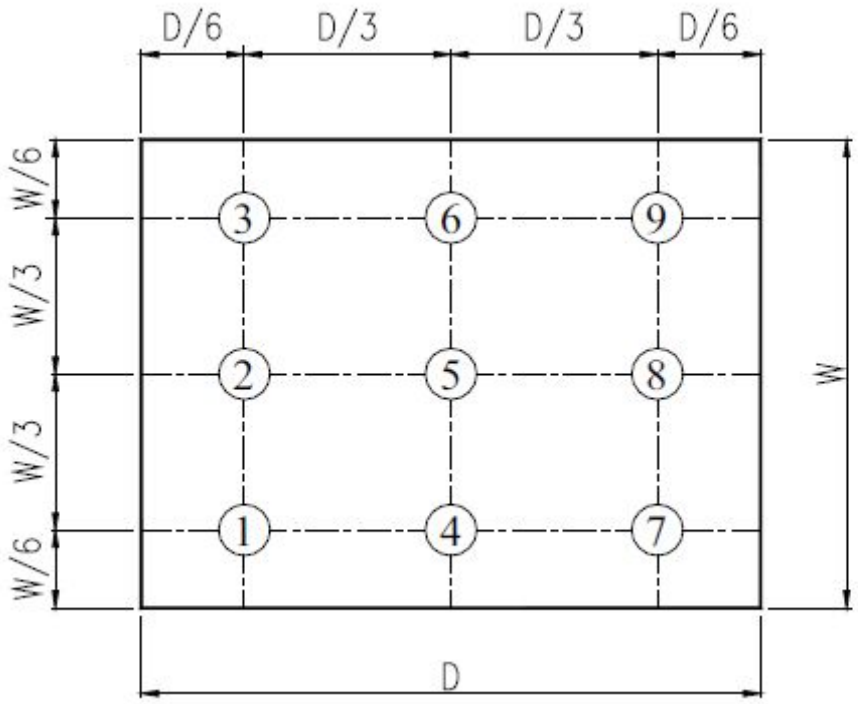


Fig. 2 Definition of uniformity

10 Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+70℃, 120hrs	Per table in below
2	Low Temp Operation	Ta= 20℃, 120hrs	Per table in below
3	High Temp Storage	Ta=+80℃, 120hrs	Per table in below
4	Low Temp Storage	Ta= 30℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+40℃, 90% RH 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non operation)	20℃ 30 min~+60℃ 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω，5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11 Precautions for Use of LCD Modules

11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the LCD module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

A. Store the products in a dark place at +25℃ 10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.