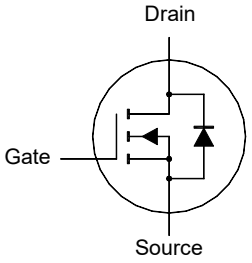
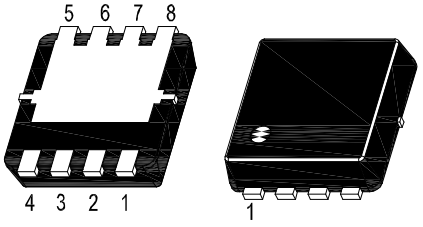
SFTN7422SMP-HAF

N-Channel Enhancement Mode MOSFET

Features

- Low Gate Charge
- Very Low $R_{DS(on)}$
- Halogen and Antimony Free(HAF), RoHS compliant





1. Source 2. Source 3. Source 4. Gate
5. Drain 6. Drain 7. Drain 8. Drain
DFN3030 Plastic Package

Application

- DC/DC Converters

Key Parameters

Parameter	Value	Unit
BV_{DSS}	30	V
$R_{DS(ON)}$ Max	4 @ V_{GS} = 10 V	mΩ
	6.8 @ V_{GS} = 4.5 V	mΩ
$V_{GS(th)}$ typ	1.7	V
Qg typ	62	nC

Absolute Maximum Ratings(at Ta = 25℃ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	30	V
Drain-Gate Voltage		V_{GS}	± 20	V
Drain Current-Continuous	T_c = 25℃ T_c = 100℃	I_D	34 27	A
Peak Drain Current, Pulsed [3]		I_{DM}	136	A
Drain Current-Continuous	T_a = 25℃ T_a = 70℃	I_{DSM}	21 17	A
Power Dissipation [2]	T_c = 25℃ T_c = 100℃	P_D	31 12	W
Power Dissipation [1]	T_a = 25℃ T_a = 70℃	P_{DSM}	3.1 2	W
Avalanche Current	L = 0.1 mH	I_{AS}	38	A
Avalanche Energy	L = 0.1 mH	E_{AS}	72.2	mJ
Operating Junction and Storage Temperature Range		T_j, T_{stg}	- 55 to + 150	℃

Thermal Characteristics

Parameter		Symbol	Max.	Unit
Thermal Resistance-Junction to Ambient [1]	t ≤ 10 s	$R_{\theta JA}$	40	℃/W
Thermal Resistance-Junction to Ambient [1] [4]		$R_{\theta JA}$	75	℃/W
Thermal Resistance-Junction to Case		$R_{\theta JC}$	4	℃/W

[1] The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_a = 25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t ≤ 10 s value and the maximum allowed junction temperature of 150°C.

[2] The power dissipation P_D is based on $T_{J(MAX)}$ = 150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

[3] Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ = 150°C.

[4] The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

Dated: 03/07/2020 Rev: 05

Characteristics at T_a = 25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I_D = 250 µA	BV_{DSS}	30	-	-	V
Gate-Source Threshold Voltage at V_{DS} = V_{GS}, I_D = 250 µA	$V_{GS(th)}$	1.2	-	2.2	V
Drain-Source Leakage Current at V_{DS} = 30 V	I_{DSS}	-	-	1	µA
Gate-Source Leakage Current at V_{GS} = ± 16 V	I_{GSS}	-	-	± 100	nA
Drain-Source On-State Resistance at V_{GS} = 10 V, I_D = 20 A at V_{GS} = 4.5 V, I_D = 16 A	$R_{DS(on)}$	- -	- -	4 6.8	mΩ
DYNAMIC PARAMETERS					
Forward Transconductance at V_{DS} = 5 V, I_D = 20 A	g_{FS}	-	40	-	S
Gate Resistance at V_{GS} = 0 V, V_{DS} = 0 V, f = 1MHz	R_g	-	1	3	Ω
Input Capacitance at V_{GS} = 0 V,V_{DS} = 15 V, f = 1 MHz	C_{iss}	-	3520	-	pF
Output Capacitance at V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz	C_{oss}	-	459	-	pF
Reverse Transfer Capacitance at V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz	C_{rss}	-	420	-	pF
Gate Charge Total at V_{DS} = 15 V, I_D = 20 A, V_{GS} = 10 V at V_{DS} = 15 V, I_D = 20 A, V_{GS} = 4.5 V	Q_g	- -	62 31	- -	nC
Gate to Source Gate Charge at V_{DS} = 15 V, I_D = 20 A, V_{GS} = 10 V	Q_{gs}	-	9	-	nC
Gate to Drain Charge at V_{DS} = 15 V, I_D = 20 A, V_{GS} = 10 V	Q_{gd}	-	13	-	nC
Turn-On Delay Time at V_{GS} = 10 V, V_{DS} = 15 V, R_L = 0.75 Ω, R_{GEN} = 3 Ω	$t_{d(on)}$	-	7	-	ns
Turn-On Rise Time at V_{GS} = 10 V, V_{DS} = 15 V, R_L = 0.75 Ω, R_{GEN} = 3 Ω	t_r	-	8.3	-	ns
Turn-Off Delay Time at V_{GS} = 10 V, V_{DS} = 15 V, R_L = 0.75 Ω, R_{GEN} = 3 Ω	t_{off}	-	24	-	ns
Turn-Off Fall Time at V_{GS} = 10 V, V_{DS} = 15 V, R_L = 0.75 Ω, R_{GEN} = 3 Ω	t_f	-	10	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at V_{GS} = 0 V, I_S = 1 A	V_{SD}	-	-	1	V

Ratings and Electrical Characteristics Curves

Fig. 1 Typical Output Characteristic

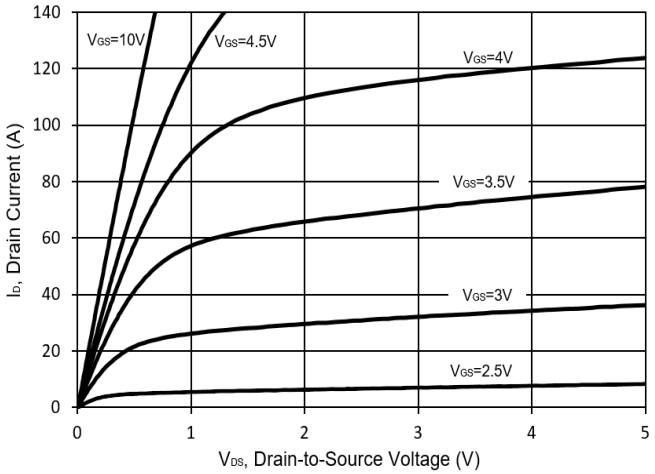


Fig. 2 Typical Transfer Characteristic

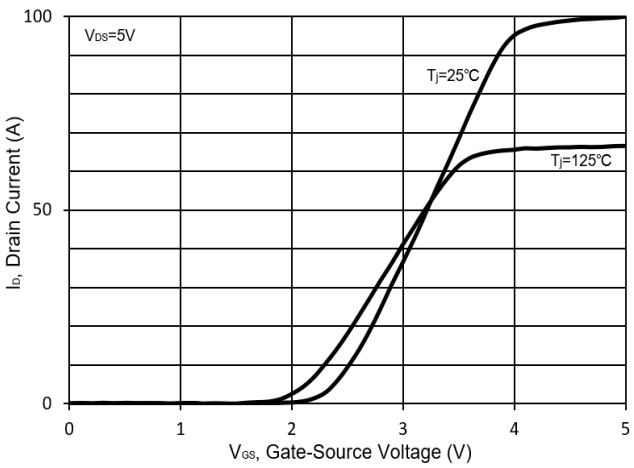


Fig. 3 on-Resistance vs. Gate Voltage

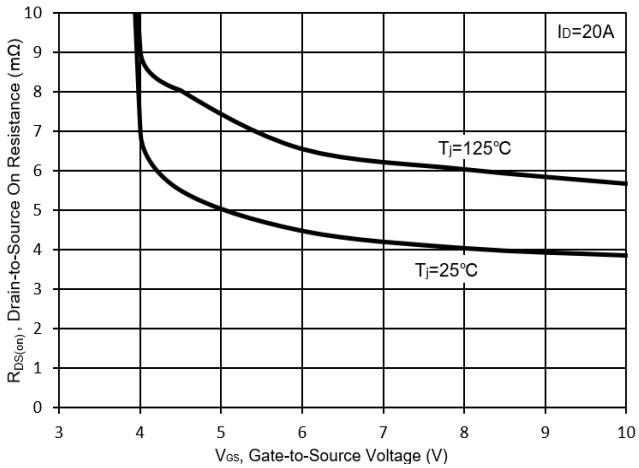


Fig. 4 on-Resistance vs.T_j

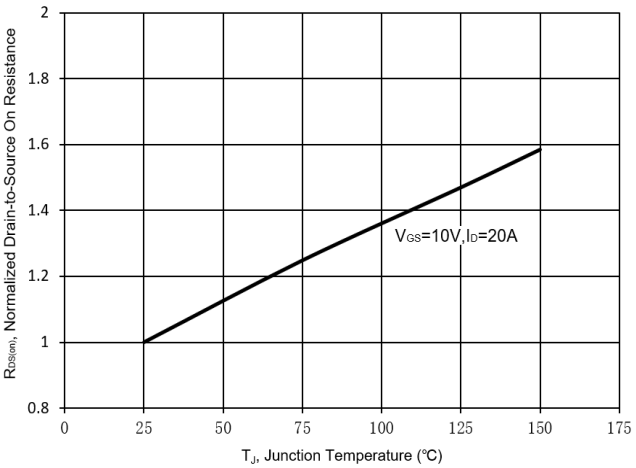


Fig. 5 Drain Source vs. on-Resistance

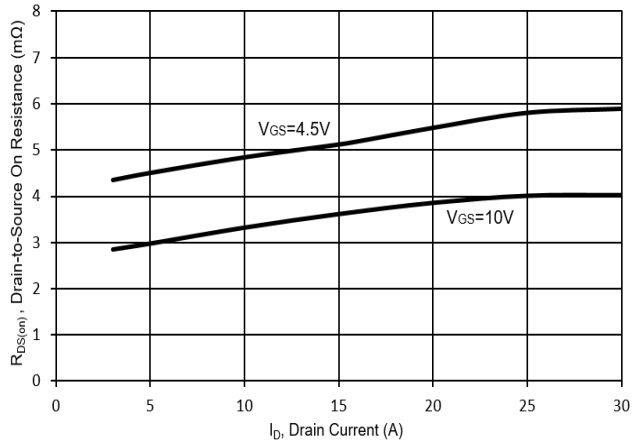
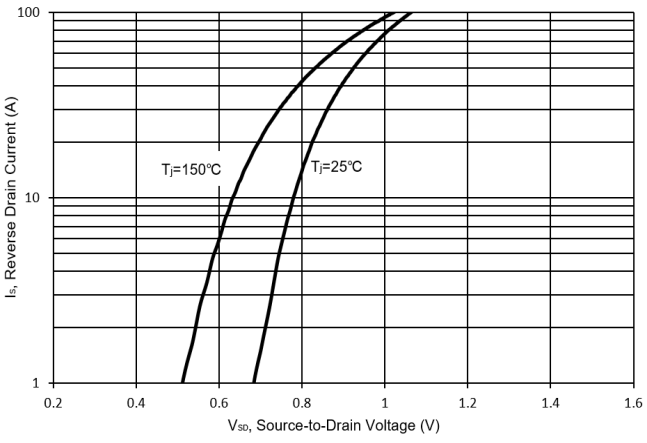


Fig. 6 Typical Forward Characteristic



Ratings and Electrical Characteristics Curves

Fig. 7 $V_{(BR)DSS}$ vs. Junction Temperature

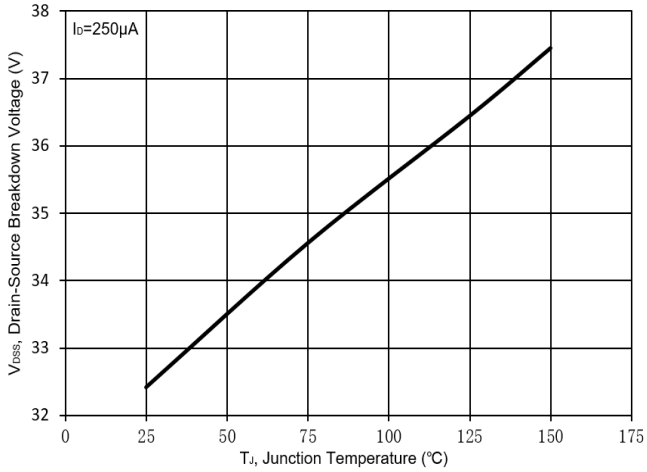


Fig. 8 Gate Threshold Variation vs. T_j

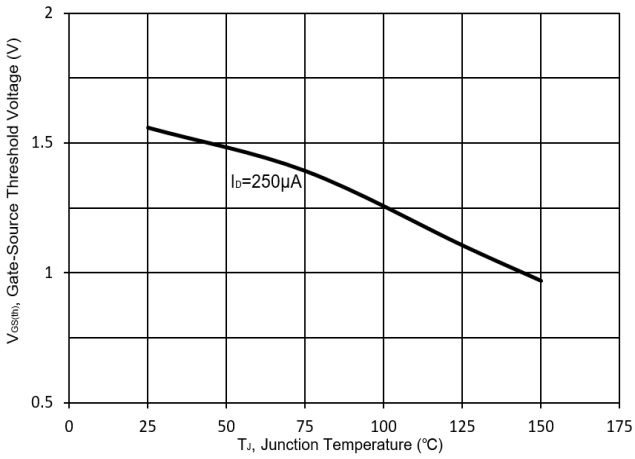


Fig. 9 Typical Junction Capacitance

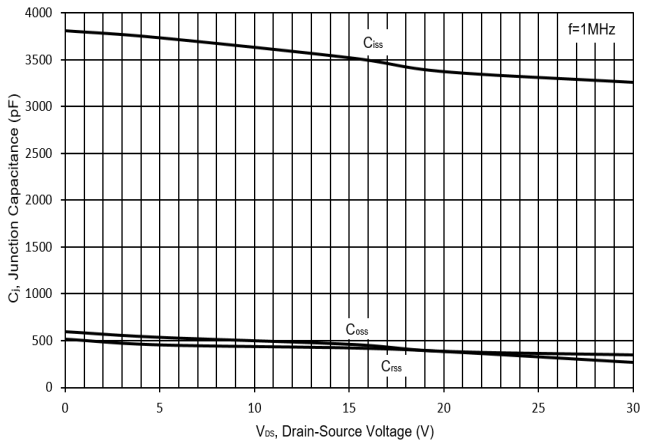


Fig. 10 Gate Charge

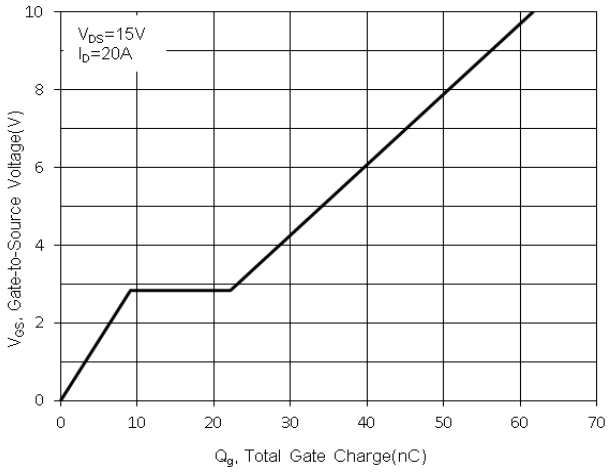


Fig. 11 Drain-Source Leakage Current vs. T_j

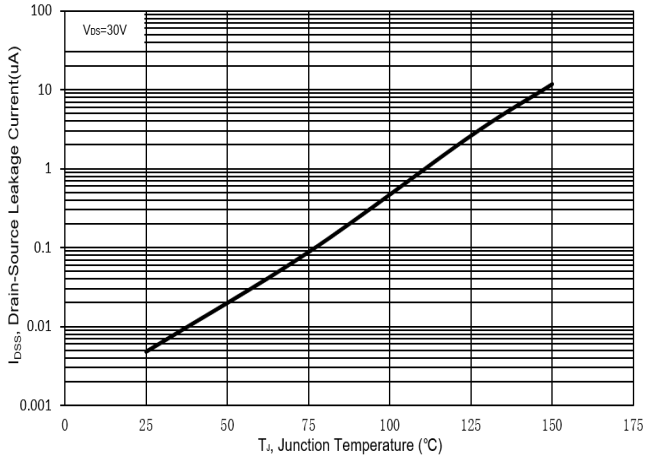
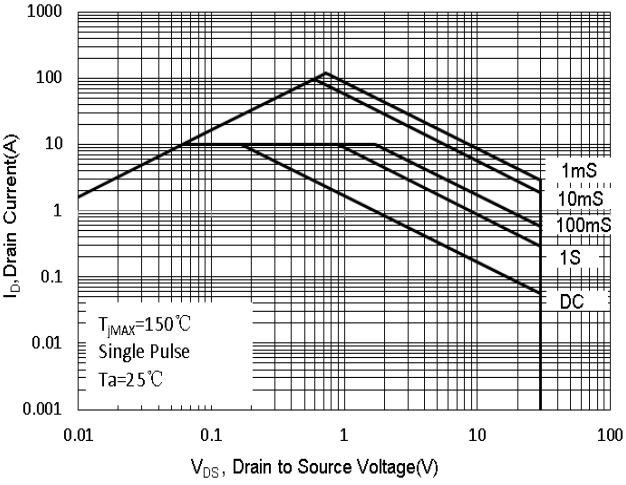


Fig. 12 Safe Operation Area



Test Circuits

Fig.1-1 Switching times test circuit

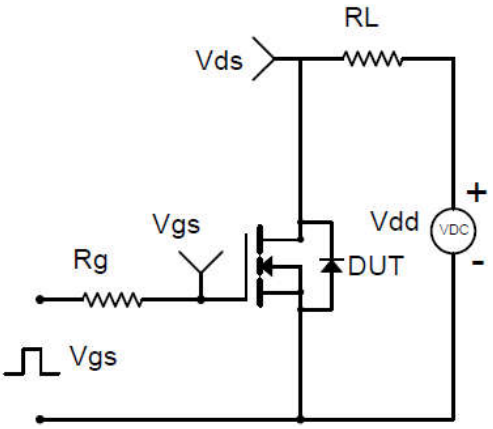


Fig.1-2 Switching Waveform

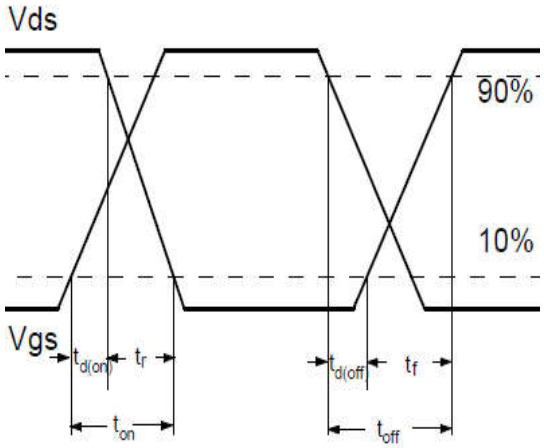


Fig.2-1 Gate charge test circuit

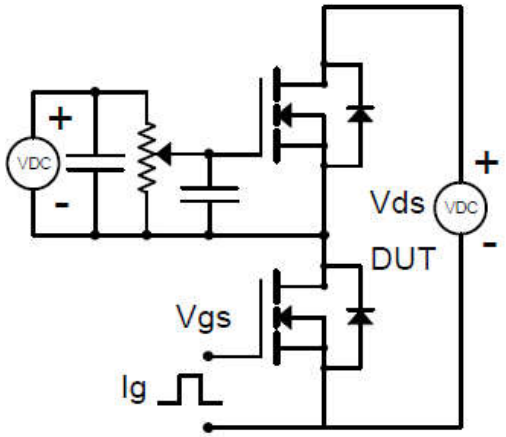


Fig.2-2 Gate charge waveform

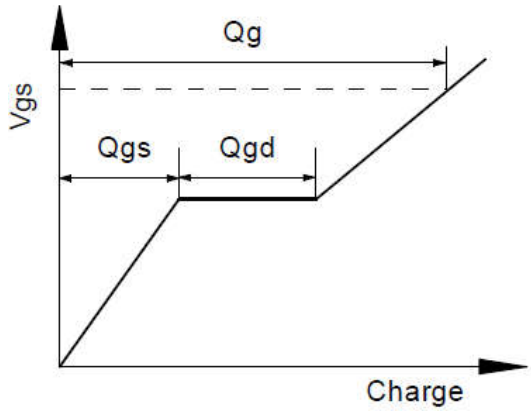


Fig.3-1 Avalanche test circuit

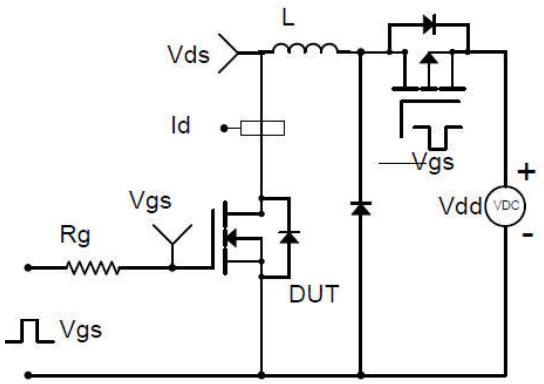
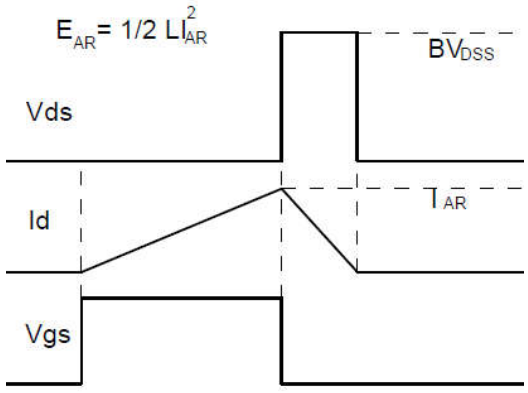
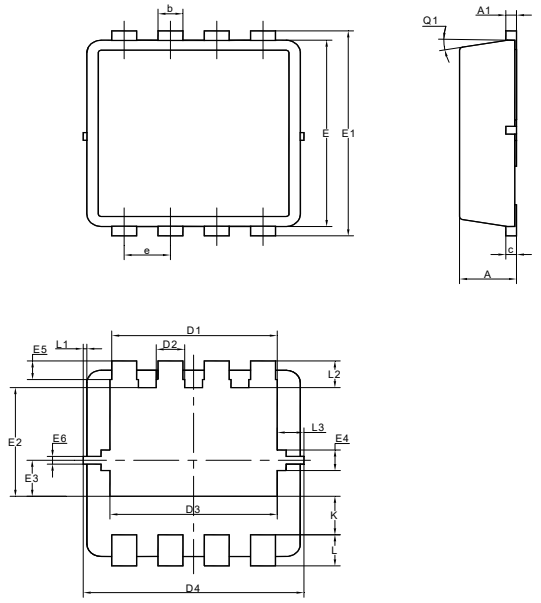


Fig.3-2 Avalanche waveform



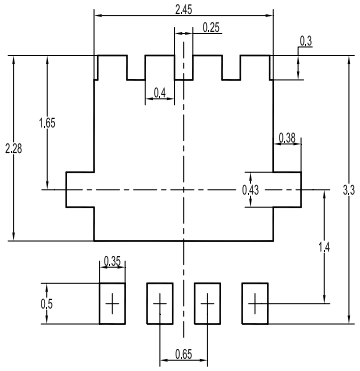
Package Outline Dimensions (Units: mm) DFN3030



UNIT	A	A1	b	c	D	D1	D2	D3	D4	E	E1	E2	E3
mm	0.9	0.05	0.35	0.25	3.1	2.45	0.5	2.7	3.2	3.1	3.3	1.85	0.68
	0.7	0	0.24	0.1	2.9	2.25	0.3	2.5	3	2.9	3.1	1.65	0.48

UNIT	E4	E5	E6	e	K	L	L1	L2	L3	θ1
mm	0.43	0.4	0.175	0.7	0.72	0.5	0.1	0.53	0.475	12°
	0.23	0.2	0.075	0.6	0.52	0.3	0	0.33	0.275	0°

Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
DFN3030	8	4 ± 0.1	0.157 ± 0.004	330	13	5,000

Marking information

" SFTN7422SMP " = Part No.

" ****** " = Date Code Marking

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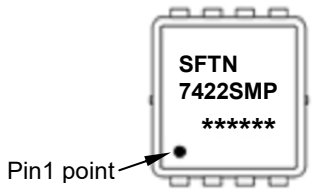

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