High Precision AC/DC PSR Controller for LED Driver

FEATURES

- **Primary Side Regulation (PSR) Control, No Secondary Feedback Circuit Required**
- **1% Precision (@Tj=25 ℃) Internal Reference Voltage for Constant Current (CC) Control**
- **Wide VDD Range (10 to 30V) Eases Flexible LED System Design**
- **Precision LED Output Voltage Clamp**
- **Compensate for Line Voltage Variation and Transformer Inductance Tolerance**
- **Built-in Soft Start**
- **All Pins Floating Protection**
- **LED Open/Short Circuit Protection**
- **PFM Control Eases EMI Design**
- **Cycle-by-Cycle Current Limiting**
- **Built-in Leading Edge Blanking (LEB)**
- **VDD Under Voltage Lockout (UVLO)**
- **Output Over Voltage Protection**
- **VDD OVP & Clamp**

APPLICATIONS

- **LED Luminaries**
- **LED Tube Light**
- **LED PAR30/PAR38, Down Light**
- **GU10/E27 LED Bulb, Spot Light**

GENERAL DESCRIPTION

SFL668 is a high precision AC/DC offline PSR (Primary Side Regulation) controller for LED luminaries. The IC can provide very tight (less than 3%) constant current control (CC) ideal for LED lighting applications.

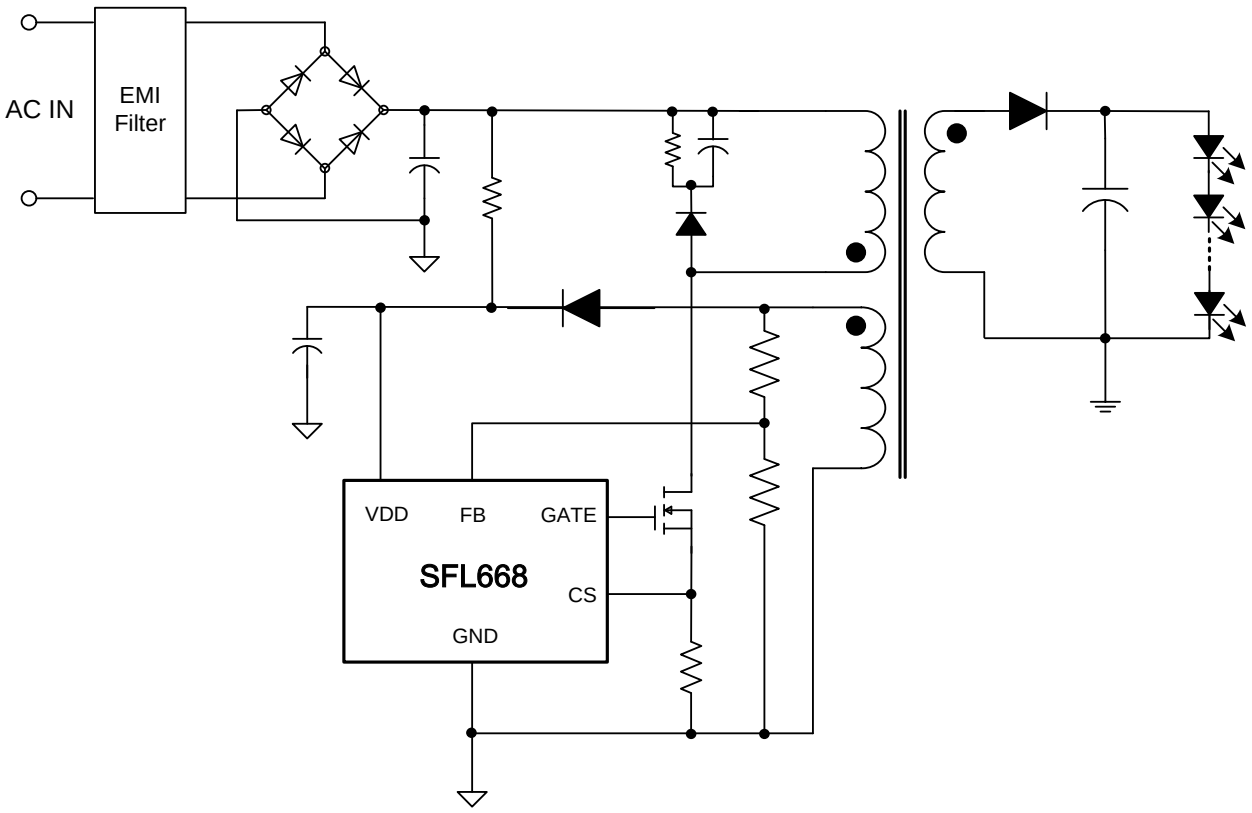
SFL668 uses Pulse Frequency Modulation (PFM) control to improve efficiency and eases system EMI design. The IC dramatically lowers system cost by eliminating secondary feedback circuits.

The wide VDD operating range (10 to 30V, typical) of SFL668 can ease flexible LED system design. The IC also has built-in soft start function to soften the stress on the MOSFET during power on period.

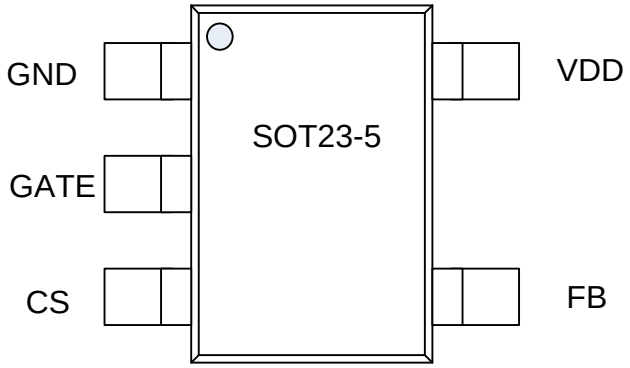
SFL668 integrates functions and protections of Under Voltage Lockout (UVLO), VDD Over Voltage Protection (VDD OVP), LED Open/Short Circuit Protection, Soft Start, Cycle-by-cycle Current Limiting (OCP), All Pins Floating Protection, Gate Clamping, VDD Clamping.

SFL668 is available in SOT23-5 package.

TYPICAL APPLICATION



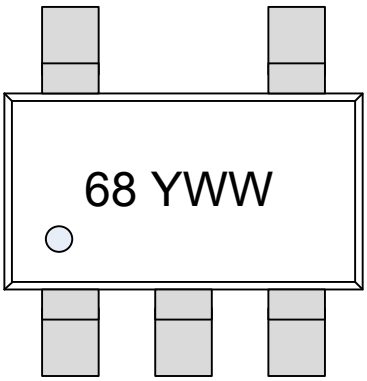
Pin Configuration



Ordering Information

Part Number	Top Mark	Package		Tape & Reel
SFL668LGT	.68YWW	SOT23-5	Green	Yes

Marking Information

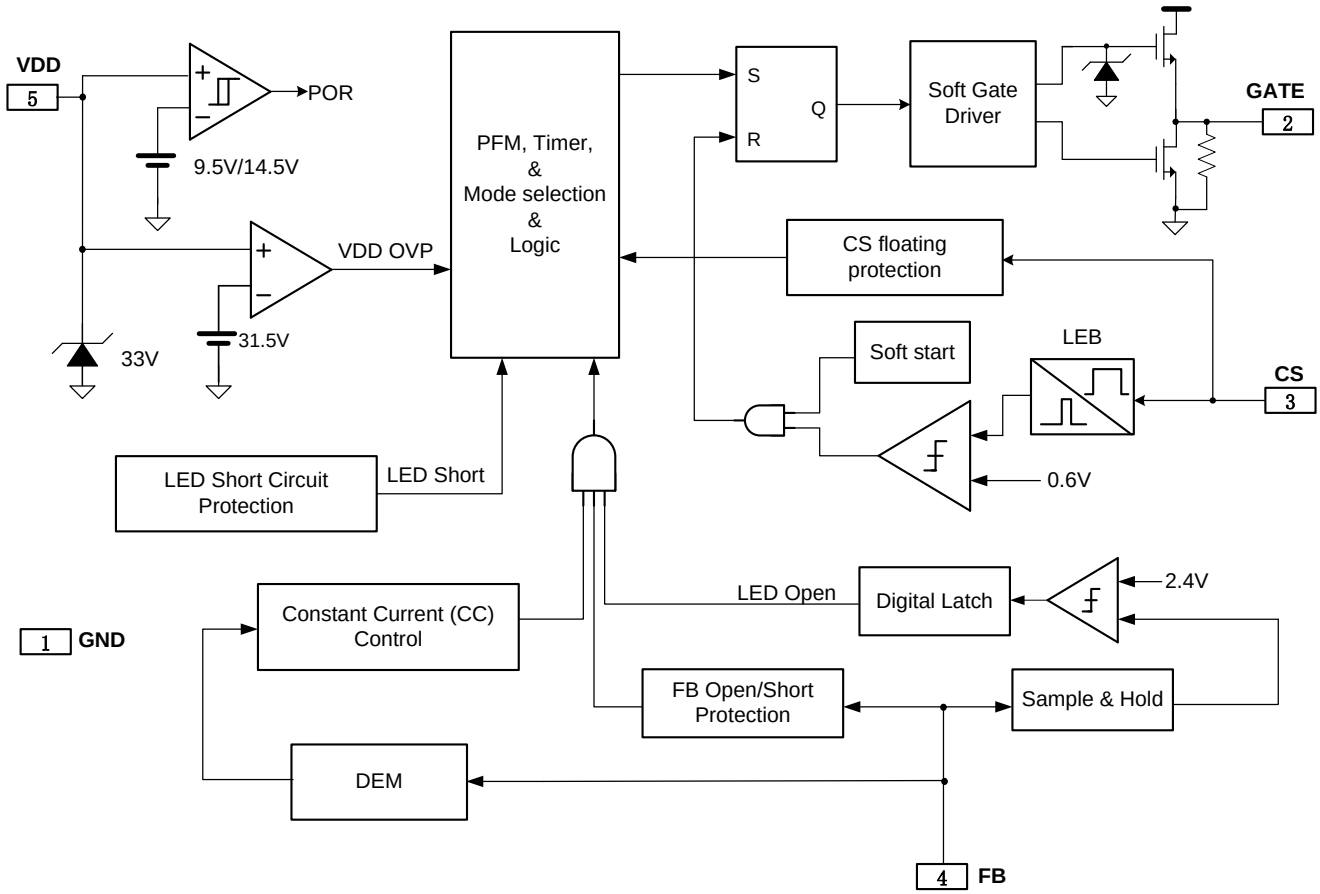


Dot: Pin1 Mark
YWW: Year & Week Code

Pin Description

Pin Num	Pin Name	I/O	Description
1	GND	P	Ground
2	GATE	O	Totem-pole gate driver output to drive the external MOSFET.
3	CS	I	Current sense pin.
4	FB	I	System feedback pin. This control input regulates both the output voltage in CV mode and output current in CC mode based on the Flyback voltage of the auxiliary winding.
5	VDD	P	IC power supply pin.

Block Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	33	V
VDD DC Clamp Current	10	mA
GATE pin	20	V
FB, CS, voltage range	-0.3 to 7	V
Package Thermal Resistance (SOT-23-5)	300	^{o}C/W
Maximum Junction Temperature	150	^{o}C
Operating Temperature Range	-40 to 85	^{o}C
Storage Temperature Range	-65 to 150	^{o}C
Lead Temperature (Soldering, 10sec.)	260	^{o}C
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	10 to 30	V
Operating Ambient Temperature	-40 to 85	^{o}C

ELECTRICAL CHARACTERISTICS

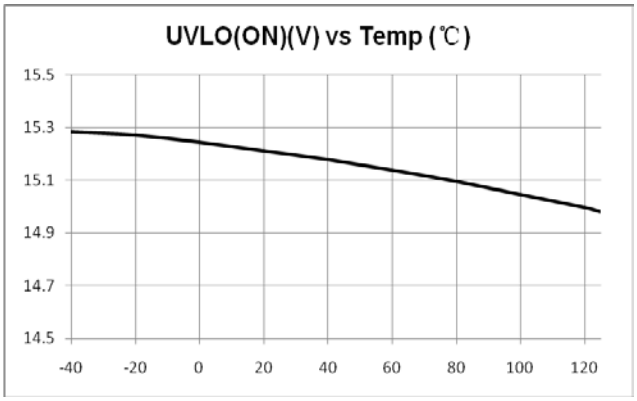
(T_A = 25^{O}C, VDD=16V, if not otherwise noted)

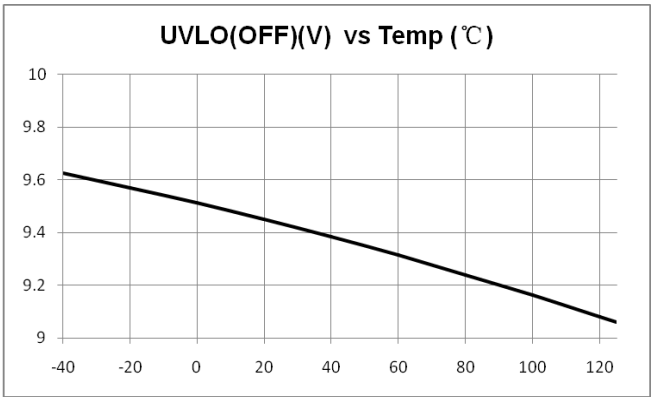
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Section (VDD Pin)						
I_Startup	VDD Start up Current	VDD =UVLO(ON)-1V, Measure current into VDD		5	20	uA
I_VDD_Op	Operation Current	V_{FB}=3V,CL=1nF, VDD=20V		1	1.5	mA
UVLO(ON)	VDD Under Voltage Lockout Exit (Startup)		14.5	15.5	16.5	V
UVLO(OFF)	VDD Under Voltage Lockout Enter		8.5	9.5	10.5	V
VDD_OVP	VDD Over Voltage Protection trigger			31.5		V
V_{DD}_Clamp	VDD Zener Clamp Voltage	I(V_{DD}) = 10 mA		33		V
T_Softstart	Soft Start Time			2		mSec
Feedback Input Section (FB Pin)						
V_{REF}_OVP	Output over voltage protection threshold		2.3	2.4	2.5	V
V_{FB}_DEM	Demagnetization comparator threshold			0.2		V
T_{min}_OFF	Minimum OFF time			2		uSec
T_{CC}/T_{DEM}	Ratio between switching period in CC mode and demagnetization time			2		
Current Sense Input Section (CS Pin)						
T_blanking	CS Input Leading Edge Blanking Time			500		nSec
Vth_OC	Current limiting threshold		594	600	606	mV
T_D_OC	Over Current Detection and Control Delay	CL=1nF at GATE,		100		nSec
Gate Drive Output (GATE Pin)						
VOL	Output Low Level	Io = 20 mA (sink)			1	V
VOH	Output High Level	Io = 20 mA (source)	7.5			V
VG_Clamp	Output Clamp Voltage Level	VDD=24V		15		V
T_r	Output Rising Time	CL = 1nF		700		nSec
T_f	Output Falling Time	CL = 1nF		35		nSec

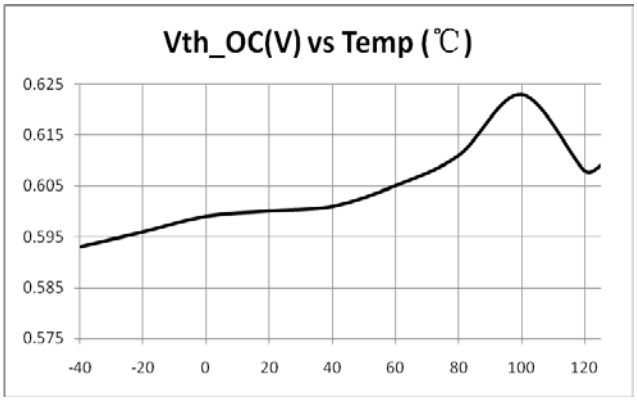
Note 1. Stresses beyond those listed under **"**Absolute Maximum Ratings**"** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

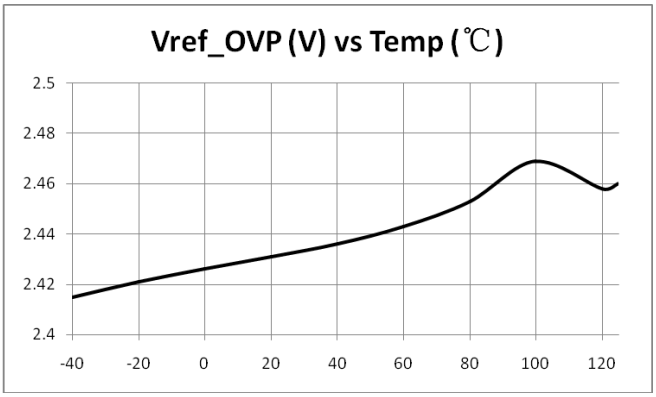
Note 2. The device is not guaranteed to function outside its operating conditions.

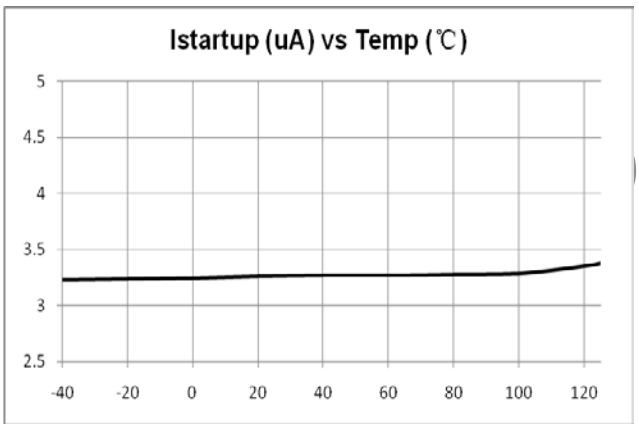
CHARACTERIZATION PLOTS











OPERATION DESCRIPTION

SFL668 is a high performance, highly integrated DCM (Discontinuous Conduction Mode) Primary Side Regulation (PSR) controller working in PFM (Pulse Frequency Modulation) mode. The built-in high precision CC(Constant Current) control with high level protection features make it very suitable for offline LED lighting applications.

◆ PSR Technology Introduction

Assuming the system works in DCM mode, the power transfer function is given by

$$P = \frac{\eta}{2} \times L_m \times I_{pk}^2 \times f_S = V_o \times I_o \qquad \text{(Eq.1)}$$

In the equation above, P is output power, Vo and Io are system output voltage and current respectively, η is system power transfer efficiency, Lm is transformer primary inductance, fs is system switching frequency, Ipk is primary peak current in a switching cycle. The following figure illustrates the waveform in a switching cycle.

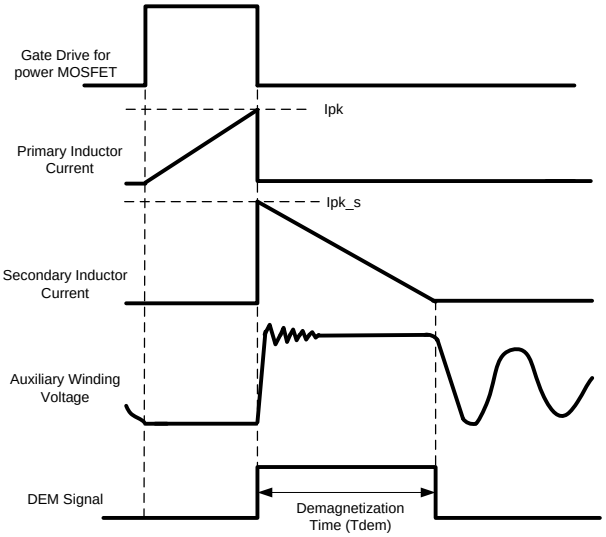


Fig.1

In the figure shown above, the IC generates a demagnetization signal (DEM) in each switching cycle through auxiliary winding. Tdem is demagnetization time for CC control. In DCM mode, Tdem can be expressed as;

$$\frac{V_o}{L_m} \times T_{dem} = \frac{N_S}{N_P} \times I_{pk} \qquad \text{(Eq.2)}$$

In Eq.2, Np and Ns are primary and secondary winding turns respectively.
Combined with Eq.1 and Eq. 2, the average output current can be expressed as:

$$I_o = \frac{\eta}{2} \times I_{pk} \times \frac{N_P}{N_S} \times f_S \times T_{dem} \qquad \text{(Eq.3)}$$

CC (Constant Current) Control Scheme

From Eq.3, it can be easily seen that there are two ways to implement CC control: one is PFM (Pulse Frequency Modulation), the control scheme is to keep Ipk to be constant, let the product of Ts and Tdem (fs*Tdem) to be a constant. In this way, Io will be a value independent to the variation of Vo, Lm, and line input voltage. Another realization method is PWM duty control, the control scheme is to keep fs to be constant, let the product of Tdem and Ipk (Tdem*Ipk) to be a constant, in another words, by modulating system duty cycle to realize a constant Io independent to the variation of Vo, Lm and line voltages.
SFL668 adopts PFM for CC control, the product of Ts and Tdem is given by

$$f_S \times T_{dem} = 0.5 \qquad \text{(Eq.4)}$$

◆ High Precision CC Threshold

In SFL668, the CC comparator threshold voltage is trimmed to tight range (±1%), which can make system CC variation to be less than ±3%, as shown in the following figure.

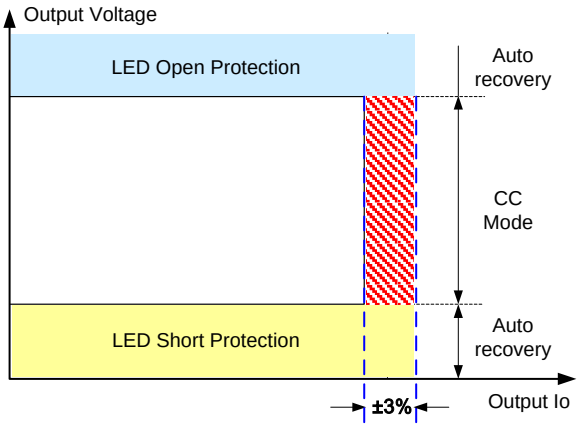


Fig.2

◆ Wide VDD Range Eases Flexible LED System Design

In SFL668, the VDD operating range is very wide, typically from 10V to 30V. Wide VDD range can ease flexible LED system design greatly.
When LED short circuit situation occurs, the IC VDD will drop below UVLO(OFF) because of flyback operation, then the system enters into auto recovery protection mode (mentioned below), as shown in Fig.2.

◆ LED Open Loop Protection

In SFL668, the output OVP is integrated by plateau sampling the auxiliary winding in flyback phase. When LED open circuit situation occurs, the output voltage will rise. When output voltage achieves to 2.4V, the system will enter into auto recovery mode protection (mentioned below), as shown in Fig.3.
System design can set the max LED output voltage based on the

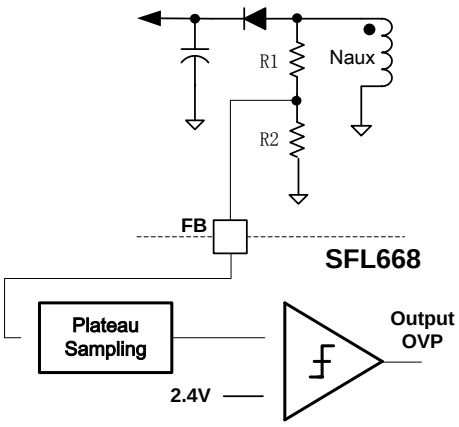


Fig.3

◆ Low Startup Current

Startup current of SFL668 is designed to be very low (typically 5uA) so that VDD could be charged up above UVLO(ON) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application.

◆ Low Operating Current

The operating current in SFL668 is as small as 1mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

◆ Soft Start

SFL668 features an internal 2ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It reduces the stress on the secondary diode during startup. Every startup process is followed by a soft start activation.

◆ PFM Control Eases System EMI Design

As mentioned above, SFL668 uses PFM control, which will eases system EMI design greatly. Since PFM control is a frequency variation system with inherent frequency shuffling function, it will have superior EMI performance than that of PWM control.

◆ Demagnetization Detection

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary winding through FB pin. This voltage features a flyback polarity. The typical detection level is fixed at 0.1V.

◆ Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (500ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the gate driver. Thus, external RC filter with a small time constant is enough for current sensing.

◆ Minimum OFF Time

In SFL668, a minimum OFF time (typically 2us) is implemented to suppress ringing when GATE is off. The minimum OFF time is necessary in applications where the transformer has a large leakage inductance, particularly at low output voltages or startup.

◆ All Pins Floating Protection

In SFL668, if pin floating situation occurs, the IC is designed to have no damage to system.

◆ VDD OVP(Over Voltage Protection)

VDD OVP (Over Voltage Protection) is implemented in SFL668 and it is a protection of auto-recovery mode.

◆ Auto Recovery Mode Protection

As shown in Fig.4, once a fault condition is detected, switching will stop. This will cause VDD to fall because no power is delivered form the auxiliary winding. When VDD falls to UVLO(off) (typical 9V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.4. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

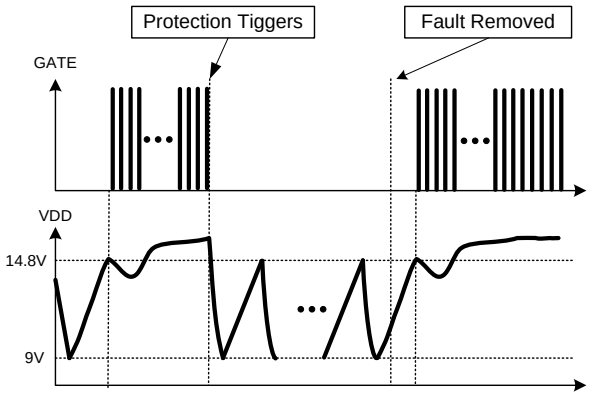


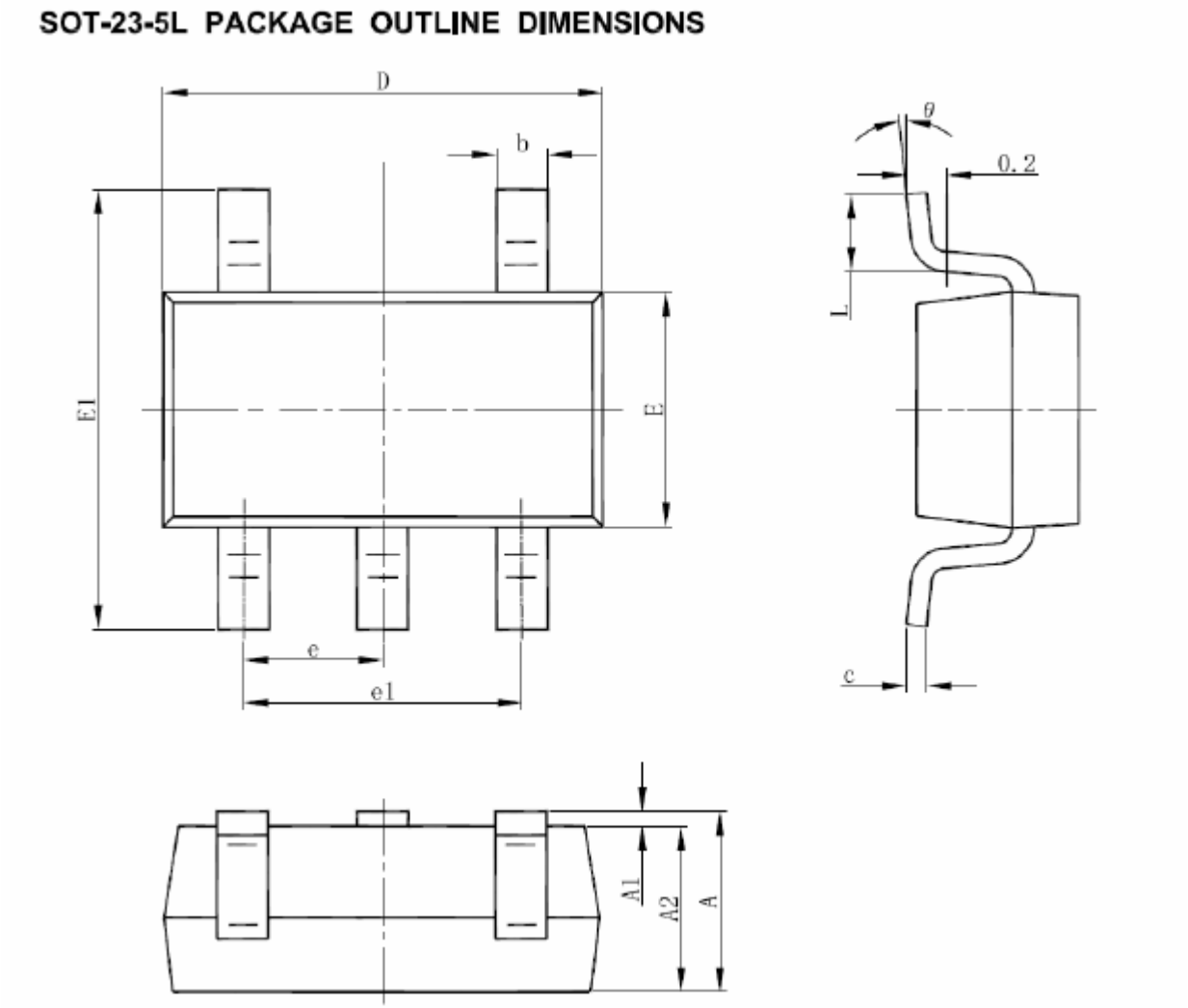
Fig.4

◆ Soft Gate Drive

SFL668 has a soft totem-pole gate driver with optimized EMI performance. An internal 15V clamp is added for MOSFET gate protection at higher than expected VDD input.

PACKAGE MECHANICAL DATA

SOT-23-5L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0º	8º	0º	8º