

## Cost Effective, High Precision Offline PSR Power Switch for LED Lighting

### FEATURES

- ◆ Built-in Power BJT Switch
- ◆ Very Few External Components
- ◆ Built-in Load and AC Line CC Compensation
- ◆ 35KHz Frequency Clamping @ LED Short Circuit
- ◆ Primary Side Regulation (PSR) Control, No Secondary Feedback Circuit Required
- ◆ 2% Precision (@Tj=25 °C) Internal Reference Voltage for Constant Current (CC) Control
- ◆ Precision LED Output Voltage Clamp
- ◆ Compensate for Transformer Inductance Tolerances and Line Voltage Variation
- ◆ Built-in Soft Start
- ◆ Pins Floating Protection
- ◆ LED Open/Short Circuit Protection
- ◆ Cycle-by-Cycle Current Limiting
- ◆ Leading Edge Blanking (LEB)
- ◆ VDD Under Voltage Lockout (UVLO)
- ◆ Output Over Voltage Protection
- ◆ VDD Clamp

### APPLICATIONS

- ◆ AC/DC LED lighting

### GENERAL DESCRIPTION

SFL629 is a high performance, cost effective, highly integrated DCM (Discontinuous Conduction Mode) Primary Side Regulation (PSR) power switch for offline LED lighting applications. The IC can provide very tight (less than 4%) constant current control (CC) ideal for LED lighting applications.

The IC has built-in power BJT and requires very few external components, which can reduce system cost greatly. The IC uses Pulse Frequency Modulation (PFM) control to improve efficiency and eases system EMI design.

SFL629 has built-in **Load CC Compensation** and **AC Line CC Compensation** function, which can further increase LED output CC accuracy.

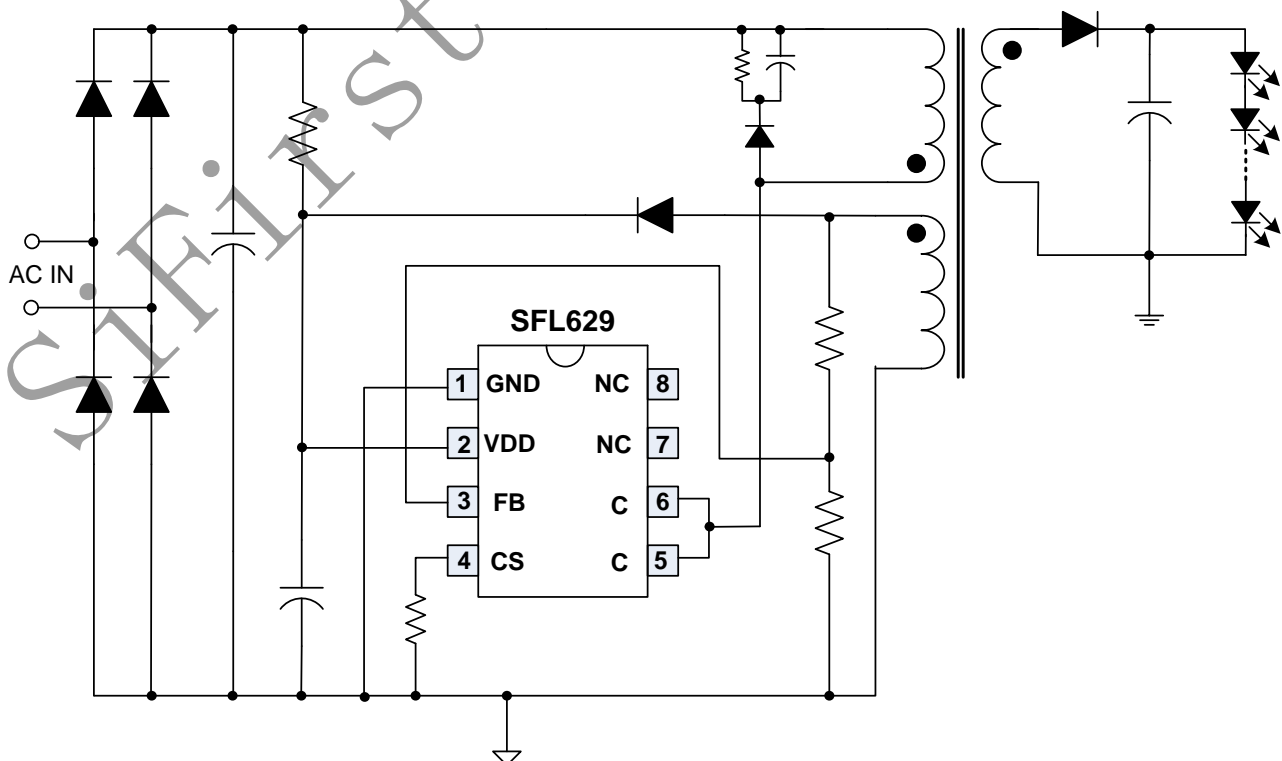
When LED output is short, the IC can automatically clamp the switching frequency to 35KHz, which can improve system reliability.

The wide VDD operating range (10 to 30V, typical) of SFL629 can ease flexible LED system design. The IC also has built-in soft start function to soften the stress on the BJT during power on period.

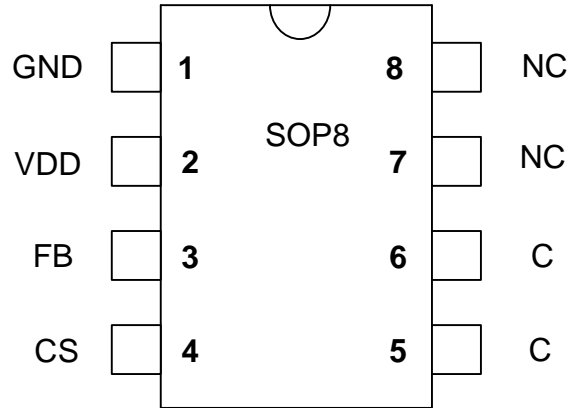
SFL629 integrates functions and protections of Under Voltage Lockout (UVLO), VDD Over Voltage Protection (VDD OVP), LED Open/Short Circuit Protection, Soft Start, Cycle-by-cycle Current Limiting (OCP), Pins Floating Protection, VDD Clamping.

SFL629 is available in SOP8 package.

### TYPICAL APPLICATION



### Pin Configuration



### Ordering Information

Part Number	Top Mark	Package	Tape & Reel
SFL629SG	SFL629SG	SOP8	Green
SFL629SGT	SFL629SG	SOP8	Green
			Yes

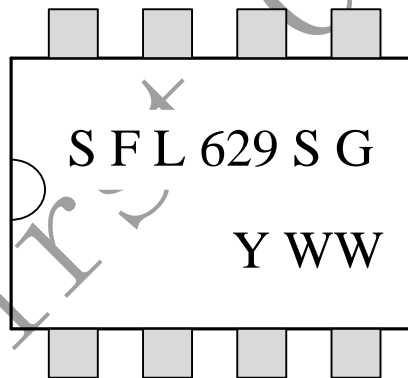
### Output Power Table<sup>(1)</sup>

Part Number	230VAC $\pm 15\%$ <sup>(2)</sup>	85-265VAC
SFL629	5W	4.5W

**Note 1.** The Max. output power is limited by junction temperature.

**Note 2.** 230VAC or 100/115VAC with doublers

### Marking Information

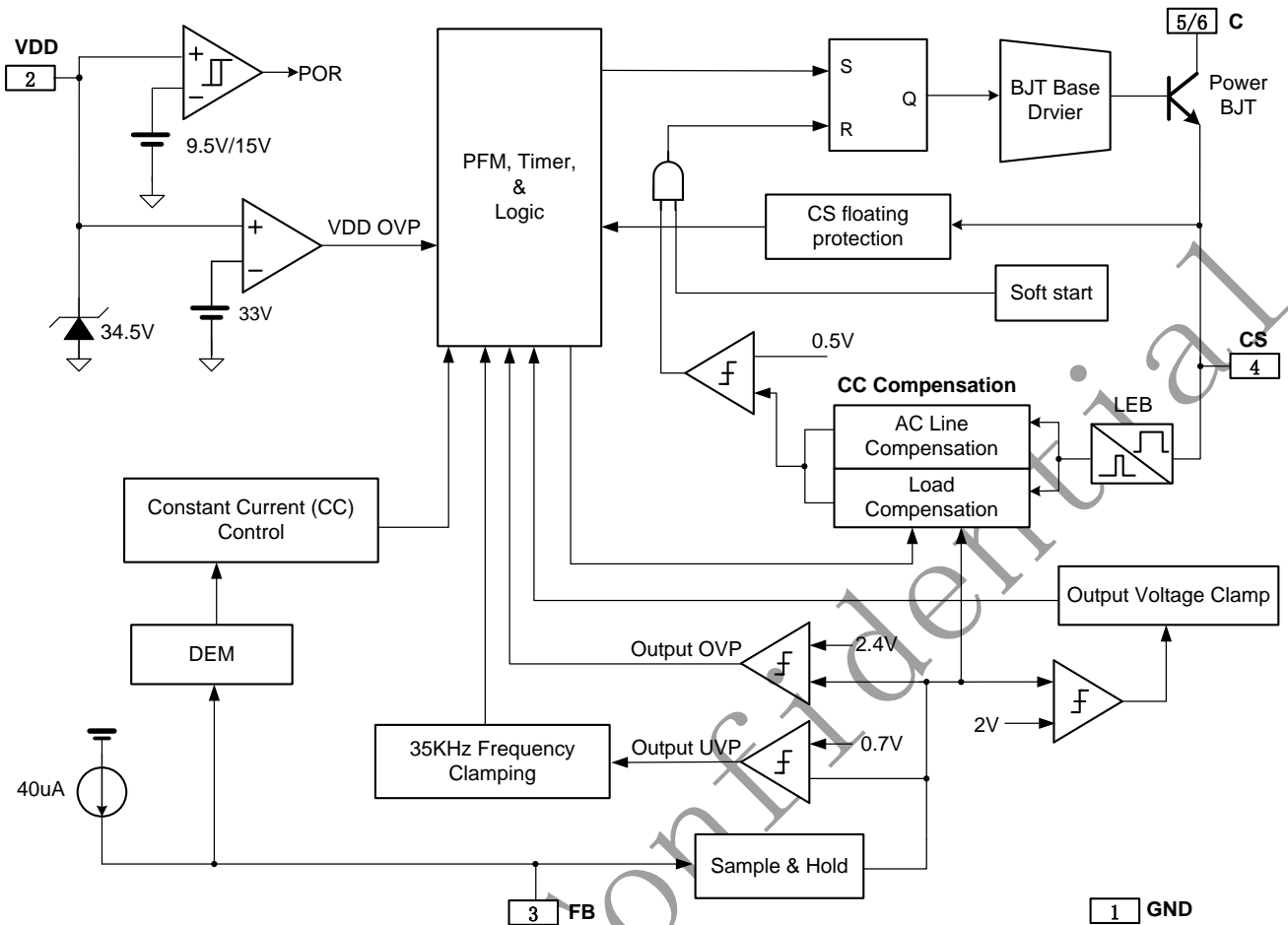


YWW: Year&Week code

### Pin Description

Pin Num	Pin Name	I/O	Description
1	GND	P	Ground
2	VDD	P	IC power supply pin.
3	FB	I	System feedback pin. This control input regulates output current based on the flyback voltage of the auxiliary winding.
4	CS	I	Current sense pin.
5-6	C	P	High voltage power BJT collector pin.
7-8	NC	-	No connection.

## Block Diagram



## Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	35	V
VDD DC Clamp Current	10	mA
FB, CS, voltage range	-0.3 to 7	V
Collector to Base Voltage	700	V
Package Thermal Resistance (SOP-8)	150	°C/W
Maximum Junction Temperature	150	°C
Operating Temperature Range	-40 to 85	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

## Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	10 to 30	V
Operating Ambient Temperature	-40 to 85	°C

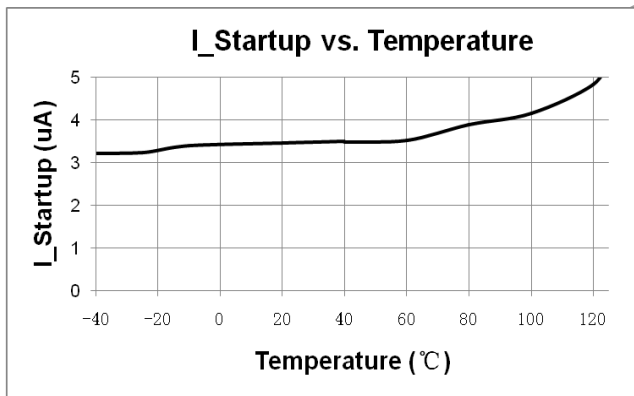
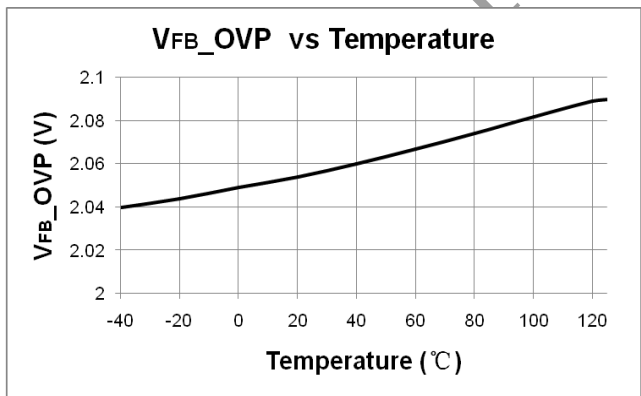
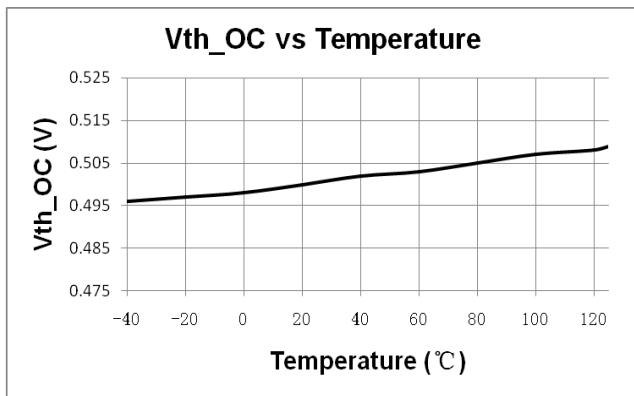
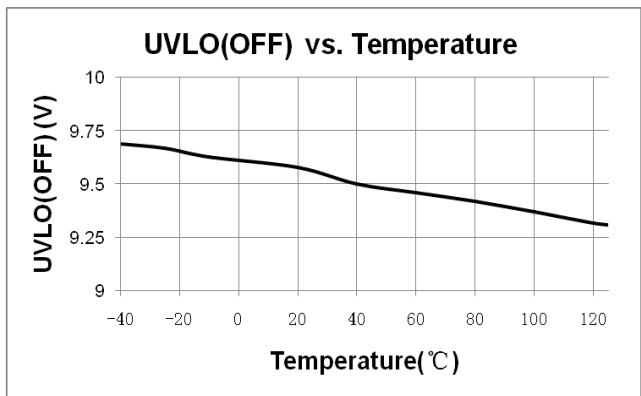
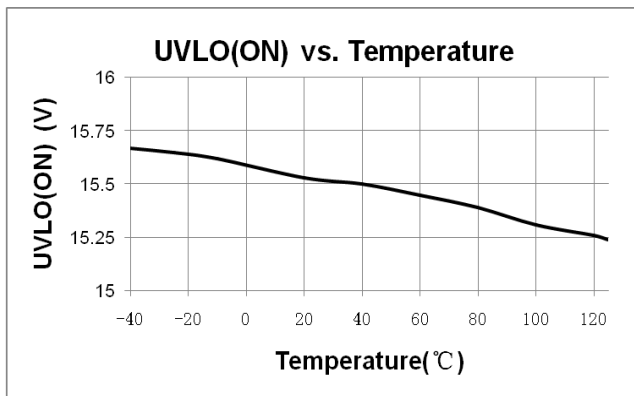
**ELECTRICAL CHARACTERISTICS**(T<sub>A</sub> = 25°C, VDD=18V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Supply Voltage (VDD) Section</b>						
I_Startup	VDD Start up Current	VDD = UVLO(ON)-1V, Measure current into VDD		3	20	uA
I_VDD_Op	Operation Current	V <sub>FB</sub> =1V, , VDD=20V		1	1.5	mA
UVLO(ON)	VDD Under Voltage Lockout Exit (Startup)		14	15	16	V
UVLO(OFF)	VDD Under Voltage Lockout Enter		8.5	9.5	10.5	V
VDD_OVP	VDD Over Voltage Protection trigger		31	33	35	V
V <sub>DD</sub> _Clamp	VDD Zener Clamp Voltage	I(V <sub>DD</sub> ) = 10 mA	33.5	34.5	36.5	V
T_Softstart	Soft Start Time			3		mSec
<b>Feedback Input Section(FB Pin)</b>						
V <sub>FB</sub> _DEM	Demagnetization comparator threshold			0.1		V
T <sub>min</sub> _OFF	Minimum OFF time			2		uSec
T <sub>CC</sub> /T <sub>DEM</sub>	Ratio between switching period in CC mode and demagnetization time			2		
V <sub>FB</sub> _CV _Clamp	Internal Error Amplifier(EA) reference input			2.0		V
V <sub>FB</sub> _OVP	Output over voltage protection threshold			2.4		V
V <sub>FB</sub> _UVP	Output under voltage protection threshold			0.7		V
F <sub>Clamp_Short</sub>	Max frequency @ Output Short Circuit			35		KHz
I <sub>FB_pullup</sub>	FB pullup current			40		uA
<b>Current Sense Input Section (CS Pin)</b>						
T_blanking	CS Input Leading Edge Blanking Time			500		nSec
V <sub>th_OC_max</sub>	Max. Current limiting threshold		490	500	510	mV
T <sub>D_OC</sub>	Over Current Detection and Control Delay			100		nSec
<b>Power BJT Section</b>						
V <sub>CEO</sub>	Collector-emitter breakdown voltage	I <sub>c</sub> =10mA, I <sub>b</sub> =0	450			V
V <sub>CBO</sub>	Collector- base breakdown voltage	I <sub>c</sub> =10mA	700			V
H <sub>fe</sub>	DC current gain	V <sub>ce</sub> =5V, I <sub>c</sub> =0.5A	10		40	
V <sub>CE_sat</sub>	Collector-emitter saturation voltage	I <sub>c</sub> =0.5A, I <sub>b</sub> =0.1A			0.5	V

**Note 1.** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2.** The device is not guaranteed to function outside its operating conditions.

**CHARACTERIZATION PLOTS**



## OPERATION DESCRIPTION

SFL629 is a high performance, cost effective, highly integrated DCM (Discontinuous Conduction Mode) Primary Side Regulation (PSR) power switch. The built-in high precision CC (Constant Current) control with high level protection features make it very suitable for offline LED lighting applications.

### ◆ PSR Technology Introduction

Assuming the system works in DCM mode, the power transfer function is given by

$$P = \frac{\eta}{2} \times L_m \times I_{pk}^2 \times f_s = V_o \times I_o \quad (\text{Eq.1})$$

In the equation above, P is output power, Vo and Io are system output voltage and current respectively, η is system power transfer efficiency, Lm is transformer primary inductance, fs is system switching frequency, Ipk is primary peak current in a switching cycle. The following figure illustrates the waveform in a switching cycle.

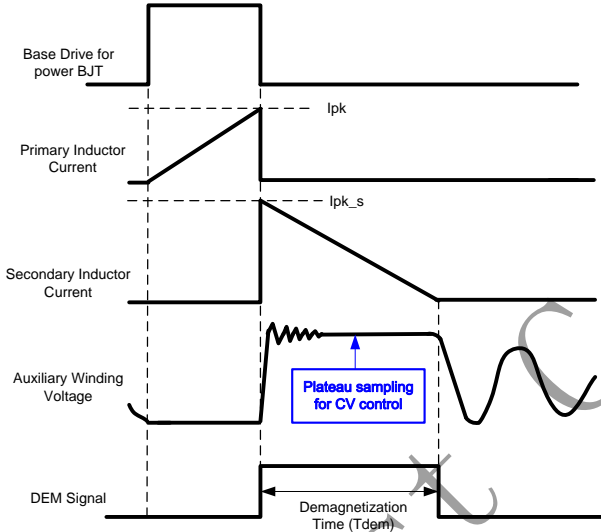


Fig.1

In the figure shown above, the IC generates a demagnetization signal (DEM) in each switching cycle through auxiliary winding. Tdem is demagnetization time for CV/CC control. In DCM mode, Tdem can be expressed as;

$$\frac{V_o}{L_m} \times T_{dem} = \frac{N_s}{N_p} \times I_{pk} \quad (\text{Eq.2})$$

In Eq.2, Np and Ns are primary and secondary winding turns respectively.

Combined with Eq.1 and Eq. 2, the average output current can be expressed as:

$$I_o = \frac{\eta}{2} \times I_{pk} \times \frac{N_p}{N_s} \times f_s \times T_{dem} \quad (\text{Eq.3})$$

### CC (Constant Current) Control Scheme

From Eq.3, it can be easily seen that there are two ways to implement CC control: one is PFM (Pulse Frequency Modulation), the control scheme is to

keep Ipk to be constant, let the product of Ts and Tdem (fs\*Tdem) to be a constant. In this way, Io will be a value independent to the variation of Vo, Lm, and line input voltage. Another realization method is PWM duty control, the control scheme is to keep fs to be constant, let the product of Tdem and Ipk (Tdem\*Ipk) to be a constant, in another words, by modulating system duty cycle to realize a constant Io independent to the variation of Vo, Lm and line voltages.

SFL629 adopts PFM for CC control, the product of Ts and Tdem is given by

$$f_s \times T_{dem} = 0.5 \quad (\text{Eq.4})$$

### ◆ High Precision CC Threshold

In SFL629, the CC comparator threshold voltage is trimmed to tight range (±2%), which can make system CC variation to be less than ±4%, as shown in the Fig.2.

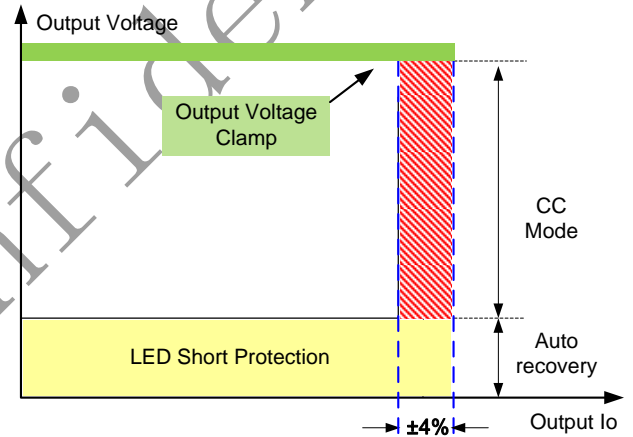


Fig.2

### ◆ Wide VDD Range Eases Flexible LED System Design

In SFL629, the VDD operating range is very wide, typically from 10V to 30V. Wide VDD range can ease flexible LED system design greatly.

### ◆ Output Voltage Clamp and Output Over Voltage Protection (Output OVP)

In SFL629, the output voltage clamp and output Over Voltage Protection (OVP) are integrated by plateau sampling the auxiliary winding in flyback phase. When LED open circuit situation occurs, the output voltage will be clamped. When output voltage achieves to 2.4V, the system will enter into auto recovery mode protection (mentioned below), as shown in Fig.3. When sensed FB voltage is below 0.7V, the IC will enter into Under Voltage Protection (UVP) mode, in which the maximum switching frequency is clamped (mentioned below). When FB is floating, and internal 40uA current source will pull up FB pin to shutdown the system.

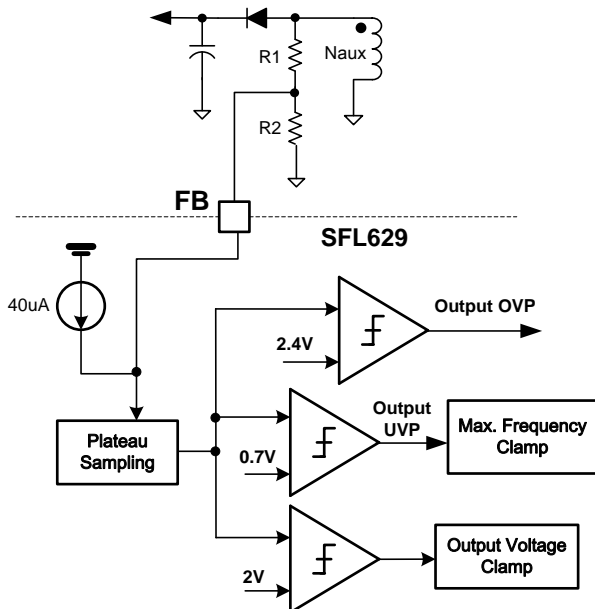


Fig.3

#### ◆ Low Startup Current

Startup current of SFL629 is designed to be very low (typically 3uA) so that VDD could be charged up above UVLO(ON) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application.

#### ◆ Built-in Load and AC Line CC Compensation

In conventional PSR system, the output CC (Constant Current) point can vary with output and AC line voltage. In SFL629, the IC has built-in blocks to compensate the variation, as shown in Fig.4. The IC can adjust CC point based on sensed output voltage and PFM duty. In this way, CC accuracy can be improved.

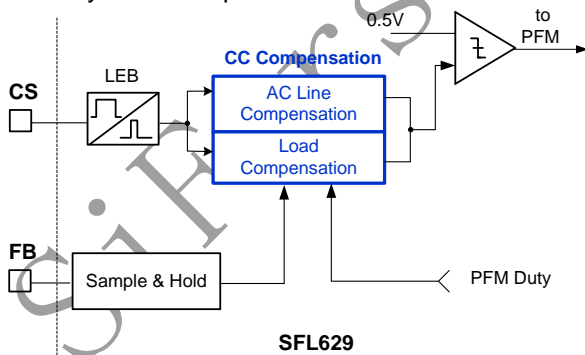


Fig.4

Typically, extra external CC compensation circuits are no needed. If a more précised CC point is needed, conventional external compensation network can be added.

#### ◆ Low Operating Current

The operating current in SFL629 is as small as 1mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

#### ◆ Soft Start

SFL629 features an internal 3ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. Every startup process is followed by a soft start activation.

#### ◆ PFM Control Eases System EMI Design

As mentioned above, SFL629 uses PFM control, which will ease system EMI design greatly. Since PFM control is a frequency variation system with inherent frequency shuffling function, it will have superior EMI performance than that of PWM control.

#### ◆ Maximum Frequency Clamping @ Output Short Circuit

In SFL629, when FB voltage is below 0.7V, the IC will enter into Under Voltage Protection (UVP) mode, the PFM switching frequency is clamped to 35KHz (typical). This protection is useful for LED short circuit protection. When output short, the frequency clamping can lower power BJT voltage spike and the system reliability can be improved, as shown in Fig.5

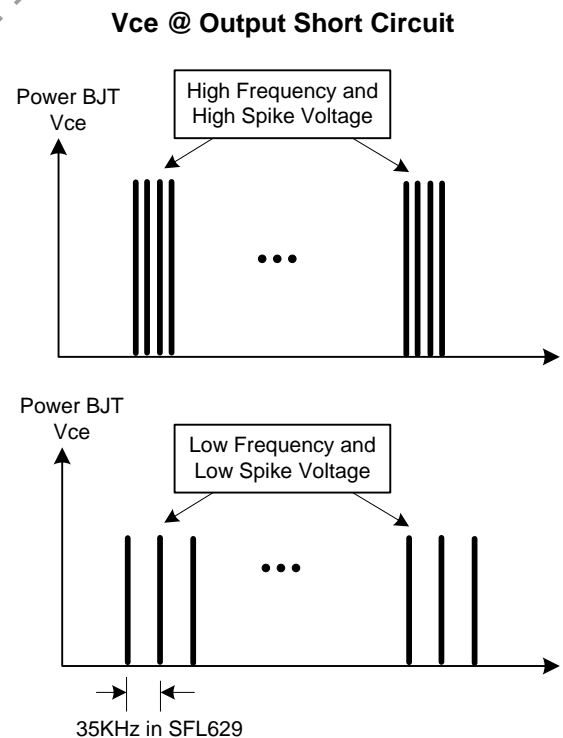


Fig.5

#### ◆ Demagnetization Detection

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary winding through FB pin. This voltage features a



flyback polarity. The typical detection level is fixed at 0.1V.

#### ◆ Leading Edge Blanking (LEB)

Each time the power BJT is switched on, a turn-on spike occurs across the sensing resistor. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (500ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the base driver.

#### ◆ Minimum OFF Time

In SFL629, a minimum OFF time (typically 2us) is implemented to suppress ringing when Base is off. The minimum OFF time is necessary in applications where the transformer has a large leakage inductance, particularly at low output voltages or startup.

#### ◆ Pins Floating Protection

In SFL629, if pin floating situation occurs, the IC is designed to have no damage to system.

#### ◆ VDD OVP(Over Voltage Protection)

VDD OVP (Over Voltage Protection) is implemented in SFL629 and it is a protection of auto-recovery mode.

#### ◆ Auto Recovery Mode Protection

As shown in Fig.6, once a fault condition is detected, switching will stop. This will cause VDD to fall because no power is delivered from the auxiliary winding. When VDD falls to UVLO(off) (typical 9.5V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.6. However, if the fault still exists, the system will

experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

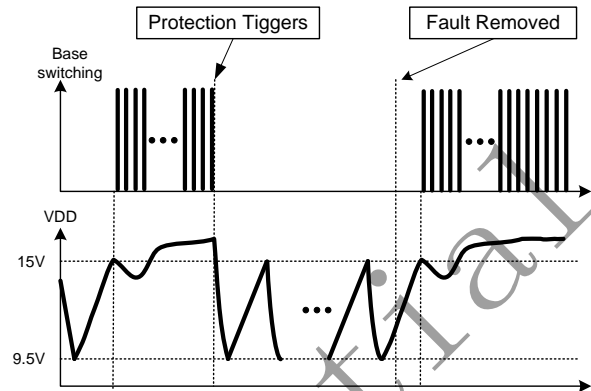
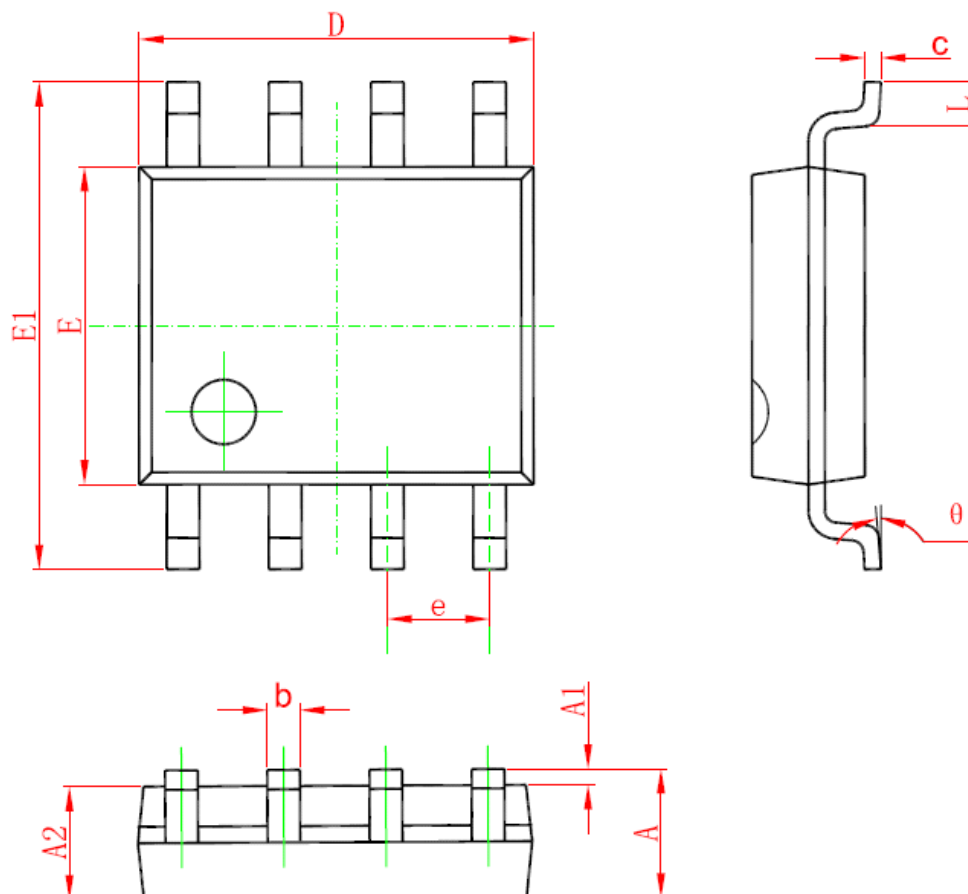


Fig.6



**PACKAGE MECHANICAL DATA**

**SOP8 PACKAGE OUTLINE DIMENSIONS**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.05 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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