

## ***super-QR/PSR*<sup>TM</sup> CV/CC Power Switch**

## FEATURES

- ◆ **Meet EPS Level 6**
- ◆ **Built-in 600V Power MOSFET**
- ◆ **Proprietary *super-QR/PSR*<sup>™</sup> (Quasi-Resonant & Primary Side Regulation) Control for High Efficiency and Low EMI**
- ◆ **Proprietary Cable Drop Compensation**
- ◆ **Max. Frequency Clamping to Limit Power MOSFET Vds Spike @ Output Short Circuit**
- ◆ **Less than 70mW Standby Power**
- ◆  **$\pm 5\%$  CC and CV Precision**
- ◆ **Multi-Mode Control**
- ◆ **Cycle-by-Cycle Current Limiting**
- ◆ **Leading Edge Blanking (LEB)**
- ◆ **Soft Start**
- ◆ **Output Over Voltage Protection**
- ◆ **VDD UVLO, OVP & Clamp**

## APPLICATIONS

- ◆ Battery chargers for cellular phones, cordless phones, PDA, digital cameras, etc
- ◆ Replaces linear transformer and RCC SMPS
- ◆ AC/DC LED lighting

## GENERAL DESCRIPTION

SF6772 is a high performance, highly integrated QR (Quasi Resonant Mode) and Primary Side Regulation (PSR) power switch for offline small power converter applications.

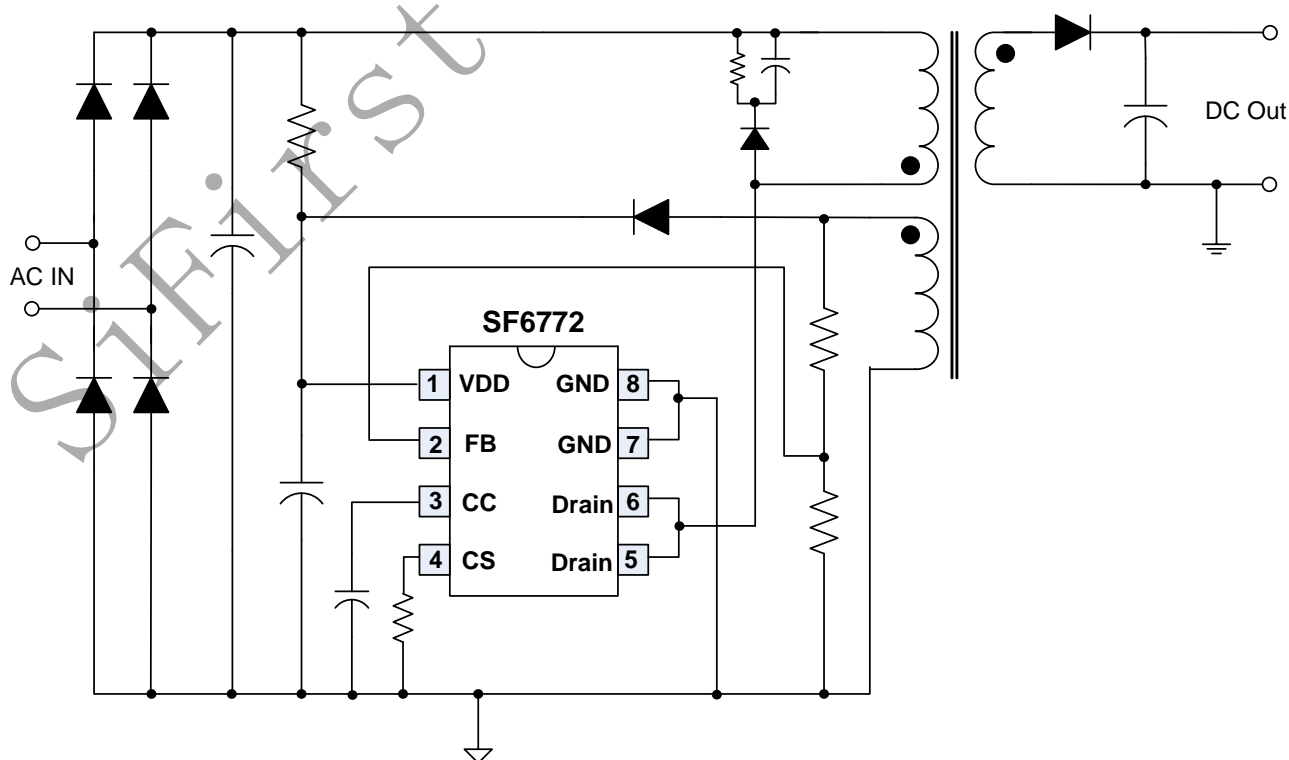
SF6772 has proprietary **super-QR/PSR™** control for high efficiency and low EMI, which can ensure system to meet EPS Level 6 energy standard. The IC also has built-in cable drop compensation function to achieve excellent CV performance.

SF6772 uses **Multi Mode Control** to improve efficiency and reliability and to decrease audio noise energy @ light loadings. SF6772 also integrates the function of “**Max. Frequency Clamping @ Output Short Circuit**” to limit power MOSFET Vds spike when output short circuits occurs.

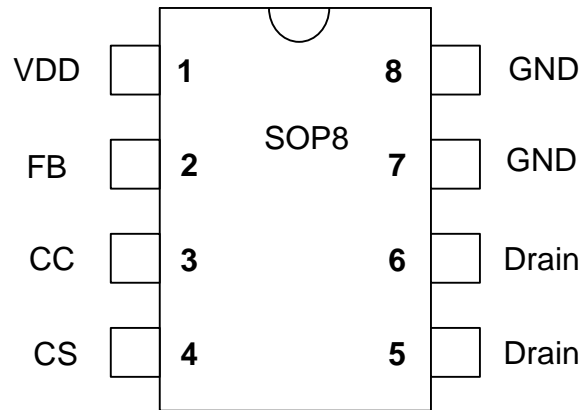
SF6772 integrates functions and protections of FB Short Protection, Under Voltage Lockout (UVLO), VDD Over Voltage Protection (VDD OVP), Output Over Voltage Protection (Output OVP), Soft Start, Cycle-by-cycle Current Limiting (OCP), Pin Floating Protection, VDD Clamping.

SF6772 is available in SOP8 package.

## TYPICAL APPLICATION



## Pin Configuration



## Ordering Information

Part Number	Top Mark	Package		Tape & Reel
SF6772SG	SF6772SG	SOP8	Green	
SF6772SGT	SF6772SG	SOP8	Green	Yes

## Output Power Table<sup>(1)</sup>

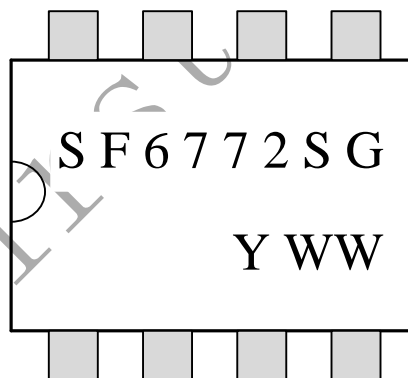
Part Number	230VAC $\pm 15\%$ <sup>(2)</sup>	85-265VAC
	Adapter <sup>(3)</sup>	Adapter <sup>(3)</sup>
<b>SF6772</b>	7.5W	5.5W

**Note 1.** The Max. output power is limited by junction temperature

**Note 2.** 230VAC or 100/115VAC with doublers

**Note 3.** Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink at 50°C ambient.

## Marking Information

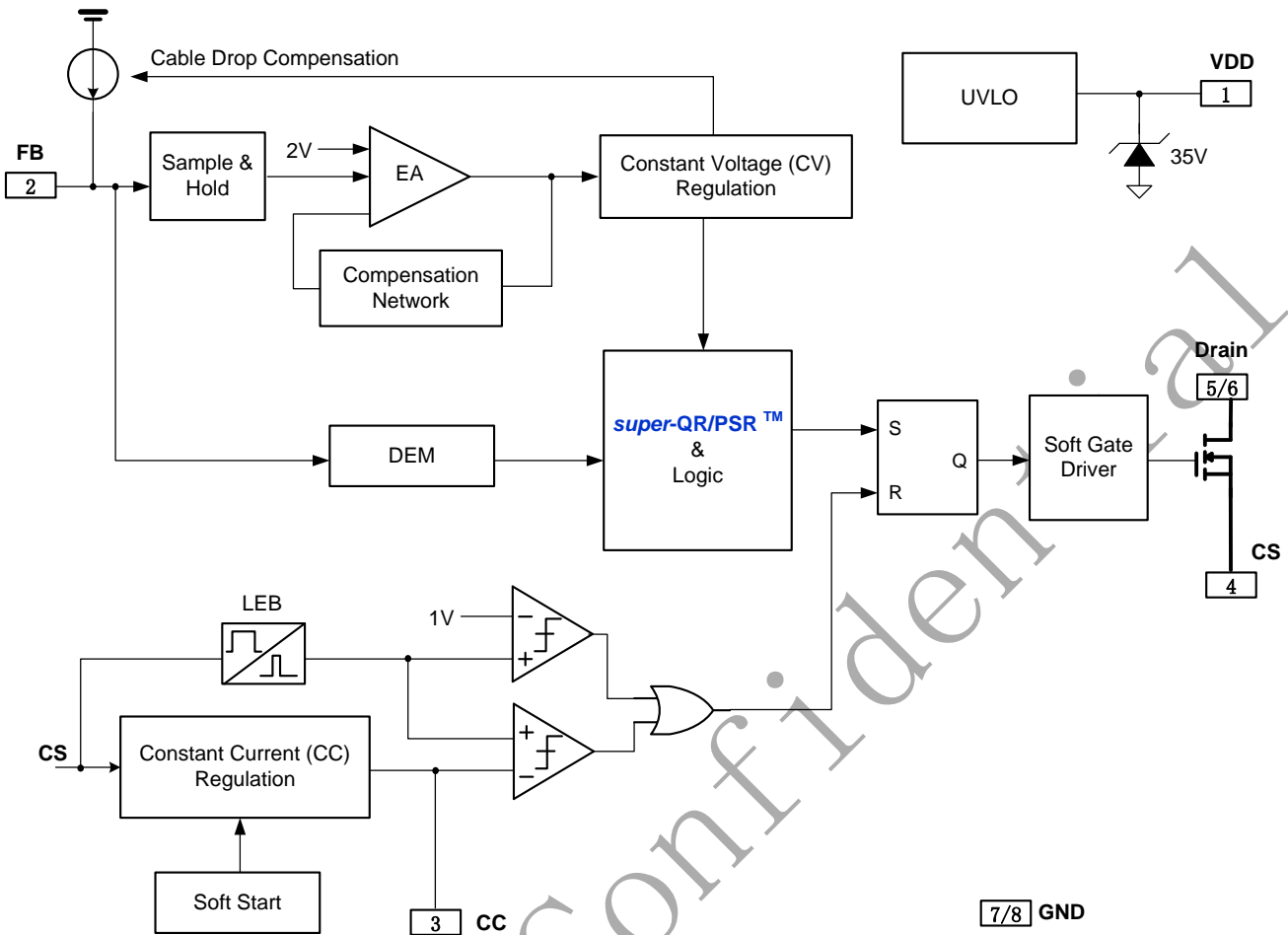


YWW: Year&Week code

## Pin Description

Pin Num	Pin Name	I/O	Description
1	VDD	P	IC power supply pin.
2	FB	I	System feedback pin. This control input regulates both the output voltage in CV mode and output current in CC mode based on the flyback voltage of the auxiliary winding.
3	CC	O	Connect a capacitor between this pin and GND for CC regulation.
4	CS	I	Current sense pin.
5-6	Drain	P	High voltage power MOSFET drain connection.
7-8	GND	P	Ground

## Block Diagram



## Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	35	V
VDD DC Clamp Current	10	mA
Drain pin	-0.3 to 600	V
CC, CS voltage range	-0.3 to 7	V
FB voltage range	-0.7 to 7	V
Package Thermal Resistance (SOP-8)	150	°C/W
Maximum Junction Temperature	150	°C
Operating Temperature Range	-40 to 85	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

## Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	10 to 30	V
Operating Ambient Temperature	-40 to 85	°C
Maximum Switching Frequency	120K	Hz

**ELECTRICAL CHARACTERISTICS**

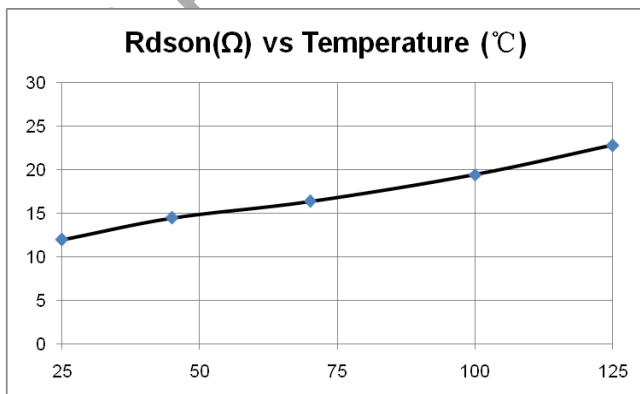
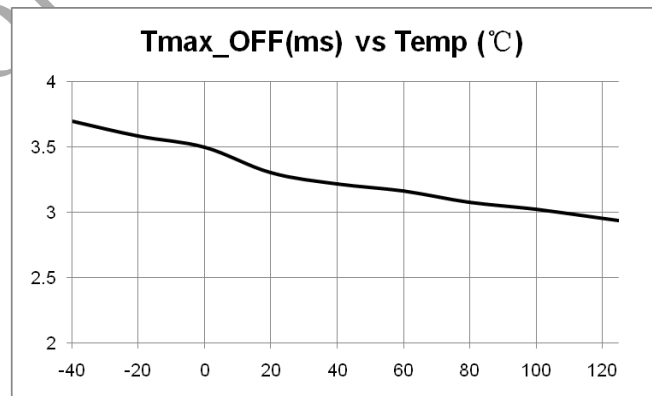
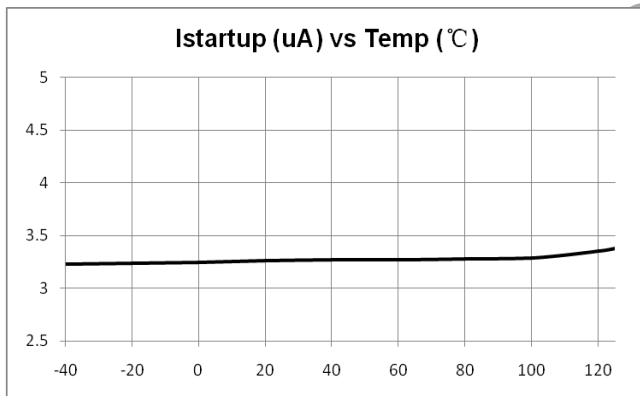
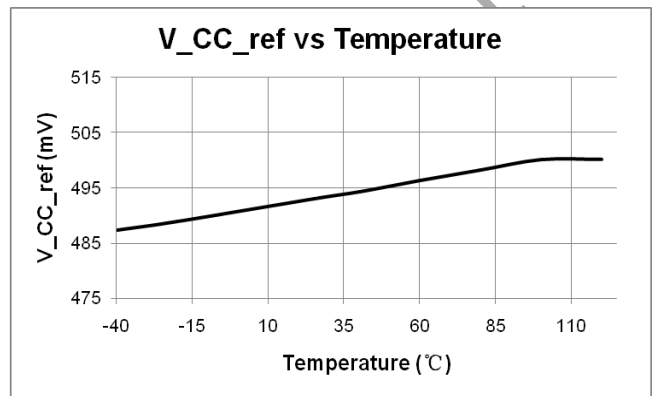
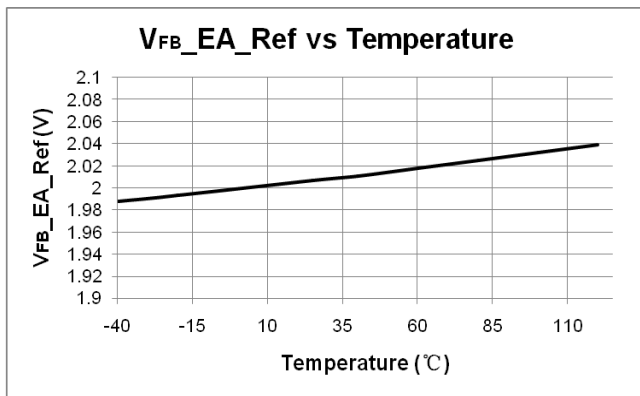
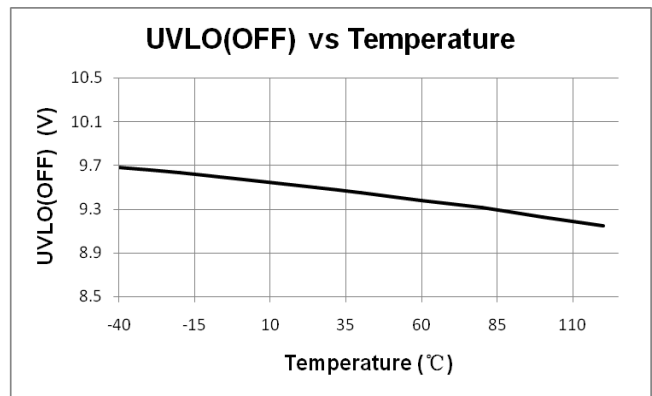
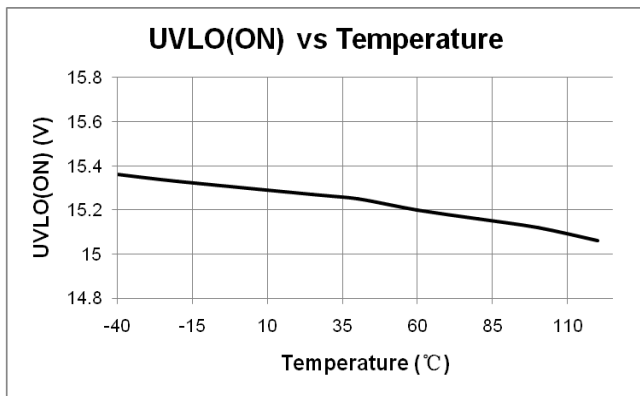
(T<sub>A</sub> = 25°C, VDD=16V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Supply Voltage (VDD) Section</b>						
I_Startup	VDD Start up Current	VDD = UVLO(ON)-1V, Measure current into VDD		2	20	uA
I_VDD_Op	Operation Current	V <sub>FB</sub> =1V, VDD=20V		1	1.5	mA
UVLO(ON)	VDD Under Voltage Lockout Exit (Startup)		14	15.5	16.5	V
UVLO(OFF)	VDD Under Voltage Lockout Enter		8.5	9.5	10.5	V
VDD_OVP	VDD Over Voltage Protection trigger		31	33	35	V
V <sub>DD</sub> _Clamp	VDD Zener Clamp Voltage	I(V <sub>DD</sub> ) = 7 mA	33	35	37	V
<b>Feedback Input Section(FB Pin)</b>						
V <sub>FB</sub> _EA_Ref	Internal Error Amplifier(EA) reference input		1.97	2.0	2.03	V
V <sub>FB</sub> _OVP	Output over voltage protection threshold			2.4		V
V <sub>FB</sub> _Short	Output Short Circuit Threshold			0.65		V
F <sub>Clamp</sub> _Short	Output Short Circuit Frequency Clamp			40		KHz
V <sub>FB</sub> _DEM	Demagnetization comparator threshold			75		mV
T <sub>min</sub> _OFF	Minimum OFF time			2		uSec
T <sub>max</sub> _OFF	Maximum OFF time			3		mSec
I <sub>Cable</sub> _max	Max Cable compensation current			40		uA
<b>Current Sense Input Section (CS Pin)</b>						
T <sub>blanking</sub>	CS Input Leading Edge Blanking Time			500		nSec
T <sub>D</sub> _OC	Over Current Detection and Control Delay			100		nSec
V <sub>CS</sub> _max	Max CS pin voltage			1		V
<b>Constant Current Section (CC Pin)</b>						
V <sub>CC</sub> _ref	Internal CC reference		490	500	510	mV
<b>Power MOSFET Section<sup>(7)</sup></b>						
BV <sub>dss</sub>	Power MOSFET Drain Source Breakdown Voltage		600			V
R <sub>dson</sub>	Static Drain-Source On Resistance	I(Drain)=0.5A		12	15	Ω
I <sub>dss</sub>	Zero Gate Voltage Drain Current				1	uA
T <sub>d(on)</sub>	Turn-on delay time			5.5		ns
T <sub>d(off)</sub>	Turn-off delay time			13		ns

**Note 1.** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2.** The device is not guaranteed to function outside its operating conditions.

# CHARACTERIZATION PLOTS



## OPERATION DESCRIPTION

SF6772 is a high performance, multi mode controlled, highly integrated QR (Quasi Resonant) Primary Side Regulation (PSR) power switch with built-in fast dynamic response control. The built-in high precision CV/CC control with high level protection features make it very suitable for offline small power converter applications.

### ◆ Startup Current and Startup Control

Startup current of SF6772 is designed to be very low (typically 2uA) so that VDD could be charged up above UVLO(ON) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application.

### ◆ Operating Current

The operating current in SF6772 is as small as 1mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement..

### ◆ Proprietary *super-QR/PSR*<sup>TM</sup> Control for EPS Level 6

SF6772 uses a proprietary *super-QR/PSR*<sup>TM</sup> control for high efficiency and low EMI. The IC works in Quasi-Resonant (QR) mode in Constant Current (CC) and Constant Voltage (CV) mode. In this way, the efficiency is boosted and the EMI is reduced greatly. The IC can meet EPS level 6 standard.

### ◆ Constant Current (CC) Regulation

SF6772 can accurately control the output current by the internal current feedback control loop. The output mean current in constant current (CC) mode can be approximately expressed as:

$$I_{cc}(\text{mA}) = \frac{N}{2} \times \frac{500(\text{mV})}{R_{cs}(\Omega)}$$

In the equation above,  
N---The turn ratio of primary side winding to secondary side winding.  
Rcs--- the sensing resistor connected between the MOSFET source to GND.  
In SF6772, the maximum CS voltage is limited to 1V.

### ◆ Precision CV/CC Performance

In SF6772, the parameters are trimmed to tight range, which makes the system CC/CV to have less than 5% variation.

### ◆ Soft Start

SF6772 features an internal soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It reduces the stress on the secondary diode during startup. Every startup process is followed by a soft start activation.

### ◆ Proprietary Cable Voltage Drop Compensation in CV Mode

When it comes to cellular phone charger applications, the battery is located at the end of cable, which causes typically several percentage of voltage drop on the actual battery voltage. SF6772 has a proprietary built-in cable voltage drop compensation block which can provide a constant output voltage at the end of the cable over the entire load range in CV mode.

### ◆ Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (500ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the gate driver.

### ◆ Minimum and Maximum OFF Time

In SF6772, a minimum OFF time (typically 2us) is implemented to suppress ringing when switching is off. The minimum OFF time is necessary in applications where the transformer has a large leakage inductance, particularly at low output voltages or startup. The maximum OFF time in SF6772 is typically 3ms, which provides a large range for frequency reduction. In this way, a low standby power of 70mW can be achieved.

### ◆ Multi Mode PSR Control for High Reliability , High Efficiency, and Audio Noise Free Operation

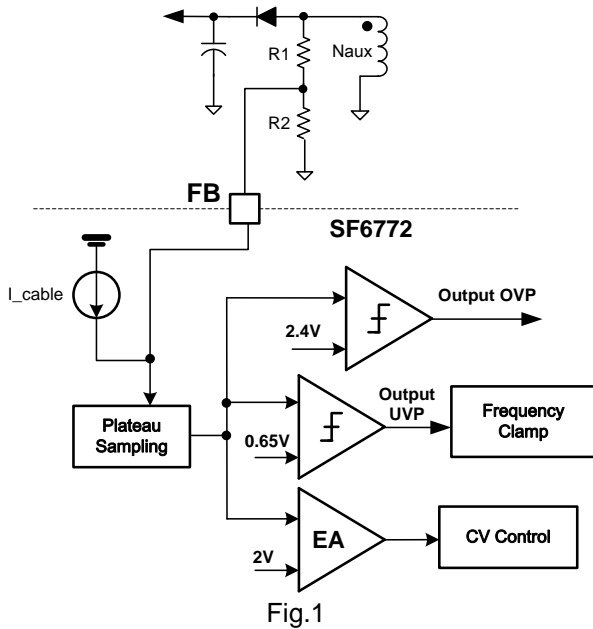
In SF6772, a proprietary multi mode control is adopted to suppress this issue. Around the full load, the system operates in PWM+PFM mode, which improve the system reliability. Under normal to light load conditions, the IC operates in PFM mode to achieve excellent regulation and high efficiency, yet meets the requirement for no-load consumption less than 70mW.

Multi mode control can also reduce audio noise in lighting loadings, compared to conventional pure PFM control.

### ◆ Output OVP(Over Voltage Protection) and Output UVP (Under Voltage Protection)

In SF6772, the output OVP is integrated by plateau sampling the auxiliary winding in flyback phase. The threshold voltage for output OVP is 2.4V, as shown in Fig.1. Output OVP is auto-recovery mode protection (mentioned below).

In SF6772, when sensed FB voltage is below 0.65V, the IC will enter into Under Voltage Protection (UVP) mode, in which the switching frequency is clamped, as shown in Fig.1.



### ◆ Frequency Clamping @ Output Short Circuit

In SF6772, when FB voltage is below 0.65V, the IC will enter into Under Voltage Protection (UVP) mode, the switching frequency is fixed to 40KHz (typical). This protection is useful for LED short circuit protection. When output is short, the frequency clamping can lower power MOSFET Vds spike and the system reliability can be improved, as shown in Fig.2

In SF6772, when output short circuit occurs, the IC will fix the switching frequency to 40KHz. In this way, the power MOSFET Vds spike voltage is suppressed greatly.

#### Vds @ Output Short Circuit

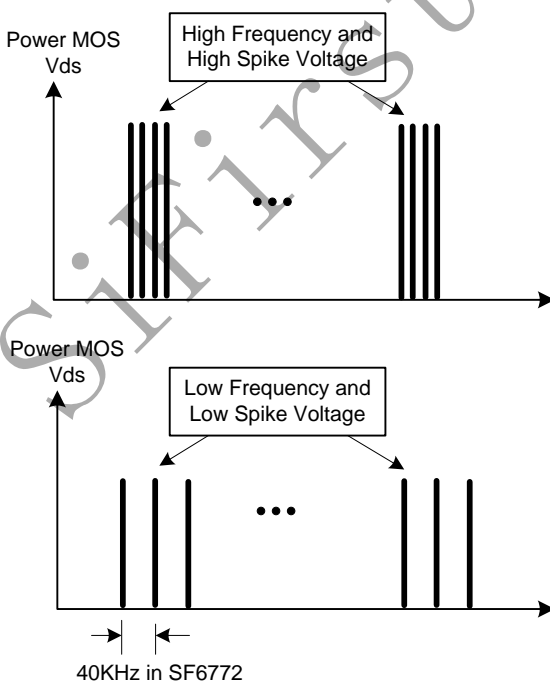


Fig.2

### ◆ Output OVP (Over Voltage Protection)

In SF6772, the output OVP is integrated by plateau sampling the auxiliary winding in flyback phase. The threshold voltage for output OVP is 2.4V. Output OVP is auto-recovery mode protection (mentioned below).

### ◆ VDD OVP(Over Voltage Protection)

VDD OVP (Over Voltage Protection) is implemented in SF6772 and it is a protection of auto-recovery mode.

### ◆ Auto Recovery Mode Protection

As shown in Fig.3, once a fault condition is detected, switching will stop. This will cause VDD to fall because no power is delivered from the auxiliary winding. When VDD falls to UVLO(off) (typical 9.5V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.3. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

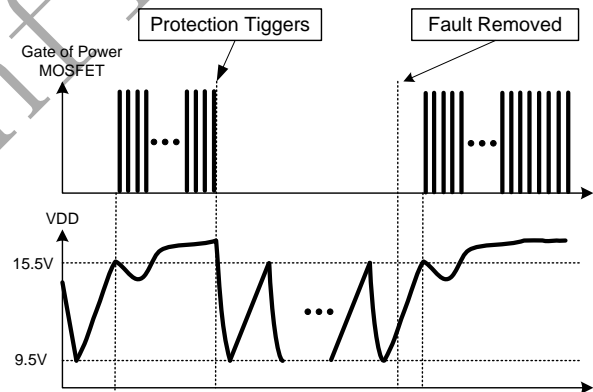


Fig.3

### ◆ Pin Floating Protection

In SF6772, if pin floating situation occurs, the IC is designed to have no damage to system.

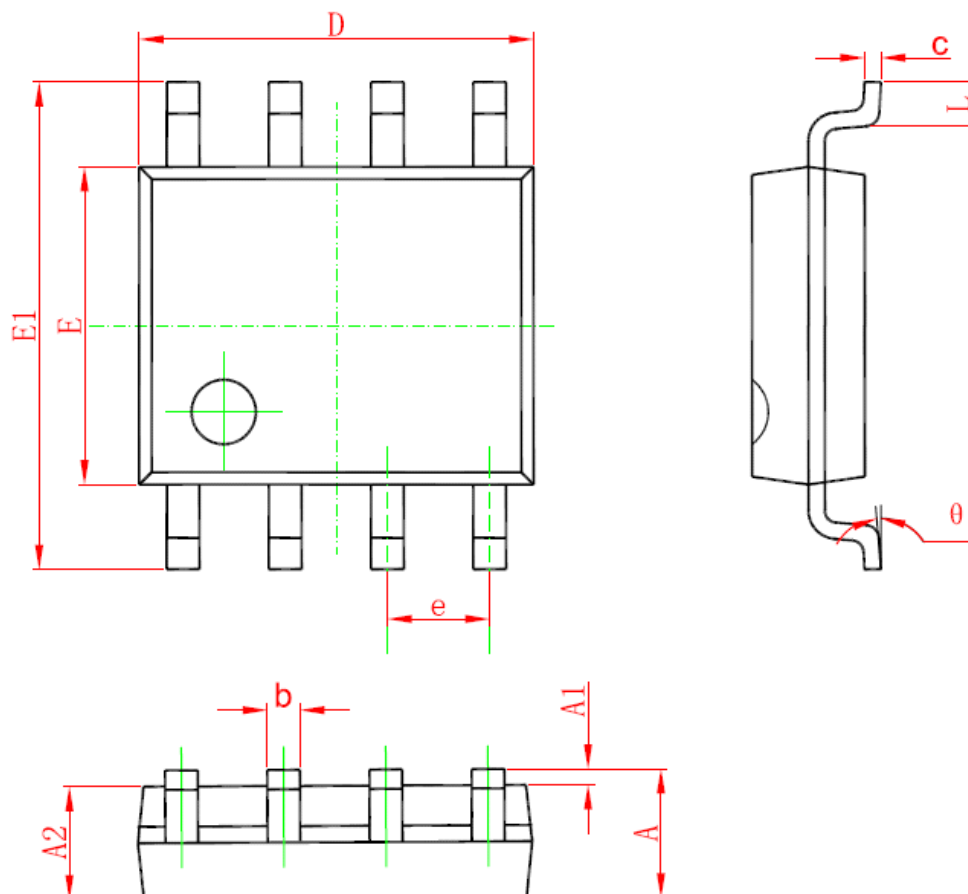
### ◆ Soft Gate Drive

The driving stage of SF6772 is a soft totem-pole gate driver to minimize EMI. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability.



# PACKAGE MECHANICAL DATA

## SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.05 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



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