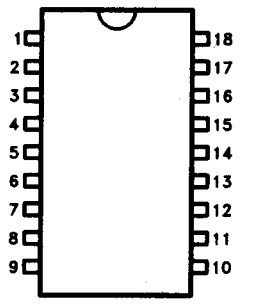
SDA 3202
1.3 GHz PLL with I²C Bus

- Low Current Consumption
- Message Transmission Via I²C Bus
- 4 Software-Controlled Outputs
- Cost-Effective and Space-Saving Design
- Prescaler Output Frequency is Free from Interference Radiation

Pin Configuration

Top View



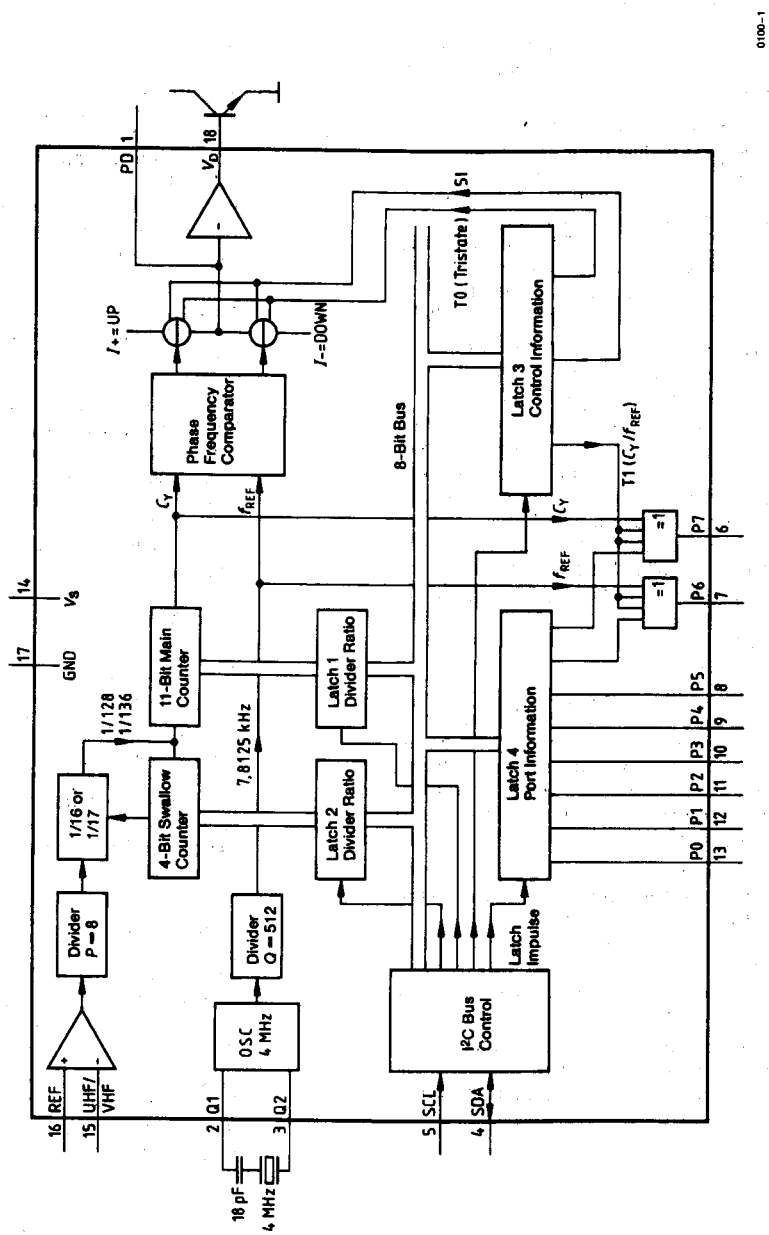
Pin Definitions

Pin	Symbol	Function
1	PD	Input for Active Filter/Output for Charge Pump
2	Q1	Crystal
3	Q2	Crystal
4	SDA	Data I/O for I²C Bus
5	SCL	Clock Input for I²C Bus
6	P7	Port Output (Open Collector)
7	P6	Port Output (Open Collector)
8	P5	Port Output (Open Collector)
9	P4	Port Output (Open Collector)
10	P3	Port Output (Current Sink)
11	P2	Port Output (Current Sink)
12	P1	Port Output (Current Sink)
13	P0	Port Output (Current Sink)
14	V_S	Supply Voltage
15	UHF/VHF	Signal Input
16	REF	Amplifier-Reference Input
17	GND	Ground
18	V_D	Output of Active Filter

Combined with a VCO (tuner), the SDA 3203 comprises a digital programmable phase-locked loop for television devices designed to use the PLL frequency synthesis tuning principle.

The PLL provides a cyrstal-stable frequency for tuner oscillators between 16 . . . 1300 MHz in the 62.5 KHz raster. By including an external prescaler 1/2, the component can also be used for synthesizing applications of up to 2.4 GHz (e.g. satellite receivers). As a result, the resolution is doubled to 125 KHz. The tuning process is controlled via an I²C bus by the microprocessor.

Block Diagram



Circuit Description

Tuning Section (refer to block diagram)

UHF/VHF The tuner signal is capacitively coupled at the UHF/VHF input and subsequently amplified.

REF The reference input REF should be disabled by a capacitor of low series inductance. The amplified signal passes through an asynchronous divider with a fixed ratio of P = 8 and an adjustable divider N = 256...32767. Subsequent to this process, the signal is compared in a digital frequency phase detector with a reference frequency f_{REF} = 7.8125 kHz.

Q1, Q2 This frequency has been derived from a 4 MHz crystal oscillator (pin Q1, Q2) by dividing its output signal by Q = 512.

The phase detector includes two outputs UP and DOWN which control the two current sources I+ and I− of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the current source I+ will pulsate for the duration of the phase difference. However, during the reversed sequence of the negative edges, the current source I− will begin to pulsate.

PD, V_D If both signals are in phase, the charge pump output PD changes into the high impedance state (PLL in lock). An active low pass filter (internal amplifier, external output transistor at V_D, and RC combination) integrates the current pulses as the tuning voltage for the VCO.

With the control bit 5 I the pump current can be switched between two values per software. Through this switch-over, the control characteristics of the PLL during lock-in can be changed, i.e. varying tuner characteristics in the various TV bands can be adjusted.

P0 . . . P3 The software-controllable outputs P0, P1, P2 and P3 can drive external PNP transistors (internal current limit) which operate as band selection switch.

P4 . . . P7 The open collector outputs P4, P5, P6, P7 can be used for a variety of different applications.

I²C Bus Interface

SCL, SDA An asynchronous bidirectional data bus is used for data transfer between the processor and the PLL. As a rule, the clock pulse is supplied by the processor (input SCL), while pin SDA operates as input or output depending on the direction of data flow (open collector, external pull-up resistor).

The data from the processor pass through an I²C bus control. Depending on their function, the data are subsequently filed in registers (latch 0–3). If the bus is free, both lines will be in the marking state (SDA, SCL are HIGH). Each tele- begins with the start conditions of SDA returning into Low, while SCL remains in High. All additional information transfer takes place during SCL = Low and the data is forwarded to the control with the positive clock edge. However, if SDA returns to High, while SCL is in High, the message is ended since the PLL acknowledges a stop condition.

For the following, also refer to table "Logic allocation".

All messages are transmitted byte-by-byte, followed by a 9. clock pulse, while the control returns the SDA line to Low (acknowledge conditions). The first byte is comprised of 7 address bits. These are used by the processor to select the PLL from several peripheral components (chip-select). The 8. bit is always Low.

In the data portion of the message the 1. bit of the 1. or 3. data byte determines whether a divider ratio or a control information is to follow. In each case, the 2. byte of the same data type or a stop condition has to follow the 1. byte.

V_S, GND When the supply voltage is injected, a Power on Reset circuit prevents the PLL from setting the SDA line at Low which would disable the bus.

Absolute Maximum Ratings*

Supply Voltage (V_S) ..... −0.3V to 6V
Output PD (V_1) ..... −0.3V to V_S
Crystal Q1 (V_2) ..... −0.3V to V_S
Crystal Q2 (V_3) ..... −0.3V to V_S
Bus Input/Output SDA (V_4) ..... −0.3V to V_S
Bus Input SCL (V_5) ..... −0.3V to V_S
Port Output P7 (V_6) ..... −0.3V to +16V
Port Output P6 (V_7) ..... −0.3V to +16V
Port Output P5 (V_8) ..... −0.3V to +16V
Port Output P4 (V_9) ..... −0.3V to +16V
Port Output P3 (V_{10}) ..... −0.3V to +16V
Port Output P2 (V_{11}) ..... −0.3V to +16V
Port Output P1 (V_{12}) ..... −0.3V to +16V
Port Output P0 (V_{13}) ..... −0.3V to +16V
Signal Input UHF/VHF (V_{15}) ..... −0.3V to +2.5V
Reference Input REF (V_{16}) ..... −0.3V to +2.5V
Output Active Filter V_D (V_{18}) ..... −0.3V to V_S
Bus Output SDA (I_{4L})
Open Collector ..... −1 mA to +5 mA
Port Output P7 (I_{6L})
Open Collector ..... −1 mA to +5 mA
Port Output P6 (I_{7L})
Open Collector ..... −1 mA to +5 mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Port Output P5 (I_{8L})
Open Collector ..... −1 mA to +5 mA
Port Output P4 (I_{9L})
Open Collector ..... −1 mA to +5 mA
Junction Temperature (T_j) ..... 125°C
Storage Temperature
Range (T_{stg}) ..... −40°C to +125°C
Thermal Resistance
System-Air ($R_{th\ SA}$) ..... 80 K/W

Operating Range

Supply Voltage (V_S) ..... 4.5V to 5.5V
Ambient Temperature (T_A) ..... 0°C to 85°C
Input Frequency (f_{15}) ..... 16 MHz to 1300 MHz
Crystal Frequency ($f_{2,3}$) ..... 4 MHz
Divider Factor (N) ..... 256 to 32767

Characteristics V_S = 5V; T_A = 25°C

Parameter	Symbol	Test Circuit	Limits			Units
			Min	Typ	Max	
Current Consumption	I_S	1	35	55	75	mA
Crystal Frequency Series Capacitance 18 pF	$f_{2,3}$*	1			4	MHz
Input Sensitivity UHF/VHF						
f_{15} = 80 . . . 500 MHz	a_{15}	2	−27/10		3/315	dBm/*
f_{15} = 500 . . . 1000 MHz	a_{15}	2	−24/14		3/315	dBm/*
f_{15} = 1200 MHz	a_{15}	2	−15/40		3/315	dBm/*
Band Selection Outputs P0 . . . P3 (current sinks with internal resistance R_i = 12 kΩ)						
Leakage Current, V_{13H} = 13.5V	I_{13H}	3			10	µA
Sink Current, V_{13H} = 12V	I_{13L}	3	0.7	1	1.5	mA
Port Outputs P4 . . . P7 (switch with open collector)						
Leakage Current, V_{9H} = 13.5V	I_{9H}	4			10	µA
Residual Voltage, I_{9L} = 1.7 mA	V_{9L}	4			0.3	V

*Listed as mV_{rms} with 50Ω

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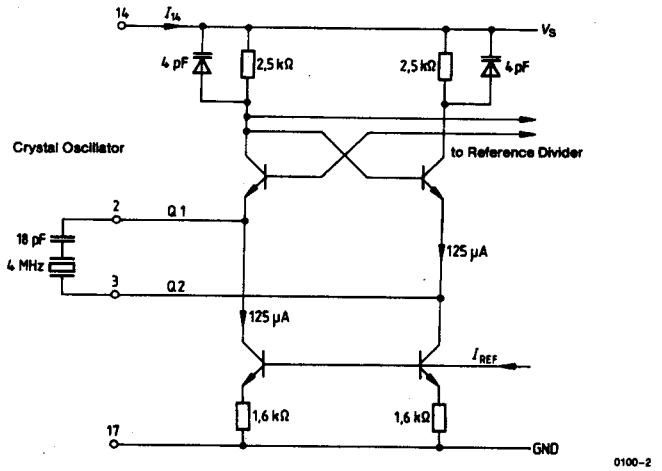
Characteristics V_S = 5V; T_A = 25°C (Continued)

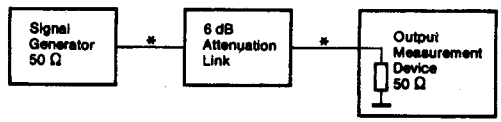
Parameter	Symbol	Test Circuit	Limits			Units
			Min	Typ	Max	
Phase Detector Output PD (V_S = 5V)						
Charge Pump Current 5 I = High; V_1 = 2V	I_{1H}	5	±90	±220	±300	µA
Charge Pump Current 5 I = Low; V_1 = 2V	I_{1H}	5	±22	±50	±75	µA
Output Voltage Locked	V_{IL}	5	1.5		2.5	V
Active Filter Output V_D (Test modus T0 = 1, PD = Tristate)						
Output Current V_{18} = 0.8V; I_{14} = 90 µA	I_{18}	5	500			µA
Output Voltage, V_{1L} = 0V	V_{18}	5			100	mV
Bus Inputs SCL, SDA						
Input Voltage	V_{5H} V_{5L}	6	3		5.5 1.5	V V
Input Current V_{5H} = V_S V_{5L} = 0V	 I_{5L} I_{5L}	 6 6			 50 −100	 µA µA
Output SDA (open collector)						
Output Voltage V_{4H} = 5.5V I_{4L} = 2 mA	 V_{4H} V_{4L}	 6 6			 12 0.4	 V V
Edges SCL, SDA						
Rise Time	t_R	6			15	µs
Fall Time	t_F	6			15	µs
Shift Register Clock Pulse SCL						
Frequency	f_5	6	0		100	KHz
H-Pulse Width	$t_{5\,HIGH}$	6	4			µs
L-Pulse Width	$t_{5\,LOW}$	6	4			µs
Start						
Set-Up Time	t_{SUSTA}	6	4			µs
Hold Time	t_{HDSTA}	6	4			µs
Stop						
Set-Up Time	t_{SUSTO}	6	4			µs
Bus Free Time	t_{BUF}	6	4			µs
Data Transfer						
Set-Up Time	t_{SUDAT}	6	0.3			µs
Hold Time	t_{HDDAT}	6	0			µs

Measurement Circuit 1

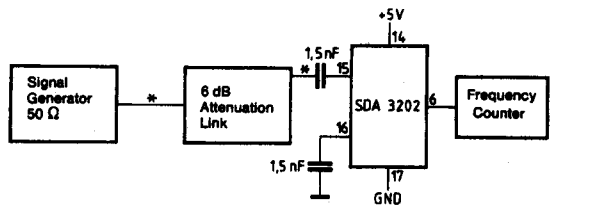


Measurement Circuit 2

Calibration of Signal Generator

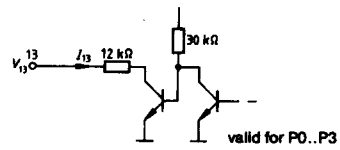


Measurement of Input Sensitivity

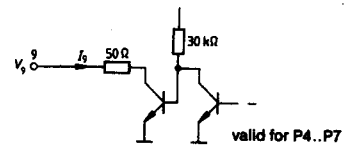


Test mode: T1 = High
* no cable

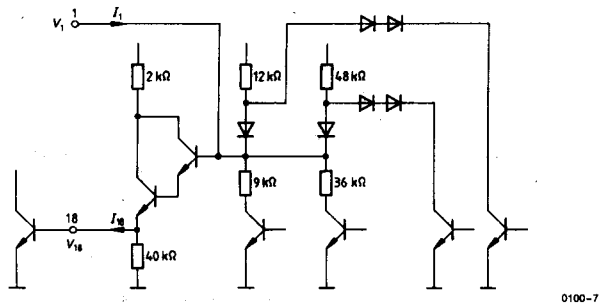
Measurement Circuit 3



Measurement Circuit 4

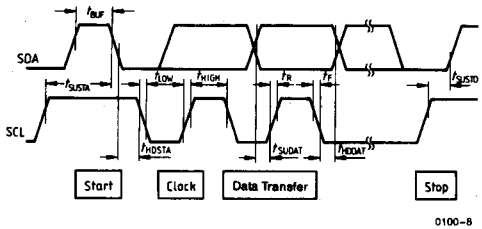


Measurement Circuit 5



Measurement Circuit 6a

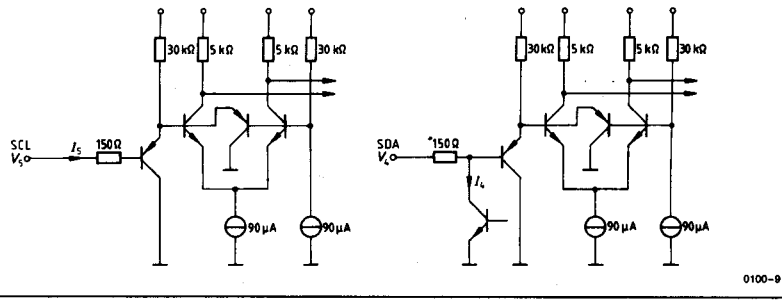
I²C Bus Time Diagram



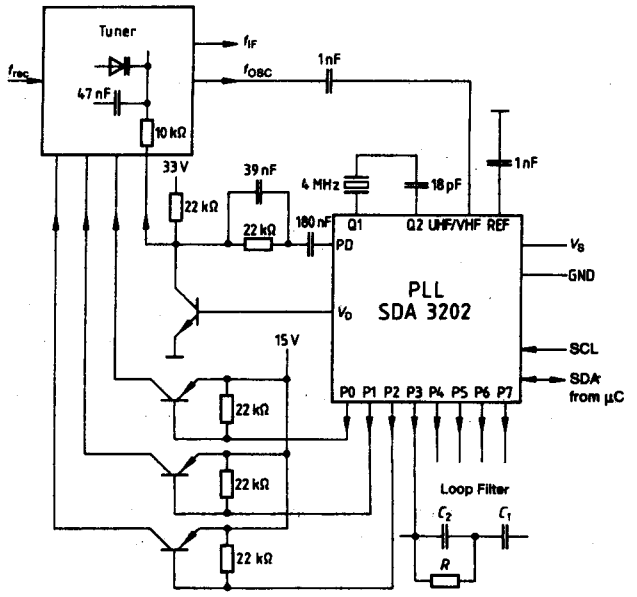
t_{SUSTA}	Set-up time (start)
t_{HDSTA}	Hold time (start)
t_{HIGH}	H-pulse width (clock)
t_{LOW}	L-pulse width (clock)
t_{SUDAT}	Set-up time (Data transfer)
t_{HDDAT}	Hold time (Data transfer)
t_{SUSTO}	Set-up time (Stop)
t_{BUF}	Bus free time
t_F	Fall time
t_R	Rise time

Above times are referenced to V_{IH} and V_{IL} values

Measurement Circuit 6b



Application Circuit



Computation for Loop Filter

Loop bandwidth: $\omega_R = \sqrt{\frac{I_p \times K_{VCO}}{C_1 \times P \times N}}$

Attenuation: $\zeta = 0.5 \times \omega_R \times R \times C_1$

P = Prescaler

N = Progr. divider

I_P = Pump current

K_{VCO} = Tuner slope

R, C_1 = Loop filter

Example for Channel 47

P = 8; N = 11520; I_p = 100 µA;
K_{VCO} = 18.7 MHz/V; R = 22 kΩ;
C_1 = 180 nF; ω_R = 336 Hz;
f_n = 54 Hz; ζ = 0.67

Standard dimensioning: $C_2 = C_{1/5}$

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Description of Function, Application and Circuit

Logic Allocation

	MSB								A = Acknowledge
Address byte	1	1	0	0	0	0	1	0	A
Prog. divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Prog. divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control info byte 1	1	5I	T1	T0	1	1	1	0	A
Control info byte 2	P7	P6	P5	P4	P3	P2	P1	P0	A

Divider ratio:

$N = 16384 \times n14 + 8192 \times n13 + 4096 \times n12 + 2048 \times n11 + 1024 \times n10 + 512 \times n9 + 256 \times n8 + 128 \times n7 + 64 \times n6 + 32 \times n5 + 16 \times n4 + 8 \times n3 + 4 \times n2 + 2 \times n1 + n0$

Band selection:

P3 . . . P0 = 1 Current sink is active

Port outputs:

P7 . . . P4 = 1 Open collector output is active

Switch-over of pump current:

5I =1 High current

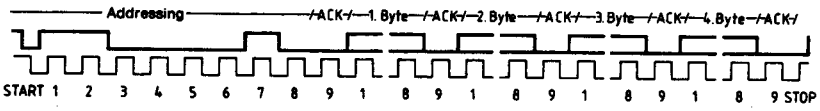
Test Mode:

T1,T0 =0,0 Normal operation

T1 =1 P6 = f_{REF}; P7 = Cy

T0 =1 Tristate charge pump

Pulse Diagram



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Command Samples

Start-Adr-Tv1-Tv2-St1-St2-Stop
Start-Adr-St1-St2-Tv1-Tv2-Stop
Start-Adr-Tv1-Tv2-St1-Stop
Start-Adr-St1-St2-Tv1-Stop
Start-Adr-Tv1-Tv2-Stop
Start-Adr-St1-St2-Stop
Start-Adr-Tv1-Stop
Start-Adr-St1-Stop

Start = start condition
Adr = addressing
Tv1 = divider ratio 1. byte
Tv2 = divider ratio 2. byte
St1 = control word 1. byte
St2 = control word 2. byte
Stop = stop condition

Ordering Information

Type	Ordering Code	Package
SDA 3202	Q67000-Y904	P-DIP 18

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