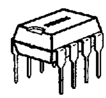
SIEMENS

Nonvolatile Memory 4-Kbit E^2PROM with I^2C Bus Interface

SDA 2546
MOS IC

Features

- Word-organized reprogrammable nonvolatile memory in n-channel floating-gate technology (E^2PROM)
- 512×8-bit organization
- Supply voltage 5 V
- Serial 2-line bus for data input and output (I^2C Bus)
- Reprogramming mode, 10 ms erase/write cycle
- Reprogramming by means of on-chip control (without external control)
- The end of the programming cycle can be checked
- Data retention in excess of 10 years
- More than 10^5 reprogramming cycles **per address**



P-DIP-8-4

Type	Ordering Code	Package	Pin Configuration
SDA 2546-5	Q67100-H5096	P-DIP-8-4	SIEMENS
SDA 25X46-5	Q67100-H3259	P-DIP-8-4	STANDARD

Circuit Description

I^2C Bus Interface

The I^2C Bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a data line SDA and a clock line SCL. The data line requires an external pull-up resistor to V_{CC} (open drain output stages).

The possible operational states of the I^2C Bus are shown in **figure 1**. In the quiescent state, both lines SDA and SCL are high, i.e. the output states are disabled. As long as SCL remains "1", information changes on the data bus indicate the start or the end of a data transfer between two components. The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" a stop condition. During a data transfer the information on the data bus will only change when the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".

In conjunction with an I^2C Bus system, the device can operate as a receiver, and as a transmitter (slave receiver/listener, or slave transmitter/talker). Between the falling edge of the eighth transmission pulse and a ninth acknowledge clock pulse, the device sets the SDA-line to low as a reception confirmation, if the chip select conditions have been met. During the output of data, the data output of the memory becomes high, during the ninth clock pulse (acknowledge master).

The signal timing required for the operation of the I^2C Bus is summarized in **figure 2**.

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Control Functions of the I^2C Bus

The device is controlled by the controller (master) via I^2C Bus in two operating modes: real cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes to the bus after the start condition. Each byte has to be followed by an acknowledge bit. During a memory read, at least eight additional clock pulses are required to accept the data from the memory, before the stop condition may follow. In the programming case, the active programming process is only started by the stop condition after data input, **see figure 3**.

The chip select word includes the chip select bit CS. Thus is possible to parallel two memory devices. Chip select is obtained when the control bits logically correspond to the condition selected at the select input CS. The most significant bits A8 and A9 are inputs with the chip select words CS/E.

Checking the End of the Programming Cycle and Breaking off the Programming Cycle

Addressing the chip by the input of CS/E during active reprogramming terminates the programming cycle. If the chip is addressed by entering CS/A, this will be ignored. Only when the programming cycle has terminated will the chip react on CS/A. With this procedure the end of the programming cycle can be checked, **see figure 3**.

Memory Read

After the input of the two control words CS/E and WA, the resetting of the start condition and the input of a third control word CS/A, the memory is set ready to read. During acknowledge clock no. 9, the memory information is transferred in parallel to the internal data register. Subsequent to the falling edge of the acknowledge clock, the data output is low-impedance and the first data bit can be sampled, **see figure 4**.

With each shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented through the master receiver acknowledge, so that any number of memory locations can be read one after the other. At address 512, an overflow to address 0 is not initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into "1" state. During the write process, "0" states are generated according to the information in the internal data register, i.e. according to the third input control word.

After the 27th and the last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under on-chip control and can be terminated by addressing the device via SCL and SDA.

The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage the erase/write process is max. 20 ms, or typically, 10 ms. For the input of a data word without write request (write request is defined as data bit in the data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

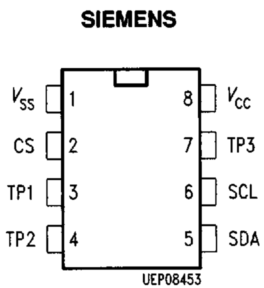
Switch-On and Chip Reset

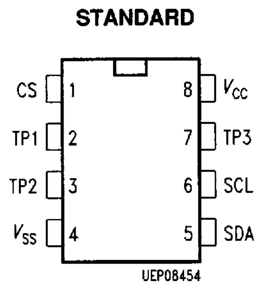
After the supply voltage V_{CC} has been connected, the data output will be in the high impedance mode. As a rule, the first operating mode to be entered should be the read process of a word address. Subsequent to the data output and to the stop condition, the internal control logic is reset. In case of a subsequent active programming operation, however, the stop condition will not reset the control logic.

Chip Erase

To erase the entire memory the control word CS/E is entered, the address register is loaded with address 0 and the data register with FF (hex), respectively. Immediately prior to generating the stop condition, the input TP2 is connected from 0 to 5 V. The subsequent stop condition initiates the chip erase. As soon as the erase procedure has terminated, TP2 is again connected to 0 V.

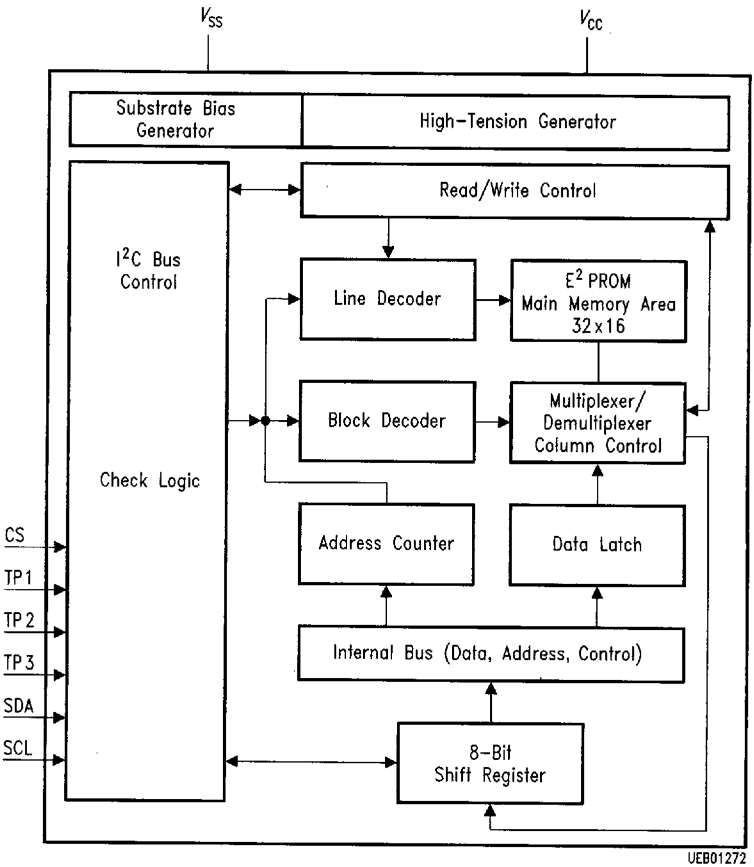
Pin Configuration
(top view)





Pin Definitions and Functions

Pin No.		Symbol	Function
SIEMENS	STANDARD		
1	4	V_{SS}	Ground
2	1	CS	Chip select
3	2	TP1	to V_{SS}
4	3	TP2	0 V normal function, TP2 = 5 V condition for the erase of the complete memory
5	5	SDA	Data line
6	6	SCL	Clock line
7	7	TP3	open
8	8	V_{CC}	Supply voltage



Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{CC}	– 0.3	6	V
Input voltage	V_I	– 0.3	6	V
Power dissipation	P_D		130	mW
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\ SA}$		100	K/W
Junction temperature	T_j		85	°C

Operating Range

Supply voltage	V_{CC}	4.75	5.25	V
Ambient temperature	T_A	0	70	°C

Characteristics
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	V_{CC}	4.75	5.0	5.25	V	
Supply current	I_{CC}			20	mA	V_{CC} = 5.25 V

Inputs

Input voltages SDA/SCL	V_{IL}			1.5	V	
Input voltages SDA/SCL	V_{IH}	3.0		V_{CC}	V	
Input currents SDA/SCL	I_{IH}			10	µA	$V_{IH} = V_{CC}$

Outputs

Output current SDA	I_{QL}			3.0	mA	V_{QL} = 0.4 V
Leakage current SDA	I_{QH}			10	µA	$V_{QH} = V_{CC\,max}$

Inputs

Input voltages CS/TP1/TP2	V_{IL}			0.2	V	
Input voltages CS/TP1/TP2	V_{IH}	4.5		V_{CC}	V	
Input currents CS/TP1/TP2	I_{IH}			100	µA	V_{CC} = 5.25 V
Clock frequency	f_{SCL}			100	kHz	
Reprogramming duration	t_{PROG}		10	20	ms	erase and write
Input capacity	C_I			10	pF	
Total erase	t_{GL}			20	ms	TP2 = 5 V

Diagrams

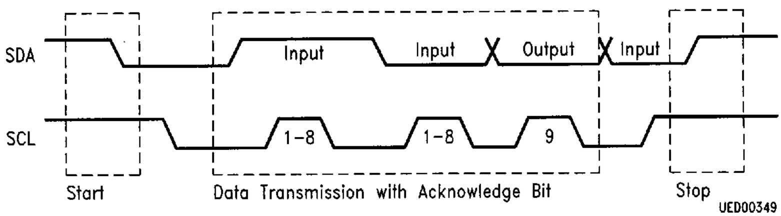


Figure 1
Operational States of the I²C Bus

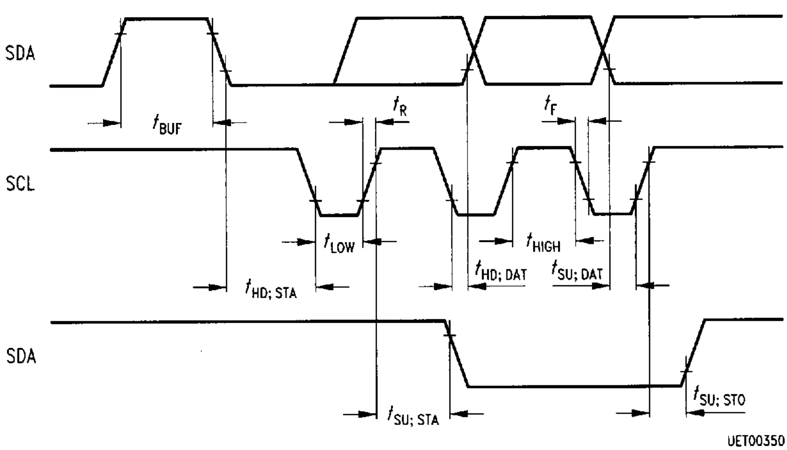


Figure 2
Timing Conditions for the I²C Bus (high-speed mode)

Timing Conditions

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Minimum time the bus must be free before a new transmission can start	t_{BUF}	4.7		µs
Start condition hold time	$t_{HD;\,STA}$	4.0		µs
Clock low period	t_{LOW}	4.7		µs
Clock high period	t_{HIGH}	4.0		µs
Start condition set-up time, only valid for repeated start code	$t_{SU;\,STA}$	4.7		µs
Data set-up time	$t_{SU;\,DAT}$	250		ns
Rise time of both the SDA- and SCL-line	t_R		1	µs
Fall time of both the SDA- and SCL-line	t_F		300	ns
Stop condition set-up time	$t_{SU;\,SPO}$	4.7		µs

Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL. All values refer to V_{IH} and V_{IL} level.

Figure 3
Programming

Control word input

ST	CS/E	As	WA	As	DE	As	SP

(the reprogramming starts after this stop condition)

Check for program end by

ST	CS/A	As

1. when As = 1 programming is not finished
2. when As = 0 programming is finished

Program interruption by

ST	CS/E	As

Figure 4
Read

Control word input read
a) complete (with word address input)

ST	CS/E	As	WA	As	ST	CS/A	As	DA	Am	DA	Am	SP
								n bytes		Last byte		

Automatic incrementation of the word address

b) shortened:
Bit 0 … 8 the last adapted word address keep unchanged

ST	CS/A	As	DA	Am	DA	Am	SP
			n bytes		Last byte		

Autoincrement	Am = 0
before stop condition	Am = 1

Control Word Table

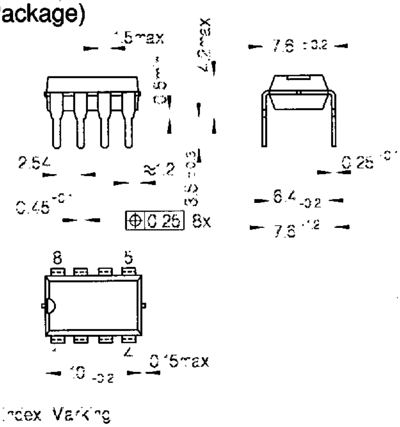
Clock No.	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	0	A8	CS	0	0	through memory
CS/A	1	0	1	0	–	–	CS	1	0	through memory
WA	A7	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0/1	through master

Control Word Input Key

CS/E	Chip select for data input into memory (with the word-address-bit A8)
CS/A	Chip select for data output out of memory
WA	Memory word address
DE	Data word for memory
DA	Data word read out of memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS	Chip select bits
A0 to A8	Memory word address bits

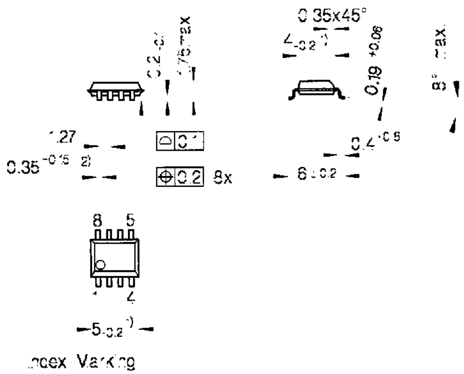
3 Package Outlines

P-DIP-8-4
(Plastic Dual In-line Package)



GPD05025

P-DSO-8-1
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

GPS05121

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm

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