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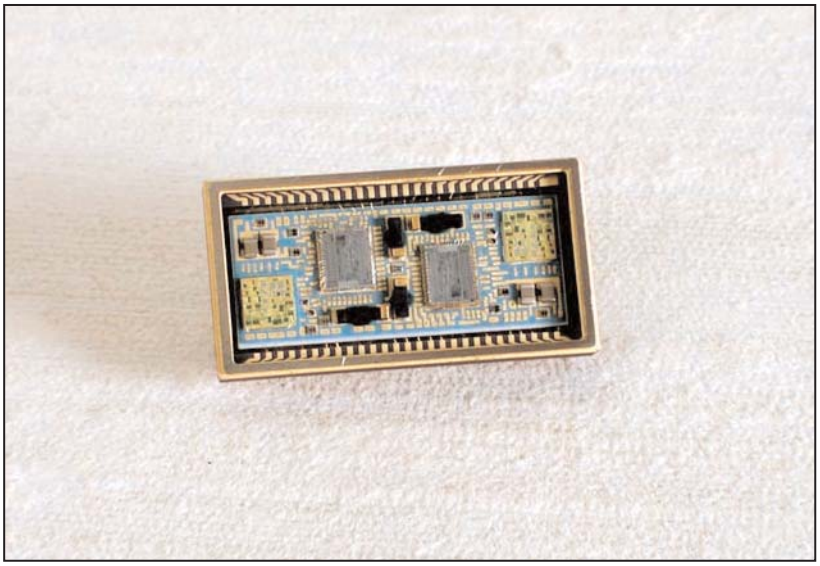
SD-14620 SERIES

TWO-CHANNEL SYNCHRO/RESOLVER-TO-DIGITAL (S/R-D) CONVERTERS



FEATURES

- Synthesized Reference Option
- 1 Minute Accuracy Available ("S" Option only)
- Single +5 V Power Supply
- 10-, 12-, 14- or 16-Bit Programmable Resolution
- Small 54-Pin Ceramic Package
- $\overline{\text{BIT}}$ Output
- Velocity Output Replaces Tachometer
- High Reliability Single Chip Monolithic
- -55°C to +125°C Operating Temperature Range
- MIL-PRF-38534 Processing Available

DESCRIPTION

The SD-14620 Series converters are small, low-cost, two-channel hybrid Synchro- or Resolver-to-Digital converters based on a single-chip monolithic. The SD-14620X"S" option offers synthesized reference circuitry to correct for phase shifts between the reference and signal inputs. The two channels are independent but share the digital output and +5 VDC power pins. The package is 54-pin ceramic, yet is the size of a 28-pin DDIP.

Resolution programming allows selection of 10-, 12-, 14- or 16-bit modes. This feature allows selection of either low-resolution for fast tracking or higher resolution for higher accuracy.

The velocity outputs (VEL A, VEL B) of the SD-14620 Series, which can be used to replace a tachometer, are ±4 V signals referenced to analog ground. The SD-14620 Series also offers Built-In-Test outputs for each channel ($\overline{\text{BIT}}$-A, $\overline{\text{BIT}}$-B). The converters are available with operating temperature ranges of 0°C to +70°C, -40°C to +85°C and -55°C to +125°C. MIL-PRF-38534 processing is available.

APPLICATIONS

With its low-cost, small size, high accuracy and versatile performance, the SD-14620 Series converters are ideal for use in modern high-performance military, commercial and position control systems. Typical applications include radar antenna positioning, motor control, robotics, navigation and fire control systems.

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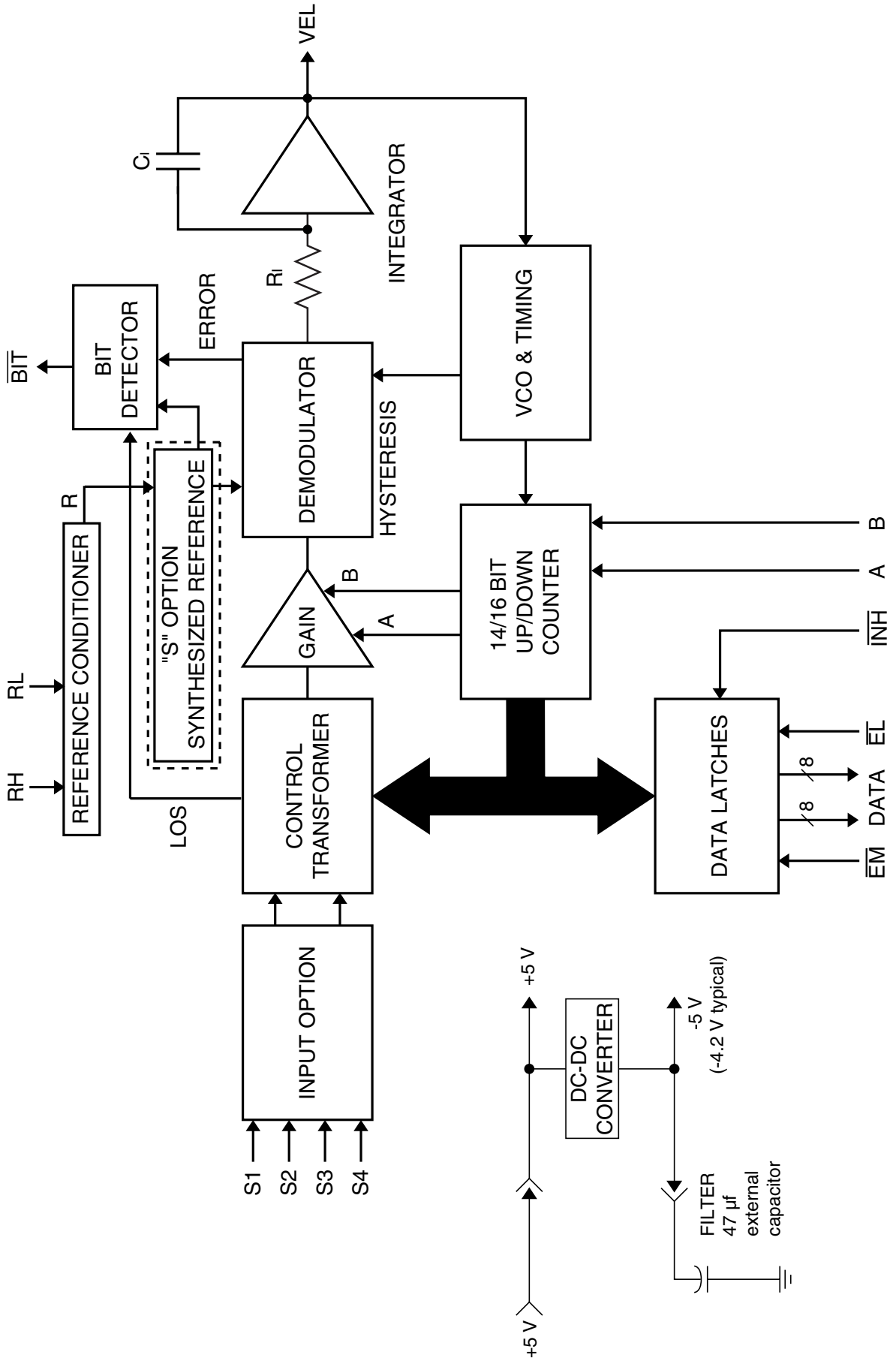


FIGURE 1. SD-14620 BLOCK DIAGRAM (ONE CHANNEL)

TABLE 1. SD-14620 SERIES SPECIFICATIONS (EACH CHANNEL)

These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion.

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	programmable 10, 12, 14, or 16	
ACCURACY	Min	±1, ±2 or ±4, + 1 LSB (see TABLE 5)	
REPEATABILITY	LSB	1 max.	
DIFFERENTIAL LINEARITY	LSB	1 max.	
REFERENCE INPUT		(RH, RL)	
Type		**Each Channel**	
		differential	
SD-14620		**2 & 11.8 V UNITS**	**90 V UNIT**
Voltage Range	Vrms	2-35	10-130
Frequency	Hz	360 - 5K	60 (47-5K) 400 (360-5K)
Input Impedance			
single ended	Ohm	60K	270K min.
differential	Ohm	120K	540K min.
Common-Mode Range	Vpeak	50, 100 transient	200, 300 transient
SD-14620XS			
Voltage Range	Vrms	2-35	—
Frequency	Hz	1K - 5K	—
Input Impedance			
single ended	Ohm	40K	—
differential	Ohm	80K	—
Common-Mode Range	Vpeak	50, 100 transient	—
±Sig/Ref Phase Shift	deg.	45 max	—
SIGNAL INPUT CHARACTERISTICS			
90 V Synchro Input (L-L)			
Zin line-to-line	Ohm	123K	
Zin line-to-ground	Ohm	80K	
Common-Mode Voltage	V	180 max.	
11.8 V Synchro Input (L-L)			
Zin line-to-line	Ohm	52K	
Zin line-to-ground	Ohm	34K	
Common-Mode Voltage	V	30 max.	
11.8 V Resolver Input (L-L)		(same for “S” option)	
Zin line-to-line	Ohm	140K	
Zin line-to-ground	Ohm	70K	
Common-Mode Voltage	V	30 max.	
2 V Direct Input (L-L)			
Voltage Range	Vrms	2 nom, 2.3 max.	
Max. Voltage w/o Damage	V	25 cont, 100 pk transient	
Input Impedance	Ohm	20 M ‖ 10 pF min.	
2 V Resolver Input (L-L)		(“S” option only)	
Zin single ended	Ohm	11K	
Zin differential	Ohm	22K	
Common-Mode Voltage	V	4.9 max.	
DIGITAL INPUT/OUTPUT			
Logic Type		TTL/CMOS compatible	
INPUTS		Logic 0 = 0.8 V max. Logic 1 = 2.0 V min. Loading (per channel) =10 µA max P.U. current source to +5 V ‖ 5 pF max. CMOS transient protected.	

TABLE 1. SD-14620 SERIES SPECIFICATIONS (CONTINUED)

PARAMETER	UNIT	VALUE
DIGITAL INPUT/OUTPUT		
INPUTS (CONTINUED)		
Each Channel		**Each Channel**
Resolution Control		See TABLE 2.
Inhibit ($\overline{\text{INH}}$) (common)		Logic 0 inhibits; Data stable within 0.5 µs (Logic 1 is transparent)
Enable Bits 1 to 8 ($\overline{\text{EM}}$)		Logic 0 enables; Data stable within 150 ns (Transparent mode)
Enable Bits 9 to 16 ($\overline{\text{EL}}$)		Logic 1 = High Impedance, Data High Z within 100 ns
OUTPUTS		**Common to all Channels**
Parallel Data	bits	16 parallel lines; 2 bytes natural binary angle, positive logic. (see TABLE 3)
Each Channel		**Each Channel**
Built-In-Test		Logic 0 = BIT condition. ~ ± 100 LSBs of error with a filter of 500 µs for LOS. (LOS and LOR for "S" option)
Drive Capability	TTL	50 PF + Logic 0; 1 TTL load, 1.6 mA at 0.5 V max Logic 1; 10 TTL loads, -0.4 mA at 2.8 V min
	CMOS	Logic 0; 100mV max. Logic 1; +5 V supply minus 100 mV min.
VELOCITY CHARACTERISTICS (see Note 1)		**Each Channel**
Polarity		Positive for increasing angle
Voltage Range (Full Scale)	±V	4.0 typ. — 3.5 min.
Scale Factor	±%	10 typ. — 20 max.
Scale Factor TC	ppm/°C	100 typ. — 200 max.
Reversal Error	±%	1 typ. — 2 max.
Linearity	±%	0.5 typ. — 1 max.
Linearity (90 V/60 Hz)	±%	2 typ. — 3 max.
Zero Offset	mV	5 typ. — 10 max.
Zero Offset TC	µV/°C	15 typ. — 30 max.
Load	KOhm	20 min.
Noise	(Vp/V)%	0.125 min. (1 typ.) 2 max.
DC ERROR (E)	V	-1.25 per +1 LSB error filtered (±3 LSB range).
POWER SUPPLIES		
Nominal Voltage	V	+5
Voltage Tolerance	%	±5
Max. Voltage w/o Damage	V	+7
Current	mA	60 typ. — 70 max.
TEMPERATURE RANGE		
Operating		
-30X	°C	0 to +70
-20X	°C	-40 to +85
-10X	°C	-55 to +125
Junction-to-Case (JC)	°C/W	+55
JC Thermal Rise	°C	+9 (see Note 2)
Junction Temperature	°C	+140 max.
Storage	°C	-65 to +150
PHYSICAL CHARACTERISTICS		
Size	in (mm)	1.50 x 0.78 x 0.21 (36.75 x 19.81 x 5.33)
Weight	oz (g)	0.66 (18.71)

NOTE:
1. Refer to TABLE 4 for full-scale tracking rate.
2. Applied to operating temperature

THEORY OF OPERATION

The SD-14620 Series of converters are based upon a single chip CMOS custom monolithic. Using the latest technology, precision analog circuitry is merged with digital logic to form a complete, high-performance tracking Synchro/Resolver-to-Digital (S/D, R/D) converter.

CONVERTER OPERATION

FIGURE 1 is the Functional Block Diagram of the SD-14620 Series. The converter operates with a single +5 VDC power supply and each channel internally generates a negative voltage of approximately 5 volts. These negative voltages are connected to pin 52 (channel "A" filter point) and pin 24 (channel "B" filter point) — see GENERAL SETUP CONSIDERATIONS.

The converter is made up of three main sections; an input front-end, an error processor, and a digital interface. The converter front-end differs for synchro, resolver and direct inputs. An electronic Scott-T is used for synchro inputs, a resolver conditioner for resolver inputs, and a sine and cosine voltage follower for direct inputs. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 16-bit digital angle ϕ. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $SIN\theta COS\phi - COS\theta SIN\phi = SIN(\theta - \phi)$ using amplifiers, switches, logic, and capacitors in precision ratios. The converter accuracy is limited by the precision of the computing elements in the CT. For enhanced accuracy, the CT in these converters use capacitors in precision ratios, instead of the more conventional precision resistor ratios. Capacitors that are used as computing elements with op-amps are sampled at a high rate to eliminate drift and the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The DC error is integrated yielding a velocity voltage which in turn drives a voltage-controlled oscillator (VCO). This VCO is an incremental integrator (constant-voltage input to position-rate output) that, together with the velocity integrator, forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and a lag at a higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above.

TABLE 2. RESOLUTION CONTROL (A AND B)

RESOLUTION	B	A
10 bit	0	0
12 bit	0	1
14 bit	1	0
16 bit	1	1

GENERAL SET-UP CONSIDERATIONS

The following recommendations should be considered when connecting the SD-14620 Series converters:

1) The +5 VDC power supply input is on pin 18. For performance with the lowest amount of noise it is recommended that a 10 µF/10 VDC (or larger) tantalum filter capacitor be connected to ground (pin 19) near the converter package.

2) Direct inputs are referenced to Analog Ground (A GND). Connections should be made as close to the converter package as possible to minimize noise. Channel A should be referenced to A GND-A (pin 5) and Channel B should be referenced to A GND-B (pin 32).

3) A 47 µF/10 V tantalum filter capacitor must be added externally from pin 52 (channel "A" filter point) to pin 19 (ground). In addition, a 47 µF/10 Vdc tantalum filter capacitor must be added externally from pin 24 (channel "B" filter point) to pin 19 (ground).

SPECIAL FUNCTIONS

PROGRAMMABLE RESOLUTION

Resolution is controlled by pins 49 and 50 for channel A; pins 21 and 22 for channel B. The resolution can be changed during converter operation, so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist between counting and changing the resolution, the resolution control is latched internally. Refer to TABLE 2 for Channel A and B resolution control.

TABLE 3. DIGITAL ANGLE OUTPUTS

BIT	DEG/BIT	MIN/BIT
1 (MSB ALL MODES)	180	10800
2	90	5400
3	45	2700
4	22.5	1350
5	11.25	675
6	5.625	337.5
7	2.813	168.75
8	1.406	84.38
9	0.7031	42.19
10 (LSB 10-BIT MODE)	0.3516	21.09
11	0.1758	10.55
12 (LSB 12-BIT MODE)	0.0879	5.27
13	0.0439	2.64
14 (LSB 14-BIT MODE)	0.0220	1.32
15	0.0110	0.66
16 (LSB 16-BIT MODE)	0.0055	0.33

Note: $\overline{EM}$ enables the MSB byte and $\overline{EL}$ enables the LSB byte.

$\overline{\text{BIT}}$, (BUILT-IN-TEST)

This output is an active low logic line that will flag an internal fault condition or LOS (Loss-Of-Signal). The internal fault detector monitors the internal loop error and, when it exceeds approximately ±100 LSBs, will set the line to a logic 0. This condition will occur during a large-step input and will reset to a logic 1 after the converter settles out. (The $\overline{\text{BIT}}$ is filtered with a 500 µs delay.) $\overline{\text{BIT}}$ will set for an overvelocity condition because the converter loop can not maintain input/output sync. For the "S" option only, this output will be active low for an LOR (Loss-Of-Reference) fault condition.

NO FALSE 180° HANGUP

The converter is designed to eliminate a "false 180° reading" during instantaneous 180° step changes. This condition most often occurs when the input is "electronically switched" from a Digital-to-Synchro converter. If the "MSB" (or 180° bit) is "toggled" on and off, a converter without the "false 180° hangup" feature may fail to respond. The condition is artificial, as a "real" synchro or resolver cannot change its output 180° instantaneously. The condition is most often noticed during wraparound verification tests, simulations, or troubleshooting.

SYNTHESIZED REFERENCE

The synthesized reference section ("S" option) eliminates errors due to phase shift between the reference and signal inputs of up to 45°. Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. Due to the inductive nature of synchros and resolvers, their output signals lead the reference input signal (RH and RL). When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. As shown in FIGURE 1, the converter synthesizes its own internal reference signal based on the SIN and COS signal inputs. Therefore, the phase of the synthesized (internal) reference is determined by the signal input, resulting in reduced quadrature errors. The synthesized reference circuit also eliminates the 180 degree false error null hang up.

INTERFACING

SOLID-STATE BUFFER PROTECTION - TRANSIENT VOLTAGE SUPPRESSION

The solid-state signal and reference inputs are true differential inputs with high AC and DC common rejection, so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The recurrent AC peak + DC common-mode voltage should not exceed the values in TABLE 1.

The 90 V line-to-line systems may have voltage transients which exceed the 300 V specification listed in TABLE 1. **These transients can destroy the thin-film input resistor network in the hybrid.** Therefore, 90 V L-L solid-state input modules may be protected by installing voltage suppressors (See FIGURE 2). Voltage transients are likely to occur whenever a synchro is switched on and off. For instance, a 1000 V transient can be generated when the primary of a CX or TX input is opened.

INHIBIT AND ENABLE TIMING

The Inhibit ($\overline{\text{INH}}$) signal is used to freeze the digital output angle in the transparent output data latch while the data is being transferred. Application of an inhibit signal does not interfere with the continuous tracking of the converter. As shown in FIGURE 3, angular output data is valid 500 nanoseconds (maximum) after the application of the low-going Inhibit pulse.

Output angle data is enabled onto the tri-state data bus in 16 bits. This Enable MSB ($\overline{\text{EM}}$-A or $\overline{\text{EM}}$-B) is used for the most significant 8 bits and Enable LSB ($\overline{\text{EL}}$-A or $\overline{\text{EL}}$-B) is used for the least significant bits. As shown in FIGURE 4, output data is valid 150 nanoseconds (maximum) after the application of a low-going enable pulse. The tri-state data bus returns to the high impedance state 100 nanoseconds (maximum) after the rising edge of the enable signal.

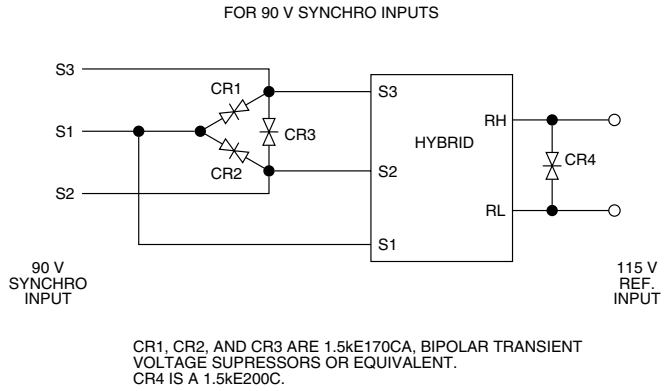


FIGURE 2. CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS

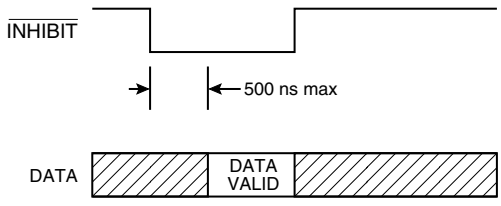


FIGURE 3. INHIBIT TIMING

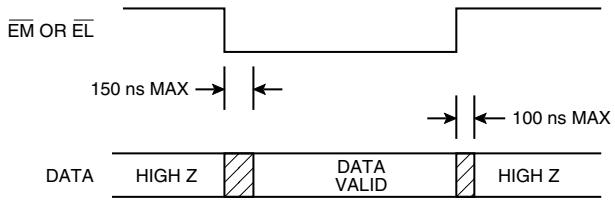


FIGURE 4. ENABLE TIMING

TABLE 4. DYNAMIC CHARACTERISTICS

EACH CHANNEL		DEVICE TYPE											
		60 Hz				400 Hz				"S" OPTION			
Input Frequency	Hz	47 - 5K				360 - 5K				1K - 5K			
Bandwidth (Closed Loop)	Hz	15				56				150			
Ka	$1/s^2$	830				17K				110K			
A1	1/s	0.17				0.41				2.47			
A2	1/s	5K				41K				44.4K			
A	1/s	29				130				333			
B	1/s	14.5				81				166			
RESOLUTION	**BITS**	**10**	**12**	**14**	**16**	**10**	**12**	**14**	**16**	**10**	**12**	**14**	**16**
Tracking Rate (rps)													
typical (Note 1)	rps	32	8	2	0.5	160	40	10	2.5	160	40	10	2.5
minimum	rps	25.6	6.4	1.6	0.4	128	32	8	2	128	32	8	2
Acceleration (1 LSB lag)	deg/s^2	720	180	45	11.3	5950	1490	372	93	39K	9760	2440	610
Settling Time (179° step max)	msec	400	500	1100	2500	90	100	180	360	51	78	150	232

Note 1: Velocity output is scaled for 3.5V at typical tracking rates per resolution shown.

DYNAMIC PERFORMANCE

A type II servo loop (Kv = ∞) and very high acceleration constants give the SD-14620 superior dynamic performance.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Functional Block Diagram (FIGURE 1), its transfer function block diagram (FIGURE 5), and its Bode Plots (open and closed loop - FIGURE 6). Values for the transfer function block can be obtained from TABLE 4.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient
and B is the frequency of lead compensation

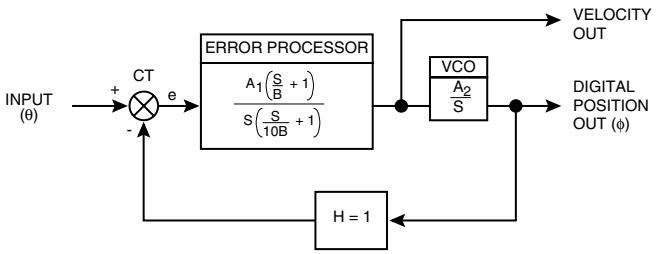
ACCURACY AND RESOLUTION

TABLE 5 lists the total accuracy including quantification of the various resolutions and accuracy grades.

TABLE 5. ACCURACY/RESOLUTION

VERSION	ACCURACY (minutes)	RESOLUTION (minutes)			
		10 BIT	12 BIT	14 BIT	16 BIT
SD-1462X-XX	±4 +1 LSB ±2 +1 LSB	42.2 42.2	10.5 10.5	5.3 3.3	4.3 2.3
SD-1462X-XS ("S" option)	±4 +1 LSB ±2 +1 LSB ±1 +1 LSB	25.1 23.1 22.1	9.3 7.3 6.3	5.3 3.3 2.3	4.3 2.3 * 1.3

* 1.3 minute accuracy available for "S" option only.
Inclusive of 1 bit of jitter.



$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)} \qquad \text{WHERE: } A^2 = A_1 A_2$$

FIGURE 5. TRANSFER FUNCTION BLOCK DIAGRAM

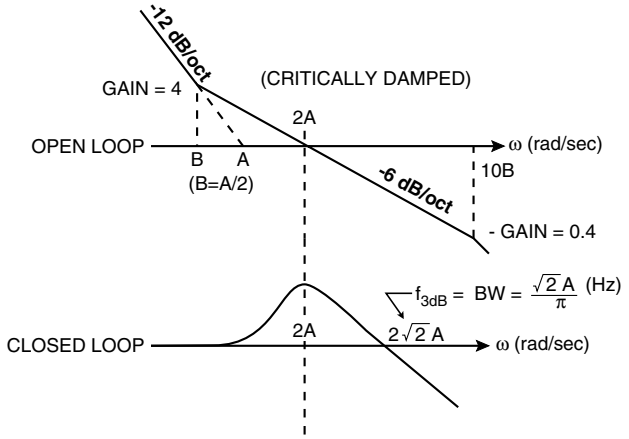
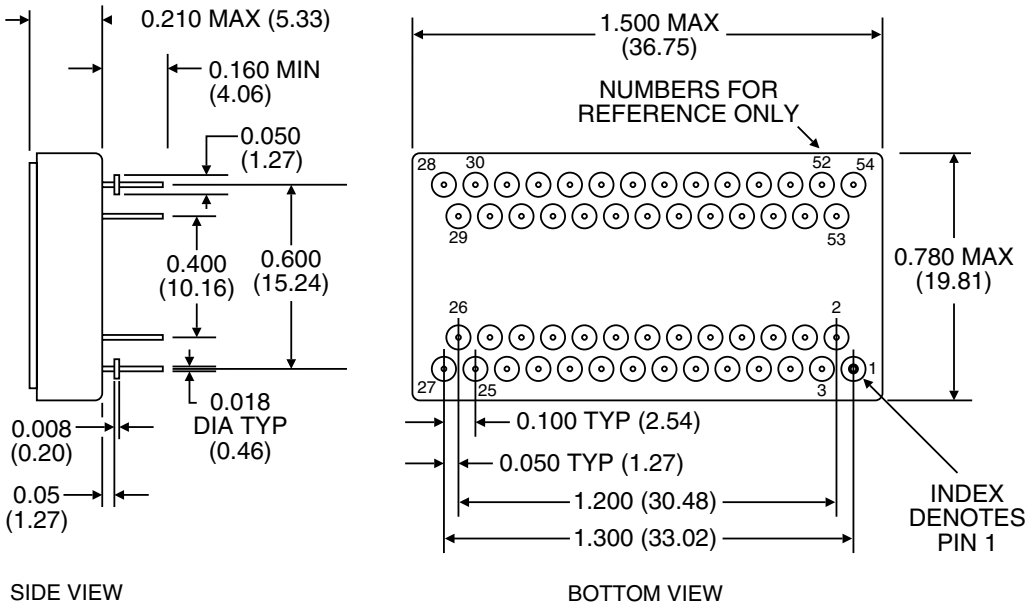


FIGURE 6. BODE PLOTS

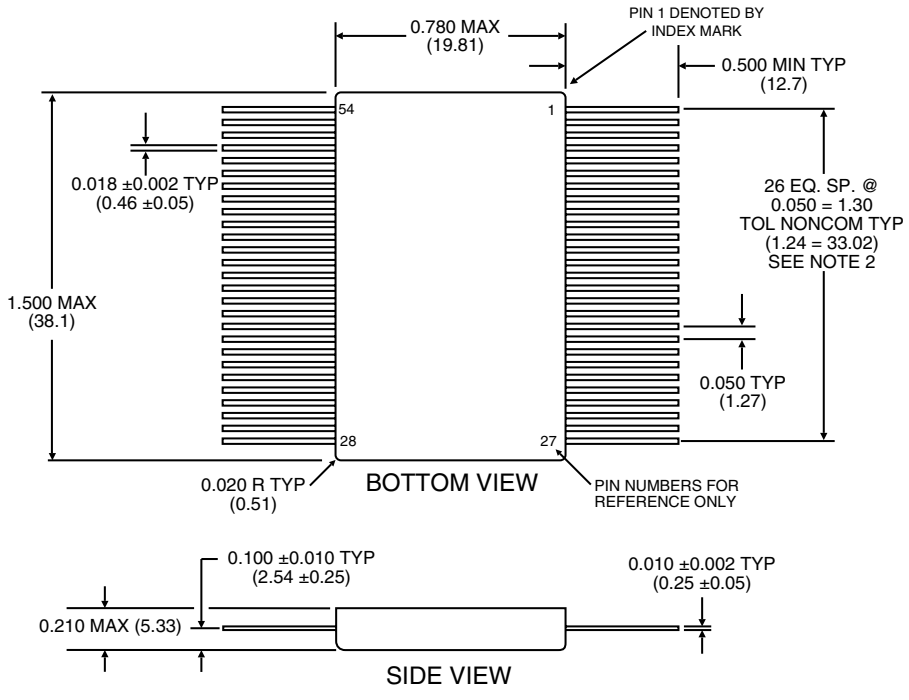
TABLE 6. PINOUTS (DIP AND FLAT PACK)							
PIN	**FUNCTION**			**PIN**	**FUNCTION**		
1	S1-A(R)	S1-A(S)	N.C.	54	VEL A (Velocity - chan. A)		
2	S2-A(R)	S2-A(S)	+COS-A(D)	53	E (DC error - channel A)		
3	S3-A(R)	S3-A(S)	+SIN-A(D)	52	Filter Point - channel A		
4	S4-A(R)	N.C.	N.C.	51	$\overline{\text{INH}}$-A (Inhibit chan. A)		
5	A GND-A (analog gnd. chan. A)			50	resolution control B (chan. A)		
6	RH-A (+Ref. Input chan. A)			49	resolution control A (chan. A)		
7	RL-A (-Ref. Input chan. A)			48	$\overline{\text{EL}}$-A (Enable LSBs chan. A)		
8	$\overline{\text{EM}}$-A (Enable MSBs chan. A)			47	N.C.		
9	$\overline{\text{BIT}}$-A (Built-In-Test chan. A)			46	Bit 16 (LSB, 16-bit mode)		
10	Bit 1 (MSB)			45	Bit 8		
11	Bit 9			44	Bit 15		
12	Bit 2			43	Bit 7		
13	Bit 10 (LSB, 10-bit mode)			42	Bit 14 (LSB, 14-bit mode)		
14	Bit 3			41	Bit 6		
15	Bit 11			40	Bit 13		
16	Bit 4			39	Bit 5		
17	Bit 12 (LSB, 12-bit mode)			38	$\overline{\text{BIT}}$-B (Built-In-Test chan. B)		
18	+5 V (Power Supply)			37	$\overline{\text{EM}}$-B (Enable MSBs chan. B)		
19	GND (Ground)			36	N.C.		
20	$\overline{\text{EL}}$-B (Enable LSBs chan. B)			35	RL-B (-Ref. Input chan. B)		
21	resolution control A (channel B)			34	RH-B (+Ref. Input chan. B)		
22	resolution control B (channel B)			33	N.C.		
23	$\overline{\text{INH}}$-B (Inhibit - chan. B)			32	A GND-B (analog gnd. chan. B)		
24	Filter Point - channel B			31	S4-B(R)	N.C.	N.C.
25	E (DC error - channel B)			30	S3-B(R)	S3-B(S)	SIN-B(D)
26	VEL B (Velocity - chan. B)			29	S2-B(R)	S2-B(S)	COS-B(D)
27	N.C.			28	S1-B(R)	S1-B(S)	N.C.

Notes:
1. (S) = Synchro; (R) = Resolver; (D) = 2 V Resolver Direct.
2. Connect a 47 µF/10 VDC tantalum filter cap from pin 24 to pin 19.
3. Connect a 47 µF/10 VDC tantalum filter cap from pin 52 to pin 19.
4. Connect a 10 µF/10 VDC tantalum filter cap from pin 18 to pin 19.



Notes:
1. Dimensions are in inches (mm).
2. Lead identification numbers are for reference only
3. Lead cluster shall be centered within ±0.005 (0.13) of outline dimensions.
   Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.
5. Case is hermetically sealed ceramic package.

FIGURE 7. SD-14620 DIP MECHANICAL OUTLINE



Notes:
1. Dimensions are in inches (mm).
2. Lead cluster shall be centralized about case centerline within ±0.010 (±0.254).

FIGURE 8. SD-14620 FLAT PACK MECHANICAL OUTLINE

ORDERING INFORMATION

SD-1462X X X - X X X X

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = 100% Pull Test
- Q = 100% Pull Test and Pre-Cap Source Inspection
- K = One Lot Date Code
- W = One Lot Date Code and Pre-Cap Source Inspection
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, Pre-Cap Source Inspection and 100% Pull Test
- Blank = None of the Above

Accuracy: (non "S" option)
- 2 = ±4 min + 1 LSB
- 4 = ±2 min + 1 LSB

Accuracy: ("S" option) (Note 3)
- 2 = ±4 min + 1 LSB
- 4 = ±2 min + 1 LSB
- 5 = ±1 min + 1 LSB

Reliability Grade:
- 0 = Standard DDC Processing, no Burn-In (See table on next page.)
- 1 = MIL-PRF-38534 Compliant (note 2)
- 2 = B (note 1)
- 3 = MIL-PRF-38534 Compliant (note 2) with PIND Testing
- 4 = MIL-PRF-38534 Compliant (note 2) with Solder Dip
- 5 = MIL-PRF-38534 Compliant (note 2) with PIND Testing and Solder Dip
- 6 = B (note 1) with PIND Testing
- 7 = B (note 1) with Solder Dip
- 8 = B (note 1) with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table on next page.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40° to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C + Variables Test Data
- 5 = -40°C to +85°C + Variables Test Data
- 8 = 0°C to +70°C + Variables Test Data

Options:
- X = None
- S = Synthesized Reference (note 3)

Package Type:
- D = DIP
- F = Flat Pack

Input Options: (non "S" option) (Note 4)
- 0 = 11.8 V, Synchro, 400 Hz
- 1 = 11.8 V, Resolver, 400 Hz
- 2 = 90 V, Synchro, 400 Hz
- 3 = 2 V, Direct, 400 Hz
- 4 = 90 V, Synchro, 60 Hz

Input Options: ("S" Option) (Notes 3, 4)
- 1 = 11.8 V, Resolver, 1 KHz
- 3 = 2 V, Resolver (Differential), 1 KHz

Notes:
1. Standard DDC processing with burn-in and full temperature test. See table on next page.
2. MIL-PRF-38534 product grading is designated with the following dash numbers:
   Class H is a -11X, 13X, 14X, 15X, 41X, 43X, 44X, 45X
   Class G is a -21X, 23X, 24X, 25X, 51X, 53X, 54X, 55X
   Class D is a -31X, 33X, 34X, 35X, 81X, 83X, 84X, 85X
3. "S" option selection categories.
4. See TABLE 4 for full frequency range specifications.
5. These products contain tin-lead solder finish as applicable to solder dip requirements.

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 (note 1), 1030 (note 2)	TABLE 1

Notes:
1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

Please visit our web site at **www.ddc-web.com** for the latest information.

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