

Features

- Fast Access Time Selection:
100ns/120ns/150ns/200ns
- Low Power Replacement for NMOS 2114 RAMs
- 883 Qualified Version: 883/21C14M
- Low Operating and Standby Current: 40mA/50 μ A
- Data Retention to 2.0V
- True TTL Compatibility
- Single 5V $\pm$ 10% Supply
- Fully Static Asynchronous Operation
- Three-State Outputs
- Common Data I/O Bus

Description

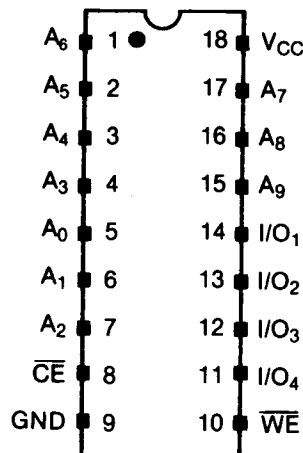
The SCM21C14 is a static silicon-gate CMOS RAM, a low-power replacement for the NMOS 2114 4K RAM. The device is fully static and requires no clocks.

The Common Data lines (I/O) allow for simple interfacing with most microprocessors. A Chip Enable input ($\overline{CE}$) is provided for memory expansion. The I/O lines are in a high impedance state when the chip is not selected ($\overline{CE} = 1$). The Write Enable ($\overline{WE}$) is used to select either the read ($\overline{WE} = 1$) or write ($\overline{WE} = 0$) mode.

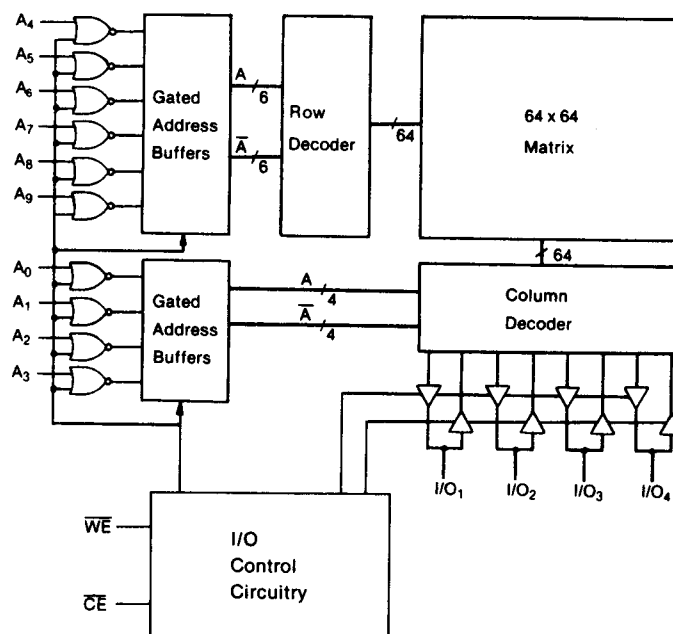
The SCM21C14 achieves its low standby power by using $\overline{CE}$ as a gating signal for the address buffers and output stages. This extends the $\overline{CE}$ access time to a point at least equal to the address access. For NMOS 2114 replacement applications, note the timing differences for $\overline{CE}$; where $\overline{CE}$ access is required to be faster than address access, use the SCM2114AL.

The SCM21C14 is available in industry standard 18 pin packages. The different versions of the SCM21C14 are outlined below.

Pin Configuration



Block Diagram



Operating Characteristics Summary

Type	Access Time t_A (max.)	Operating Current I_{CC} (max.)	Standby Current I_{CCL} (max.)
SCM21C14-1	100ns	40mA	50 μ A
SCM21C14-2	120ns	40mA	50 μ A
SCM21C14-3	150ns	40mA	50 μ A
SCM21C14-4	200ns	40mA	50 μ A
SCM21C14M	200ns	50mA	100 μ A
883/21C14M	200ns	50mA	100 μ A

Absolute Maximum Limits

DC Supply Voltage (V_{CC}):	− 0.5 to + 6.0V
Storage Temperature (T_S):	− 65° to + 150°C
Input Voltage (V_{IN}):	$(V_{SS} - 0.3V) \leq V_{IN} \leq (V_{CC} + 0.3V)$

Recommended Operating Conditions

Parameter	Limits
DC Supply Voltage (V_{CC})	5V $\pm$ 10%
Operating Temperature (T_A)	
21C14-1/-2/-3/-4	0° to + 70°C
21C14M	− 55° to 125°C

Pin Description

$A_{0,9}$	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$I/O_{1,4}$	Data In/Out

Truth Table

$\overline{CE}$	$\overline{WE}$	$I/O_{0,3}$	Mode
1	X	High Z	Not Selected
0	1	Outputs	Read
0	0	Inputs	Write

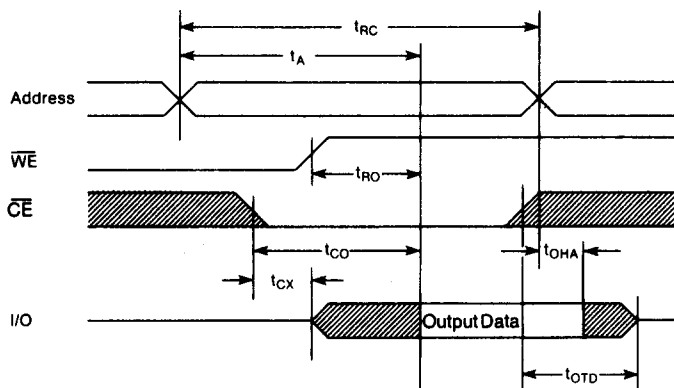
D. C. Characteristics ($V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Min.	Typ. ⁽¹⁾	Max.	Units	Test Conditions
I _{IL}	Input Current			1.0	μA	I _{OL} = 3.2mA I _{OH} = − 1.0mA V _{IH} /V _{IL} = 2.0/0.8V V _{IH} /V _{IL} = 2.0/0.8V CE ≥ V _{CC} − 0.4V CE ≥ V _{CC} − 0.4V
I _{LO}	Output Leakage Current			1.0	μA	
V _{IL}	Input Low Voltage			0.8	V	
V _{IH}	Input High Voltage	2.0			V	
V _{OL}	Output Low Voltage			0.4	V	
V _{OH}	Output High Voltage	2.4			V	
I _{CC}	Operating Current 21C14		30	40	mA	
I _{CC}	Operating Current 21C14M		30	50	mA	
I _{CCL}	Standby Current 21C14		10	50	μA	
I _{CCL}	Standby Current 21C14M		10	100	μA	
Low V _{CC} Data Retention Characteristics						
V _{DR}	V _{CC} Data Retention	2.0			V	CE ≥ V _{CC} − 0.4V
I _{CCDR}	Data Retention Current			25	μA	CE ≥ V _{CC} − 0.4V
t _R	Recovery Time	t _{RC}			ns	t _{RC} = Read Cycle Time
t _{CDR}	Chip Disable to Data Retention Time	0			ns	

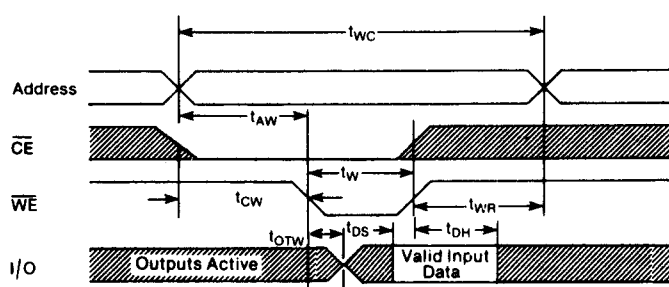
A. C. Characteristics⁽²⁾ ($V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	21C14-1 Min. Max.	21C14-2 Min. Max.	21C14-3 Min. Max.	21C14-4 Min. Max.	21C14M Min. Max.	Units
Read Cycle							
t_{RC}	Read Cycle	100	120	150	200	200	ns
t_A	Access from Address		120	150	200	200	ns
t_{CO}	Chip Enable to Output Valid		120	150	200	200	ns
t_{CX}	Chip Enable to Output Active	5	5	5	5	5	ns
t_{RO}	Read to Output Valid		90	120	120	120	ns
t_{OTD}	Chip Enable to Output Float		35	40	50	50	ns
t_{OHA}	Output Hold from Address Change	5	5	5	5	5	ns
Write Cycle							
t_{WC}	Write Cycle	100	120	150	200	200	ns
t_{AW}	Address to Write	40	45	50	75	75	ns
t_{CW}	Chip Enable to Write	40	45	50	75	75	ns
t_W	Write Pulse Width	60	75	100	125	125	ns
t_{DS}	Data Setup	60	75	100	125	125	ns
t_{DH}	Data Hold	0	0	0	0	0	ns
t_{OTW}	Write to Output Float		35	40	50	50	ns
t_{WR}	Write Recovery	0	0	0	0	0	ns

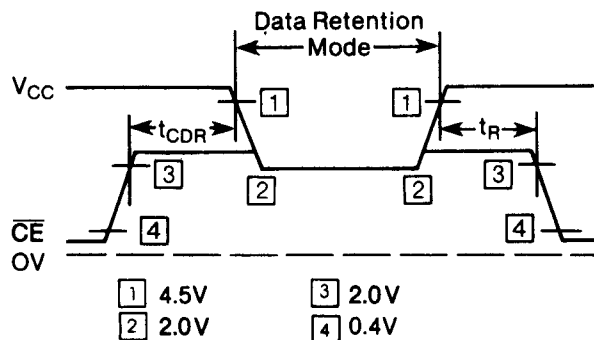
Read Cycle



Write Cycle



Low V_{CC} Data Retention Waveform



1. $T_A = 25^\circ\text{C}$; $V_{CC} = 5.0V$
2. A.C. TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
 Input Rise/Fall Times: $\leq 10\text{ns}$
 Time Measurement Reference Level: 1.5V
 Output Load: 1 TTL Load and $C_L = 100\text{pF}$