

SCAN90CP02 1.5 Gbps 2x2 LVDS Crosspoint Switch with Pre-Emphasis and IEEE 1149.6

Check for Samples: SCAN90CP02

FEATURES

- 1.5 Gbps per channel
- Low power: 70 mA in dual repeater mode @1.5 Gbps
- Low output jitter
- Configurable 0/25/50/100% pre-emphasis drives lossy backplanes and cables
- Non-blocking architecture allows 1:2 splitter, 2:1 mux, crossover, and dual buffer configurations

- Flow-through pinout
- LVDS/BLVDS/CML/LVPECL inputs, LVDS Outputs
- IEEE 1149.1 and 1149.6 compliant
- Single 3.3V supply
- Separate control of inputs and outputs allows for power savings
- Industrial -40 to +85°C temperature range
- 28-lead LLP package, or 32-lead LQFP package

DESCRIPTION

The SCAN90CP02 is a 1.5 Gbps 2 x 2 LVDS crosspoint switch. High speed data paths and flow-through pinout minimize internal device jitter, while configurable 0/25/50/100% pre-emphasis overcomes external ISI jitter effects of lossy backplanes and cables. The differential inputs interface to LVDS and Bus LVDS signals such as those on National's 10-, 16-, and 18- bit Bus LVDS SerDes, as well as CML and LVPECL. The SCAN90CP02 can also be used with ASICs and FPGAs. The non-blocking crosspoint architecture is pin-configurable as a 1:2 clock or data splitter, 2:1 redundancy mux, crossover function, or dual buffer for signal booster and stub hider applications.

Integrated IEEE 1149.1 (JTAG) and 1149.6 circuitry supports testability of both single-ended LVTTL/CMOS and differential LVDS PCB interconnect. The 3.3V supply, CMOS process, and LVDS I/O ensure high performance at low power over the entire industrial -40 to +85°C temperature range.

Block Diagram



Figure 1. SCAN90CP02 Block Diagram

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Pin Functions

Pin Descriptions

Pin Name	LLP Pin Number	LQFP Pin Number	I/O, Type	Description
DIFFEREN	TIAL INPU	гѕ соммо	N TO ALL MUXES	
IN0+ IN0-	9 10	9 10	I, LVDS	Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
IN1+ IN1-	12 13	13 14	I, LVDS	Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
SWITCHED	DIFFERE	NTIAL OUT	PUTS	
OUT0+ OUT0-	27 26	32 31	O, LVDS	Inverting and non-inverting differential outputs. $OUT0\pm$ can be connected to any one pair IN0±, or IN1±. LVDS compatible ⁽¹⁾ .
OUT1+ OUT1-	24 23	28 27	O, LVDS	Inverting and non-inverting differential outputs. $OUT1\pm$ can be connected to any one pair IN0±, or IN1±. LVDS compatible ⁽²⁾ .
DIGITAL C		TERFACE		
SEL0, SEL1	6 5	7 6	I, LVTTL	Select Control Inputs
EN0, EN1	7 15	8 17	I, LVTTL	Output Enable Inputs
PEM00, PEM01	4 3	4 3	I, LVTTL	Channel 0 Output Pre-emphasis Control Inputs
PEM10, PEM11	2 1	2 1	I, LVTTL	Channel 1 Output Pre-emphasis Control Inputs
TDI	19	22	I, LVTTL	Test Data Input to support IEEE 1149.1 features
TDO	20	23	O, LVTTL	Test Data Output to support IEEE 1149.1 features
TMS	18	21	I, LVTTL	Test Mode Select to support IEEE 1149.1 features
ТСК	17	19	I, LVTTL	Test Clock to support IEEE 1149.1 features
TRST	21	24	I, LVTTL	Test Reset to support IEEE 1149.1 features
N/C	8, 28			Not Connected
POWER		1		
V _{DD}	11, 14, 16, 22, 25	12, 16, 18, 25, 29	I, Power	V_{DD} = 3.3V ±0.3V. At least 4 low ESR 0.01 μF bypass capacitors should be connected from V_{DD} to GND plane.
GND	(3)	5, 11, 15, 20, 26, 30		Ground reference to LVDS and CMOS circuitry. For the LLP package, the DAP is used as the primary GND connection to the device. The DAP is the exposed metal contact at the bottom of the LLP-28 package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance.

(1) The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the SCAN90CP02 device have been optimized for point-to-point backplane and cable applications.

(2) The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the SCAN90CP02 device have been optimized for point-to-point backplane and cable applications.

(3) Note that for the LLP package GND is not an actual pin on the package, the GND is connected thru the DAP on the back side of the LLP package.



Connection Diagram







Configuration Select Truth Table⁽⁴⁾

SEL0	SEL1	EN0	EN1	OUT0	OUT1	Mode
0	0	0	0	IN0	IN0	1:2 Splitter (IN1 powered down)
0	1	0	0	IN0	IN1	Dual Channel Repeater
1	0	0	0	IN1	IN0	Dual Channel Switch
1	1	0	0	IN1	IN1	1:2 Splitter (IN0 powered down)
0	1	0	1	IN0	PD	Single Channel Repeater (Channel 1 powered down)
1	1	0	1	IN1	PD	Single Channel Switch (IN0 and OUT1 powered down)
0	0	1	0	PD	IN0	Single Channel Switch (IN1 and OUT0 powered down)
0	1	1	0	PD	IN1	Single Channel Repeater (Channel 0 powered down)
Х	Х	1	1	PD	PD	Both Channels in Power Down Mode

(4) PD = Power Down mode to minimize power consumption X = Don't Care



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SEL0	SEL1	EN0	EN1	OUT0	OUT1	Mode
0	0	0	1			Invalid State ⁽¹⁾
1	0	0	1			Invalid State ⁽¹⁾
1	0	1	0			Invalid State ⁽¹⁾
1	1	1	0			Invalid State ⁽¹⁾

(1) Entering these states is not forbidden, however device operation is not defined in these states.

Pre-Emphasis

The pre-emphasis is used to compensate for long or lossy transmission media. Separate pins are provided for each output to minimize power consumption. Pre-emphasis is programmable to be off or to preset values per Table 1.

Output Characteristics

The output characteristics of the SCAN90CP02 device have been optimized for point-to-point backplane and cable applications.

Chan	inel 0	Char	Pre-emphasis	
PEM01	PEM00	PEM11	PEM10	
0	0	0	0	0%
0	1	0	1	25%
1	0	1	0	50%
1	1	1	1	100%

Table 1. Pre-emphasis Control Selection Table



Applications Information



Dual Channel Repeater















Figure 4. SCAN90CP02 Configuration Select Decode

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



Absolute Maximum Ratings ⁽¹⁾

Supply Voltage (V _{DD})	-0.3V to +4.0V
CMOS Input Voltage	-0.3V to (V _{DD} +0.3V)
LVDS Receiver Input Voltage	-0.3V to +3.6V
LVDS Driver Output Voltage	-0.3V to +3.6V
LVDS Output Short Circuit Current	40mA
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
LLP-28	4.31 W
LQFP-32	1.47 W
Derating above 25°C	
LLP-28	34.5 mW/°C
LQFP-32	11.8 mW/°C
Thermal Resistance, θ_{JA}	
LLP-28	29°C/W
LQFP-32	85°C/W
ESD Rating	
HBM, 1.5 kΩ, 100 pF	6.5 kV
EIAJ, 0Ω, 200 pF	>250V

(1) "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Recommended Operating Conditions

	Min	Тур	Max	Unit
Supply Voltage (V _{DD} - GND)	3.0	3.3	3.6	V
Receiver Input Voltage	0		3.6	V
Operating Free Air Temperature	-40	25	85	°C
Junction Temperature			150	°C



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Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Тур (1)	Max	Units
LVTTL DO	C SPECIFICATIONS (SEL0, SEL1, EN	I, EN2, PEM00, PEM01, PEM10, PEM11, T	DI, TCK, TM	S, TRST)	1	
VIH	High Level Input Voltage		2.0		V _{DD}	V
VIL	Low Level Input Voltage		GND		0.8	V
I _{IH}	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	-10		+10	μA
I _{IL}	Low Level Input Current	$V_{IN} = V_{SS}, V_{DD} = V_{DDMAX}$	-10		+10	μA
I _{ILR}	Low Level Input Current	TDI, TMS, TRST	-40		-200	μA
C _{IN1}	Input Capacitance	Any Digital Input Pin to V _{SS}		3.5		pF
C _{OUT1}	Output Capacitance	Any Digital Output Pin to V _{SS}		5.5		pF
V _{CL}	Input Clamp Voltage	I _{CL} = −18 mA	-1.5	-0.8		V
V _{OH}	High Level Output Voltage	I _{OH} = −12 mA, V _{DD} = 3.0 V	2.4			V
	(TDO)	$I_{OH} = -100 \ \mu A, V_{DD} = 3.0 \ V$	V _{DD} -0.2			V
V _{OL}	Low Level Output Voltage	$I_{OL} = 12 \text{ mA}, V_{DD} = 3.0 \text{ V}$			0.5	V
	(TDO)	I _{OL} = 100 μA, V _{DD} = 3.0 V			0.2	V
los	Output Short Circuit Current	TDO	-15		-125	mA
	PUT DC SPECIFICATIONS (IN0±, IN1±)				1
V _{TH}	Differential Input High Threshold ⁽²⁾	$V_{CM} = 0.8V$ or 1.2V or 3.55V, $V_{DD} = 3.6V$		0	100	mV
VTI	Differential Input Low Threshold	$V_{CM} = 0.8V \text{ or } 1.2V \text{ or } 3.55V. V_{DD} = 3.6V$	-100	0		mV
Vin	Differential Input Voltage	$V_{CM} = 0.8V$ to 3.55V. $V_{DD} = 3.6V$	100			mV
VCMP	Common Mode Voltage Range	$V_{\rm ID} = 150 \text{ mV}$. $V_{\rm DD} = 3.6 \text{ V}$	0.05		3.55	V
	Input Capacitance	$IN+$ or $IN-$ to V_{SS}		3.5		pF
	Input Current	$V_{\rm IN} = 3.6V V_{\rm DD} = V_{\rm DDMAX} \text{ or } 0V \qquad -10$			+10	uA
-111		$V_{\rm IN} = 0V$, $V_{\rm DD} = V_{\rm DDMAX}$ or $0V$	-10		+10	uA
LVDS OU	TPUT DC SPECIFICATIONS (OUT0±.	OUT1±)				P
V _{OD}	Differential Output Voltage, 0% Pre-emphasis ⁽²⁾	$R_L = 100\Omega$ between OUT+ and OUT-	250	400	575	mV
ΔV_{OD}	Change in V _{OD} between Complementary States		-35		35	mV
V _{OS}	Offset Voltage (3)		1.09	1.25	1.475	V
ΔV_{OS}	Change in V _{OS} between Complementary States		-35		35	mV
I _{OS}	Output Short Circuit Current, One Complementary Output	OUT+ or OUT- Short to GND		-60	-90	mA
C _{OUT2}	Output Capacitance	OUT+ or OUT- to GND when TRI- STATE [®]		5.5		pF
SUPPLY	CURRENT (Static)	1				1
I _{CC0}	Supply Current	All inputs and outputs enabled and active, terminated with differential load of 100Ω between OUT+ and OUT		42	60	mA
I _{CC1}	Supply Current - one channel powered down	Single channel crossover switch or single channel repeater modes (1 channel active, one channel in power down mode)		22	30	mA
I _{CC2}	Supply Current - one input powered down	Splitter mode (One input powered down, both outputs active)		30	40	mA
I _{CCZ}	TRI-STATE Supply Current	Both input/output Channels in Power Down Mode		1.4	2.5	mA

Typical parameters are measured at $V_{DD} = 3.3V$, $T_A = 25^{\circ}C$. They are for reference purposes, and are not production-tested. Differential output voltage V_{OD} is defined as ABS(OUT+-OUT-). Differential input voltage V_{ID} is defined as ABS(IN+-IN-). Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states. (1)

(2) (3)

STRUMENTS

EXAS

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions		Min	Тур (1)	Мах	Units
SWITCHIN	NG CHARACTERISTICS—LVDS OUT	PUTS (Figure 5, Figure 6)					
t _{LHT}	Differential Low to High Transition Time	Use an alternating 1 and 0 pattern Mb/s, measure between 20% and	rn at 200 d 80% of	70	150	215	ps
t _{HLT}	Differential High to Low Transition Time	V _{OD} .		50	135	180	ps
t _{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern Mb/s, measure at 50% V _{OD} betw	rn at 200 een	0.5	2.4	3.5	ns
t _{PHLD}	Differential High to Low Propagation Delay	input to output.		0.5	2.4	3.5	ns
t _{SKD1}	Pulse Skew	t _{PLHD} -t _{PHLD}			55	120	ps
t _{SKCC}	Output Channel to Channel Skew	Difference in propagation delay (t _{PHLD}) among all output channels Splitter mode (any one input to a outputs).	t _{PLHD} or s in II	0	130	315	ps
tJIT	Jitter (0% Pre-emphasis)	RJ - Alternating 1/0 @ 750 MHz	(5)		1.4	2.5	psrms
	(4)	DJ - K28.5 Pattern	LQFP		110	140	psp-p
		1.5 Gbps ⁽⁶⁾	LLP		42	75	psp-p
		TJ - PRBS 2 ²³ -1 Pattern	LQFP		113	148	psp-p
		1.5 Gbps ⁽⁷⁾	LLP		93	126	psp-p
t _{ON}	LVDS Output Enable Time	Time from ENx to OUT± change TRI-STATE to active.	from	50	110	150	ns
t _{OFF}	LVDS Output Disable Time	Time from $\overline{\text{ENx}}$ to OUT change active to TRI-STATE.	from		5	12	ns
t _{SW}	LVDS Switching Time SELx to OUT±	Time from configuration select (S new switch configuration effective OUT±.	SELx) to e for		110	150	ns

(4) Jitter is not production tested, but guaranteed through characterization on a sample basis.

Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage = VID = 500mV, 50% (5) duty cycle at 750MHz, $t_r = t_f = 50ps$ (20% to 80%).

(6) Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. The input voltage = V_{ID} = 500mV, K28.5

pattern at 1.5 Gbps, $t_r = t_f = 50ps$ (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 110000101). Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture jitter has been subtracted. The input voltage = $V_{ID} = 500mV$, 2^{23} -1 PRBS pattern at 1.5 Gbps, $t_r = t_f = 50ps$ (20% to 80%).

(7)

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SCAN Circuitry Timing Requirements

Symbol	Parameter	Conditions	Min	Тур	Max	Units
f _{MAX}	Maximum TCK Clock Frequency	$R_L = 500\Omega$,	25.0			MHz
t _S	TDI to TCK, H or L	C _L = 35 pF	1.0			ns
t _H	TDI to TCK, H or L	_	2.0			ns
t _S	TMS to TCK, H or L		2.0			ns
t _H	TMS to TCK, H or L		1.5			ns
t _W	TCK Pulse Width, H or L		10.0			ns
t _W	TRST Pulse Width, L		2.5			ns
t _{REC}	Recovery Time, TRST to TCK		2.0			ns

Timing Diagrams



Figure 5. LVDS Signals



Figure 6. LVDS Output Transition Time



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Figure 7. LVDS Output Propagation Delay



Figure 8. Configuration and Output Enable/Disable Timing

Input Interfacing

The SCAN90CP02 accepts differential signals and allow simple AC or DC coupling. With a wide common mode range, the SCAN90CP02 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers.



Figure 9. Typical LVDS Driver DC-Coupled Interface to SCAN90CP02 Input





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Figure 11. Typical LVPECL Driver DC-Coupled Interface to SCAN90CP02 Input

Output Interfacing

The SCAN90CP02 outputs signals that are compliant to the LVDS standard. Their outputs can be DC-coupled to most common differential receivers. Figure 12 illustrates typical DC-coupled interface to common differential receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.





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Dynamic power supply current was measured while running a PRBS Total Jitter measured at 0V differential while running a PRBS 2²³-1 2²³-1 pattern in dual channel repeater mode. V_{CC} = 3.3V, T_A = +25°C, pattern in single channel repeater mode. V_{CC} = 3.3V, T_A = +25°C, V_{ID} $V_{ID} = 0.5V, V_{CM} = 1.2V$



= 0.5V, 0% Pre-emphasis Positive Edge Transition

	vs.										
I	Pre-emphasis Level										
100 mV/Div											
25%	7										
0%											
			2	200 p	 s/Div						

Total Jitter measured at 0V differential while running a PRBS 2²³-1 pattern in dual channel repeater mode. V_{CC} = 3.3V, V_{ID} = 0.5V, V_{CM} = 1.2V, 1.5 Gbps data rate, 0% Pre-emphasis

Figure 13. Typical Performance Characteristics

Design-For-Test (DfT) Features

IEEE 1149.1 SUPPORT

The SCAN90CP02 supports a fully compliant IEEE 1149.1 interface. The Test Access Port (TAP) provides access to boundary scan cells at each LVTTL I/O on the device for interconnect testing. Differential pins are included in the same boundary scan chain but instead contain IEEE1149.6 cells. IEEE1149.6 is the improved IEEE standard for testing high-speed differential signals.

Refer to the BSDL file located on National's website for the details of the SCAN90CP02 IEEE 1149.1 implementation.



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IEEE 1149.6 SUPPORT

AC-coupled differential interconnections on very high speed (1+ Gbps) data paths are not testable using traditional IEEE 1149.1 techniques. The IEEE 1149.1 structures and methods are intended to test static (DC-coupled), single ended networks. IEEE1149.6 is specifically designed for testing high-speed differential, including AC coupled networks.

The SCAN90CP02 is intended for high-speed signaling up to 1.5 Gbps and includes IEEE1149.6 on all differential inputs and outputs.

FAULT INSERTION

Fault Insertion is a technique used to assist in the verification and debug of diagnostic software. During system testing faults are "injected" to simulate hardware failure and thus help verify the monitoring software can detect and diagnose these faults. In the SCAN90004 an IEEE1149.1 "stuck-at" instruction can create a stuck-at condition, either high or low, on any pin or combination of pins.

A more detailed description of the stuck-at feature can be found in NSC Applications note AN-1313.



PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Samples
	(1)		Drawing			(2)		(3)	(Requires Login)
SCAN90CP02SP/NOPB	ACTIVE	UQFN	NJD	28	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	
SCAN90CP02SPX	ACTIVE	UQFN	NJD	28	4500	TBD	Call TI	Call TI	
SCAN90CP02VY/NOPB	ACTIVE	LQFP	NEY	32	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	
SCAN90CP02VYX/NOPB	ACTIVE	LQFP	NEY	32	1000	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SCAN90CP02SP/NOPB	UQFN	NJD	28	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
SCAN90CP02VYX/NOPB	LQFP	NEY	32	1000	330.0	16.4	9.3	9.3	2.2	12.0	16.0	Q2

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PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SCAN90CP02SP/NOPB	UQFN	NJD	28	1000	203.0	190.0	41.0
SCAN90CP02VYX/NOPB	LQFP	NEY	32	1000	358.0	343.0	63.0

NEY0032A





MECHANICAL DATA

NJD0028A





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