National Semiconductor

SCAN25100
2457.6, 1228.8, and 614.4 Mbps CPRI SerDes with Auto RE Sync and Precision Delay Calibration Measurement

General Description

The SCAN25100 is a 2457.6, 1228.8, and 614.4 Mbps serializer/deseralizer (SerDes) for high-speed bidirectional serial data transmission over FR-4 printed circuit board backplanes, balanced cables, and optical fiber. The SCAN25100 integrates precision delay calibration measure-ment (DCM) circuitry that measures link delay components to better than ± 800 ps accuracy.

The SCAN25100 features independent transmit and receive PLLs, on-chip oscillator, and intelligent clock management circuitry to automatically perform remote radio head synchro-nization and reduce the cost and complexity of external clock networks.

The SCAN25100 is programmable though an MDIO inter-face as well as through pins, featuring configurable transmit-ter de-emphasis, receiver equalization, speed rate selection, internal pattern generation/verification, and loop back modes. In addition to at-speed BIST, the SCAN25100 in-cludes IEEE 1149.1 and 1149.6 testability.

Features

- Exceeds LV and HV CPRI voltage and jitter requirements
- 2457.6, 1228.8, and 614.4 Mbps operation
- Integrated delay calibration measurement (DCM) directly measures T14 and Toffset delays to ≤ ± 800 ps

- DCM also measures chip and other delays to ≤ ± 1200 ps accuracy
- Deterministic chip latency
- Automatic receiver lock and RE synchronization without reference clock or external crystal
- Independent transmit and receive PLLs for seamless RE synchronization
- Low noise recovered clock output
- Requires no jitter cleaning in single-hop application
- >8 kV ESD on the CML IO, >7 kV on all other pins, >2 kV CDM
- Hot plug protection
- LOS, LOF, 8b/10b line code violation, comma, and receiver PLL lock reporting
- Programmable hyperframe length and start of hyperframe character
- Programmable transmit de-emphasis and receive equalization with on-chip termination
- Advanced testability features
  — IEEE 1149.1 and 1149.6
  — At-speed BIST pattern generator/verifier
  — Multiple loopback modes
- 1.8V or 3.3V compatible parallel bus interface
- 100-pin TQFP package with exposed dap
- Industrial −40 to +85˚ C temperature range
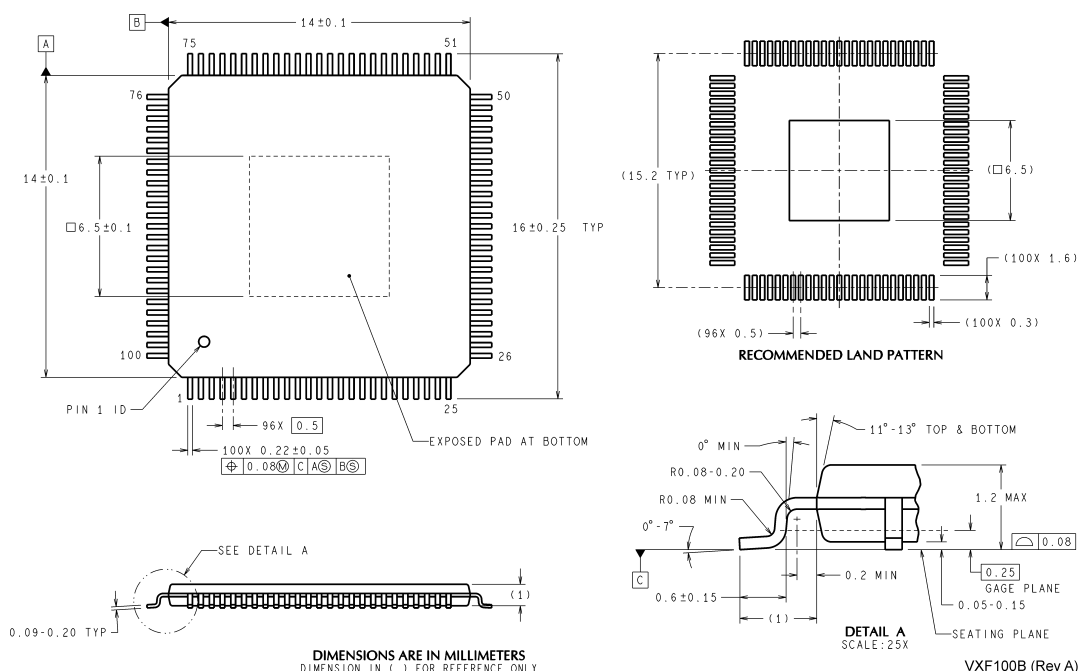
Block Diagram

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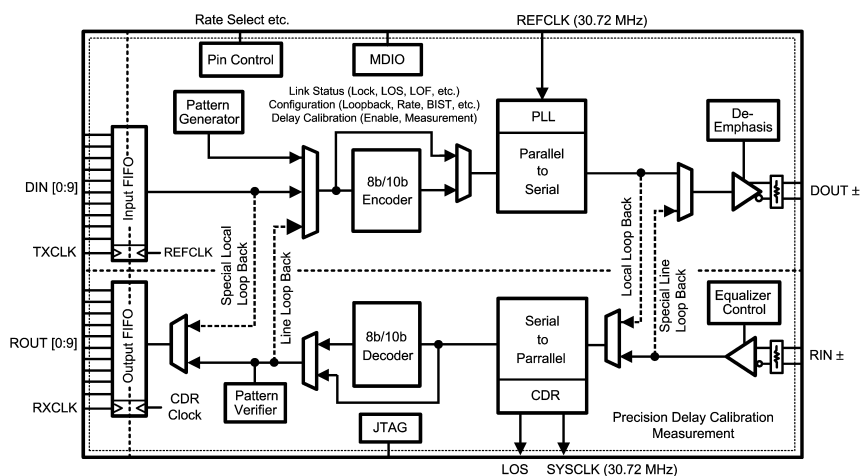
Pin Diagram
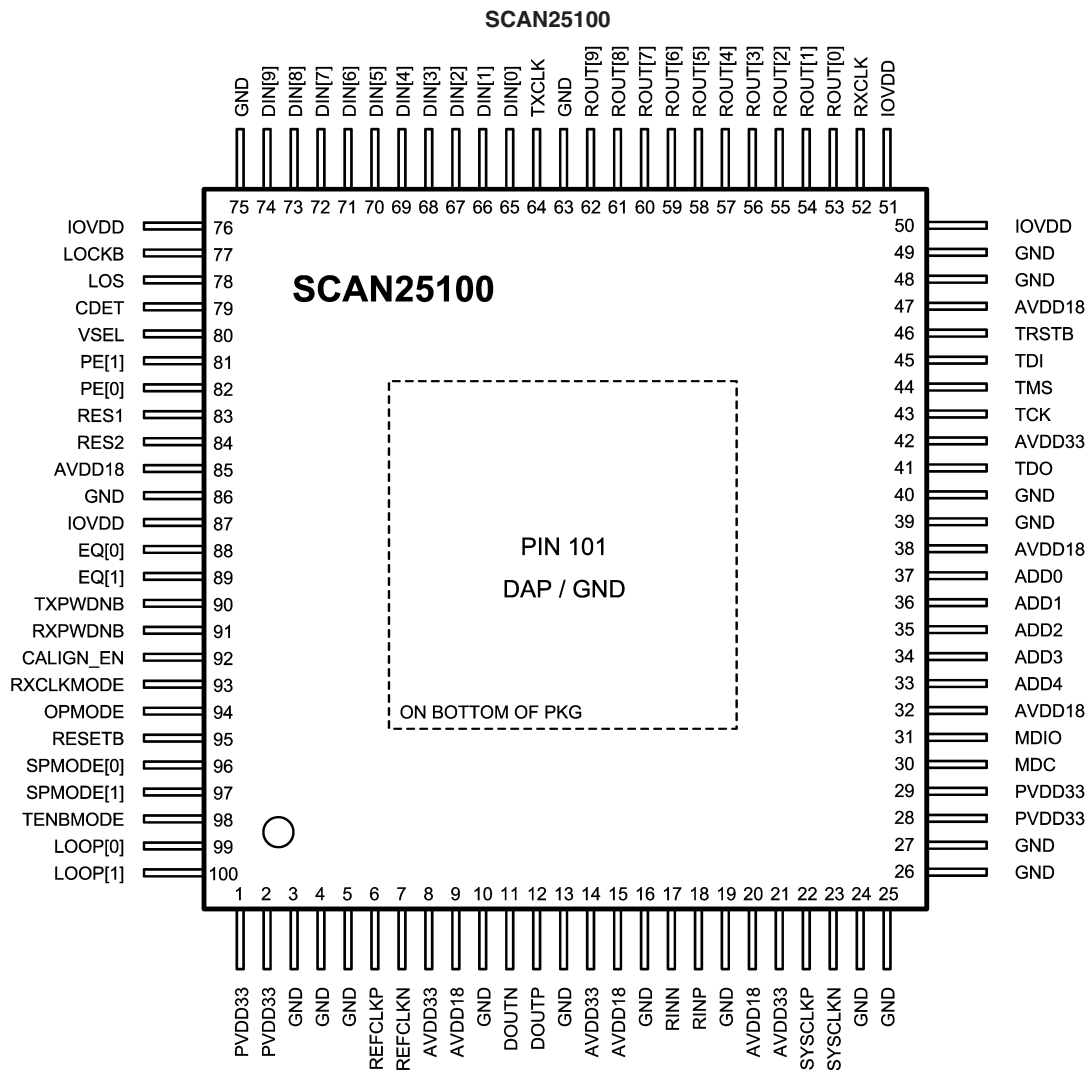
SCAN25100

(Top View)
100–Pin TQFP with Exposed Ground Pad
Order Number SCAN25100TYA
See NS Number VXF100B

20183402

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Physical Dimensions inches (millimeters) unless otherwise noted

14±0.1

75   51

76   50

14±0.1

□6.5±0.1

16±0.25 TYP

100   26

PIN 1 ID   1   25

96X 0.5

100X 0.22±0.05

⊕ 0.08 Ⓜ C AⓈ BⓈ

EXPOSED PAD AT BOTTOM

RECOMMENDED LAND PATTERN

(15.2 TYP)

(□ 6.5)

(100X 1.6)

(96X 0.5)

(100X 0.3)

SEE DETAIL A

0.09-0.20 TYP

(1)

DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN ( ) FOR REFERENCE ONLY

11°-13° TOP & BOTTOM

0° MIN

R0.08-0.20

R0.08 MIN

0°-7°

0.6±0.15

0.2 MIN

(1)

1.2 MAX

☐ 0.08

0.25
GAGE PLANE
0.05-0.15

SEATING PLANE

DETAIL A
SCALE:25X

VXF100B (Rev A)

100-Pin TQFP with Exposed Ground Pad (Top View)
Order Number SCAN25100TYA
NS Package Number VXF100B
See www.national.com/quality/marking_conventions.html for additional part marking information

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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