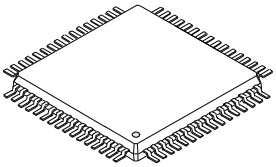
MP3 DECODER WITH ESP FUNCTION AND CD INTERFACE

DESCRIPTION

SC9822P is a sing-chip Mp3 decoder with electronic shockproof function. It can be used in CD player, DISC-MAN and such systems which need MP3 decoder. And this chip provides smaller package, lower power dissipation and higher cost performance ratio.



LQFP-64-10x10-0.5

FEATURES

* Provide ECC and EDC functions for CD-ROM data error correcting.
* ISO/IEC 11172-3 L3 L2 L1 decode
* ISO/IEC 13818-3 L3 L2 L1 decode
* Support all MP3 bit rates and free formats under SO/IEC 11172-3 L3 L2 L1 specifications.
* Support all MP3 bit rates and free formats under SO/IEC 13818-3 L3 L2 L1 specifications.
* Support 48K/44.1K/32K MP3 standard sampling rate, 24K/22.05K/16K and 12K/11.025/8K low sampling rate
* Support single/double/stereo/union stereo
* Provide 16: 4, 16: 5, 16: 6 and non-compression four compression modes
* Provide 3 pairs data, 2 pairs data and direct comparison connect three comparison connect modes.
* Serial host interface
* Support CD-DA straight through mode
* Support SDRAM/DRAM interface
* Only one external 16.9344MHz crystal oscillator
* Power management: normal mode, brownout mode and dormancy mode
* Various playing functions: skip forward/backward in track, skip forward/backward between tracks, pause, play and so on.
* Support the file systems in ISO9660, Joliet and UDF formats
* Support 1M/4M/8M/16Mx16 SDRAM, 1M/4M x16 DRAM

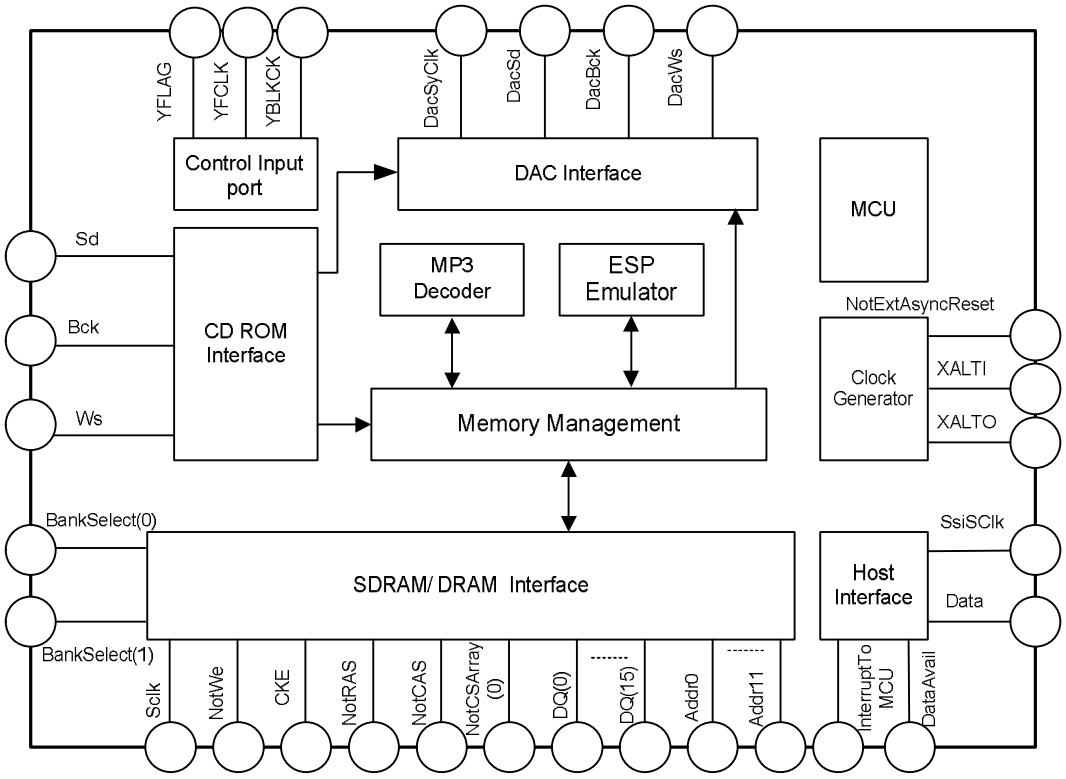
ORDERING INFORMATION

Device	Package
SC9822P	LQFP-64-10X10-0.5

APPLICATIONS

* Desk-top audio
* Portable CD/Mp3 player
* Car audio

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Rating	Unit
Kernel Voltage	V_{CCInt}	1.4 ~ 2.3	V
Port Voltage	V_{CCIO}	2.9 ~ 4.2	V
Input Voltage on pins	V_{IN}	-0.3 ~V_{CCIO} + 0.3	V
Ambient Temperature	T_{amb}	-20~90	°C
Storage Temperature	T_{stg}	-60~150	°C

ELECTRICAL CHARACTERISTICS (V_{CCINT}=1.8V, V_{CCIO}=3.3V, T_{amb}=25°C)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Kernel Operating Voltage	V_{CCInt}	Normal working	1.6	1.8	2.0	V
Port Operating Voltage	V_{CCIO}	Normal working	3.1	3.3	3.9	V
Quiescent Current	IDDInt	Kernel VDD1.8 supply current	--	5.3	--	μA
	I_{DDIO}	Port VDD3.3 supply current	--	0	--	μA
Operating Current	I_{CCInt}	Kernel VDD1.8 supply current	10.1	--	11.9	mA
	I_{CCIO}	Port VDD3.3 supply current	1.3	--	2.5	mA
Operating Frequency	MClk	--	--	16.9344	--	MHz

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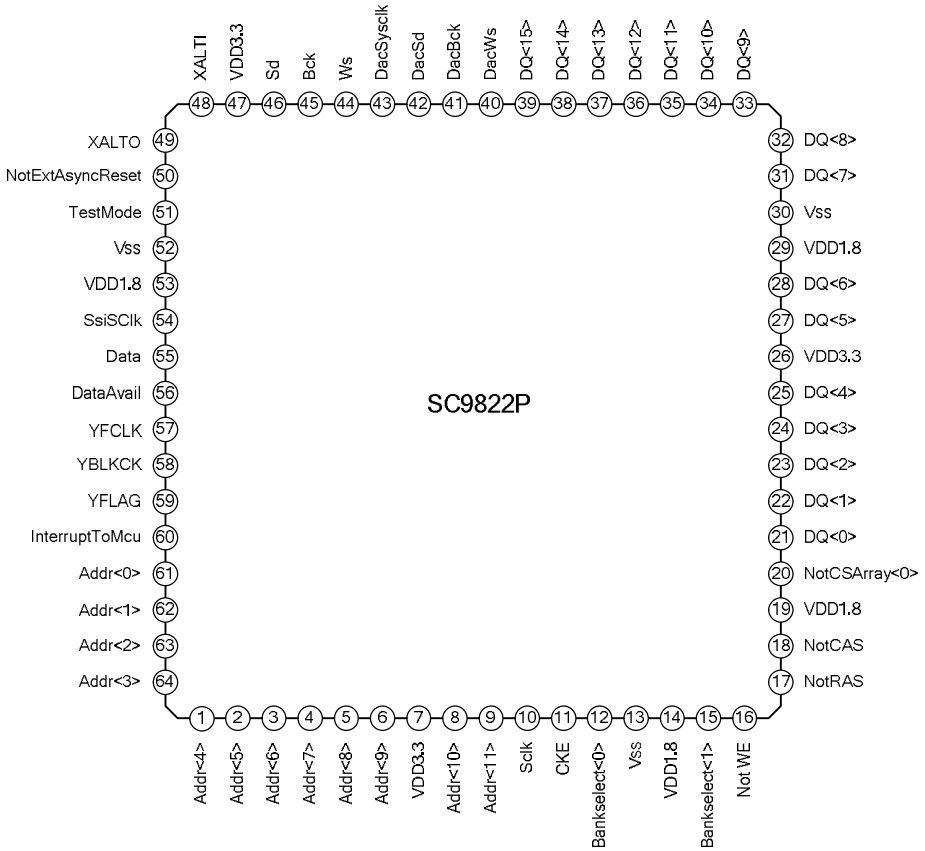
Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
High Level Input Voltage	V_{IH}	--		2.1	--	--	V
Low Level Input Voltage	V_{IL}	--		--	--	0.6	V
High Level Input Current	I_{IH}	Type a[note]	$V_{IN}=V_{DD}$	0	--	--	μA
Low Level Input Current	I_{IL}	Type a[note]	$V_{IN}=V_{SS}$	0	--	--	μA
High Level Output Voltage	V_{OH}	I_{OH}=1mA		--	3.29	--	V
		I_{OH}=2mA		--	3.28	--	
Low Level Output Voltage	V_{OL}	I_{OL}=1mA		--	0.02	--	V
		I_{OL}=2mA		--	0.04	--	
Tri-State Output leakage current	I_{OZ}	$V_{OUT}=V_{SS}$ or V_{DD}		0	--	--	μA
Output Short Circuit Current	I_{OS}	V_{DD}=3.3V, $V_O=V_{DD}$		--	47	--	mA
		V_{DD}=3.3V, $V_O=V_{SS}$		--	35	--	

Note: Type a: Common input port; Type b: Input port with pull-up resistor

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin name	I/O	Pin description
1	Addr<4>	O	SDRAM/DRAM address pin 4
2	Addr<5>	O	SDRAM/DRAM address pin 5
3	Addr<6>	O	SDRAM/DRAM address pin 6
4	Addr<7>	O	SDRAM/DRAM address pin 7
5	Addr<8>	O	SDRAM/DRAM address pin 8
6	Addr<9>	O	SDRAM/DRAM address pin 9
7	VDD3.3	I	Port supply voltage (3.3V)
8	Addr<10>	O	SDRAM/DRAM address pin 10
9	Addr<11>	O	SDRAM/DRAM address pin 11
10	SClk	O	16.9344M SDRAM/DRAM clock output pin
11	CKE	O	SDRAM/DRAM clock enable output pin
12	BankSelect<0>	O	SDRAM/DRAM block selecting output pin 0
13	VSS	I	Ground
14	VDD1.8	I	Kernel supply voltage (1.8V)
15	BankSelect<1>	O	SDRAM/DRAM block selecting output pin 1
16	NotWE	O	SDRAM/DRAM write output pin which is a low active.
17	NotRAS	O	SDRAM/DRAM row address strobe pin which is a low active.
18	NotCAS	O	SDRAM/DRAM column address strobe pin which is a low active.
19	VDD1.8	I	OTP download voltage.
20	NotCSArray<0>	O	SDRAM/DRAM chip selection output 0 which is a low active.
21	DQ<0>	I/O	SDRAM/DRAM data pin 0 with internal pull-up resistor.
22	DQ<1>	I/O	SDRAM/DRAM data pin 1 with internal pull-up resistor.
23	DQ<2>	I/O	SDRAM/DRAM data pin 2 with internal pull-up resistor.
24	DQ<3>	I/O	SDRAM/DRAM data pin 3 with internal pull-up resistor.
25	DQ<4>	I/O	SDRAM/DRAM data pin 4 with internal pull-up resistor.
26	VDD3.3	I	Port supply voltage (3.3V)
27	DQ<5>	I/O	SDRAM/DRAM data pin 5 with internal pull-up resistor.
28	DQ<6>	I/O	SDRAM/DRAM data pin 6 with internal pull-up resistor.
29	VDD1.8	I	Kernel supply voltage(1.8V)
30	VSS	I	Ground
31	DQ<7>	I/O	SDRAM/DRAM data pin 7 with internal pull-up resistor.
32	DQ<8>	I/O	SDRAM/DRAM data pin 8 with internal pull-up resistor.
33	DQ<9>	I/O	SDRAM/DRAM data pin 9 with internal pull-up resistor.
34	DQ<10>	I/O	SDRAM/DRAM data pin 10 with internal pull-up resistor.
35	DQ<11>	I/O	SDRAM/DRAM data pin 11 with internal pull-up resistor.
36	DQ<12>	I/O	SDRAM/DRAM data pin 12 with internal pull-up resistor.
37	DQ<13>	I/O	SDRAM/DRAM data pin 13 with internal pull-up resistor.
38	DQ<14>	I/O	SDRAM/DRAM data pin 14 with internal pull-up resistor.

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Pin No.	Pin name	I/O	Pin description
39	DQ<15>	I/O	SDRAM/DRAM data pin 15 with internal pull-up resistor.
40	DacWs	O	Word selection clock pin output to DAC.
41	DacBck	O	Bit clock pin output to DAC.
42	DacSd	O	Data pin output to DAC.
43	DacSysClk	O	System clock output to DAC.
44	Ws	I	Word selection clock input pin of CD-DSP.
45	Bck	I	Bit clock input pin of CD-DSP.
46	Sd	I	Data input pin of CD-DSP.
47	VDD3.3	I	Port supply voltage (3.3V).
48	XALTI	I	Oscillator input pin.
49	XALTO	O	Oscillator output pin.
50	NotExtAsyncReset	I	System reset pin which is a low active.
51	TestMode	I	Test mode pin which is a high active and connected to ground when it is not in test mode.
52	VSS	I	Ground
53	VDD1.8	I	Kernel supply voltage (1.8V)
54	SsiSClk	I	MCU clock input pin.
55	Data	I/O	MCU data pin.
56	DataAvail	I	MCU telecommunication control pin.
57	YFCLK	I	Sync signal of sub code frame.
58	YBLKCK	I	Sync signal of sub code block.
59	YFLAG	I	CD servo error flag.
60	InterruptToMcu	O	Interrupt pin which is a high active and output to MCU.
61	Addr<0>	O	SDRAM/DRAM address pin 0
62	Addr<1>	O	SDRAM/DRAM address pin 1
63	Addr<2>	O	SDRAM/DRAM address pin 2
64	Addr<3>	O	SDRAM/DRAM address pin 3

FUNCTION DESCRIPTION

1. CD/MP3 Register function

Register description (The register address of SC9822P is 8 bits)

Symbol	Address	Read/write	Initialization	Description
SC9822P play state registers				
TotalTimeMin[5:0]	0x61	R	0x00	Total time's minutes of current playing music:0-59
TotalTimeSec[5:0]	0x62	R	0x00	Total time's seconds of current playing music:0-59
CurrentTimeMin[5:0]	0x63	R	0x00	Already played time's minutes of current music:0-59
CurrentTimeSec[5:0]	0x64	R	0x00	Already played time's seconds of current music: 0-59
FrameInform[7:0]	0x65	R	0x03	bit[3:0]: Sampling rate of current playing music 0x0: 44.1KHz 0x1: 48KHz 0x2: 32KHz 0x4: 22.05KHz 0x5: 24KHz 0x6: 16Khz 0x0C: 11.025KHz 0x0D:12KHz 0x0E:8KHz Reserve the rest; When the music format is Layer III: Bit [7:4]: The bit rate of current playing music, together with sampling rate to decide current bit rate. This chip provides variable bit rate and free bit rate (*1). When the sampling rate is 44.1, 48, 32KHz, the other sampling rate is: 0x0: Free mode 0x1: 32kbps 8kbps 0x2: 40kbps 16kbps 0x3: 48kbps 24kbps 0x4: 56kbps 32 kbps 0x5: 64 kbps 40 kbps 0x6: 80 kbps 48 kbps

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Symbol	Address	Read/write	Initialization	Description
FrameInform[7:0]	0x65	R	0x03	0x7: 96 kbps 56 kbps 0x8: 112 kbps 64 kbps 0x9: 128 kbps 80 kbps 0x0A: 160 kbps 96 kbps 0x0B: 192 kbps 112 kbps 0x0C: 224 kbps 128 kbps 0x0D: 256 kbps 144 kbps 0x0E: 320 kbps 160 kbps 0x0F: Forbid When the music format is Layer I: 0x0: Free mode 0x1: 32kbps 0x2: 64kbps 0x3: 96kbps 0x4: 128kbps 0x5: 160 kbps 0x6: 192 kbps 0x7: 224 kbps 0x8: 256 kbps 0x9: 288 kbps 0x0A: 320 kbps 0x0B: 352 kbps 0x0C: 384 kbps 0x0D: 416 kbps 0x0E: 448 kbps 0x0F: Forbid When the music format is Layer II:(Nonsupport single channel mode) 0x0: Free mode 0x1: Nonsupport 0x2: Nonsupport 0x3: Nonsupport 0x4: 64kbps 0x5: Nonsupport 0x6: 96 kbps 0x7: 112 kbps 0x8: 128 kbps 0x9: 160 kbps 0x0A: 192 kbps 0x0B: 224 kbps 0x0C: 256 kbps 0x0D: 320 kbps 0x0E: 384 kbps 0x0F: Forbid

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Symbol	Address	Read/write	Initialization	Description
StereoMode[7:0]	0x66	R	0x00	SC9822PC02 operating mode: Bit0: HostMemoryOpEnable 0b0: Disable Host operate external Sdram 0b1: Enable Host operate external Sdram Bit1: Mute 0b0: the current play is in the normal mode 0b1: the current play is in the mute mode Bit2: Pause 0b0: the current play is in the normal mode 0b1: the current play is in the pause mode Bit3: Sleep 0b0: the current play is in the normal mode 0b1: the current play is in the sleep mode Bit4: MusicWillStart 0b0: no music playing 0b1: the music will output after 100ms delay. Bit5: Stereo mode 0x0: Single channel 0x1: Stereo Bit[7:6]: Mpeg music file 11: Layer I 10: Layer II 01: Layer III 00: reserved

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Symbol	Address	Read/write	Initialization	Description
CdrMode[7:0]	0x67	R	0x00	SC9822P state register: Bit[7:4]: 0b0000: Idle state 0b0001: PreDecode state 0b0010: NormalPlay state 0b0011: FastForward state 0b0100: FastBackward state Others: Reserved CD-ROM format: bit2: 0: Mode-1 1: Mode-2 bit1: Effective when bit2=1: 0: Form1 1: Form2
StatusReg[7:0]	0x60	R	0x00	SC9822P state register: Bit[3:0]: 0000: Invalid state, no response 0001: ConfigFinished 0010: FileSystemFinished 0011: PreDecodeFinished 0100: SongEnd 0101:Fast backward to the first song 0110: OperationErr, error occurs, need host to process. 0111: FatalErr, serious error, require the host jump to the next song 1000: GetMaxPhysicalMSF, already received the max. physics address of the CD. Others: Reserved Bit[5:4]: 0b00: Invalid state 0b01: RequestData, apply for download new data 0b10: IntoCapture Bit6: 0b1: DownloadFinished, finish one time download. Others Reserved

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Symbol	Address	Read/write	Initialization	Description
HOST and internal registers which control the communication				
OutReg2High[7:0]	0x68	R	0x00	The high 8 bits of general purpose register.
OutReg2Low[7:0]	0x6C	R	0x00	The low 8 bits of general purpose register.
OutRegHigh[7:0]	0x69	R	0x00	The high 8 bits of general purpose output register.
OutRegLow[7:0]	0x6A	R	0x00	The low 8 bits of general purpose output register.
InpRegHigh[7:0]	0x71	W	0x00	The high 8 bits of general purpose input register
InpRegLow[7:0]	0x72	W	0x00	The low 8 bits of general purpose input register
InpReg2High[7:0]	0x73	W	0x00	The high 8 bits of general purpose input register 2
InpReg2Low[7:0]	0x74	W	0x00	The low 8 bits of general purpose input register 2
HostMcuCmd[7:0]	0x70	W	0x00	HOST sends to internal control command register, HostMcuCmd[7:0]： 0x01: StartConfigure 0x02: SetUpCDFS 0x03: DecodeMp3 0x04: ContinueAfterPreDecode 0x05: Fast Forward 0x06: Fast Backward 0x07: Resume 0x08: Pause 0x09: Stop 0x0A: Soft Mute On 0x0B: Soft Mute Off 0x0C: CDDA Through 0x0D: ForwardSkipFrame (*2) 0x0E: StartCapture （CDITF） 0x0F－0x11:Reserved 0x12: Mem Read Write Request 0x13: Mem Read Write End 0x14: SystemSleep 0x15: SystemWakeUp 0x16: Reserved

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Symbol	Address	Read/write	Initialization	Description
HostMcuCmd[7:0]	0x70	W	0x00	0x17: TestMode 0x18: PcmStart 0x19: PcmStop 0x1b: SetUpCDFS2 0x1c: GetVersion 0x1d: SetMaxPhysicalMSF Others: Reserved
External interface control registers				
HramType[4:0]	0x75	W	0x00	External SRAM/DRAM type: bit4 = 1, SDRAM type bit[3:0]: 0000:1BANK*(4096*256 => 1M*16) 0001: 2BANK*(2048*256 => 512K) 0100: 2BANK*(4096*512 => 2M) 0101: 4BANK*(4096*256 => 1M) 0110: 2BANK*(4096*1024 => 4M) 0111: 4BANK*(4096*512 => 2M) 1000: 4BANK*(4096*1024 => 4M) Reserve the rest When bit4 = 0, Dram type bit[3:0]: 0110:4M * 16bit(4K*1K*16) (4k ref) 0101:4M * 16bit(8K*512*16) (8k ref) 0100:1M * 16bit(1k*1k*16) (1k ref) 0011:1M * 16bit(2k*512*16) (4k ref) 0010:1M * 16bit(4k*256*16) (4k ref) 0001:256k*16(512*512*16) Reserve the rest
BitStreamType[5:0]	0x76	W	0x00	bit[3:2] is the input interface of CD-DA, bit[1:0] is the output interface of DAC(*3) bit3: 1: Input is IIS interface 0: Output is EIAJ interface bit2: 0: Input word clock has 16 bitclk 1: Input word clock has 24 bitclk bit1: 1: Input is IIS interface 0: Output is EIAJ interface bit0: 0: Output word clock has 16 bitclk 1:Output word clock has 24 bitclk

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Symbol	Address	Read/write	Initialization	Description
CdRomType	0x77	W	0x00	Bit[0]: 1:CD-ROM XA format disk 0:Common CD-ROM format disk
Read external RAM registers				
MemAddrHigh[7:0]	0x7A	W	0x00	High 8 bits of start address when external RAM outburst method to read
MemAddrMid[7:0]	0x7B	W	0x00	Middle 8 bits of start address when external RAM outburst method to read
MemAddrLow[7:0]	0x7C	W	0x00	Low 8 bits of start address when external RAM outburst method to read
MemCmd[7:0]	0x7D	W	0x01	External RAM read-write command register Bit[7:0]: 0x00: External RAM read command 0x80: External RAM write command

Note: 1. when it is in free mode, do not displays the bit rate of current music in FrameInform register. At this time, the display time may be wrong.

2. ForwardSkipFrame is when occurs error, if CD-DSP can not ensure the position of M.S.F needed by SC9822P, Host denotes SC9822P to skip the number of Second and Frame. Hereinto, the number of second is stored in InpRegHigh(8'h71), and the number of Frame is stored in InpRegLow(8'h72).

3. The interface data of DAC and word clock are changing at the falling edge of the bit clock.

2. CD/MP3 Exchange with Host

The general purpose register provides parameter for main control command, and output register together with state register provide some parameters:

1) StartConfigure

InpRegHigh&InpRegLow is a 16 bits unsigned number, if the blank data CdItf input to the buffer is larger than this threshold, it will startup the next download operation; through configuring this value, the Mp3 shockproof time and CD pick up head jump frequency can remain balance; the value has an effective range related with SDRAM configuration; If the input value exceeds the enable range, the default value will replace the input value; Before send StartConfigure, the main controller will configure the HramType BitStreamType and CdRomType.

2) SetUpCDFS

InpRegHigh, InpRegLow, InpReg2High are file start MSF physics address respectively; InpReg2Low is the number of folders required (the maximum value is 0xFF). During file building, if operation occurs error, the Host can repeat sending SetUpCDFS command; when file system is finished, the OutReg1High&OutReg1Low indicate music file number; if the file number is 0, it means the file system cannot be finished.

3) DecodeMp3：

InpRegHigh&InpRegLow is 16 bits unsigned number, indicate the playing music file number; InpReg2High is an 8 bits unsigned number, indicate whether this music needs ID3 decode;

4) PreDecodeFinished：

OutReg1High&OutReg1Low, 16 bits unsigned number, is used to indicate the ID3 start page address in the process of PreDecode after ID3 decode; OutReg2High, 8 bits unsigned number, ID3 shift address; If these three registers are all 0xFF, this song will not contain ID3 information;

5) ContinueAfterPreDecode

After host detects the PreDecodeFinished, the system will send command for playing music; and the host has read the ID3 information before send command.

6) FastForward：

InpReg1High, is used to express the second of each fastforward unit; InpReg1Low, is used to express the fastforward ratio, the detail see the following table:

InpRegHigh	00h	10h	20h	30h
play time(s)	0.5	1	2	4

Not support others

InpRegLow	00h	01h	02h	≥03h
Skip scale	1:1	1:2	1:4	1:8

Skip scale is the ratio of play time and leap time.

7) FastBackward

InpReg1High, is used to express the second of each fastbackward unit; InpReg1Low，is used to express the fastforward ratio; Where the meanings of InpRegHigh is the same as fastforward; but the InpRegLow is different, it expresses n of the play time: skip time=1: n.

8) RequestData

OutReg1High, OutReg1Low, OutReg2High are the MSF of download address;

9) OperationErr

Except SetUpCDFS, if host detects the OperationErr at other state, it will send ForwardSkipFrame command; if the host received this command time after time during one song, it indicates this song has been serious damaged; it can jump to the next song.

10）SetUpCDFS2

Establish the tile document system; the meanings of the input and output parameter is the same as SetUpCDFS;

11）GetVersion

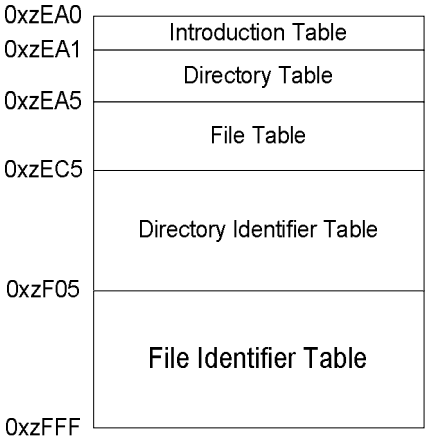
Return to the current version number, OutRegHigh is the main version number, and the OutRegLow is the vice version number.

12）SetMaxPhysicalMSF

The master indicates the SC9822P the maximum physical address of the CD by this command. The registers InpReg1High, InpReg1Low, and InpReg2High are corresponding to MSF value;

3. CDFS Tables

CDFS Table impropriate 351page（351*256*16bit）, the default address is the highest part of external RAM, 0xxEA0-0xxFFF(Page address), the following figure is the configuration in the RAM:



If RAM is 1M*16bit, z is 0; if RAM is 2M*16bit, z is 1; if RAM is 4M*16bit, z is 3; if RAM is 8M*16bit, z is 7; if RAM is 16M*16bit, z is F.

File configuration:

Address	Contents
Introduction Table (1 page)	
0xxEA000(16bit)	Total folder number in CD
0xxEA001(16bit)	Total mp3 file in CD
0xxEA002(16bit)	Total mp3 folder in CD
0xxEA003(16bit)	The folder no. of the first mp3 file
0xxEA004(16bit)	Including mp3 file number
Directory Table(4 pages）(each folder)	
8bit	The start folder no. of this directory
8bit	The folder number of this directory
16bit	The started mp3 file no. of this directory
16bit	Total Mp3 file number of this directory
8bit	Parent directory no.
8bit	Folder name length
File Table (32 pages) (each file)	
32bit	M.S.F information of Mp3 file
32bit	The size of Mp3 file
16bit	The length of Mp3 file name
16bit	Mp3 file type
32bit	Reserved
Directory Identifier Table (64 pages)	
128Byte	Folder name
File Identifier Table (250 pages)	
128Byte	Mp3 file name

Maximum file number is 1024, and the maximum folder number is 256 supported.

4. ESP Register description

Symbol	Address	R/W	Initialization	Description
Esp control register				
MSC80H [7:0]	0x50	W	0x00	Bit[0] : Control Esp operation mode 0-> straight in mode 1->electronic shockproof mode Bit[1] : 0-> Esp enable 1-> Esp disable Note: In the normal Esp operation, each time write to MSC80H, this bit should be set to 0. Bit[3:2]: Compare and connect command 00-> stop command 01-> execute command 10-> 2 pairs of commands 11-> 3 pairs of commands Note: During the compare and connect, if receive the new command, it will execute according the new command; and if receive the stop command, it will exit the compare and connect operation, and not output any result. Bit[4] : LocalReset command 0-> NOOP 1->reset the codec Bit[5] : Decode start command 0-> decode disable, 1-> decode enable. Bit[6]： LocalReset command 0-> NOOP 1->reset the codec Bit[7] : Encode start command 0-> stop encode 1-> start encode Note: When the compare& connect command and encode start command occur at the same time, the compare & connect command have the high PRI. If the encode command occurs in the compare & connect process, it will execute the compare and connect command.

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Symbol	Address	R/W	Initialization	Description
MSC83H [7:0]	0x51	W	0x00	Bit[3] : Mute control signal 0-> NOOP 1-> mute operation Bit[6:5] : Set compare & connect modes 00-> 16-bit precision 01-> 12-bit precision others-> 8-bit precision Bit[7] : WAQV signal, is the data valid signal send by MCU. 0-> NOOP 1-> data enable, execute the Valid operation
MSC85H [7:0]	0x52	W	0x00	Bit[3:0] : Encoder operation modes 1000-> non-compress mode, the audio data not compressed, and enter DRAM buffer directly 0100-> 6-bit compress mode 0010-> 5-bit compress mode 0001-> 4-bit compress mode others-> 6-bit compress mode, this is the default mode. Bit[5:4]: CD shock signal detect modes 00-> YFCKP falling edge, YFLAG＝0, judge it is shock 01-> YFCKP rising edge, YFLAG＝0, judge it is shock 10-> YFLAG＝0, judge it is shock 11-> YFLAG = 1, judge it is shock Bit[6]: SBSY sync modes 0-> SBSY falling edge sync, execute the Latch operation 1-> SBSY rising edge sync, execute the Latch operation Note: The default mode is 0.
Esp status register				
MSC90H [7:0]	0x53	W	0x00	Bit[1]: Decoder stop because the internal reason. 0-> decoder normal operation, (Encoder local reset, register execute the read/write operation, external reset). 1-> decoder stop because the internal reason, (detect the remain valid data is 0).

(To be continued)

(Continued)

Symbol	Address	R/W	Initialization	Description
MSC90H [7:0]	0x53	W	0x00	Bit[2] : Encoder stop because the internal reason. 0->encoder normal operation (compare & connect complete, encoder local reset, external reset). 1->Encoder stop because the internal reason (FLAG6, BOVF, MSOVF are set). Bit[3]:Compare and connect operation symbol : 0->not connect the coding (compare & connect complete, compare & connect stop, external reset), 1->execute the coding connect operation (compare & connect command). Note: During the compare & connect, send the encoder start command, it is equal to send compare & connect command directly. So there can clear the compare & connect symbol. Bit[5] :Input buffer overflow symbol. 0-> input buffer normal, (this register read operation, codec local reset, external reset) 1->input buffer overflow, (input buffer overflow). Bit[6]: External DRAM write overflow symbol. 0-> external DRAM normal write, (this register read operation, codec local reset, external reset). 1-> external DRAM write overflow Bit[7]: Shock symbol. 0-> normal operation, no shock, (this register read operation, Esp operation mode from straight in switch to shockproof mode, external reset). 1-> CD shock, (detect the CD vibrate)
SC91H [7:0] Note: The flag of this register denotes the state signal; if the status is not satisfied, the corresponding bit will clear automatically.	0x54	R	0x00	Bit[2] : Restore status signal 0-> the current Restore operation not execute(have been completed) 1-> Restore is operating Note: In normal, Restore operating time is very short, so this signal should remain 0.

(To be continued)

(Continued)

Symbol	Address	R/W	Initialization	Description
SC91H [7:0] Note: The flag of this register denotes the state signal; if the status is not satisfied, the corresponding bit will clear automatically.	0x54	R	0x00	Bit[3] : LocalReset status signal 0-> none LocalReset operation 1-> LocalReset operating Note: In normal, LocalReset operating time is very short, so the status signal should remain 0. Bit[4]: Decoder operation status signal 0-> decoder stop 1-> decoder operate Bit[5]: Encoder operation status signal: 0-> encoder stop, 1-> encoder operate Bit[6]: Dram overflow symbol 0-> Dram in normal 1-> Dram overflow Bit[7]: Dram empty symbol 0-> Dram have valid data supply for decoder, 1-> Dram empty, no valid data supply for decoder.
MSC92H High[7:0]	0x55	R	0x00	Bit[7:0]: The remain valid data in DRAM take page as unit. The high 8 bit data, each page is 256×16bit.
MSC92HLow [7:0]	0x56	R	0x00	Bit[7:0]: The remain valid data in Dram take page as unit, there is the low 8 bits, each page is 256×16bits. Note: because the 16-bit pointer is divided two parts for read operation, in the reading, the pointer also operating, so we should notice the carry bit in reading operation of main control processing.
Esp configuration register				
BitPoolPageLimitHigh [7:0]	0x58	W	0x07	BitPoolPageLimitHigh and BitPoolPageLimitLow form the up limit of DRAM, and determined the DRAM space as ESP buffer; Note: the external DRAM space of BitPool address which can be accessed by BitPool is Page[0, BitPoolLimitHigh & BitPoolPageLimitLow]. In the current MCU design, each page is 256×16bit

(To be continued)

(Continued)

Symbol	Address	R/W	Initialization	Description
BitPoolPageLimitLow [7:0]	0x59	W	0xff	
ShockMsk[7:0]	0x5B	W	0x00	Shock signal shield register. Its unit is 128*59ns=7.552us, if the signal length is less than input time, it is not consider the shock. The max. shock shield time is 255x7.552us = 1,925.880 us.
Register in the Mmu module				
MmuHostCmd[7:0]	0x00	RW	0x08	Bit[2:0]: Control the Sdram operation. 0—>no operation 1—>control Sdram carry out Precharge 2—>control Sdram carry out CBR 3—> control Sdram set modes 4—>enable Sdram controllable refresh 5—>disable Sdram controllable refresh, but enable Sdram auto refresh. When Sdram not used in a period, but there should remain the data, it can adopt this mode, then reduce the power dissipation. 6—>DRAM SELF-REFRESH MODE, only for “s” version dram. When enter this mode for more than 100us, DRAM will be in SELF-REFRESH state. you can change mode only by set MmuHostCmd BIT[2:0] to 7(that’s change to normal mode of dram) 7—> DRAM NORMAL MODE, before read or write operation of DRAM, you should enter NORMAL MODE for 200us for DRAM initialization (auto execute internal 8 cycles of refresh to initiate dram device) Bit[3] : Enable Sdram initialization 0—> enable Sdram initialization, and do it in the control of Bit[2:0] 1—> disable Sdram initialization, *—> for DRAM, this bit is not care Bit[7:4] : When use sdram, Bit[7:4] select Sdram type 0000：1BANK*(4096*256 => 1M*16) 0001：2BANK*(2048*256 => 512K)

(To be continued)

(Continued)

Symbol	Address	R/W	Initialization	Description
MmuHostCmd[7:0]	0x00	RW	0x08	0100：2BANK*(4096*512 => 2M) 0101：4BANK*(4096*256 => 1M) 0110：2BANK*(4096*1024 => 4M) 0111：4BANK*(4096*512 => 2M) 1000：4BANK*(4096*1024 => 4M) 1001：4BANK*(8192*512 => 4M) when use dram, Bit[7:4] select dram type: 0110：4M * 16bit(4K*1K*16) (4k ref) 0101：4M * 16bit(8K*512*16) (8k ref) 0100：1M * 16bit(1k*1k*16) (1k ref) 0011：1M * 16bit(2k*512*16) (4k ref) 0010：1M * 16bit(4k*256*16) (4k ref) 0001：256k*16(512*512*16) * Note: for dram, access timing of 50ns and 60ns dram are supported, 70ns haven't been tested.
CompareDataBaseAddressHigh [7:0]	0x02	RW	XX	Store the page base address Bit15 — Bit8 of compare & connect data.
CompareDataBaseAddressLow [7:0]	0x03	RW	XX	Store the page base address Bit7 — Bit0 of compare & connect data.
G722StatusBaseAddressHigh [7:0]	0x04	RW	XX	Store the page base address Bit15 — Bit8 of G722 status data.
G722StatusBaseAddressLow [7:0]	0x05	RW	XX	Store the page base address Bit7 — Bit0 of G722 status data.

5. ESP Program Guide

5.1 Enter Esp Mode

✧ First send short command 0x04, then enter Esp mode.

100: EspMode (Enter Esp mode command)

011: UnEspMode (Exit Esp mode command)

5.2 Configure external Sdram

✧ HOST need to initialize Sdram. Send the command 0x51 0x52 0x52 0x53 0x54 0x50 0x58 to register MmuHostCmd(8'h00) in turn.

✧ Host initialized Dram. Send the command 0x47 to register MmuHostCmd(8'h00)

✧ HOST need to configure the address of comparative data and decoding information. Send the command 0x0f to register CompareDataBaseAddressHigh (8'h02), send the command 0xf4 to register CompareDataBaseAddressLow (8'h03), send the command 0x0f to register G722StatusBaseAddressHigh (8'h04) and send the command 0xf8 to register G722StatusBaseAddressLow (8'h05).

✧ HOST need to configure the size of Sdram. Now it can only support page as unit, BitPoolPageLimitHigh(8'h58) BitPoolPageLimitLow(8'h59) .

5.3 Configure audio input and output interface

- ✧ HOST need to configure audio input interface. The input and output are 24 Bitclk of IIS interface. Send the command 0x0f to register BitStreamType (8'h76).

5.4 Configure compress mode, shake detecting mode, and shake signal shield time

- ✧ HOST need to configure the compress mode. There are 4 compress modes to be selected (16: 4 compress, 16:5 compress, 16:6 compress and non-compress), which will send the command to register MSC85H(8'h52).
- ✧ HOST need to configure the shake detecting mode. There are 4 modes to be detected(rising edge of sub block sync signal, shake signal low level determinant; falling edge of sub block sync signal, shake signal high level determinant; shake signal low level determinant; shake signal high level determinant), Send the command to register MSC85H(8'h52).
- ✧ HOST can configure shake signal shield time. Because Cd servo only receives some very short level jam signal, but not the signal we need, we can solve this problem by setting the shake signal shield time. Send the shielded time to register (8'h5b), the unit is 128*59ns=7.552us, the length of shake signal within the input value, it will not be considered as shake signal. The maximum shake shield time is 255x7.552us = 1,925.880 us.

5.5 Begin to encode and decode

- ✧ HOST sends encoding start command. Send 0xa1 to register MSC80H (8'h50).

5.6 Read Q sub code

- ✧ Read Q sub code of Cd every other time, and if the Q sub code is not continuous, do not enter Esp control flow, delay and read again. if the Q sub code is continuous, enter Esp main control flow.

5.7 Adopt query method to detect the state

- ✧ HOST will send query command every other time. Read register MSC90H (8'h53).

5.8 Send WAQV signal

- ✧ HOST sends affirm command of effective signal. When the state is normal, send the command 0x80 to register MSC83H (8'h51), and record the current effective address of Q sub code.

5.9 Send the compare& connect command

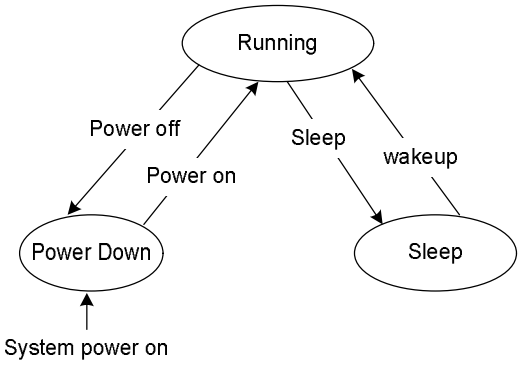
When read the three abnormal states of shake signal, input buffer overflow and Sdram data overflow, take CD back according to the effective address of Q sub code. Then begin to compare& connect to correct data.

- ✧ HOST configures the compare&connect command. There are 3 methods (16-bit, 12-bit, 8-bit precision). Send the command to register MSC83H(8'h51).
- ✧ HOST sends the compare & connect start command. There are two methods(3 pairs data comparative, direct compare & connect). Send the command to register MSC80H(8'h51).

6. Power Management Description

SC9822P has PowerDown, Running and Sleep three working mode:

PowerDown:	Close the system oscillator
Sleep:	The oscillator of chip is not closed, but the working main clock is closed, and refreshes the SDRAM/DRAM periodically.
Running:	Normal working mode



The command used for controlling the power supply is the short command format referred in SSI command interface: The specific command of Host is 2 bytes, whose format is: DevCmd[7:0]: HostCmd[7:0], thereinto, DevCmd[7:4]="0110" is specific byte, DevCmd[3:0] is still denoted receiving the Guest's address of this command. The specific command of HostCmd is: HostCmd[2:0]:

000:	PwrReset	(Software reset command. The chip is in the reset state once the command is sent out, and release the reset state until Host sends the releasing reset command)
111:	UnPwrReset	(software release reset command)
001:	PowerOn	(software power on command)
110:	PowerOff	(software power off command)
010:	Sleep	(enter Sleep state)
101:	WakeUp	(exit Sleep state)
101:	WakeUp	(exit Sleep state)

System power on:

- ✧ Host sends HostCmd: PwrReset(0x0)command, make the system in reset state;
- ✧ Host sends HostCmd: PowerOn(0x1)command, start the system oscillator (or make the external clock into SC9822P), and after a time (7－10 clock cycles), the main clock is into the system;
- ✧ Host is waiting for a time (wait until OSC clock is in the stable state, about 100ms), and then sends HostCmd: UnReset(0x7)command, make the system exit the reset state, and prepares to receive the Host's normal commands.

System power off:

- ✧ Host sends HostCmd: PwrReset(0x0)command, making the system in reset state;
- ✧ Host sends HostCmd: PowerOff(0x6)command;
- ✧ The system is in power off state.

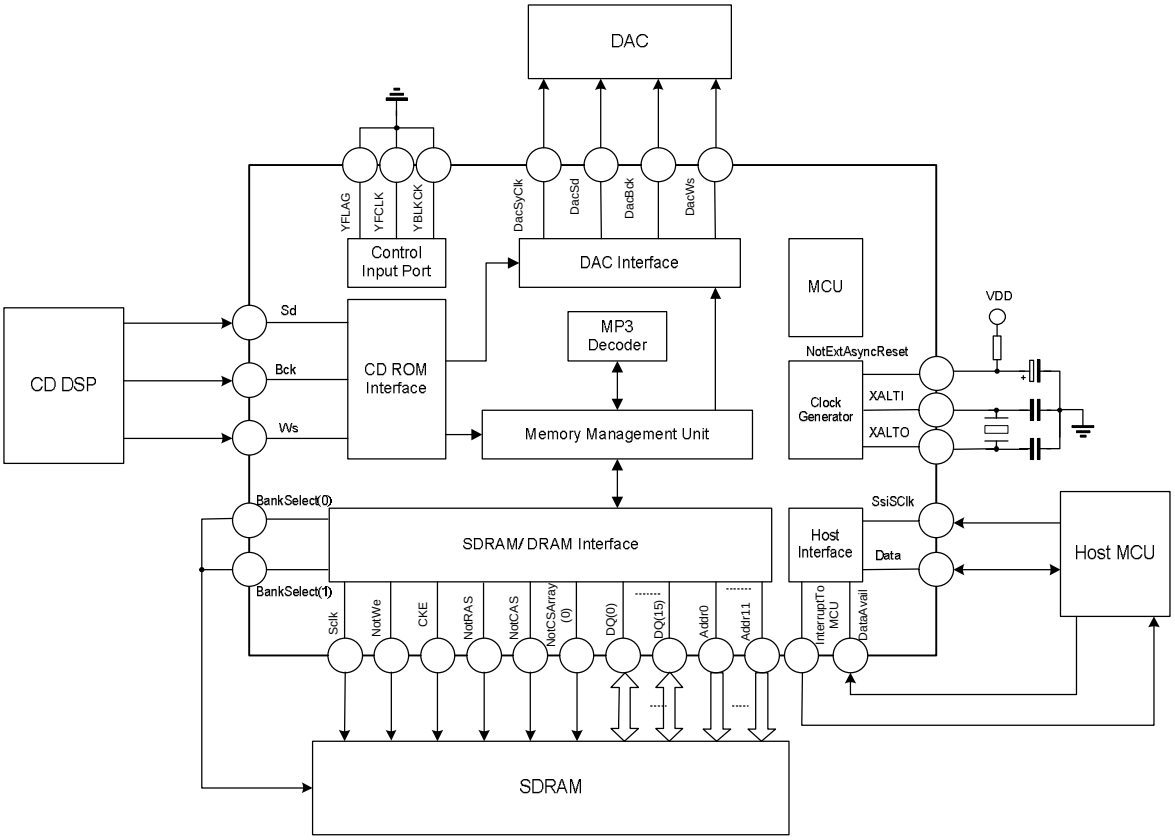
System standby (Sleep):

- ✧ Sleep command starts at the Pause stage;
- ✧ Host sends HostCmd: Sleep(0x2)command;
- ✧ Host sends system standby command (SystemSleep:0x31)to HostMcuCmd(8'h70);
- ✧ After a time, the system comes into standby state, but it will time-lapse refresh SDRAM/DRAM, and protect the data of SDRAM/DRAM from losing.

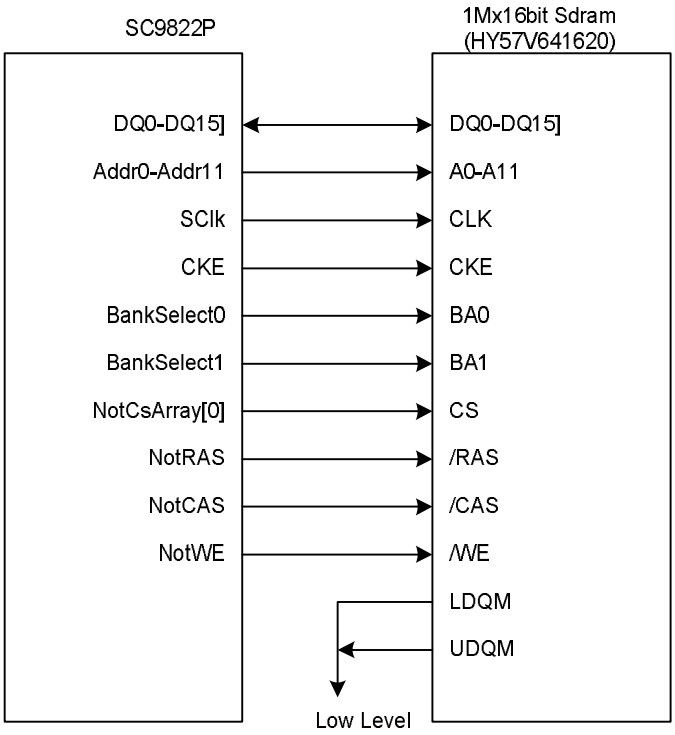
System recovery (WakeUp):

- ✧ Host sends HostCmd: WakeUp(0x5)command, exit the Sleep state;
- ✧ Host sends SystemWakeUp command (0x32) to HostHostCmd(8'b70)to start the system after waiting for about 5 ms;
- ✧ Host waits for 5 ms to return to normal working state.

TYPICAL APPLICATION CIRCUIT

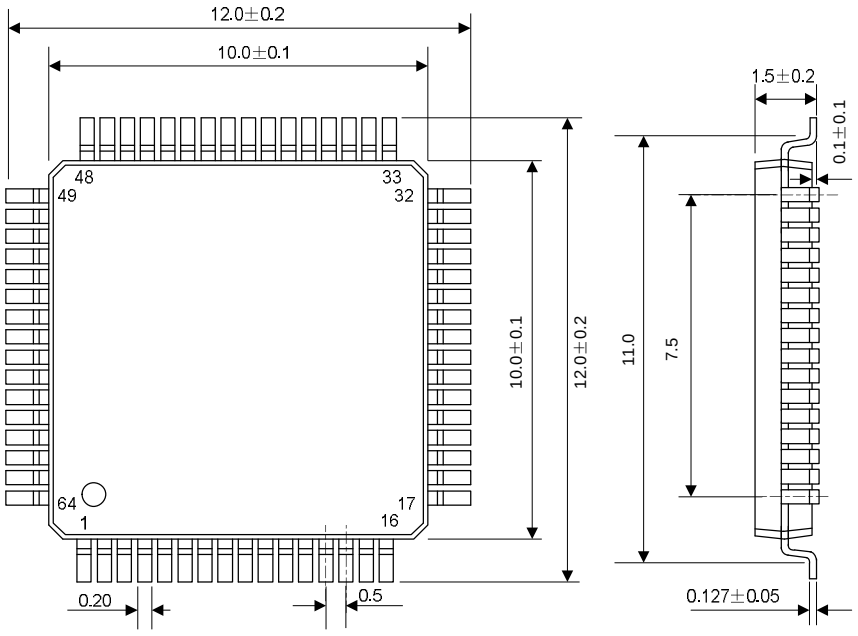


SC9822P EXTERNAL MEMORY DIAGRAM



PACKAGE OUTLINE

LQFP-64-10x10-0.5 Unit: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.

ATTACHMENT

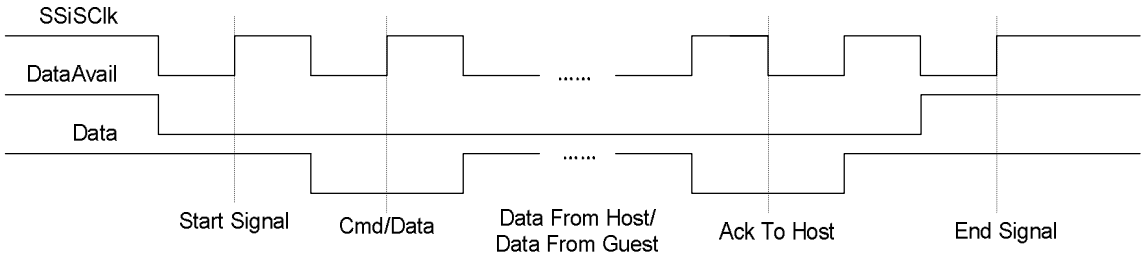
INTERFACE FUNCTION DESCRIPTION

1. Interface to main control MCU

SC9822P communicates with host computer's MCU in synchronism serial bus (SSI) data interface of our company.

1.1 Serial interface signal form

The serial interface communicating with MCU has 3 signal lines including control signal, data signal, and the sequence is as followed:



Thereinto, SsiSClk is the clock generating from Host port, and the frequency can rebound in a wide range (as long as the wave is not distortion), and is independent with Guest port; DataAvail used for marking effective data time quantum is also sent by host computer and it is a low active; Data is a bidirectional signal with pull-up resistor and used for specific data communication and feedback. As above picture, the data sent by the host port is all at the falling edge of SsiSClk and the feedback data or Ack signal of guest port are at the rising edge. We define one transmitting process as a frame, and the details of the coherent signal are as followed:

Start Signal: Start of frame

We define the first checking low level of DataAvail at the rising edge of SsiSClk at Guest port as the start of frame. When check the start signal, the guest can receive the data at the next rising edge.

Data Signal: Data signal

Data signal bit wide sent by host computer is one SsiSClk clock cycle.

Ack: Feedback signal

1. When Guest port receives the right addressing data, it feeds back to Host signal. And the width is a SsiSClk cycle. Used for data lead avoiding unmatched signal between two rising edges or corresponding to the data feedback to Host.
2. When Host sends to all Guest ports, signal before sending data is as lead signal, and between two falling edges of SsiSClk.

EndSignal: End of frame

When Guest detects the DataAvail at rising edge of SsiSClk, it means the transmission is end and waits for the next one.

1. 2 Serial communication protocol processing

Host and Guest realize the communication between each other by different explanation and processing for the data. The transmission process of one frame is as followed:

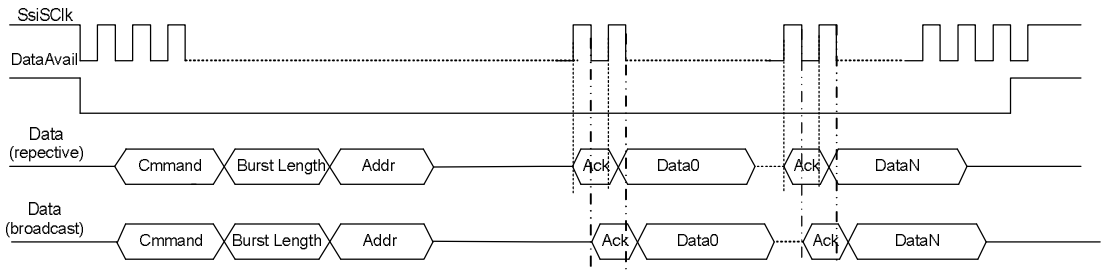


Figure 1 SSI frame signal

In the above transmission, Command pack explains the type of the frame; BurstLength suggests the data byte length (don't have this byte in non Burst mode); Addr is 8-bit address length. Data0~DataN is to define the length of BurstLength; the leading Ack is given to Guest by Host (Customers address check all mode common), and may be fed back by Guest. That is all decided by the information of Command pack.

Command: In the process of the whole protocol processing, the Command pack byte is critical.

8 bits of Command byte are as followed:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Read/Write	Burst	Reset	AddrExtend	Address[3]	Address[2]	Address[1]	Address[0]

Read/Write: Read-write flag bit; 1 denotes read data from Guest to Host, and 0 denotes the data flow is from Host to Guest.

Burst: Denote it is whether in Burst mode; 1 denotes this mode, and the byte behind Command byte is used as denoting the Burst length.

Reset: 1 denotes selected Guest reset, at this time, have no next byte; When Burst and Reset are 1 at the same time, denotes short command form. The form of short command is introduced in power management.

AddrExtend: 1 denotes this operation based on 16-bit address mode, and high 8-bit follows the low 8-bit; 0 is default 8-bit address operation mode.

Address[3:0]: Assign the operation object. Note: When Address[3:0] = 4'b1111, all the Guests will be operation objects (common), but at this time , the Guest should close the feedback channel and only receive the data sending by Host. And when selected the only Guest, it can be bidirectional communication (respective).

BurstLength: Denote the operation length of Burst.

Addr: 8-bit addressing address of Host.

Ack: It is an acknowledge signal. In the address check all modes; this signal is only used as leading data (low level) to denote the beginning of the data pack because the feedback channel of Guest is closed. In one-to-one mode, After the Guest receives a serial of pack leading with Command byte; it must feed back to Host an Ack signal in defined time which is decided by Host itself. When sending the data, if the transmission direction is from Host to Guest this time, Guest must feed back an Ack signal in defined time every time it receives a data; if overstep, Host will pull up DataAvail and end this transmission. When Host sends the data, if there is other data needed transmission after Host receives the Ack signal, it must transmit following the next cycle; When Host receives data, it must come into receiving state (otherwise end this transmission directly) after Host receives the Ack signal.

Data: The transmitted data is following the leading Ack signal, and the bytes of data are decided by BurstLength byte or Burst of Command. The former is used for Burst effective, and the latter limited a data when Burst is 0. When over the provision data, the receiver may not correspond to Ack signal.

According to above description, if complete the operations from Host to Guest, different transmission patterns are as followed:

Adopt non-Burst mode, 8-bit effective address, and assume the addressing address of guest is 0H:

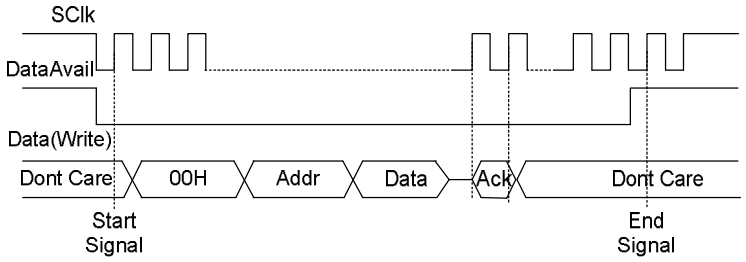


Figure 2 Write flow of non-Burst mode

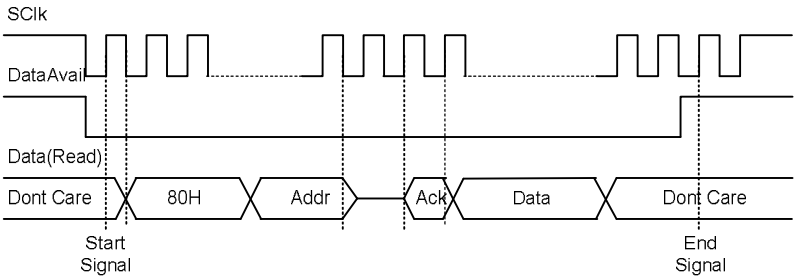


Figure 3 Read flow of non-Burst mode

Adopt Burst mode, and suppose Burst Length = N, Guest addressing is 00H:

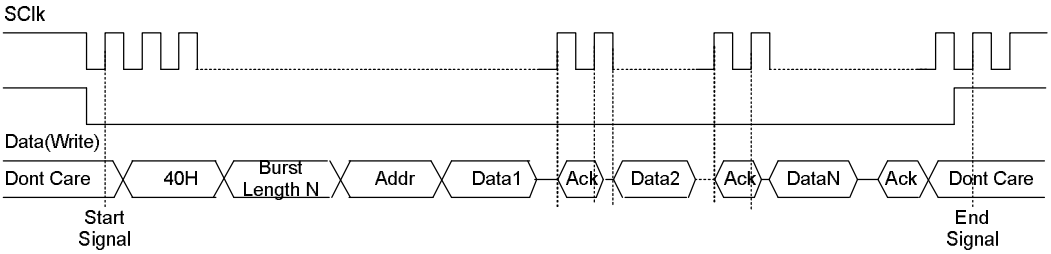


Figure4 Write flow of Burst mode

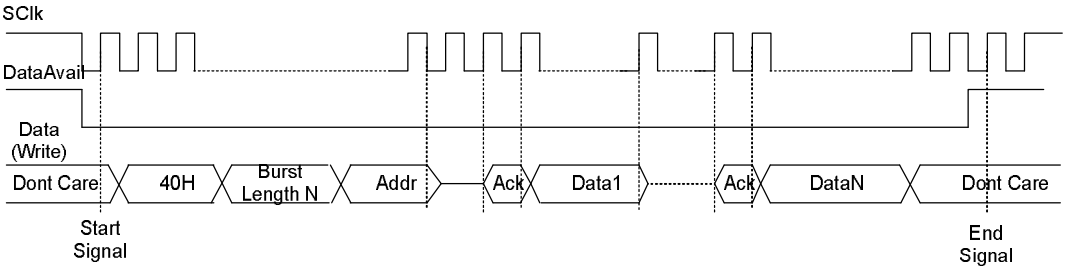


Figure 5 Read flow of Burst mode

1. 3 SC9822P register read-write protocol

A single register read command:

S	DevReadCmd	RegAddr	Waiting	Ack	DataFromClient	P

Thereinto, S is Start Signal, P is Stop Signal, DevReadCmd is read command (suppose Guest's address is 1, and DveReadCmd is: 0x81), RegAddr is the address of the register, Waiting is the waiting time of Host, StartAddr is the address of start register when read constinuously.

Constant register read command:

S	DevReadCmd	BurstLength	StartAddr	Waiting	Ack	Data 0	----------	Waiting	Ack	Data(n)	p

A single register write command:

S	DevWriteCmd	RegAddr	Data	Waiting	Ack	p

Constant register write command:

S	DevWriteCmd	BurstLength	StartAddr	Data 0	Waiting	Ack	----------	Data(n)	Waiting	Ack	p

1.4 Read-write Memory Protocol

Read operation

- ✧ HOST originates one data read operation of SDRAM/DRAM;
- ✧ HOST sends Mem read-write application (0x12) to HostMcuCmd(8'h70);
- ✧ HOST waits for Mem read-write enable interrupt;
- ✧ HOST writes the start address of SDRAM/DRAM to MemAddrHigh(8'h7A), MemAddrMid (8'h7B), MemAddrLow (8'h7C) after read-write enable interrupt; and the read command(0x00) write to MemCmd(8'h7D);
- ✧ HOST originates data read operation, and appoints the number of the operation, the range is 2-255 bytes, and the default value is 2. Then read the data of BL*8bit (BL is the appointed value of BurstLength: MemDataBL, and is expressed as n+1= MemDataBL in figure 7);
- ✧ If HOST still need read data, repeat the above operation;
- ✧ HOST completes read operation, send Mem read-write end command (0x13) to HostMcuCmd(8'h70).

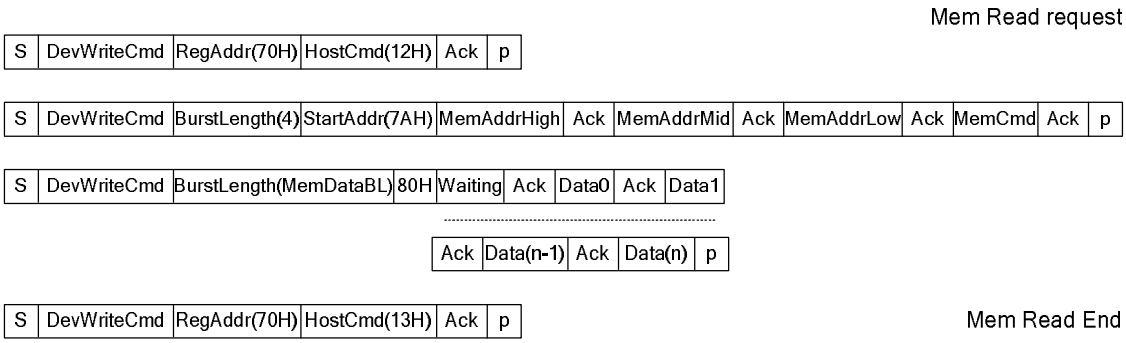


Figure6 Memory read operation

Write operation

- ✧ HOST originates one data write operation of SDRAM/DRAM;
- ✧ HOST sends Mem read-write application (0x12)to HostMcuCmd(8'h70);
- ✧ HOST waits for Mem read-write enable interrupt;

- ✧ HOST writes the start address of SDRAM/DRAM to MemAddrHigh(8'h7A), MemAddrMid (8'h7B), MemAddrLow (8'h7C) after read-write enable interrupt; and the read command(0x80)write to MemCmd(8'h7D);
- ✧ HOST originates data write operation, and appoints the number of the operation, the range is 2-255 bytes, and the default value is 2. Then read the data of BL*8bit (BL is the appointed value of BurstLength: MemDataBL, and is expressed as n+1= MemDataBL in the following figure);
- ✧ If HOST still need write data to external RAM, repeat the above operation; after HOST completes read operation, send Mem read-write end command (0x13) to HostMcuCmd(8'h70).

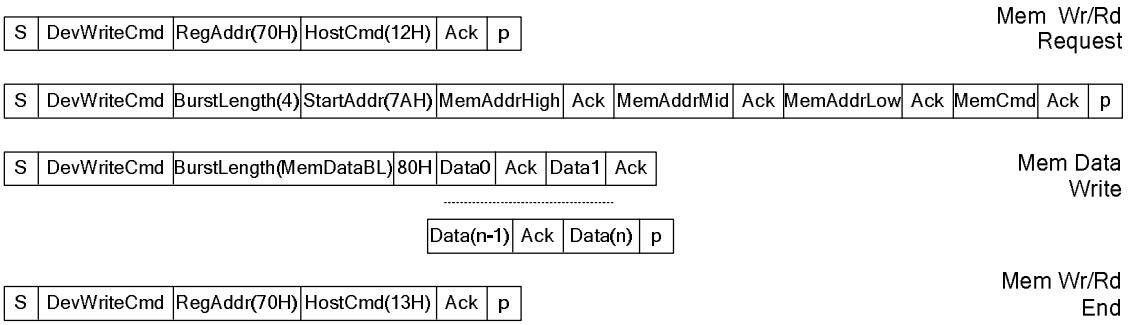
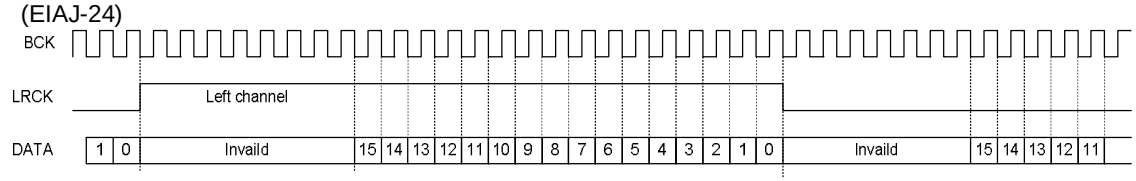


Figure7 Memory write operation

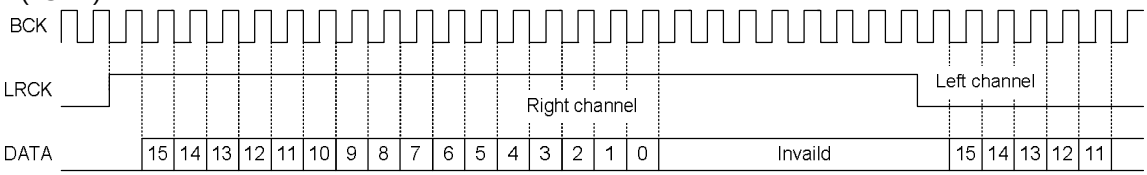
Note: 1. the memory read-write operation in figure 7and figure 8, it needs Waiting before every Ack signal;
2. every time read or write, it needs a specific register (8'h80) as the start address of Memory;
3. Only support 32 words (each word 16 bits) for Memory read-write addressing, that is to say every read-write begins with 32 times address value.

2. Interface with CD-DSP

1) 24-bit Bck, the MSB send first, and the data is right flush, the word selection signal of right channel is low (EIAJ-24)



2) 24-bit Bck, the MSB send first, and the data is left flush, the word selection signal of right channel is high (IIS-24)



3) 16-bit Bck, the MSB send first, the word selection signal of right channel is low (EIAJ-16)/ the word selection signal of right channel is high (IS-16)