CONTENT

1 GENERAL DESCRIPTION

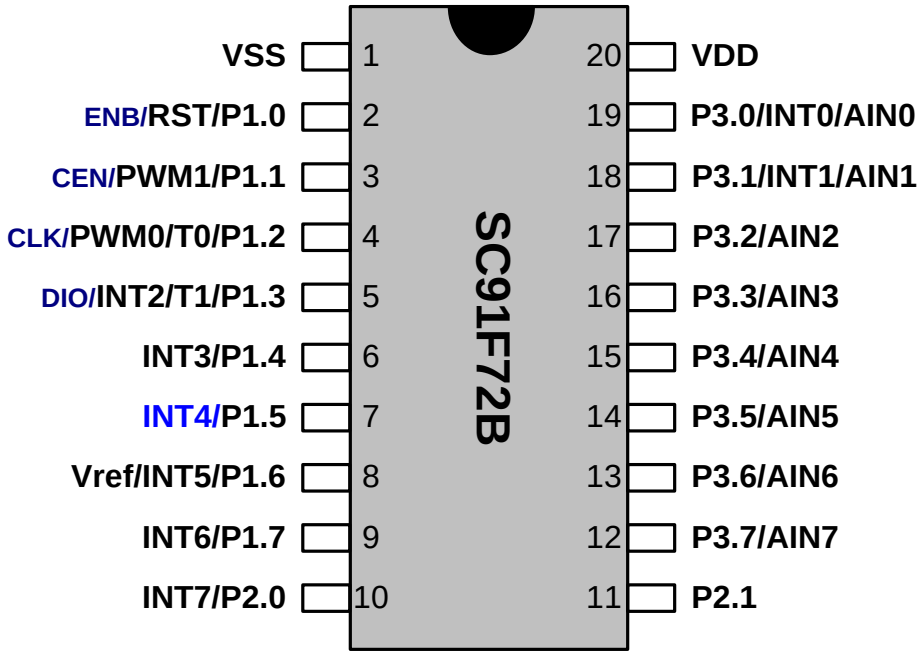
The SC91F72B is an enhanced ultra-fast industrial class 1T 8051 Flash microcontroller. The instruction set is fully compatible with standard 8051 products. The device is integrated with 4KB Flash ROM (256B used as EEPROM), 128B SRAM, up to 18 GP I/O, two16-bit timers/counters, 8-channel high-precision 10-bit ADC, 2-channel 8-bit PWM, internal precision 16M/8M Hz oscillator and other resources. To improve reliability and simplify user circuit, the SC91F72B also features with four optional LVR, precious tuned 2.4V ADC voltage reference, WDT and other high-reliability power supply circuit. The SC91F72B can be widely used in a variety of small domestic appliances, chargers andindustrial control applications.

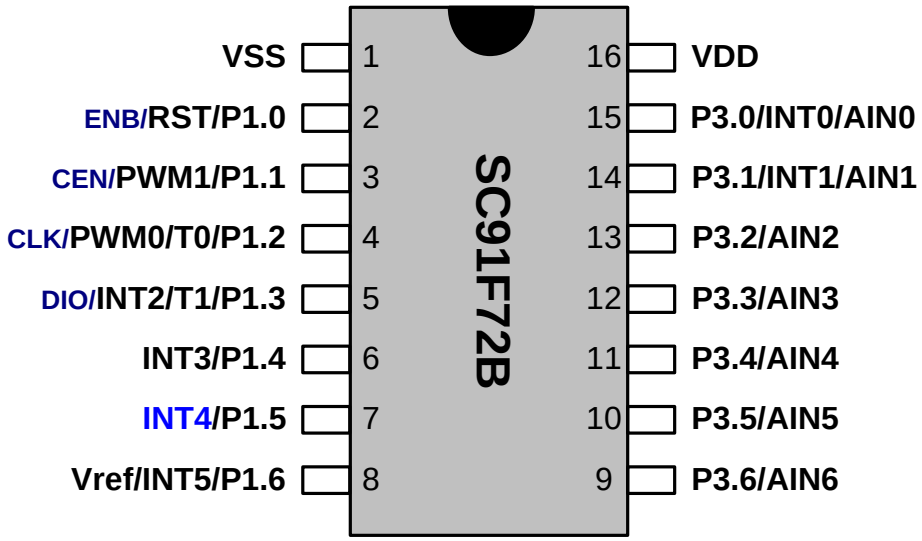
2 FEATURES

- Operating voltage: 3.6V~5.5V
- Operating temperature: -40 ~ 85℃
- Package: DIP20L 、SOP20L、SOP16L
- CPU core: Ultra fast 1T 8051
- Memory: 4KB Flash ROM（MOVC pprohibit addressing 0000H~00FFH）, 128B SRAM
- System Clock: Built-in 16M/8M Hz Oscillator
  - IC system clock can be set by the programmer to select
  - Frequency deviation: no more than ±2%＠(4.5V~5.5V) & (-40~85℃)
- Low voltage reset（LVR）:
  - Four Options：4.1V、3.9V、3.7V、3.5V
  - Default: configured by user on programmer
- Flash programming: 4 wire serial programming interface
- Interrupt（INT）:
  - 12 interrupt sources:TIMER0, TIMER1, INT0~7, ADC, PWM
  - INT0~3、INT5~7 have separate interrupt vector，Negative-edge trigger
  - INT4 can be set to Positive-edge trigger、Negative-edge trigger or Double-edge triggered
  - two-level interrupt priority
- Digital peripherals:
  - 18 GP I/O，4 Modes
  - 16 bit WDT with configurable clock divider ratio
  - 2 standard 80C51 16bit timers:TIMER0、TIMER1
  - 2-channel 8 bit PWM with variable frequency and duty cycle
- Analog peripherals:
  - 8 channel 10 bit ADC
    1) Built-in precious tuned 2.4V reference voltage
    2) Internal reference voltage：VDD、Vref(P1.6) and Internal 2.4V
    3) Support ADC interrupt
- Power saving mode:
  - STOP MODE
  - INT0~7 or RSTN can activate STOP MODE

3 PIN DEFINITION

3.1 PIN CONFIGURATION





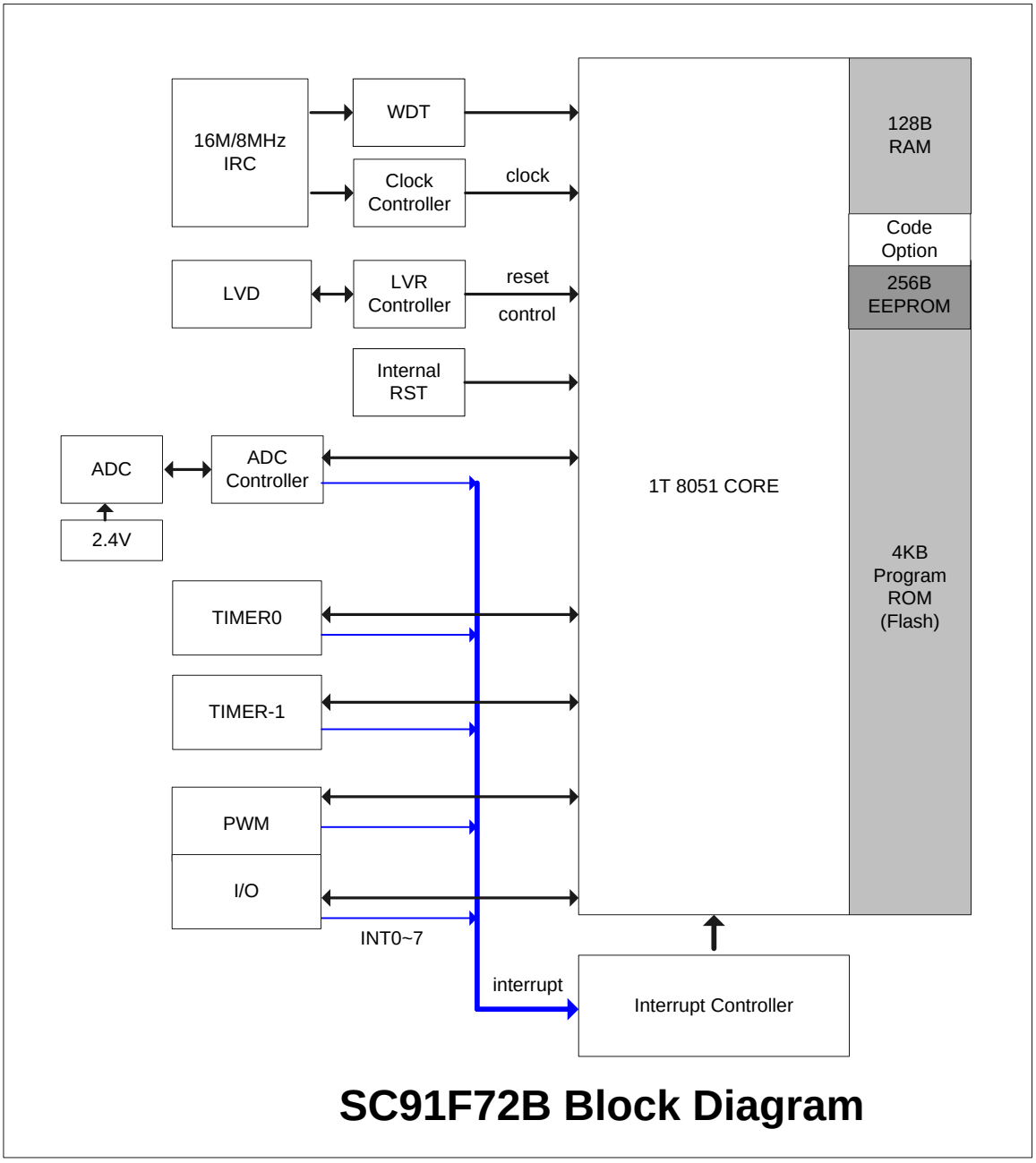
3.2 PIN DEFINITION

（20Pin）

Pin No	Pin Name	Pin Type	Function Description
1	**VSS**	Power	Ground
2	**RST/P1.0**	I/O	1) RST : RESET pin (Default), low enabled. User circuit can not be forced to Low while power on (when power-on is initializing, thedefault RST can be modified by setting SFRs (RSTCFG) and set the PIN as an IO. 2) P1.0 : GPIO P1.0 3) Flash programming pin ENB
3	**PWM1/P1.1**	I/O	1) P1.1 : GPIO P1.1 2) PWM1 : PWM1 output 3) Flash programming pin CEN
4	**PWM0/T0/P1.2**	I/O	1) P1.2 : GPIO P1.2 2) PWM0 : PWM0 output 3) T0 : external input of Timer0 4) Flash programming pin CLK
5	**INT2/T1/P1.3**	I/O	1) INT2 : external interrupt 2 2) P1.3 : GPIO P1.3 3) T1: external input of Timer1 4) Flash programming pin DIO
6	**INT3/P1.4**	I/O	1) INT3 : external interrupt3 2) P1.4 : GPIO P1.4
7	**INT4/P1.5**	I/O	1) INT4 : external interrupt4 INT4 can be set to positive edge, negative edge, double edge interrupt by SFRs (INT4IT). When detectingAC zero-crossing function, this pin is recommended.） 2) P1.5 : GPIO P1.5
8	**Vref/INT5/P1.6**	I/O	1) Vref : External voltage reference for ADC 2) INT5 : external interrupt 5 3) P1.6 : GPIO P1.6
9	**INT6/P1.7**	I/O	1) INT6 : external interrupt 6 2) P1.7 : GPIO P1.7
10	**INT7/P2.0**	I/O	1) INT7 :

			external interrupt7 2) P2.0 : GPIO P2.0
11	**P2.1**	I/O	P2.1 : GPIO P2.1
12	**P3.7/AIN7**	I/O	1) P3.7 : GPIO P3.7 2) AIN7 : ADC input channel 7
13	**P3.6/AIN6**	I/O	1) P3.6 : GPIO P3.6 2) AIN6 : ADC input channel 6
14	**P3.5/AIN5**	I/O	1) P3.5 : GPIO P3.5 2) AIN5 : ADC input channel 5
15	**P3.4/AIN4**	I/O	1) P3.4 : GPIO P3.4 2) AIN4 : ADC input channel 4
16	**P3.3/AIN3**	I/O	1) P3.3 : GPIO P3.3 2) AIN3 : ADC input channel 3
17	**P3.2/AIN2**	I/O	1) P3.2 : GPIO P3.2 2) AIN2 : ADC input channel 2
18	**P3.1/INT1/AIN1**	I/O	1) P3.1 : GPIO P3.1 2) INT1 : external interrupt1 3) AIN1 : ADC input channel 1
19	**P3.0/INT0/AIN0**	I/O	1) P3.0 : GPIO P3.0 2) INT0 : external interrupt0 3) AIN0 : ADC input channel 0
20	**VDD**	Power	3.6V – 5.5V

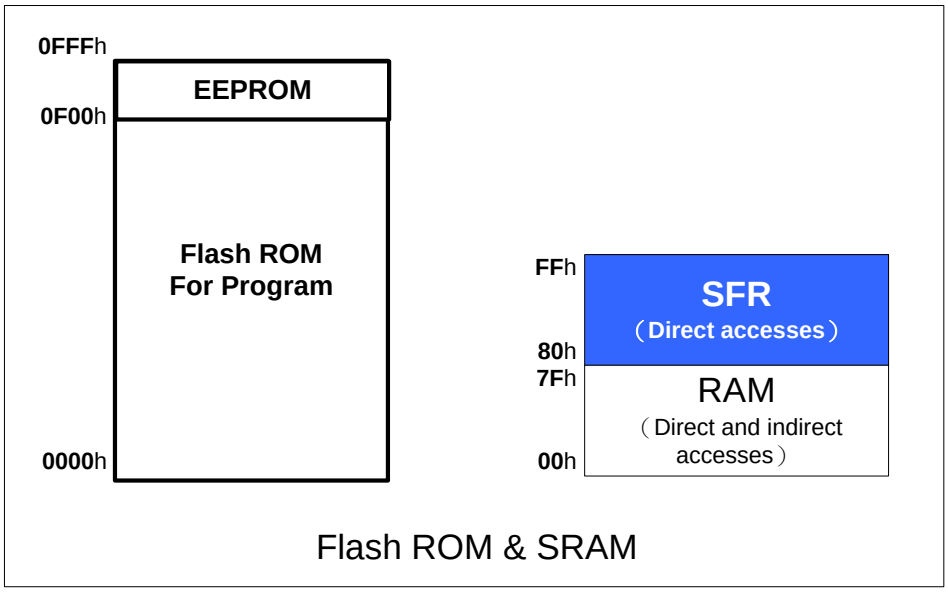
4 BLOCK DIAGRAM



SC91F72B Block Diagram

5 FLASH ROM & SRAM

The architecture of Flash ROM and SRAM is as follows:



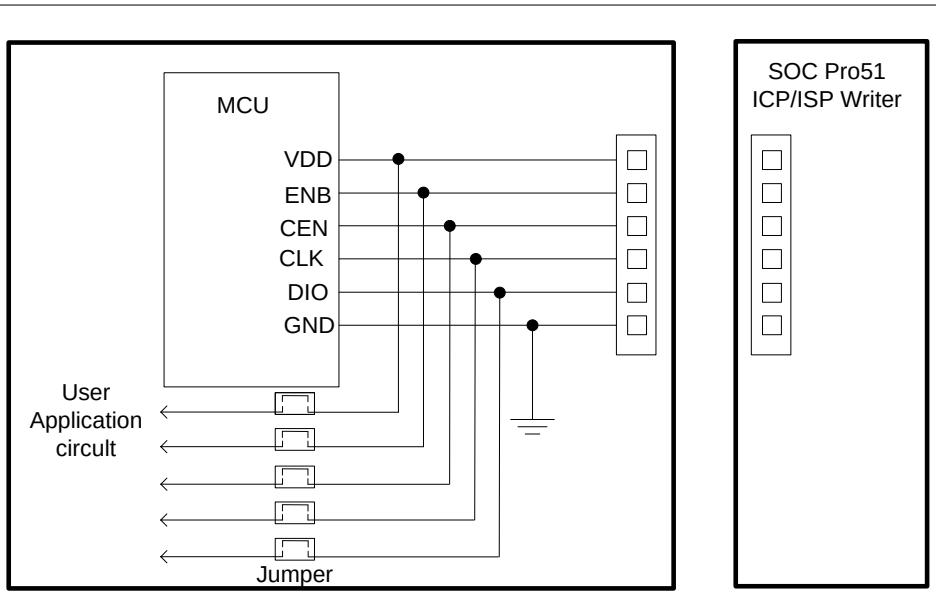
Flash ROM & SRAM

5.1 FLASH ROM

The SC91F72B has 4KB Flash ROM with address 0000H ~ 0FFFH. The 256 Bytes Flash of the address 0F00H ~ 0FFFH can be used as EEPROM (for in-application programming, see the IAP chapter for details). The Flash ROM has about 100,000 erase lifecycle with SinOneChip Programmer (SOC PRO51 and DPT51). Note the 256 Bytes Flash ROM with address 0000H ~ 00FFH can not be addressed by interval MOVC instruction.

The 4KB Flash ROM can be functioned for blank check (BLANK), programming (PROGRAM), verify (VERIFY) and erase (ERASE), but not for read （READ）.

The Flash ROM is programmed by the following pins: Pin2（ENB）、Pin3（CEN）、Pin4（CLK）、Pin5（DIO）、VDD、VSS. The connection diagram is as below:



Connection diagram of MCU with Programmer in ICP Mode

5.2 CODE OPTION FLASH AREA

The SC91F72B has an individual Flash area for user initial data storage.This area is called as Code Option area. which can be programmed by SOC Programmer.

IFB	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
IFB1	Vrefs[1:0]			ENWDT		DISLVR	LVRS[1:0]	
IFB2	8MHz							

IFB1	Symbol	Description
7,6	**Vrefs[1:0]**	ADC reference voltage selection 00：internal VDD 01：internal tuned 2.4V 10：external reference voltage P1.6 11：reversed
4	**ENWDT**	WDT enable 0：WDT disable 1：WDT enable（However, in the implementation of the IAP, the WDT will stop counting）
2	**DISLVR**	LVR enable 0：LVR enable 1：LVR disable
1,0	**LVRS [1:0]**	LVR voltage selection 00： 4.1V 01： 3.9V 10： 3.7V 11： 3.5V

IFB2	Symbol	Description
7	**8MHz**	System clock selection 0：16MHz 1：8MHz（Default）

5.3 SRAM

The SC91F72B provides 128bytes RAM (address 00H to 7FH) for random data storage. The 128B SRAM are directly and indirectly addressable.

Working registers:

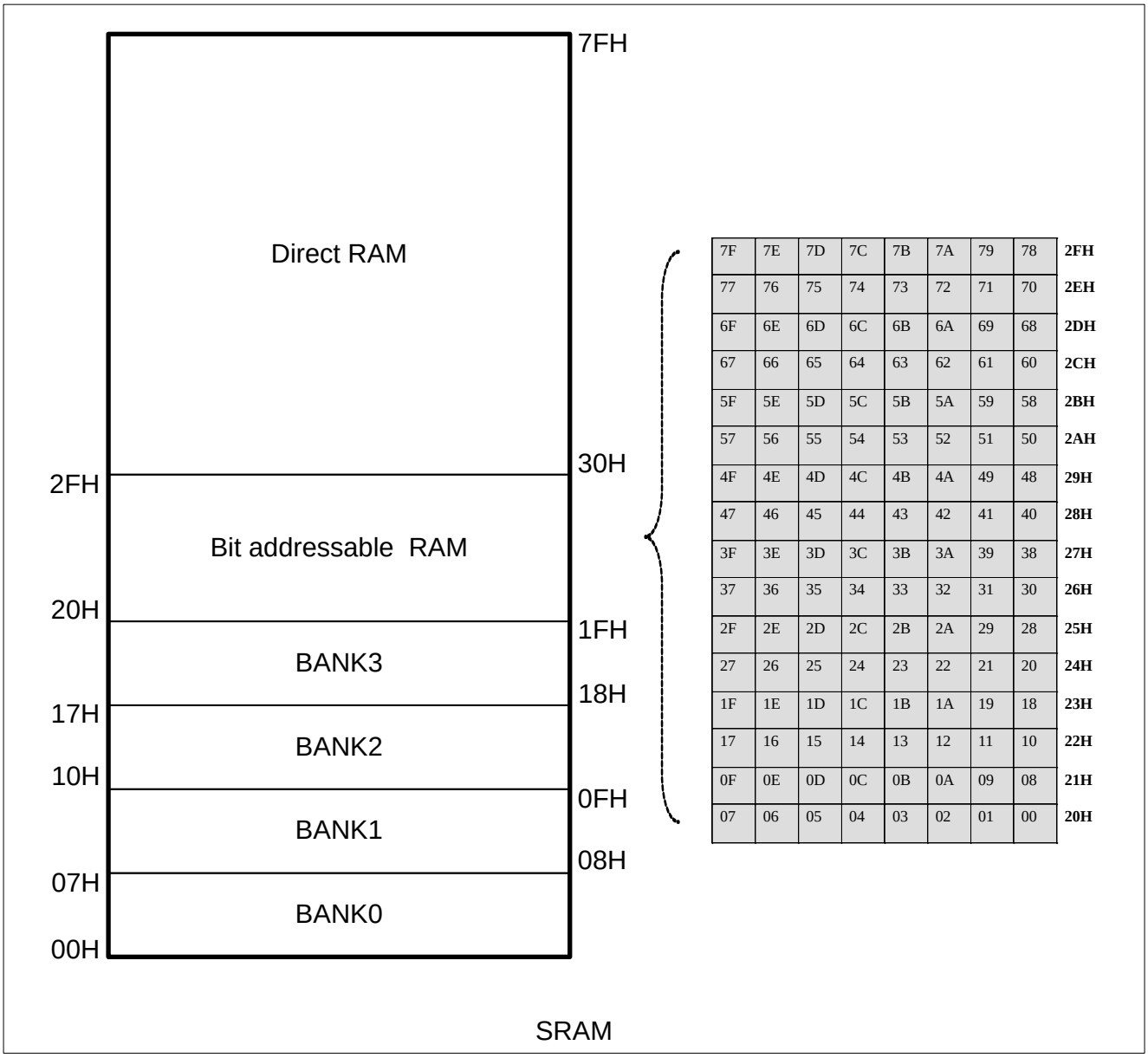
There are four sets of working registers, named as Banks 0, 1, 2, and 3.Each sets contain eight 8-bit registers. Individual register within these banks can be directly accessed by individual instruction. These workingregisters are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, the SC91F72B can only work with one particular bank at a time. The bank selection is done by setting RS1~RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

Bit addressable Locations:

The RAM area with address 20h to 2Fh is bit addressable, whichmeans one bit in this area can be individually addressed. In addition, some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of eh instruction itself. In the SFR area, any existing SFR with address ends in 0 or 8 is bit addressable.

User RAM area and Stack RAM:

The RAM address 30h to 7F can be used for stack. This area is selected by the Stack Pointer, which stores the address for the top ofstack. The Stack Pointer contains 07h at reset. User can change this to any value.



7F	7E	7D	7C	7B	7A	79	78	**2FH**
77	76	75	74	73	72	71	70	**2EH**
6F	6E	6D	6C	6B	6A	69	68	**2DH**
67	66	65	64	63	62	61	60	**2CH**
5F	5E	5D	5C	5B	5A	59	58	**2BH**
57	56	55	54	53	52	51	50	**2AH**
4F	4E	4D	4C	4B	4A	49	48	**29H**
47	46	45	44	43	42	41	40	**28H**
3F	3E	3D	3C	3B	3A	39	38	**27H**
37	36	35	34	33	32	31	30	**26H**
2F	2E	2D	2C	2B	2A	29	28	**25H**
27	26	25	24	23	22	21	20	**24H**
1F	1E	1D	1C	1B	1A	19	18	**23H**
17	16	15	14	13	12	11	10	**22H**
0F	0E	0D	0C	0B	0A	09	08	**21H**
07	06	05	04	03	02	01	00	**20H**

6 SPECIAL FUNCTION REGISTERS (SFR)

6.1 SFR TABLE

The SC91F72B uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs within the register address 80h~FFh are only accessable for by direct addressing. Some of the SFRs are bit addressable, which are those SFRs with addresses ended in 0 or 8..

The list of he SFRs is as follows.

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
F8h	PWMCR	PWMPRD	PWMDTY1	PWMDTY0	PWMCFG	-	-	Reserved
F0h	B	-	-	-	-	-	RSTCFG	Reserved
E8h	-	-	IAPKEY		IAPADL	IAPDAT	IAPCTL	Reserved
E0h	ACC	-	-	-	-	-	-	-
D8h	-	-	-	-	-	-	-	-
D0h	PSW	-	-	-	-	-	-	-
C8h	-	-	-	-	-	-	-	-
C0h	-	WDTCR	-	-	ADCCFG	ADCCR	ADCVH	ADCVL
B8h	IP	-	-	-	-	-	-	-
B0h	P3	P3CFG1	P3CFG0		EXIE	EXIP	P3ADC	-
A8h	IE	-	-	-	-	-	-	-
A0h	P2		P2CFG0	-	-	-	-	-
98h	-	-	-	-	-	-	-	-
90h	P1	P1CFG1	P1CFG0	INT4IT	-	-	-	-
88h	TCON	TMOD	TL0	TL1	TH0	TH1	TMCON	-
80h		SP	DPL	DPH	-	-	-	PCON
	Bit addressable	Not bit addressable						

6.2 SFR DESCRIPTION

symbol	address	description	7	6	5	4	3	2	1	0	reset value
SP	81h	Stack Pointer	SP[7:0]								00000111b
DPL	82h	DPTR Low	DPL[7:0]								00000000b
DPH	83h	DPTR High	DPH[7:0]								00000000b
PCON	87h	Power control	-	-	-	-	-	-	STOP	-	xxxxxx0xb
TCON	88h	Timer control	TF1	TR1	TF0	TR0	-	-	-	-	0000xxxxb
TMOD	89h	timer mode	GATE1	C/T1	M11	M01	GATE0	C/T0	M10	M00	00000000b
TL0	8Ah	Timer 0 low	TL0[7:0]								00000000b
TL1	8Bh	Time 1 low	TL1[7:0]								00000000b
TH0	8Ch	Timer 0 high	TH0[7:0]								00000000b
TH1	8Dh	Timer 1 high	TH1[7:0]								00000000b
TMCON	8Eh	Timer CLK Selection	-	-	-	-	-	-	T1FD	T0FD	xxxxxx00b
P1	90h	P1 data	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	11111111b
P1CFG1	91H	P1 configuration1	P17M[1:0]		P16M[1:0]		P15M[1:0]		P14M[1:0]		00000000b
P1CFG0	92H	P1 configuration0	P13M[1:0]		P12M[1:0]		P11M[1:0]		P10M[1:0]		00000000b
INT4IT	93H	INT4 interrupt edge type	-	-	-	-	-	-	INT4ES[1:0]		00000000b
P2	A0h	P2 data	-	-	-	-	-	-	P2.1	P2.0	xxxxxx11b

P2CFG0	A2H	P2 configuration0	-		-		P21M[1:0]		P20M[1:0]		xxxx0000b
IE	A8h	Interrupt enable	EA	EADC	EPWM	-	ET1	-	ET0	-	000x0x0xb
P3	B0h	P3 data	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	11111111b
P3CFG1	B1H	P3 conguration1	P37M[1:0]		P36M[1:0]		P35M[1:0]		P34M[1:0]		00000000b
P3CFG0	B2H	P2 conguration0	P33M[1:0]		P32M[1:0]		P31M[1:0]		P30M[1:0]		00000000b
EXIE	B4h	external INT enable	EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0	00000000b
EXIP	B5h	External INT priority	IPEX7	IPEX6	IPEX5	IPEX4	IPEX3	IPEX2	IPEX1	IPEX0	00000000b
P3ADC	B6h	P3/ADC control	RP37U	RP36U	RP35U	RP34U	RP33U	RP32U	RP31U	RP30U	00000000b
IP	B8h	Interrupt priority	-	IPADC	IPPWM	-	IPT1	-	IPT0	-	x00x0x0xb
WDTCR	C1h	WDT control	ENWDT	-	-	CLRWDT	-	-	WDTCKS[1:0]		nxx0xx00b
ADCCFG	C4h	ADC Vref selection	-	-	-	-	-	-	VREFS[1:0]		xxxxxxnnb
ADCCR	C5h	ADC control	ADCEN	ADCCKS[1:0]		EOC	ADCS	ADCIS[2:0]			00000000b
ADCVH	C6h	ADC converter result ADCV[9:2]	ADCV[9:2]								10000000b
ADCVL	C7h	ADC converter result ADCV[1:0]	-	-	-	-	-	-	ADCV[1:0]		xxxxxx00b
PSW	D0h	PSW	CY	AC	F0	RS1	RS0	OV	-	P	000000x0b
ACC	E0h	ACC									00000000b
IAPKEY	EAH	IAP protection	IAPKEY[7:0]								00000000b
IAPADL	ECH	IAP address low 8 bit，high bit is always high	IAPADR[7:0]								00000000b
IAPDAT	EDH	IAP data	IAPDAT[7:0]								00000000b
IAPCTL	EEH	IAP control	-	-	-	-	PAYTIMES[1:0]		CMD[1:0]		xxxx0000b
B	F0h	B									00000000b
RSTCFG	F6h	Reset configuration	-	-	-	-	DISRST	DISLVR	LVRS[1:0]		xxxx0nnnb
PWMCR	F8h	PWM control	ENPWM	PWMIF	-	-	DTY18	ENPWM1O	DTY08	ENPWM0O	00xx0000b
PWMPRD	F9h	PWM period	PWMPRD[7:0]								11111111b
PWMDTY1	FAh	PWM1 duty	PWMDTY1[7:0]								00000000b
PWMDTY0	FBh	PWM0 duty	PWMDTY0[7:0]								00000000b
PWMCFG	FCh	PWM configuration	-	-	INV1	INV0	-	CKS[2:0]			xx00x000b

8051 CPU Core SFR：ACC, B, PSW, SP, DPL, DPH

1. ACC（E0h）

ACC stands for Accumulator register. “A” is used as instruction Mnemonics.

2. B registers (F0h)

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

3. SP (81H)

The Stack Pointer Register is 8 bits wide, It is incremented before data is stored during PUSH, CALL executions and it is decremented after data is out of stack during POP, RET, RETI executions. The stack may reside anywhere in on-chip internal RAM (00H-FFH). On reset, the Stack Pointer is initialized to 07H causing the stack to begin at 08H.

4. PSW (D0h) Program status words

bit No	7	6	5	4	3	2	1	0
SYMBOL	CY	AC	F0	RS1	RS0	OV	-	P
Reset	0	0	0	0	0	0	x	0

Bit No	Symbol	Description
7	**CY**	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the operations.
6	**AC**	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	**F0**	User flag 0: The General purpose flag that can be set or cleared by the user.
4~3	**RS1、RS0**	Register bank select bits:

		RS1 RS0 Register Bank & Address 0 0 BANK 0 （00H~07H） 0 1 BANK 1 （08H~0FH） 1 0 BANK 2 （10H~17H） 1 1 BANK 3 （18H~1FH）
2	**OV**	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.
0	**P**	Parity flag: Set/cleared by hardware to indicate odd/even number of “1” in the ACC.
1	reserved	reserved

5. DPTR （82H、83H）

DPTR is the 16-bit data pointer of 8051.

7 POWER, RESET & CLOCK

7.1 POWER

SC91F72B has a built-inprecisely tuned 2.4V Voltage, which can also be used as ADC reference voltage.

7.2 POWER ON RESET

SC91F72B power-on reset process can be divided into the following stages:：

- Reset stage
- Loading information stage
- Normal operating stage

Reset stage

The device will always be in reset mode unlessthe supplied voltage is a higher than a certain value, And then CPU starts valid Clock. The Reset duration depends on the speed of the external power supply increasing. The reset process won’t complete until the external power supply reaches to a higher value than the optional value of the LVR voltage.

Loading information stage

During Reset, user settings will be loaded subject to the SFR, in order to work properly.

Normal operating stage

Finishing information loading,the device begins to read the instruction code from Flash and enter into the normal operation stage. LVR voltage value is the value written to the Code Option.

7.3 RESET MODE

SC91F72B have 5 reset modes:① External Reset②Low Voltage Reset③Power On Reset④Software Reset⑤WDT Reset.

7.3.1 EXERNAL RESET

The SC91F72B should be reset if user put the reset pulse into RST Pin from external.

RST/P1.0 used for RST Pin as default. User can modify RST to P1.0 by Writing the SFR RSTCFG.

7.3.2 LOW VOLTAGE RESET

SC91F72B features a LVR Reset Circuit. The LVR voltage has four options, the default value is written to MCU by programmer.

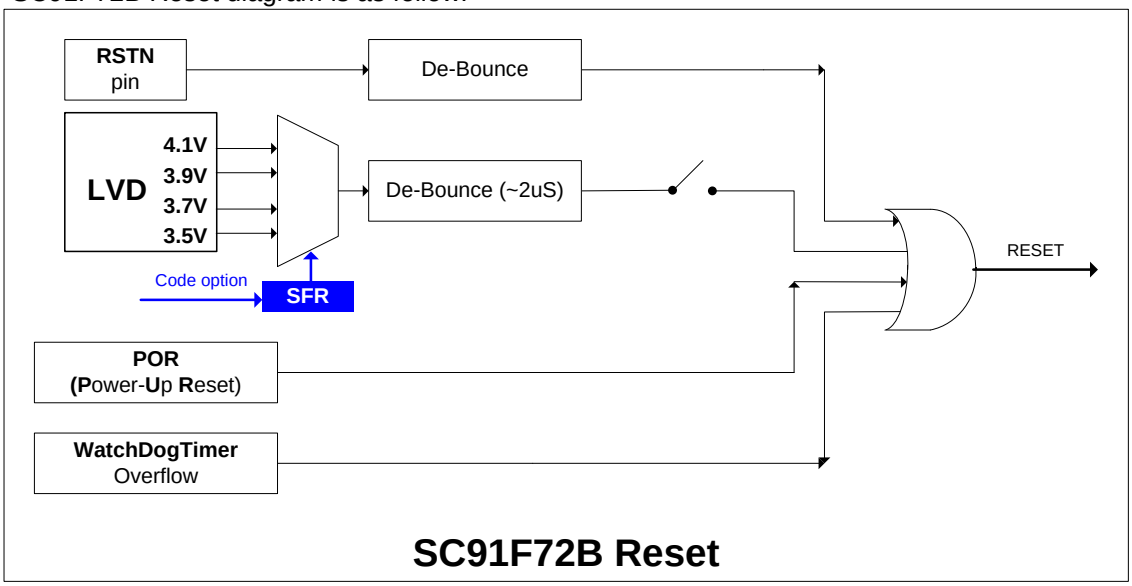
RSTCFG (F6h) Reset Configuration Register（R/W）

Bit No	7	6	5	4	3	2	1	0

SYMBOL	-	-	-	-	DISLVR	DISRST	LVRS[1:0]	
R/W	-	-	-	-	R/W	R/W	R/W	
Reset	x	x	x	x	n	n	n	n

Bit No	SYMBOL	Description
7~4	**reserved**	reserved
3	**DISLVR**	LVR enable 0：LVR ON 1：LVR Off
2	**DISRST**	IO/RST Control 0 ： P1.0 used as reset pin 1 ： P1.0 used as GPIO
1,0	**LVRS [1:0]**	LVR Voltage selection 00： 4.1V 01： 3.9V 10： 3.7V 11： 3.5V

SC91F72B Reset diagram is as follow:



SC91F72B Reset

7.3.3 POWER ON RESET

The device will automatically reset when the supply voltage exceeds the POR voltage.

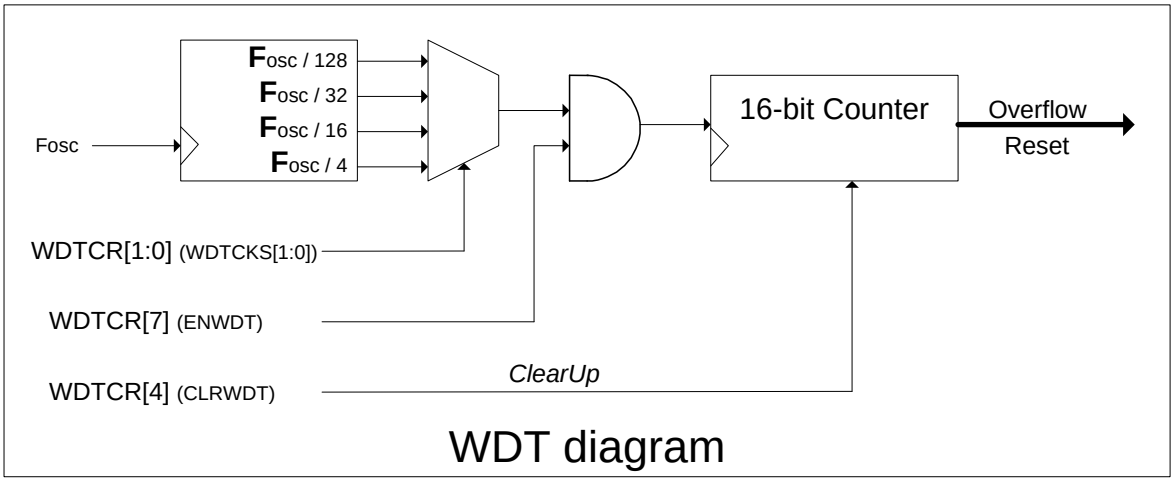
7.3.4 SOFTWARE RESET

A special reset way is also provided. When RST/P1.0 pin is defined as reset, the system will reset by Writing “0” to the P1.0.

7.3.5 WDT RESET

The SC91F72B has a 16-bit WDT.The clock source is the internal 16M/8M HZ RC Oscillator.

The diagram is shown below:



WDT diagram

WDTCR (C1h) WDT control（read/write）

Bit No	7	6	5	4	3	2	1	0
SYMBOL	ENWDT	-	-	CLRWDT	-	-	WDTCKS[1:0]	
R/W	R/W	-	-	R/W	-	-	R/W	
Reset	0	x	x	0	X	x	0	0

Bit No	SYMBOL	Description
7	ENWDT	WDT Control 1: WDT ON 0: WDT OFF
4	CLRWDT	Clear WDT(Write “1”) 1 ： WDT Timer Reset
1,0	**WDTCKS [1:0]**	WDT clock Source Selection

WDTCKS.1	WDTCKS.0	WDT Clock	WDT Overflow Time
0	0	Fosc/128	524.288ms@16MHz 1.048S@8MHz
0	1	Fosc/32	131.072ms@16MHz 262.144ms@8MHz
1	0	Fosc/16	65.536ms@16MHz 131.072ms@8MHz
1	1	Fosc/4	16.384ms@16MHz 32.768ms@8MHz

7.3.6 RESET STATUS

When the device is in reset state, most registers will return to their initial state. WDT is turned off, and port registers is set to FFh.The initial value of the program counter is 0000h, and initial value of the stack pointer SP is 07h.

The reset Value of SFR:

SFR name	reset value	SFR name	reset value
ACC	00000000b	TMCON	xxxxxx00b
B	00000000b	EXIE	00000000b
PSW	000000x0b	EXIP	00000000b
SP	00000111b	INT4IT	00000000b
DPL	00000000b	P3ADC	00000000b
DPH	00000000b	WDTCR	nxx0xx00b
PCON	xxxxxx0xb	ADCCFG	xxxxxx00b

IE	000x0x0xb	ADCCR	00000000b
IP	x00x0x0xb	ADCVH	10000000b
P1	11111111b	ADCVL	xxxxxx00b
P2	xxxxxx11b	IAPKEY	00000000b
P3	11111111b	IAPADL	00000000b
P1CFG0	00000000b	IAPDAT	00000000b
P1CFG1	00000000b	IAPCTL	xxxx0000b
P2CFG0	xxxx0000b	RSTCFG	xxxx0nnnb
P3CFG0	00000000b	PWMCR	00xx0000b
P3CFG1	00000000b	PWMPRD	11111111b
TCON	0000xxxxb	PWMDTY1	00000000b
TMOD	00000000b	PWMDTY0	00000000b
TH0	00000000b	PWMCFG	xx00x000b

7.4 CLOCK

The SC91F72B is integrated an adjustable high-precision IRC oscillator for which the factory setting is precisely tuned to 8MHz @ 5V/25. User can change system clock to 16M Hz by programmer. But in the 16M mode, IAP function can not be used.

The IRC deviation will be controlled less than ±2% in the condition of 5V operating Voltage and temperature (-40~85℃).

7.5 STOP

SC91F72B provides a special SFR PCON. CPU will enter STOP mode if user write “1” to PCON.1. In STOP mode, MCU can be waked up by INT0~INT7 and external Reset.

PCON (87h) Power control register（write only）

Bit No	7	6	5	4	3	2	1	0
SYMBOL	-	-	-	-	-	-	STOP	-
R/W	-	-	-	-	-	-	write only	-
Reset	x	x	x	x	x	x	0	x

Bit No	SYMBOL	Description
1	**STOP**	STOP mode control 0： operating mode 1： STOP mode , internal oscillator stop

8 INSTRUCTION SET

8.1 CPU

THE SC91F72B CPU is an ultra-fast 1T standard 8051 CORE; the instruction is fully compatible with the traditional 8051 microcontroller core.

8.2 ADDRESSING MODE

The SC91F72B 1T 8051 CPU instruction addressing modes: ① immediately addressing ② directly addressing ③ indirect addressing ④ register addressing ⑤ relative addressing ⑥Indexed Addressing ⑦ bit addressing

8.3 INSTRUCTION SET

Instruction set table

Op code	Description	Byte	Cycle
Arithmetic operations			

ADD A, Rn	Add register to accumulator	1	1
ADD A, direct	Add direct byte to accumulator	2	2
ADD A, @Ri	Add indirect RAM to accumulator	1	2
ADD A, #data	Add immediate data to accumulator	2	2
ADDC A, Rn	Add register to accumulator with carry flag	1	1
ADDC A, direct	Add direct byte to A with carry flag	2	2
ADDC A, @Ri	Add indirect RAM to A with carry flag	1	2
ADDC A, #data	Add immediate data to A with carry flag	2	2
SUBB A, Rn	Subtract register from A with borrow	1	1
SUBB A, direct	Subtract direct byte from A with borrow	2	2
SUBB A, @Ri	Subtract indirect RAM from A with borrow	1	2
SUBB A, #data	Subtract immediate data from A with borrow	2	2
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	2
INC direct	Increment direct byte	2	3
INC @Ri	Increment indirect RAM	1	3
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	2
DEC direct	Decrement direct byte	1	3
DEC @Ri	Decrement indirect RAM	2	3
INC DPTR	Increment data pointer	1	1
MUL AB	Multiply A and B	1	2
DIV AB	Divide A by B	1	6
DA A	Decimal adjust accumulator	1	3
Logic Operations			
ANL A, Rn	AND register to accumulator	1	1
ANL A, direct	AND direct byte to accumulator	2	2
ANL A, @Ri	AND indirect RAM to accumulator	1	2
ANL A, #data	AND immediate data to accumulator	2	2
ANL direct, A	AND accumulator to direct byte	2	3
ANL direct, #data	AND immediate data to direct byte	3	3
ORL A, Rn	OR register to accumulator	1	1
ORL A, direct	OR direct byte to accumulator	2	2
ORL A, @Ri	OR indirect RAM to accumulator	1	2
ORL A, #data	OR immediate data to accumulator	2	2
ORL direct, A	OR accumulator to direct byte	2	3
ORL direct, #data	OR immediate data to direct byte	3	3
XRL A, Rn	Exclusive OR register to accumulator	1	1
XRL A, direct	Exclusive OR direct byte to accumulator	2	2
XRL A, @Ri	Exclusive OR indirect RAM to accumulator	1	2
XRL A, #data	Exclusive OR immediate data to accumulator	2	2
XRL direct, A	Exclusive OR accumulator to direct byte	2	3
XRL direct, #data	Exclusive OR immediate data to direct byte	3	3
CLR A	Clear accumulator	1	1
CPL A	Complement accumulator	1	1
RL A	Rotate accumulator left	1	1
RLC A	Rotate accumulator left through carry	1	1
RR A	Rotate accumulator right	1	1
RRC A	Rotate accumulator right through carry	1	1
SWAP A	Swap nibbles within the accumulator	1	1
Boolean Manipulation			
CLR C	Clear carry flag	1	1
CLR bit	Clear direct bit	2	3
SETB C	Set carry flag	1	1
SETB bit	Set direct bit	2	3
CPL C	Complement carry flag	1	1
CPL bit	Complement direct bit	2	3
ANL C, bit	AND direct bit to carry flag	2	2
ANL C,/bit	AND complement of direct bit to carry	2	2
ORL C,bit	OR direct bit to carry flag	2	2

ORL C,/bit	OR complement of direct bit to carry	2	2
MOV C, bit	Move direct bit to carry flag	2	2
MOV bit, C	Move carry flag to direct bit	2	3
JC rel	Jump if carry flag is set	2	3
JNC rel	Jump if carry flag is not set	2	3
JB bit, rel	Jump if direct bit is set	3	5
JNB bit, rel	Jump if direct bit is not set	3	5
JBC bit, rel	Jump if direct bit is set and clear bit	3	5
Data Transfers			
MOV A, Rn	Move register to accumulator	1	1
MOV A, direct	Move direct byte to accumulator	2	2
MOV A, @Ri	Move indirect RAM to accumulator	1	2
MOV A, #data	Move immediate data to accumulator	2	2
MOV Rn, A	Move accumulator to register	1	1
MOV Rn, direct	Move direct byte to register	2	3
MOV Rn, #data	Move immediate data to register	2	2
MOV direct, A	Move accumulator to direct byte	2	2
MOV direct, Rn	Move register to direct byte	2	2
MOV direct1,direct2	Move direct byte to direct byte	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	2	3
MOV direct, #data	Move immediate data to direct byte	3	3
MOV @Ri, A	Move accumulator to indirect RAM	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	2	2
MOV DPTR,#data16	Load data pointer with a 16-bit constant	3	3
MOVC A,@A+DPTR	Move code byte relative to DPTR to A	1	5
MOVC A,@A+PC	Move code byte relative to PC to A	1	4
MOVX A，@Ri	Move external RAM (8-bit address) to A	1	3
MOVX @Ri，A	Move external RAM (16-bit address) to A	1	4
MOVX A,@DPTR	Move A to external RAM (8-bit address)	1	2
MOVX @DPTR，A	Move A to external RAM (16-bit address)	1	3
PUSH direct	Push direct byte onto stack	2	3
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange register with accumulator	1	2
XCH A, direct	Exchange direct byte with accumulator	2	3
XCH A, @Ri	Exchange indirect RAM with accumulator	1	3
XCHD A, @Ri	Exchange low-order nibble indirect RAM with A	1	3
Program Branches			
ACALL address11	Absolute subroutine call	2	4
LCALL address16	Long subroutine call	3	4
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
AJMP address11	Absolute jump	2	3
LJMP address16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A+DPTR	Jump indirect relative to the DPTR	1	5
JZ rel	Jump if accumulator is zero	2	4
JNZ rel	Jump if accumulator is not zero	2	4
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	5
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	4
CJNE Rn, #data, rel	Compare immediate to reg. and jump if not equal	3	4
CJNE @Ri, #data, rel	Compare immediate to Ri and jump if not equal	3	5
DJNZ Rn, rel	Decrement register and jump if not zero	2	4
DJNZ direct, rel		3	5

	Decrement direct byte and jump if not zero		
NOP	No operation	1	1
MOVC instruction in SC91F72B prohibit addressing ROM addressed 0000~00FFH.			

9 INTERRUPT

The SC91F72B provide total 12 interrupt sources：Timer0, Timer1, PWM, ADC, INT0~INT7. Each interrupt source can be individually enable and disable by setting or clearing the corresponding bit in the register IE & EXIE. The IE register also contains global interrupt enable bit, EA, which can enable/disable all the interrupts at once. Each interrupt has its own interrupt flag, interrupt vector, interrupt enable bit and interrupt priority.

9.1 INTERRUPT SOURCE & VECTOR

Interrupt Summary：

Interrupt source	Interrupt timing	Interrupt flag	Enable bit	Interrupt priority	vector address	Polling priority	Interrupt No（C51）	Clearing flag	Wake up STOP
Timer0	Timer0 overflow	TCON[5] (TF0)	IE[1] (ET0)	IP[1]	000BH	1（high）	1	H/W Auto	no
Timer1	Timer1 overflow	TCON[7] (TF1)	IE[3] (ET1)	IP[3]	001BH	2	3	H/W Auto	no
PWM	PWM overflow	PWMCR[7] (PWMIF)	IE[5] (EPWM)	IP[5]	002BH	3	5	User Software	no
ADC	ADC complete	ADCCR[4] (EOC/ADCIF)	IE[6] (EADC)	IP[6]	0033H	4	6	User Software	no
INT0	N-edge	Hidden	EXIE[0]	EXIP[0]	003BH	5	7	H/W Auto	yes
INT1	N	Hidden	EXIE[1]	EXIP[1]	0043H	6	8	H/W Auto	yes
INT2	N	Hidden	EXIE[2]	EXIP[2]	004BH	7	9	H/W Auto	yes
INT3	N	Hidden	EXIE[3]	EXIP[3]	0053H	8	10	H/W Auto	yes
INT4	N-edge P-edge Double edge	Hidden	EXIE[4]	EXIP[4]	005BH	9	11	H/W Auto	yes
INT5	N	Hidden	EXIE[5]	EXIP[5]	0063H	10	12	H/W Auto	yes
INT6	N	Hidden	EXIE[6]	EXIP[6]	006BH	11	13	H/W Auto	yes
INT7	N	Hidden	EXIE[7]	EXIP[7]	0073H	12（low）	14	H/W Auto	yes

Setting all the bits in register IE, when interrupt occurs, corresponding flag will be set by hardware.

The **Timer0/1 interrupt** is generated when they overflows, the flag (TF0/1) in the register TCON, which is set by hardware, and will be automatically be cleared by hardware when the service routine is vectored.

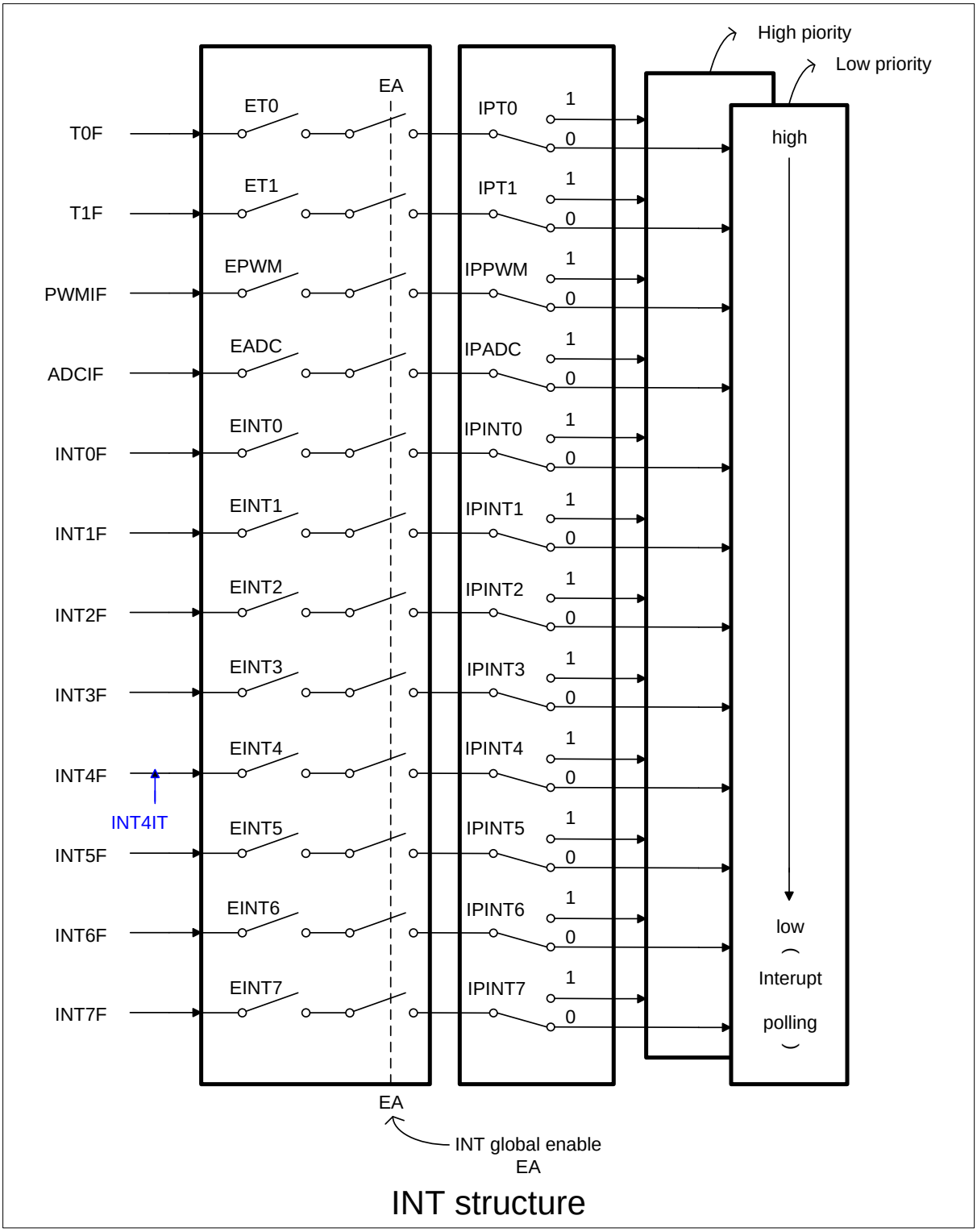
The **PWM interrupt** is generated by PWMIF. The flag can be cleared by software.

The **ADC interrupt** is generated by ADCIF/EOC. If an interrupt is generated, the converted result in ADCH/ADCL will be valid. If continuous compare function in ADC Module is Enabling, ADCIF will not be set at each conversion, but set if converted result is larger than compare value. The ADCIF flag must be cleared by software.

External INTx(x=0~7)：External interrupt INT0~7 have separate interrupt vectors. When the external interrupt port interrupt condition occurs, the external interrupt occurred. Eight external interrupt flag is hidden, hardware will automatically clear and does not require user to clear. External INT INT0~3 and INT5~7 only respond to the negative edge triggered without user settings. INT4 default for negative edge triggered external interrupt, if the user need double-edge or positive edge triggered interrupt, can be achieved by setting SFRs (INT4IT)。Users can set the priority of each interrupt by SFR registers EXIP. INT0~7 also can wake up the STOP of the SC91F72B.

9.2 INTERRUPT DIAGRAM

interrupt diagram：



INT structure

9.3 INTERRUPT PRIORITY

Each interrupt source can be individually programmed to one of two priority levels by setting or clearing corresponding bits in the register IP.

An interrupt service routine in progress can be interrupted by a higher priority interrupt, but can not by another interrupt with the same or lower priority.

If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If request of the same priority level are pending at the start of an instruction cycle, an internal polling sequence determines which request is serviced.

9.4 INTERRUPT HANDLING

When an interrupt occurs, the main program is interrupted. CPU will perform the following operation:

1， complete the instruction being executed;
2， Push on the PC to stack;
3， Long Call to the interrupt vector;
4， executing the corresponding interrupt service routine;
5， complete the interrupt service routine and RETI;
6， POP the PC from stack, and return the program before the interrupt.

In this process, the system does not immediately interrupt the other with the same priority, but the flag will be retained. System will perform the retained interrupt request after completing the interrupt handling in the current.

9.5 SFR REGISTERS FOR INTERRUPT

IE (A8h) intterupt enable register(R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	EA	EADC	EPWM	-	ET1	-	ET0	-
R/W	R/W	R/W	R/W	-	R/W	-	R/W	-
Reset	0	0	0	x	0	x	0	x

Bit No	Symbol	Description
7	**EA**	All interrupt enable bit 0: Disable all interrupt 1: Enable all interrupt
6	**EADC**	ADC interrupt enable bit 0: Disable ADC interrupt 1: Enable ADC interrupt
5	**EPWM**	PWM interrupt enable bit 0: Disable PWM interrupt 1: Enable PWM interrupt
3	**ET1**	Timer1 interrupt enable bit 0: Disable timer1 interrupt 1: Enable tomer1 interrupt
1	**ET0**	Timer0 interrupt enable bit 0: Disable timer0 interrupt 1: Enable timer0 interrupt
4,2,0	**reserved**	reserved

IP (B8h) interrupt priority(R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	-	IPADC	IPPWM	-	IPT1	-	IPT0	-
R/W	-	R/W	R/W	-	R/W	-	R/W	-
Reset	x	0	0	x	0	x	0	x

Bit No	Symbol	Description
6	**IPADC**	ADC interrupt priority 0：ADC low priority 1：ADC high priority
5	**IPPWM**	PWM interrupt priority

		0：PWM low priority 1：PWM high priority
3	**IPT1**	Timer1 interrupt priority 0：Timer1 low priority 1：Timer1 high priority
1	**IPT0**	Timer0 interrupt priority 0：Timer0 low priority 1：Timer0 high priority
7,4,2,0	**reserved**	Reserved

EXIE (B4h) External interrupt enable(R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit No	Symbol	Description
7~0	**EINTx (x=0~7)**	External interrupt enable 0： disable INTx(x=0~7) 1： enable INTx(x=0~7)

EXIP (B5h) External interrupt priority(R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	IPEX7	IPEX6	IPEX5	IPEX4	IPEX3	IPEX2	IPEX1	IPEX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit No	Symbol	Description
7~2	**IPEXn (n=0~7)**	EXT INT priority selection 0 : INTn(n=0~7) priority low 1: INTn(n=0~7) priority high
1,0	**reserved**	reserved

INT4IT (93h) INT4 edge type(R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT4ES[1:0]	
R/W	-	-	-	-	-	-	R/W	R/W
Reset	x	x	x	x	x	x	0	0

Bit No	Symbol	Description
1,0	**INT4ES[1:0]**	INT4 Edge Selction 00：N-edge 01：reserved 10：double edge 11：P-edge
7~2	**reserved**	reserved

10 TIMER0/TIMER1

The SC91F72B has two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. The two Timer/Counters can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a “Timer”, the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the “Counter” mode, the register is incremented on the falling edge of the external input pins.

The “Timer” or “Counter” function is selected by the “CTx” bit in the TMOD SFR. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0x and M1x in the TMOD SFR.

Timer/Counter0 has 4 Modes, and Timer/Counter1 has 3 Mode only (No Mode 3）：

① Mode 0：13-bit up Timer/Counter
② Mode 1：16-bit up Timer/Counter
③ Mode 2：Auto-reload up 8-bit Timer/Counter
④ Mode 3：Two 8-bit up Timer/Counters

10.1 TIMER SFR

Symbol	Address	Description	7	6	5	4	3	2	1	0	Reset
TCON	**88H**	Timer control	TF1	TR1	TF0	TR0	-	-	-	-	0000xxxxb
TMOD	**89H**	Timer Mode	GATE1	C/T1	M11	M01	GATE0	C/T0	M10	M00	00000000b
TL0	**8AH**	Timer0 Low									00000000b
TL1	**8BH**	Timer1 Low									00000000b
TH0	**8CH**	Timer0 high									00000000b
TH1	**8DH**	Timer1 high									00000000b
TMCON	**8EH**	Timer clock selection	-	-	-	-	-	-	T1FD	T0FD	xxxxxx00b

TCON (88h) Timer Control Register (R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	-	-	-	-
R/W	R/W	R/W	R/W	R/W	-	-	-	-
Reset	0	0	0	0	x	x	x	x

Bit No	Symbol	Description
7	**TF1**	Timer1 overflow flag. 0: Timer1 no overflow ,can be cleared by software 1: Timer1 overflow, set by hardware;
6	**TR1**	Timer1 start/stop Control bits 0: Stop timer1 1: Start timer1
5	**TF0**	Timer0 overflow flag. 0: Timer0 no overflow ,can be cleared by software 1: Timer0 overflow, set by hardware;
4	**TR0**	Timer0 start/stop Control bits 0: Stop timer0 1: Start timer0
3~0	**reserved**	reserved

TMOD (89h) Timer Mode Control Register（R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	GATE1	C/T1	M11	M01	GATE0	C/T0	M10	M00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

	T1	T0

Bit No	Symbol	Description
7	**GATE1**	Timer1 Gate control bits 0: Timer1 is enabled whenever TR1 control bit is set 1: Timer1 is disable
6	**C/T1**	Timer1 Timer/Counter mode selected bits 0：Timer Mode， Timer CLK source is from system CLK 1：Counter Mode, Counter CLK source is from external pin P1.3
5,4	**M11,M01**	Timer1 Mode Selected bits 0 0 ： Mode0, 13bit up timer/Counter, bit7~5 of TL1 is ignored 0 1 ： Mode1, 16bit up Timer/Counter 1 0 ： Mode2, 8bit auto-reload up Timer/Counter 1 1 ： Reserved
3	**GATE0**	Timer0 Gate control bits 0: Timer0 is enabled whenever TR0 control bit is set 1: Timer0 is disable
2	**C/T0**	Timer0 Timer/Counter mode selected bits 0：Timer Mode， Timer CLK source is from system CLK 1：Counter Mode, Counter CLK source is from external pin P1.3
1,0	**M10,M00**	Timer0 Mode Selected bits 0 0 ： Mode0, 13bit up timer/Counter, bit7~5 of TL1 is ignored 0 1 ： Mode1, 16bit up Timer/Counter 1 0 ： Mode2, 8bit auto-reload up Timer/Counter 1 1 ： Mode3, two 8 bit up timer

TMCON (8Eh) Timer Clock Selection Register（R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	T1FD	T0FD
R/W	-	-	-	-	-	-	R/W	R/W
Reset	x	x	x	x	x	x	0	0

Bit No	Symbol	Description
1	**T1FD**	Timer1 Clock source selected bit 0：Timer1 clock source is from Fosc/12 1：Timer1 clock source is from Fosc/4
0	**T0FD**	Timer0 Clock source selected bit 0：Timer0 clock source is from Fosc/12 1：Timer0 clock source is from Fosc/4
7~2	**reserved**	reserved

IE (A8h) Interrupt enable control Register（R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	EA	EADC	EPWM	-	ET1	-	ET0	-
R/W	R/W	R/W	R/W	-	R/W	-	R/W	-
Reset	0	0	0	x	0	x	0	x

Bit No	Symbol	Description
3	**ET1**	Timer1interrupt enable control 0：Disable Timer1 interrupt 1： Enable Timer1 interrupt
1	**ET0**	Timer0 interrupt enable control 0：Disable Timer0 interrupt

		1： Enable Timer0 interrupt

IP (B8h) Interrupt Priority Register（R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	-	IPADC	IPPWM	-	IPT1	-	IPT0	-
R/W	-	R/W	R/W	-	R/W	-	R/W	-
Reset	x	0	0	x	0	x	0	X

Bit No	Symbol	Description
3	**IPT1**	Timer1interrupt priority 0：Timer 1 interrupt priority low 1：Timer 1 interrupt priority high
1	**IPT0**	Timer0 interrupt priority 0：Timer0 interrupt priority low 1：Timer0 interrupt priority high

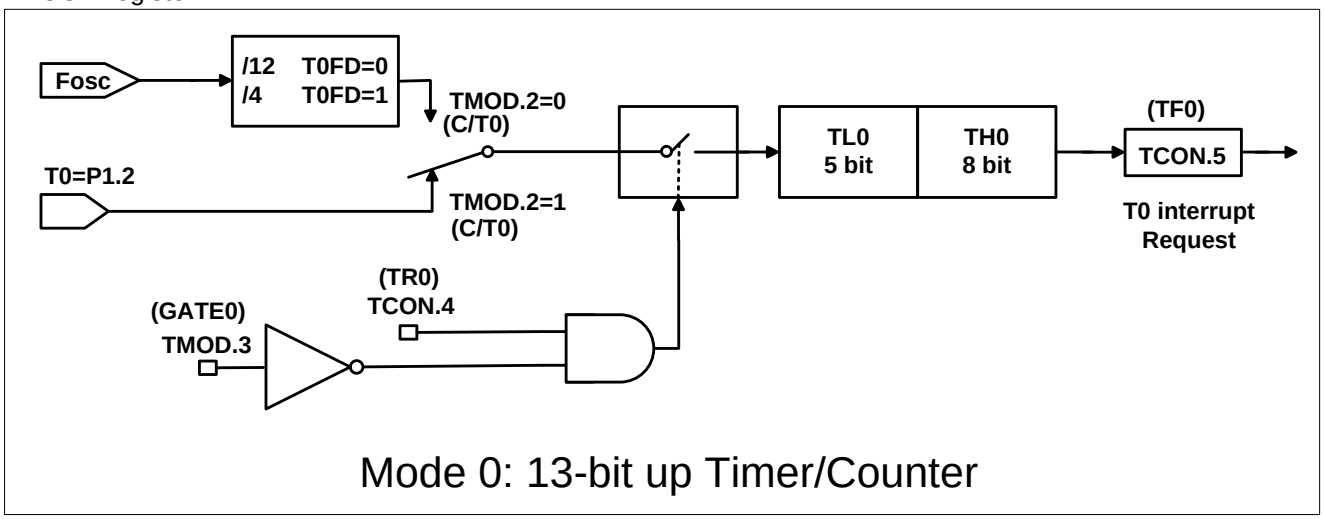
10.2 TIMER0 MODE

Mode 0: 13-bit Timer/Counter

Timer0 operate as 13-bit timer/counters in mode0. The TH0 register holds the high 8bits of the 13-bit timer/counter, TL0 holds the 5 low bits TL0.4~TL0.0. The three upper bits(TL0.7~TL0.5) of TL0 are indeterminate and should be ignored when reading. As the 13-bit timer register increments and overflow, the timer0 overflow flag is set and an interrupt will occur if Timer0 interrupt is enabled.

The CT0 bit selects the timer/counter's clock source. If CT0=1, high-to-low transitions at the Timer input pin(T0) will increase the timer/counter Data register. Else if CT0=0, selects the system clock to increase the timer/counter Data register. Setting the TR0 bit anables the timer when GATE0=0.

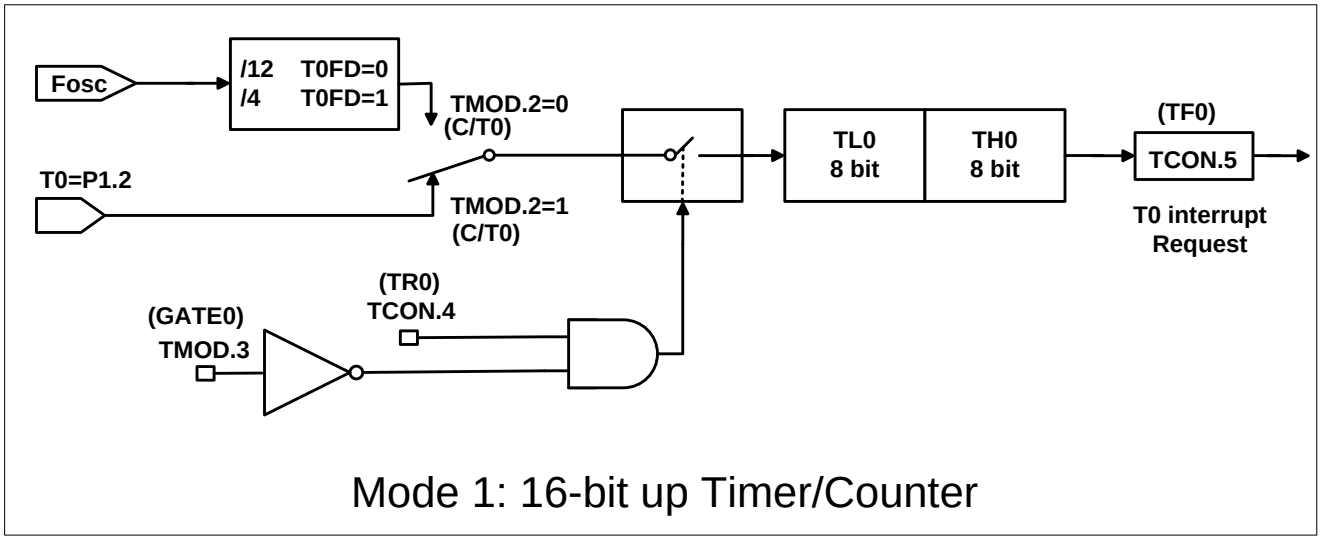
1/4 system clock or 1/12 system clock can be selected as Timer0 clock source by configuring T0FD bit in TMCON register.



Mode 0: 13-bit up Timer/Counter

Mode1:16-bit Timer/Counter

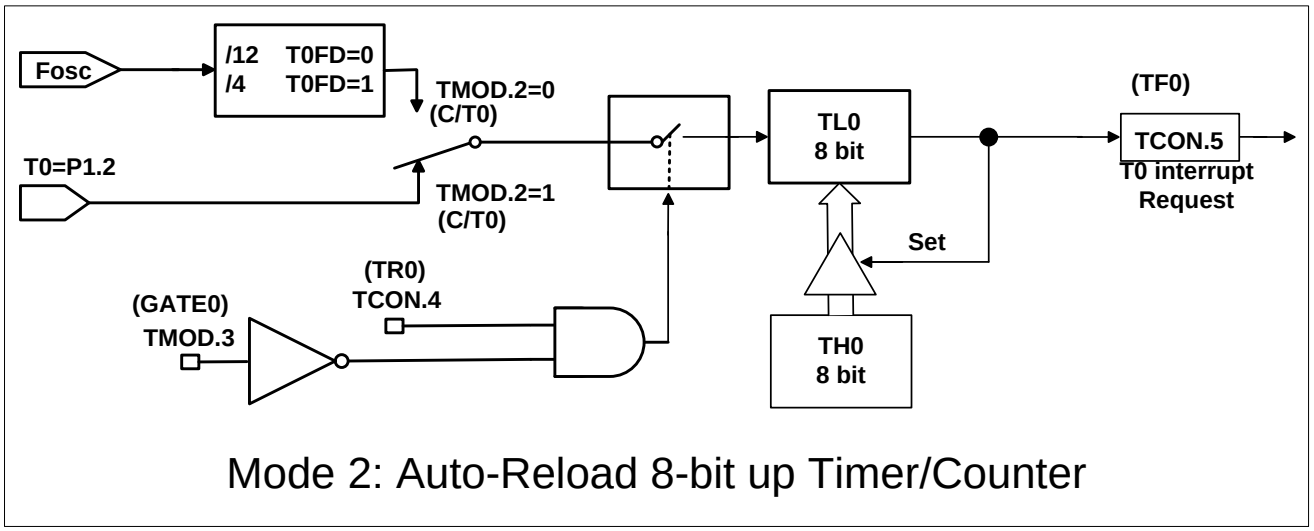
Mode1 operation is the same as Mode 0, except that the Timer/Counter register use all 16 bits. The Timer/Counter are enabled and configured in Mode1 in the same manner as for Mode 0.



Mode 1: 16-bit up Timer/Counter

Mode 2: 8-bit auto-reload Timer/Counter

Mode 2 configures timer0 to operate as 8-bit timer/counters with automatic reload of the start value. TL0 holds the count and TH0 holds the reload value. When the counter in TL0 overflows from 0xFF to TH0, the timer overflow flag TF0 is set and the counter in TL0 is reloaded from TH0. If Timer0 interrupt are enabled, an interrupt will occur when the TF0 flag is set. The reload value in TH0 is not changed. TL0 must be initialized to the desired value before enabling the timer for the first count to be correct. Except the Auto-reload function, both timer/counters are enable and configures in Mode2 is the same as in Mode 0 & Mode 1.

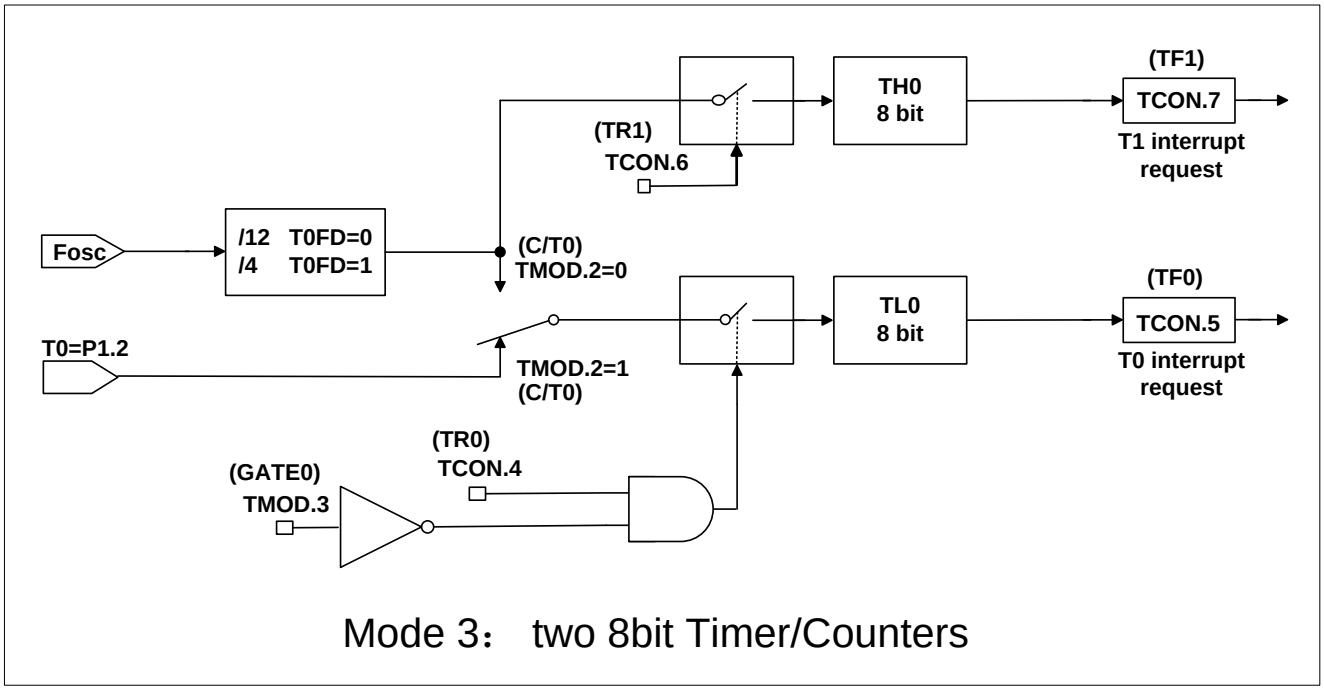


Mode 2: Auto-Reload 8-bit up Timer/Counter

Mode 3：Two 8-bit Timer/Counters(Timer0 only）

In Mode 3, Timer0 is configured as two separate 8-bit timer/counters held in TL0 and TH0. TL0 is controlled using the timer0 control/status bits in TCON and TMOD: TR0, CT0, GATE0 and TF0. TL0 can use either the system clock or an external input signal as it's time base.

The TH0 is restricted to a timer function sourced by the system clock. TH0 is enabled using the Timer1 control bit TR1. TH0 sets the timer1 overflow flag TF1 on overflow and thus controls the timer 1 interrupt.



Mode 3： two 8bit Timer/Counters

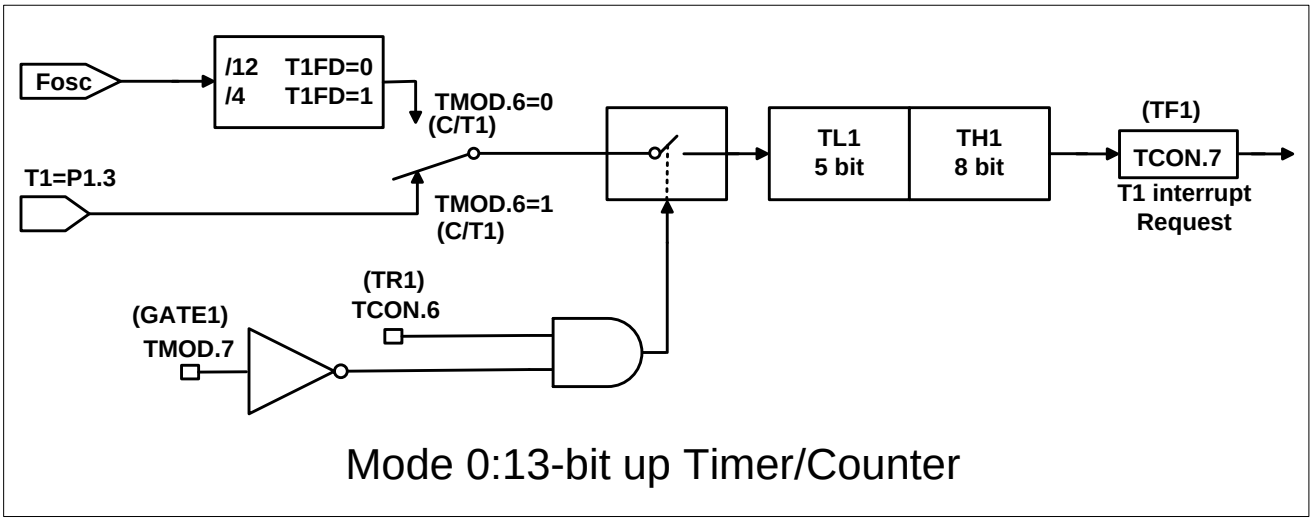
10.3 TIMER1 MODE

Mode 0: 13-bit Timer/Counter

Timer1 operate as 13-bit timer/counters in mode0. The TH1 register holds the high 8bits of the 13-bit timer/counter, TL1 holds the 5 low bits TL1.4~TL1.0. The three upper bits(TL1.7~TL1.5) of TL1 are indeterminate and should be ignored when reading. As the 13-bit timer register increments and overflow, the timer1 overflow flag is set and an interrupt will occur if Timer1 interrupt is enabled.

The CT1 bit selects the timer/counter's clock source. If CT1=1, high-to-low transitions at the Timer input pin(T1) will increase the timer/counter Data register. Else if CT1=0, selects the system clock to increase the timer/counter Data register. Setting the TR1 bit anables the timer when GATE1=0.

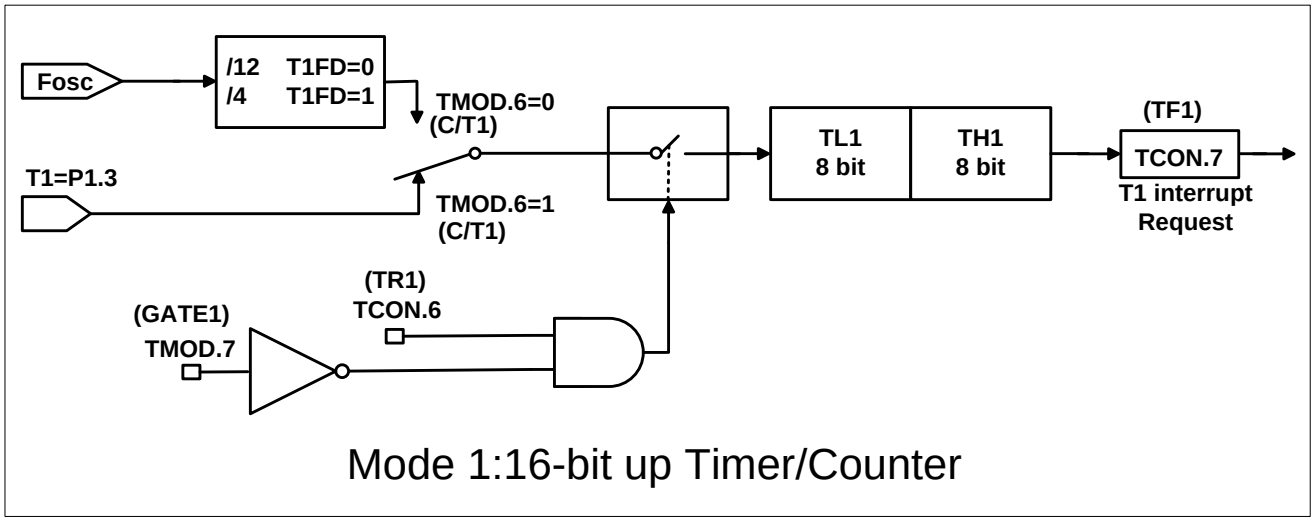
1/4 system clock or 1/12 system clock can be selected as Timer0 clock source by configuring T1FD bit in TMCON register.



Mode 0:13-bit up Timer/Counter

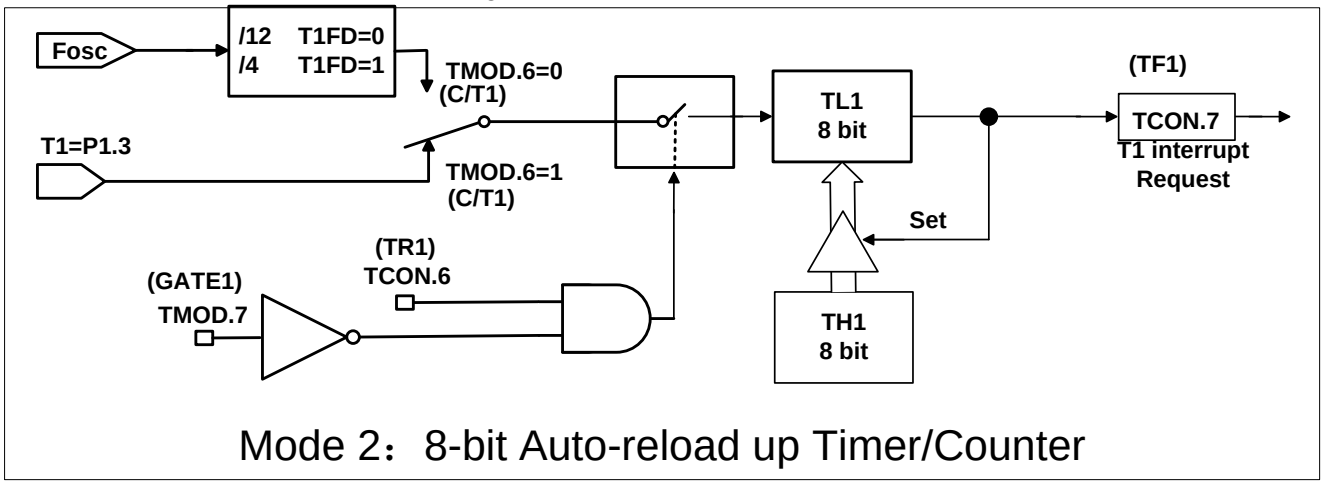
Mode1:16-bit Timer/Counter

Mode1 operation is the same as Mode 0, except that the Timer/Counter register use all 16 bits. The Timer/Counter are enabled and configured in Mode1 in the same manner as for Mode 0.



Mode 2: 8-bit auto-reload Timer/Counter

Mode 2 configures timer1 to operate as 8-bit timer/counters with automatic reload of the start value. TL1 holds the count and TH1 holds the reload value. When the counter in TL1 overflows from 0xFF to TH1, the timer overflow flag TF1 is set and the counter in TL1 is reloaded from TH1. If Timer1 interrupt are enabled, an interrupt will occur when the TF1 flag is set. The reload value in TH1 is not changed. TL1 must be initialized to the desired value before enabling the timer for the first count to be correct. Except the Auto-reload function, both timer/counters are enable and configures in Mode2 is the same as in Mode 0 & Mode 1.



11 PWM

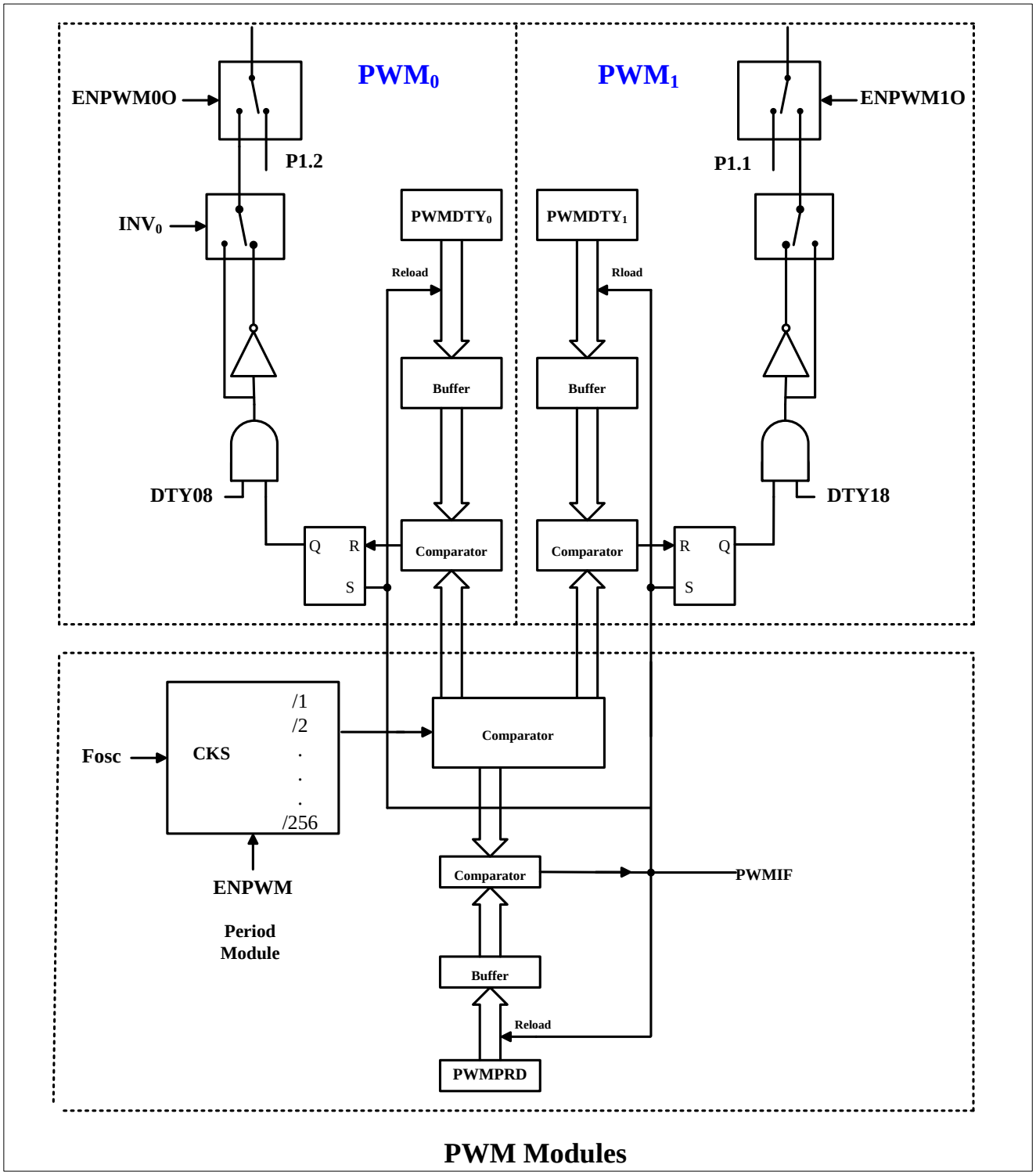
The SC91F72B provides a separate counter; it can support two PWM outputs: PWM1 and PWM0.

PWM Features:

① 8-bit PWM Modules
② PWM0 and PWM1 have the same period, but the duty cycle can be independently set
③ Selectable output polarity
④ Provide interrupt function on period overflow

The SC91F72B has an 8-bit PWM Modules, it provide two channel PWM output. The PWM Modules can provide the pulse width modulation waveform with the period and the duty being controlled, individually. The PWMPRD is used to control the period cycle of the PWM0 and PWM1. The PWMDTY0 is used to control the duty in the waveform of the PWM0, and the PWMDTY1 is used for PWM1. PWMCR and PWMCFG are used to control and configure the PWM Modules.

11.1 PWM DIAGRAM



PWM Modules

11.2 PWM SFR

PWMCR (F8h)PWM Control Register（R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	ENPWM	PWMIF	-	-	DTY18	ENPWM1O	DTY08	ENPWM0O

R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset	0	0	x	x	0	0	0	0

Bit No	Symbol	Description
7	**ENPWM**	PWM Module Enable 1：PWM Module ON 0：PWM Module Off
6	**PWMIF**	**PWM I**nterrupt **F**lag 0: PWM period counter not overflow 1: Set by hardware to indicate that the PWM period counter overflow, must be cleared by software
3	**DTY18**	Force PWM1 as HIGH 1：PWM1 output always high 0：PWM1 output is controlled by PWMPRD and PWMDTY1
2	**ENPWM1O**	PWM1and P1.1 share selection 1：PWM1 output enable 0：PWM1 output disable, used as GPIO P1.1
1	**DTY08**	Force PWM0 as HIGH 1：PWM0 output always high 0：PWM0 output is controlled by PWMPRD and PWMDTY0
0	**ENPWM0O**	PWM0 and P1.2 share selection 1：PWM0 output enable 0：PWM0 output disable, used as GPIO P1.2
5,4	**reserved**	reserved

PWMPRD (F9h) PWM period control Register（R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	**PWMPRD[7:0]**							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit No	Symbol	Description
7~0	**PWMPRD[7:0]**	PWM output period cycle=(PWMPRD[7:0]+1)*PWM CLK

PWMCFG (FCh) PWM configuration Register（R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	-	-	INV1	INV0	-	CKS[2:0]		
R/W	-	-	R/W	R/W	-	R/W		
Reset	x	x	0	0	x	0	0	0

Bit No	Symbol	Description
5	**INV1**	**INV**erse PWM**1** Output 1 ： Inverse the PWM1 output 0 ： Don’t Inverse the PWM1 output
4	**INV0**	**INV**erse PWM0 Output 1 ： Inverse the PWM0 output 0 ： Don’t Inverse the PWM0 output
2~0	**CKS**	PWM **C**loc**k** source **S**election 000：Fosc 001：Fosc/2 010：Fosc/4 011：Fosc/8

		100：Fosc/32 101：Fosc/64 110：Fosc/128 111：Fosc/256
7,6,3	**reversed**	reversed

PWMDTY1 (FAh) PWM1 Duty Control Register（R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	**PWMDTY1[7:0]**							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit No	Symbol	Description
7~0	**PWMDTY1[7:0]**	PWM1 Duty = (PWMDTY1[7:0])* PWM CLK

PWMDTY0 (FBh) PWM0 Duty Control Register（R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	**PWMDTY0[7:0]**							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit No	Symbol	Description
7~0	**PWMDTY0[7:0]**	PWM0 Duty = (PWMDTY0[7:0])* PWM CLK

IE (A8h) Interrupt enable（R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	EA	EADC	EPWM	-	ET1	-	ET0	-
R/W	R/W	R/W	R/W	-	R/W	-	R/W	-
Reset	0	0	0	x	0	x	0	X

Bit No	Symbol	Description
5	**EPWM**	PWM interrupt enable 0：Disable PWM interrupt 1：Enable PWM interrupt

IP (B8h) Interrupt Priority (读/写)

Bit No	7	6	5	4	3	2	1	0
Symbol	-	IPADC	IPPWM	-	IPT1	-	IPT0	-
R/W	-	R/W	R/W	-	R/W	-	R/W	-
Reset	x	0	0	x	0	x	0	x

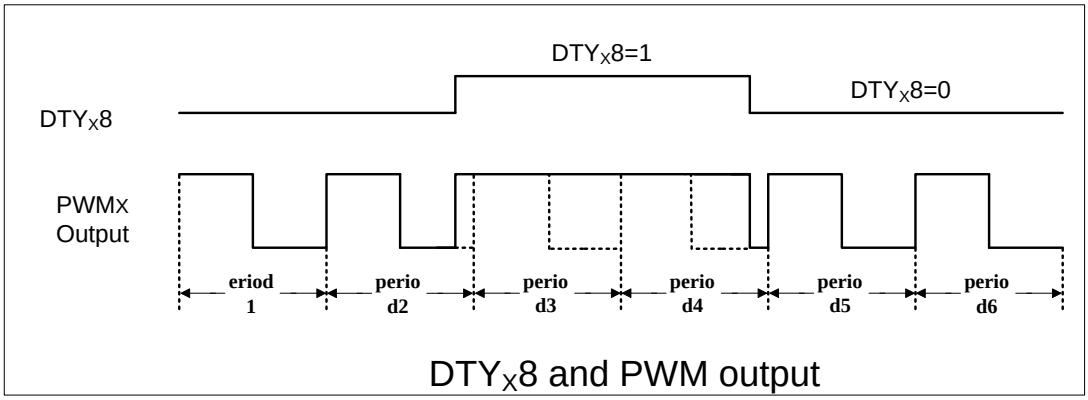
Bit No	Symbol	Description
5	**IPPWM**	PWM interrupt priority 0：PWM interrupt priority is Low 1：PWM interrupt priority is High

Note：
1. ENPWM bit is used to Enable/Disable the PWM Modules.
2. ENPWMxO bits are used to selecting the PWM output share with GPIO.
3. EPWM (IE.5) bit is used to enable/disable PWM interrupt.
4. PWM interrupt can be used as an 8-bit timer if you don't use it as PWM.
5. It is the same interrupt Vector for PWM0 and PWM1 interrupt.

11.3 PWM WAVEFORM AND APPLICATION

The SFR parameter affects the PWM waveform as follows:

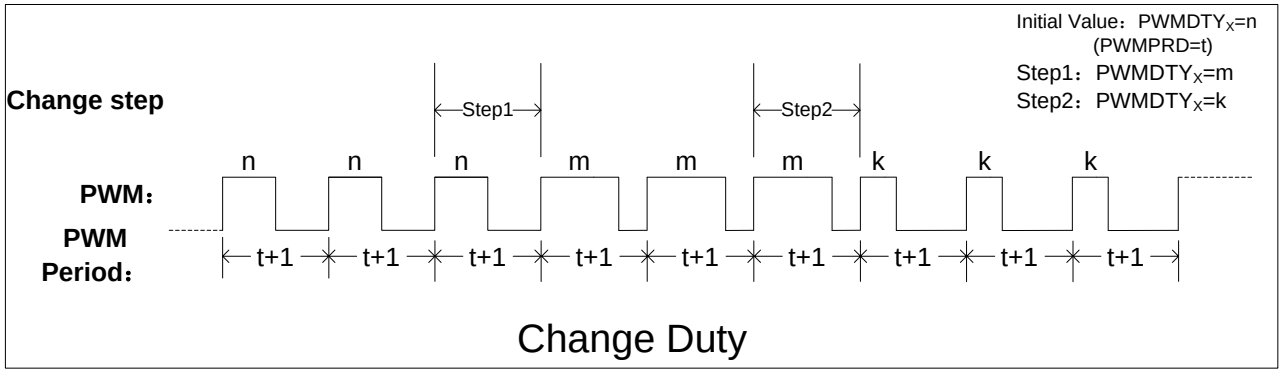
①DTYx8



DTYX8 and PWM output

When the PWMx is outputting waveform, if DTYx8 (PWMCR.1 / PWMCR.3) change, PWMx waveform will change immediately.

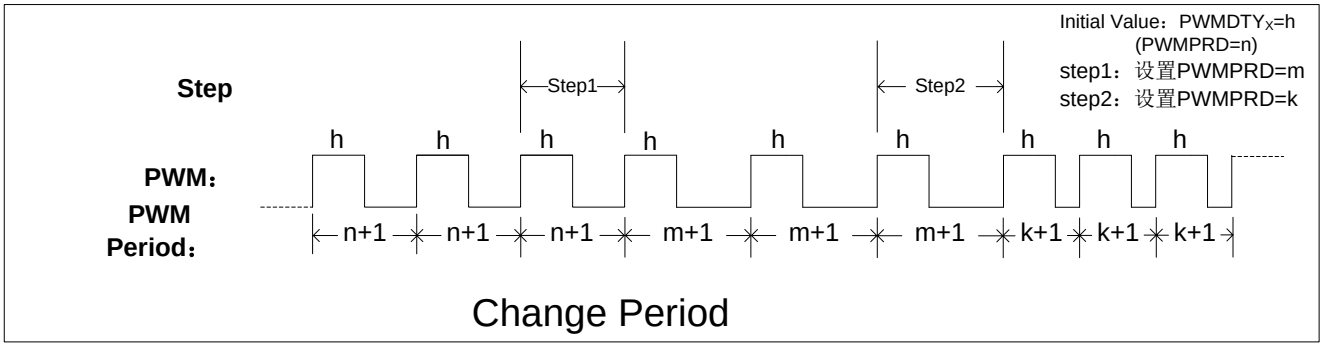
②CHANGE DUTY



Change Duty

When the PWMx is outputting waveform, user can change the duty by changing the PWMDTYx register. However, the duty cycle will not change immediately until the next PWM cycle.

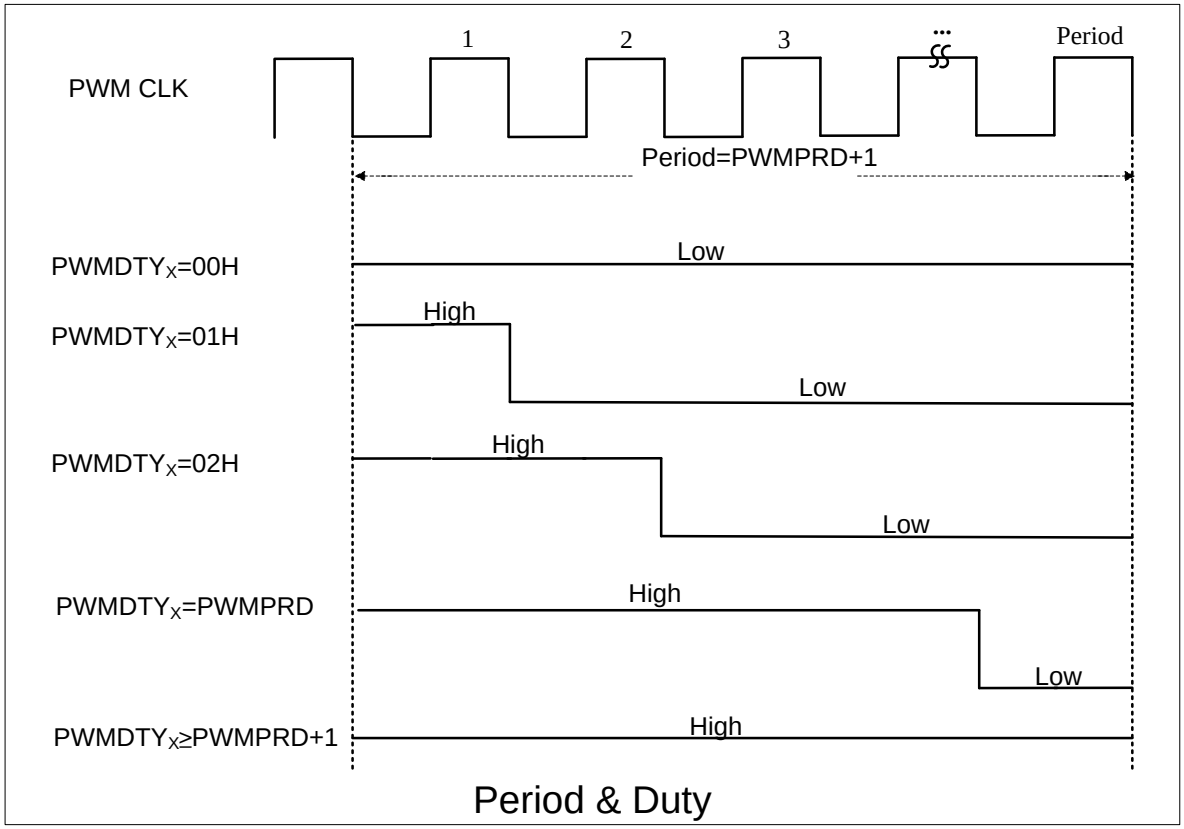
③CHANGE PERIOD



Change Period

When the PWMx is outputting waveform, user can change the period by changing the PWMPRD register. However, the period cycle will not change immediately until the next PWM cycle.

④REALTIONSHIP BETWEEN PERIODS WITH DUTY



When INVx=0, you can get the waveform of PWM as shown above. The waveform of PWMx will change immediately if you change the INVx bit.

12 GP I/O

SC91F72B provides up to 18 GPIO ports, 18 I/O multiplexed with other functions. The same as the standard 8051 I/O port, the SC91F72B I/O port is a bidirectional I/O port with a strong push-pull output. There are four I/O modes: quasi-bidirectional I/O mode, the strong push-pull output mode, high impedance input, only the N-type open-drain output mode.

12.1 GPIO STRUCTURE

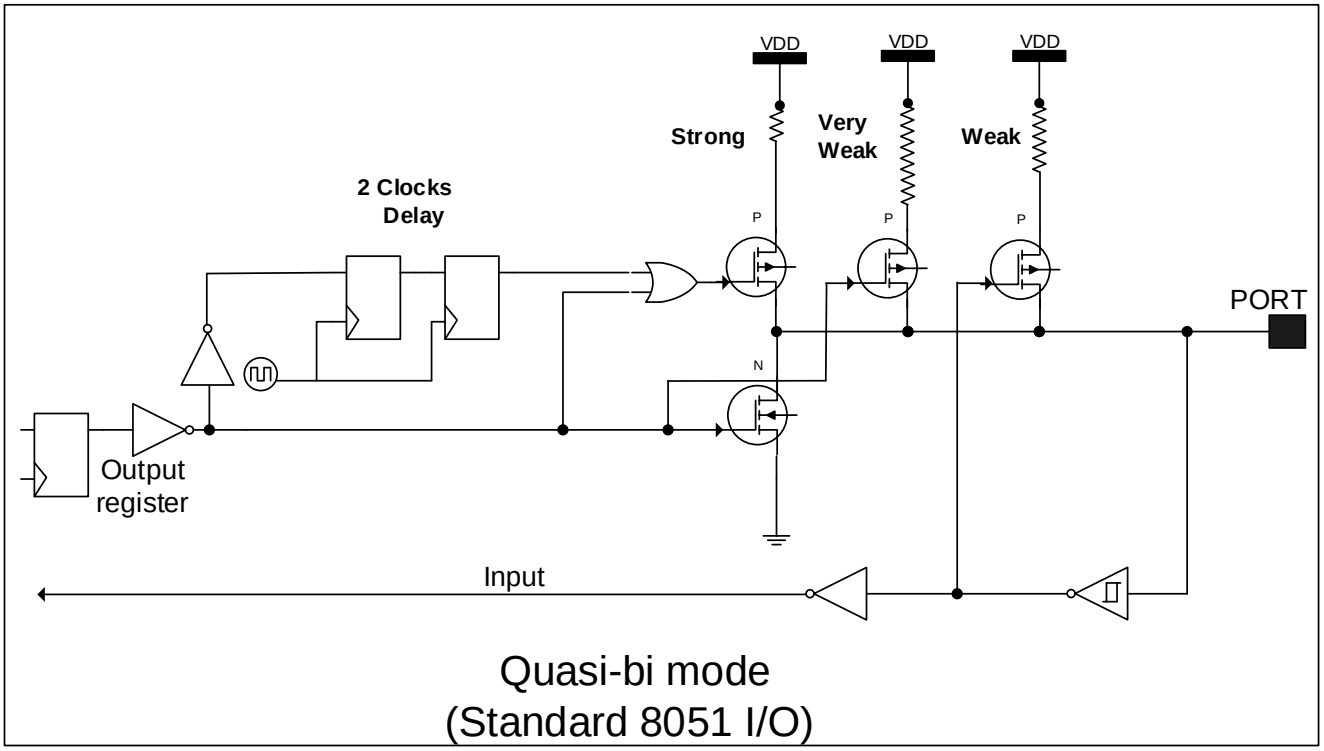
1. Quasi-Bi mode

Quasi-Bi I/O has 3 pull-up MOS to adapt to different needs: weak pull-up, very weak pull-up and strong pull-up.

Weak pull-up MOS: When Data register and pin are set 1, this pull-up provides the basic drive current that quasi- bidirectional ports output high. External circuit pull the output-high pin to low, weak pull-up will be off and very weak pull-up will keep on. In order to pull this pin low intensity, external circuit must have sufficient sink current capability to drop the voltage of port below the threshold voltage.

Very weak pull-up MOS: Provide weak pull-up current to pull the pin high when port latch is 1 and the port is floating.

Strong pull-up Mos: When the port latch transition from 0 to 1, strong pull-up is used to speed up the quasi-bi port conversion from logic 0 to logic 1 in almost 2 machine cycles. Quasi-bi model port structure diagram is shown below.

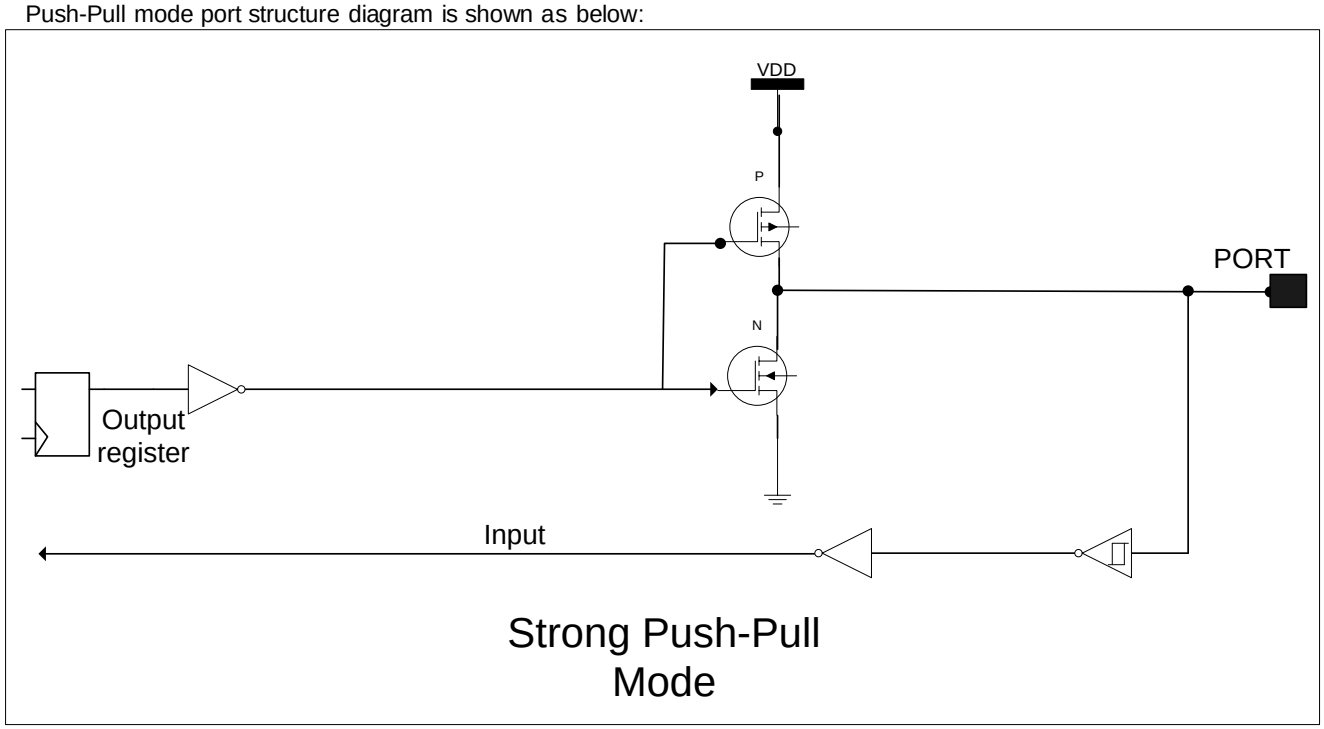


Quasi-bi mode
(Standard 8051 I/O)

2. Strong Push-Pull Mode

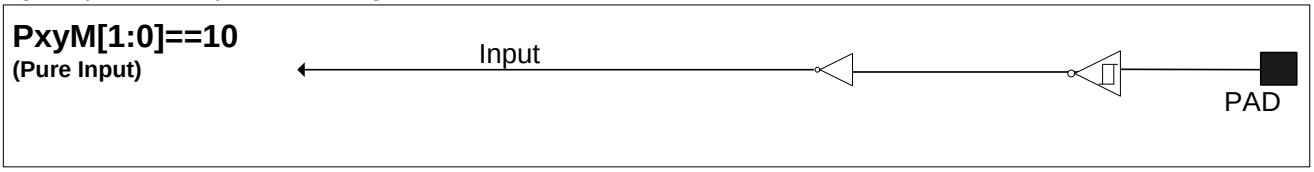
The pull-low structure in push-pull mode is same as Quasi-Bi mode, but the port provides a continuous strong pull-up when the port latch is 1.

Push-Pull mode port structure diagram is shown as below:



3， high impedance input

high impedance input mode diagram is shown as below:

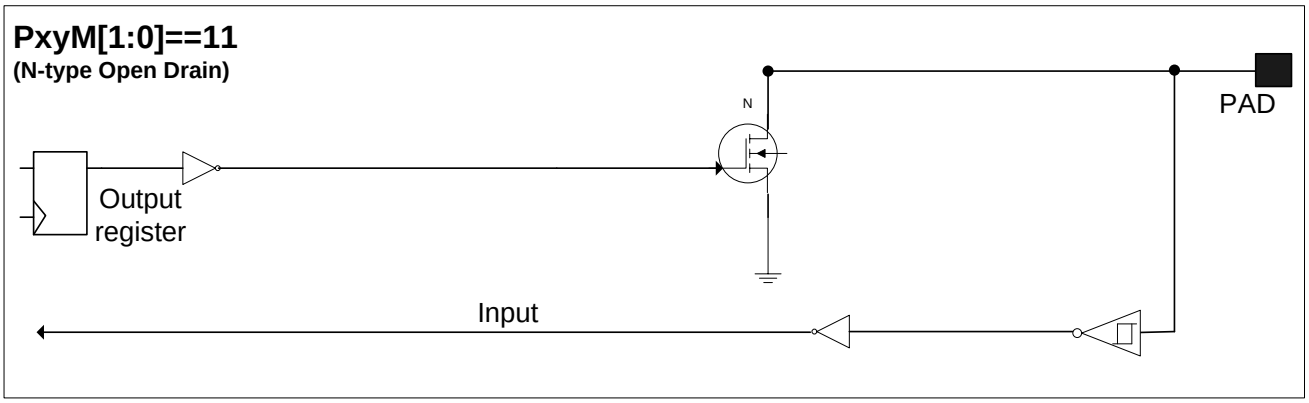


High impedance input Mode

4， Open Drain Mode

This mode does not output a high capacity. If you need high output, the user must pull-up resistor. The applied voltage on Pin can not exceed the VDD +0.3 V.

Open drain mode diagram is shown as below:



Open Drain Mode

12.2 I/O SFR

P1CFG1 (91h) P1 configuration1(R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	P17M[1:0]		P16M[1:0]		P15M[1:0]		P14M[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

P1CFG0 (92h) P1 configuration0(R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	P13M[1:0]		P12M[1:0]		P11M[1:0]		P10M[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

P2CFG0 (A2h) P2 configuration0(R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	P21M[1:0]		P20M[1:0]	
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	x	x	x	x	0	0	0	0

P3CFG1 (B1h) P3 configuration1(R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	P37M[1:0]		P36M[1:0]		P35M[1:0]		P34M[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

P3CFG0 (B2h) P3 configuration0(R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	P33M[1:0]		P32M[1:0]		P31M[1:0]		P30M[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit No	Symbol	Description
7~0	**P1xM[1:0]** **（x=0~7）**	P1 Mode setting 00：P1 as Quasi-bi mode 01：P1 as strong push pull mode 10：P1 as high impedance input mode 11：P1 as N type open drain mode

1~0	**P2xM[1:0]** **（x=0~1）**	P2 Mode setting 00：P2 as Quasi-bi mode 01：P2 as strong push pull mode 10：P2 as high impedance input mode 11：P2 as N type open drain mode
7~0	**P3xM[1:0]** **（x=0~7）**	P3 Mode setting 00：P3 as Quasi-bi mode 01：P3 as strong push pull mode 10：P3 as high impedance input mode 11：P3 as N type open drain mode

P1 (90h) P1 Data Register (R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

P2 (A0h) P2 Data Register (R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	P2.1	P2.0
R/W	-	-	-	-	-	-	R/W	R/W
Reset	x	x	x	x	x	x	1	1

P3(B0h) P3 Data Register (R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit No	Symbol	Description
7~0	**P1.x** **（x=0~7）**	P1 Data
1~0	**P2.x** **(x=0,1)**	P2 Data
7~0	**P3.x** **(x=0~7)**	P3 Data

12.3 I/O SHARE

Pin No	Share Function	Description	Control bit name（SFR Address）	Control bit
2	**RST**	**Reset pin**	DISRST	DISRST=0
	P1.0	**GPIO P1.0**	RSTCFG.3(F6h)	DISRST=1
3	**PWM1/P1.1**	PWM1 output	ENPWM1O	ENPWM1O=1
	P1.1	**GPIO P1.1**	PWMCR.2(F8h)	ENPWM1O=0
4	**PWM0**	PWM0 output	ENPWM0O	ENPWM0O=1
	P1.2/T0	**External input of T0** **GPIO P1.2**	PWMCR.0(F8h)	ENPWM0O=0
5	**INT2**	**External INT2**		EA=1and EXIE.2(B3h)=1
	T1/P1.3	**External input of T1**		

		GPIO P1.3		
6	**INT3**	**External INT3**		EA=1and EXIE.3(B3h)=1
	P1.4	**GPIO P1.4**		
7	**INT4**	**External INT4**		EA=1and EXIE.4(B3h)=1
	P1.5	**GPIO P1.5**		
8	**Vref**	**External Vref of ADC**		
	INT5	**INT5**		EA=1and EXIE.7(B3h)=1
	P1.6	**GPIO P1.6**		
9	**INT6**	**External INT6**		EA=1and EXIE.6(B3h)=1
	P1.7	**GPIO P1.7**		
10	**INT7**	**External INT7**		EA=1and EXIE.7(B3h)=1
	P2.0	**GPIO P2.0**		
11	**P2.1 No share**	**P2.1**	no	No
12	**AIN7**	**ADC input channel 7**	RP37U P3ADC.7（B2h）	RP37U=1
	P3.7	**GPIO P3.7**		RP37U=0
13	**AIN6**	**ADC input channel 6**	RP36U P3ADC.6（B2h）	RP36U=1
	P3.6	**GPIO P3.6**		RP36U=0
14	**AIN5**	**ADC input channel 5**	RP35U P3ADC.5（B2h）	RP35U=1
	P3.5	**GPIO P3.5**		RP35U=0
15	**AIN4**	**ADC input channel 4**	RP34U P3ADC.4（B2h）	RP34U=1
	P3.4	**GPIO P3.4**		RP34U=0
16	**AIN3**	**ADC input channel 3**	RP33U P3ADC.3（B2h）	RP33U=1
	P3.3	**GPIO P3.3**		RP33U=0
17	**AIN2**	**ADC input channel 2**	RP32U P3ADC.2（B2h）	RP32U=1
	P3.2	**GPIO P3.2**		RP32U=0
18	**AIN1**	**ADC input channel 1**	RP31U P3ADC.1（B2h）	RP31U=1
	INT1	**External INT1**		RP31U=0 EA=1and EXIE.1(B3h)=1
	P3.1	**GPIO P3.1**		RP31U=0
19	**AIN0**	**ADC input channel 0**	RP30U P3ADC.0（B2h）	RP30U=1
	INT0	**External INT0**		RP30U=0 EA=1and EXIE.0(B3h)=1
	P3.0	**GPIO P3.0**		RP30U=0

13 ANALOG DIGITAL CONVERTER (ADC)

The SC91F72B include a 10-bit SAR Analog to Digital Converter (ADC) with build in reference voltage connected to the V_{DD}, external voltage or internal precious tuned 2.4V. The 8 channel ADC are shared with 1 ADC module; each channel can be programmed to connect with the analog input individually. Only one channel can be available at one time. ADCS signal is available to start convert, and the EOC/ADCIF indicate end of convert. When conversion is completed, the data in AD convert data register will be updated and ADCIF bit in ADCCR register will be set. If ADC Interrupt is enabled, the ADC interrupt will generate.

There are three options for ADC reference voltage:

①internal VDD;

②internal Precious tuned 2.4V;

③external reference voltage from P1.6;

13.1 ADC SFR

ADCCFG (C4h)ADC refrence voltage Configuration Register（R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	VREFS[1:0]	
R/W	-	-	-	-	-	-	R/W	R/W
Reset	x	x	x	x	x	x	0	0

Bit No	Symbol	Description
1~0	**VREFS[1:0]**	**reference voltage selection** 00：internal VDD 01：internal precious tuned 2.4V 10：External reference voltage Pin 11：reversed

P3ADC (B2h) ADC Configuration Register (R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	RP31U	RP36U	RP35U	RP34U	RP33U	RP32U	RP31U	RP30U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit No	Symbol	Description
7~0	**RP3xU** **(x=0~7)**	**ADC Port Configuration** 0：PORT3.x are GPIO 1：PORT3.x are ADC input

ADCCR (C5h)ADC Control Register (R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	ADCEN	ADCKS[1:0]		EOC/ ADCIF	ADCS	ADCIS[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit No	Symbol	Description
7	**ADCEN**	**Turn on ADC** **0**：Power off ADC Modules 1：turn on ADC Modules
6~5	**ADCKS[1:0]**	**ADC Clocks Selector** 00： Fosc 01： Fosc/2 10： Fosc/4

		11： Fosc/6
4	**EOC /ADCIF**	**End Of Conversion / ADC Interrupt Flag** 0：Conversion is not completed 1：Conversion has been completed
3	**ADCS**	**ADC Start** Set this bit to convert ADC once time
2~0	**ADCIS**	**ADC Input Selector** 000：ADC channel AIN0 001：ADC channel AIN1 010：ADC channel AIN2 011：ADC channel AIN3 100：ADC channel AIN4 101：ADC channel AIN5 110：ADC channel AIN6 111：ADC channel AIN7

ADCVH (C6h)ADC Data register High（High 8bit）(R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	ADCV[9:2]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

ADCVL (C7h) ADC Data register Low（Low 2bit）(R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	ADCV[1:0]	
R/W	-	-	-	-	-	-	R/W	R/W
Reset	x	x	x	x	x	x	0	0

Bit No	Symbol	Description
7~0	**ADCV[9:2]**	ADC Data high 8 bit
2~0	**ADCV[1:0]**	ADC Data Low 2 bit

IE (A8h) Interrupt Enable Register(R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	EA	EADC	EPWM	-	ET1	-	ET0	-
R/W	R/W	R/W	R/W	-	R/W	-	R/W	-
Reset	0	0	0	X	0	x	0	x

Bit No	Symbol	Description
6	**EADC**	**ADC interrupt Enable** 0： Disable ADC interrupt 1： Enable ADC interrupt

IP (B8h) Interrupt priority Register(R/W)

Bit No	7	6	5	4	3	2	1	0
Symbol	-	IPADC	IPPWM	-	IPT1	-	IPT0	-
R/W	R/W	R/W	R/W	-	R/W	-	R/W	-
Reset	0	0	0	x	0	x	0	x

Bit No	Symbol	Description
6	**IPADC**	**ADC interrupt Priority** 0：ADC interrupt Priority is Low

		1：ADC interrupt Priority is high

13.2 ADC CONVERSION STEPS

ADC Conversion Steps are as follows:

① Select the ADC input channel (set IO used as ADC input)；
② Select the ADC reference voltage and ADC clock；
③ Enable the ADCEN；
④ Configure the ADCIS；
⑤ Set ADCS，the conversion start；
⑥When EOC/ADCIF=1，If EADC=1,，ADC interrupt occurs，user clear the EOC/ADCIF ；
⑦ Read the ADC Data from ADCVH and ADCVL, ADCVH read first and then ADCVL；
⑧ Repeat the Steps from 5 to 7, user can complete conversion once a time。

14 IAP OPERATION

The 256B ROM allows In-Application Programming (IAP). User can write dynamic data to the internal Flash as EEPROM。

SC91F72B currently only supports IAP in 8MHz frequency mode.

14.1 IAP SFR

IAP SFR Description：

symbol	address	description	7	6	5	4	3	2	1	0	Reset value
IAPKEY	**EAH**	IAP key	IAPKEY[7:0]								00000000b
IAPADL	**ECH**	IAP address low	IAPADR[7:0]								00000000b
IAPDAT	**EDH**	IAP Data(write)	IAPDAT[7:0]								00000000b
IAPCTL	**EEH**	IAP command	-	-	-	-	PAYTIMES [1:0]		CMD[1:0]		xxxx0000b

IAPKEY（EAH） IAP key（R/W）

Bit No	7	6	5	4	3	2	1	0
Symbol	IAPKEY[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit No	Symbol	Description
7~0	**IAPKEY[7:0]**	Enable IAP function and set IAP operating time limited Write a value n， means：①enable IAP function；②In n system clock, the MCU does not receive IAP write command, then the IAP function will be re-closed;

IAPADL（ECH）IAP Write address Low 8bit

Bit No	7	6	5	4	3	2	1	0
Symbol	IAPADR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit No	Symbol	Description
7~0	**IAPADR[7:0]**	IAP write address low 8bit

IAPDAT（EDH）IAP Data

Bit No	7	6	5	4	3	2	1	0
Symbol	IAPDAT[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit No	Symbol	Description
7~0	**IAPDAT**	IAP write data

IAPCTL（EEH）IAP control

Bit No	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PAYTIMES[1:0]		CMD[1:0]	
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset	X	x	x	x	0	0	0	0

Bit No	Symbol	Description
3~2	**PAYTIMES[1:0]**	In IAP function, CPU Hold Time setting（only in 8MHz system clock） 00： CPU HOLD TIME about 8ms@8MHz 01： CPU HOLD TIME about 4ms@8MHz 10： CPU HOLD TIME about 2ms@8MHz 11： reversed Note: the CPU only hold PC, the other functional modules will continue to work. Interrupt flag will be saved, and will respond after the end of the Hold interrupt. If the same interrupt occurs several times, the system can retain and respond to the last.
1~0	**CMD[1:0]**	IAP write command 00 : reversed 01 : reversed 10 : write 11 : reversed

14.2 IAP OPERATION PROCESS

The operation process of SC91F72B IAP is shown as below:

① Write IAPDAT[7:0]（prepare the data to write）；

② write {IAPADR[11:8], IAPADR[7:0]}（prepare the address of IAP operation，IAPADR[11:8] is always 1）；

③ write IAPKEY[7:0] to value *n*（Open IAP，please give writing command of IAP in n system Clocks）；

④ write IAPCTL[3:0]（setting CPU Hold time，write CMD[1:0] to 1、0，CPU Hold and start to IAP operation）；

⑤ IAP writing completed, CPU continue others operations；

Note：User can read the Data of IAP by using MOVC instruction.

14.3 IAP DEMO PROGRAM

```
#include ”intrins.h”
unsigned char  code *POINT=0x0f00;
unsigned char  DATA1,ADDR1;
```

IAP writing operation , C Demo program：

```
IAPDAT=DATA1;          //send DATA1 to IAP Data register
IAPADL=ADDR1;          //write address ADDR1
IAPKEY=0xf0;           //you can change this value
                       // Pay special attention to the value when you use interrupt
IAPCTL=0x06;           // IAP  command，4 ms@8M
_nop_();               // wait (need at least 1_nop_())
```

```
_nop_();
_nop_();
_nop_();
```

IAP reading operation, C Demo program:

```
DATA1=*(POINT+ADDR1);        //read  Data of ADDR1  to  DATA1
```

IAP reading operation, Assembly Demoprogram:

```
MOV DPTR，#0f00H;            //DPTR initial value
MOV A, ADDR1;                //address to A
MOVC A, @A+DPTR;             //read the value of  ADDR1 to A
```

15 ELECTRICAL CHARACTERISTICS

15.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	UNIT
VDD/VSS	Operating Voltage	-0.3	5.5	V
Voltage ON any Pin	Input/Output Voltage	-0.3	VDD+0.3	V
TA	Operating Temperature	-40	85	℃
TSTG	Storage Temperature	-55	125	℃

15.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	UNIT
VDD	Operating Voltage	3.6	5.5	V
TA	Operating Temperature	-40	85	℃

15.3 DC ELECTRICAL CHARACTERISTICS (VDD = 3.6V ~ 5.5V, TA = 25℃)

Symbol	Parameter	Min	Type	Max	Unit	condition
current						
Iop1	operating current1		4.7	10	mA	IRC=16MHz VDD=5V
Iop2	operating current2		3.7	10	mA	IRC=8MHz VDD=5V
Ipd	STOP current （Power Down mode）	-	0.1	1	uA	IRC=16MHz VDD=5V all IO in quasi-bi mode
IO characteristics						
VIH	Input High Voltage	0.7VDD	-	VDD+0.5	V	
VIL	Input Low Voltage	-0.5	-	0.3VDD	V	
VIH,RSTN	Input High Voltage(RSTN Pin)	2.0		VDD	V	
VIL,RSTN	Input Low Voltage (RSTN Pin)	-0.2		1.5	V	
IOL1	Sink current P1/P2/P3		20		mA	VDD=5V Vpin=0.8V
IOL2	Sink current P1/P2/P3		10		mA	VDD=5V Vpin=0.4V
IOH1	Pull-up current（Quasi-Bi Mode）P1/P2/P3		50		uA	VDD=5V Vpin=4.7V
IOH2	Pull-up current（Push-pull mode）P1/P2/P3		10		mA	VDD=5V Vpin=4.3V
IOH3	Pull-up current（Push-pull mode）P1/P2/P3		5		mA	VDD=5V Vpin=4.7V
Internal Precious 2.4V						
VDD2.4	internal 2.4V	2.37	2.40	2.45	V	TA=-40~85℃ VDD=5V

15.4 AC ELECTRICAL CHARACTERISTICS (VDD = 3.6V ~ 5.5V, TA = 25℃)

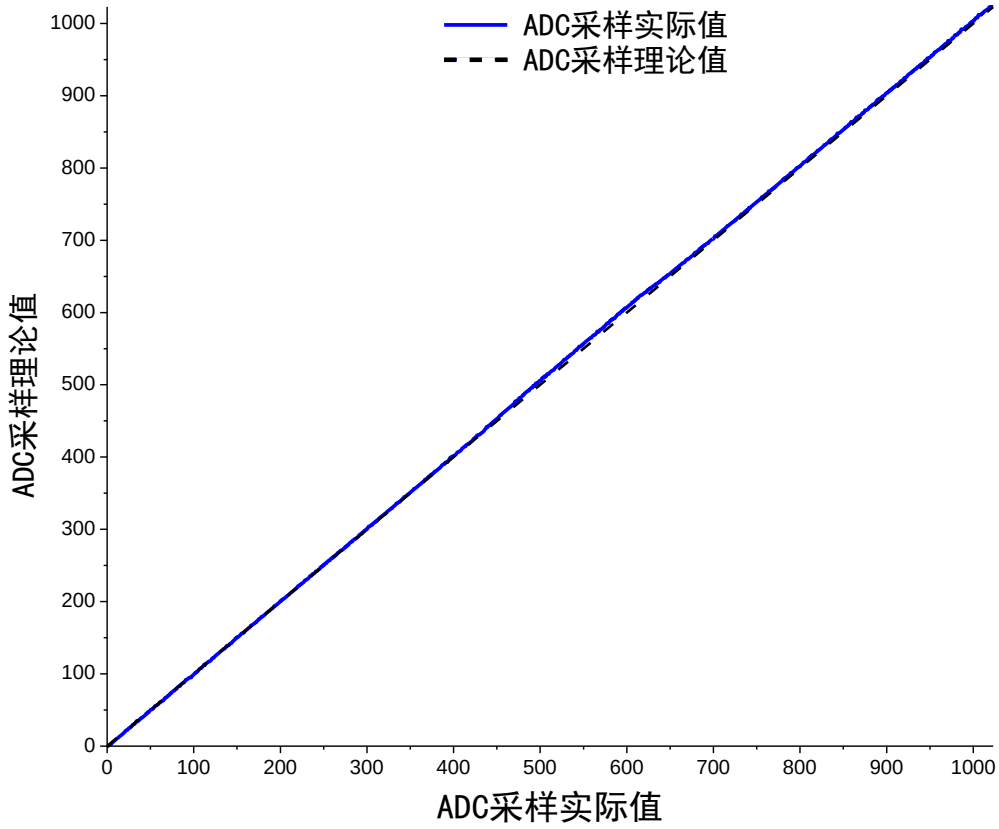
Symbol	Parameter	Min	Max	UNIT	Symbol	Parameter
Tosc	Oscillator start time		5	20	us	IRC=16MHz VDD=5V
Treset	Reset pulse width	64			us	Low active
FIRC	Frequency Stability(RC)	15.70	16	16.30	MHz	VDD=5V TA=-40~85 ℃

15.5 ADC ELECTRICAL CHARACTERISTICS (TA = 25℃)

Symbol	Parameter	Min	Type	Max	Unit	condition
VAD	ADC supply Voltage	3.6	5.0	5.5V	V	
NR	Resolution		10		bit	GND≤VAIN≤VREF
VAIN	ADC Input voltage	GND		VDD	V	
RAIN	ADC Input Resistor	5			MΩ	VIN=5V
Rref	Vref input resistor		13.5		KΩ	
ZAIN	Recommended impedance of analog voltage source			10	KΩ	
IADC	ADC conversion current		1.0		mA	ADC ON VDD=5V
DNL	Differential linearity error		±1	±1.5	LSB	VDD=5V
INL	Integral linearity error		±3	±5	LSB	VDD=5V
EAD	Total Absolute error		±3	±5	LSB	VDD=5V
TADC	Total conversion Time	90 ADC Clocks				

15.6 ADC ACTUAL TEST CURVE

ADC actual test curve is as follow：（Condition：5V, ADC CLK Fosc/6, Connect 100pF C between the ADC input pin with VSS）

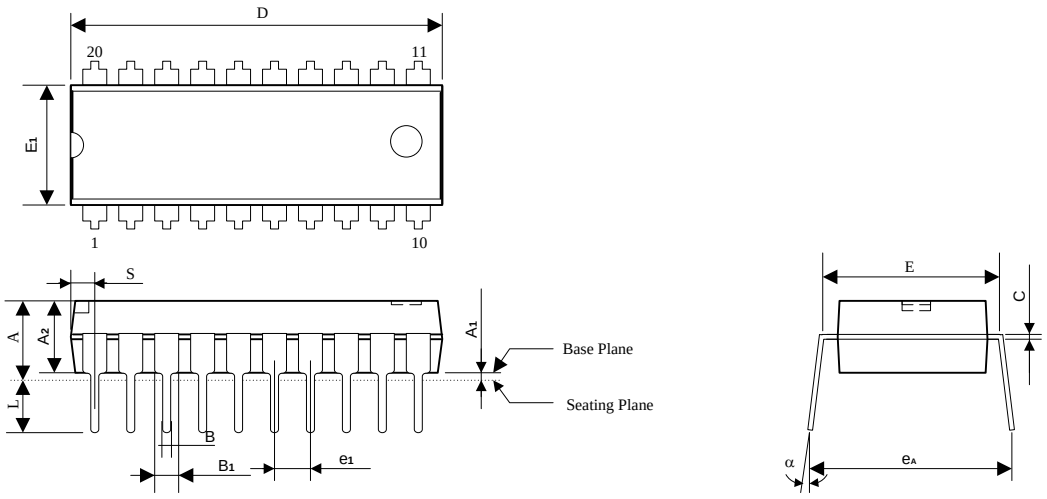


16 ORDERING INFORMATION

PRODUCT NO	PKG	PACKING
SC91F72BD20U	DIP20	TUBE
SC91F72BM20U	SOP20	TUBE
SC91F72BM16U	SOP16L	TUBE

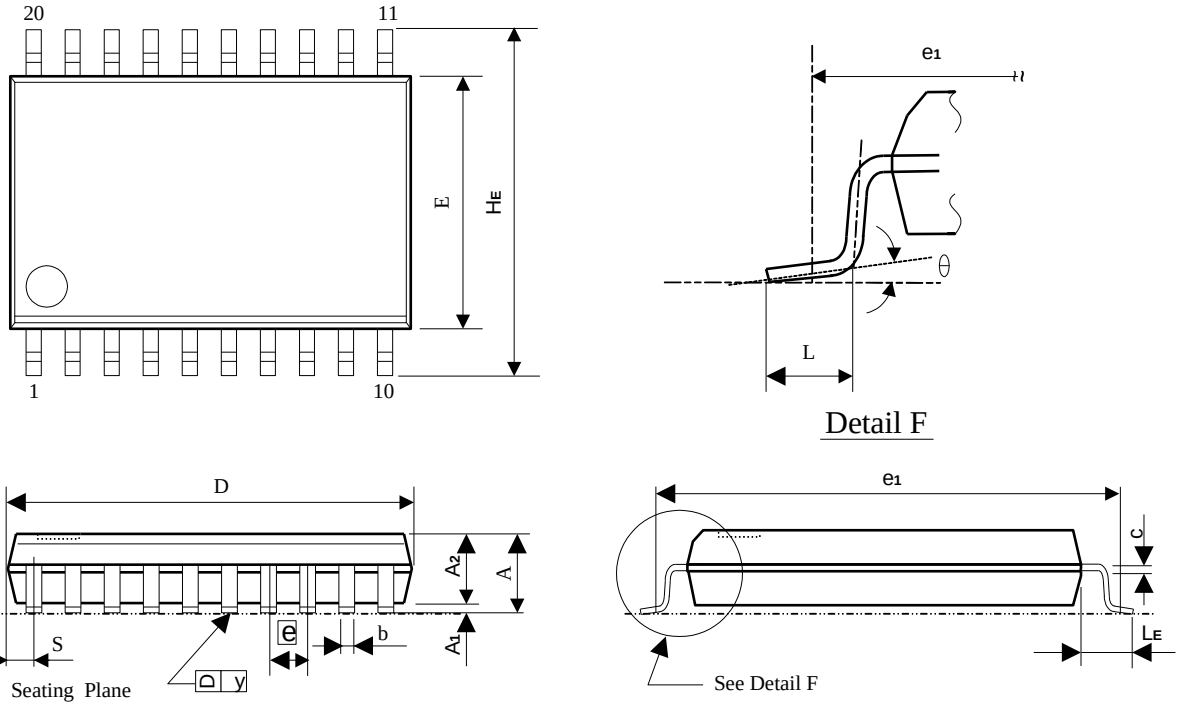
17 PACKAGE INFORMATION

P-DIP 20L （300mil）outline dimensions unit: mm



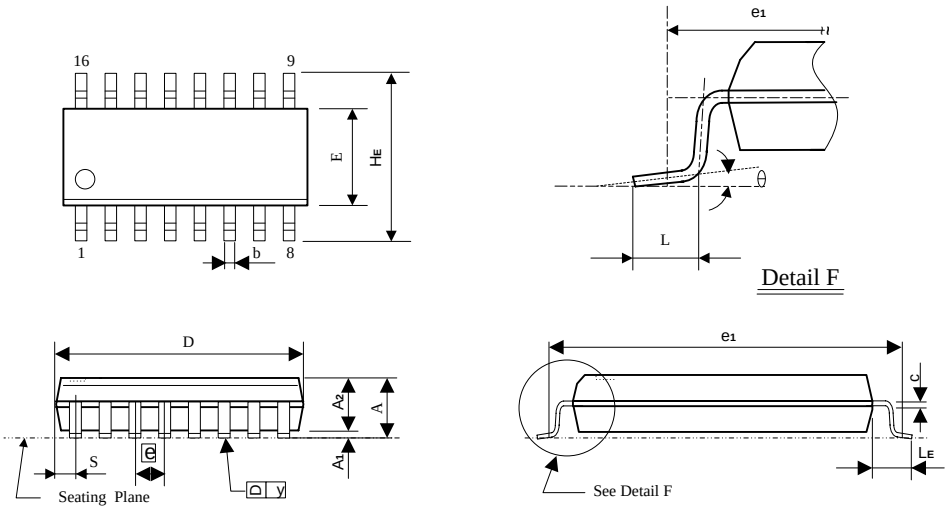
Symbol	mm		
	Min	Type	Max
A	3.60	3.80	4.00
A1	0.51	-	-
A2	3.20	3.30	3.40
B	0.44	-	0.53
B1	1.52(BSC)		
C	0.25	-	0.31
D	25.70	25.90	26.10
E1	6.35	6.55	6.75
e1	2.54(BSC)		
L	3.00	-	-
eA	7.62	-	9.30

SOP 20L (300mil) outline dimensions **unit: mm**



Symbol	mm		
	Min	Type	Max
A	2.465	2.515	2.565
A1	0.100	0.150	0.200
A2	2.100	2.300	2.500
b	0.356	0.406	0.456
C	0.254(BSC)		
D	12.500	12.700	12.900
E	7.400	7.450	7.500
HE	10.206	10.306	10.406
e	1.27(BSC)		
L	0.800	0.864	0.900
LE	1.303	1.403	1.503
θ	0°	-	10°
S	0.660(BSC)		

SOP 16L (150mil) outline dimensions **unit: mm**



Symbol	mm		
	Min	Type	Max
A	-	-	1.75
A_1	0.05	-	0.225
A_2	1.30	1.40	1.50
b	0.39	-	0.48
C	0.21	-	0.26
D	9.70	9.90	10.10
E	3.70	3.90	4.10
H_E	5.80	6.00	6.20
e	1.27(BSC)		
L	0.50	-	0.80
L_E	1.05(BSC)		
θ	0°	-	8°

18 DATASHEET CHANGE NOTICE

Version	content	Date
V1.2	Update product No	Aug,2014
V1.1	Update IAP demo program Update DIP20,SOP20,SOP16L outline dimensions	May,2014
V1.0	Original	Feb, 2012