

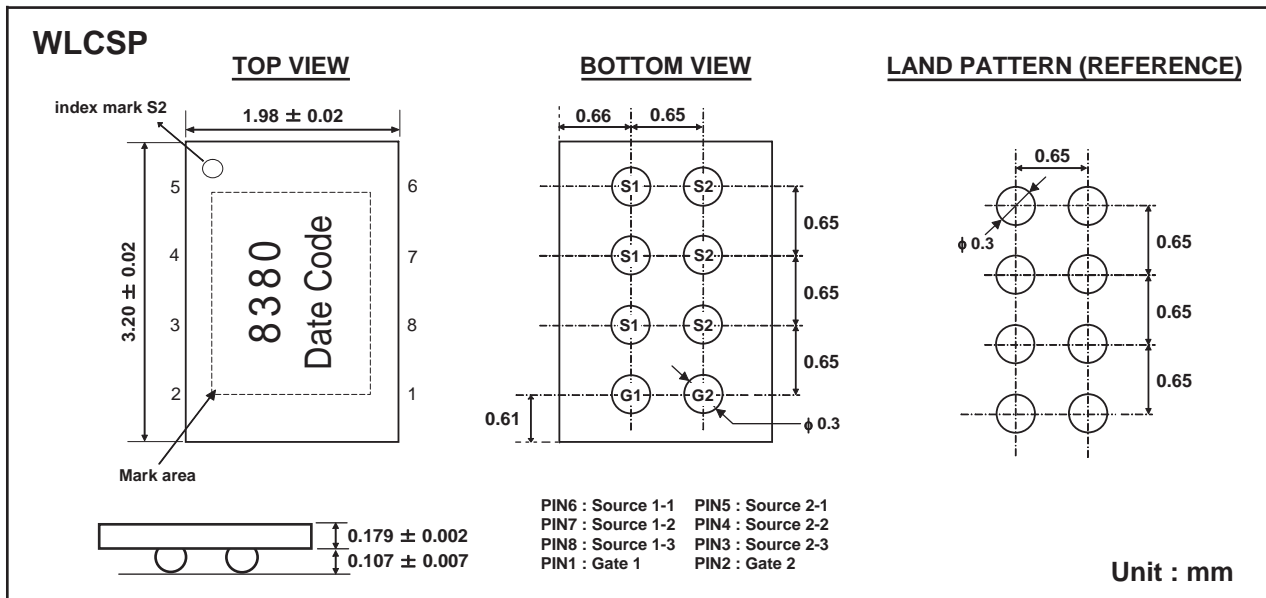


Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V _{SSS}	I _S	R _{SS(ON)} (mΩ) Max
30V	9A	8 @ V _{GS} =10V
		13 @ V _{GS} =4.5V

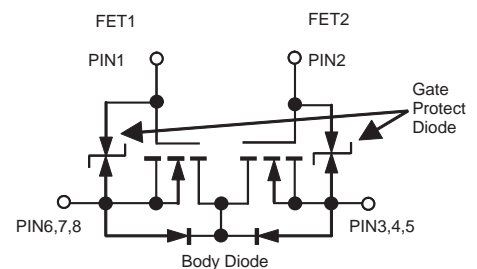
FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- Wafer level CSP.
- ESD Protected.



ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

Symbol	Parameter	Limit	Units
V _{SSS}	Source-Source Voltage	30	V
V _{GSS}	Gate-Source Voltage	±20	V
I _S	Source Current-Continuous ^a	9	A
I _{SP}	-Pulsed ^b	90	A
P _T	Total Power Dissipation ^a	0.4	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C



PIN6 : Source 1-1 PIN5 : Source 2-1
 PIN7 : Source 1-2 PIN4 : Source 2-2
 PIN8 : Source 1-3 PIN3 : Source 2-3
 PIN1 : Gate 1 PIN2 : Gate 2

SC8380

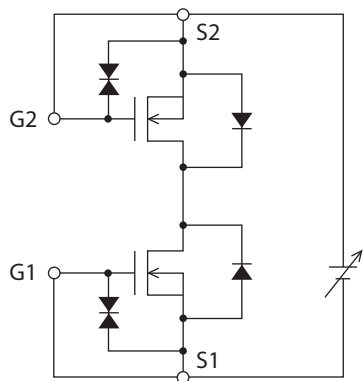
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ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

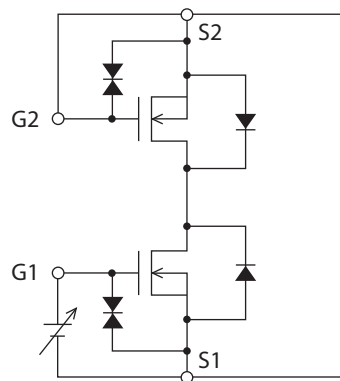
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{SSS}	Source-Source Breakdown Voltage	V _{GS} =0V , I _S =250uA	30			V
I _{SSS}	Zero Gate Voltage Source Current	V _{SS} =30V , V _{GS} =0V			1	uA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±16V , V _{SS} =0V			±10	uA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{SS} =V _{GS} , I _S =1mA	1.0	1.5	2.5	V
R _{SS(ON)}	Source-Source On-State Resistance	V _{GS} =10V , I _S =4.5A		7	8	m ohm
		V _{GS} =4.5V , I _S =4.5A		10	13	m ohm
DYNAMIC CHARACTERISTICS ^c						
C _{ISS}	Input Capacitance	V _{SS} =10V, V _{GS} =0V f=1.0MHz		2870		pF
C _{OSS}	Output Capacitance			410		pF
C _{RSS}	Reverse Transfer Capacitance			154		pF
SWITCHING CHARACTERISTICS ^c						
t _{D(ON)}	Turn-On Delay Time	V _{DD} =15V I _S =4.5A V _{GS} =10V		42		ns
t _r	Rise Time			168		ns
t _{D(OFF)}	Turn-Off Delay Time			538		ns
t _f	Fall Time			396		ns
Q _g	Total Gate Charge	V _{DD} =15V, I _S =9A, V _{GS} =4.5V		22.8		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V _{FSS}	Diode Forward Voltage	V _{GS} =0V, I _S =4.5A		0.8	1.2	V
Note						
a. Mounted on FR4 board of 25.4mm x 25.4mm x 1.0mm.						
b. Pulse Test: Pulse Width < 10us, Duty Cycle < 1%.						
c. Guaranteed by design, not subject to production testing.						

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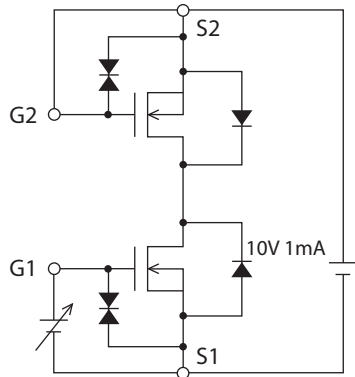
V_{SSS} / I_{SSS}



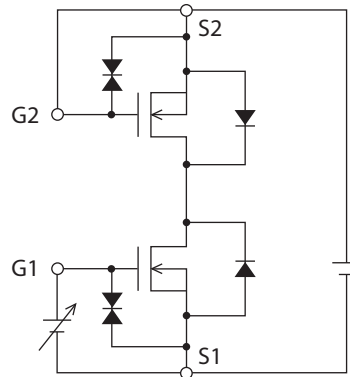
$I_{GSS} (+) / (-)$



$V_{GS} \text{ (off)}$



$|y_{fs}|$

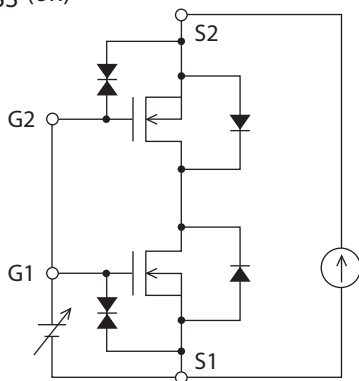


* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

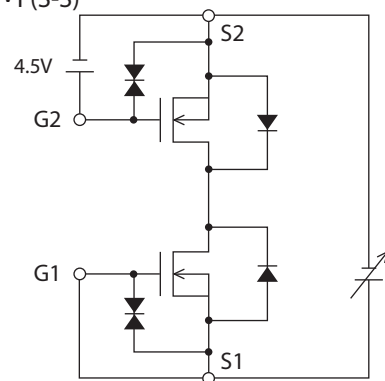
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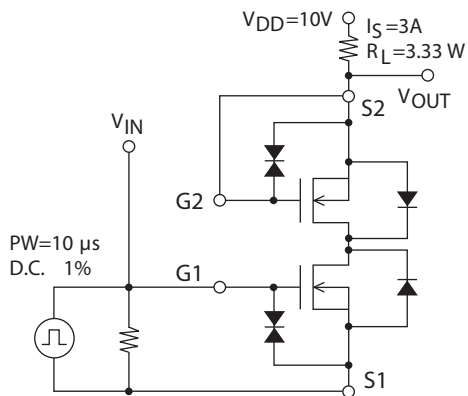
$R_{SS} \text{ (on)}$



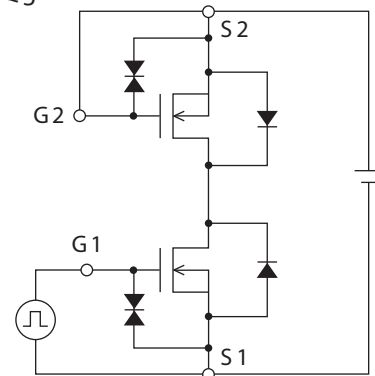
$V_F(S-S)$



$t_d(\text{on}), t_r, t_d(\text{off}), t_f$



Q_g



* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

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TOP MARKING DEFINITION

