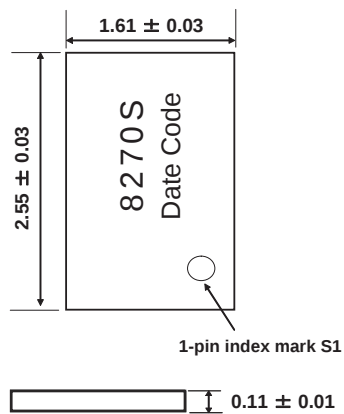
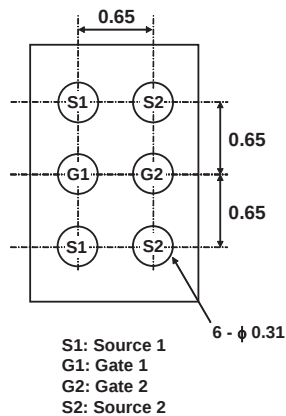
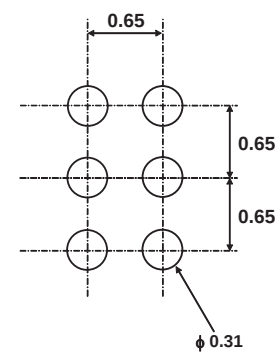


**Dual N-Channel Enhancement Mode Field Effect Transistor****PRODUCT SUMMARY**

V _{SSS}	I _S	R _{SS(ON)} (mΩ) Max
24V	9A	10.2 @ V _{GS} =4.5V
		10.5 @ V _{GS} =4.0V
		11.5 @ V _{GS} =3.8V
		12.0 @ V _{GS} =3.1V
		14.0 @ V _{GS} =2.5V

FEATURES

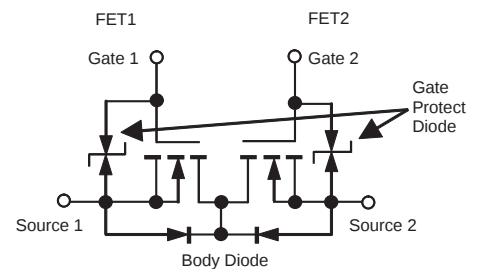
- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- Wafer level CSP.
- ESD Protected.

WLCSP**TOP VIEW****BOTTOM VIEW****LAND PATTERN (REFERENCE)**

Unit : mm

ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

Symbol	Parameter	Limit	Units
V _{SSS}	Source-Source Voltage	24	V
V _{GSS}	Gate-Source Voltage	±12	V
I _S	Source Current-Continuous ^a	9	A
I _{SP}	-Pulsed ^b	90	A
P _T	Total Power Dissipation ^a	1.3	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C



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ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

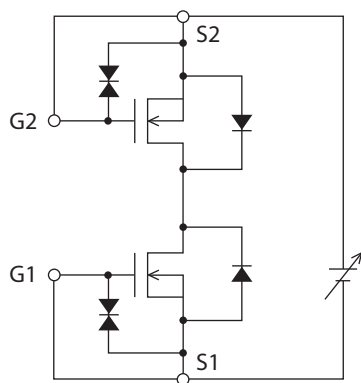
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{SSS}	Source-Source Breakdown Voltage	V _{GS} =0V, I _S =250uA	24			V
I _{SSS}	Zero Gate Voltage Source Current	V _{SS} =24V, V _{GS} =0V			1	uA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±8V, V _{SS} =0V			±1	uA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{SS} =V _{GS} , I _S =1mA	0.5	0.8	1.5	V
R _{SS(ON)}	Source-Source On-State Resistance	V _{GS} =4.5V, I _S =2A	6.0	8.2	10.2	m ohm
		V _{GS} =4.0V, I _S =2A	6.2	8.5	10.5	m ohm
		V _{GS} =3.8V, I _S =2A	6.6	9.0	11.5	m ohm
		V _{GS} =3.1V, I _S =2A	7.0	9.5	12.0	m ohm
		V _{GS} =2.5V, I _S =2A	8.0	11.0	14.0	m ohm
g _{FS}	Forward Transconductance	V _{SS} =5V, I _S =2A		14		S
SWITCHING CHARACTERISTICS ^c						
t _{D(ON)}	Turn-On Delay Time	V _{DD} =24V I _S =2A V _{GS} =4.0V R _{GEN} =6 ohm		430		ns
t _r	Rise Time			1700		ns
t _{D(OFF)}	Turn-Off Delay Time			5390		ns
t _f	Fall Time			3970		ns
Q _g	Total Gate Charge	V _{DD} =24V, I _S =4A, V _{G1S1} =4.0V		23		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V _{FSS}	Diode Forward Voltage	V _{GS} =0V, I _S =2A		0.77	1.2	V
Note a. Mounted on FR4 board of 25.4mm x 25.4mm x 1.6mm. b. Pulse Test: Pulse Width ≤ 10us, Duty Cycle ≤ 1%. c. Guaranteed by design, not subject to production testing.						

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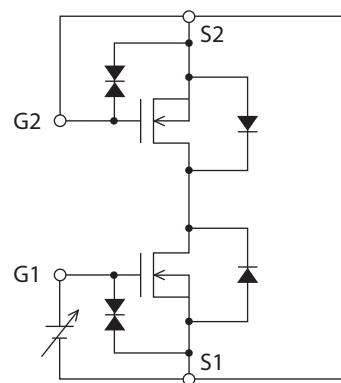
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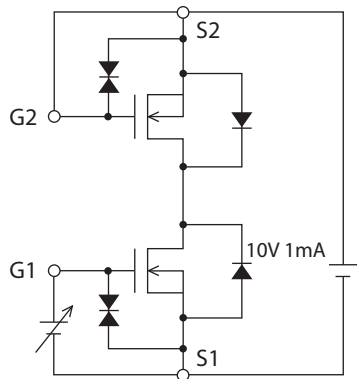
V_{SSS} / I_{SSS}



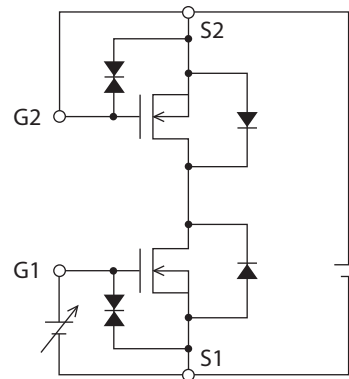
$I_{GSS} (+) / (-)$



$V_{GS} \text{ (off)}$



$|y_{fs}|$



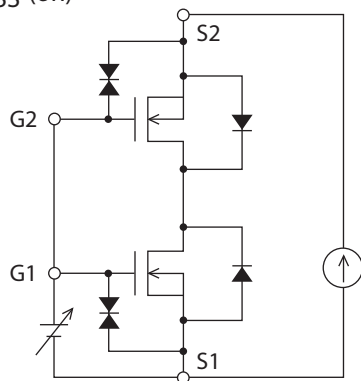
* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

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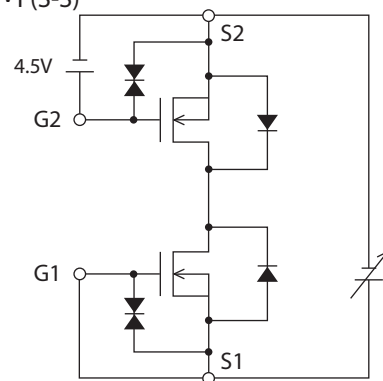
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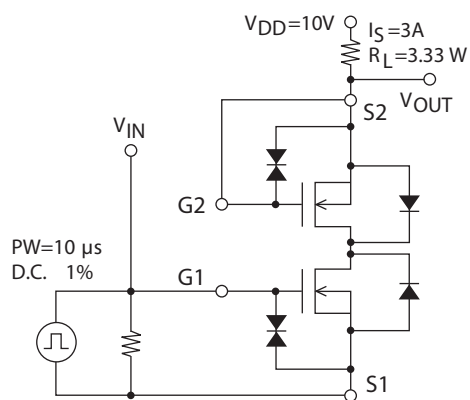
$R_{SS} \text{ (on)}$



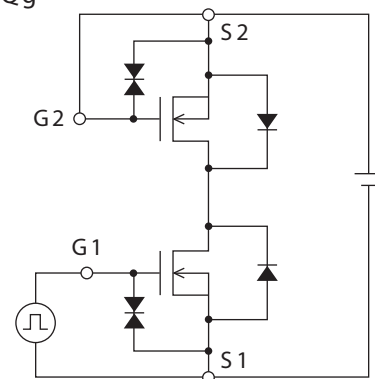
$V_F(S-S)$



$t_d(\text{on}), t_r, t_d(\text{off}), t_f$



Q_g

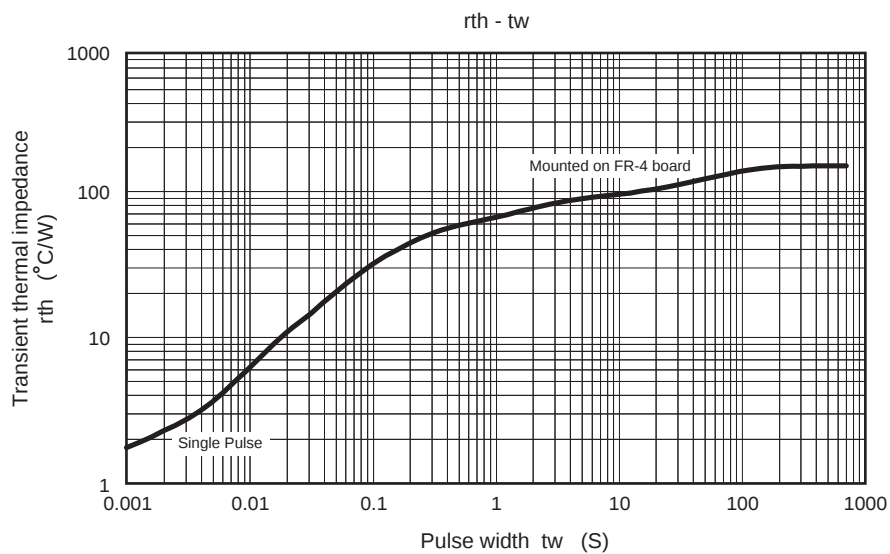
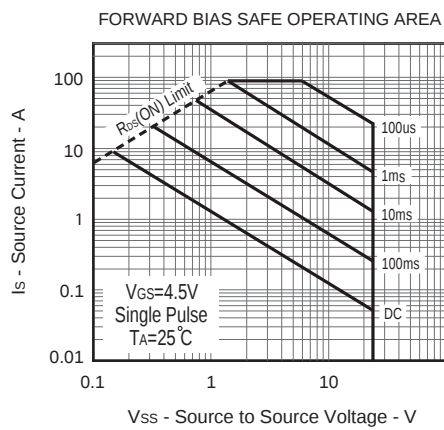
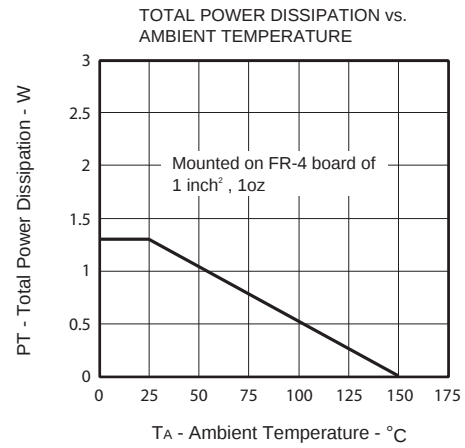
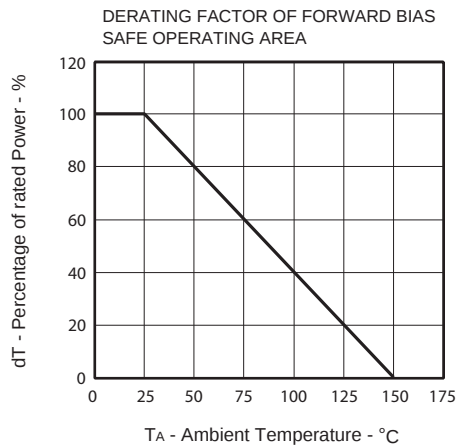


* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

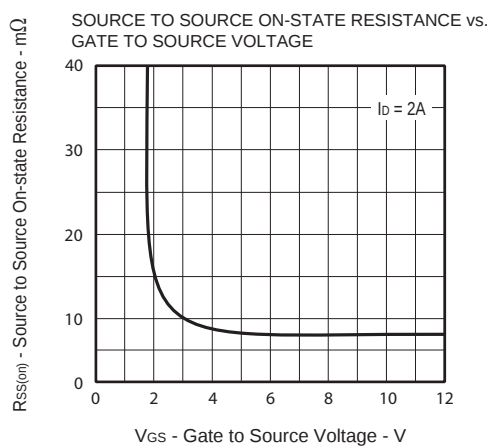
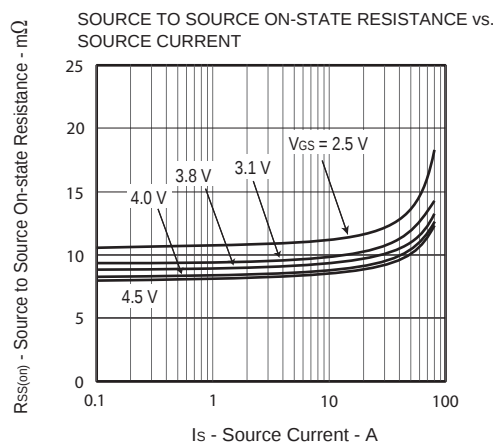
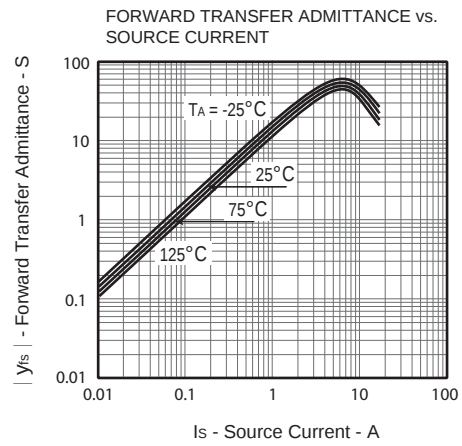
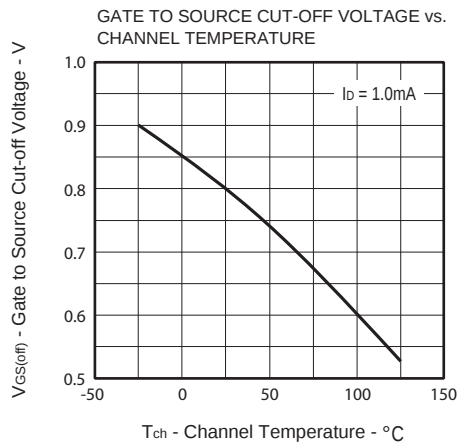
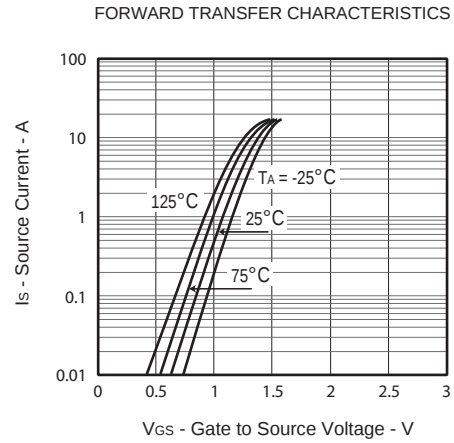
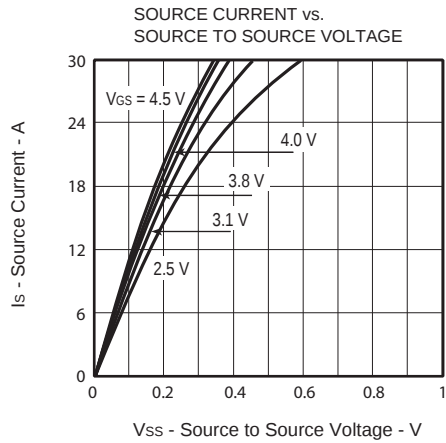
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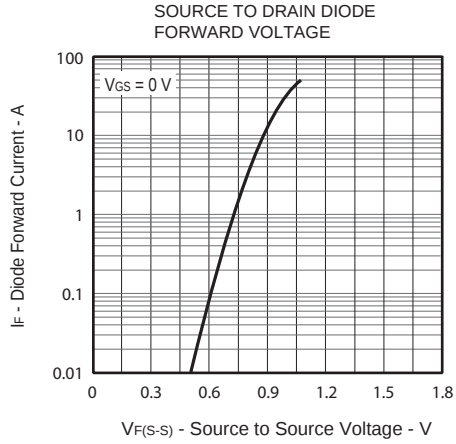
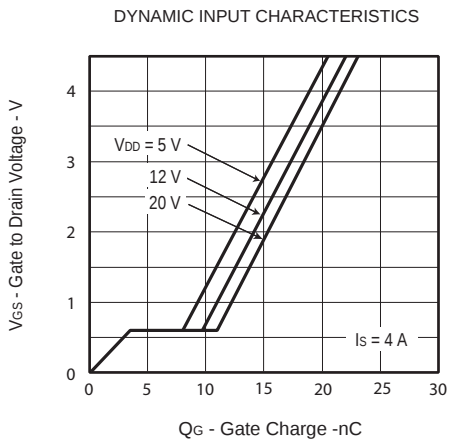
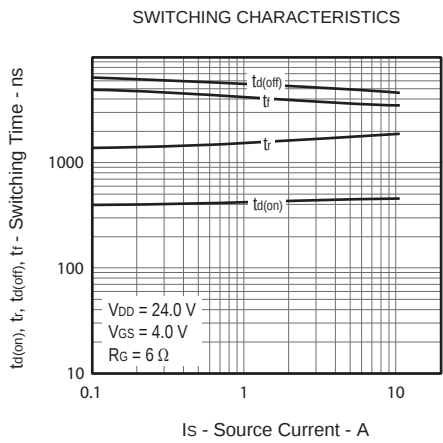
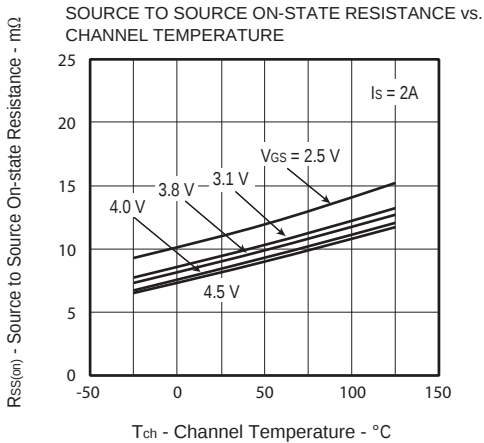
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TOP MARKING DEFINITION

