PROGRAMMABLE INFRARED REMOTE TRANSMITTER WITH BUILT-IN TRANSISTOR

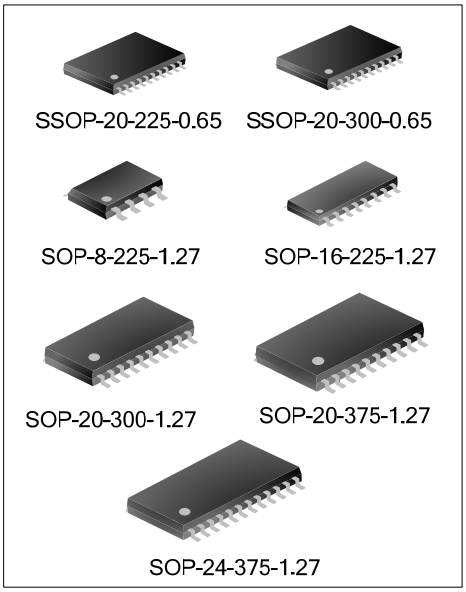
DESCRIPTION

SC73P2602 is SC73 core based programmable remote transmitter (4-bit MCU) with infrared transmitting transistor and built-in 2K OTP program memory supporting in-system program (ISP) which can optimize the stock control.

Due to the infrared transmitting transistor embedded, few periphery components are needed and the cost is reduced.

And the quick mask function that SC73P2602 supported can meet the mass production delivery requirements as soon as possible due to its mask cycle is 2~3 weeks less than the traditional mask cycle.

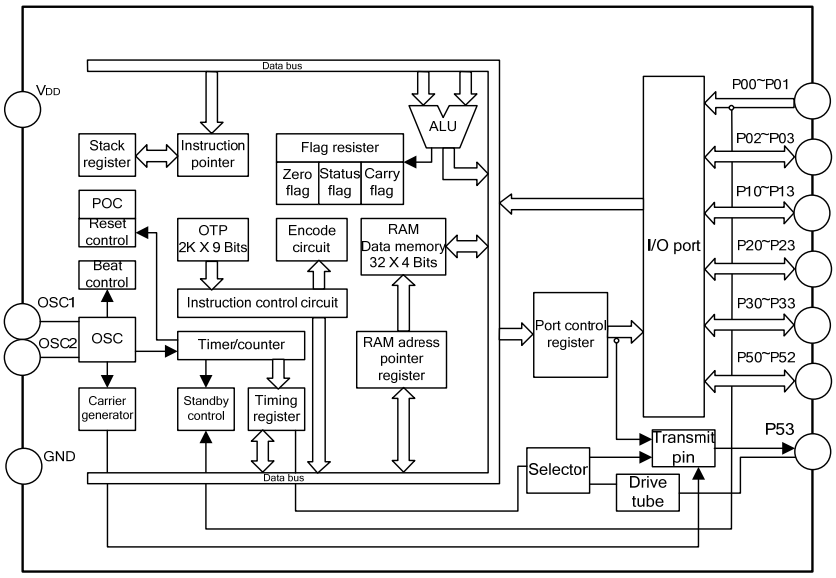
SC73P2602 is available in several packages and pin to pin compatible with all the products of SC73C16 and SC73P16 series.



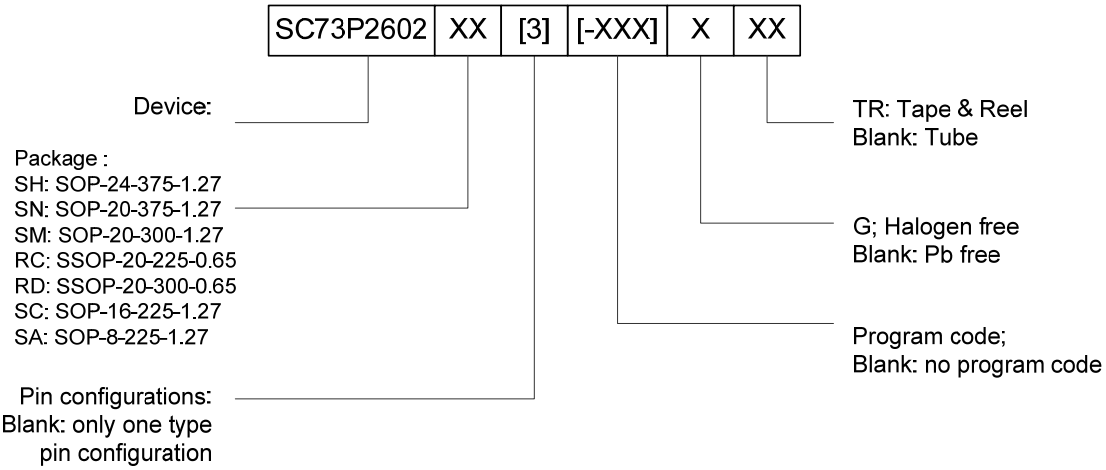
FEATURES

- SC73 core.
- 2K×9 bit OTP and 32×4 bit RAM
- Built-in infrared transmitting transistor: IOL = 350mA.
- Support external infrared transmitting transistor.
- Internal carrier generator.
- Internal power-on clear circuit (POC).
- Internal watchdog timer (WDT).
- 3-level program stack.
- Support low voltages detect (LVD).
- Supports In-System Programming (ISP).
- Oscillator frequency: FOSC=4MHz (Typ.).
- System clock: FMAIN= FOSC /8.
- Instruction period: 5/ FMAIN.
- Operating voltage: 1.8V~3.6V, quiescent current is no higher than 1μA.

BLOCK DIAGRAM



ORDERING INFORMATION



Part No.	I/O	Package	Marking	Material	Packing type
SC73P2602SH1	18	SOP-24-375-1.27	SC73P2602SH1	Pb free	Tube
SC73P2602SN1	15	SOP-20-375-1.27	SC73P2602SN1	Pb free	Tube
SC73P2602SM2	15	SOP-20-300-1.27	SC73P2602SM2	Pb free	Tube
SC73P2602SN2	15	SOP-20-375-1.27	SC73P2602SN2	Pb free	Tube
SC73P2602RC2	15	SSOP-20-225-0.65	SC73P2602RC2	Pb free	Tube
SC73P2602RD2	15	SSOP-20-300-0.65	SC73P2602RD2	Pb free	Tube
SC73P2602SM3	15	SOP-20-300-1.27	SC73P2602SM3	Pb free	Tube
SC73P2602SN3	15	SOP-20-375-1.27	SC73P2602SN3	Pb free	Tube
SC73P2602RC3	15	SSOP-20-225-0.65	SC73P2602RC3	Pb free	Tube
SC73P2602RD3	15	SSOP-20-300-0.65	SC73P2602RD3	Pb free	Tube
SC73P2602SC1	11	SOP-16-225-1.27	SC73P2602SC1	Pb free	Tube
SC73P2602SC2	11	SOP-16-225-1.27	SC73P2602SC2	Pb free	Tube
SC73P2602SC3	11	SOP-16-225-1.27	SC73P2602SC3	Pb free	Tube
SC73P2602SA	4	SOP-8-225-1.27	SC73P2602SA	Pb free	Tube
SC73P2602SH1TR	18	SOP-24-375-1.27	SC73P2602SH1	Pb free	Tape & Reel
SC73P2602SN1TR	15	SOP-20-375-1.27	SC73P2602SN1	Pb free	Tape & Reel
SC73P2602SM2TR	15	SOP-20-300-1.27	SC73P2602SM2	Pb free	Tape & Reel
SC73P2602SN2TR	15	SOP-20-375-1.27	SC73P2602SN2	Pb free	Tape & Reel
SC73P2602RC2TR	15	SSOP-20-225-0.65	SC73P2602RC2	Pb free	Tape & Reel
SC73P2602RD2TR	15	SSOP-20-300-0.65	SC73P2602RD2	Pb free	Tape & Reel
SC73P2602SM3TR	15	SOP-20-300-1.27	SC73P2602SM3	Pb free	Tape & Reel
SC73P2602SN3TR	15	SOP-20-375-1.27	SC73P2602SN3	Pb free	Tape & Reel
SC73P2602RC3TR	15	SSOP-20-225-0.65	SC73P2602RC3	Pb free	Tape & Reel
SC73P2602RD3TR	15	SSOP-20-300-0.65	SC73P2602RD3	Pb free	Tape & Reel
SC73P2602SC1TR	11	SOP-16-225-1.27	SC73P2602SC1	Pb free	Tape & Reel

Part No.	I/O	Package	Marking	Material	Packing type
SC73P2602SC2TR	11	SOP-16-225-1.27	SC73P2602SC2	Pb free	Tape & Reel
SC73P2602SC3TR	11	SOP-16-225-1.27	SC73P2602SC3	Pb free	Tape & Reel
SC73P2602SATR	4	SOP-8-225-1.27	SC73P2602SA	Pb free	Tape & Reel

ABSOLUTE MAXIMUM RATINGS

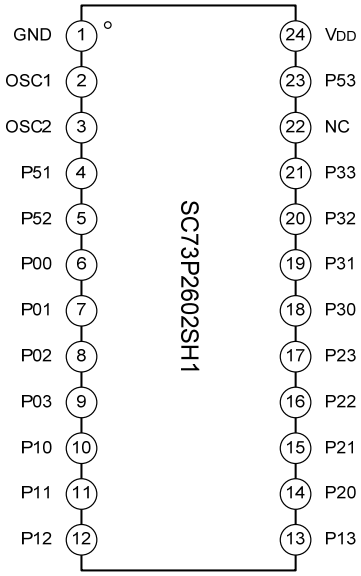
Characteristics	Symbol	Value	Units
Supply Voltage	V_{DD}	-0.3 ~ +4.0	V
Input Voltage	V_I	-0.3 ~ V_{DD}+0.3	V
Storage Temperature	T_{STG}	-65 ~ +125	°C
Operating Temperature	T_{OPR}	-20 ~ +70	°C

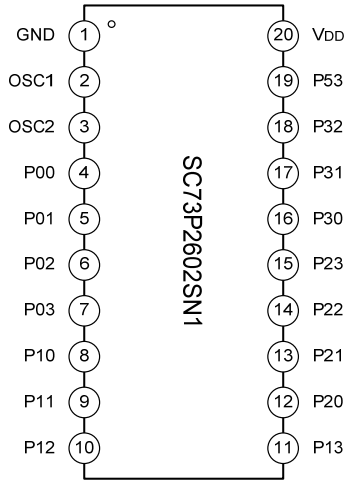
DC ELECTRICAL CHARACTERISTICS (unless otherwise specified, V_{DD}=3V, T_{amb}=25°C)

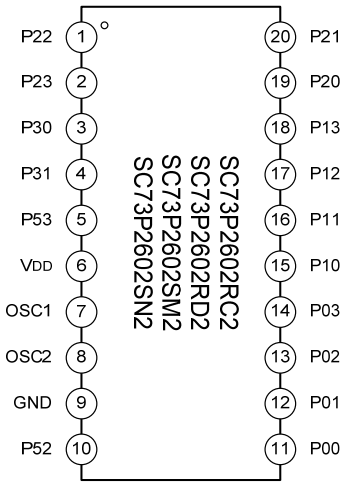
Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Units.
Operating Voltage	V_{DD}	-		1.8	-	3.6	V
Low-Voltage Reset	V_{LVR}	-		-	1.55	-	V
Low-Voltage Detect	V_{LVD}	-		-	1.7	-	V
Operating Current	I_{DD}	Operating mode: F_{OSC}=4MHz	V_{DD}=3.6V	-	3.0	-	mA
			V_{DD}=3.0V	-	2.0	-	
			V_{DD}=1.8V	-	0.3	-	
		Stop mode (oscillator is off)		-	-	1	μA
Oscillator Frequency	F_{OSC}	-		2	4	6	MHz
Oscillator Voltage	V_{OSC}	-		-	1.35	-	V
Input High Voltage	V_{IH}	-		0.7V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	-		0	-	0.3V_{DD}	
Output High Current	I_{OH}	V_{OH}=2.7V	P53	-	9.5	-	mA
			P02~P03 P1, P2, P3 P50~P52	-	0.6	-	
Output Low Current	I_{OL}	V_{OL}=0.3V	P53	-	-19	-	mA
			P53(N-MOS open drain)	-	-350	-	
			P02~P03 P1, P2, P3 P50~P52	-	-5.5	-	

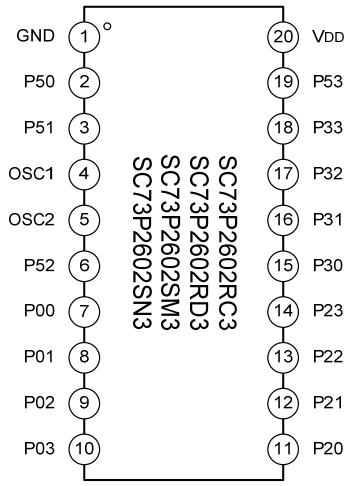
Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Units.
Pull-Up Resistor	RPU	VDD=3.6V	P00	-	50	-	kΩ
			P01~P03 P1, P2, P3 P50~P52	-	150	-	
		VDD=3.0V	P00	-	100	-	
			P01~P03 P1, P2, P3 P50~P52	-	220	-	
		VDD=1.8V	P00	-	600	-	
			P01~P03 P1, P2, P3 P50~P52	-	650	-	

PIN CONFIGURATIONS

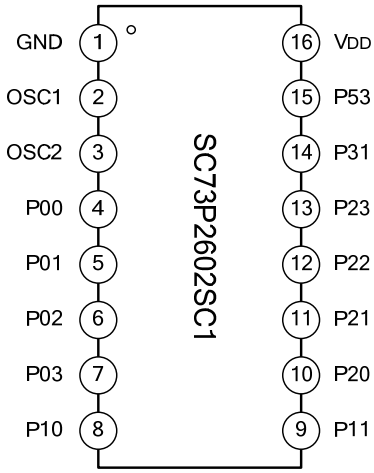


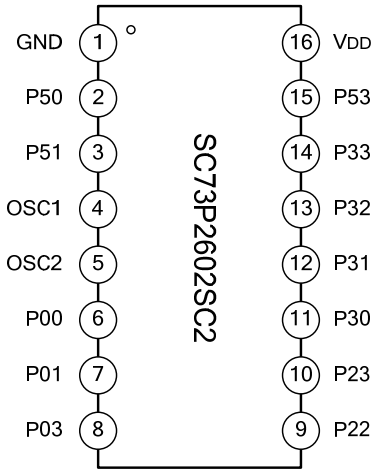


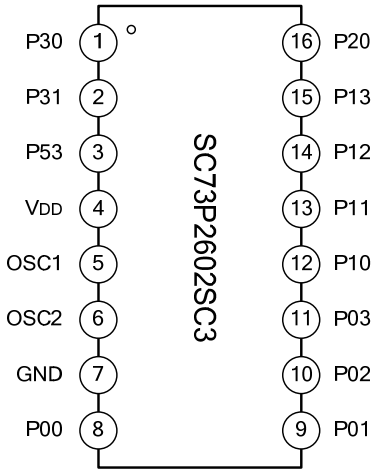


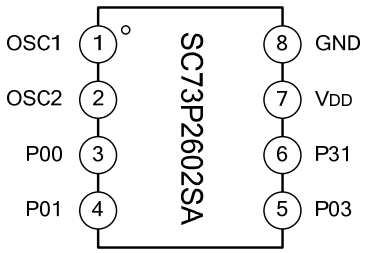


PIN CONFIGURATIONS





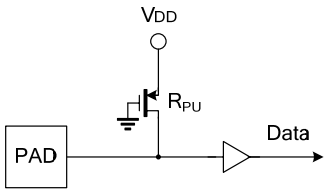
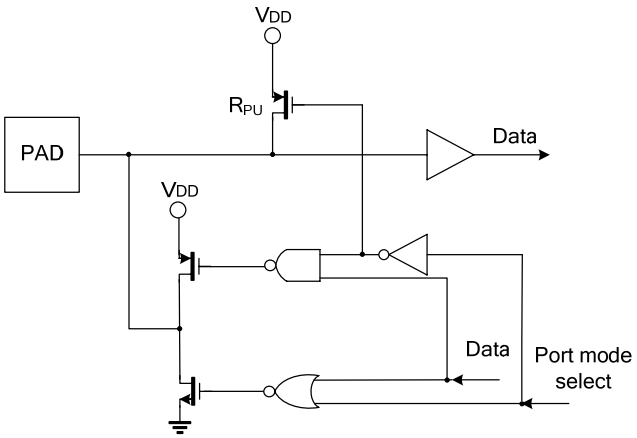
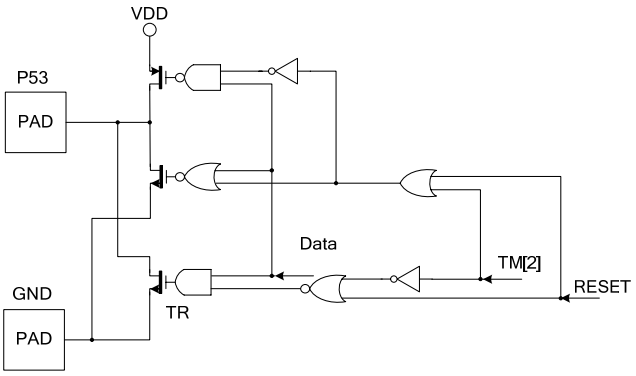
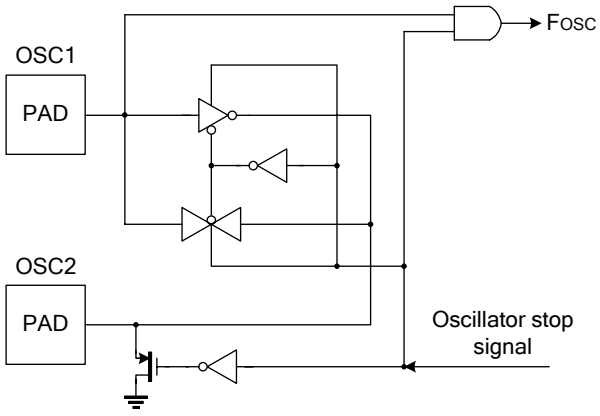




PIN DESCRIPTIONS

Pin No.								Pin name	Pin type	Description
-SH1	-SN1	-RC2 -RD2 -SM2 -SN2	-RC3 -RD3 -SM3 -SN3	-SC1	-SC2	-SC3	-SA			
24	20	6	20	16	16	4	7	VDD	PWR	Power supply
1	1	9	1	1	1	7	8	GND	PWR	Ground
2	2	7	4	2	4	5	1	OSC1	I	External oscillator input port
3	3	8	5	3	5	6	2	OSC2	O	External oscillator output port
6	4	11	7	4	6	8	3	P00	I	Input port
7	5	12	8	5	7	9	4	P01	I	
8	6	13	9	6	-	10	-	P02	I/O	I/O port
9	7	14	10	7	8	11	5	P03	I/O	
10	8	15	-	8	-	12	-	P10	I/O	
11	9	16	-	9	-	13	-	P11	I/O	
12	10	17	-	-	-	14	-	P12	I/O	
13	11	18	-	-	-	15	-	P13	I/O	
14	12	19	11	10	-	16	-	P20	I/O	
15	13	20	12	11	-	-	-	P21	I/O	
16	14	1	13	12	9	-	-	P22	I/O	
17	15	2	14	13	10	-	-	P23	I/O	
18	16	3	15	-	11	1	-	P30	I/O	
19	17	4	16	14	12	2	6	P31	I/O	
20	18	-	17	-	13	-	-	P32	I/O	
21	-	-	18	-	14	-	-	P33	I/O	
-	-	-	2	-	2	-	-	P50	I/O	
4	-	-	3	-	3	-	-	P51	I/O	
5	-	10	6	-	-	-	-	P52	I/O	
23	19	5	19	15	15	3	-	P53	O	Remote signal output with carrier. Can be set as push-pull output or big current open-drain output by program
22	-	-	-	-	-	-	-	NC	-	NC

PIN STRUCTURE

Pin name	Pin type	Pin structure	Remark
P00~P01	I		Built-in pull-up resistor
P02~P03 P10~P13 P20~P23 P30~P33 P50~P52	I/O		Enter input mode after reset; Pull-up resistor available in input mode; Push-pull output in output mode, and LED can be driven by low level.
P53	O		High-impedance status after reset; Open-drain output for using internal infrared LED driver transistor ; Push-pull output for using external infrared LED driver transistor.
OSC1 OSC2	I O		

FUNCTION DESCRIPTION

1. Word width

Word width for SC73P2602 is 9-bit, that is 2K word is 2K×9-bit.

2. Instruction period

Instruction and internal operation are both based on main clock. The instruction period is the time of executing a whole instruction. There are single-/double-period instructions available for SC73P2602.
An instruction period consists of 5 beat which is a system clock period (1/FMAIN). Hence, an instruction period is 5/ FMAIN.

3. PC

PC for SC73P2602 is 11-bit and the maximum addressable memory is 2K.
PC value is the address of next instruction to be executed and it is 0 after reset. In general, PC is added by 1 after executing an instruction because instructions for SC73P2602 is single-byte instruction. Fixed value is evaluated to PC when executing jump, subprogram call and subprogram return.

4. MBR

Memory buffer register (MBR) is the write-only, higher 5-bit of the program pointer. The ROM of SC73P1602 can be divided into 15 blocks and each block has 128 bytes. These blocks can be addressed by the MBR. For program jump, the BLOCK value containing the target address should be loaded to MBR before executing BSS addr7 instruction.

5. STACK

11-bit stack register is used for storing PC when calling subprogram. 3-level subprogram can be called for there is only 3-level hardware stack registers in SC73P2602.

6. B, H, D

4-bit data look-up pointer registers. Lower 3-bit of register B and all bits (4-bit) of H, D are used as pointers pointing to data table when accessing constant data in OTP whose space of 2K can be used for data table or program memory, otherwise, register B, H, D act as general purpose register as others. Constant data stored in the table can be accessed through table look-up instruction.

7. ALU

The arithmetic and logic unit plays a leading role in performing various operations of 4-bit binaries. The operation of ALU will change the carry flag (CF) and the zero flag (ZF).

8. ACC

4-bit accumulator, it is mostly used to store data and results.

9. CF

Carry flag.

10. SF

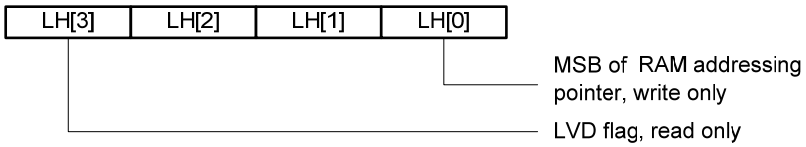
Status flag. jump instruction is only effective only when SF=1. SF is 1 after reset.

11. CH0, CH1, CL0, CL1

CH0, CH1, CL0 and CL1 are carrier level control registers for controlling the high and low level to (CH+1)/Fosc and(CL+1)/Fosc. Where, Fosc is oscillator frequency, CH0 and CH1 are higher 4-bit and lower 4-bit of CH respectively, while CL0 and CL1 are higher 4-bit and lower 4-bit of CL.

12. LL, LH

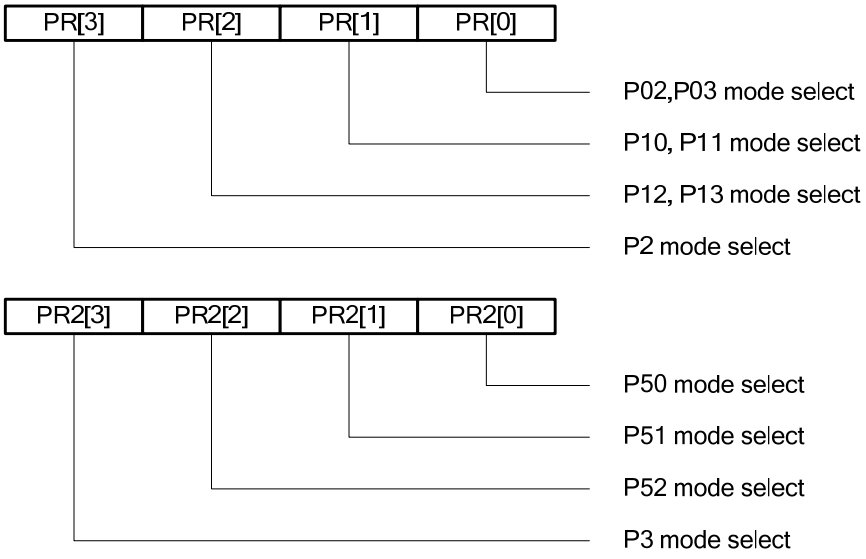
4-bit LL register, lower 4-bit of RAM addressing pointer, can be used as general register as well.
4-bit LH register, LH[0] is the MSB of RAM addressing pointer.



Note: LH[3] is LVD flag and it is “0” when V_{DD}< V_{LVD}, otherwise it is “1”. Typical application: this bit is used for judging whether the circuit is working in low-voltage area to avoid incomplete code transmission. Typical value for is V_{LVD} 1.7V.

13. PR (PR, PR2)

The port mode register, which specifies the input mode or output mode of the I/O port, is 4-bit write-only. When PR=1, the corresponding port is set to output mode. PR=0, it is set to input mode. The execution of the HOLD instruction won’t affect the I/O modes of operation. When reset, PR=0. The port is in input mode.

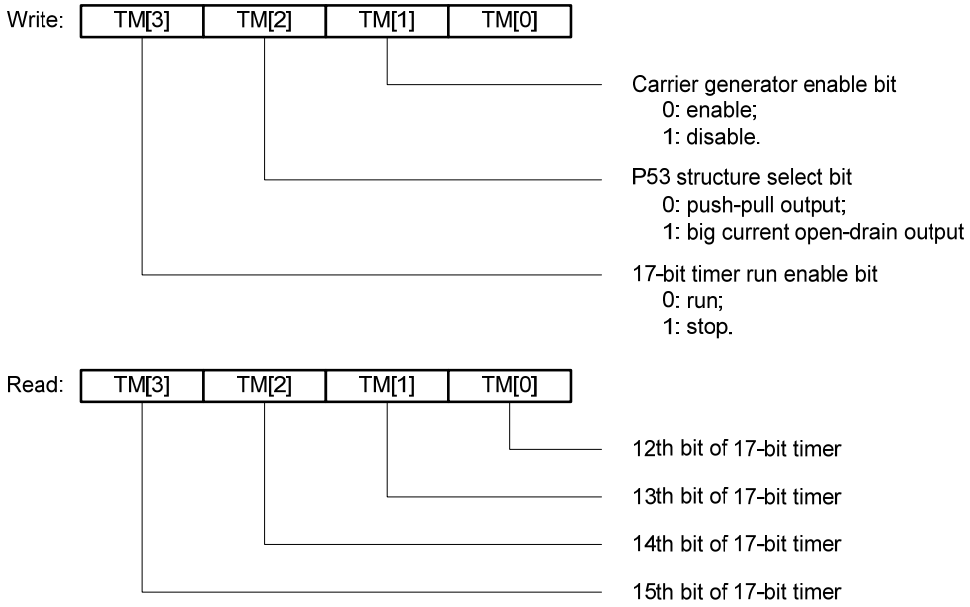


14. TM

4-bit function register with different functions for write TM and read TM.

Write TM: 17-bit timer run enable, P53 structure select and carrier generator enable;

Read TM: the 12th~15th bit value of 17-bit timer (the lowest bit is the first bit)



15. OTP address assignment

OTP ROM for SC73P2602 is 2K (9-bit), and the address assignment is shown below:

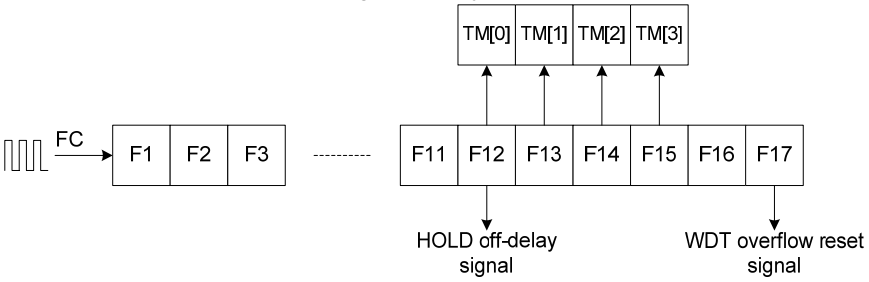
Address	Description
0000H ~ 003FH	Subprogram entry address (can be multiplexed as normal program area)
0040H ~ 07FFH	Program area (can be multiplexed as data table)

16. RAM

Data memory consists of 32x4 bits and is used to store temporary data and results after a program is executed. It can address the entire RAM areas by r LH[0] and LL[3:0]. When reset, the contents of RAM are not defined. It is recommend to initialize it at the beginning of program.

17. TIMER

SC73P2602 has one 17-bit timer whose operating frequency is FC＝FMAIN.



Reset value for timer is 1FFFFH, and it counts down.
WDT overflow reset signal is generated if the 17th bit of timer is converted from “1” to “0”.
Timer is reset if system is reset (including power-up reset, low-voltage reset and WDT overflow reset), HOLD is cleared or reset instruction TMRST is executed.
Program is only executed when the 12th bit of time is converted from “1” to “0” after HOLD cleared.

18. Carrier generator

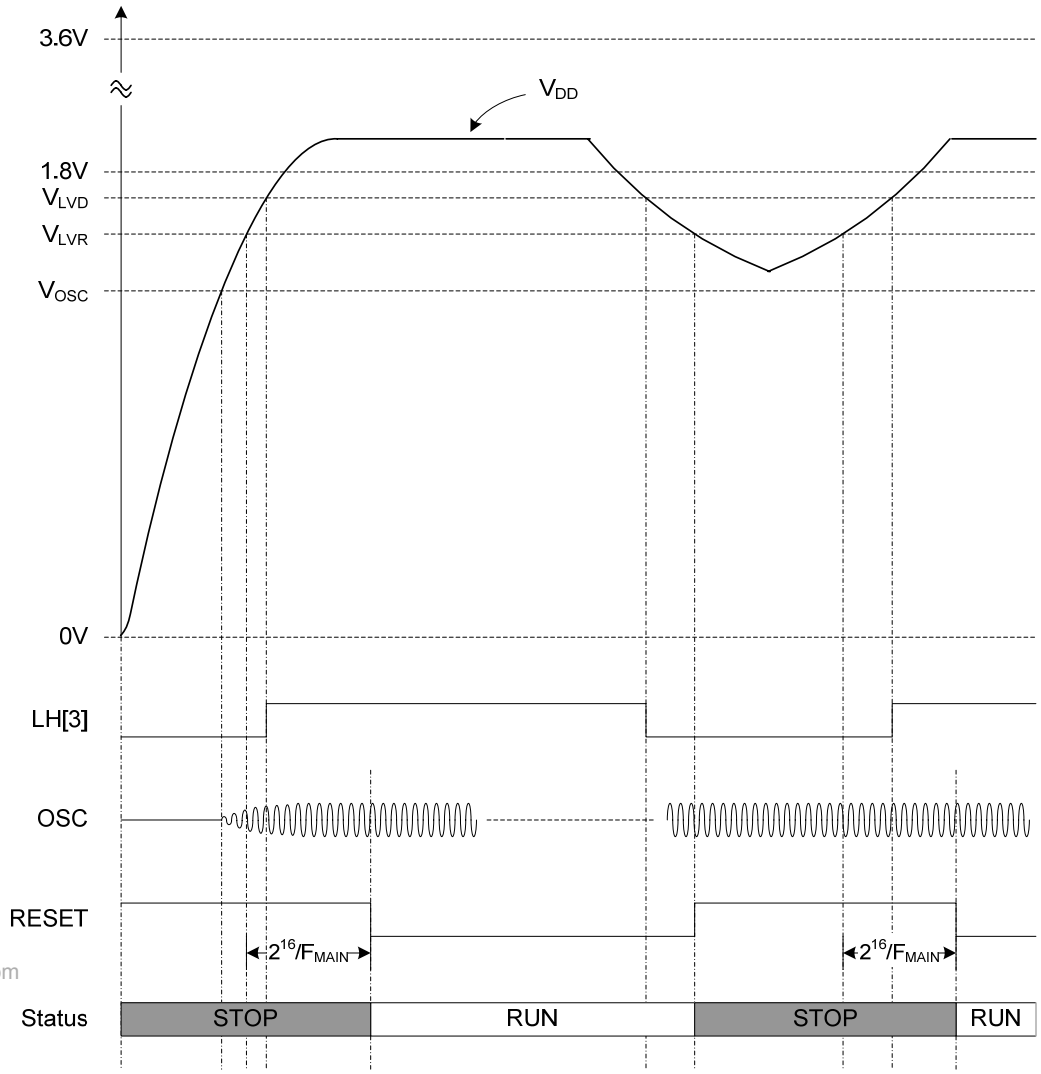
Various carrier with different duty factors and frequencies are generated through setting high/low level duration by carrier register (see CH0, CH1, CL0, CL1 description).

19. I/O port

SC73P2602 has 5 groups (20 in all) of I/O ports and most have both input/output modes (except P00 and P01 can only be used as input and P53 can only be used as output), details are as follows:
P00-P01: input pin with pull-up resistor. It can be used for keyboard scan input and input low level can clear HOLD status;
P02-P03: input/output port. The input/output characteristic is decided by PR. When used as input port, it has pull-up resistor and can be used as keyboard scan input, input low level can clear HOLD status; when used as output pin, it can be used for keyboard scan output and output low level can drive LED directly.

P10-P13: same as P02;
P20-P23: same as P02;
P30-P33: same as P02;
P50-P52: same as P02;
P53: output infrared remote signal with carrier. There are two structures: push-pull structure is for external infrared emitter driving and big current open-drain structure is for driving infrared emitter directly, with opposite pole of the former structure.

20. Low voltage detect (LVD)



Note:

1. When VDD<VLVR, RESET signal is generated (high level reset).
2. When VDD changes form lower than VLVR to higher than it, Program is normally run after a delay of 216 main clock with frequency of FMAIN (counter by timer) to guarantee reliability.
3. When VDD>VOSC, oscillation start up.
4. When VDD>VLVD, LH[3] = “1”; when VDD<VLVD, LH[3] = “0”.
5. VLVD = 1.7V (Typ.); VLVR = 1.55V(Typ.); VOSC = 1.35V(Typ.).

INSTRUCTION SET

Symbol

addr7	lower 7-bit of address
b	Bit address (0~3)
C	carry flag
vect	Subprogram entry address vector
Z	Zero flag: when ACC=0, Z=" 1"; ACC≠0, Z="0"
#k	immediate data(0~15)
%p	port address
←	evaluate the right value to left
PUSH	Push
POP	pop
TIMER	17-bit timer

1. Transmit instruction

Instruction	Operation	Flag		cycle
		CF	SF	
LD A, LL	A ← LL	-	1	2
LD A, B	A ← B	-	1	2
LD A, H	A ← H	-	1	2
LD A, D	A ← D	-	1	2
LD A, @LL	A ← RAM(LL)	-	1	1
LD A, #k	A ← k	-	1	1
LD CL1, A	CL1 ← A	-	1	2
LD CL0, A	CL0 ← A	-	1	2
LD CH1, A	CH1 ← A	-	1	2
LD CH0, A	CH0 ← A	-	1	2
LDH A, @BD	A ← ROM(BD)7-4	-	1	2
LDL A, @BD	A ← ROM(BD)3-0	-	1	2
LDS A, @BD	A ← ROM(BD)8	-	1	2
LDH @LL, @BD	RAM(LL) ← ROM(BD)7-4	-	1	2
LDL @LL, @BD	RAM(LL) ← ROM(BD)3-0	-	1	2
LDS @LL, @BD	RAM(LL) ← ROM(BD)8	-	1	2
LD LL, A	LL ← A	-	1	2
LD LL, #k	LL ← k	-	1	1
LD @LL, A	RAM(LL) ← A	-	1	1
LD @LL, #k	RAM(LL) ← k	-	1	1
LD D, A	D ← A	-	1	2
LD H, A	H ← A	-	1	2
LD B, A	B ← A	-	1	2
LD PR, A	PR ← A	-	1	2

Instruction	Operation	Flag		cycle
		CF	SF	
LD PR2, A	PR2 ← A	-	1	2
LD TM, A	TM ← A	-	1	2
LD A,TM	A ←TM	-	1	2

01.	LD A, LL	Load values in the LL register to the accumulator.
02.	LD A, B	Load values in the BR register to the accumulator.
03.	LD A, H	Load values in the HR register to the accumulator.
04.	LD A, D	Load values in the DC register to the accumulator.
05.	LD A, @LL	Load the contents of RAM pointed at by the LL register to accumulator.
06.	LD A, #k	Load the 4 bit immediate K to accumulator.
07.	LD CL1, A	Load the content of the accumulator to the CL1 register.
08.	LD CL0, A	Load the content of the accumulator to the CL0 register.
09.	LD CH1, A	Load the content of the accumulator to the CH1 register.
10.	LD CH0, A	Load the content of the accumulator to the CH0 register.
11.	LDH A, @BD	Load the higher 4 bit of ROM data pointed at by the BHD to accumulator.
12.	LDL A, @BD	Load the lower 4 bit of ROM data pointed at by the BHD to accumulator.
13.	LDS A, @BD	Load the MSB of ROM data pointed at by the BHD to accumulator
14.	LDH @LL, @BD	Load the higher 4 bit of ROM data pointed at by the BHD to RAM pointed at by the LL register.
15	LDL @LL, @BD	Load the lower 4 bit of ROM data pointed at by the BHD to RAM pointed at by the LL register.
16.	LDS @LL, @BD	Load the MSB of ROM data pointed at by the BHD to RAM pointed at by the LL register.
17.	LD LL, A	Load the contents of the accumulator to the LL register.
18.	LD LH, A	Load the contents of the accumulator to the LH register.
19.	LD LL, #k	Load immediate K to the LL register.
20.	LD @LL, A	Load the content of the accumulator to the RAM pointed at by the LL register.
21.	LD @LL, #k	Load the immediate K to RAM pointed at by the LL register.
22.	LD D, A	Load the content of the accumulator to the DC register.
23.	LD H, A	Load the content of the accumulator to the HR register.
24.	LD B, A	Load the content of the accumulator to the BR register.
25.	LD PR, A	Load the content of the accumulator to the port register(PR).
26.	LD PR2, A	Load the content of the accumulator to the port register(PR2).
27.	LD TM, A	Load the content of the accumulator to the timer register.
28.	LD A,TM	Load the content of the timer register to the accumulator.

Note: executing transmit instructions above will not change CF and SF remains 1.

2. Input/output instructions

Instruction	Operation	Flag		Cycle
		CF	SF	
LD A, %p	A ← PORT(p)	-	/Z	2
LD @LL, %p	@LL ← PORT(p)	-	/Z	2
LD %p, A	PORT(p) ← A	-	1	2
LD %p, @LL	PORT(p) ← @LL	-	1	2

01. LD A, %p — Load the value of port(P) to the accumulator
02. LD @LL, %p — Load the value of port(P) to RAM pointed at by the LL register.
03. LD %p, A — Load the contents of the accumulator to port (P).
04. LD %p, @LL — Load the contents of RAM pointed at by the LL register to port(P).

Note: The above four input/output instructions are used mostly for port operation, and the two read instructions will affect the status flag SF.

3. Arithmetic and logic instructions

Instruction	Operation	Flag		Cycle
		CF	SF	
ADD A, @LL	A ← A+RAM(LL)	-	/C	1
ADDC A, @LL	A ← A+RAM(LL)+CF	C	/C	1
ADD A, #k	A ← A+k	-	/C	1
ADD LL, #k	LL ← LL+k	-	/C	2
SUBRC A, @LL	A ← RAM(LL)-A-/CF	C	C	1
INC @LL	RAM(LL) ← RAM(LL)+1	-	/C	1
DEC @LL	RAM(LL) ← RAM(LL)-1	-	C	1
INC LL	LL ← LL+1	-	/C	2
DEC LL	LL ← LL-1	-	C	2
INC D	D ← D+1	-	/C	2
INC H	H ← H+1	-	/C	2
INC B	B ←B+1	-	/C	2
DEC D	D ← D-1	-	C	2
DEC H	H ← H-1	-	C	2
DEC B	B ← B-1	-	C	2
AND A, @LL	A ← A&RAM(LL)	-	/Z	1
OR A, @LL	A ← A | RAM(LL)	-	/Z	1
XOR A, @LL	A ← A^RAM(LL)	-	/Z	1

01. ADD A, @LL — Add the contents of RAM pointed at by the LL to accumulator, and store the sum in the ACC. This operation will affect SF, SF=/C.
02. ADDC A, @LL — Add the contents of RAM pointed at by the LL register to accumulator with carry. Store the carry bit in the CF. This operation will affect SF, SF=/C.

03.	ADD A, #k	Add immediate K to accumulator. And store the sum in the ACC. This will affect SF, SF=/C.
04.	ADD LL, #k	Add immediate K to the LL register and store the sum in the LL. This will affect SF, SF=/C.
05.	SUBRC A, @LL	Subtract instruction with borrow (the complement of carry). Subtract the contents of the accumulator from the contents of RAM pointed at by the LL register, subtract the complement of the carry bit, then store the results in the accumulator, transfer the carry bit to the CF, this will affect SF and CF, SF=C.
06.	INC @LL	Increment instruction. Increment the contents of RAM pointed at by the LL register by 1. This will affect SF, SF=/C.
07.	DEC @LL	Decrement instruction. Decrement the contents of RAM pointed at by the LL register by 1. This will affect SF, SF=C.
08.	INC LL	Increment instruction. Increment the contents of the LL register by 1. This will affect SF, SF=/C.
09	DEC LL	Subtract 1 from the content in register LL. SF is affected, SF=C.
10.	INC D	Increment instruction. Increment the contents of the DC register by 1. This will affect SF, SF=/C.
11.	INC H	Increment instruction. Increment the contents of the HR register by 1. This will affect SF, SF=/C.
12.	INC B	Increment instruction. Increment the contents of the BR register by 1. This will affect SF, SF=/C.
13.	DEC D	Decrement instruction. Decrement the contents of the DC register by 1. This will affect SF, SF=C.
14.	DEC H	Decrement instruction. Decrement the contents of the HR register by 1. This will affect SF, SF=C.
15.	DEC B	Decrement instruction. Decrement the contents of the BR register by 1. This will affect SF, SF=C.
16.	AND A, @LL	The contents of the accumulator and RAM pointed at by the LL register are ANDed and the results are stored in the accumulator. SF is changed, SF=/Z.
17.	OR A, @LL	The contents of the accumulator and RAM pointed at by the LL register are ORed and the results are stored in the accumulator. SF is changed, SF=/Z.
18.	XOR A,@LL	The contents of the accumulator and RAM pointed at by the LL register are XORed and the results are stored in the accumulator. SF is changed, SF=/Z.

4. Bit operation instructions

Instruction	Operation	Flag		Cycle
		CF	SF	
CLR @LL, b	RAM(LL)b←0	-	1	2
SET @LL, b	RAM(LL)b←1	-	1	2
TEST @LL, b	SF←/RAM(LL)b	-	*	2

01.	CLR @LL, b	Clear the B-bit of the RAM pointed at by the LL register.
02.	SET @LL, b	Set the B-bit of the RAM pointed at by the LL register to 1.
03.	TEST @LL, b	Test the B-bit of the RAM pointed at by the LL register. If this bit is1, the SF is set to 0; otherwise, the SF is set to 1.

5. Carry operation instructions

Instruction	Operation	Flag		Cycle
		CF	SF	
CLR CF	CF←0	0	1	2
SET CF	CF←1	1	1	2
TESTP CF	SF←CF	-	CF	1

01.	CLR CF	Clear the carry flag to 0.
02.	SET CF	Set the carry flag to 1.
03.	TESTP CF	Test the carry flag, send the carry flag to SF.

6. Jump instructions

Instruction	Operation	Flag		Cycle
		CF	SF	
BSS addr7	PC[6:0] ← addr7	-	1	2

01.	BSS addr7	Jump to addr7, jump range: in the block (128-byte)

7. Subroutine instructions

Instructions	Operation	Flag		Cycle
		CF	SF	
CALLS vect	PUSH(PC+1); PC ← vect	-	-	2
RET	POP(PC)	-	-	2

01.	CALLS vect	Call the subroutine, and the subroutine address can only be 000H-01FH.
02.	RET	Subroutine back

8. Other instructions

Instructions	Operation	Flag		Cycle
		CF	SF	
HOLD	-	-	1	1
NOP	-	-	-	1
TMRST	TIMER ← 1FFFFH	-	-	1

01.	HOLD	MCU enters power-saving mode with little power dissipation after executing this instruction.
02.	NOP	Nop instruction, this instruction has no effect.
03.	TMRST	Timer reset. Set all bits of timer to 1. this instruction is usually used for reset watchdog.

MACRO INSTRUCTIONS

symbol:

addr7	lower 7-bit of program address

1. JMPS

【Format】

JMPS address

【Function】

Jump in ROM

【Expression】

Address is the absolute address, it can be a digital, symbol defined by EQU or the address symbol.

Combined by:

```
LD MBR, #k    ;address=k*128+addr7
BSS addr7
```

【Example】

```
JMPS MAIN
JMPS 100H
```

2. VENT

【Format】

VENT address

【Function】

Define the entry address of sub-program and main program.

【Expression】

Address is the absolute address, it can be a digital, symbol defined by EQU or the address symbol.

Combined by:

Same as JMPS addr11, it is combined by:

```
LD MBR, #k    ;address=k*128+addr7
BSS addr7
```

This instruction should be included and must be at the beginning of the program. The first VENT denotes the main program address and the following VENT instructions denote the entry of the sub-program. In general, 15 sub-programs can be defined at most. All the sub-programs called by CALL instruction should be defined in VENT, or else errors will occur in assembly.

【Example】

```
VENT MAIN
VENT SUB1
VENT SUB2
……
```

```
        ORG 100H    ;pseudo instruction for redefining address of following instructions
MAIN:
        NOP
        NOP
        CALLS SUB1
        CALLS SUB2
        ……
SUB1:
        ……
SUB2:
        ……
```

PSEUDO INSTRUCTIONS

1. ORG

【Format】

ORG address

【Function】

Redefine following start address

【Expression】

Address: redefined address, can be binary, decimal or hexadecimal.

Redefined address is an absolute address and should be higher than that above, or a fault is occurred during compiling. 0000H is defaulted if no address is set by ORG instruction.

【Example】

ORG 0100H

2. EQU

【Format】

Symbol EQU digital

【Function】

Define a digital as a symbol. Symbol ＝ digital.

【Expression】

Symbol should be legal (begin as a letter and composed by letters, digital and underline), and digital should be binary, decimal or hexadecimal. There is no colone before EQU in definition, and it can only be used after the definition.

【Example】

```
Data1 EQU 12H
Data2 EQU 1001B
```

3. DB

【Format】

[Num] DB data

【Function】

Define data with number of num.

【Expression】

Num: indicates number of data, default value is 1.

Data: data to be written to ROM. lower 9-bit value of data is taken without warning if data is larger than 1FFH because ROM is only 9-bit.

【Example】

```
DB 12H          ; fill in one data
DB 10010B       ; fill in one data
12H DB 55H      ; fill in 18 data
```

4. END

【Format】

END

【Function】

Indicates the ending

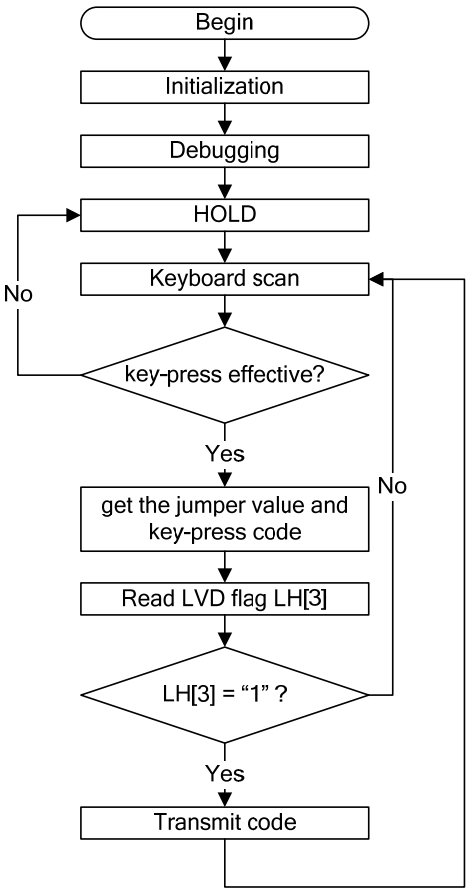
【Expression】

Content after END will not be processed by assembler. If END is omitted, the assembler will process all the lines of the source file.

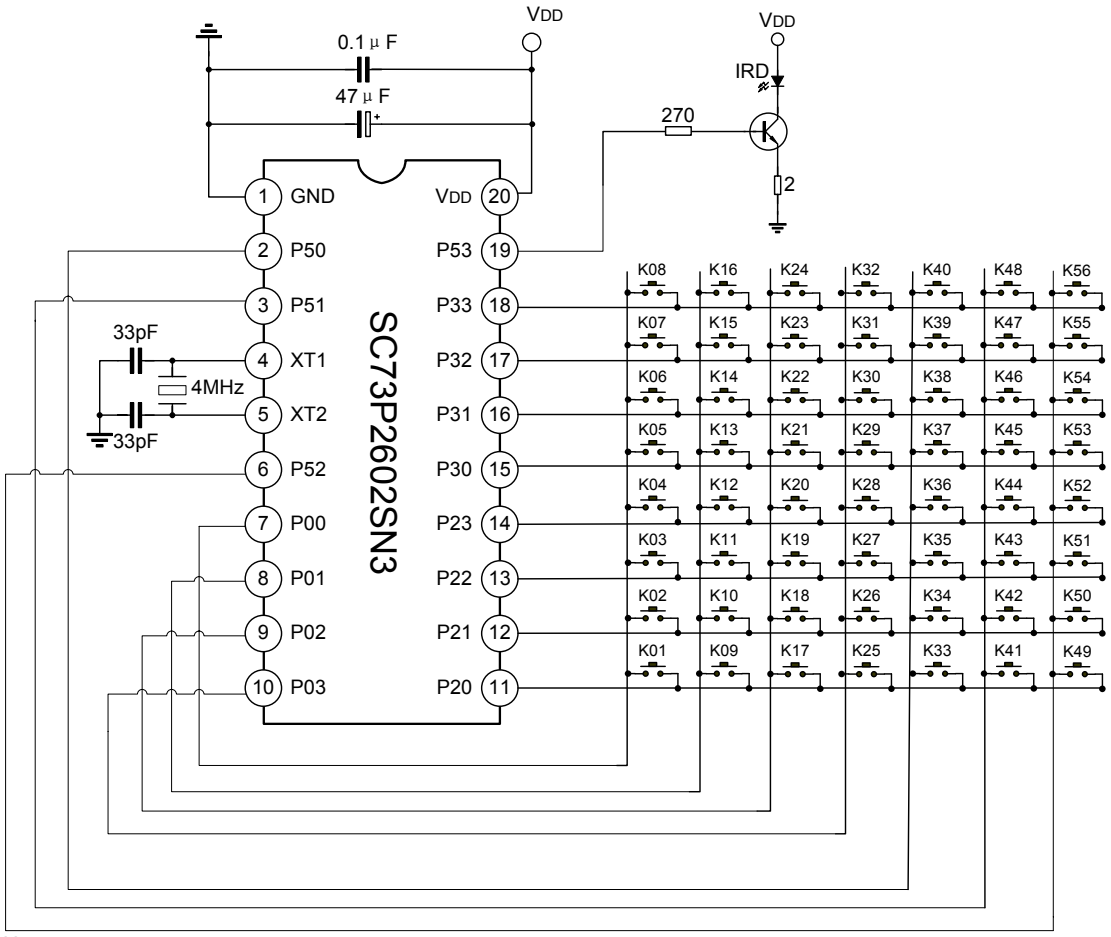
【Example】

```
END
```

REMOTE CONTROL FLOW CHART

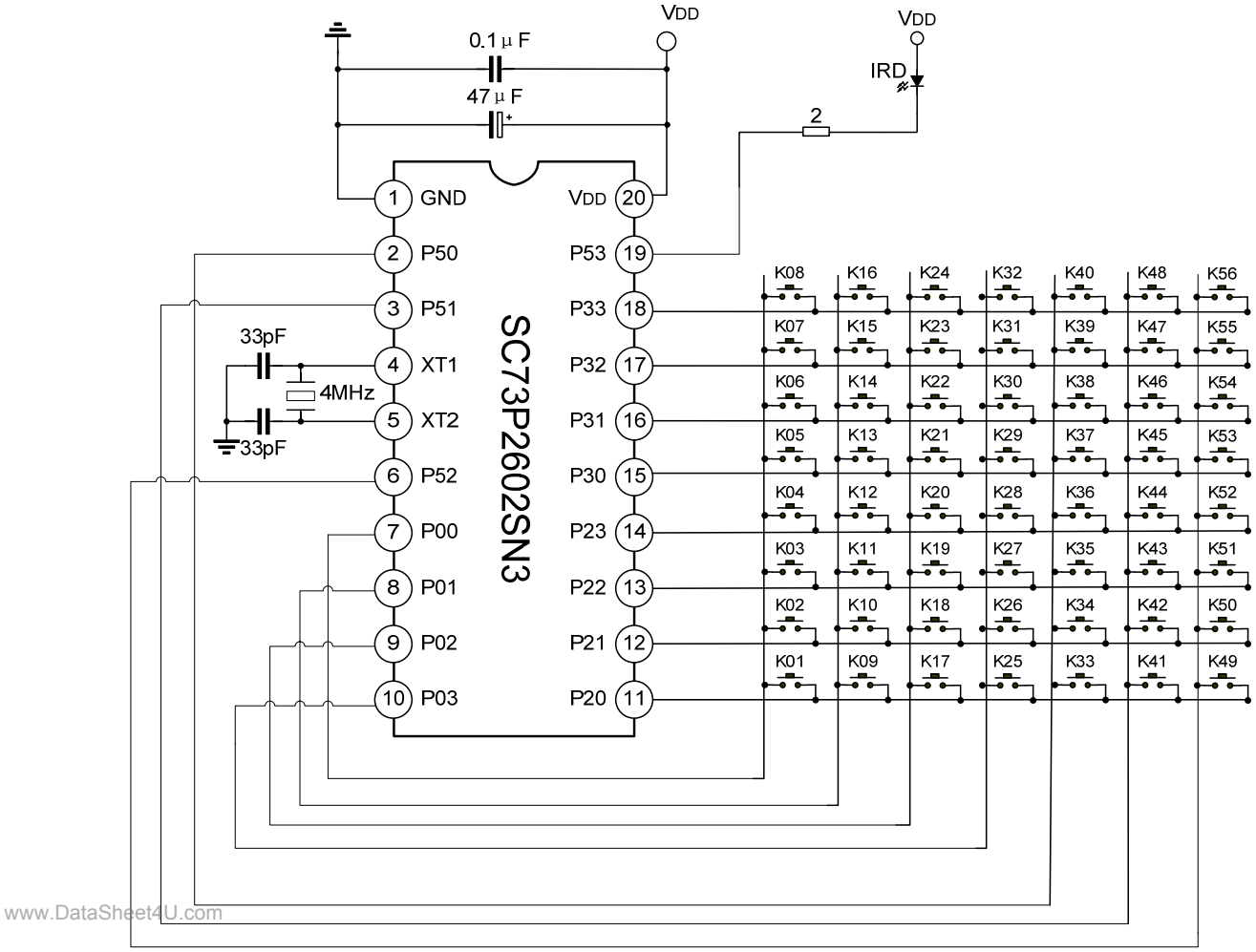


TYPICAL APPLICATION CIRCUIT1 ---(56 Keys)



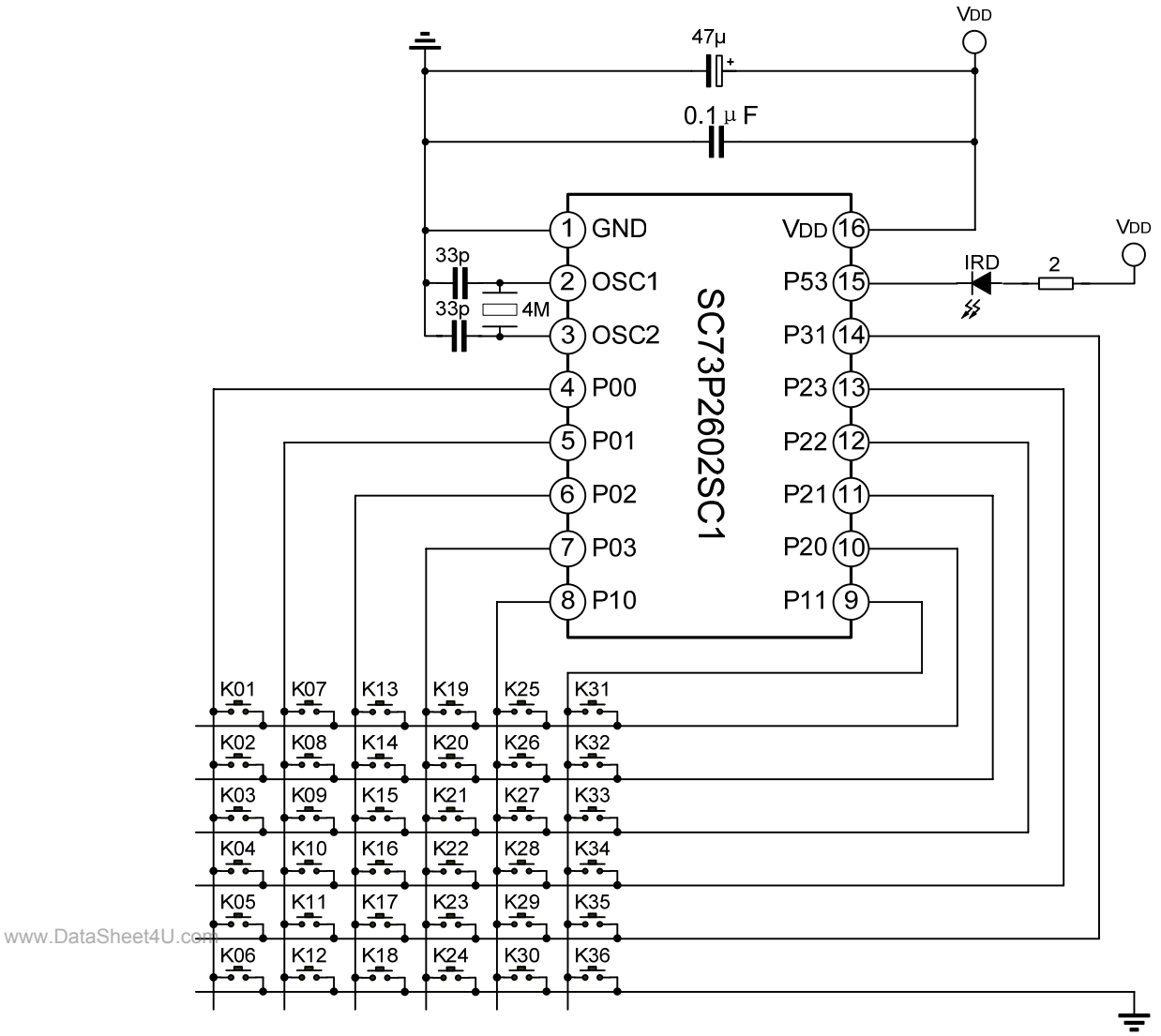
The capacitor between VDD and GND should be close to IC and the routing should be as short as possible.

TYPICAL APPLICATION CIRCUIT2 ---(56 Keys with built in TR)



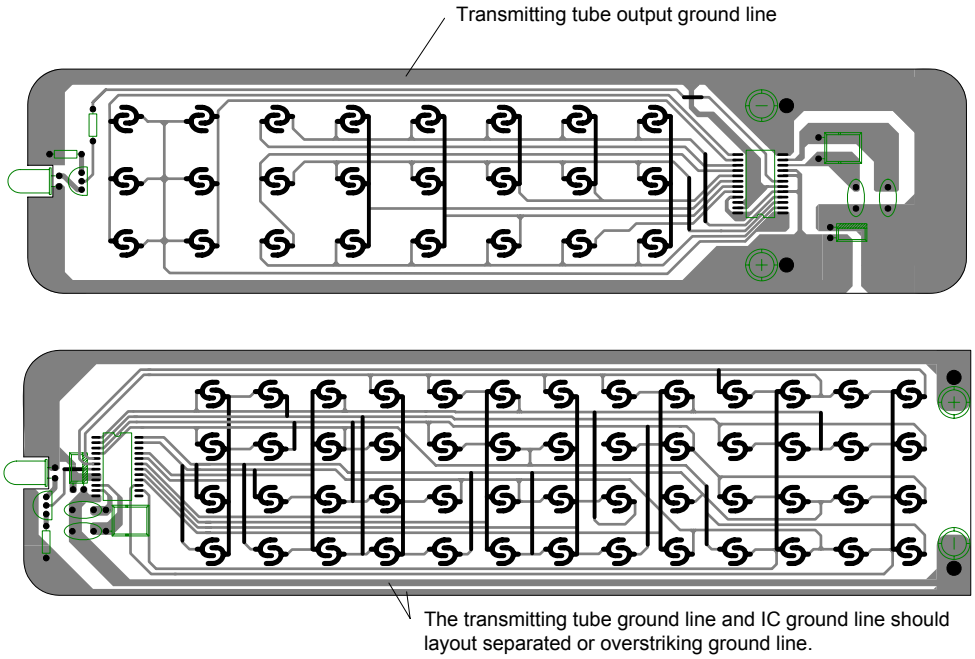
The capacitor between VDD and GND should be close to IC and the routing should be as short as possible.

TYPICAL APPLICATION CIRCUIT3 ---(36 Keys with built in TR)



The capacitor between V_{DD} and GND should be close to IC and the routing should be as short as possible.

PCB WIRE LAYOUT SCHEMATIC:



The above IC only use to hint, not to specified.

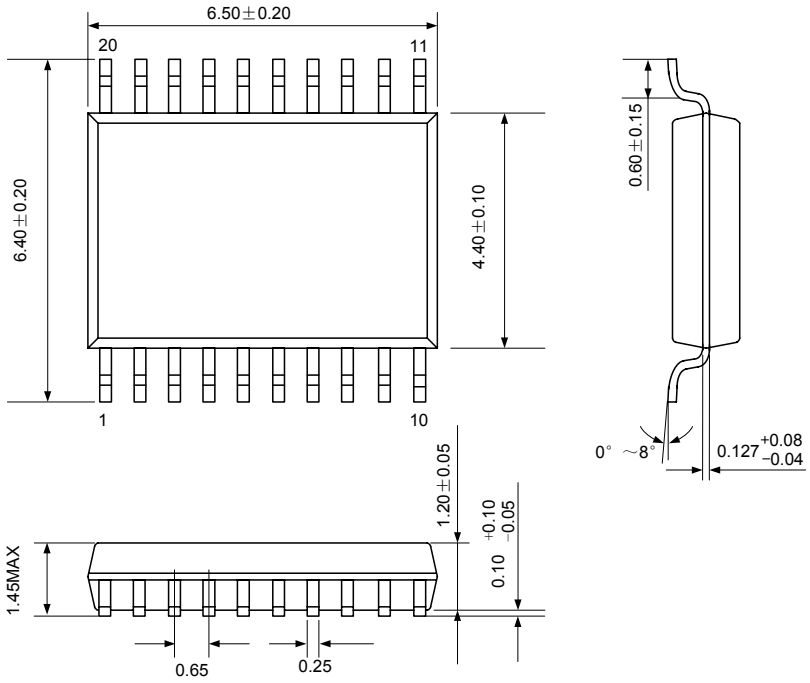
Note:

* In wire layout, the power filter capacitor should be close to IC.
* In wire layout, should avoid power line and ground line too long.
* Recommended infrared transmit unit and IC ground line should layout separated, or overstriking lines.
* The emitter of triode connect 2Ω resistor at least.
* Recommended triode use 8050.

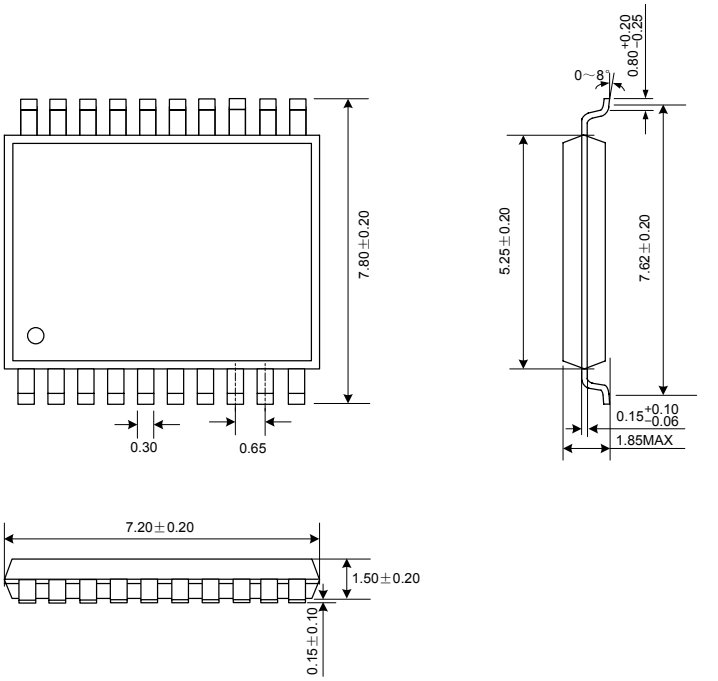
* IC oscillator input mustn't be on the outside layer, thus to avoid the abnormal working when human body touches the remote controller without crust in testing.

PACKAGE OUTLINE

SSOP-20-225-0.65 Unit: mm

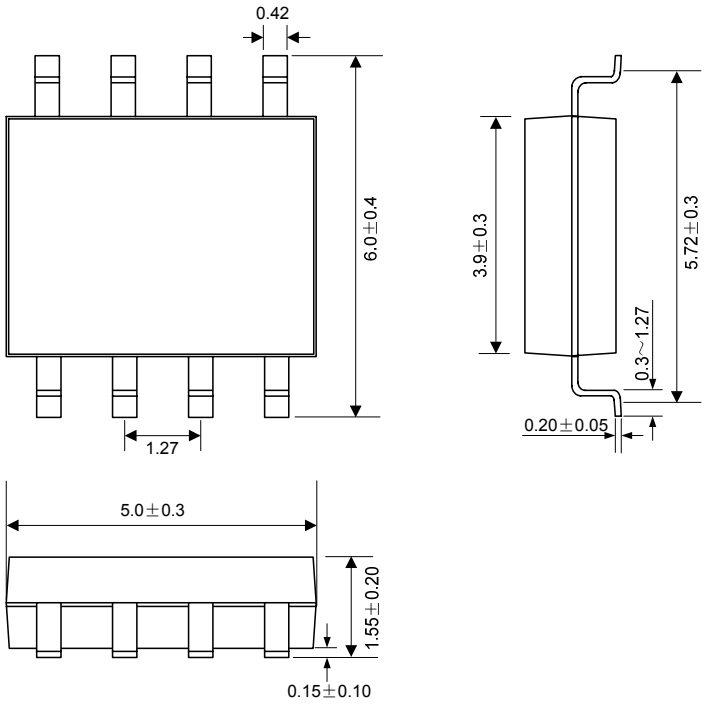


SSOP-20-300-0.65 Unit: mm

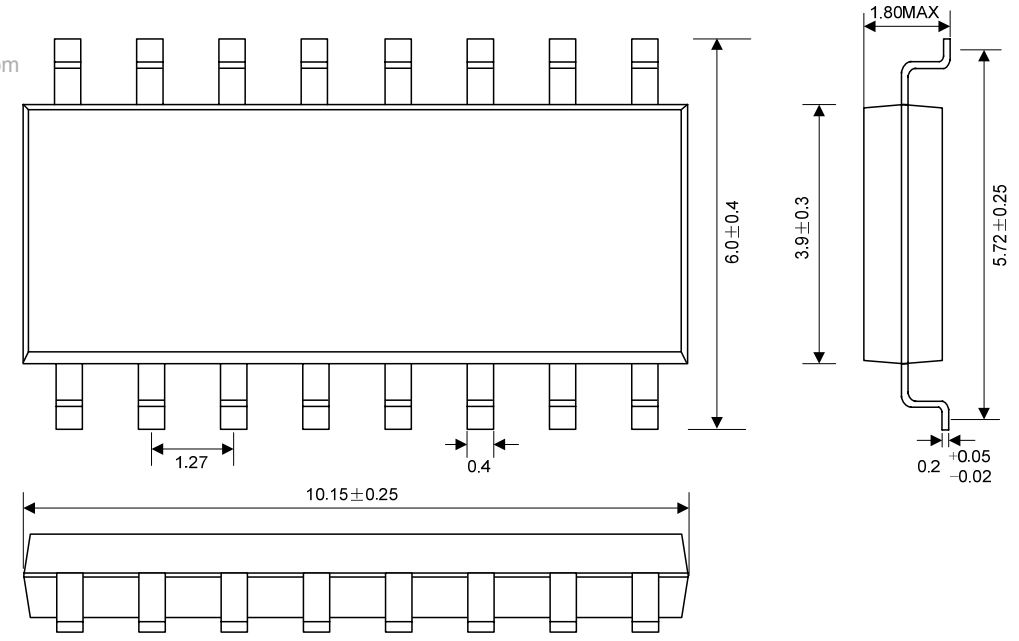


PACKAGE OUTLINE (Continued)

SOP-8-225-1.27 Unit: mm

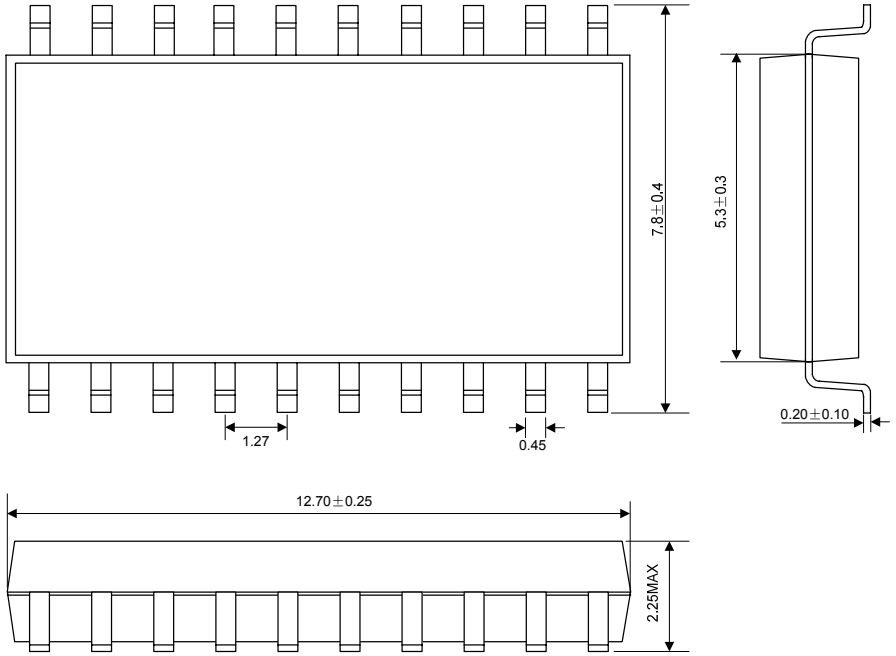


SOP-16-225-1.27 Unit: mm

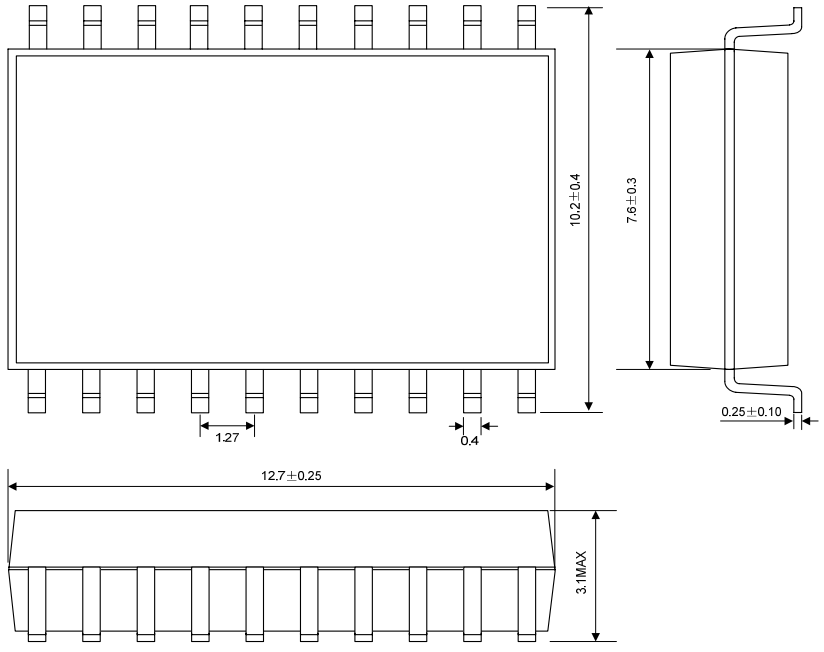


PACKAGE OUTLINE (Continued)

SOP-20-300-1.27 Unit: mm

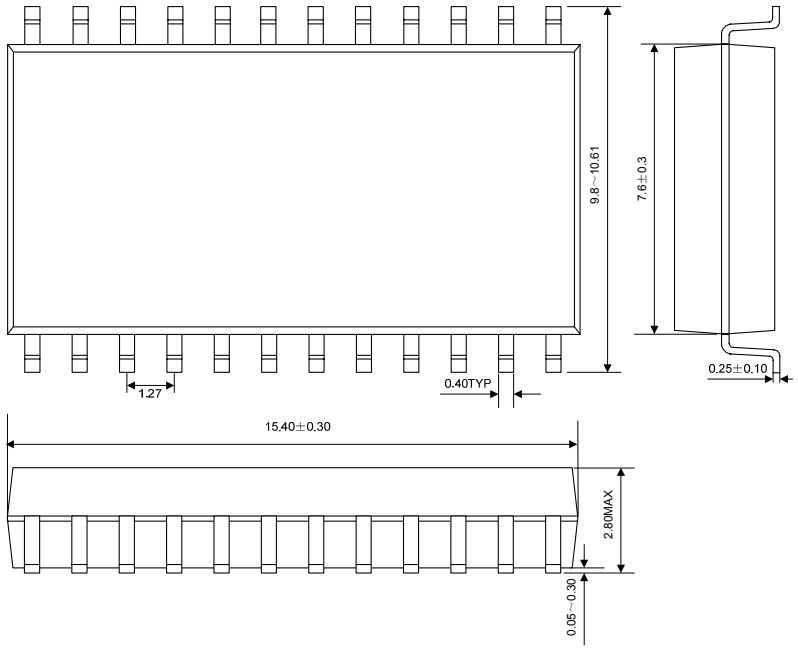


SOP-20-375-1.27 Unit: mm



PACKAGE OUTLINE (Continued)

SOP-24-375-1.27 Unit: mm



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Disclaimer :

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without further notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.
- Silan will supply the best possible product for customers!