SC6820
Device Specification

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D1

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Revision History

Version	Data	Owner	Note
0.8	10/26/2011	Joey Jiang	First draft;
1.0	12/12/2011	Joey Jiang	Update chapter 3,4,9,10

1 System Overview

SC6820 is a GSM/GPRS/EDGE baseband (BB) chip for mobile devices, and it also integrated a lot of multimedia accelerators and 3D graphic engine to develop rich multimedia applications. This document specifies the functions and features of SC6820.

1.1 General Description

SC6820 is a highly integrated mixed signal baseband processor for GSM/GPRS/EDGE applications. It consists with support of specially optimized architecture and many dedicate accelerators. SC6820 can achieve high performance and low power for a lot of applications. Proprietary architectures and algorithms were developed for low power ASIC design and power management. Unique techniques are used for noise/offset calibration and cancellation. Overall, SC6820 presents a revolutionary platform for mobile devices.

Platform

SC6820 is capable of running the ARM® Cortex A5™ 32-bit RISC processor at up to 1GHz, thus providing fast data processing capabilities. The high clock frequency, separate code and data caches are included to improve the overall system efficiency.

For large amount of data transfer, high performance DMA（Direct Memory Access）with hardware flow control is implemented, which greatly enhance the data movement efficiency with reducing MCU and DSP processing load.

Targeted as a high performance platform for mobile applications, Unique ID（UID）and secure boot are also provided to prevent unauthorized porting of the software load and fulfill other applications.

External Memory

SC6820 supports mobile DDR/SDR-SDRAM, Nand flash. The external memory interface is designed for 1.8V I/O voltage. The driving strength is configurable for signal integrity adjustment.

Multi-media

SC6820 integrated digital still camera processor, H.264 decoder and MPEG4/H.263/JPEG codec engines. The multi-media subsystem provides a connection to up to 2 CMOS image sensors. With its high performance application platform.

SC6820 utilizes high resolution DAC, digital audio, and audio synthesis technology to provide superior audio features for all future multi-media needs.

Furthermore, a dedicated LCDC controller enables MCU interface to 8/9/16/18/24 bit LCM panels, which provides much better configurability for multi-media products.

Peripherals and connectivity interface

SC6820 incorporates myriads of advanced peripherals for different applications. It supports 3 UART, 2 IIS/PCM, 2 SPI, Keypad controller, 2 SIM controller, 4 PWM, 4 I^2C, USB2.0, 2 SDIO, Touch Panel controller, and General Purpose Programmable I/Os(GPIO). These interfaces provide SC6820 users with the highest degree of flexibility in implementing solutions suitable for the targeted application.

Radio

SC6820 integrates a mixed-signal baseband front-end in order to provide a well-organized radio interface with flexibility for efficient customization. The front-end contains gain and offset calibration mechanisms, and filters with programmable coefficients for comprehensive compatibility control on RF modules.

The RF interface also consists of the following parts:

- An RF power amplifier control, which controls the timing of an RF power amplifier ON/OFF as well as its output power.
- An RF serial port, which is used to program control registers inside the RF module.
- RF parallel controls, which form a group of control signals to control the ON/OFF of the RF active components and passive couplers/switches.

Audio

SC6820 audio interface integrates D/A and A/D converters for Voice band, it also provides stereo input and analog MUX.

Power Management

With 2 DCDC and 22 LDO on chip ,SC6820 offers various low-power features to help reduce system power consumption. These features include deep sleep(standby mode), ARM system sleep, DSP system sleep, ARM processor sleep mode, DSP processor sleep mode, power down mode for individual peripheral etc. The advanced low leakage CMOS process which SC6820 adopted provide and overall low leakage solution.

Package

SC6820 is offered in a 13 mm x 13 mm x 1.4 mm 454 ball, 0.5 mm ball pitch LFBGA package

1.2 SC6820 Features

SC6820 is Spreadtrum's 3rd-generation GSM/GPRS/EDGE ASIC solution chip. It inherits most of the features from SC6820 series with performance improvement and feature enhancement.

1.2.1 General Features

- With ARM® Cortex™ A5 @ 1GHz, 32 bits DDR @ 400MHz, embedded Graphics and multimedia accelerators. The overall system performance of processor, graphics engine, DDR interface have been well organized, so SC6820 completes the AP requirements of prevalent Android phone
- mixed signal baseband processor for GSM/GPRS/EDGE applications
- Low power and high-performance device of mixed signal CMOS technology
- External supply voltages: battery 3.6V(typical),optional backup battery 3.0V(typical)
- Internal supply voltages: analog 3.0V or 3.3V, digital I/O 2.85V or 1.8V(typical), digital core 1.1V(typical) and RTC power supply 1.8V(typical)
- Integrated power management, voice band, audio band, and base band analog front ends

1.2.2 Platform Features

MCU subsystem

- ARM® Cortex™ A5 32-bit RISC processor, up to 1G Hz
- 32 KB L1 I-cache and 32 KB L1 D-cache
- 256KB L2 Cache
- 32 KB dedicate on-chip SRAM
- 10 KB on-chip SRAM shared with DCAM (Digital Camera module)
- High performance multi-layer AHB-Lite bus system and low power APB system
- 24KB on-chip ROM for laboratory or factory programming and system boot
- Support boot from NAND, USB or UART
- Support memory re-mapping mechanism
- Dedicate DMA with 32 logical request channels
- Two general purpose RTC timers for task schedule and system timing recording
- One system timer with 1 ms counting scale
- Watchdog timer for system crash recovery
- 4 bus monitors for MCU system debug or performance analysis
- JTAG port for in-circuit emulation
- Support UID and secure boot

Note:

- ARM® Cortex™ A5is a registered trademark of Advanced RISC Machines Limited.

Graphics subsystem

Integrate Mali-300 GPU, a hardware accelerator for 2D and 3D graphics systems, consisits of

- A Pixel Processor (PP)
- a Geometry Processor(GP)
- a Level 2 Cache Controller(L2)
- a Memory Management Unit (MMU) for each GP and PP included in the GPU

External memory interface

- Support NAND flash, mobile DDR/SDR-SDRAM
- Two external memory controllers: NAND controller and External Memory Controller (EMC), supporting the following memory combinations:
  - NAND + DDR/SDR-SDRAM
- NAND flash is supported by NAND controller, with the following features:
  - Support 8 bit and 16 bit devices
  - Support 1.8 V and 3.0 V devices
  - Support hardware ECC generation up to 24 bits
  - Support small page (512 bytes) and large page (up to 8K bytes)
  - For small page device, support 4 consecutive memory read/write, and for large page, only support single page operation

- SDR/DDR SDRAM are supported by External Memory Controller, with the features list below:
  - ¡ Support only 1.8 V devices
  - ¡ Support up to 2G bits with single CS
  - ¡ SDRAM support 16 bit and 32 bit devices
  - ¡ Support up to 2 chip select channels (2 CS)
  - ¡ Support up to 512M byte devices
  - ¡ Memory clock is optional to clk_emc/2 or clk_emc/4 (clk_emc is the EMC controller clock, up to 400 MHz)

Peripheral and connectivity interfaces

- Support 4 SIM cards and both 1.8 V or 3.0 V devices
- Support SDIO 2.0
- Support USB 2.0 High speed
- Three UARTs
- Two SPI, support both master and slave, support 3-wire SPI, 4-wire SPI and synchronous SPI
- Two IIS and PCM, for audio codec connection
- Support 8-column x 8-row keypad with internal pull-up resistors
- Four I2C interface
- More than 100 GPIO pins
- Four PWM outputs
- Four 10-bit ADC input
- ETM port

1.2.3 Modem Features

Implementation

- ¡ Signal processing for modem functions is mainly implemented in CEVA DSP sub-system
- System timing
  - ¡ For GSM/GPRS/EDGE, recommend use a low swing 26 MHz master clock input.
  - ¡ Time tracking in power saving mode
- 16 general RFCTL wires for RF chip or antenna control
- 1 dedicate SPI ports for BB-RF chip communication
- 10-bit D/A converter with programmable gain

Note:

- CEVAX® is a registered trademark of CEVA, Inc.

GSM/GPRS/EDGE baseband

- Compatible with GSM/GPRS/EDGE Release 1999, GSM850,GSM900, DCS1800, and PCS1900 recommendations
- Complete in-phase and quadrature (I/Q) component interface between the Digital Signal Processor (DSP) and RF module
- EGPRS class12，typeB (MCS1-9 in downlink and MCS1-9 in uplink)

- Cryptographic Algorithms: (A5/1 ,A5/2 and A5/3, GEA 1,GEA 2 and GEA3 algorithms)

Voice and modem codec

- Audio signal conversion between microphone/earphone and DSP
- Second set converters for auxiliary microphone/speaker
- Stereo audio output
- Integrated microphone bias
- Integrated Class A/B or Class D
- Quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), half rate(HR), and full rate (FR)
- Dial tone generation
- Voice memo
- Noise reduction
- Echo suppression/echo cancellation
- Digital sidetone generator with programmable gain
- Voice power amplifier with programmable gain

1.2.4 Power Management Features

- Integrated two DC-DC and 25 low dropout regulators (LDOs), supplying power for internal chip or external devices. All such DC-DC and LDOs can be powered down and up with software management.
- Support standby mode with small deep-sleep current
- Integrated Li-ion battery charger, support charging from USB or external adaptor. The charger voltage can be measured with auxiliary ADC.

1.2.5 Multi-media Features

LCD display

- Integrated LCD controller (LCDC), support 2 chip select: LCD_CS0 and LCD_CS1
- Support MCU interface
- Support dual display panels: use LCD_CS1 to connect sub-panel, and LCD_CS0 to connect main display panel
- Support 8/9/16/18/24 bit LCM interfaces
- Support LCM format RGB565 and RGB666 and RGB888
- Typical image sizes: QCIF, QVGA,WQVGA, CIF, VGA,WVGA, FWVGA
- Support hardware display rotation

Image signal processor

- Support image sensor sizes up to 5M pixels
- Support image sensor data YUV422 format and JPEG format
- Support scaling down/up function, scaling factor from 1/4 to 2
- Support hardware rotation
- Support JPEG decoder baseline profile, as defined in ISO/IEC 10918-1, with sizes up to 8M pixels, and color format YUV444, YUV422/YUV422R, YUV420, YUV411 /YUV411R or gray scale.

- Support JPEG encoder baseline profile, as defined in ISO/IEC 10918-1, with sizes up to 8M pixels, and color format YUV422 or YUV420
- Support PNG,GIF decoder

Video codec

- Support H264 decoder compliant with ITU-T H.264 baseline profile, D1 30 fps
- Support H263 decoder, compliant with ITU H.263 profile 0. D1 30fps.
- Support H263 encoder compliant with ITU H.263 baseline profile CIF 30fps
- Support MPEG4 decoder compliant with ISO/IEC 14496-2 (MPEG4 Part 2 2001) @ simple profile, D1 30 fps
- Support MPEG4 encoder compliant with ISO/IEC 14496-2 (MPEG4 Part 2 2001) @ simple profile, D1 15fps

Audio codec

- Wavetable synthesis up to 64 tones
- Support AAC/AAC+ decoding,
- PCM record and playback
- Digital audio playback
- MPEG1 audio layer3, MPEG2 low sampling rate extension layer3, MPEG 2.5 layer3
- MIDI
- AMR-NB
- DRA
- WMA

1.3 Applications

SC6820 provides a single-chip baseband solution for GSM/GPRS/EDGE dual-mode wireless telephone handsets and data modems conforming to the GSM/GPRS (Release 1999, GSM850, GSM900, DCS1800 and PCS1900, quad-band).

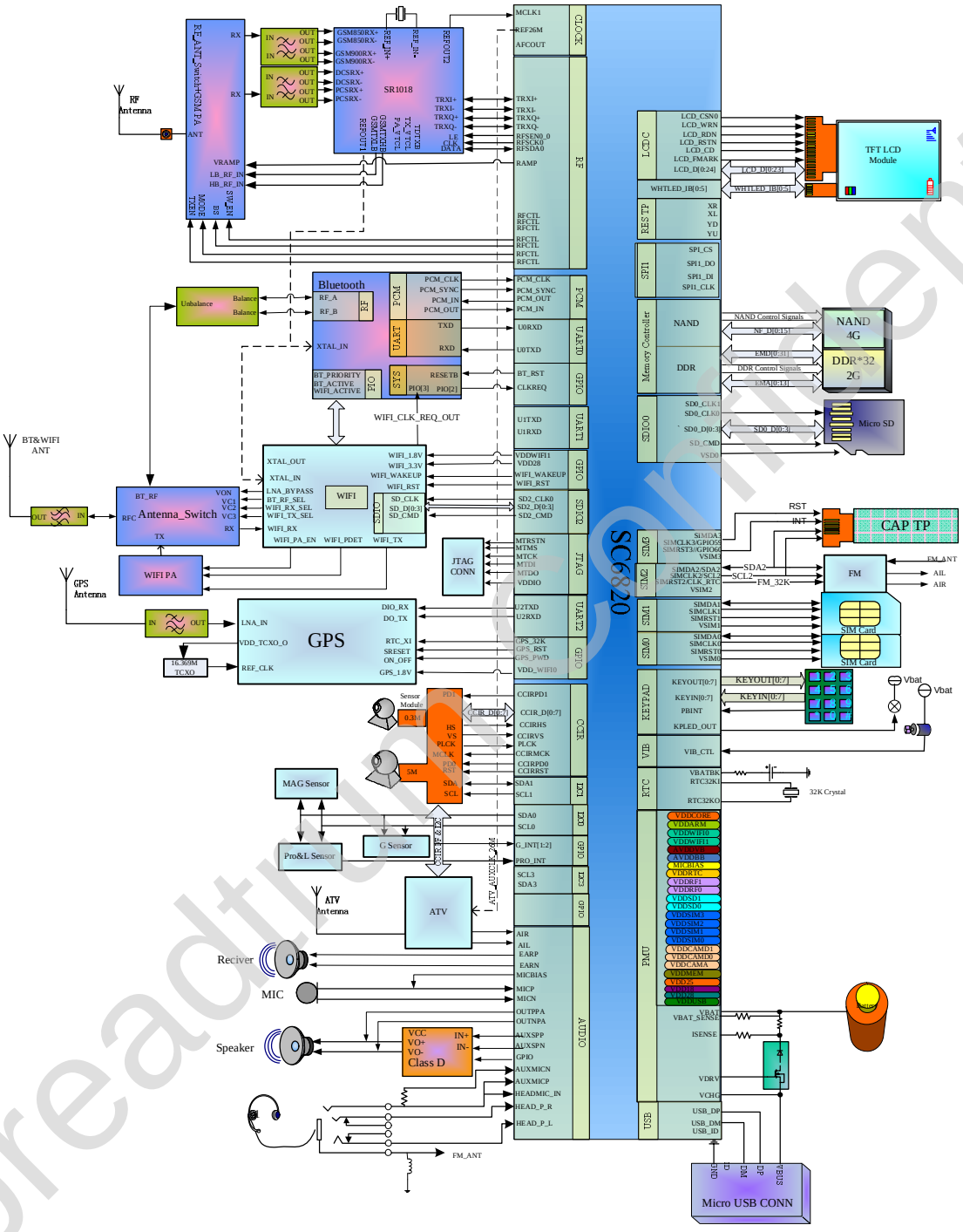


Figure 1-1 A typical application diagram of SC6820

1.4 Chip Architecture

Figure 1-2 shows the chip-level functional block diagram of SC6820. This chip architecture is based on two processor subsystems, an MCU and a DSP, and other functional blocks are connected to one or both of the buses and provide various hardware accelerations and interfaces to other components in the system.

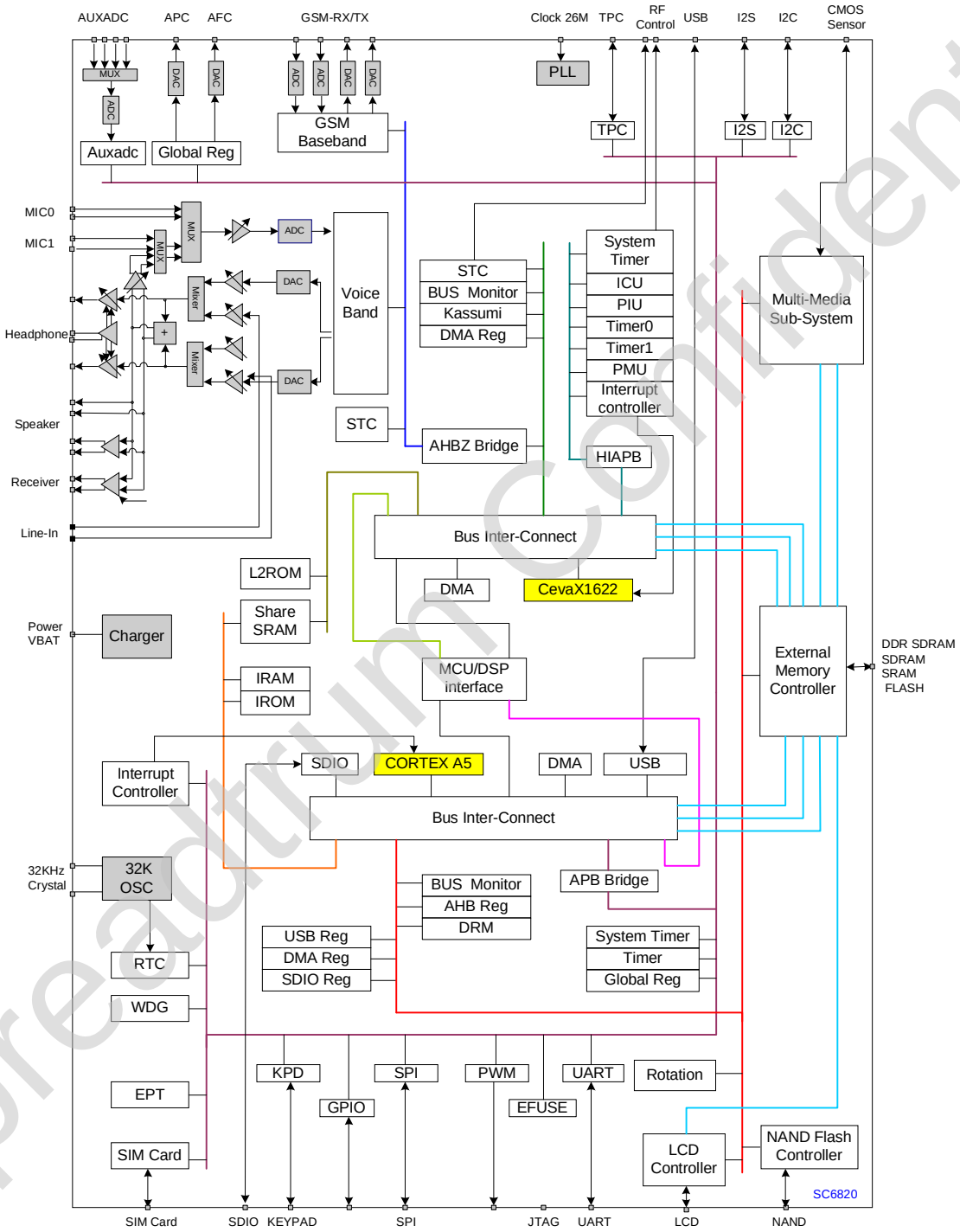


Figure 1-2 SC6820 chip-level functional block diagram

2 Package Information

Plastic-encapsulated surface mount packages are sensitive to damage induced by absorbed moisture and temperature. ALL the SC6820 chips are MSL 3, which had been marked on the label for every package.

2.1 Top Marking Definition

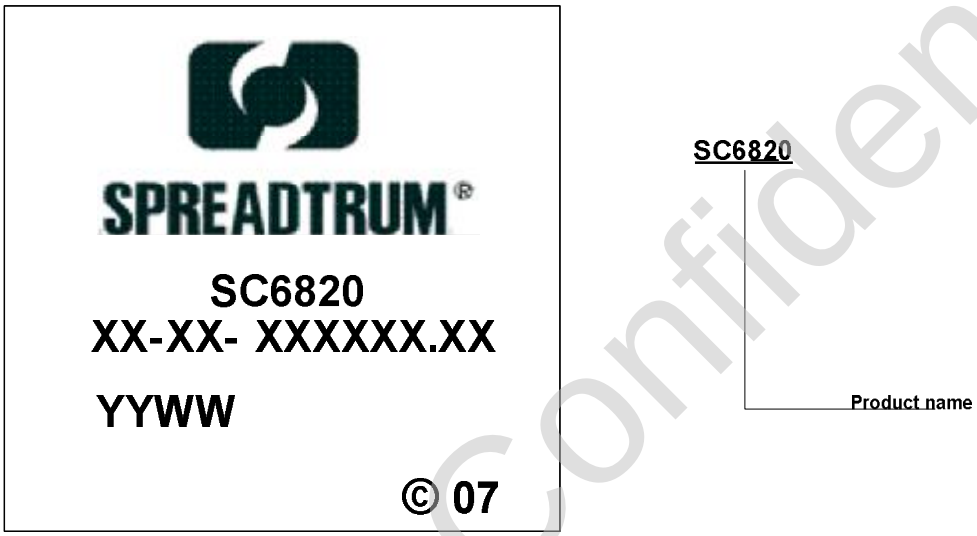
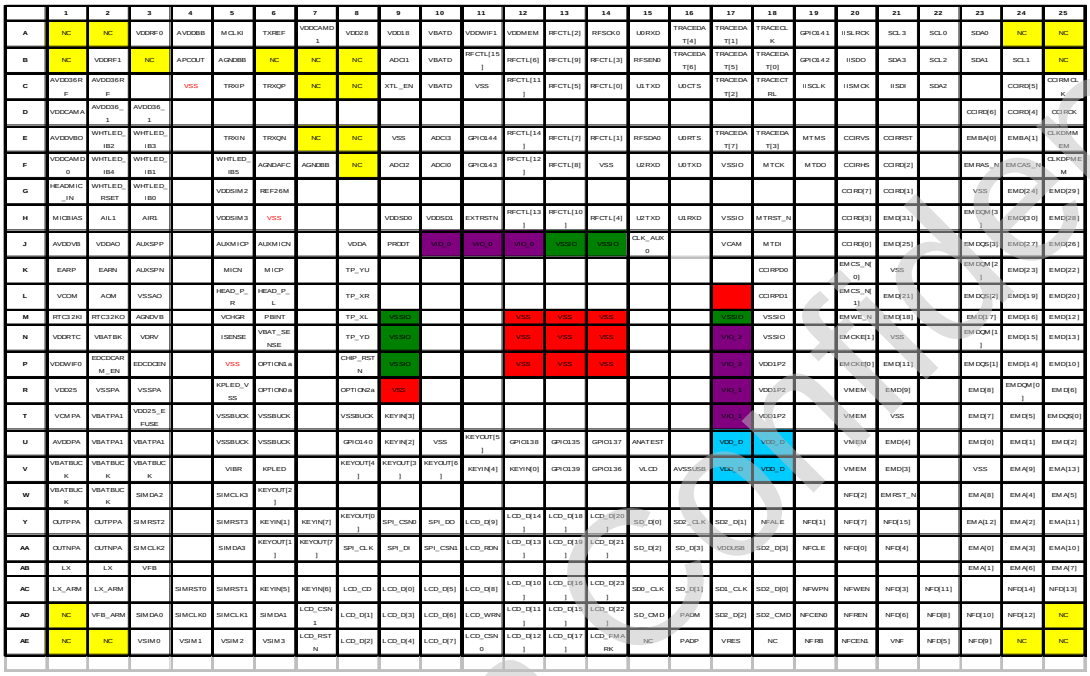


Figure 2-1 Top marking definition

2.2 LFBGA Pinout



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	NC	NC	VDDRF0	AVDD88	MCLKI	TXREF	VDDCAMD1	VDD28	VDD18	VBATD	VDDWIF1	VDDMEM	RFCTL[2]	RFSCK0	U0RXD	TRACEDAT[4]	TRACEDAT[1]	TRACECLK	GPIO141	ISLRCK	SCL3	SCL0	SDA0	NC	NC
B	NC	VDDRF1	NC	APCOUT	AGND88	NC	NC	NC	ADCI1	VBATD	RFCTL[15]	RFCTL[6]	RFCTL[9]	RFCTL[3]	RFSEN0	TRACEDAT[6]	TRACEDAT[5]	TRACEDAT[0]	GPIO142	IISDO	SDA3	SCL2	SDA1	SCL1	NC
C	AVDD36RF	AVDD36RF		VSS	TRXIP	TRXQP	NC	NC	XTL_EN	VBATD	VSS	RFCTL[11]	RFCTL[5]	RFCTL[0]	U1TXD	U0CTS	TRACEDAT[2]	TRACECTRL	IISCLK	IISMCK	IISDI	SDA2		CORD[5]	CORMCLK
D	VDDCAMA	AVDD36_1	AVDD36_1																				CORD[6]	CORD[4]	CORCK
E	AVDDVBO	WHTLED_IB2	WHTLED_IB3		TRXN	TRXQN	NC	NC	VSS	ADCI3	GPIO144	RFCTL[14]	RFCTL[7]	RFCTL[1]	RFSDA0	U0RTS	TRACEDAT[7]	TRACEDAT[3]	MTMS	CCIRVS	CCIRRST		EMBA[0]	EMBA[1]	CLKDIVMEM
F	VDDCAMD0	WHTLED_IB4	WHTLED_IB1		WHTLED_IB5	AGNDAFC	AGND88	NC	ADCI2	ADCI0	GPIO143	RFCTL[12]	RFCTL[8]	VSS	U2RXD	U0TXD	VSSIO	MTCK	MTDO	CCIRHS	CCIRD[2]		EMRAS_N	EMCAS_N	CLKDPMEM
G	HEADMIC_IN	WHTLED_RSET	WHTLED_IB0		VDDSIM2	REF26M						RFCTL[13]	RFCTL[10]	RFCTL[4]	U2TXD	U1RXD	VSSIO	MTRST_N		CCIRD[7]	CCIRD[1]		VSS	EMD[24]	EMD[29]
H	MICBIAS	AIL1	AIR1		VDDSIM3	VSS			VDDSD0	VDDSD1	EXTRSTN	RFCTL[13]	RFCTL[10]	RFCTL[4]	U2TXD	U1RXD	VSSIO	MTRST_N		CCIRD[3]	EMD[31]		EMDQM[3]	EMD[30]	EMD[28]
J	AVDDVB	VDDAO	AUXSPIP		AUXMICP	AUXMICN		VDDA	PRDDT	VIO_0	VIO_0	VIO_0	VSSIO	VSSIO	CLK_AUX0		VCAM	MTDI		CCIRD[0]	EMD[25]		EMDQS[3]	EMD[27]	EMD[26]
K	EARP	EARN	AUXSPIN		MICN	MICP		TP_YU												EMCS_N[0]	VSS		EMDQM[2]	EMD[23]	EMD[22]
L	VCOM	AOM	VSSAO		HEAD_PR	HEAD_PL		TP_XR										CCIRPD1		EMCS_N[1]	EMD[21]		EMDQS[2]	EMD[19]	EMD[20]
M	RTC32KI	RTC32KO	AGNDVB		VCHGI	PBINT		TP_XL	VSSIO			VSS	VSS	VSS			VSSIO	VSSIO		EMWE_N	EMD[18]		EMD[17]	EMD[16]	EMD[12]
N	VDDRTC	VBATBK	VDRV		ISENSE	VBAT_SENSE		TP_YD	VSSIO			VSS	VSS	VSS			VIO_2	VSSIO		EMCKE[1]	VSS		EMDQM[1]	EMD[15]	EMD[13]
P	VDDWIF0	EDCDCAR M_EN	EDCDCEN		VSS	OPTION1a		CHIP_RSTN	VSSIO			VSS	VSS	VSS			VIO_2	VDD12		EMCKE[0]	EMD[11]		EMDQS[1]	EMD[14]	EMD[10]
R	VDD25	VSSPA	VSSPA		XPLED_VSS	OPTION2a		OPTION2a	VSS								VIO_1	VDD12		VMEM	EMD[9]		EMD[8]	EMDQM[0]	EMD[6]
T	VCMPA	VBATPA1	VDD25_EFUSE		VSSBUCK	VSSBUCK		VSSBUCK	KEYIN[3]								VIO_1	VDD12		VMEM	VSS		EMD[7]	EMD[5]	EMDQS[0]
U	AVDDPA	VBATPA1	VBATPA1		VSSBUCK	VSSBUCK		GPIO140	KEYIN[2]	VSS	KEYOUT[5]	GPIO138	GPIO135	GPIO137	ANATEST		VDD_D	VDD_D		VMEM	EMD[4]		EMD[0]	EMD[1]	EMD[2]
V	VBATBUCK	VBATBUCK	VBATBUCK		VIBR	KPLED		KEYOUT[4]	KEYOUT[3]	KEYOUT[6]	KEYIN[4]	KEYIN[0]	GPIO139	GPIO136	VLCD	AVSSDSP	VDD_D	VDD_D		VMEM	EMD[3]		VSS	EMA[9]	EMA[13]
W	VBATBUCK	VBATBUCK	SIMDA2		SIMCLK3	KEYOUT[2]														NFD[2]	EMRST_N		EMA[8]	EMA[4]	EMA[5]
Y	OUTPPA	OUTPPA	SIMRST2		SIMRST3	KEYIN[1]	KEYIN[7]	KEYOUT[0]	SPI_CSN0	SPI_D0	LCD_D[9]	LCD_D[14]	LCD_D[18]	LCD_D[20]	SD_D[0]	SD2_CLK	SD2_D[1]	NFALE	NFD[1]	NFD[7]	NFD[15]		EMA[12]	EMA[2]	EMA[11]
AA	OUTNPA	OUTNPA	SIMCLK2		SIMDA3	KEYOUT[1]	KEYOUT[7]	SPI_CLK	SPI_DI	SPI_CSN1	LCD_RDN	LCD_D[13]	LCD_D[19]	LCD_D[21]	SD_D[2]	SD_D[3]	VDDUSB	SD2_D[3]	NFCLE	NFD[0]	NFD[4]		EMA[0]	EMA[3]	EMA[10]
AB	LX	LX	VFB																				EMA[1]	EMA[6]	EMA[7]
AC	LX_ARM	LX_ARM		SIMRST0	SIMRST1	KEYIN[5]	KEYIN[6]	LCD_CD	LCD_D[0]	LCD_D[5]	LCD_D[8]	LCD_D[10]	LCD_D[16]	LCD_D[23]	SD0_CLK	SD_D[1]	SD1_CLK	SD2_D[0]	NFWPN	NFWEN	NFD[3]	NFD[11]		NFD[14]	NFD[13]
AD	NC	VFB_ARM	SIMDA0	SIMCLK0	SIMCLK1	SIMDA1	LCD_CSN1	LCD_D[1]	LCD_D[3]	LCD_D[6]	LCD_WRN	LCD_D[11]	LCD_D[15]	LCD_D[22]	SD_CMD	PADM	SD2_D[2]	SD2_CMD	NFCEN0	NFREN	NFD[6]	NFD[8]	NFD[10]	NFD[12]	NC
AE	NC	NC	VSIM0	VSIM1	VSIM2	VSIM3	LCD_RSTN	LCD_D[2]	LCD_D[4]	LCD_D[7]	LCD_CSN0	LCD_D[12]	LCD_D[17]	LCD_FMARK	NC	PADP	VRES	NC	NFRB	NFCEN1	VNF	NFD[5]	NFD[9]	NC	NC

Figure 2-2 454-ball LFBGA pinout

2.3 Package Outline

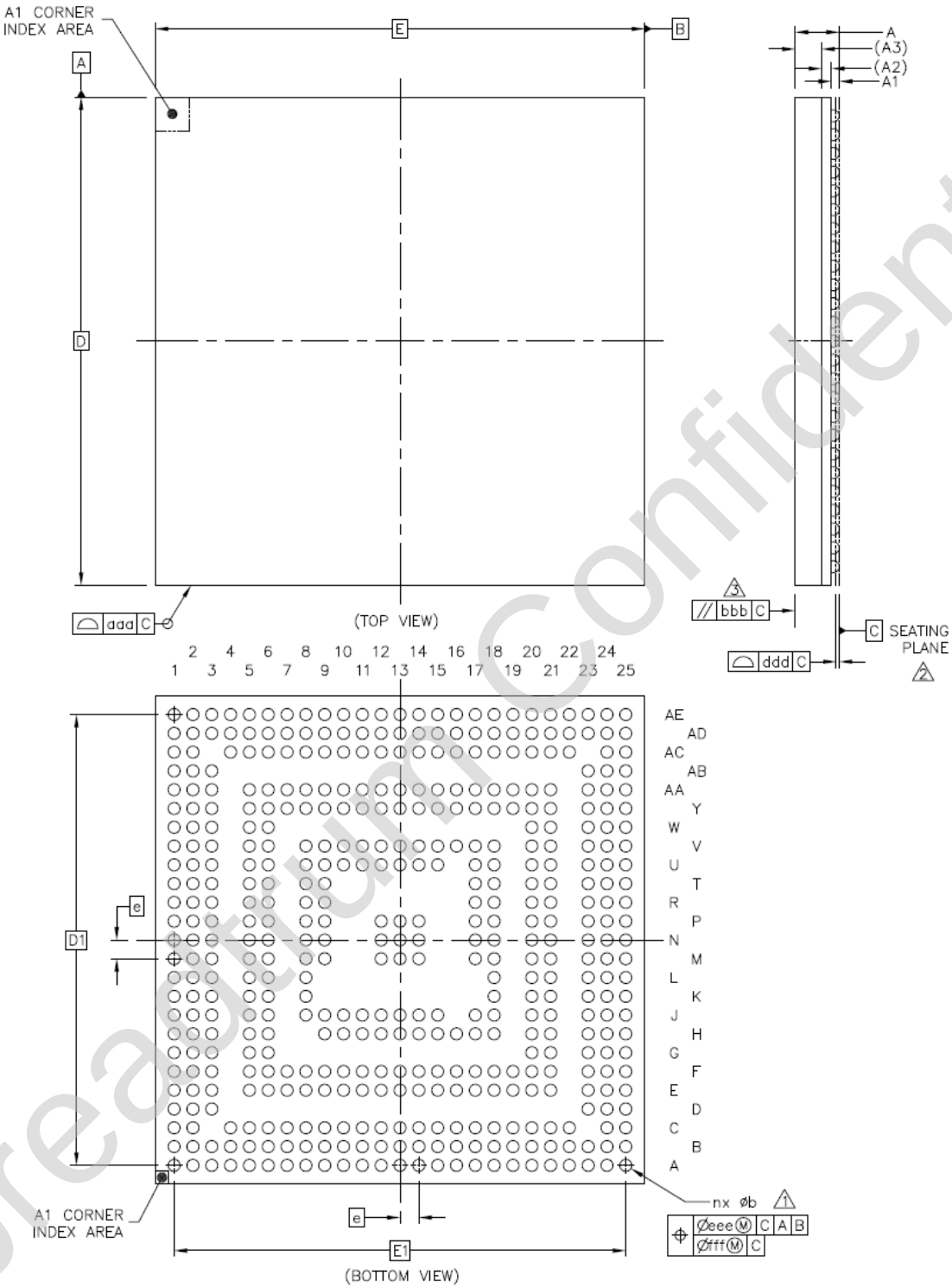


Figure 2-3 Package outline

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.3
STAND OFF	A1	0.16	---	0.26
SUBSTRATE THICKNESS	A2		0.26 REF	
MOLD THICKNESS	A3		0.7 REF	
BODY SIZE	D		13 BSC	
	E		13 BSC	
BALL DIAMETER			0.3	
BALL OPENING			0.275	
BALL WIDTH	b	0.27	---	0.37
BALL PITCH	e		0.5 BSC	
BALL COUNT	n		454	
EDGE BALL CENTER TO CENTER	D1		12 BSC	
	E1		12 BSC	
BODY CENTER TO CONTACT BALL	SD		--- BSC	
	SE		--- BSC	
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

Figure 2-4 Package parameters

2.4 Reflow Profile

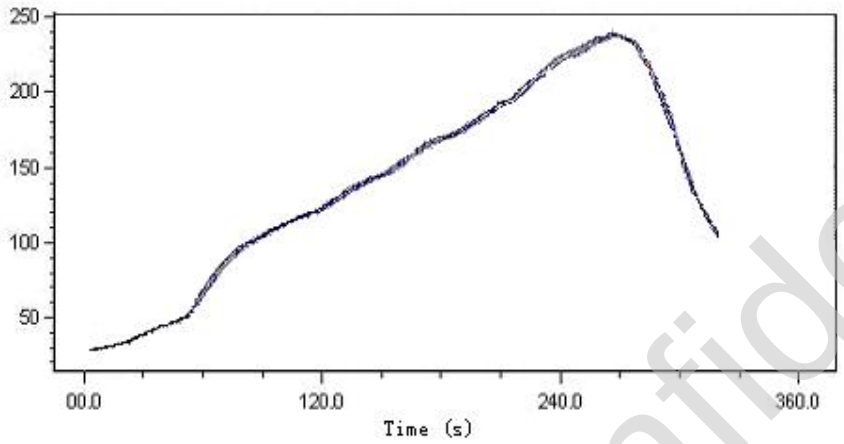


Figure 2-5 Reflow profile

Note:

1. Recommended reflow profile for lead-free solder paste
   - ¡ Ramp at 1-2°C per second to 245+/-5°C
   - ¡ Dwell at 235°C for 10 seconds
   - ¡ Dwell at 217°C for 30~60s
   - ¡ Total reflow time is about 220~270 s
   - ¡ Cold down ramp < 4°C/s
2. Recommended solder paste type
   - ¡ SnAgCu solder paste
   - ¡ Metal contents should be about 88.5%
3. Recommended parameter for stencil making
   - ¡ Metal mask thickness: 5 mils
   - ¡ Opening area ratio: 100%

3 Pin Information

3.1.1 Pin symbol descriptions

The following table explains the symbols used in the pin lists.

Table 3-1 Definition of pin symbols

Field	Symbol	Type Description
Pin Type	I	Digital input
	O	Digital output
	O/T	Digital output with tri-state option
	I/O	Digital bi-directional pin
	I/O/T	Digital bi-directional pin with tri-state option
	PI	Power pin, input from external power supply
	PIO	Power pin, input from external or floating to use internal LDO power supply
	PO	Power pin, output for external devices
	G	Ground pin
	AI	Analog input pin
	AO	Analog output pin
	AIO	Analog bi-directional pin
Pin Value	IPU	Input with pull-up
	IPD	Input with pull-down
	OH	Output “1”
	OL	Output “0”
	Z	Tri-state
Power	VBAT	Battery power supply input
	VDD_D /VDD1P2	Power supply for core and ARM, the internal power source are DCDC for CORE and DCDC for ARM
	VIO /VIO_1 /VIO_2	Power supply for I/O, the internal power source is VDD18 or VDD28
	VMEM	Power supply for SRAM/SDRAM memories, the internal power source is VDDMEM
	VCAM	Power supply for Digital Camera, the internal power source is VDDCARM0 or VDDCARM1 or VDDCARMA
	VNF	Power supply for NAND flash and LCM, the internal power source is VDD28 or VDD18
	VSIM0 /VSIM1 /VSIM2	Power supply for SIM card 0 1 2 3, the internal power source are LDO_SIM0 LDO_SIM1 LDO_SIM2 and LDO_SIM3

Field	Symbol	Type Description
	/VSIM3	
	VDDRF0 /VDDRF1	Power supply for RF , the internal power source are VDDRF0/VDDRF1
	VDDRTC	Power supply for RTC
	VDDUSB	Power supply for USB
	VDD25	Power supply for PLL and Efuse
	VSD	Power supply for SD card , the internal power source is VDDSD0 or VDDSD1
	AVDDBB	Analog base-band RX/TX power supply, the internal power source is AVDDBB
	AVDDVB	Analog voice-band power supply , the internal power source is AVDDVB
	VDDWIF0 /VDDWIF1	Power supply for external Wif or other application
	VDD_A	Supply for 26MHz buffer and pLL

3.1.2 Pin List

Table 3-2 Pin List

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
Clock & Reset Interface (3 Pins)							
C9	SPBC2_24X	XTL_EN	O	VIO_2	Ie=0, oe=1, 1	ie=0, oe=1, 1	External Crystal Enable
P8	SPBC2_24X_S	CHIP_RSTN	I	VIO	Ie=1, oe=0	Ie=1, oe=0	
M6	SPSOS2_24X_H	PBINT	I	VIO	Ie=1, oe=0	Ie=1, oe=0	
Production Test Interface (1 Pins)							
J9	SPPAD3_S	PRODT		VIO			
GPIO Interface (10 Pins)							
U13	SPBC2_24X	GPIO135	I/O	VIO_1	Ie=0, oe=1, 0	ie=1, oe=0	
V14	SPBC2_24X	GPIO136	I/O	VIO_1	ie=0, oe=1, 0	ie=1, oe=0	
U14	SPBC2_24X	GPIO137	I/O	VIO_1	ie=0, oe=1, 0	ie=1, oe=0	
U12	SPBC2_24X	GPIO138	I/O	VIO_1	ie=0, oe=1, 0	ie=1, oe=0	
V13	SPBC2_24X	GPIO139	I/O	VIO_1	ie=0, oe=1, 0	ie=1, oe=0	
U8	SPBC2_24X	GPIO140	I/O	VIO_1	ie=0,	ie=1, oe=0	

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
					oe=1, 0		
A19	SPBC2_24X	GPIO141	I/O	VIO_2	ie=0, oe=1, 0	ie=1, oe=0	
B19	SPBC2_24X	GPIO142	I/O	VIO_2	ie=0, oe=1, 0	ie=1, oe=0	
F11	SPBC2_24X	GPIO143	I/O	VIO_2	ie=0, oe=1, 0	ie=1, oe=0	
E11	SPBC2_24X	GPIO144	I/O	VIO_2	ie=0, oe=1, 0	ie=1, oe=0	
SIM0 Interface (3 Pins)							
AD4	SPCBC2_24X	SIMCLK0	O	VSIM0	ie=0, oe=1, 0	ie=0, oe=1, 0	
AD3	SPSBC2_24X	SIMDA0	I/O/T	VSIM0	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
AC4	SPCBC2_24X	SIMRST0	O	VSIM0	ie=0, oe=1, 0	ie=0, oe=1, 0	
SIM1 Interface (3 Pins)							
AD5	SPCBC2_24X	SIMCLK1	O	VSIM1	ie=0, oe=1, 0	ie=0, oe=1, 0	
AD6	SPSBC2_24X	SIMDA1	I/O/T	VSIM1	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
AC5	SPCBC2_24X	SIMRST1	O	VSIM1	ie=0, oe=1, 0	ie=0, oe=1, 0	
SIM2 Interface (3 Pins)							
AA3	SPCBC2_24X	SIMCLK2	O	VSIM2	ie=0, oe=1, 0	ie=0, oe=1, 0	
W3	SPSBC2_24X	SIMDA2	I/O/T	VSIM2	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
Y3	SPCBC2_24X	SIMRST2	O	VSIM2	ie=0, oe=1, 0	ie=0, oe=1, 0	
SIM3 Interface (3 Pins)							
W5	SPCBC2_24X	SIMCLK3	O	VSIM3	ie=0, oe=1, 0	ie=0, oe=1, 0	
AA5	SPSBC2_24X	SIMDA3	I/O/T	VSIM3	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
Y5	SPCBC2_24X	SIMRST3	O	VSIM3	ie=0, oe=1, 0	ie=0, oe=1, 0	
SDIO Interface (7 Pins)							
AC15	SPCBC2_24X	SD0_CLK	I/O/T	VSD	ie=0, oe=1, 0	ie=0, oe=1, 0	
AD15	SPCBC2_24X	SD_CMD	I/O/T	VSD	ie=1, oe=0,wpu	ie=1, oe=0,wpu	
Y15	SPCBC2_24X	SD_D[0]	I/O/T	VSD	ie=1, oe=0,wpu	ie=1, oe=0,wpu	

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
AC16	SPCBC2_24X	SD_D[1]	I/O/T	VSD	ie=1, oe=0,wpu	ie=1, oe=0,wpu	
AA15	SPCBC2_24X	SD_D[2]	I/O/T	VSD	ie=1, oe=0,wpu	ie=1, oe=0,wpu	
AA16	SPCBC2_24X	SD_D[3]	I/O/T	VSD	ie=1, oe=0,wpu	ie=1, oe=0,wpu	
AC17	SPCBC2_24X	SD1_CLK	I/O/T	VSD	ie=0, oe=1, 0	ie=0, oe=1, 0	
SDIO2 Interface (6 Pins)							
Y16	SPCBC2_24X	SD2_CLK	I/O/T	VSD2	ie=0, oe=1, 0	ie=0, oe=1, 0	
AD18	SPCBC2_24X	SD2_CMD	I/O/T	VSD2	ie=1, oe=0,wpu	ie=1, oe=0,wpu	
AC18	SPCBC2_24X	SD2_D[0]	I/O/T	VSD2	ie=1, oe=0,wpu	ie=1, oe=0,wpu	
Y17	SPCBC2_24X	SD2_D[1]	I/O/T	VSD2	ie=1, oe=0,wpu	ie=1, oe=0,wpu	
AD17	SPCBC2_24X	SD2_D[2]	I/O/T	VSD2	ie=1, oe=0,wpu	ie=1, oe=0,wpu	
AA18	SPCBC2_24X	SD2_D[3]	I/O/T	VSD2	ie=1, oe=0,wpu	ie=1, oe=0,wpu	
Keypad Interface (16 Pins)							
Y8	SPCBC2_24X	KEYOUT[0]	O/T	VIO_1	ie= oe=0	ie= oe=0	
AA6	SPCBC2_24X	KEYOUT[1]	O/T	VIO_1	ie= oe=0	ie= oe=0	
W6	SPCBC2_24X	KEYOUT[2]	O/T	VIO_1	ie= oe=0	ie= oe=0	
V9	SPCBC2_24X	KEYOUT[3]	O/T	VIO_1	ie= oe=0	ie= oe=0	
V8	SPCBC2_24X	KEYOUT[4]	O/T	VIO_1	ie= oe=0	ie= oe=0	
U11	SPCBC2_24X	KEYOUT[5]	O/T	VIO_1	ie= oe=0	ie= oe=0	
V10	SPCBC2_24X	KEYOUT[6]	O/T	VIO_1	ie= oe=0	ie= oe=0	
AA7	SPCBC2_24X	KEYOUT[7]	O/T	VIO_1	ie= oe=0	ie= oe=0	
V12	SPCBC2_24X	KEYIN[0]	I	VIO_1	ie= oe=0	ie=1, oe=0, wpu	
Y6	SPCBC2_24X	KEYIN[1]	I	VIO_1	ie=1, oe=0, wpd	ie=1, oe=0, wpu	
U9	SPCBC2_24X	KEYIN[2]	I	VIO_1	ie= oe=0	ie=1, oe=0, wpu	
T9	SPCBC2_24X	KEYIN[3]	I	VIO_1	ie= oe=0	ie=1, oe=0, wpu	
V11	SPCBC2_24X	KEYIN[4]	I	VIO_1	ie= oe=0	ie=1, oe=0, wpu	
AC6	SPCBC2_24X	KEYIN[5]	I	VIO_1	ie= oe=0	ie=1, oe=0, wpu	
AC7	SPCBC2_24X	KEYIN[6]	I	VIO_1	ie= oe=0	ie=1, oe=0, wpu	
Y7	SPCBC2_24X	KEYIN[7]	I	VIO_1	ie= oe=0	ie=1, oe=0, wpu	
SPI Interface (5 Pins)							
AA9	SPBC2_24X	SPI_DI	I	VIO_1	ie=1, oe=0,wpu	ie=1, oe=0,wpu	
AA8	SPBC2_24X	SPI_CLK	I/O	VIO_1	ie=0,	ie=0, oe=1, 0	

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
					oe=1, 0		
Y10	SPBC2_24X	SPI_DO	I/O	VIO_1	ie=0, oe=1, 0	ie=0, oe=1, 0	
Y9	SPBC2_24X	SPI_CSN0	O/T	VIO_1	ie=0, oe=1, 1	ie=0, oe=1, 1	
AA10	SPBC2_24X	SPI_CSN1	O/T	VIO_1	ie=0, oe=1, 1	ie=0, oe=1, 1	
JTAG Interface (5 Pins)							
F19	SPCBC2_24X	MTDO	O/T	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
J18	SPCBC2_24X	MTDI	I	VIO_2	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
F18	SPCBC2_24X	MTCK	I	VIO_2	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
E19	SPCBC2_24X	MTMS	I	VIO_2	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
H18	SPCBC2_24X	MTRST_N	I	VIO_2	ie=1, oe=0, wpd	ie=1, oe=0, wpd	
UART0 Interface (4 Pins)							
F16	SPCBC2_24X	U0TXD	O	VIO_2	ie=0, oe=1, 1	ie=0, oe=1, 1	
A15	SPCBC2_24X	U0RXD	I	VIO_2	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
C16	SPCBC2_24X	U0CTS	I	VIO_2	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
E16	SPCBC2_24X	U0RTS	O	VIO_2	ie=0, oe=1, 1	ie=0, oe=1, 1	
UART1 Interface (2 Pins)							
C15	SPCBC2_24X	U1TXD	O	VIO_2	ie=1, oe=0, wpu	ie=0, oe=1, 1	
H16	SPCBC2_24X	U1RXD	I	VIO_2	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
UART2 Interface (2 Pins)							
H15	SPCBC2_24X	U2TXD	O	VIO_2	ie=1, oe=0, wpu	ie=0, oe=1, 1	
F15	SPCBC2_24X	U2RXD	I	VIO_2	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
LCD Interface (31 Pins)							
AD7	SPCBC2_24X	LCD_CSN1	O	VLCD	ie=0,	ie=0, oe=1, 1	

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
					oe=1, 1		
AE7	SPCBC2_24X	LCD_RSTN	O	VLCD	ie=0, oe=1, 0	ie=0, oe=1, 1	
AC8	SPCBC2_24X	LCD_CD	O	VLCD	ie=0, oe=1, 0	ie=0, oe=1, 0	
AC9	SPCBC2_24 X	LCD_D[0]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AD8	SPCBC2_24X	LCD_D[1]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AE8	SPCBC2_24X	LCD_D[2]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AD9	SPCBC2_24X	LCD_D[3]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AE9	SPCBC2_24X	LCD_D[4]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AC10	SPCBC2_24X	LCD_D[5]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AD10	SPCBC2_24X	LCD_D[6]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AE10	SPCBC2_24X	LCD_D[7]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AC11	SPCBC2_24X	LCD_D[8]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AD11	SPCBC2_24X	LCD_WRN	O	VLCD	ie=0, oe=1,1	ie=0, oe=1,1	
AA11	SPCBC2_24X	LCD_RDN	O	VLCD	ie=0, oe=1,1	ie=0, oe=1,1	
AE11	SPCBC2_24X	LCD_CSN0	O	VLCD	ie=0, oe=1,1	ie=0, oe=1,1	
Y11	SPCBC2_24X	LCD_D[9]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AC12	SPCBC2_24X	LCD_D[10]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AD12	SPCBC2_24X	LCD_D[11]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AE12	SPCBC2_24X	LCD_D[12]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AA12	SPCBC2_24X	LCD_D[13]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
Y12	SPCBC2_24X	LCD_D[14]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AD13	SPCBC2_24X	LCD_D[15]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AC13	SPCBC2_24X	LCD_D[16]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AE13	SPCBC2_24X	LCD_D[17]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
Y13	SPCBC2_24X	LCD_D[18]	I/O	VLCD	ie=1,	ie=1, oe=0	

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
					oe=0		
AA13	SPCBC2_24X	LCD_D[19]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
Y14	SPCBC2_24X	LCD_D[20]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AA14	SPCBC2_24X	LCD_D[21]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AD14	SPCBC2_24X	LCD_D[22]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AC14	SPCBC2_24X	LCD_D[23]	I/O	VLCD	ie=1, oe=0	ie=1, oe=0	
AE14	SPCBC2_24X	LCD_FMARK	I	VLCD	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
Nand Interface (24 Pins)							
AC19	SPBC2_24X	NFWPN	O	VNF	ie=0, oe=1, 0	ie=0, oe=1, 0	
AE19	SPCBC2_24X	NFRB	I	VNF	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
AA19	SPBC2_24X	NFCLE	O	VNF	ie=0, oe=1, 0	ie=0, oe=1, 0	
Y18	SPBC2_24X	NFALE	O	VNF	ie=0, oe=1, 0	ie=0, oe=1, 0	
AD19	SPBC2_24X	NFCEN0	O	VNF	ie=0, oe=1, 1	ie=0, oe=1, 1	
AE20	SPBC2_24X	NFCEN1	O	VNF	ie=0, oe=1, 1	ie=0, oe=1, 1	
AD20	SPBC2_24X	NFREN	O	VNF	ie=0, oe=1, 1	ie=0, oe=1, 1	
AC20	SPBC2_24X	NFWEN	O	VNF	ie=0, oe=1, 1	ie=0, oe=1, 1	
AA20	SPBC2_24X	NFD[0]	I/O	VNF	ie=1, oe=0, wpu	ie=1, oe=0	
Y19	SPBC2_24X	NFD[1]	I/O	VNF	ie=1, oe=0, wpu	ie=1, oe=0	
W20	SPBC2_24X	NFD[2]	I/O	VNF	ie=1, oe=0,wpu	ie=1, oe=0	
AC21	SPBC2_24X	NFD[3]	I/O	VNF	ie=1, oe=0,wpu	ie=1, oe=0	
AA21	SPBC2_24X	NFD[4]	I/O	VNF	ie=1, oe=0,wpu	ie=1, oe=0	
AE22	SPBC2_24X	NFD[5]	I/O	VNF	ie=1, oe=0	ie=1, oe=0	
AD21	SPBC2_24X	NFD[6]	I/O	VNF	ie=1, oe=0	ie=1, oe=0	
Y20	SPBC2_24X	NFD[7]	I/O	VNF	ie=1,	ie=1, oe=0	

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
					oe=0		
AD22	SPBC2_24X	NFD[8]	I/O	VNF	ie=1, oe=0	ie=1, oe=0	
AE23	SPBC2_24X	NFD[9]	I/O	VNF	ie=1, oe=0	ie=1, oe=0	
AD23	SPBC2_24X	NFD[10]	I/O	VNF	ie=1, oe=0	ie=1, oe=0	
AC22	SPBC2_24X	NFD[11]	I/O	VNF	ie=1, oe=0	ie=1, oe=0	
AD24	SPBC2_24X	NFD[12]	I/O	VNF	ie=1, oe=0	ie=1, oe=0	
AC25	SPBC2_24X	NFD[13]	I/O	VNF	ie=1, oe=0	ie=1, oe=0	
AC24	SPBC2_24X	NFD]14]	I/O	VNF	ie=1, oe=0	ie=1, oe=0	
Y21	SPBC2_24X	NFD[15]	I/O	VNF	ie=1, oe=0	ie=1, oe=0	
EMC Interface (66 Pins)							
W21	SPBC2_24X_18	EMRST_N	O	VMEM	ie=0, oe=1, 0	oe=1, ie=0, 1	
AA23	SPBC2_24X_18	EMA[0]	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
AB23	SPBC2_24X_18	EMA[1]	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
Y24	SPBC2_24X_18	EMA[2]	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
AA24	SPBC2_24X_18	EMA[3]	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
W24	SPBC2_24X_18	EMA[4]	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
W25	SPBC2_24X_18	EMA[5]	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
AB24	SPBC2_24X_18	EMA[6]	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
AB25	SPBC2_24X_18	EMA[7]	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
W23	SPBC2_24X_18	EMA[8]	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
V24	SPBC2_24X_18	EMA[9]	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
AA25	SPBC2_24X_18	EMA[10]	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
Y25	SPBC2_24X_18	EMA[11]	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
Y23	SPBC2_24X_18	EMA[12]	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
V25	SPBC2_24X_18	EMA[13]	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
U23	SPBC2_24X_18	EMD[0]	I/O	VMEM	ie=oe=0	ie=oe=0	
U24	SPBC2_24X_18	EMD[1]	I/O	VMEM	ie=oe=0	ie=oe=0	
U25	SPBC2_24X_18	EMD[2]	I/O	VMEM	ie=oe=0	ie=oe=0	
V21	SPBC2_24X_18	EMD[3]	I/O	VMEM	ie=oe=0	ie=oe=0	
U21	SPBC2_24X_18	EMD[4]	I/O	VMEM	ie=oe=0	ie=oe=0	
T24	SPBC2_24X_18	EMD[5]	I/O	VMEM	ie=oe=0	ie=oe=0	
R25	SPBC2_24X_18	EMD[6]	I/O	VMEM	ie=oe=0	ie=oe=0	
T23	SPBC2_24X_18	EMD[7]	I/O	VMEM	ie=oe=0	ie=oe=0	
R24	SPBC2_24X_18	EMDQM[0]	O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
T25	SPBC2_24X_18	EMDQS[0]	I/O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
R23	SPBC2_24X_18	EMD[8]	I/O	VMEM	ie=oe=0	ie=oe=0	
R21	SPBC2_24X_18	EMD[9]	I/O	VMEM	ie=oe=0	ie=oe=0	
P25	SPBC2_24X_18	EMD[10]	I/O	VMEM	ie=oe=0	ie=oe=0	
P21	SPBC2_24X_18	EMD[11]	I/O	VMEM	ie=oe=0	ie=oe=0	
M25	SPBC2_24X_18	EMD[12]	I/O	VMEM	ie=oe=0	ie=oe=0	
N25	SPBC2_24X_18	EMD[13]	I/O	VMEM	ie=oe=0	ie=oe=0	
P24	SPBC2_24X_18	EMD[14]	I/O	VMEM	ie=oe=0	ie=oe=0	
N24	SPBC2_24X_18	EMD[15]	I/O	VMEM	ie=oe=0	ie=oe=0	
N23	SPBC2_24X_18	EMDQM[1]	O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
P23	SPBC2_24X_18	EMDQS[1]	I/O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
M24	SPBC2_24X_18	EMD[16]	I/O	VMEM	ie=oe=0	ie=oe=0	
M23	SPBC2_24X_18	EMD[17]	I/O	VMEM	ie=oe=0	ie=oe=0	
N20	SPBC2_24X_18	EMCKE[1]	I/O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
M21	SPBC2_24X_18	EMD[18]	I/O	VMEM	ie=oe=0	ie=oe=0	
L24	SPBC2_24X_18	EMD[19]	I/O	VMEM	ie=oe=0	ie=oe=0	
L25	SPBC2_24X_18	EMD[20]	I/O	VMEM	ie=oe=0	ie=oe=0	
L21	SPBC2_24X_18	EMD[21]	I/O	VMEM	ie=oe=0	ie=oe=0	
K25	SPBC2_24X_18	EMD[22]	I/O	VMEM	ie=oe=0	ie=oe=0	
K24	SPBC2_24X_18	EMD[23]	I/O	VMEM	ie=oe=0	ie=oe=0	
K23	SPBC2_24X_18	EMDQM[2]	O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
L23	SPBC2_24X_18	EMDQS[2]	I/O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
G24	SPBC2_24X_18	EMD[24]	I/O	VMEM	ie=oe=0	ie=oe=0	
J21	SPBC2_24X_18	EMD[25]	I/O	VMEM	ie=oe=0	ie=oe=0	
J25	SPBC2_24X_18	EMD[26]	I/O	VMEM	ie=oe=0	ie=oe=0	

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
J24	SPBC2_24X_18	EMD[27]	I/O	VMEM	ie=oe=0	ie=oe=0	
H25	SPBC2_24X_18	EMD[28]	I/O	VMEM	ie=oe=0	ie=oe=0	
G25	SPBC2_24X_18	EMD[29]	I/O	VMEM	ie=oe=0	ie=oe=0	
H24	SPBC2_24X_18	EMD[30]	I/O	VMEM	ie=oe=0	ie=oe=0	
H21	SPBC2_24X_18	EMD[31]	I/O	VMEM	ie=oe=0	ie=oe=0	
H23	SPBC2_24X_18	EMDQM[3]	O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
J23	SPBC2_24X_18	EMDQS[3]	I/O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
F25	SPBC2_24X_18	CLKDPMEM	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
E25	SPBC2_24X_18	CLKDMMEM	O	VMEM	ie=0, oe=1, 0	ie=0, oe=1, 0	
F23	SPBC2_24X_18	EMRAS_N	O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
F24	SPBC2_24X_18	EMCAS_N	O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
M20	SPBC2_24X_18	EMWE_N	O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
K20	SPBC2_24X_18	EMCS_N[0]	O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
L20	SPBC2_24X_18	EMCS_N[1]	O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
E23	SPBC2_24X_18	EMBA[0]	O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
E24	SPBC2_24X_18	EMBA[1]	O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
P20	SPBC2_24X_18	EMCKE[0]	O	VMEM	ie=0, oe=1, 1	ie=0, oe=1, 1	
DCAM Interface (15 Pins)							
C25	SPCBC2_24X	CCIRMCLK	O	VCAM	ie=0, oe=1, 0	ie=0, oe=1, 0	
D25	SPCBC2_24X	CCIRCK	I	VCAM	ie=1, oe=0	ie=1, oe=0	
F20	SPCBC2_24X	CCIRHS	I	VCAM	ie=1, oe=0	ie=1, oe=0	
E20	SPCBC2_24X	CCIRVS	I	VCAM	ie=1, oe=0	ie=1, oe=0	
J20	SPCBC2_24X	CCIRD[0]	I	VCAM	ie=1, oe=0	ie=1, oe=0	
G21	SPCBC2_24X	CCIRD[1]	I	VCAM	ie=1, oe=0	ie=1, oe=0	
F21	SPCBC2_24X	CCIRD[2]	I	VCAM	ie=1, oe=0	ie=1, oe=0	
H20	SPCBC2_24X	CCIRD[3]	I	VCAM	ie=1, oe=0	ie=1, oe=0	

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
D24	SPCBC2_24X	CCIRD[4]	I	VCAM	ie=1, oe=0	ie=1, oe=0	
C24	SPCBC2_24X	CCIRD[5]	I	VCAM	ie=1, oe=0	ie=1, oe=0	
D23	SPCBC2_24X	CCIRD[6]	I	VCAM	ie=1, oe=0	ie=1, oe=0	
G20	SPCBC2_24X	CCIRD[7]	I	VCAM	ie=1, oe=0	ie=1, oe=0	
E21	SPCBC2_24X	CCIRRST	O	VCAM	ie=0, oe=1, 0	ie=0, oe=1, 1	
L18	SPCBC2_24X	CCIRPD1	O	VCAM	ie=0, oe=1, 1	ie=0, oe=1, 1	
K18	SPCBC2_24X	CCIRPD0	O	VCAM	ie=0, oe=1, 1	ie=0, oe=1, 1	
I2C Interface (8 Pins)							
A22	SPCBC2_24X	SCL0	I/O/T	VIO_2	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
A23	SPCBC2_24X	SDA0	I/O/T	VIO_2	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
B24	SPCBC2_24X	SCL1	I/O/T	VCAM	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
B23	SPCBC2_24X	SDA1	I/O/T	VCAM	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
B22	SPCBC2_24X	SCL2	I/O/T	VIO_2	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
C22	SPCBC2_24X	SDA2	I/O/T	VIO_2	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
A21	SPCBC2_24X	SCL3	I/O/T	VIO_2	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
B21	SPCBC2_24X	SDA3	I/O/T	VIO_2	ie=1, oe=0, wpu	ie=1, oe=0, wpu	
Aux Clock Interface (1 Pin)							
J15	SPBC2_24X	CLK_AUX0	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
IIS Interface (5 Pins)							
C21	SPBC2_24X	IISDI	O/T	VIO_2	ie=1, oe=0,wpd	ie=1, oe=0,wpd,fun_sel=1	
B20	SPBC2_24X	IISDO	I	VIO_2	ie=0, oe=0,	ie=0, oe=0,fun_sel=1	
C19	SPBC2_24X	IISCLK	I	VIO_2	ie=1, oe=0, wpd	ie=1, oe=0, wpd,fun_sel=1	

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
A20	SPBC2_24X	IISLRCK	I	VIO_2	ie=1, oe=0, wpd	ie=1, oe=0, wpd,fun_sel=1	
C20	SPBC2_24X	IISMCK	O	VIO_2	ie=1, oe=0, wpd	ie=1, oe=0, wpd,fun_sel=1	
TRACE port（10 Pins）							
A18	SPBC2_24X	TRACECLK	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
C18	SPBC2_24X	TRACECTRL	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
B18	SPBC2_24X	TRACEDAT[0]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
A17	SPBC2_24X	TRACEDAT[1]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
C17	SPBC2_24X	TRACEDAT[2]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
E18	SPBC2_24X	TRACEDAT[3]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
A16	SPBC2_24X	TRACEDAT[4]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
B17	SPBC2_24X	TRACEDAT[5]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
B16	SPBC2_24X	TRACEDAT[6]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
E17	SPBC2_24X	TRACEDAT[7]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
RF Interface (19 Pins)							
E15	SPBC2_24X	RFSDA0	I/O/T	VIO_2	ie=oe=0, wpd	ie=oe=0, wpd	
A14	SPBC2_24X	RFSCK0	O/T	VIO_2	ie=oe=0, wpd	ie=oe=0, wpd	
B15	SPBC2_24X	RFSEN0	O/T	VIO_2	ie=oe=0, wpu	ie=oe=0, wpu	
C14	SPBC2_24X	RFCTL[0]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
E14	SPBC2_24X	RFCTL[1]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
A13	SPBC2_24X	RFCTL[2]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
B14	SPBC2_24X	RFCTL[3]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
H14	SPBC2_24X	RFCTL[4]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
C13	SPBC2_24X	RFCTL[5]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
B12	SPBC2_24X	RFCTL[6]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
E13	SPBC2_24X	RFCTL[7]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
F13	SPBC2_24X	RFCTL[8]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
B13	SPBC2_24X	RFCTL[9]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
H13	SPBC2_24X	RFCTL[10]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
C12	SPBC2_24X	RFCTL[11]	O	VIO_2	ie=0, oe=1, 0	ie=0, oe=1, 0	
F12	SPBC2_24X	RFCTL[12]	O	VIO_0	ie=0, oe=1, 0	ie=0, oe=1, 0	
H12	SPBC2_24X	RFCTL[13]	O	VIO_0	ie=0, oe=1, 0	ie=0, oe=1, 0	
E12	SPBC2_24X	RFCTL[14]	O	VIO_0	ie=0, oe=1, 0	ie=0, oe=1, 0	
B11	SPBC2_24X	RFCTL[15]	O	VIO_0	ie=0, oe=1, 0	ie=0, oe=1, 0	
Touch Panel Interface (4 Pins)							
M8	SPCBC2_24X_GP_S	TP_XL	I/O/T	VIO	Ie=1, oe=0	Ie=1, oe=0	
L8	SPCBC2_24X_GP_S	TP_XR	I/O/T	VIO	Ie=1, oe=0	Ie=1, oe=0	
K8	SPCBC2_24X_GP_S	TP_YU	I/O/T	VIO	Ie=1, oe=0	Ie=1, oe=0	
N8	SPCBC2_24X_GP_S	TP_YD	I/O/T	VIO	Ie=1, oe=0	Ie=1, oe=0	
Supply Input							
AE3	SPVDD2	VSIM0					VSIM0 supply input
AE4	SPVDD2	VSIM1					VSIM1 supply input
AE5	SPVDD2	VSIM2					VSIM2 supply input
AE6	SPVDD2	VSIM3					VSIM3 supply input
G5	SPAVDD3	VDDSIM2					
H5	SPAVDD3	VDDSIM3					
F17	SPVSS2	VSSIO					3V IO ring Ground
H17	SPVSS2	VSSIO					3V IO ring Ground
J13	SPVSS2	VSSIO					3V IO ring Ground

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
J14	SPVSS2	VSSIO					3V IO ring Ground
M9	SPVSS2	VSSIO					3V IO ring Ground
N9	SPVSS2	VSSIO					3V IO ring Ground
P9	SPVSS2	VSSIO					3V IO ring Ground
M17	SPVSS2	VSSIO					3V IO ring Ground
M18	SPVSS2	VSSIO					3V IO ring Ground
N18	SPVSS2	VSSIO					3V IO ring Ground
U17	SPVDD1	VDD_D					VDD core supply input
U18	SPVDD1	VDD_D					VDD core supply input
V17	SPVDD1	VDD_D					VDD core supply input
V18	SPVDD1	VDD_D					VDD core supply input
P18	SPVDD1ANA	VDD1P2					VDD ARM SUPPLY
R18	SPVDD1ANA	VDD1P2					VDD ARM SUPPLY
T18	SPVDD1ANA	VDD1P2					VDD ARM SUPPLY
C4	SPVSS1	VSS					1.1V Core Ground
C11	SPVSS1	VSS					1.1V Core Ground
E9	SPVSS1	VSS					1.1V Core Ground
F14	SPVSS1	VSS					1.1V Core Ground
G23	SPVSS1	VSS					1.1V Core Ground
H6	SPVSS1	VSS					1.1V Core Ground
K21	SPVSS1	VSS					1.1V Core Ground
M12	SPVSS1	VSS					1.1V Core Ground
M13	SPVSS1	VSS					1.1V Core

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
							Ground
M14	SPVSS1	VSS					1.1V Core Ground
N12	SPVSS1	VSS					1.1V Core Ground
N13	SPVSS1	VSS					1.1V Core Ground
N14	SPVSS1	VSS					1.1V Core Ground
P12	SPVSS1	VSS					1.1V Core Ground
P13	SPVSS1	VSS					1.1V Core Ground
P14	SPVSS1	VSS					1.1V Core Ground
T21	SPVSS1	VSS					1.1V Core Ground
U10	SPVSS1	VSS					1.1V Core Ground
V23	SPVSS1	VSS					1.1V Core Ground
N21	SPVSS1	VSS					1.1V Core Ground
P5	SPVSS1	VSS					1.1V Core Ground
R9	SPVSS1	VSS					1.1V Core Ground
J10	SPVDD2	VIO0					VIO0 supply input
J11	SPVDD2	VIO0					VIO 0supply input
J12	SPVDD2	VIO0					VIO0 supply input
R17	SPVDD2	VIO1					VIO1 supply input
T17	SPVDD2	VIO1					VIO1 supply input
N17	SPVDD2	VIO2					VIO2 supply input
P17	SPVDD2	VIO2					VIO 2 supply input
V15	SPVDD2	VLCD					VLCD supply

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
							input
AE21	SPVDD2	VNF					VLCD supply input
R20	SPVDD2	VMEM					VMEM supply input
T20	SPVDD2	VMEM					VMEM supply input
U20	SPVDD2POC	VMEM					VMEM supply input
V20	SPVDD2POC	VMEM					VMEM supply input
J17	SPVDD2	VCAM					VCAM supply input
AA17		VDDUSB					VUSB supply input
V16		AVSSUSB					
J1		AVDDBB					
B5		AGNDBB					
F7		AGNDBB					
E1	SPAVDD3	AVDDVBO					
L1	SPAPAD3	VCOM					
M3	SPAVDD3	AGNDVB					
L3	SPAVSS3	VSSAO					
J2	SPAVDD3	VDDAO					
N1	SPAVDD2_RTC	VDDRTC					
J8	SPAVDD3	VDD_A					
R3		VSSPA					
R2		VSSPA					
U1	SPAVDD3(diode)	AVDDPA					
T5		VSSBUCK					
T6		VSSBUCK					
U5		VSSBUCK					
U6		VSSBUCK					
T8		VSSBUCK					
A9	SPAVDD3	VDD18					
H9	SPAVDD3	VDDSD0					
H10	SPAVDD3	VDDSD1					

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
P1	SPAVDD3	VDDWIF0					
A11	SPAVDD3	VDDWIF1					
T3	SPVDD2ANA	VDD_EFUSE					
A8	SPAVDD3	VDD28					
A12	SPAVDD3	VDDMEM					
A7	SPAVDD3	VDDCAMD1					
F6	SPAVSS3_H	AGNDAFC					
A4	SPAVDD3_H	AVDDBB					
B2	SPAVDD3	VDDRF1					
A3	SPAVDD3	VDDRF0					
F1	SPAVDD3_Double	VDDCAMD0					
D1	SPAVDD3	VDDCAMA					
USB interface(2 pads)							
U15		ANATEST					
AE17		VRES					
AD16		PADM					
AE16		PADP					
USB interface(2 pads)							
R6	SPAPAD2	OPTION0A					
P6	SPAPAD2	OPTION1A					
R8	SPAPAD2	OPTION2A					
White LED interface(7 pins)							
F5	SPAPAD3	WHTLED_IB5					
F2	SPAPAD3	WHTLED_IB4					
E3	SPAPAD3	WHTLED_IB3					
E2	SPAPAD3	WHTLED_IB2					
F3	SPAPAD3	WHTLED_IB1					
G3	SPAPAD3	WHTLED_IB0					
G2	SPAPAD3	WHTLED_RSET					
Voice band interface(5 pins)							
G1	SPAPAD3	HEADMIC_IN					
J5	SPAPAD3	AUXMICP					
J6	SPAPAD3	AUXMICN					
K6	SPAPAD3	MICP					
K5	SPAPAD3	MICN					
H1	SPAPAD3	MICBIAS					
H2	SPAPAD3	AIL1					
H3	SPAPAD3	AIR1					

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
L6	SPAPAD3	HEAD_P_L					
L2	SPAPAD3	AOM					
L5	SPAPAD3	HEAD_P_R					
J3	SPAPAD3	AUXSPP					
K3	SPAPAD3	AUXSPN					
K2	SPAPAD3	EARN					
K1	SPAPAD3	EARP					
VBAT input(pins)							
D2	SPAVBAT	AVDD36_1					
D3	SPAVBAT	AVDD36_1					
N6	SPAVBAT	VBAT_SENSE					
N2	SPAVBAT	VBATBK					
T2		VBATPA1					
U2		VBATPA1					
U3		VBATPA1					
V1		VBATBUCK					
V2		VBATBUCK					
V3		VBATBUCK					
W1		VBATBUCK					
W2		VBATBUCK					
A10	SPAVBAT	VBATD					
B10	SPAVBAT	VBATD					
C10	SPAVBAT	VBATD					
C2	SPAVBAT	AVDD36RF					
C1	SPAVBAT	AVDD36RF					
R1	SPAVDD3	VDD25					
R5	SPAVSS3	KPLED_VSS					
Charger Interface (3 pins)							
N5	SPAVBAT	ISENSE					
M5	SPVCHG_HVT	VCHG					
N3	SPVDRV_HVT	VDRV					
RTC Interface (2 pins)							
M2	SPAPAD3	RTC32KO					
M1	SPAPAD3	RTC32KI					
Viberator Driver (1 pins)							
V5	SPAPAD3_DRV	VIBR					
Keypad LED Driver (1 pins)							
V6	SPAPAD3_DRV	KPLED					
ClassD output(2 pins)							

Ball	Pin Type	Pin Name	Default Direction	Power	At Reset	After Reset	Descrption
Y1		OUTPPA					
Y2		OUTPPA					
AA1		OUTNPA					
AA2		OUTNPA					
DCDC interface(4 pins)							
P3	SPAPAD3	EDCDCEN					
T1	SPAPAD3	VCMPA					
AB3	SPAPAD3	VFB					
AB1		LX					
AB2		LX					
P2		EDCDCARM_EN					
AD2	SPAPAD3	VFB_ARM					
AC1		LX_ARM					
AC2		LX_ARM					
Clock input(2 pins)							
G6	SPAPAD3_H	REF26M					
A5	SPAPAD3_H	MCLKI					
Analog Baseband Interface (5 pins)							
E6	SPAPAD3_H	TRXQN					
C6	SPAPAD3_H	TRXQP					
A6	SPAPAD3_H	TXREF					
E5	SPAPAD3_H	TRXIN					
C5	SPAPAD3_H	TRXIP					
APC output (1 pin)							
B4	SPAPAD3_H	APCOUT					
External reset input(1 pin)							
H11	SPAPAD3_ADCI	EXTRSTN					
Aux ADC Interface (4 Pins)							
F10	SPAPAD3_ADCI	ADCI0					
B9	SPAPAD3_ADCI	ADCI1					
F9	SPAPAD3_ADCI	ADCI2					
E10	SPAPAD3_ADCI	ADCI3					

3.1.3 Pin Multiplexed Function List

SC6820 adopts programmable pin multiplexing to reduce pin number as well as providing enough flexibililty. Multiple signals are connected to a multiplexer that connects to the same I/O pin.

Table 3-3 Pin Multiplexed Functions

Pin Name	Mode0	Mode1	Mode2	Mode3
Clock and Reset Interface (3 Pins)				
XTL_EN	XTL_EN			GPIO106
TESTRSTN	TESTRSTN	DOPHIN_12M_EXT	PLL_DIV32OUT_padtest	GPIO201
PBINT	PBINT			
GPIO Interface (10 Pins)				
GPIO135	GPIO135			
GPIO136	GPIO136			PWMC
GPIO137	GPIO137			PWMD
GPIO138	GPIO138			
GPIO139	GPIO139			
GPIO140	GPIO140			
GPIO141	GPIO141			
GPIO142	GPIO142			
GPIO143	GPIO143			PWMA
GPIO144	GPIO144			PWMB
SIM0 Interface (3 Pins)				
SIMCLK0	SIMCLK0			
SIMDA0	SIMDA0			
SIMRST0	SIMRST0			
SIM1 Interface (3 Pins)				
SIMCLK1	SIMCLK1			GPIO16
SIMDA1	SIMDA1			
SIMRST1	SIMRST1			GPIO17
SIM2 Interface (3 Pins)				
SIMCLK2	SIMCLK2	SCL2		GPIO18
SIMDA2	SIMDA2	SDA2		
SIMRST2	SIMRST2	CLK_RTC		
SIM3 Interface (3 Pins)				
SIMCLK3	SIMCLK3		U1RXD	GPIO59
SIMDA3	SIMDA3			
SIMRST3	SIMRST3		U1TXD	GPIO60
SDIO Interface (7 Pins)				
SD0_CLK	SD0_CLK			
SD_CMD	SD_CMD			

Pin Name	Mode0	Mode1	Mode2	Mode3
SD_D[0]	SD_D0			
SD_D]1]	SD_D1			
SD_D[2]	SD_D2			
SD_D[3]	SD_D3			
SD1_CLK	SD1_CLK			GPIO39
SDIO2 Interface (7 Pins)				
SD2_CLK	SD2_CLK	SPI1_CLK		GPIO19
SD2_CMD	SD2_CMD	SPI1_DI		GPIO20
SD2_D[0]	SD2_D0	SPI1_DO		GPIO21
SD2_D]1]	SD2_D1	SPI1_CSN0		GPIO22
SD2_D[2]	SD2_D2	SPI1_CSN1		GPIO23
SD2_D[3]	SD2_D3			GPIO24
Keypad Interface (16 Pins)				
KEYOUT[0]	KEYOUT0			
KEYOUT[1]	KEYOUT1			
KEYOUT[2]	KEYOUT2			
KEYOUT[3]	KEYOUT3			
KEYOUT[4]	KEYOUT4			
KEYOUT[5]	KEYOUT5			GPIO25
KEYOUT[6]	KEYOUT6			GPIO26
KEYOUT[7]	KEYOUT7	CLK_AUX1		GPIO27
KEYIN[0]	KEYIN0			
KEYIN[1]	KEYIN1			
KEYIN[2]	KEYIN2	MRTCK		
KEYIN[3]	KEYIN3			
KEYIN[4]	KEYIN4			
KEYIN[5]	KEYIN5			GPIO28
KEYIN[6]	KEYIN6			EIC0
KEYIN[7]	KEYIN7			EIC1
SPI Interface (5 Pins)				
SPI_DI	SPI_DI	IISDI_VBDA		GPIO29
SPI_CLK	SPI_CLK	IISCLK_VBDA		GPIO30
SPI_DO	SPI_DO	IISLRCK_VBDA		GPIO31
SPI_CSN[0]	SPI_CSN0			GPIO32
SPI_CSN[1]	SPI_CSN1			GPIO33
JTAG Interface (5 Pins)				

Pin Name	Mode0	Mode1	Mode2	Mode3
MTDO	MTDO		DTDO	GPIO34
MTDI	MTDI		DTDI	GPIO35
MTCK	MTCK		DTCK	GPIO36
MTMS	MTMS		DTMS	GPIO37
MTRST_N	MTRST_N		DRTCK	GPIO38
TRACE PORT(10pin)				
TRACECLK	TRACECLK		SPI1_DI	GPIO41
TRACECTRL	TRACECTRL		SPI1_CLK	GPIO42
TRACEDAT0	TRACEDAT0		SPI1_DO	GPIO43
TRACEDAT1	TRACEDAT1		SPI1_CSN0	GPIO44
TRACEDAT2	TRACEDAT2		SPI1_CSN1	GPIO65
TRACEDAT3	TRACEDAT3	IIS1DI		GPIO66
TRACEDAT4	TRACEDAT4	IIS1DO		GPIO67
TRACEDAT5	TRACEDAT5	IIS1CLK		GPIO68
TRACEDAT6	TRACEDAT6	IIS1LRCK		GPIO69
TRACEDAT7	TRACEDAT7	IIS1MCK		GPIO70
UART0 Interface (4 Pins)				
U0TXD	U0TXD		SPI_DO	
U0RXD	U0RXD		SPI_DI	
U0CTS	U0CTS	U2CTS	SPI_CSN0	
U0RTS	U0RTS	U2RTS	SPI_CLK	
UART1 Interface (2 Pins)				
U2TXD	U2TXD			
U2RXD	U2RXD			
UART2 Interface (2 Pins)				
U1TXD	U1TXD			
U1RXD	U1RXD			
LCD Interface (25 Pins)				
LCD_CSN1	LCD_CSN1	CLK_RTC		GPIO62
LCD_RSTN	LCD_RSTN			
LCD_CD	LCD_CD			
LCD_D[0]	LCD_D0			
LCD_D[1]	LCD_D1			
LCD_D[2]	LCD_D2			
LCD_D[3]	LCD_D3			
LCD_D[4]	LCD_D4			

Pin Name	Mode0	Mode1	Mode2	Mode3
LCD_D[5]	LCD_D5			
LCD_D[6]	LCD_D6			
LCD_D[7]	LCD_D7	utmifs_speed		
LCD_D[8]	LCD_D8	utmifs_suspend		
LCD_WRN	LCD_WRN			
LCD_RDN	LCD_RDN			
LCD_CSN0	LCD_CSN0			
LCD_D[9]	LCD_D9	utmifs_tx_enable		
LCD_D[10]	LCD_D10	utmifs_tx_dat		
LCD_D[11]	LCD_D11	utmifs_tx_se0		
LCD_D[12]	LCD_D12	utmifs_int		
LCD_D[13]	LCD_D13	utmifs_rx_dp		
LCD_D[14]	LCD_D14	utmifs_rx_dm		
LCD_D[15]	LCD_D15	utmifs_rx_rcv		
LCD_D[16]	LCD_D16			GPIO63
LCD_D[17]	LCD_D17			GPIO64
LCD_D[18]	LCD_D18			GPIO75
LCD_D[19]	LCD_D19			GPIO76
LCD_D[20]	LCD_D20			GPIO77
LCD_D[21]	LCD_D21			GPIO78
LCD_D[22]	LCD_D22			GPIO79
LCD_D[23]	LCD_D23			GPIO80
LCD_FMARK	LCD_FMARK			GPIO81
Nand Interface (23 Pins)				
NFWPN	NFWPN			
NFRB	NFRB			
NFCLE	NFCLE			
NFALE	NFALE			
NFCEN0	NFCEN0			
NFCEN1	NFCEN1			GPIO71
NFWEN	NFWEN			
NFREN	NFREN			
NFD[0]	NFD0			
NFD[1]	NFD1			
NFD[2]	NFD2			
NFD[3]	NFD3			

Pin Name	Mode0	Mode1	Mode2	Mode3
NFD[4]	NFD4			
NFD[5]	NFD5			
NFD[6]	NFD6			
NFD[7]	NFD7			
NFD[8]	NFD8	CLK_AUX1		GPIO45
NFD[9]	NFD9			GPIO46
NFD[10]	NFD10			GPIO47
NFD[11]	NFD11			GPIO48
NFD[12]	NFD12			GPIO49
NFD[13]	NFD13			GPIO50
NFD[14]	NFD14			GPIO51
NFD[15]	NFD15			GPIO52
EMC Interface (68 Pins)				
EMRST_N	EMRST_N			GPIO40
EMA[0]	EMA0			
EMA[1]	EMA1			
EMA[2]	EMA2			
EMA[3]	EMA3			
EMA[4]	EMA4			
EMA[5]	EMA5			
EMA[6]	EMA6			
EMA[7]	EMA7			
EMA[8]	EMA8			
EMA[9]	EMA9			
EMA[10]	EMA10			
EMA[11]	EMA11			
EMA[12]	EMA12			
EMA[13]	EMA13			
EMD[0]	EMD0			
EMD[1]	EMD1			
EMD[2]	EMD2			
EMD[3]	EMD3			
EMD[4]	EMD4			
EMD[5]	EMD5			
EMD[6]	EMD6			
EMD[7]	EMD7			

Pin Name	Mode0	Mode1	Mode2	Mode3
EMDQM[0]	EMDQM0			
EMDQS[0]	EMDQS0			GPIO54
EMD[8]	EMD8			
EMD[9]	EMD9			
EMD[10]	EMD10			
EMD[11]	EMD11			
EMD[12]	EMD12			
EMD[13]	EMD13			
EMD[14]	EMD14			
EMD[15]	EMD15			
EMDQM[1]	EMDQM1			
EMDQS[1]	EMDQS1			GPIO55
EMD[16]	EMD16			
EMD[17]	EMD17			
EMCKE[1]	EMCKE1			GPIO53
EMD[18]	EMD18			
EMD[19]	EMD19			
EMD[20]	EMD20			
EMD[21]	EMD21			
EMD[22]	EMD22			
EMD[23]	EMD23			
EMDQM[2]	EMDQM2			
EMDQS[2]	EMDQS2			GPIO56
EMD[24]	EMD24			
EMD[25]	EMD25			
EMD[26]	EMD26			
EMD[27]	EMD27			
EMD[28]	EMD28			
EMD[29]	EMD29			
EMD[30]	EMD30			
EMD[31]	EMD31			
EMDQM[3]	EMDQM3			
EMDQS[3]	EMDQS3			GPIO57
CLKDPMEM	CLKDPMEM	CLK_DSP		
CLKDMMEM	CLKDMMEM	CLK_RTC	CLK_AHB	GPIO58
EMRAS_N	EMRAS_N			

Pin Name	Mode0	Mode1	Mode2	Mode3
EMCAS_N	EMCAS_N			
EMWE_N	EMWE_N			
EMCS_N[0]	EMCS_N0			
EMCS_N[1]	EMCS_N1			
EMBA[0]	EMBA0			
EMBA[1]	EMBA1			
EMCKE[0]	EMCKE0			GPIO61
DCAM Interface (15 Pins)				
CCIRMCLK	CCIRMCLK		CLK_DSP	
CCIR_CK	CCIR_CK	RFT_GPO8		
CCIR_HS	CCIR_HS	RFT_GPO9		
CCIR_VS	CCIR_VS	RFT_GPO10		
CCIR_D[0]	CCIR_D0		IISLRCK_VBDA	
CCIR_D[1]	CCIR_D1		IISDI_VBDA	
CCIR_D[2]	CCIR_D2	RFT_GPO0	IISCLK_VBDA	
CCIR_D[3]	CCIR_D3	RFT_GPO1		
CCIR_D[4]	CCIR_D4	RFT_GPO2		
CCIR_D[5]	CCIR_D5	RFT_GPO3		
CCIR_D[6]	CCIR_D6	RFT_GPO4		
CCIR_D[7]	CCIR_D7	RFT_GPO5		
CCIRRST	CCIRRST	RFT_GPO6		GPIO72
CCIRPD1	CCIRPD1	RFT_GPO7		GPIO73
CCIRPD0	CCIRPD0			GPIO74
I2C0 Interface (2 Pins)				
SCL0	SCL0			
SDA0	SDA0			
SCL1	SCL1			
SDA1	SDA1			
SCL2	SCL2			
SDA2	SDA2			
SCL3	SCL3			
SDA3	SDA3			
Aux Clock Interface (1 Pin)				

Pin Name	Mode0	Mode1	Mode2	Mode3
CLK_AUX0	CLK_AUX0			GPIO82
IIS Interface (5 Pins)				
IISDI	IISDI	DTDO		GPIO83
IISDO	IISDO	DTDI		GPIO84
IISCLK	IISCLK	DTCK	ttout0p	GPIO85
IISLRCK	IISLRCK	DTMS		GPIO86
IISMCK	IISMCK	DRTCK	BTXLEN	EIC2
RF Interface (19 Pins)				
RFSDA0	RFSDA0			GPIO87
RFSCK0	RFSCK0			GPIO88
RFSEN0	RFSEN0			GPIO89
RFCTL[0]	RFCTL0			GPIO90
RFCTL[1]	RFCTL1			GPIO91
RFCTL[2]	RFCTL2			GPIO92
RFCTL[3]	RFCTL3	PWMA		GPIO93
RFCTL[4]	RFCTL4	PWMB		GPIO94
RFCTL[5]	RFCTL5			GPIO95
RFCTL[6]	RFCTL6	PWMC		GPIO96
RFCTL[7]	RFCTL7			GPIO97
RFCTL[8]	RFCTL8			GPIO98
RFCTL[9]	RFCTL9	PWMD		GPIO99
RFCTL[10]	RFCTL10	ttout1p		GPIO100
RFCTL[11]	RFCTL11			GPIO101
RFCTL[12]	RFCTL12			GPIO102
RFCTL[13]	RFCTL13			GPIO103
RFCTL[14]	RFCTL14			GPIO104
RFCTL[15]	RFCTL15			GPIO105
Touch Panel Interface (4 Pins)				
TP_XL	TP_XL			GPIO202
TP_XR	TP_XR			GPIO203
TP_YU	TP_YU			GPIO204
TP_YD	TP_YD			GPIO205

3.1.4 Control Registers

3.1.4.1 Memory map

ARM base address: 0x8C00_0000

Offset Address	Pin Name	Default Value after Reset
0x0004	ANA_INT	10'h100
0x0008	EXT_RST_B	10'h100
0x000C	CHIP_SLEEP	10'h100
0x0010	XTL_BUF_EN	10'h100
0x0014	VBDA_D	10'h101
0x0018	VBDA_LR	10'h100
0x001C	VBDA_SCLK	10'h100
0x0020	VBAD_D	10'h100
0x0024	VBAD_LR	10'h100
0x0028	VBAD_SCLK	10'h100
0x0034	GSM_TXPD	10'h100
0x0038	GSM_RXPD	10'h100
0x0040	CLK_32K	10'h100
0x0044	CLK_26M	10'h100
0x0048	ADI_D	10'h100
0x004C	ADI_SYNC	10'h101
0x0050	ADI_SCLK	10'h101
0x0054	IF_SPR	10'h100
0x0058	COM_TX_APCD	10'h100
0x005C	COM_TX_DQ[1]	10'h100
0x0060	COM_TX_DQ[0]	10'h100
0x0064	COM_TX_DI[1]	10'h100
0x0068	COM_TX_DI[0]	10'h100
0x006C	COM_TX_SYNC	10'h100
0x0070	COM_TX_SCLK	10'h100
0x0074	COM_RX_DQ[1]	10'h100
0x0078	COM_RX_DQ[0]	10'h100
0x007C	COM_RX_DI[1]	10'h100
0x0080	COM_RX_DI[0]	10'h100
0x0084	COM_RX_SYNC	10'h100
0x0088	COM_RX_SCLK	10'h100
0x008C	SIMCLK0	10'h100
0x0090	SIMDA0	10'h180

0x0094	SIMRST0	10'h100
0x0098	SIMCLK1	10'h100
0x009C	SIMDA1	10'h180
0x00A0	SIMRST1	10'h100
0x00A4	SD0_CLK	10'h100
0x00A8	SD_CMD	10'h180
0x00AC	SD_D[0]	10'h180
0x00B0	SD_D[1]	10'h180
0x00B4	SD_D[2]	10'h180
0x00B8	SD_D[3]	10'h180
0x00BC	SD1_CLK	10'h100
0x00C0	KEYOUT[0]	10'h100
0x00C4	KEYOUT[1]	10'h100
0x00C8	KEYOUT[2]	10'h100
0x00CC	KEYOUT[3]	10'h100
0x00D0	KEYOUT[4]	10'h100
0x00D4	KEYOUT[5]	10'h100
0x00D8	KEYOUT[6]	10'h100
0x00DC	KEYOUT[7]	10'h100
0x00E0	KEYIN[0]	10'h180
0x00E4	KEYIN[1]	10'h180
0x00E8	KEYIN[2]	10'h180
0x00EC	KEYIN[3]	10'h180
0x00F0	KEYIN[4]	10'h180
0x00F4	KEYIN[5]	10'h180
0x00F8	KEYIN[6]	10'h180
0x00FC	KEYIN[7]	10'h180
0x0100	SPI_DI	10'h18A
0x0104	SPI_CLK	10'h106
0x0108	SPI_DO	10'h10A
0x010C	SPI_CSN0	10'h10A
0x0110	SPI_CSN1	10'h106
0x0114	MTDO	10'h101
0x0118	MTDI	10'h18A
0x011C	MTCK	10'h146
0x0120	MTMS	10'h18A
0x0124	MTRST_N	10'h18A
0x0128	U0TXD	10'h100

0x012C	U0RXD	10'h180
0x0130	U0CTS	10'h180
0x0134	U0RTS	10'h100
0x0138	U1TXD	10'h100
0x013C	U1RXD	10'h180
0x0140	NFWPN	10'h100
0x0144	NFRB	10'h180
0x0148	NFCLE	10'h100
0x014C	NFALE	10'h100
0x0150	NFCEN0	10'h100
0x0154	NFWEN	10'h100
0x0158	NFREN	10'h100
0x015C	NFD[0]	10'h100
0x0160	NFD[1]	10'h100
0x0164	NFD[2]	10'h100
0x0168	NFD[3]	10'h100
0x016C	NFD[4]	10'h100
0x0170	NFD[5]	10'h100
0x0174	NFD[6]	10'h100
0x0178	NFD[7]	10'h100
0x017C	NFD[8]	10'h100
0x0180	NFD[9]	10'h100
0x0184	NFD[10]	10'h100
0x0188	NFD[11]	10'h100
0x018C	NFD[12]	10'h100
0x0190	NFD[13]	10'h100
0x0194	NFD[14]	10'h100
0x0198	NFD[15]	10'h100
0x019C	EMRST_N	10'h100
0x01A0	EMA[0]	10'h100
0x01A4	EMA[1]	10'h100
0x01A8	EMA[2]	10'h100
0x01AC	EMA[3]	10'h100
0x01B0	EMA[4]	10'h100
0x01B4	EMA[5]	10'h100
0x01B8	EMA[6]	10'h100
0x01BC	EMA[7]	10'h100
0x01C0	EMA[8]	10'h100

0x01C4	EMA[9]	10'h100
0x01C8	EMA[10]	10'h100
0x01CC	EMA[11]	10'h100
0x01D0	EMA[12]	10'h100
0x01D4	EMA[13]	10'h100
0x01D8	EMCKE[1]	10'h100
0x01DC	EMD[0]	10'h100
0x01E0	EMD[1]	10'h100
0x01E4	EMD[2]	10'h100
0x01E8	EMD[3]	10'h100
0x01EC	EMD[4]	10'h100
0x01F0	EMD[5]	10'h100
0x01F4	EMD[6]	10'h100
0x01F8	EMD[7]	10'h100
0x01FC	EMDQM[0]	10'h100
0x0200	EMDQS[0]	10'h100
0x0204	EMD[8]	10'h100
0x0208	EMD[9]	10'h100
0x020C	EMD[10]	10'h100
0x0210	EMD[11]	10'h100
0x0214	EMD[12]	10'h100
0x0218	EMD[13]	10'h100
0x021C	EMD[14]	10'h100
0x0220	EMD[15]	10'h100
0x0224	EMDQM[1]	10'h100
0x0228	EMDQS[1]	10'h100
0x022C	EMD[16]	10'h100
0x0230	EMD[17]	10'h100
0x0234	EMD[18]	10'h100
0x0238	EMD[19]	10'h100
0x023C	EMD[20]	10'h100
0x0240	EMD[21]	10'h100
0x0244	EMD[22]	10'h100
0x0248	EMD[23]	10'h100
0x024C	EMDQM[2]	10'h100
0x0250	EMDQS[2]	10'h100
0x0254	EMD[24]	10'h100
0x0258	EMD[25]	10'h100

0x025C	EMD[26]	10'h100
0x0260	EMD[27]	10'h100
0x0264	EMD[28]	10'h100
0x0268	EMD[29]	10'h100
0x026C	EMD[30]	10'h100
0x0270	EMD[31]	10'h100
0x0274	EMDQM[3]	10'h100
0x0278	EMDQS[3]	10'h100
0x027C	CLKDPMEM	10'h100
0x0280	CLKDMMEM	10'h100
0x0284	EMRAS_N	10'h100
0x0288	EMCAS_N	10'h100
0x028C	EMWE_N	10'h100
0x0290	EMCS_N[0]	10'h100
0x0294	EMCS_N[1]	10'h100
0x0298	EMGPRE_LOOP	10'h100
0x029C	EMGPST_LOOP	10'h100
0x02A0	EMBA[0]	10'h100
0x02A4	EMBA[1]	10'h100
0x02A8	EMCKE[0]	10'h100
0x02AC	LCD_CSN1	10'h100
0x02B0	LCD_RSTN	10'h100
0x02B4	LCD_CD	10'h100
0x02B8	LCD_D[0]	10'h100
0x02BC	LCD_D[1]	10'h100
0x02C0	LCD_D[2]	10'h100
0x02C4	LCD_D[3]	10'h100
0x02C8	LCD_D[4]	10'h100
0x02CC	LCD_D[5]	10'h100
0x02D0	LCD_D[6]	10'h100
0x02D4	LCD_D[7]	10'h100
0x02D8	LCD_D[8]	10'h100
0x02DC	LCD_WRN	10'h100
0x02E0	LCD_RDN	10'h100
0x02E4	LCD_CSN0	10'h100
0x02E8	LCD_D[9]	10'h100
0x02EC	LCD_D[10]	10'h100
0x02F0	LCD_D[11]	10'h100

0x02F4	LCD_D[12]	10'h100
0x02F8	LCD_D[13]	10'h100
0x02FC	LCD_D[14]	10'h100
0x0300	LCD_D[15]	10'h100
0x0304	LCD_D[16]	10'h100
0x0308	LCD_D[17]	10'h100
0x030C	LCD_FMARK	10'h180
0x0310	CCIRMCLK	10'h100
0x0314	CCIRCK	10'h100
0x0318	CCIRHS	10'h100
0x031C	CCIRVS	10'h100
0x0320	CCIRD[0]	10'h100
0x0324	CCIRD[1]	10'h100
0x0328	CCIRD[2]	10'h100
0x032C	CCIRD[3]	10'h100
0x0330	CCIRD[4]	10'h100
0x0334	CCIRD[5]	10'h100
0x0338	CCIRD[6]	10'h100
0x033C	CCIRD[7]	10'h100
0x0340	CCIRRST	10'h100
0x0344	CCIRPD1	10'h100
0x0348	CCIRPD0	10'h100
0x034C	SCL1	10'h180
0x0350	SDA1	10'h180
0x0354	CLK_AUX0	10'h106
0x0358	IISDI	10'h146
0x035C	IISDO	10'h10A
0x0360	IISCLK	10'h14A
0x0364	IISLRCK	10'h14A
0x0368	IISMCK	10'h146
0x036C	RFSDA0	10'h140
0x0370	RFSCK0	10'h140
0x0374	RFSEN0	10'h180
0x0378	RFCTL[0]	10'h100
0x037C	RFCTL[1]	10'h100
0x0380	RFCTL[2]	10'h100
0x0384	RFCTL[3]	10'h100
0x0388	RFCTL[4]	10'h100

0x038C	RFCTL[5]	10'h100
0x0390	RFCTL[6]	10'h100
0x0394	RFCTL[7]	10'h100
0x0398	RFCTL[8]	10'h100
0x039C	RFCTL[9]	10'h100
0x03A0	RFCTL[10]	10'h100
0x03A4	RFCTL[11]	10'h100
0x03A8	RFCTL[12]	10'h100
0x03AC	RFCTL[13]	10'h100
0x03B0	RFCTL[14]	10'h100
0x03B4	RFCTL[15]	10'h100
0x03B8	XTL_EN	10'h101
0x03BC	PTEST	10'h101
0x03C0	GPIO135	10'h100
0x03C4	GPIO136	10'h100
0x03C8	GPIO137	10'h100
0x03CC	GPIO138	10'h100
0x03D0	GPIO139	10'h100
0x03D4	GPIO140	10'h100
0x03D8	GPIO141	10'h100
0x03DC	GPIO142	10'h100
0x03E0	GPIO143	10'h100
0x03E4	GPIO144	10'h100
0x03E8	SD2_CLK	10'h100
0x03EC	SD2_CMD	10'h180
0x03F0	SD2_D[0]	10'h180
0x03F4	SD2_D[1]	10'h180
0x03F8	SD2_D[2]	10'h180
0x03FC	SD2_D[3]	10'h180
0x0400	U2TXD	10'h100
0x0404	U2RXD	10'h180
0x0408	NFCEN1	10'h100
0x040C	SCL0	10'h180
0x0410	SDA0	10'h180
0x0414	SCL2	10'h180
0x0418	SDA2	10'h180
0x041C	SCL3	10'h180
0x0420	SDA3	10'h180

0x0424	LCD_D[18]	10'h100
0x0428	LCD_D[19]	10'h100
0x042C	LCD_D[20]	10'h100
0x0430	LCD_D[21]	10'h100
0x0434	LCD_D[22]	10'h100
0x0438	LCD_D[23]	10'h100
0x043C	TRACECLK	10'h10A
0x0440	TRACECTRL	10'h106
0x0444	TRACEDAT[0]	10'h10A
0x0448	TRACEDAT[1]	10'h100
0x044C	TRACEDAT[2]	10'h100
0x0450	TRACEDAT[3]	10'h106
0x0454	TRACEDAT[4]	10'h100
0x0458	TRACEDAT[5]	10'h106
0x045C	TRACEDAT[6]	10'h106
0x0460	TRACEDAT[7]	10'h106
0x0464	SIMCLK2	10'h100
0x0468	SIMDA2	10'h180
0x046C	SIMRST2	10'h100
0x0470	SIMCLK3	10'h100
0x0474	SIMDA3	10'h180
0x0478	SIMRST3	10'h100

ARM base address: 0x8200_0180

Offset Address	Pin Name	Default Value after Reset
0x008C	TESTRSTN	10'h102
0x0094	PBINT	10'h100
0x0098	TP_XL	10'h100
0x009C	TP_XR	10'h100
0x00A0	TP_YU	10'h100
0x00A4	TP_YD	10'h100

3.1.4.2 Register Description

3.1.4.2.1 PIN_CTRL_REG

Description：Pin control register

0x0000			Pin control register (reset 0x0)													PIN_CTRL_REG
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Sim3_clk_pl	Sim2_clk_pl	wpd_sim3pd	wpd_sim2pd	wpd_sd2pd	SDA3_wpus	SCL3_wpus	SDA2_wpus	SCL2_wpus	SDA0_wpus	SCL0_wpus	Sim1_clk_pl	Sim0_clk_pl	SIMCLK2_wpus	SIMDA2(3)_wpus	MTRST_N
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MTMS_wpus	MTDI_wpus	KEYIN_wpus	NFRB_wpus	SIMDA1_wpus	SIMDA0_wpus	SDA1_wpus	SCL1_wpus	wpd_campd	wpd_iopd	wpd_sim1pd	wpd_sdpd	wpd_nfpd	wpd_sim0pd	wpd_mempd	wpd_lcd_pd
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:

PIN_CTL_REG[7:0], [29:27] are used to avoid current leakage when LDO Pad is shut down, each bit corresponding to pads in the same Voltage Domain, These bits should be set before LDO shut down.

PIN_CTL_REG[18:8], [26:21] are used to select pull up resistor from 72K and 4.7K,1'b1 is 4.7K,1'b0 is 72K.

Field Name	Bit	Type	Reset Value	Description
Sim3_clk_pl	[31]	R/W	1'h0	Clock polarity sel of SIM_CLK3,when sim3 haven't been selected.
Sim2_clk_pl	[30]	R/W	1'h0	Clock polarity sel of SIM_CLK2,when sim3 haven't been selected.
Wpd_sim3pd	[29]	R/W	1'h0	Weakly pull down pads in VSIM3 domain before the domain is shut down
Wpd_sim2pd	[28]	R/W	1'h0	Weakly pull down pads in VSIM2 domain before the domain is shut down
Wpd_sd2pd	[27]	R/W	1'h0	Weakly pull down pads in VSD2 domain before the domain is shut down
SDA3_wpus	[26]	R/W	1'h0	Wake up pull up resistor select for SDA3
SCL3_wpus	[25]	R/W	1'h0	Wake up pull up resistor select for SCL3
SDA2_wpus	[24]	R/W	1'h0	Wake up pull up resistor select for SDA2
SCL2_wpus	[23]	R/W	1'h0	Wake up pull up resistor select for SCL2
SDA0_wpus	[22]	R/W	1'h0	Wake up pull up resistor select for SDA0
SCL0_wpus	[21]	R/W	1'h0	Wake up pull up resistor select for SCL0
Sim1_clk_pl	[20]	R/W	1'h0	Clock polarity sel of SIM_CLK1,when sim3 haven't been selected.
Sim0_clk_pl	[19]	R/W	1'h0	Clock polarity sel of SIM_CLK0,when sim3 haven't been selected.
SIMCLK2_wpus	[18]	R/W	1'h0	Wake up pull up resistor select for SIMCLK2

SIMDA23_wpus	[17]	R/W	1'h0	Wake up pull up resistor select for SIMDA2 and SIMDA3
MTRST_N_wpus	[16]	R/W	1'h0	Wake up pull up resistor select for MTRST_N
MTMS_wpus	[15]	R/W	1'h0	Wake up pull up resistor select for MTMS
MTDI_wpus	[14]	R/W	1'h0	Wake up pull up resistor select for MTDI
KEYIN_wpus	[13]	R/W	1'h0	Wake up pull up resistor select for KEYIN
NFRB_wpus	[12]	R/W	1'h0	Wake up pull up resistor select for NFRB
SIMDA1_wpus	[11]	R/W	1'h0	Wake up pull up resistor select for SIMDA[1]
SIMDA0_wpus	[10]	R/W	1'h0	Wake up pull up resistor select for SIMDA[0]
SDA1_wpus	[9]	R/W	1'h0	Wake up pull up resistor select for SDA1
SCL1_wpus	[8]	R/W	1'h0	Wake up pull up resistor select for SCL1
wpd_campd	[7]	R/W	1'h0	Weakly pull down pads in VCAM domain before the domain is shut down
wpd_iopd	[6]	R/W	1'h0	Weakly pull down pads in VIO/VIO_0/VIO_1/VIO_2 domain before the domain is shut down
wpd_sim1pd	[5]	R/W	1'h0	Weakly pull down pads in VSIM1 domain before the domain is shut down
wpd_sdpd	[4]	R/W	1'h0	Weakly pull down pads in VSD domain before the domain is shut down
wpd_nfpd	[3]	R/W	1'h0	Weakly pull down pads in VNF domain before the domain is shut down
wpd_sim0pd	[2]	R/W	1'h0	Weakly pull down pads in VSIM0 domain before the domain is shut down
wpd_mempd	[1]	R/W	1'h0	Weakly pull down pads in VMEM domain before the domain is shut down
wpd_lcdpd	[0]	R/W	1'h0	Weakly pull down pads in VLCD domain beforen the domain is shut down

3.1.4.2.2 Other Pin Control Register

Description：Other Pin control register share the same bit format shown as below:

Offset Address			Other Pin control register (reset value depends)										PIN_NAME_ REG			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						PIN_NAME_ drv		PIN_ NAM E_fu nc_ wpu	PIN_ NAM E_fu nc_ wpd	PIN_NAME_ sel		PIN_ NAM E_w pu	PIN_ NAM E_w pd	PIN_ NAM E_ie	PIN_ NAM E_o e
Type	RO						R/W		R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:

"**PIN_NAME**" represents each pin. Function 0, 1, 2, 3 of each pin is detailed in Pin Multiplexed Function List, the default value of each control bit is detailed in Memory Map.

Field Name	Bit	Type	Reset Value	Description
	[31:10]	RO	22'h0	**Reserved**
PIN_NAME_drv	[9:8]	R/W		**Driver Strength select**
PIN_NAME_func_wpu	[7]	R/W		**Weakly pull up for function mode**
PIN_NAME_func_wpd	[6]	R/W		**Weakly pull down for function mode**
PIN_NAME_sel	[5:4]	R/W		**Function select:** **2'b00: Mode0** **2'b01: Mode1** **2'b10: Mode2** **2'b11: Mode3**
PIN_NAME_wpu	[3]	R/W		**Weak pull up for chip deep sleep mode**
PIN_NAME_wpd	[2]	R/W		**Weak pull down for chip deep sleep mode**
PIN_NAME_ie	[1]	R/W		**Input enable for chip deep sleep mode**
PIN_NAME_oe	**[0]**	**R/W**		**Output enable for chip deep sleep mode**

4 Electrical Specifications

4.1 DC Specifications

4.1.1 Absolute Maximum Ratings

The functionality of SC6820 is subject to the absolute maximum/minimum values listed in Table 4-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 4-1 Absolute maximum ratings of SC6820

Symbol	Parameter	Min	Max	Unit
VCHG	Charger input voltage from adaptor or USB	-0.3	18	V
VBAT	Supply voltage from a battery	-0.3	5.2	V
V_{DI}	Input voltage on any digital input	-0.3	3.6	V
V_{AI}	Input voltage on any analog input	-0.3	3.6	V
I_{AI2}	DC drive current for EARP, EARN, AUXSPP and AUXSPN		60	mA
$V_{max, ESD}$	Maximum ESD stress voltage, Human Body Model, any pin to any supply pin, either polarity or any pin to all non-supply pins together, either polarity. Three stresses maximum.		2,000	V
$I_{max, DC}$	Maximum DC Input current for any non-supply pin		5	mA
T_a	Ambient temperature	-45	+95	°C
$T_{storage}$	Storage temperature	-65	+125	°C
V_{pulse}, T_{width}	Voltage surge on vbat		14 10	V μs

Note: Vpulse and Twidth is described below:

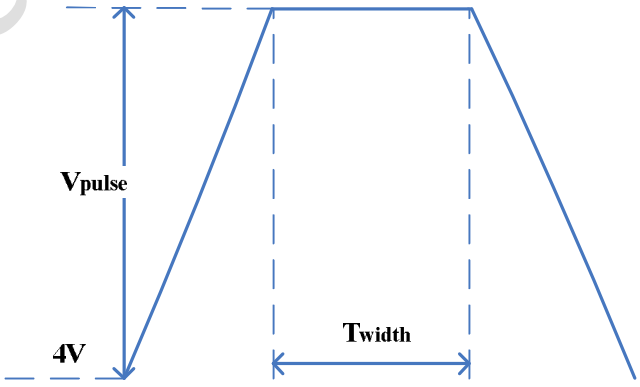


Figure 4-1 Voltage surge on VBAT

4.1.2 Recommended Operating Conditions

SC6820 is recommended to operate under the conditions list in Table 4-2.

Table 4-2 Recommended operating conditions

Symbol	Parameter	Min	Typical	Max	Unit
VCHG	Charger input voltage	4.5	5.0	5.5	V
VBAT	Supply voltage from a battery	3.2	3.6	4.2	V
VDD	Core supply voltage	1.0	1.1	1.2	V
	Arm supply voltage	1.1	1.2	1.3	V
$T_{junction}$	Junction temperature	-20		+125	°C
$T_{ambient}$	Ambient operating temperature	-40		+85	°C

Note1: Hardware stops charging if VCHG is higher than 9V and the maximum value of VCHG can be set by software. The higher maximum value of VCHG, the stricter Vds requirement of external MOSFET.

Note2: The value set by software should be 10% higher than maximum value of VCHG listed in table to guarantee all chips can stop charging over the maximum value of VCHG.

4.1.3 Thermal Characteristics

The thermal characteristics are as shown in Table 4-3.

Table 4-3 Thermal characteristics

Symbol	Parameter	Condition	Value	Unit
Theta JA	Junction-to-Ambient thermal resistance	Air flow: 0 m/sec	40	°C/watt

4.1.4 ESD Characteristics

The ESD characteristics are shown in Table 4-4.

Table 4-4 ESD characteristics

Symbol	Parameter	Condition	Value	Unit
HBM	Human body model	MIL STD 883G, method 3015.7	±2K	V
CDM	Charged-device model	JESD22-C101-C	±800	V
MM	Machine model	JESD22-A115-A	±200	V

4.1.5 DC Characteristics

SC6820 typical core voltage (VDD) is 1.1 V and the I/O supply (VDDIO) is typically at 2.8 V. The analog circuits are typically powered at 3.0 V. The core and analog power supplies are provided by the on-chip LDOs. The external battery can be connected directly to pins VBATD, VBATPA, VBATBUCK, AVDD36_1, AVDD36RF. If not specified, VBAT means all and VBATA includes VBATPA, AVDD36-1, AVDD36RF. The power pins should be connected with a decoupling capacitor to ground (VSS, VSSIO).

For the following table, T_{amb} = -40 to +85 °C, VSS = 0 V (ground), VBAT = 3.6 V, and all voltages are measured with respect to VSS, unless otherwise specified.

Table 4-5 DC characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
$I_{standby\ (tot)}$	Total standby current	The whole chip is in deep sleep mode	–	0.8	–	mA
I_{dp}	Deep power-down current	The whole chip is powered down by software		50		uA
Digital supply voltage: pins VDDIO						
VDDIO	Digital supply voltage		1.5	–	3.1	V
Digital supply voltage: pins VLCD						
VLCD	Digital supply voltage		1.5	–	3.1	V
Digital supply voltage: pins VCAM						
VCAM	Digital supply voltage		1.5	–	3.1	V
Digital supply voltage: pins VMEM						
VMEM	Digital supply voltage		1.6	–	2.0	V
Digital supply voltage: pins VNF						
VNF	Digital supply voltage		1.5	–	3.1	V
Digital supply voltage: internal VDD						
VDD	Digital core supply voltage		1.0	1.1	1.2	V
	Sleep mode digital core supply voltage		0.8	0.9	1.0	V
	Arm Core supply voltage		1.1	1.2	1.3	V
Digital input						
V_{IL}	Input voltage LOW-level		0	–	0.3 Vpad	V
V_{IH}	Input voltage HIGH-level		0.7 Vpad	–	Vpad	V
I_{LI}	Input leakage current		–	±2	–	µA
Digital output						
V_{OL}	Output voltage LOW-level	At I_{sink} = 2,4,6,10 mA (programmable)	0	–	0.1 Vpad	V

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{OH}	Output voltage HIGH-level	At I_{source} = 2,4,6,10 mA (programmable)	0.9 Vpad	–	Vpad	V
Analog supply voltage: pins VBATA						
VBATA	Analog supply voltage		3.3	3.6	4.2	V
I_{VBATA}	Analog supply current	AVDD = 2.8 V All analog blocks are active, but no load at EARP, EARN, AUXSPP and AUXSPN	–	5	–	mA
Analog supply voltage: internal AVDD						
AVDD	Analog core supply voltage		2.7	3.0	3.3	V
RTC supply: pin RTCVDD						
RTCVDD	Supply voltage		1.6	1.8	2	V
I_{RTCVDD}	Supply current			10		µA
Iquiescent	LDORTC quiescent current			9		µA

Note1: Vpad means the power supply voltage at the corresponding pad.

Note2: Supply voltage of RTCVDD can be set as 1.8V, 1.7V, 1.6V and 1.5V, please refer to 4.3.10 about details. When VBAT is on, I_{RTCVDD} can be reduce to 2uA through setting V_{RTCVDD} as 1.5V in power down mode. When VBAT is off, I_{RTCVDD} can be reduce to 5uA through reducing the amplitude of XTL32K.

4.2 AC Characteristics

A pin's AC characteristics include input and output capacitance, which determine loading for external drivers or other load analysis. The AC characteristics also include a de-rating factor, which indicates how much faster or slower the AC timings get with different loads.

Table 4-6 Standard input, output and I/O pin AC characteristics

Symbol	Parameters	Min	Typical	Max	Units
C_{in}	Input capacitance, all standard input and IO pins			3.5	pF
C_{load}	Output capacitance, all standard output and IO pins			30	pF
T_{dr}	Output de-rating falling edge on all standard output and I/O pins, from 30 pF load		0.166		ns/pF

Note:

1. The AC specifications are tested with a 30 pF load as indicated in Figure 4-2

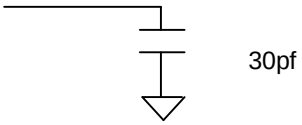


Figure 4-2 Test circuit of an I/O pin

2. The output capacitance and de-rating falling edge are measured under the condition of maximum driving strength: 24 mA @ 3 V.

For the following tables, T_{amb} = -40 to +85 °C, VSS = 0 V (ground), VBAT = 3.6 V, and all voltages are measured with respect to VSS, unless otherwise specified.

Table 4-7 AC characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
f_{mclk}	Master clock frequency		–	26	–	MHz
f_{rtcclk}	Real-time clock frequency		–	32.768	–	kHz
Digital input						
C_I	Input capacitance		–	3	–	pF
Digital output						
T_R	Output rise time	Output load = 20 pF	2	–	5	ns
T_F	Output fall time	Output load = 20 pF	2	–	5	ns
Master clock input						
$\triangle f/f_{mclk}$	Frequency compensation range		-27		27	ppm
V_{mclk}	Master clock amplitude	AC coupling	0.65	–	2.4	V
δ_{mclk}	Master clock duty cycle		40	–	60	%
Real-time clock input						
$\triangle f/f_{rtclk}$	Frequency tolerance	Standard deviation	-80		80	ppm
δ_{rtclk}	Clock duty cycle		35	–	65	%

4.3 Performance Specifications

This section specifies the performance of some major SC6820 modules.

4.3.1 GSM Baseband

4.3.1.1 Baseband Transmit Path

The outputs of GMSK modulator are converted to analog levels by 10-bit D/A Converters (DAC), and then passed to an analog Butterworth low pass filter. Each analog part has special offset cancellation.

Table 4-8 Performance of GSM baseband transmit path

Parameter	Conditions/Comments	Min	Typical	Max	Unit
Transmission buffer length			160		bits
GMSK modulator					
Input data word rate			270.833		kHz
I/Q interpolation output size			10		bits
DAC					
Number of Channels			2		
Resolution			10		bits
Signal to noise ratio		54			dB
Dynamic Range		54			dB
Total harmonic distortion				-54	dBFs
GMSK phase trajectory error					
RMS error	Including analog filter			1.5	°
Peak error				7	°
LP analog filter					
Cutoff frequency (3 dB)			250 (± 20%)		kHz
Group delay				9	µsec
I/Q mismatch					
I/Q amplitude mismatch				0.2	dB
I/Q phase mismatch				0.1	°
Maximum differential output voltage	TX_B [1:0] = 00		±0.6		V
	TX_B [1:0] = 10		±0.9		
	TX_B [1:0] = 01		±1.2		
	TX_B [1:0] = 11		±1.5		
Output common mode voltage			1.15 1.25 1.05 1.35		V
DC offset				10	mV
Minimum load resistance					
Single-ended		100			kΩ

Parameter	Conditions/Comments	Min	Typical	Max	Unit
Differential		50			kΩ
Maximum load Capacitance					
Single-ended				50	pF
Differential				50	pF
Relative output power	Complies with GSM spectral mask				
	0 – 100 kHz	-3		0	dB
	200 kHz			-32	
	250 kHz			-35	
	400 kHz			-63	
	600 kHz			-71	
	1200 kHz			-71	
	> 1800 kHz			-71	

4.3.1.2 Baseband Receive Path

The differential I/Q signal from the RF module is modulated to two-bit words by Σ-Δ modulator at a frequency much higher than the Nyquist rate. Then the signal passes through a digital filter. Each analog part has special offset cancellation.

Table 4-9 Performance of the baseband receive path

Parameter	Conditions/Comments	Min	Typical	Max	Unit
Input common mode signal range		1.26	1.4	1.54	V
Input differential full scale voltage		-	6	-	V
Input sampling frequency		-	26	-	MHz
Output data					
Analog input signal bandwidth			262.5		kHz
Dynamic range		78			dB
Signal to (noise + distortion) ratio			78		dB
Input DC offset			2		mV
In-band gain flatness		-0.25		0.25	dB

4.3.2 Voice Band

4.3.2.1 Micbias

Table 4-10 Electrical specification of micbias

Symbol	Parameter description	Condition	Min	Typ	Max	Unit
Vi	Input supply voltage	From AVDDVB	2.9	3.3	3.6	V

Symbol	Parameter description	Condition	Min	Typ	Max	Unit
Vo	Regulated output voltage	Vi=3.3 Vi=3.4 Vi=3.2 Vi=2.9		2.8 2.85 2.7 2.45		V
Iout	Output current		2		4	mA
Output Noise	A-Weighted, RMS output level			20	40	μV
Cext	External cap	ESR typical <0.5ohm		2.2		μF

4.3.2.2 Voice Band Uplink PGA

Table 4-11 Electrical specification of Voice band uplink PGA

Symbol	Parameter description	Condition	Min	Typ	Max	Unit
Gain range	Gain range		0		22.5	dB
Gain step	Gain step size		1.1	1.5	1.7	dB
Gain accuracy		GI@1kHz	-0.2		0.2	dB
Gain boost	Boost gain GM activated			20		dB
Notes: GI is for PGATM gain and GIM is for boost gain.						

4.3.2.3 Voice Band Uplink Sigma-Delta ADC

Table 4-12 Electrical specification of Voice band uplink sigma-delta ADC

Symbol	Parameter description	Condition	Min	Typ	Max	Unit
AVDD	Power supply		2.9	3.3	3.6	V
Input Level	Input full scale voltage	GIM=0dB GI=0dB GIM=20dB GI=0dB	2.49 0.24	2.8 0.28	3.5 0.35	V
Input Resistance		GI=0 or 22.5dB, GIM=20dB	14	20	26	KOhm
Input bypass capacitor	Cbymic			1		μF
SNR	Signal to noise ratio	A-weighted, 1kHz sine wave @ Full Scale GI = 0dB, GIM = 20dB or 0dB	80	85		dB
THD	Total harmonic distortion	1kHz sine wave @ Full Scale GI = 0dB, GIM = 20dB or 0dB		-70	-65	dB
Dynamic range	Dynamic range	A-weighted, 1kHz sine wave @ Full Scale -60dB		80		dB

Symbol	Parameter description	Condition	Min	Typ	Max	Unit
		GIM = 20dB				
PSRR	Power rejection ratio	100mVpp 1kHz sine wave is applied to AVDD, input data is 0, GI=0dB, GIM = 20dB	50	63		dB

4.3.2.4 Voice Band Downlink DAC to Headphone Output

Table 4-13 Electrical specification of voice band downlink DAC to headphone output

Symbol	Parameter description	Condition	Min	Typ	Max	Unit
AVDD	Power supply		2.9	3.3	3.6	V
Output level	Output range	Full Scale, Gain GOL,GOR=-1.5dB, GODL, GODR = 0dB		2.35		V
Maximum output level		Full Scale, Gain GOL,GOR=1dB, GODL, GODR = 0dB,32ohm loading		3.05		V
Maximum output power		R=16 Ohms		30		mW
		R=32 Ohms		20		
SNR		A-weighted, 1kHz sine wave @ Full Scale GOL,GOR=-1.5dB, GODL, GODR = 0dB, 32 Ohm load	85	90		dB
DR		A-weighted, 1kHz sine wave @ Full Scale –60dB GOL/R=-1.5dB, GODL/R=0dB	85	90		dB
THD		1kHz sine wave @ Full Scale –1dB /-6dB GOL/R=-1.5dB, GODL/R=0dB			-70	dB
Output noise		A-weighted, RMS Noise level @ 0vpp output		16		μV
PSRR		100/450mVpp 217/434/651Hz sine wave is applied to AVDD, input is 0 GOL/R=-1.5dB ,GOD L/R =0dB	50	68		dB
Channel separation		Full scale at one output, detection the signal at the other	70			dB

Symbol	Parameter description	Condition	Min	Typ	Max	Unit
		side				
DAC channel mismatch		L and R channel output level mismatch			0.15	dB
Gain range(GOL/GOR)		GOL, GOR 5-bit programmable range, mixed analog/digital control, @1kHz	-33.5		+4.5	dB
Gain step(GOL/GOR)		GOL/R: +4.5dB ~ +0.5dB		0.5		dB
		GOL/R: +0.5dB ~ -11.5dB		1		
		GOL/R: -11.5dB ~ -33.5dB		2		
Gain accuracy(GOL/GOR)		GOL/GOR @1kHz	-0.2		0.2	dB
Gain range(GODL/GODR)		GODL, GODR 4-bit programmable range, mixed analog/digital control, @1kHz	-22.5		0	dB
Gain step(GODL/GODR)		GODL/GODR		1.5		dB
Gain accuracy(GODL/GODR)		GODL/GODR @1kHz	-0.5		0.5	dB
Output Resistance			16			ohm
Output Capacitance					100	pF

4.3.2.5 Voice Band Downlink Line Input to Headphone Output

Table 4-14 Electrical specification of Voice band downlink Line input to Headphone output

Symbol	Parameter description	Condition	Min	Typ	Max	Unit
AVDD	Power supply		2.9	3.3	3.6	V
Input level				2.8		V
Output level	Output range	Full Scale, Gain GOL,GOR=-1.5dB, GOBL/GOBR = 0dB		2.09		V

Symbol	Parameter description	Condition	Min	Typ	Max	Unit
Input Resistance				40		kohm
Input bypass capacitor	Cbyline			1		µF
SNR		A-weighted, 1kHz sine wave @ Full Scale GOL,GOR=-1.5dB, GOBL/GOBR = 0dB, 32 Ohm load		87		dB
THD		A-weighted, 1kHz sine wave @ Full Scale –1dB /-6dB GOL/R=-1.5dB, GOBL/GOBR =0dB		-78		dB
Mute attenuation			80	98		dB
Gain range		GOBL, GOBR 5-bit programmable range, mixed analog/digital control, @1kHz	-22.5		+6	dB
Gain step		GOBL/GOBR		1.5		dB
Gain accuracy		GOBL/GOBR @1kHz	-0.5		0.5	dB

4.3.2.6 Voice Band Downlink DAC to BTL

Table 4-15 Electrical specification of Voice band downlink DAC to BTL

Symbol	Parameter description	Condition	Min	Typ	Max	Unit
AVDD	Power supply		2.9	3.3	3.6	V
Output level	Output range	Full Scale, 32 Ohms load, Gain GODL, GODR = 0dB,		5.1		V
		Full Scale, 16 Ohms load, Gain GODL, GODR = 0dB,		4.9		V
		Full Scale, 8 Ohms load, Gain GODL, GODR = 0dB,		4.2		V
Maximum output power		R=32 Ohms		110		mW
		R=16 Ohms		190		mW
		R=8 Ohms		240		mW
SNR		A-weighted, 1kHz sine wave @ Full	85	90		dB

Symbol	Parameter description	Condition	Min	Typ	Max	Unit
		Scale-1dB GODL, GODR = 0dB				
DR		A-weighted, 1kHz sine wave @ Full Scale –60dB GODL/R=0dB	90			dB
THD		1kHz sine wave @ Full Scale –1dB /-6dB GOL/R=-1.5dB, GODL/R=0dB R=8 Ohms			-70	dB
Output noise		A-weighted, RMS Noise level @ 0vpp output		30	35	μV
PSRR		100/450mVpp 217/434/651Hz sine wave is applied to AVDD, input is 0 GODL/R =0dB		75		dB
Output Resistance			8			ohm
Output Capacitance					100	pF

4.3.2.7 Voice Band Downlink DAC to Line out

Table 4-16 Electrical specification of Voice band downlink DAC to Line out

Symbol	Parameter description	Condition	Min	Typ	Max	Unit
AVDD	Power supply		2.9	3.3	3.6	V
Output level	Output range	Full Scale, 10k Ohms load, Gain GODL, GODR = 0dB,		4.98		V
SNR		A-weighted, 1kHz sine wave @ Full Scale-1dB GODL, GODR = 0dB,10kohm loading	90			dB
DR		A-weighted, 1kHz sine wave @ Full Scale –60dB GODL/R=0dB,10kohm loading	90			dB
THD		1kHz sine wave @ Full Scale –1dB /-6dB GOL/R=-1.5dB, GODL/R=0dB, 10kOhm loading			-75	dB

Symbol	Parameter description	Condition	Min	Typ	Max	Unit
Output noise		A-weighted, RMS Noise level @ 0vpp output		36		μV
PSRR		100/450mVpp 217/434/651Hz sine wave is applied to AVDD, input is 0 GODL/R =0dB		84		dB
Output resistance			10			Kohm
Output capacitance					100	pF

4.3.2.8 Linein Record

Table 4-17 Electrical specification of Linein record

Symbol	Parameter Description	Condition	Min.	Typ.	Max.	Unit
AVDD	Analog power supply		3	3.3	3.6	V
DVDD	Digital power supply		1.6	1.8	2	V
Idd	Current consumption				1	uA
Ipd	Power down leakage				10	nA
VFS	Input level	VI Analog full-scale 0 dB input voltage		5	6.6	Vpp
SNR	Signal-to-noise ratio, A-weighted	Gain=0dB	80	85		dB
THD	Total harmonic distortion	Gain=0dB		-70	-60	dB
DR	Dynamic range, A-weighted	Gain=0dB	85	90		dB
	Gain range	3-bit programmable range, @1kHz	-10.5		0	dB
Gp	Gain step		1	1.5	2	dB
Ri	Input resistance	Gain=0dB, Dolphin boost gain=0dB	48	60	72	kOhm
		Gain=-10.5dB, Dolphin boost gain=0dB	165	205	250	kOhm

Note: Input sine wave with a frequency of 1kHz, measurement bandwidth 20Hz – 20kHz.

4.3.2.9 Head detect

Table 4-18 Electrical specification of head detect

Condition: VDDIO=1.8V, Temp=27C					
HEADDETECT_PD	HEADMIC_IN	HEADMIC_DETECT	HEAD_BUTTON	Function Descriptions	Current
(V)	(V)	(V)	(V)		(uA)
0	1.8	1.8	0	Without headset	0.1
0	0.6-1.4	0	0	Headset insert	0.1
0	0	0	1.8	Headset's mic button pressed	0.5
1.8	x	1.8	0	Power down	<1e-3
Condition: VDDIO=2.8V, Temp=27C					
HEADDETECT_PD	HEADMIC_IN	HEADMIC_DETECT	HEAD_BUTTON	Function Descriptions	Current
(V)	(V)	(V)	(V)		(uA)
0	2.8	2.8	0	Without headset	1.3
0	0.9-2.2	0	0	Headset insert	1.6
0	0	0	2.8	Headset's mic button pressed	2.9
2.8	x	2.8	0	Power down (VDDIO=2.8V)	<1e-3

4.3.3 Phase-Locked Loop (PLL)

Table 4-19 Performance of the phase-locked loop

Parameter	Conditions/Comments	Min	Typ	Max	Unit
Power supply	Digital power Analog power		1.1 3.0/2.5		V
Input clock coupling capacitor	External coupling capacitor		1000		pF
Input reference			26		MHz
Frequency Range	MPLL		1000		MHz
	APLL		384		MHz
	DPLL		400		MHz
	TDPLL		768		MHz
cycle to cycle jitter (RMS)	All other circuits on		20		ps
Cycle to cycle jitter (p-p)	All other circuits on		200		ps/cycle

Parameter	Conditions/Comments	Min	Typ	Max	Unit
Settling time		100	400		μs
Sleep mode	Yes				
Idd	3.0V		1		mA
	2.5V		1.5		mA
	1.1V		1.5		mA

Note:

- For MPLL, fin is always at 26 MHz, while for the other three PLLs, fin frequency is the same as the external oscillator.
- TDPLL frequency should always be multiple of 5.12 MHz, for TD-SCDMA Rx/Tx timing.

4.3.4 RTC Oscillator

SC6820 contains an RTC oscillator, for a specific crystal frequency at 32.768 kHz. The 32.768 kHz crystal is connected at RTC32KI and RTC32KO.

Table 4-20 Performance of the 32.768-kHz oscillator

Description	Symbol	Min	Typical	Max	Units
Power supply			1.8		V
Crystal Frequency			32.768		KHz
Frequency tolerance	△f/f	-80		80	ppm
clock duty cycle	δ_{clk32K}	35		65	%
Equivalent series resistance		6		65	KOhm
Drive Level				1	uW
Internal power supply	VRTC		1.8		V
Input High Voltage RTC32XI		0.8 VRTC		--	V
Input Low Voltage RTC32XI		--		0.2 VRTC	V
Input Leakage, RTC32XI				1	uA
Input Capacitance RTC32XI/RTC32XO			18		pF
Amplifier Stabilization Time		2		10	s
Parasitic Resistance RTC32XI/RTC32XO to any node		20			MOhm
Parasitic Capacitance, RTC32XI/RTC32XO			5		pF

Note1: The recommended frequency tolerance of crystal is ±20ppm.

Note2: SC6820 also supports digital 32.768KHz clock input. The digital clock should be connected through a 10-51K Ω series resistor to RTC32KI, while RTC32KO can be left floating. The logic low of this digital clock should be between 0-0.4V while the logic high should be between 1.4-1.8V. The drive strength of this digital clock must be larger than 1mA.

4.3.5 USB 2.0 PHY

The USB 2.0 PHY in SC6820 is fully compliant with USB 1.1 specifications. Please refer to Universal Serial Bus Specification revision 1.1 at http://www.usb.org/developers/docs.

4.3.6 GSM APC DAC

Two general DACs are used to control power ramping and gain in SC6820, which name as GSM APC。It is a all 10 bits D/A converters with a programmable-gain output driver. Special offset cancellation is applied in those DACs.

Physically they copy from the same design (but with different control method),so they almost have the same performance, list as follow,

Table 4-21 Performance of the AGC/APC DACs

Parameter	Conditions/Comments	Min	Typical	Max	Units
Power supply		2.7	3	3.3	V
Resolution			10		bits
Integral non-linearity		-2		+2	LSB
Differential non-linearity		-1		+1	LSB
Settling time			4		μs
Gain range		1.9		2.4	x
Minimum output voltage			0		V
Maximum output voltage	Gain = 2.4		2.9		V
Minimum load resistance			50		kΩ
Maximum load capacitance			50		PF

4.3.7 Auxiliary Analog-to-Digital Converter (ADC)

The auxiliary ADC is a 10-bit successive approximation A/D converter. The ADC has 11 input channels, three are from internal analog circuit used to monitor battery voltage, charging current and voltage and the others are for external usage. Two are specially used for touch panel. Special offset cancellation is applied in the ADC.

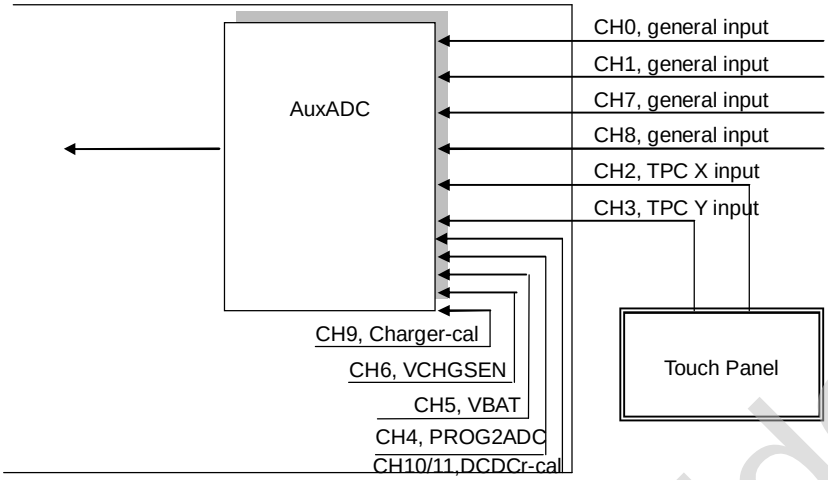


Figure 4-3 AUXADC circuit

Table 4-22 Performance of the Auxiliary ADC

Parameter	Conditions/Comments	Min	Typical	Max	Unit
Power supply		2.7	3	3.3	V
Resolution			10		bits
Integral non-linearity		-2		+2	LSB
Differential non-linearity		-1		+1	LSB
Number of input channels	For external users		4		
Analog input range	Small range		1.2		V
	Large range		3		V
Conversion time				15	μs

4.3.8 Low Dropout Regulators

Table 4-23 Performance of the integrated LDO regulators

Parameter	Comments	Min	Typical	Max	Unit
External Memory Voltage(VDDMEM)					
Status after reset	on				
Application	SDRAM				
Output Voltage	0(default)	1.7	1.8	1.9	V
Output Current				300	mA
Line regulation	Vi=3.6V-4.2V;Io=100mA;	5	10	20	mV
Line Transient Response	Vi=3.6V-4.2V;Io=100mA;Tr=10us	25	50	75	mV
Load regulation	Vi=3.8V; Io=0-200mA;	25	50	75	mV

Parameter	Comments	Min	Typical	Max	Unit
Load Transient Response	Vi=3.8V; Io=0-200mA;Co=2.2uF; Tr=10us	30	60	90	mV
PSRR	F=217Hz,Io=100mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	50	85	120	us
Tpd	Vo=0.1V (Iout=Imax/2)	50	80	120	us
Isleep	Io=0mA	8	10	20	uA
Cext	External cap	2.2	2.2	4.7	uF
Digital 2.8V IO Voltage(VDD28)					
Status after reset	on				
Application	IO/ NAND Flash/LCM				
Output Voltage	00(default)	2.7	2.8	2.9	V
	01	2.9	3.0	3.1	V
	10	2.55	2.65	2.75	V
	11	1.75	1.8	1.85	V
Output Current				200	mA
Line regulation	Vi=3.6V-4.2V;Io=100mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=100mA;Tr=10us	15	25	50	mV
Load Regulation	Vi=3.8V; Io=0-200mA;	30	50	75	mV
Load Transient Regulation	Vi=3.8V; Io=0-200mA;Co=2.2uF; Tr=10us	30	50	75	mV
Short current limit		75	90	120	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=100mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	80	100	120	us
Tpd	Vo=0.1V (Iout=Imax/2)	200	300	400	us
Isleep	Io=0mA	12	15	25	uA
Cext	External cap	2.2	2.2	4.7	uF
Digital 1.8V IO Voltage(VDD18)					
Status after reset	on				
Application	IO/ NAND Flash/LCM				
Output Voltage	00(default)	1.75	1.8	1.85	V
	01	2.7	2.8	2.9	V
	10	1.45	1.5	1.55	V
	11	1.15	1.2	1.25	V
Output Current				200	mA
Line Regulation	Vi=3.6V-4.2V;Io=100mA;	6	12	24	mV

Parameter	Comments	Min	Typical	Max	Unit
Line Transient Regulation	Vi=3.6V-4.2V;Io=100mA;Tr=10us	10	20	30	mV
Load regulation	Vi=3.8V; Io=0-200mA;	30	60	90	mV
Load Transient Regulation	Vi=3.8V; Io=0-200mA;Co=2.2uF; Tr=10us	30	60	90	mV
Short current limit		75	90	120	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=100mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	90	150	225	us
Tpd	Vo=0.1V (Iout=Imax/2)	90	150	225	us
Isleep	Io=0mA	10	15	25	uA
Cext		2.2	2.2	4.7	uF
LDO for RF0(VDDRF0)					
Status after reset	on				
Application	RF/TCXO				
Output Voltage	00(default)	2.75	2.85	2.95	V
	01	2.85	2.95	3.05	V
	10	2.65	2.75	2.85	V
	11	1.75	1.8	1.85	V
Output Current				200	mA
Line regulation	Vi=3.6V-4.2V;Io=100mA;	3	5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=100mA;Tr=10us	5	10	20	mV
Load regulation	Vi=3.8V; Io=0-200mA;	25	50	75	mV
Load Transient Regulation	Vi=3.8V; Io=0-200mA;Co=2.2uF; Tr=10us	25	50	75	mV
PSRR	F=217Hz,Io=100mA,	48	60	72	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	30	50	75	us
Tpd	Vo=0.1V (Iout=Imax/2)	110	160	240	us
Isleep	Io=0mA	30	40	55	uA
Cext		2.2	2.2	4.7	uF
LDO for RF1 (VDDRF1)					
Status after reset	off				
Application	Supply for external terminal				
Output Voltage	00(default)	2.75	2.85	2.95	V
	01	2.85	2.95	3.05	V
	10	2.4	2.5	2.6	V
	11	1.75	1.8	1.85	V

Parameter	Comments	Min	Typical	Max	Unit
Output Current				200	mA
Line regulation	Vi=3.6V-4.2V;Io=100mA;	3	5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=100mA;Tr=10us	5	10	20	mV
Load regulation	Vi=3.8V; Io=0-100mA;	25	50	75	mV
Load Transient Regulation	Vi=3.8V; Io=0-100mA;Co=2.2uF; Tr=10us	25	50	75	mV
PSRR	F=217Hz,Io=100mA,	48	60	72	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	30	50	75	us
Tpd	Vo=0.1V (Iout=Imax/2)	96	160	240	us
Isleep	Io=0mA	32	40	55	uA
Cext		2.2	2.2	4.7	uF
Digital SDIO0 Voltage (VDDSD0)					
Status after reset	off				
Application	SD Card				
Output Voltage	00(default)	2.7	2.8	2.9	V
	01	2.9	3.0	3.1	V
	10	2.4	2.5	2.6	V
	11	1.7	1.8	1.9	V
Output Current				150	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	15	30	45	mV
Load regulation	Vi=3.8V; Io=0-50mA;	15	30	45	mV
Load Transient Regulation	Vi=3.8V; Io=0-50mA;Co=1uF; Tr=10us	25	50	75	mV
Short current limit		75	90	120	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=50mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	20	35	50	us
Tpd	Vo=0.1V (Iout=Imax/2)	110	180	270	us
Isleep	Io=0mA	16	20	30	uA
Cext		1	2.2	4.7	uF
Digital SDIO1 Voltage (VDDSD1)					
Status after reset	off				
Application	SD Card				
Output Voltage	00(default)	2.7	2.8	2.9	V
	01	2.9	3.0	3.1	V

Parameter	Comments	Min	Typical	Max	Unit
	10	2.4	2.5	2.6	V
	11	1.7	1.8	1.9	V
Output Current				150	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	15	30	45	mV
Load regulation	Vi=3.8V; Io=0-50mA;	15	30	45	mV
Load Transient Regulation	Vi=3.8V; Io=0-50mA;Co=1uF; Tr=10us	25	50	75	mV
Short current limit		75	90	120	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=50mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	20	35	50	us
Tpd	Vo=0.1V (Iout=Imax/2)	110	180	270	us
Isleep	Io=0mA	16	20	30	uA
Cext		1	2.2	4.7	uF
General LDO(VDDCAMD0)					
Status after reset	off				
Application	Supply for external sensor				
Output Voltage	00(default)	1.75	1.8	1.85	V
	01	2.7	2.8	2.9	V
	10	1.45	1.5	1.55	V
	11	1.25	1.3	1.35	V
Output Current				100	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	10	20	30	mV
Load regulation	Vi=3.8V; Io=0-50mA;	15	30	45	mV
Load Transient Regulation	Vi=3.8V; Io=0-50mA;Co=1uF; Tr=10us	15	30	45	mV
PSRR	F=217Hz,Io=50mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	12	20	30	us
Tpd	Vo=0.1V (Iout=Imax/2)	110	180	270	us
Isleep	Io=0mA	16	20	30	uA
Cext		1	1	2.2	uF
General LDO (VDDCAMDA)					
Status after reset	off				
Application	Supply for external sensor				

Parameter	Comments	Min	Typical	Max	Unit
Output Voltage	00(default)	2.7	2.8	2.9	V
	01	2.9	3.0	3.1	V
	10	2.4	2.5	2.6	V
	11	1.7	1.8	1.9	V
Output Current				150	mA
Line regulation	Vi=3.6V-4.2V;Io=80mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=80mA;Tr=10us	10	20	30	mV
Load regulation	Vi=3.8V; Io=0-80mA;	15	30	45	mV
Load Transient Regulation	Vi=3.8V; Io=0-80mA;Co=1uF; Tr=10us	15	30	45	mV
PSRR	F=217Hz,Io=50mA,	36	40	50	dB
Cext		1	1	2.2	uF
General LDO (VDDCAMD1)					
Status after reset	off				
Application	Supply for external sensor				
Output Voltage	00(default)	2.7	2.8	2.9	V
	01	3.2	3.3	3.4	V
	10	1.75	1.8	1.85	V
	11	1.15	1.2	1.25	V
Output Current				100	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	10	20	30	mV
Load regulation	Vi=3.8V; Io=0-50mA;	15	30	45	mV
Load Transient Regulation	Vi=3.8V; Io=0-50mA;Co=1uF; Tr=10us	15	30	45	mV
PSRR	F=217Hz,Io=50mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	12	20	30	us
Tpd	Vo=0.1V (Iout=Imax/2)	110	180	270	us
Isleep	Io=0mA	16	20	30	uA
Cext		1	1	2.2	uF
Small battery and Real time clock LDO (VDDBK and VDDRTC)					
Status after reset	On				
Application	Supply for small battery and RTC				
VBATBK Output Voltage	00	2.45	2.6	2.75	V
	01 (default)	2.65	2.8	2.95	V

Parameter	Comments	Min	Typical	Max	Unit
	10	2.85	3.0	3.15	V
	11	3.05	3.2	3.35	V
VBATBK output resistor	00 (default)	160	200	240	Ω
	01	400	500	600	Ω
	10	1200	1500	1800	Ω
	11	1600	2000	2400	Ω
VDDRTC Output Voltage	00(default)	1.75	1.8	1.85	V
	01	1.65	1.7	1.75	V
	10	1.55	1.6	1.65	V
	11	1.45	1.5	1.55	V
Output Current				1	mA
Line regulation	Vi=3.6V-4.2V;Io=0.2mA;	8	15	30	mV
Load regulation	Vi=3.8V; Io=0-0.2mA	5	10	20	mV
Tpu	Supply ramp from 0 to 3.6v in 10µs	50	80	120	us
Isleep	Vbat Vbuk	15 10	**18** **11.5**	24 17	uA uA
Cext		0.01	0.01	0.047	uF
SIMO LDO (VSIM0)					
Status after reset	On				
Application	Supply for SIM Card				
Output Voltage	00(default)	1.7	1.8	1.9	V
	01	2.8	2.9	3.0	V
	10	2.9	3.0	3.1	V
	11	3.0	3.1	3.2	V
Output Current				60	mA
Line regulation	Vi=3.6V-4.2V;Io=30mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=30mA;Tr=10us	10	20	30	mV
Load regulation	Vi=3.8V; Io=0-30mA;	15	30	45	mV
Load Transient Regulation	Vi=3.8V; Io=0-30mA;Co=1uF; Tr=10us	15	30	45	mV
Short current limit		25	30	45	mA
Current limit	Vi=3.8V	120	150	225	mA
PSRR	F=217Hz,Io=30mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	60	100	150	us
Tpd	Vo=0.1V (Iout=Imax/2)	150	250	375	us

Parameter	Comments	Min	Typical	Max	Unit
Isleep	Io=0mA	12	15	23	uA
Cext		1	1	2.2	uF
SIM1 LDO (VSIM1)					
Status after reset	Off				
Application	Supply for SIM Card				
Output Voltage	00(default)	1.7	1.8	1.9	V
	01	2.8	2.9	3.0	V
	10	2.9	3.0	3.1	V
	11	3.0	3.1	3.2	V
Output Current				60	mA
Line regulation	Vi=3.6V-4.2V;Io=30mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=30mA;Tr=10us	10	20	30	mV
Load regulation	Vi=3.8V; Io=0-30mA;	15	30	45	mV
Load Transient Regulation	Vi=3.8V; Io=0-30mA;Co=1uF; Tr=10us	15	30	45	mV
Short current limit		25	30	45	mA
Current limit	Vi=3.8V	120	150	225	mA
PSRR	F=217Hz,Io=30mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	60	100	150	us
Tpd	Vo=0.1V (Iout=Imax/2)	150	250	375	us
Isleep	Io=0mA	12	15	23	uA
Cext		1	1	2.2	uF
Analog BB Voltage(AVDDBB)					
Status after reset	On				
Application	Supply for BB circuit, for example ADC/DAC/APC				
Output Voltage	00(default)	2.9	3.0	3.1	V
	01	3.0	3.1	3.2	V
	10	2.8	2.9	3.0	V
	11	2.7	2.8	2.9	V
Output Current				60	mA
Line regulation	Vi=3.6V-4.2;Io=50mA;	3	5	10	mV
Line Transient Regulation	Vi=3.6V-4.2;Io=50mA;Tr=10us	5	10	20	mV
Load regulation	Vi=3.8V; Io=0-100mA;	15	30	60	mV
Load Transient Regulation	Vi=3.8V; Io=0-50mA;Co=2.2uF; Tr=10us	25	50	100	mV
PSRR	F=217Hz,Io=50mA,	48	60	72	dB

Parameter	Comments	Min	Typical	Max	Unit
Tpu	Supply ramp from 0 to 3.6v in 10μs	36	60	90	us
Tpd	Vo=0.1V (Iout=Imax/2)	90	150	225	us
Isleep	Io=0mA	32	40	60	uA
Cext		2.2	2.2	4.7	uF
Analog VB Voltage(AVDDVB)					
Status after reset	Off				
Application	VB analog/VB output				
Output Voltage	00(default)	3.2	3.3	3.4	V
	01	3.3	3.4	3.5	V
	10	3.1	3.2	3.3	V
	11	2.8	2.9	3.0	V
Output Current				100	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	3	5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	5	10	20	mV
Load regulation	Vi=3.8V; Io=0-100mA;	8	15	30	mV
Load Transient Regulation	Vi=3.8V; Io=0-50mA;Co=4.7F; Tr=10us	25	50	75	mV
PSRR	F=217Hz,Io=50mA,	48	60	72	dB
Tpu	Supply ramp from 0 to 3.6v in 10μs	30	50	75	us
Tpd	Vo=0.1V (Iout=Imax/2)	210	350	500	us
Isleep	Io=0mA	32	40	60	uA
Cext		2.2	2.2	4.7	uF
USB High Voltage(VDDUSBH)					
Status after reset	Off				
Application	USB IP				
Output Voltage	00 (default)	3.2	3.3	3.4	V
	01	3.3	3.4	3.5	V
	10	3.1	3.2	3.3	V
	11	3.0	3.1	3.2	V
Output Current				60	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	10	20	40	mV
Load regulation	Vi=3.8V; Io=0-30mA;	15	30	60	mV
Load Transient Regulation	Vi=3.8V; Io=0-30mA;Co=2.2uF; Tr=10us	15	30	60	mV
PSRR	F=217Hz,Io=50mA,	36	40	50	dB

Parameter	Comments	Min	Typical	Max	Unit
Tpu	Supply ramp from 0 to 3.6v in 10µs	9	15	23	us
Tpd	Vo=0.1V (Iout=Imax/2)	240	400	600	us
Isleep	Io=0mA	12	15	23	uA
Cex		1	1	2.2	uF
VDD25(VDD25)					
Status after reset	On				
Application	PLL and EFUSE				
Output Voltage	00 (default)	2.4	2.5	2.6	V
	01	2.65	2.75	2.85	V
	10	2.9	3.0	3.1	V
	11	2.8	2.9	3.0	V
Output Current				60	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	10	20	40	mV
Load regulation	Vi=3.8V; Io=0-30mA;	20	40	80	mV
Load Transient Regulation	Vi=3.8V; Io=0-30mA;Co=2.2uF; Tr=10us	20	40	80	mV
Tpu	Supply ramp from 0 to 3.6v in 10µs	60	100	200	us
PSRR	F=217Hz,Io=30mA,	48	60	72	dB
Cex		2.2	2.2	4.7	uF
DVDD18(VDD_A)					
Status after reset	On				
Application	Analog 1.8V power				
Output Voltage		1.7	1.8	1.9	V
Output Current				80	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	10	20	40	mV
Load regulation	Vi=3.8V; Io=0-30mA;	20	40	80	mV
Load Transient Regulation	Vi=3.8V; Io=0-30mA;Co=2.2uF; Tr=10us	20	40	80	mV
PSRR	F=217Hz,Io=50mA,	36	40	50	dB
Cex		1	1	2.2	uF
WIF0 LDO Voltage (VDDWIF0)					
Status after reset	Off				
Application	Supply for external Wif terminal				
Output Voltage	00	2.7	2.8	2.9	V

Parameter	Comments	Min	Typical	Max	Unit
	01(default)	3.15	3.3	3.45	V
	10	1.7	1.8	1.9	V
	11	1.1	1.2	1.3	V
Output Current				200	mA
Line regulation	Vi=3.6V-4.2V;Io=100mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=100mA;Tr=10us	12	25	50	mV
Load Regulation	Vi=3.8V; Io=0-200mA;	25	50	100	mV
Load Transient Regulation	Vi=3.8V; Io=0-200mA;Co=2.2uF; Tr=10us	25	50	100	mV
Short current limit		75	90	120	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=100mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	60	100	150	us
Tpd	Vo=0.1V (Iout=Imax/2)	180	300	450	us
Isleep	Io=0mA	12	15	23	uA
Cext	External cap	2.2	2.2	4.7	uF
WIF1 LDO Voltage (VDDWIF1)					
Status after reset	Off				
Application	Supply for external Wif terminal				
Output Voltage	00	2.7	2.8	2.9	V
	01(default)	3.15	3.3	3.45	V
	10	1.7	1.8	1.9	V
	11	1.1	1.2	1.3	V
Output Current				200	mA
Line regulation	Vi=3.6V-4.2V;Io=100mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=100mA;Tr=10us	12	25	50	mV
Load Regulation	Vi=3.8V; Io=0-200mA;	25	50	100	mV
Load Transient Regulation	Vi=3.8V; Io=0-200mA;Co=2.2uF; Tr=10us	25	50	100	mV
Short current limit		75	90	120	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=100mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	60	100	150	us
Tpd	Vo=0.1V (Iout=Imax/2)	180	300	450	us
Isleep	Io=0mA	12	15	23	uA

Parameter	Comments	Min	Typical	Max	Unit
Cext	External cap	2.2	2.2	4.7	uF
SIM2 LDO (VSIM2)					
Status after reset	Off				
Application	Supply for SIM Card or CMMB RF				
Output Voltage	00	2.7	2.8	2.9	V
	01	2.9	3	3.1	V
	10(default)	1.7	1.8	1.9	V
	11	1.3	1.2	1.1	V
Output Current				**200**	mA
Line regulation	Vi=3.6V-4.2V;Io=30mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=30mA;Tr=10us	10	20	40	mV
Load regulation	Vi=3.8V; Io=0-30mA;	15	30	60	mV
Load Transient Regulation	Vi=3.8V; Io=0-30mA;Co=1uF; Tr=10us	15	30	60	mV
Short current limit		130	150	200	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=30mA,	48	60	72	dB
Tpu	Supply ramp from 0 to 3.63v in 10µs	72	120	180	us
Tpd	Vo=0.1V (Iout=Imax/2)	150	250	333	us
Isleep	Io=0mA	12	15	23	uA
Cext		2.2	2.2	4.7	uF
SIM3 LDO (VSIM3)					
Status after reset	Off				
Application	Supply for SIM Card or CMMB RF				
Output Voltage	00	2.7	2.8	2.9	V
	01	2.9	3	3.1	V
	10(default)	1.7	1.8	1.9	V
	11	1.3	1.2	1.1	V
Output Current				**200**	mA
Line regulation	Vi=3.6V-4.2V;Io=30mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=30mA;Tr=10us	10	20	40	mV
Load regulation	Vi=3.8V; Io=0-30mA;	15	30	60	mV
Load Transient Regulation	Vi=3.8V; Io=0-30mA;Co=1uF; Tr=10us	15	30	60	mV
Short current limit		130	150	200	mA
Current limit	Vi=3.8V	410	480	640	mA

Parameter	Comments	Min	Typical	Max	Unit
PSRR	F=217Hz,Io=30mA,	48	60	72	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	72	120	180	us
Tpd	Vo=0.1V (Iout=Imax/2)	150	250	333	us
Isleep	Io=0mA	12	15	23	uA
Cext		2.2	2.2	4.7	uF
LDO_PA					
Status after reset	off				
Application	Audio PA				
Output voltage	000	2.7	2.9	3.1	V
	001	2.8	3.0	3.2	V
	010	2.9	3.1	3.3	V
	011	3.0	3.2	3.4	V
	100(default)	3.1	3.3	3.5	V
	101	3.2	3.4	3.6	V
	110	3.3	3.5	3.6	V
	111	3.4	3.6	-	V
Output current				400	mA
Line regulation	Vsupply=3.6->4.2V, Iout=200mA	5	10	20	mV
Line transient regulation	Vsupply=3.6->4.2V, Iout=200mA, Trise=10us	10	20	40	mV
Load regulation	Vsupply=3.8V, Iout=0->400mA	40	80	160	mV
Load transient regulation	Vsupply=3.8V, Iout=0->400mA, Trise=10us	50	100	200	mV
PSRR	Freq=217Hz, Iout=400mA	36	40	50	dB
Time to power up	Vsupply=0->3.8V, Trise=10us	60	100	150	us
Time to power down	Vout=0.1V, Iout=400mA	180	300	450	us
Isleep	Iout=0mA	12	15	23	uA
Output capacitor	Required for stability and ripple rejection	4.7	4.7	10	µF

Note1. There are two structures for these intergrated LDOs.

Note2. The PSRR listed means the worst value for all loading statuses and cover all frequency range.

4.3.9 Charger

Table 4-24 Performance of charger circuit

Symbol	Description	Condition	Min	Typical	Max	Unit
VCHG	Power supply pin	Charging condition	4.5	5.0	5.5	V
Vtolerance	Maxim tolerance				18	V

Symbol	Description	Condition	Min	Typical	Max	Unit
	voltage at VCHG					
Vuvh	Supply under voltage high threshold	AVDD low to high	4.3	4.5	4.7	V
Vuvl	Supply under voltage low threshold	AVDD high to low	4.05	4.25	4.45	V
Vuvhys	Supply under voltage hysteresis		160	200	240	mV
Vtrickle	Trickle threshold voltage		2.5	2.7	2.9	V
Itrickle	Trickle charge current	VBAT < Vtrickle	40	50	60	mA
Vrego	Regulated output voltage	Floating or when charging finished	4.1	4.2	4.3	V
Imbat	Charging current	Adapter mode 00 01 10 11 USB mode 00 01 10 11	 360 540 720 900 270 360 450 450	 400 600 800 1000 300 400 500 500	 440 660 880 1100 330 440 550 550	mA
Istop	Charging stop current threshold			Imbat/10		mA
Idd	Current consumption			0.5	1	mA
Istdby	Standby current	When charging finished		1		μA
Ipd	Power down leakage				1	μA
Irev	Reverse leakage current	VCHG=0; Vrego=4.2V			1	μA

Note1: Hardware stops charging if VCHG is higher than 9V and the maximum value of VCHG can be set by software. The higher maximum value of VCHG, the stricter Vds requirement of external MOSFET.

Note2: The value set by software should be 10% higher than maximum value of VCHG listed in table to guarantee all chips can stop charging over the maximum value of VCHG.

Note3: Istop can be set according to specific requirement.

4.3.10 DC-DC

Table 4-25 Performance of DC-DC circuit

Table 4-26 Performance of DC-DC circuit

Parameter	Comments/Conditions	Min	Typical	Max	Unit
DCDC for ARM					
Status after reset	on				
Application	Digital core power				
Output voltage	000	0.55	0.65	0.75	V
	001	0.6	0.7	0.8	V
	010	0.7	0.8	0.9	V
	011	0.8	0.9	1	V
	100	0.9	1.0	1.1	V
	101	1	1.1	1.2	V
	110(default)	1.1	1.2	1.3	V
	111	1.2	1.3	1.4	V
Trim voltage	Trim votage step (32 step)	2	3	4	mv
Output current				500	mA
Line regulation	Vsupply=3.6->4.2V, Iout=200mA	5	10	20	mV
Line transient regulation	Vsupply=3.6->4.2V, Iout=200mA, Trise=10us	15	30	60	mV
Load regulation	Vsupply=3.8V, Iout=0->400mA	40	80	160	mV
Load transient regulation	Vsupply=3.8V, Iout=0->400mA, Trise=10us	50	100	200	mV
Time to power up	Vsupply=0->4.3V, Trise=10us	60	100	150	us
Switching frequency		1	1.5	2.25	MHz
Isleep	Iout=0mA	72	90	100	uA
Effiency	100mA loading	80	85	90	%
Parameter	**Comments/Conditions**	**Min**	**Typical**	**Max**	**Unit**
DCDC for other Core					
Status after reset	on				
Application	Digital core power				
Output voltage	000	0.55	0.65	0.75	V
	001	0.6	0.7	0.8	V
	010	0.7	0.8	0.9	V
	011	0.8	0.9	1	V
	100	0.9	1.0	1.1	V
	101(default)	1	1.1	1.2	V
	110	1.1	1.2	1.3	V

Parameter	Comments/Conditions	Min	Typical	Max	Unit
	111	1.2	1.3	1.4	V
Trim voltage	Trim votage step (32 step)	2	3	4	mv
Output current				500	mA
Line regulation	Vsupply=3.6->4.2V, Iout=200mA	5	10	20	mV
Line transient regulation	Vsupply=3.6->4.2V, Iout=200mA, Trise=10us	15	30	60	mV
Load regulation	Vsupply=3.8V, Iout=0->400mA	40	80	160	mV
Load transient regulation	Vsupply=3.8V, Iout=0->400mA, Trise=10us	50	100	200	mV
Time to power up	Vsupply=0->4.3V, Trise=10us	60	100	150	us
Switching frequency		1	1.5	2.25	MHz
Isleep	Iout=0mA	72	90	100	uA
Effiency	100mA loading	80	85	90	%

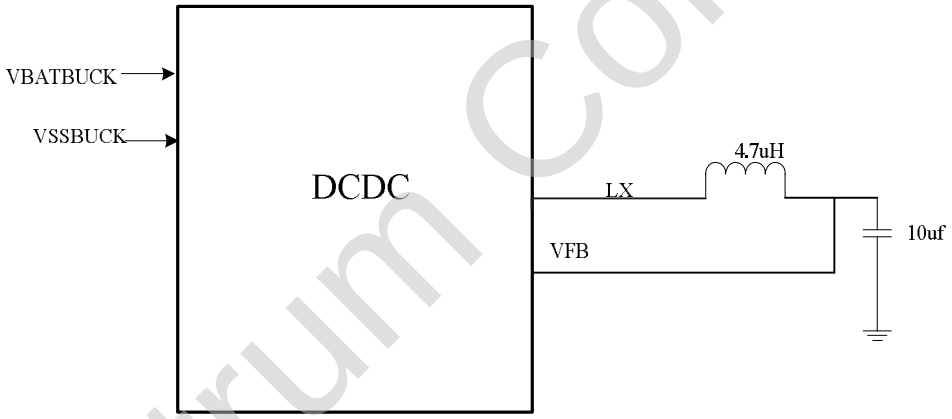


Figure 4-4 DCDC application diagram

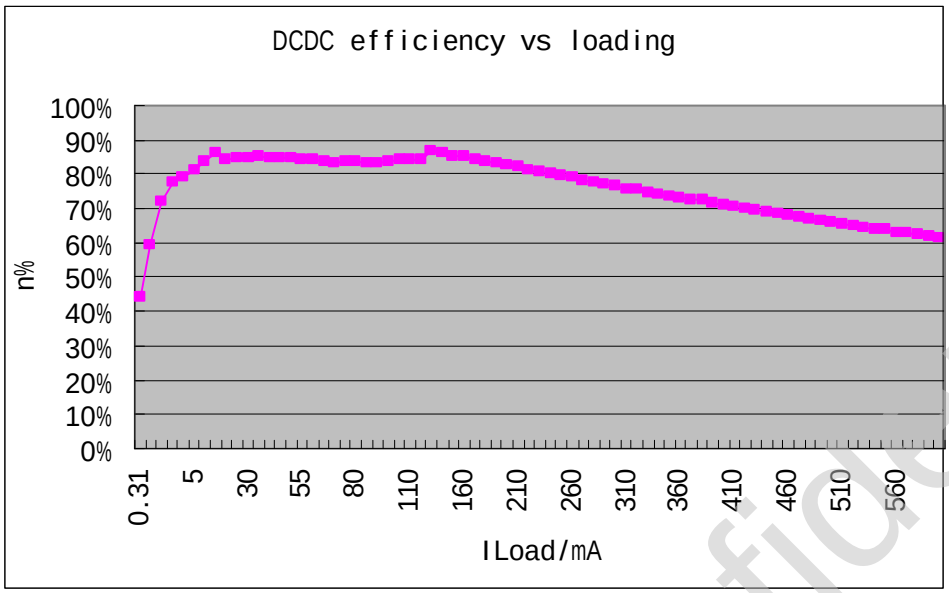


Figure 4-5 DCDC efficiency vs loading

4.3.11 Audio PA

The block is an audio amplifier, which is Class-AB mode and Class-D mode optional. It can deliver 800mW of continuous average power into a mono 8Ω bridged-tied load (BTL) with 1% THD+N in Class-D mode or 500mW with 0.1% THD+N in Class-AB mode, using a 3.8V power supply.

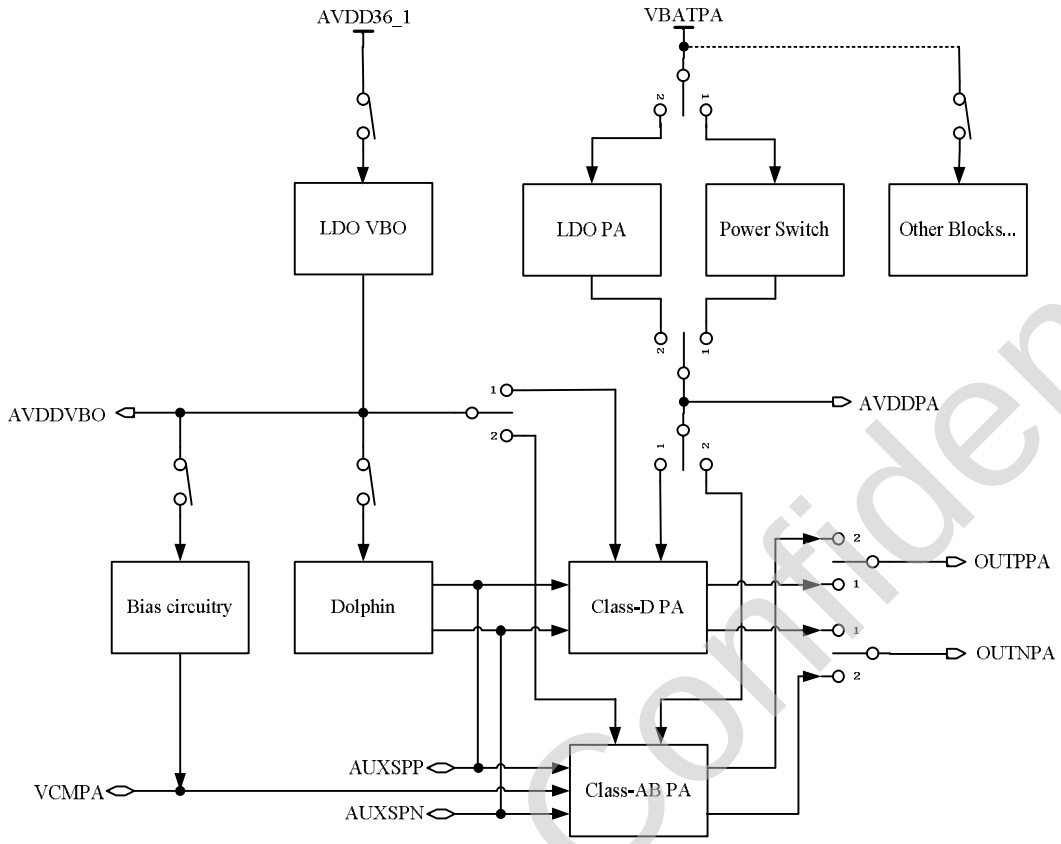


Figure 4-6 Audio PA structure

Table 4-27 Absolute maximum ratings

Parameter	Description	Condition	MIN	TYP	MAX	UNIT
VBAT	Driver power supply		3.6	3.8	5.2	V
AVDD	Analog power supply		3.0	3.3	3.6	V
TA	Operating free-air temperature		0		80	C

Table 4-28 Performance of PA circuit

Test condition: VBAT=3.8V, AVDDVB=3.3V, AVDDPA=3.6V, T=27ºC, Rload=8Ω. Input sine wave with a frequency of 1kHz, measurement bandwidth 20-20kHz, unless otherwise specified.

Parameter	Description	Condition		MIN	TYP	MAX	UNIT
Psleep	Sleep mode power consumption				10		uA
Idd	Current consumption	Class-AB			15		mA
		Class-D			10		mA
Pomax	Maximum output	Class-AB	THD>=1%		500		mW

	power		VBAT=3.3V, AVDDVB=AVDDPA =2.9V, THD>=1%		350		mW
		Class-D	THD>=1%	700*	800		mW
			VBAT=3.3V, AVDDVB=AVDDPA =2.9V, THD>=1%		500		mW
			Rload=4Ω, THD>=1%		1.2		W
PSRR(Note1)	Power supply rejection ratio	Class-AB			-75	-55	dB
		Class-D			-70	-45	dB
THD	Total harmonic distortion plus noise	Class-AB	Po=0.5W		0.2%		
			Po=0.3W		0.1%		
		Class-D	Po=0.7W		1%		
			Po=0.3W		0.5%		
SNR	Signal-to-noise ratio	Class-AB	Po=0.5W		90		dB
		Class-D	Po=0.7W		70		dB
			Po=0.3W		80		dB
Vn(Note2)	Output voltage noise	Class-AB			15	50	uV
		Class-D			100	150	uV
Efficiency	Power efficiency	Class-AB	Po=0.5W		50%		
			Po=0.3W		30%		
		Class-D	Po=0.7W		85%		
			Po=0.3W		80%		
Gain		Class-AB			6		dB
		Class-D			9		dB
fsw	Switching frequency	Class-D		0.5	0.6	0.7	MHz
tsw	Power switch slow start-up time				1	2	ms
tcom	PA Class-AB mode common voltage fast start-up time				30	50	ms
Area	Layout area				0.84		mm2

Note *: When set Dolphin's control register GODL=GODR=-6dB, set digital gain=Full scale-1dB, the maximum output power on the speaker (with bead and 1nF capacitor low pass filter) with THD>=1% is 700mW.

Note 1: Ripple voltage on VBAT is 0.3Vpp at 217Hz and 1kHz.

Note 2: When PA's input comes from Dolphin, the output voltage noise will be 50uV in Class-AB mode, 150uV in Class-D mode.

4.3.12 LCD Backlight LED Driver

The LCD Backlight module provides six matched current sources, sinks up to 24.75 mA of load current to accommodate each of the six White LEDs. The module uses current mirror to construct LCD backlight driver. The reference current source ISET is set with an external resistor R. Each of the matched current regulators has a 100:1 current ratio between the VLEDx outputs (one channel) and the ISET currents. It requires no charge pump. Brightness can be controlled by software. The module is in shut down mode when the whtled_pd is active.

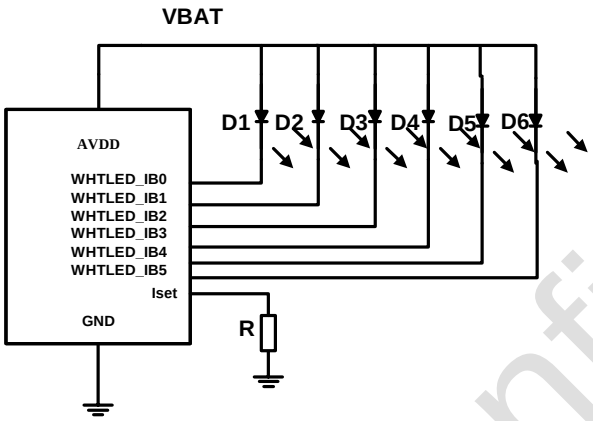


Figure 4-7 LCD backlight LED driver application

Note1: D1 in the diagram must be connected to a LED when in use, otherwise the LED driver current control bits will not be effective.

Table 4-29 Peformance of LCD backlight LED driver

Parameter	Conditions/Comments	Min	Typical	Max	Unit
Status after reset	off				
Output current	00000(min current) (default)		1.5		mA
	00001		2.25		
	00010		3.0		
	00011		3.75		
	00100		4.5		
	00101		5.25		
	00110		6.0		
	00111		6.75		
	01000		7.5		
	01001		8.25		
	01010		9		
	01011		9.75		
	01100		10.5		
	01101		11.25		
	01110		12.0		
	01111		12.75		

	10000		13.5		
Output current	10001		14.25		mA
	10010		15.0		
	10011		15.75		
	10100		16.5		
	10101		17.25		
	10110		18.0		
	10111		18.75		
	11000		19.5		
	11001		20.25		
	11010		21.0		
	11011		21.75		
	11100		22.5		
	11101		23.25		
	11110		24.0		
	11111(max current)		24.75		

4.3.13 Keypad Backlight LED Driver

The keypad backlight driver is constructed with current mirror.

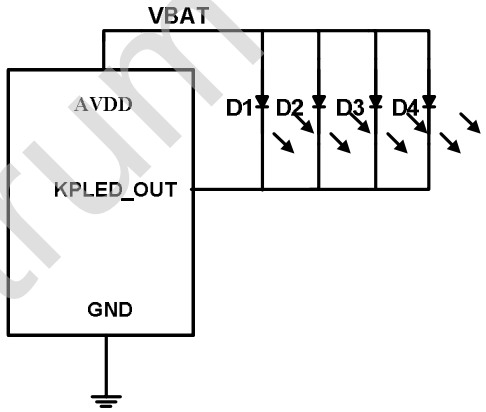


Figure 4-8 Keypad backlight LED driver application

Table 4-30 Performance of Keypad backlight LED driver

Parameter	Conditions/Comments	Min	Typical	Max	Unit
Status after reset	off				
Output current	000(min current) (default)		5		mA
	001		10		
	010		15		
	011		20		

	100		25		
	101		30		
	110		35		
	111		40		

4.3.14 Vibarator

The vibrator driver is constructed with current mirror.

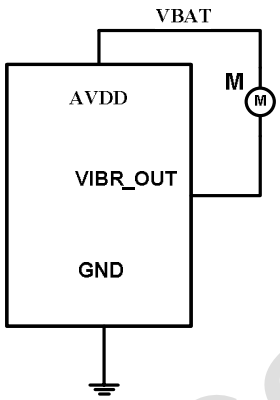


Figure 4-9 Vibrator driver application

Table 4-31 Performance of Vibrator driver

Parameter	Conditions/Comments	Min	Typical	Max	Unit
Status after reset	off				
Output current	0000 (default)		20		mA
	0001		30		
	0010		40		
	0011		50		
	0100		60		
	0101		70		
	0110		80		
	0111		90		
	1000		100		mA
	1001		110		
	1010		120		
	1011		130		
	1100		140		
	1101		150		
	1110		160		
	1111		170		

5 Micro-Controller Unit Subsystem

SC6820 has two embedded processor cores: CortexA5 and Ceva-X1622. In general, the MCU and DSP control the operation of various ASIC hardware modules. The MCU or DSP prepares the data that needs the ASIC to process and sets up some control registers that tells the ASIC how to process the data. Therefore, the software control interface consists of data memories and control registers. The software interface sections define the organization of the data memories and the meanings of control register bits.

5.1 Processor

SC6820 contains one 32-bit RSIC core, CortexA5, with 32kB L1 cache for data and program and also with 128KB L2 cache.

ARM Memory Map

On the ARM side, the address bus is 32-bit wide and the address map is presented in this section. In order to support multiple boot modes, the ARM memory space can be remapped after reset.

Table 5-1 SC6820 ARM memory address map after reset

Address Range	Memory Sector	Sub-Sector	Note
0x0000_0000 – 0x0FFF_FFFF	External Memory Space		256M bytes
0x1000_0000 – 0x1FFF_FFFF	reserved		
0x2000_0000 – 0x200F_FFFF	External Memory Control Register		
0x2010_0000 – 0x201F_FFFF	DMA Control Register		
0x2020_0000 – 0x202F_FFFF	DCAM Control Register		
0x2030_0000 – 0x203F_FFFF	USB 2.0		
0x2040_0000 – 0x2040_0FFF	Bus Monitor 0		
0x2040_1000 – 0x2040_1FFF	Bus Monitor 1		
0x2050_0000 – 0x205F_FFFF	SDIO0 Control Register		
0x2060_0000 – 0x206F_FFFF	SDIO1 Control Register		
0x2070_0000 – 0x207F_FFFF	LCD Control Register		
0x2080_0000 – 0x208F_FFFF	Rotation Control Register		

Address Range	Memory Sector	Sub-Sector	Note
0x2090_0000 – 0x209F_FFFF	AHB Global Control Register		
0x20A0_0000 – 0x20AF_FFFF	AXI Bus Monitor		Monitor the AXI bus between ARM and EMC
0x20B0_0000 – 0x20BF_FFFF	DRM Control Register		
0x20C0_0000 – 0x20CF_FFFF	VSP Control Register		
		0X20C0_0000	Global Registers
		0X20C0_0400	BSM
		0X20C0_0800	VLD
		0X20C0_0C00	VLC
		0X20C0_1000	DCT
		0X20C0_1400	MCA
		0X20C0_1800	MBC
		0X20C0_1C00	DBK
		0X20C0_2000	MEA
0x20D0_0000 – 0x20DF_FFFF	GPU_ACC Control Register		
0x20E0_0000 – 0x20EF_FFFF	Reserved		
0x3000_0000 – 0x3FFF_FFFF	Reserved		
0x4000_0000 – 0x4FFF_FFFF	Internal On Chip RAM space/ Internal On Chip ROM space	There are three RAMs used as Internal RAM. IRAM0 0x4000_0000 – 0x4000_3FFF Dedicate for ARM (16 KB) IRAM1 0x4000_4000 – 0x4000_7FFF Dedicate for ARM (16 KB) IRAM2 0x4000_8000 – 0x4000_AFFF Share with DCAM (12 KB)	If remap = 0: Internal On Chip RAM Space 0x4000_0000 – 0x4000_7FFF is used. If remap = 1: Internal On Chip ROM Space
0x5000_0000 – 0x5FFF_FFFF	Share Memory with DSP	0x5000_0000 – 0x5000_0FFF Dual Port Memory Shared with DSP (4	

Address Range	Memory Sector	Sub-Sector	Note
		KB)	
0x6000_0000 – 0x6FFF_FFFF	NAND Controller Space		
0x7000_0000 – 0x7FFF_FFFF	DSP-Side Space	Map to 0x0000_0000 – 0x0FFF_FFFF space on DSP-side	
0x8000_0000 – 0x8FFF_FFFF	Peripheral Address Space		
	0x8000_0000	Reserved	
	0x8000_3000	INTC	
	0x8100_0000	General RTC Timers	
	0x8200_0000	ADI master	
	0x8200_0040	Watch dog	Analog control
	0x8200_0080	Real Time Clock	Analog control
	0x8200_0100	Dophin MC	Analog control
	0x8200_0180	Pin reg	Analog control
	0x8200_0280	Touch panel	Analog control
	0x8200_0300	Aux ADC	Analog control
	0x8200_0380	INTC	Analog control
	0x8200_03c0	Charger WDG	Analog control
	0x8200_0400	COM slave	Analog control
	0x8200_0480	GPIO	Analog control
	0x8200_0600	Ana_reg	Analog control
	0x8200_0700	EIC	Analog control
	0x8200_3000	Voice Band	
	0x8300_0000	UART0	
	0x8400_0000	UART1	
	0x8500_0000	SIM Card0	
	0x8500_3000	SIM Card1	
	0x8600_0000	I2C0	
	0x8600_1000	I2C1	
	0x8600_2000	I2C2	
	0x8600_3000	I2C3	
	0x8700_0000	Keypad	
	0x8700_3000	System Counter0	
	0x8800_0000	PWM	

Address Range	Memory Sector	Sub-Sector	Note
	0x8900_0000	Efuse	
	0x8A00_0000	GPIO	
	0x8A00_1000	EIC	
	0x8B00_0000	Global registers	
	0x8C00_0000	Chip pin registers	
	0x8D00_0000	EPT	
	0x8E00_0000	UART 2	
	0x8E00_1000	IIS0	
	0x8E00_2000	SPI0	
	0x8E00_3000	SPI1	
	0x8E00_4000	IIS1	
	0x8F00_0000	Reserved	
0x9000_0000 – 0x9FFF_FFFF	Reserved		
0xA000_0000- 0xA000_FFFF	Coresight components		
	0xA000_0000- 0xA000_0FFF	Coresight debug rom table	
	0xA000_1000- 0xA000_1FFF	Coresight ETB	
	0xA000_2000- 0xA000_2FFF	Coresight CTI	
	0xA000_3000- 0xA000_3FFF	Coresight TPIU	
	0xA000_4000- 0xA000_4FFF	Coresight Funnel	
	0xA000_7000- 0xA000_7FFF	A5 integration rom table	
	0xA000_8000- 0xA000_8FFF	A5 debug unit	
	0xA000_9000- 0xA000_9FFF	A5 PMU	
	0xA000_A000- 0xA000_AFFF	A5 integration CTI	
	0xA000_B000- 0xA000_BFFF	ETM	

Address Range	Memory Sector	Sub-Sector	Note
	0xA000_C000- 0xA000_FFFF	Reserved	
0xA001_0000- 0xA001_FFFF	MALI		
0xA002_0000- 0xA00F_FFFF	Reserved		
0xA010_0000- 0xA01F_FFFF	CPU NIC301		
0xA020_0000- 0xA1FF_FFFF	Reserved		
0xA200_2000- 0xA200_2FFF	L2 cache controller		
0xA200_3000 – 0xBFFF_FFFF	Reserved		
0xC000_0000 – 0xCFFF_FFFF	External Memory Space		
0xD000_0000 – 0xDFFF_FFFF	Reserved		
0xE000_0000 – 0xEFFF_FFFF	External Memory Space (in case using 4Gb DDR, this area should be second half)		
0xF000_0000 – 0xFFFE_FFFF	Reserved		
0xFFFF_0000	Internal On Chip ROM Space / Internal On-chip RAM space	If remap = 0: Internal On Chip ROM Space 0xFFFF_0000 – 0xFFFF_7FFF is used. If remap = 1: Internal On Chip RAM Space	32K bytes

It should be noted that:

1. The re-map (address space swapping) among the on chip RAM and internal ROM is controlled only by write value to remap control bit when system was powered up.

5.2 External Memory Controller

5.2.1 Overview

The EMC is a multiple AHB channels and one AXI channel external memory controller, and it supports only DRAM.

- 16-bit SDR-SDRAM and DDR-SDRAM
- 32-bit SDR-SDRAM and DDR-SDRAM

5.2.2 Features

5.2.2.1 AHB Related Features

General features:

- Support multiple AHB channel.
- Support 32-bit AHB and 64-bit AHB
- Support AHB big-endian or AHB little-endian
- Support multiple options for data endian converting
- Support asynchronous mode and synchronous mode between AHB clock and EMC clock (configurable)
- Support all AHB-compatible transaction.
- Support a FIFO for read in each channel
- Support a single-buffer or double-buffer (configurable) for write in each channel
- Support automatically channel closing or forcedly channel closing (configurable) for power saving

5.2.2.2 AXI Related Features

General features:

- Support one AXI channel.
- Support 64-bit AXI
- Support AXI big-endian or AXI little-endian
- Support multiple options for data endian converting
- Support asynchronous mode and synchronous mode between AXI clock and EMC clock (configurable)
- Support all AXI-compatible transaction.
- Support a FIFO for command (write address and read address) in the channel
- Support a FIFO for read in the channel
- Support a FIFO for write in the channel
- Support automatically channel closing or forcedly channel closing (configurable) for power saving

5.2.2.3 Channel Multiplex Features

- 4-level configurable priority.
- For the same priority, robin-round algorithm is used.
- For the same priority, read bursts and write bursts are taken with the same priority.

5.2.2.4 External Memory Related Features

Device type:

- All kinds of 16-bit SDR-SDRAM
- All kinds of 16-bit DDR-SDRAM
- All kinds of 32-bit SDR-SDRAM
- All kinds of 32-bit DDR-SDRAM

DRAM Operation mode features:

- Support SDR-SDRAM and DDR-SDRAM.
- Support from 16Mbit to 8Gbit SDRAM. (Still no data sheet for single-die 1G/2G/4G/8G bit SDRAM).
- Support up to 2 CS. And all SDRAM must have the same type.
- Support 4-bank.
- Support 11/12/13/14-bit row width.
- Support 8/9/10/11/12-bit column width.
- Support 16/32-bit data width.
- For 16-bit SDR, support 2/4/8/16/32-burst

  For 32-bit SDR, support 1/2/4/8/16-burst

  For 16-bit DDR, support 2/4/8/16/32-burst

  For 32-bit DDR, support 2/4/8/16-burst
- Support 1/1.5/2/2.5/3/3.5 CAS latency.
- Support 0/0.5/1/1.5 WRITE latency.
- Only support sequential type, not support interleave type.
- Support configurable auto-precharge bit location.
- Support configurable mode register and extended mode registers.

DRAM Timing features:

- All timing parameters of SDR-SDRAM and DDR-SDRAM can be met by controlling EMC.
- Support configurable auto refresh interval time tREF.
- Support configurable Minimum PRECHARGE(m) to ACTIVE(m) delay tRP.
- Support configurable Minimum ACTIVE(m) to READ/WRITE(m) delay tRCD.
- Support configurable Minimum ACTIVE(m) to ACTIVE(n) delay tRRD.
- Support configurable Minimum ACTIVE(m) to ACTIVE(m) delay tRC. But tRC and tRAS make use of the same configuration register to control timing. That is, the configuration register of tRAS also MUST guarantee tRC.
- Support configurable Minimum ACTIVE(m) to PRECHARGE(m) delay tRAS.
- Support configurable Minimum WRITE(m) to PRECHARGE(m) delay tWR.
- Support configurable AUTO REFRESH command period tRFC/tRC/tARFC.
- Support configurable exit SELF REFRESH to ACTIVE command time tXSR/tSREX/tSRFX.
- Support configurable LOAD MODE REGISTER command to ACTIVE or REFRESH command delay tMRD.
- Support configurable Minimum read to write turn around delay tRTW.
- Support configurable Minimum write to read turn around delay tWTR.
- Support configurable Minimum different-CS read to read turn around delay tRTR.

5.2.3 Signal Description

Table 5.2-1 EMC signal description

PAD name	16-bit SDR	DIR	16-bit DDR	DIR	32-bit SDR	DIR	32-bit DDR	DIR
EMRSTN_M								
EMCLKDP_M	CLK	O	CLK	O	CLK	O	CLK	O
EMCLKDM_M			CLK#	O			CLK#	O
EMCKE_M	CKE	O	CKE	O	CKE	O	CKE	O
EMCSN0_M	CS#[0]	O	CS#[0]	O	CS#[0]	O	CS#[0]	O
EMCSN1_M	CS#[1]	O	CS#[1]	O	CS#[1]	O	CS#[1]	O
EMCSN2_M	CS#[2]	O	CS#[2]	O	CS#[2]	O	CS#[2]	O
EMCSN3_M	CS#[3]	O	CS#[3]	O	CS#[3]	O	CS#[3]	O
EMRASN_M	RAS#	O	RAS#	O	RAS#	O	RAS#	O
EMCASN_M	CAS#	O	CAS#	O	CAS#	O	CAS#	O
EMWEN_M	WE#	O	WE#	O	WE#	O	WE#	O
EMDQM0_M	DQM#[0]	O	DQM#[0]	O	DQM#[0]	O	DQM#[0]	O
EMDQM1_M	DQM#[1]	O	DQM#[1]	O	DQM#[1]	O	DQM#[1]	O
EMDQM2_M					DQM#[2]	O	DQM#[2]	O
EMDQM3_M					DQM#[3]	O	DQM#[3]	O
EMDQS0_M			DQS[0]	I/O			DQS[0]	I/O
EMDQS1_M			DQS[1]	I/O			DQS[1]	I/O
EMDQS2_M							DQS[2]	I/O
EMDQS3_M							DQS[3]	I/O
EMBA1_M	BA[1]	O	BA[1]	O	BA[1]	O	BA[1]	O
EMA0_M	A[0]	O	A[0]	O	A[0]	O	A[0]	O
EMA1_M	A[1]	O	A[1]	O	A[1]	O	A[1]	O
EMA2_M	A[2]	O	A[2]	O	A[2]	O	A[2]	O
EMA3_M	A[3]	O	A[3]	O	A[3]	O	A[3]	O
EMA4_M	A[4]	O	A[4]	O	A[4]	O	A[4]	O
EMA5_M	A[5]	O	A[5]	O	A[5]	O	A[5]	O
EMA6_M	A[6]	O	A[6]	O	A[6]	O	A[6]	O
EMA7_M	A[7]	O	A[7]	O	A[7]	O	A[7]	O
EMA8_M	A[8]	O	A[8]	O	A[8]	O	A[8]	O
EMA9_M	A[9]	O	A[9]	O	A[9]	O	A[9]	O

EMA10_M	A[10]	O	A[10]	O	A[10]	O	A[10]	O
EMA11_M	A[11]	O	A[11]	O	A[11]	O	A[11]	O
EMA12_M	A[12]	O	A[12]	O	A[12]	O	A[12]	O
EMA13_M	A[13]	O	A[13]	O	A[13]	O	A[13]	O
EMA14_M / EMBA0_M	BA[0]	O	BA[0]	O	BA[0]	O	BA[0]	O
EMA15_M / EMD16_M					D[16]	I/O	D[16]	I/O
EMA16_M / EMD17_M					D[17]	I/O	D[17]	I/O
EMA17_M / EMD18_M					D[18]	I/O	D[18]	I/O
EMA18_M / EMD19_M					D[19]	I/O	D[19]	I/O
EMA19_M / EMD20_M					D[20]	I/O	D[20]	I/O
EMA20_M / EMD21_M					D[21]	I/O	D[21]	I/O
EMA21_M / EMD22_M					D[22]	I/O	D[22]	I/O
EMA22_M / EMD23_M					D[23]	I/O	D[23]	I/O
EMA23_M / EMD24_M					D[24]	I/O	D[24]	I/O
EMA24_M / EMD25_M					D[25]	I/O	D[25]	I/O
EMA25_M / EMD26_M					D[26]	I/O	D[26]	I/O
EMA26_M / EMD27_M					D[27]	I/O	D[27]	I/O
EMA27_M / EMD28_M					D[28]	I/O	D[28]	I/O
EMA28_M / EMD29_M					D[29]	I/O	D[29]	I/O
/ EMD30_M					D[30]	I/O	D[30]	I/O
/ EMD31_M					D[31]	I/O	D[31]	I/O
EMD0_M	D[0]	I/O	D[0]	I/O	D[0]	I/O	D[0]	I/O
EMD1_M	D[1]	I/O	D[1]	I/O	D[1]	I/O	D[1]	I/O
EMD2_M	D[2]	I/O	D[2]	I/O	D[2]	I/O	D[2]	I/O
EMD3_M	D[3]	I/O	D[3]	I/O	D[3]	I/O	D[3]	I/O
EMD4_M	D[4]	I/O	D[4]	I/O	D[4]	I/O	D[4]	I/O
EMD5_M	D[5]	I/O	D[5]	I/O	D[5]	I/O	D[5]	I/O
EMD6_M	D[6]	I/O	D[6]	I/O	D[6]	I/O	D[6]	I/O
EMD7_M	D[7]	I/O	D[7]	I/O	D[7]	I/O	D[7]	I/O
EMD8_M	D[8]	I/O	D[8]	I/O	D[8]	I/O	D[8]	I/O
EMD9_M	D[9]	I/O	D[9]	I/O	D[9]	I/O	D[9]	I/O
EMD10_M	D[10]	I/O	D[10]	I/O	D[10]	I/O	D[10]	I/O
EMD11_M	D[11]	I/O	D[11]	I/O	D[11]	I/O	D[11]	I/O
EMD12_M	D[12]	I/O	D[12]	I/O	D[12]	I/O	D[12]	I/O
EMD13_M	D[13]	I/O	D[13]	I/O	D[13]	I/O	D[13]	I/O
EMD14_M	D[14]	I/O	D[14]	I/O	D[14]	I/O	D[14]	I/O
EMD15_M	D[15]	I/O	D[15]	I/O	D[15]	I/O	D[15]	I/O

5.2.4 Function Description

5.2.4.1 Block Diagram

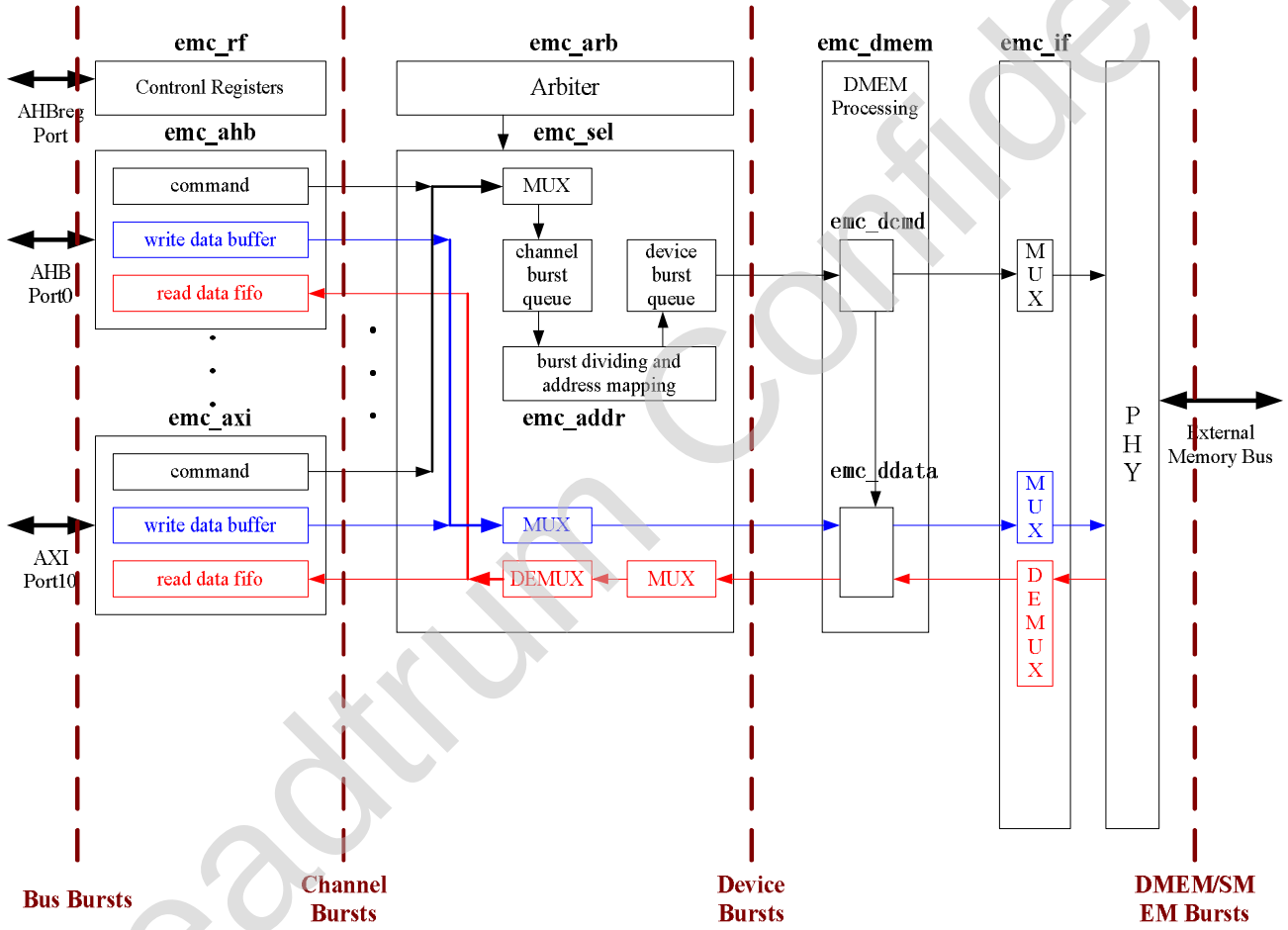


Figure 5.2-1 EMC block diagram

EMC mainly have six parts:

- emc_ahb32 and emc_ahb64 are used to interface with AHB, and emc_axi64 is used to interface with AXI.
- emc_sel, emc_arb and emc_addr are used to multiplex multiple channels and divide channel bursts to device bursts
- emc_dmem and emc_if are used to generate external memory bus sequence.
- emc_phy is used to interface with external memory and handle timing.
- emc_rf is configuration registers.

- emc_pmu is used to gate clock automatically or forcedly.

5.2.4.2 Configuration AHB Interface Descriptions

This port is a very simple asynchronous AHB slave only used for EMC configuring.

- 32-bit AHB slave
- No endian issue
- READ, WRITE
- Only support WORD accessing
- Support All AHB burst types (EMC takes all types as SINGLE transactions)
- No requirement for the frequency of configuration AHB slave clock and clk_emc. Or, support any combination between the two clocks.
- Wait state: 0 wait state.
- Always response OK.

5.2.4.3 Accessing AHB Interface Descriptions

EMC supports multiple accessing AHB channels, 32-bit or 64-bit, big-endian or little-endian, asynchronous or synchronous.

5.2.4.3.1 Block Diagram

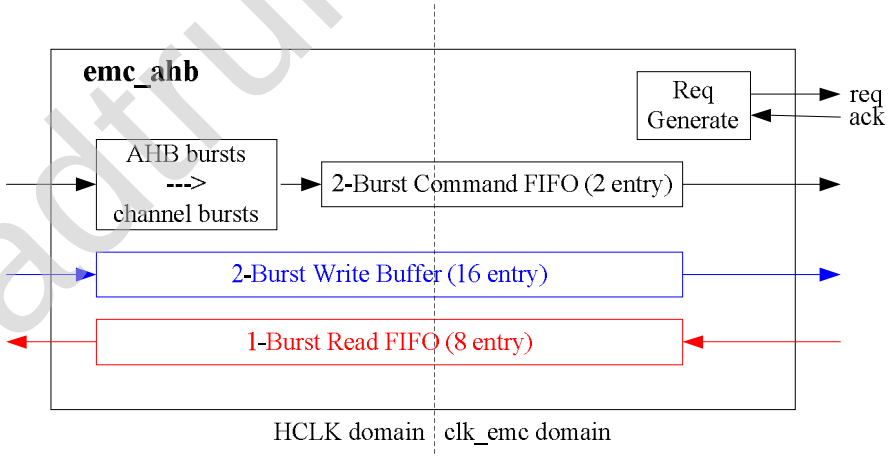


Figure 5.2-2 Accessing AHB interface block diagram

5.2.4.3.2 AHB Compatibility

- 32-bit AHB channel
- 64-bit AHB channel
- AHB big-endian or AHB little-endian
- Asynchronous or synchronous between AHB clock and EMC clock
- READ, WRITE
- BYTE, HALF, WORD for 32-bit AHB channels and DWORD for 64-bit AHB channels
- All burst types: SINGLE, INCR, WRAP4, INCR4, WRAP8, INCR8, WRAP16, INCR16
- For INCR, support HLENGTH from 1 to 15
- Support BUSY-inserted
- Cannot response ERROR to AHB
- Cannot issue SPLIT transactions
- Don't care about HPROT

5.2.4.3.3 AHB Bursts Mapping to Channel Bursts

EMC maps AHB bursts to channel bursts in emc_ahb32 or emc_ahb64 because of too long AHB burst length or undefined burst length.

Burst mapping includes three steps – pre-mapping, burst mapping, post-adjusting.

Pre-mapping divides the too long bursts, and follows these rules:

To WRAP16 Bursts:

- If a burst starts from WRAP16 boundary, the burst is mapped to one INCR burst.
- If a burst doesn't start from WRAP16 boundary, the burst is divided to two INCR burst. The first one is from start to WRAP16 boundary, and the other is from boundary to end.

To INCR16 Bursts:

- A INCR16 burst is divided to two INCR8 bursts, each of which includes 8 data.

To INCR Bursts:

- If HLENGTH is 0, do nothing.
- If HLENGTH is not more than 8, do nothing.
- If HLENGTH is more than 8, the burst is divided to two bursts, the first 8 data constitutes the first burst with HLENGTH of 8, and the left data constitutes the next burst with HLENGTH of original HLENGTH minus 8.

Burst-mapping follows these rules:

- If related rf_hburst_ren_csx for reading or rf_hburst_ren_csx for writing is cleared, this burst is taken as multiple single transactions, and burst length is 1 BYTE for BYTE transaction, or 1 HALF for HALF transaction, or 1 WORD for WORD transaction, or 1 DWORD for DWORD transaction. It's IMPORTANT that this rule is only used by SMEM.
- If HBURST is SINGLE, burst mode is INCR, and burst length is 1 data (BYTE, HALF, WORD or DWORD).
- If HBURST is WRAP4, burst mode is WRAP, and burst length is 4 data (BYTE, HALF, WORD or DWORD).
- If HBURST is INCR4, burst mode is INCR, and burst length is 4 data (BYTE, HALF, WORD or DWORD).
- If HBURST is WRAP8, burst mode is WRAP, and burst length is 8 data (BYTE, HALF, WORD or DWORD).

- If HBURST is INCR8, burst mode is INCR, and burst length is 8 data (BYTE, HALF, WORD or DWORD).
- If HBURST is INCR and HLENGTH is not 0, burst mode is INCR, and burst length is HLENGTH of data (BYTE, HALF, WORD or DWORD).
- If HBURST is INCR and HLENGTH is 0, burst mode is INCR, and burst length is from related rf_hburst_rlength_incr_chx or rf_hburst_wlength_incr_chx.

  rf_hburst_xlength_incr_chx = 0 : burst length is 2 WORD

  rf_hburst_xlength_incr_chx = 1 : burst length is 4 WORD

  rf_hburst_xlength_incr_chx = 2 : burst length is 6 WORD

  rf_hburst_xlength_incr_chx = 3 : burst length is 8 WORD

  rf_hburst_xlength_incr_chx = 4 : burst length is 10 WORD (only for 64-bit AHB interface)

  rf_hburst_xlength_incr_chx = 5 : burst length is 12 WORD (only for 64-bit AHB interface)

  rf_hburst_xlength_incr_chx = 6 : burst length is 14 WORD (only for 64-bit AHB interface)

  rf_hburst_xlength_incr_chx = 7 : burst length is 16 WORD (only for 64-bit AHB interface)

Post-adjusting deals with burst length from above in order to unify the unit

- For 32-bit AHB interface, burst length is unified to WORD.
- For 64-bit AHB interface, burst length is unified to DWORD.

In AHB interface logic, both WRAP bursts and INCR bursts are taken with the same optimization method.

5.2.4.3.4 Read Operation Description

An 8-entry (8-WORD for 32-bit AHB and 8-DWORD for 64-bit AHB) read FIFO is used in each AHB channel to improve accessing performance. All reading operations, single access or burst access, cannot bypass this FIFO.

The read FIFO always contains only one channel burst at the same time.

For read operations, only one channel burst is on process in emc_ahb at the same time, and there is only one pipeline stage, unlike write operations. All read operations are executed one by one.

5.2.4.3.5 Write Operation Description

There is only one data path for write, and all write transactions should pass write buffer. One AHB bursts should be written into write buffer firstly, and then EMC transfers data to external memory from write buffer.

Write buffer is a 16-entry (16-WORD for 32-bit AHB and 16-DWORD for 64-bit AHB) double buffer.

There are two pipeline stages for write operations. One is AHB writes data to write buffer, and the other is write buffer transfers data to external memory. So there are at most two channel bursts on process in one emc_ahb.

Because software completes one transfer only after data is written into write buffer, there is a delay time between software transfer completing and external memory transfer completing. The maximum delay time is the time that EMC writes two channel bursts to external memory.

5.2.4.3.6 Data Endian Switching

There two types of endian issues in EMC, one is AHB protocol endian, and the other is data endian.

For AHB protocol endian, EMC can handle it automatically by hardware.

For data endian, because EMC cannot understand different requirements from software, it provides different converting options for software.

For each AHB channel, EMC provides one rf_endian_swt_chx to select the converting options.

For 32-bit AHB:

rf_endian_swt_chx = 0 : BYTE switching

0 -> 3
1 -> 2
2 -> 1
3 -> 0

rf_endian_swt_chx = 1 : HALF switching

0 -> 2
2 -> 0

rf_endian_swt_chx = 2 : Not supported

rf_endian_swt_chx = 3 : no-switching

For 32-bit AHB:

rf_endian_swt_chx = 0 : BYTE switching

0 -> 7
1 -> 6
2 -> 5
3 -> 4
4 -> 3
5 -> 2
6 -> 1
7-> 0

rf_endian_swt_chx = 1 : HALF switching

0 -> 6
2 -> 4
4 -> 2
6 -> 0

rf_endian_swt_chx = 2 : WORD switching

0 -> 4
4 -> 0

rf_endian_swt_chx = 3 : no-switching

5.2.4.3.7 Channel Sleep Control

EMC provides a method to hold each channel for system sleep control.

If rf_auto_sleep_en_chx is set, this method is enabled. System can use some hardware signals to hold EMC AHB channels and make these channel sleep.

5.2.4.4 Channel Multiplex Descriptions

This logic mainly has four functions: channel bursts arbitrating and multiplexing, multiplexed command queue, channel bursts being divided to device bursts, and device bursts address mapping.

5.2.4.4.1 Block Diagram

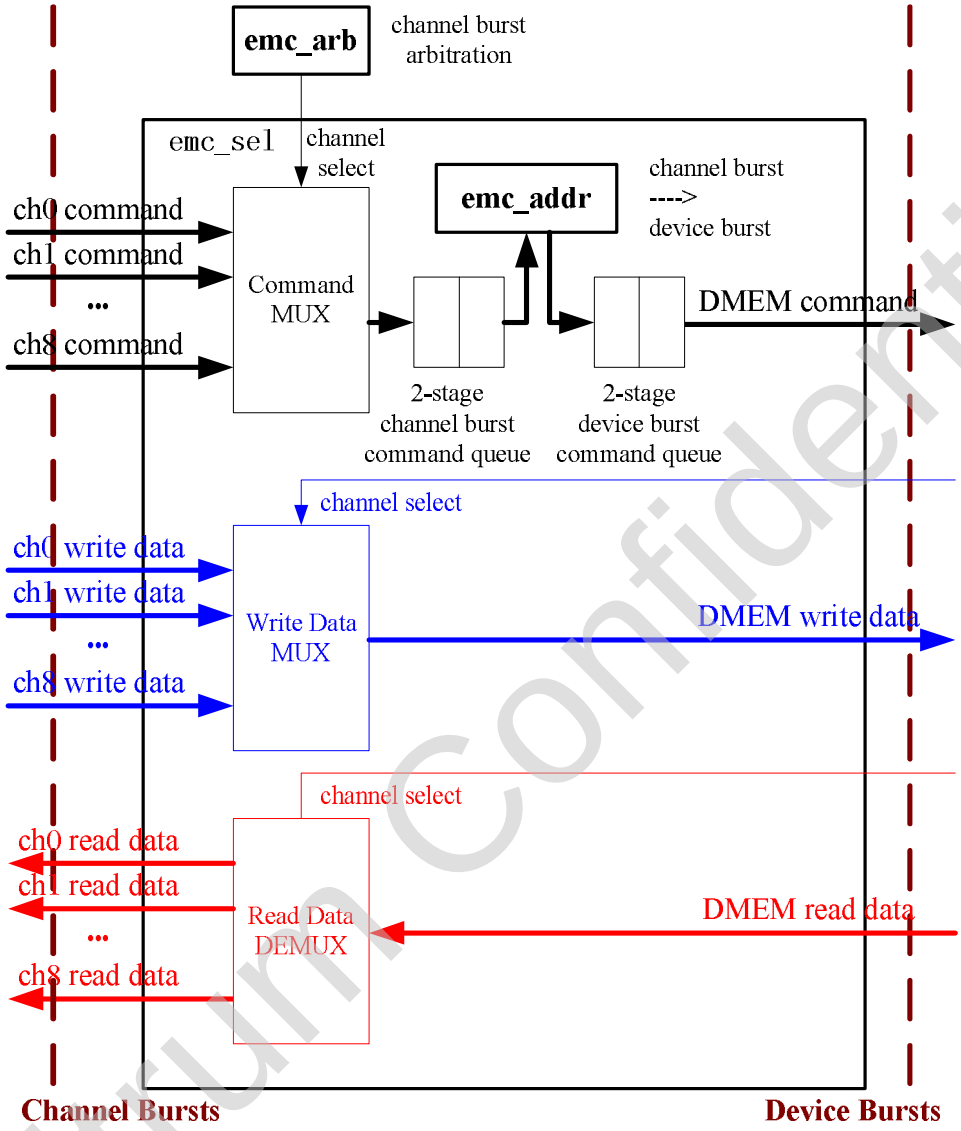


Figure 5.2-3 Channel multiplex block diagram

5.2.4.4.2 Channel Burst Arbitration and Multiplex

- Arbitration is done based on channel bursts.
- The arbitrator receives channel burst requests from each channel logic, and response acknowledges to them if accepting related requests.
- The request signals MUST be held until related acknowledge is received. And also, the command information MUST be issued together with requests.
- Arbiter strategy: 4-level priority robin-round.
  - 4-level configurable priority.
  - For the same priority, robin-round algorithm is used.
  - For the same priority, read bursts and write bursts are taken with the same priority.

- This part of logic completes another function, which is to multiplex channel command and write data and to de-multiplex read data to each channel.

5.2.4.4.3 Channel Burst Command Queue

- After arbitration and multiplexing, multiplexed commands are stored into a stage-configurable channel burst command queue. Output from channel burst command queue, channel bursts are divided into device bursts (this part is described in next chapter) and AHB address is mapped to external memory address (this part is described in following chapter). Then device bursts are written into 2-stage device burst command queue. At last, both commands (current command and next command) in device burst command queue is transmitted to DMEM controller, and current command is transmitted to SMEM controller.
- Channel burst command queue is stage-configurable (controlled by rf_cmd_queue_mode), and the configuration is:
  - 0-stage (rf_cmd_queue_mode is 0): if the 2nd command in device burst command queue is empty, arbitration is issued, and new channel burst command is written to the 1st command.
  - 1-stage (rf_cmd_queue_mode is 1): if the 1st command in channel burst command queue is empty, arbitration is issued, and new channel burst command is written to the 1st command.
  - 2-stage (rf_cmd_queue_mode is 2): if the 2nd command in channel burst command queue is empty, arbitration is issued, and new channel burst command is written to the 1st command (if 1st is empry) or the 2nd command (if 1st is not empty).
- Channel burst sequence in channel burst command queue is fixed and cannot be changed.
- Channel burst command structure:

Table 5.2-2 Channel burst command structure

Bit	Item	Note
[50]	Command valid 0: empty in this entry 1: one valid command in this entry	
[49:46]	Channel number 0: this command is for channel 0 1: this command is for channel 1 … 15: this command is for channel 15	
[45:44]	Reserved	
[43]	External memory chip select 0: CS0 1: CS1	
[42]	Channel burst operating mode 0: read 1: write	
[41:40]	Data width 0: 8-bit (only for SMEM single mode)	

	1: 16-bit (only for SMEM single mode) 2: 32-bit 3: 64-bit (only for SMEM single mode)	
[39]	Channel burst enable 0: single access 1: burst access	
[38]	Channel burst mode 0: wrap mode 1: increase mode	
[37:35]	Channel wrap mode length 0: wrap of 1 WORD 1: wrap of 2 WORD 2: wrap of 4 WORD 3: wrap of 8 WORD 4: wrap of 16 WORD 5: reserved 6: reserved 7: reserved	
[34:30]	Channel burst length The unit is WORD The supported range is from 1 to 16 WORD	
[29:0]	Channel burst first address The unit is BYTE	

5.2.4.4.4 Device Burst Command Queue

- Device burst command queue is 2-stage, which is fixed. The two stage commands are:
  - Current command: current executing command
  - Next command: next executing command
- Same with channel burst command queue, device burst sequence in device burst command queue is fixed and cannot be changed.
- Device burst command structure:

Table 5.2-3 Device burst command structure

Bit	Item	Note
[46]	Command valid 0: empty in this entry 1: one valid command in this entry	
[45]	The last device burst flag in one channel burst 0: not last device bursts 1: last device burst	

[44:41]	Channel number 0: this command is for channel 0 1: this command is for channel 1 … 15: this command is for channel 15	
[40:39]	Reserved	
[38]	External memory chip select 0: CS0 1: CS1	
[37]	Device burst operating mode 0: read 1: write	
[36:35]	Data width 0: 8-bit (only for SMEM single mode) 1: 16-bit (only for SMEM single mode) 2: 32-bit 3: 64-bit (only for SMEM single mode)	
[34]	Device burst enable 0: single access 1: burst access	
[33:30]	Device burst length The unit is WORD The supported range is from 1 to 16 WORD	

For DMEM:

[29:28]	reserved	
[27:26]	DMEM device burst bank address	
[25:12]	DMEM device burst row address	
[11:0]	DMEM device burst column address	

5.2.4.4.5 AHB Channel Bursts Dividing to Device Bursts

AHB channel bursts from AHB interface logic are mapped to external device bursts in this part. Device burst information comes from configuration registers

One channel burst is divided into several device bursts according to:

- Device burst length is met
- If channel burst is WRAP mode, and WRAP boundary is hit
- If external memory is in WRAP mode, and WRAP boundary is hit
- Channel burst end is met

Notes,

- Device burst information from configuration registers MUST be matched with external memory configuration information.

- In order to simplify hardware design, all device bursts are INCR mode even if channel bursts are WRAP mode or external memory is in WRAP mode. an WRAP channel burst is divided on WRAP boundary.

5.2.4.4.6 AHB Address Mapping

EMC should map AHB address to external memory address. AHB address is used by AHB transactions and this address is the same as software accessing address. BYTE is the unit of AHB address. External memory address is used by external memory accessing, and the unit is external memory data width.

Another work of EMC is to map AHB address (or software address) to which device, because EMC supports multiple external devices.

EMC provides **rf_cs_position** and **rf_cs_mode** to finish this mapping:

Table 5.2-4 AHB address mapping

	rf_cs_position=2'h0	**rf_cs_position**=2'h1	**rf_cs_position**=2'h2	**rf_cs_position**=2'h3
Note	The 8 domains of HADDR[29:27] is from 0 to 7 are equivalent and duplicated	The 4 domains of HADDR[29:28] is from 0 to 3 are equivalent and duplicated	The 2 domains of HADDR[29] is from 0 to 1 are equivalent and duplicated	
rf_cs_mode =3'b000	CS0: HADDR[26:25]=0 CS1: HADDR[26:25]=1 CS2: HADDR[26:25]=2 CS3: HADDR[26:25]=3	CS0: HADDR[27:26]=0 CS1: HADDR[27:26]=1 CS2: HADDR[27:26]=2 CS3: HADDR[27:26]=3	CS0: HADDR[28:27]=0 CS1: HADDR[28:27]=1 CS2: HADDR[28:27]=2 CS3: HADDR[28:27]=3	CS0: HADDR[29:28]=0 CS1: HADDR[29:28]=1 CS2: HADDR[29:28]=2 CS3: HADDR[29:28]=3
rf_cs_mode =3'b001	CS0: HADDR[26]=0 CS1: NA CS2: HADDR[26:25]=2 CS3: HADDR[26:25]=3	CS0: HADDR[27]=0 CS1: NA CS2: HADDR[27:26]=2 CS3: HADDR[27:26]=3	CS0: HADDR[28]=0 CS1: NA CS2: HADDR[28:27]=2 CS3: HADDR[28:27]=3	CS0: HADDR[29]=0 CS1: NA CS2: HADDR[29:28]=2 CS3: HADDR[29:28]=3
rf_cs_mode =3'b010	CS0: HADDR[26:25]=0 CS1: HADDR[26:25]=1 CS2: HADDR[26]=1 CS3: NA	CS0: HADDR[27:26]=0 CS1: HADDR[27:26]=1 CS2: HADDR[27]=1 CS3: NA	CS0: HADDR[28:27]=0 CS1: HADDR[28:27]=1 CS2: HADDR[28]=1 CS3: NA	CS0: HADDR[29:28]=0 CS1: HADDR[29:28]=1 CS2: HADDR[29]=1 CS3: NA
rf_cs_mode =3'b011	CS0: HADDR[26]=0 CS1: NA CS2: HADDR[26]=1 CS3: NA	CS0: HADDR[27]=0 CS1: NA CS2: HADDR[27]=1 CS3: NA	CS0: HADDR[28]=0 CS1: NA CS2: HADDR[28]=1 CS3: NA	CS0: HADDR[29]=0 CS1: NA CS2: HADDR[29]=1 CS3: NA
rf_cs_mode =3'b1xx	CS0: Always Selected CS1: NA CS2: NA CS3: NA	CS0: Always Selected CS1: NA CS2: NA CS3: NA	CS0: Always Selected CS1: NA CS2: NA CS3: NA	CS0: Always Selected CS1: NA CS2: NA CS3: NA

5.2.4.4.7 DMEM Address Mapping

In this part, EMC generates DMEM address according to **drf_data_width** and **drf_column_mode**.

Table 5.2-5 DMEM address mapping

drf_data_width	drf_column_mode	row mapping	bank mapping	column mapping
16-bit	8-bit	HADDR[24:11]	HADDR[10:9]	{HADDR[8:2],1'b0}
	9-bit	HADDR[25:12]	HADDR[11:10]	{HADDR[9:2],1'b0}
	10-bit	HADDR[26:13]	HADDR[12:11]	{HADDR[10:2],1'b0}
	11-bit	HADDR[27:14]	HADDR[13:12]	{HADDR[11:2],1'b0}
	12-bit	HADDR[28:15]	HADDR[14:13]	{HADDR[12:2],1'b0}
32-bit	8-bit	HADDR[25:12]	HADDR[11:10]	HADDR[9:2]
	9-bit	HADDR[26:13]	HADDR[12:11]	HADDR[10:2]
	10-bit	HADDR[27:14]	HADDR[13:12]	HADDR[11:2]
	11-bit	HADDR[28:15]	HADDR[14:13]	HADDR[12:2]
	12-bit	HADDR[29:16]	HADDR[15:14]	HADDR[13:2]

5.2.4.5 DMEM Operation Descriptions

DMEM controller is made of three paths, command path, write data path and read data path. The architecture is described in the following diagram.

One write burst is executed in two pipelined stage, command stage on command path and data stage on write data path.

One read burst is executed also in two pipelined stage, command stage on command path and data stage on read data path.

The command path mainly have three functions, planning and issuing commands, organizing DMEM bursts from difference device bursts, handling DMEM timing constraints.

The write data path mainly have three functions, getting and generating write data and controlling its delay time, getting and generating write DM and controlling its delay time, generating write DQS and controlling its delay time.

The read data path mainly have three functions, sampling and handling read data, generating read DM and control its delay time, controlling input DQS signals.

When a device burst is issued, the command path translates it to DMEM bursts in command stage and issues related DMEM commands, then the command path transmits this DMEM bursts to the data path through delay-configurable shift registers, and also the command path begins to handle next device burst.

When the data path receives a DMEM burst, it handles data, DM and DQS parts, and completes this read or write burst.

This chapter describes the DMEM device features, main command control, other command control, write data path and read data path.

DMEM timing control, sampling control and PHY control are described in following chapters.

5.2.4.5.1 Block Diagram

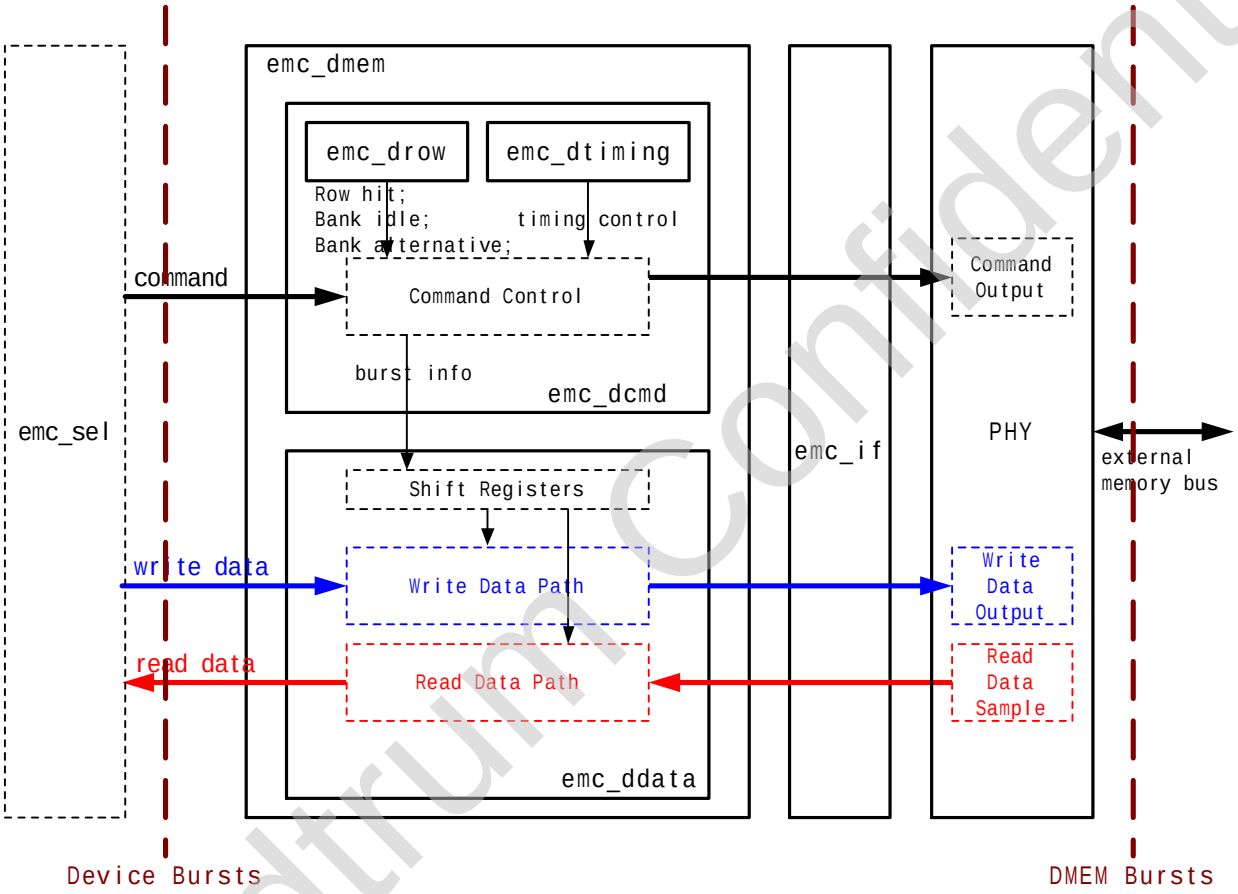


Figure 5.2-4 DMEM controller block diagram

Refer to EMC PHY Specifications for detailed circuits in EMC PHY.

5.2.4.5.2 Device Features and Device Control

- Support up to 1G byte space.
- Support SDR-SDRAM and DDR-SDRAM.
- Support from 16Mbits to 8Gbits SDRAM. (Still no data sheet for single-die 1G/2G/4G/8G bit SDRAM).
- Support up to 2 CS. And all SDRAM must have the same type.

- Support 4-bank.
- Support 11/12/13/14-bit row width.
- Support 8/9/10/11/12-bit column width.
- Support 16/32-bit data width.
- For 16-bit SDR, support 2/4/8/16/32-burst

  For 32-bit SDR, support 1/2/4/8/16-burst

  For 16-bit DDR, support 2/4/8/16/32-burst

  For 32-bit DDR, support 2/4/8/16-burst
- Support 1/1.5/2/2.5/3/3.5 CAS latency.
- Support 0/0.5/1/1.5 WRITE latency.
- Support real wrap mode burst. That is, one wrap burst is implemented by one SDRAM burst stead of divided into two SDRAM bursts.
- Only support sequential type, not support interleave type.
- Support configurable auto-precharge bit location.
- Support configurable mode register and extended mode registers.
- SDRAM output clock features:
  - Clock frequency is fixed to the half of clk_emc frequency.
  - Support two phase-inverted options for delay coarse adjustment.
  - Support delay fine adjustment by a dedicated delay line.

EMC provides the following registers to configure external memory type.

- **drf_data_width:**

  0: 16-bit

  1: 32-bit
- **drf_column_mode:**

  0: 8-bit

  1: 9-bit

  2: 10-bit

  3: 11-bit

  4: 12-bit

  5: reserved

  6: reserved

  7: reserved
- **drf_row_mode:**

  0: 11-bit

  1: 12-bit

  2: 13-bit

  3: 14-bit
- **drf_auto_pre_position:**

  0: A[10]

  1: A[11]

  2: A[12]

  3: A[13]

5.2.4.5.3 Device Command Descriptions

- **Device Command Truth Table:**

Table 5.2-6 Device command truth table

Command	CS#	CKE	RAS#	CAS#	WE#	BA	ADDR
NOP	H	X	X	X	X	X	X
NOP	L	H	H	H	H	X	X
ACTIVE	L	H	L	H	H	bank	row
READ	L	H	H	L	H	bank	column
WRITE	L	H	H	L	L	bank	column
BURST TERMINATE	L	H	H	H	L	X	X
PRECHARGE (one bank)	L	H	L	H	L	bank	A10 low
PRECHARGE (all bank)	L	H	L	H	L	X	A10 high
AUTO REFRESH	L	H	L	L	H	X	X
SELF REFRESH	L	L	L	L	H	X	X
LOAD MODE REGISTER	L	H	L	L	L	Op-Code	

l LOAD MODE REGISTER

The mode register is loaded via EMA, and EMBA is used to select mode register or extended mode register. The detailed description of mode register can be achieved from device specifications. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

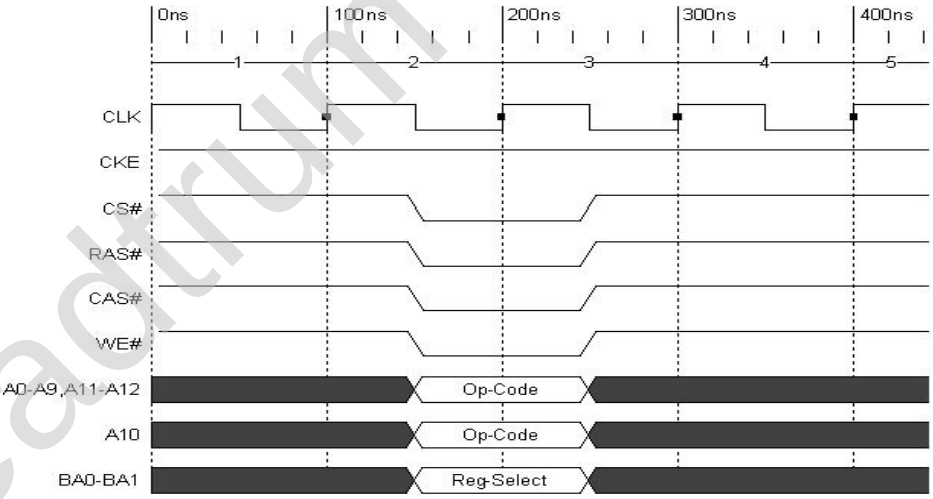


Figure 5.2-5 Load mode register command

l ACTIVE

The ACTIVE command is used to open a row in a particular bank for a subsequent access. The value on the EMBA select the bank, and the EMA select the row. This row remains active for accesses until a PRECHARGE command is issued to this bank. A PRECHARGE command must be issued before opening a different row in the same bank.

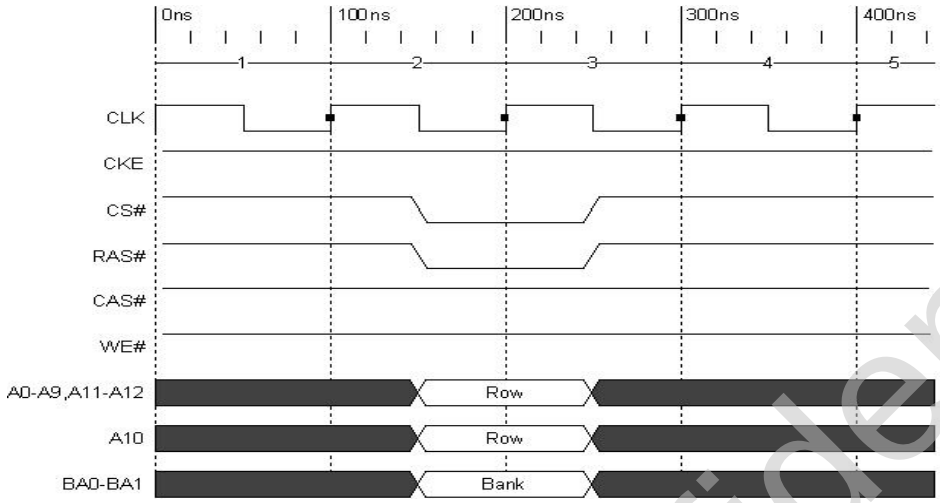


Figure 5.2-6 Active command

l PRECHARGE (one bank)

The PRECARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The banks will be available for a subsequent row operations a specified time tRP after the PRECHARGE command is issued. EMA[10] indicates whether on or all banks are to be pre-charged. If EMA[10] is 0, EMBA indicates which bank to be pre-charged, otherwise, all banks are pre-charged and EMBA is DON'T CARE. Once a bank has been pre-charge, it's in the idle state and must be activated before next accessing issued to this bank.

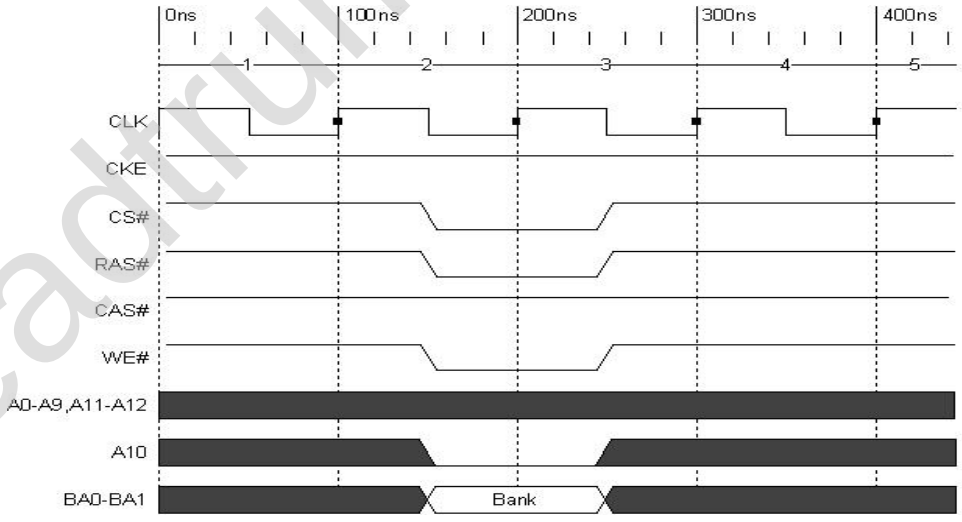


Figure 5.2-7 Precharge (one bank) command

l PRECHARGE (all bank)

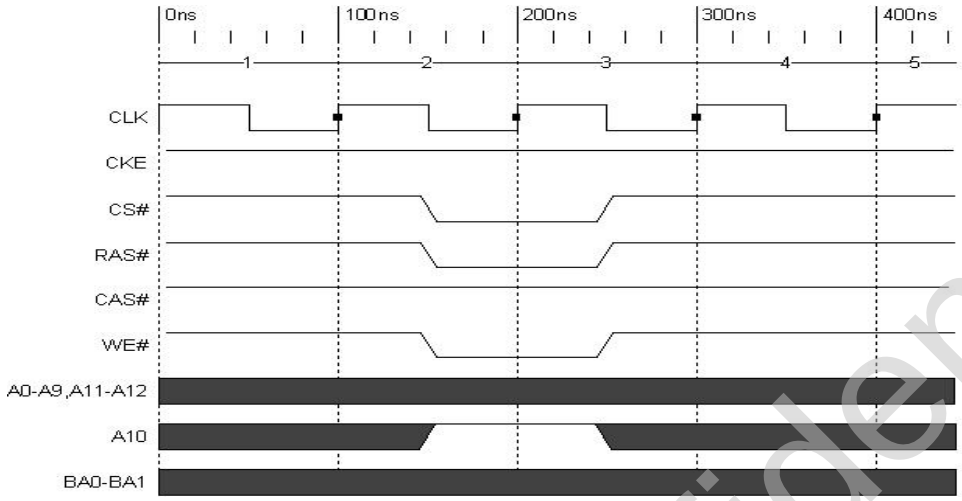


Figure 5.2-8 Precharge (all bank) command

l AUTO REFRESH

AUTO REFRESH is used to retain data in DRAM. This command is non-persistent, so it must be issued each time a refresh is required. All active banks should be pre-charged before an AUTO REFRESH is issued. During AUTO REFRESH, EMA and EMBA is DON'T CARE, and the refresh address is generated by the internal logic. One AUTO REFRESH command starts only one row refresh, and all rows must be refresh one time every specified time (in normal cases, it's 64ms). The total row number can be achieved from device specification, so the maximum interval between two refresh commands can be calculated. To complete one refresh, tRFC should be guaranteed.

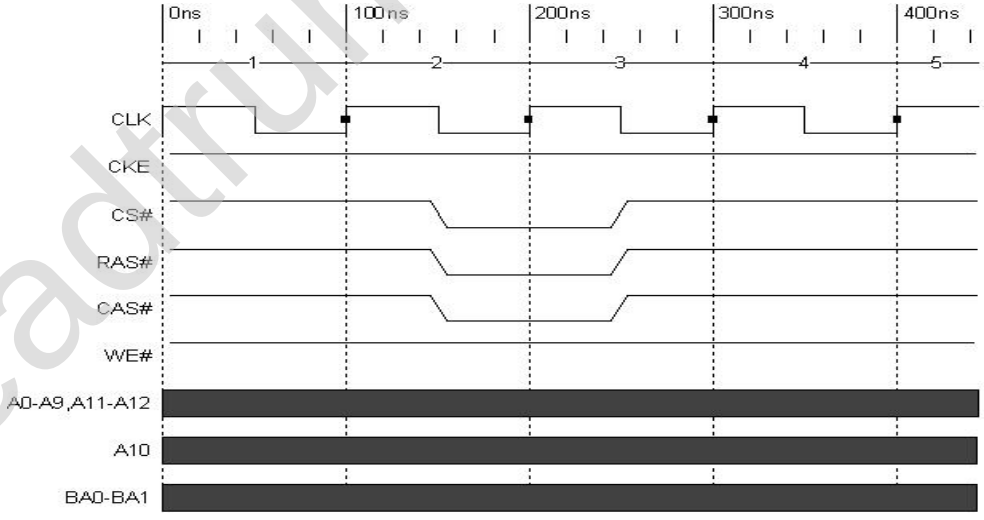


Figure 5.2-9 Auto refresh command

l Enter SELF REFRESH

SELF REFRESH command can be used to retain data in DRAM even if the clock is shut down. SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is low. Once the SELF REFRESH command is issued, all inputs to DRAM are DON'T CARE except CKE, which must remain low. And DRAM generates an internal clock to refresh all rows.

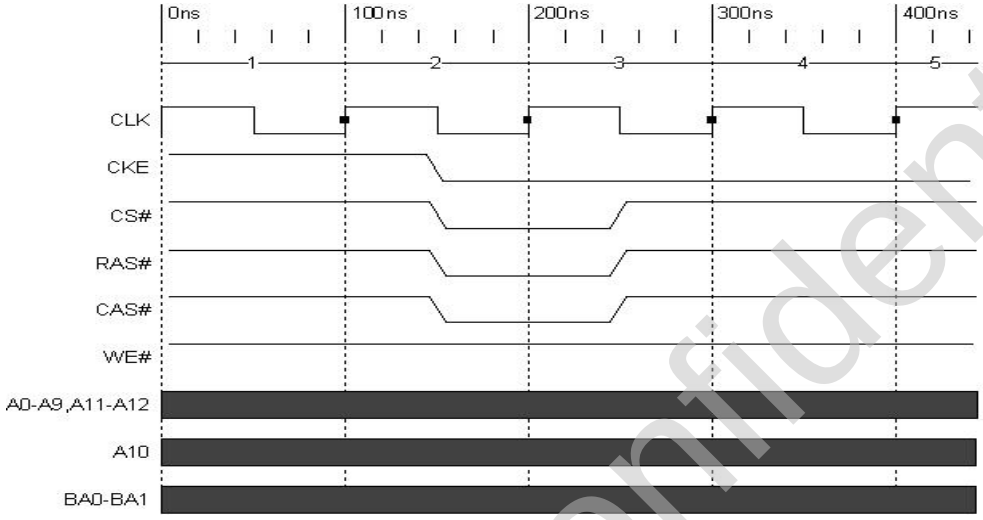


Figure 5.2-10 Enter self refresh command

l Exit SELF REFRESH

To exit SELF REFRESH needs CKE comes back to high and NOP is issued with clock stable. After exiting SELF REFRESH, tXSR must be guaranteed for the completion of any internal refresh in progress.

Upon exiting the SELF REFRESH, AUTO REFRESH commands must be restarted issued.

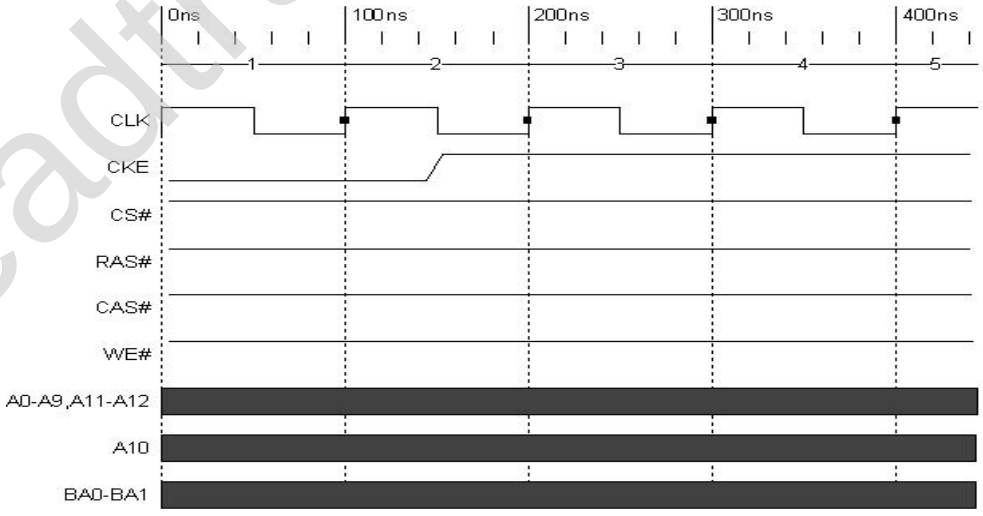


Figure 5.2-11 Exit self refresh command

l READ

The READ command is used to initiate a burst read access to an active row. EMBA selects the bank, and EMA selects the start column address. EMA[10] determines whether or not auto-precharge is used. In current EMC, DRAM controller always issues READ without auto-precharge, and the row remain open for subsequent accesses.

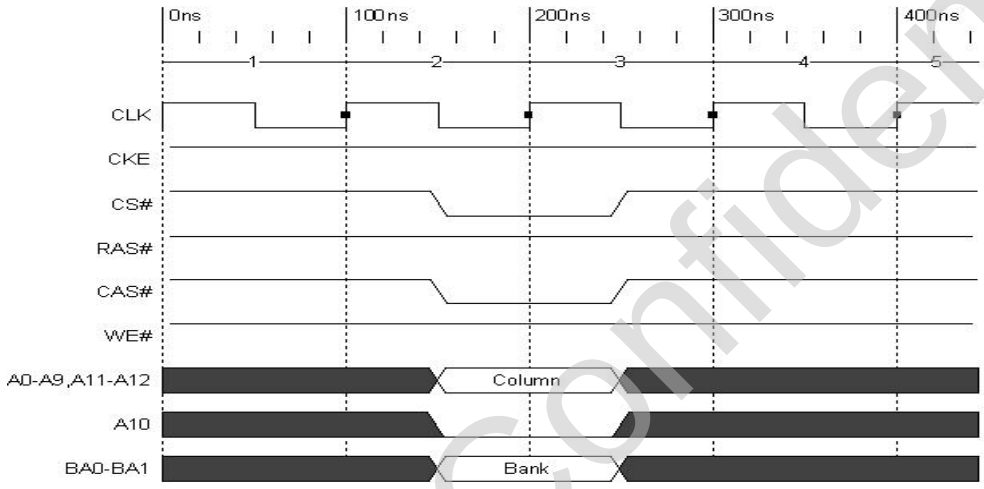


Figure 5.2-12 Read command

l WRITE

The WRITE command is used to initiate a burst write access to an active row. EMBA selects the bank, and EMA selects the start column address. EMA[10] determines whether or not auto-precharge is used. In current EMC, DRAM controller always issues WRITE without auto-precharge, and the row remain open for subsequent accesses.

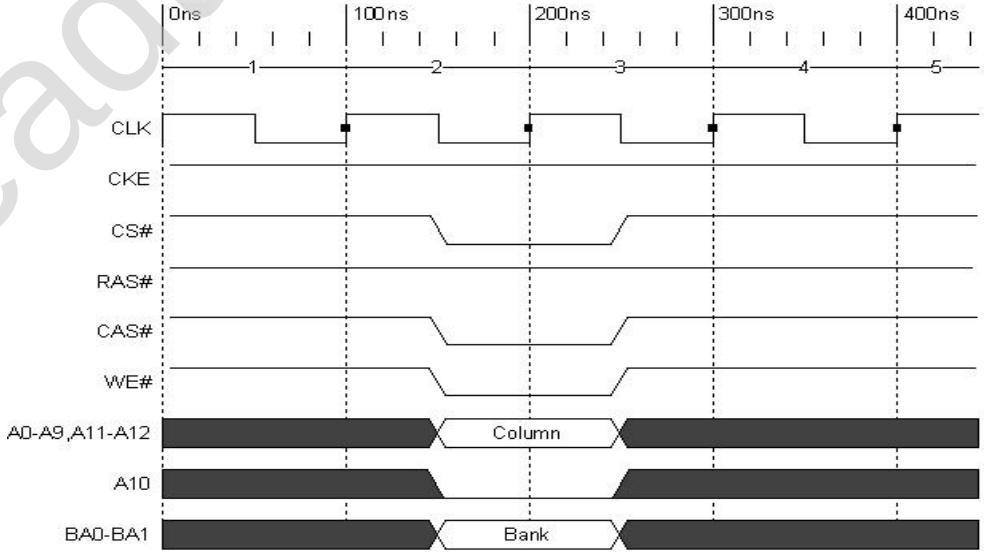


Figure 5.2-13 Write command

l SDR-SDRAM Burst Read and Write

Single Read (CAS Latency = 2)

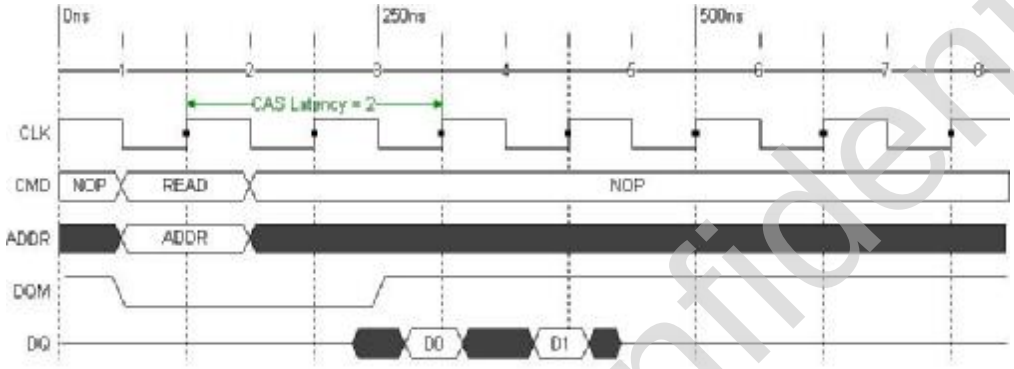


Figure 5.2-14 SDR-SDRAM read (CAS latency = 2)

Single Read (CAS Latency = 3)

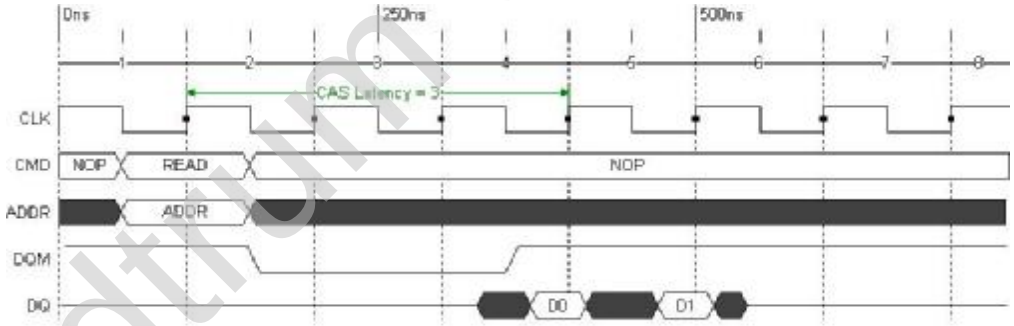


Figure 5.2-15 SDR-SDRAM read (CAS latency = 3)

Single Write

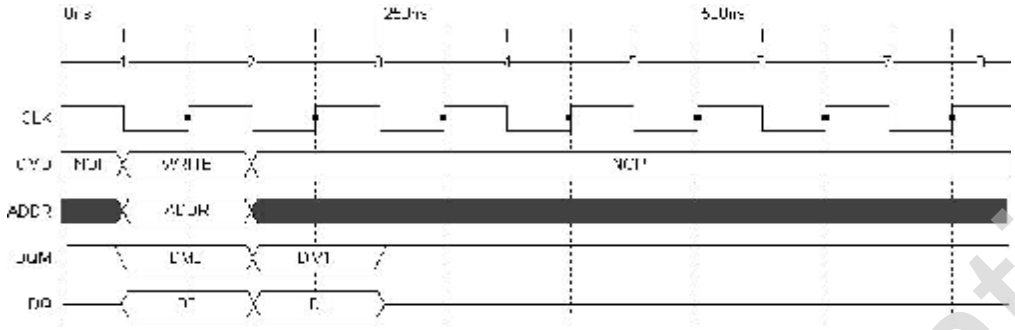


Figure 5.2-16 SDR-SDRAM write

Read to Read

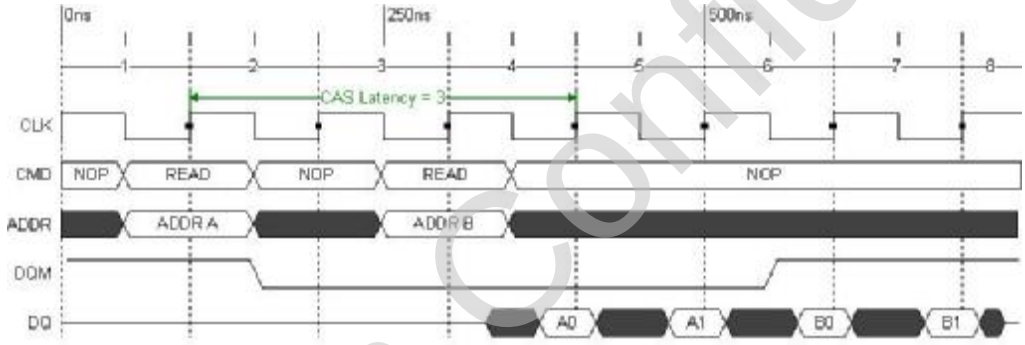


Figure 5.2-17 SDR-SDRAM read to read

Read to Write

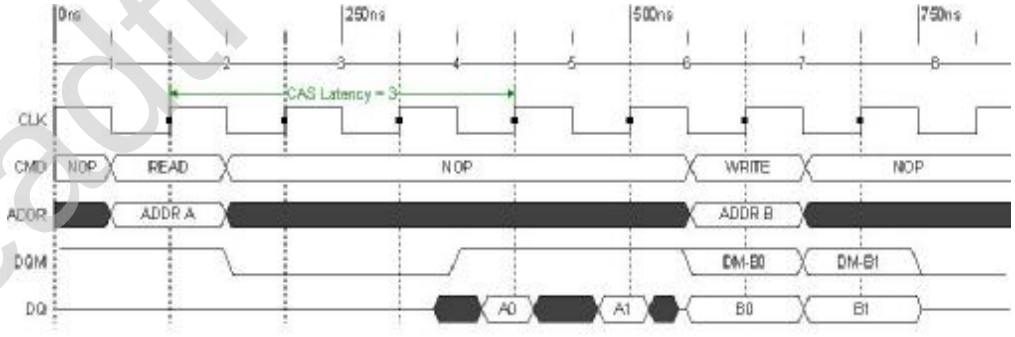


Figure 5.2-18 SDR-SDRAM read to write

Write to Write

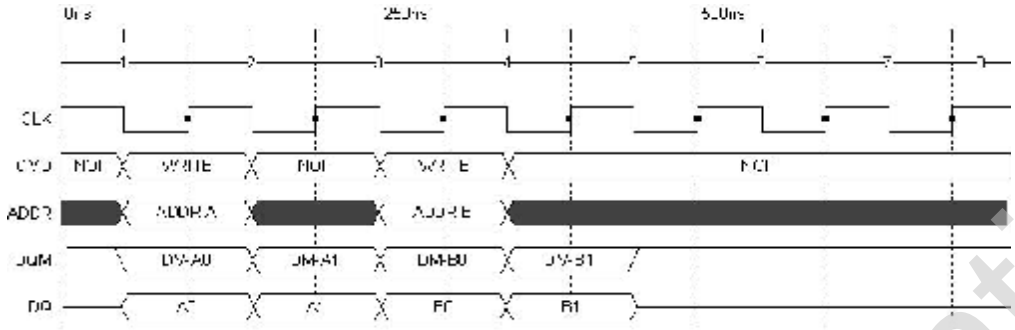


Figure 5.2-19 SDR-SDRAM write to write

Write to Read

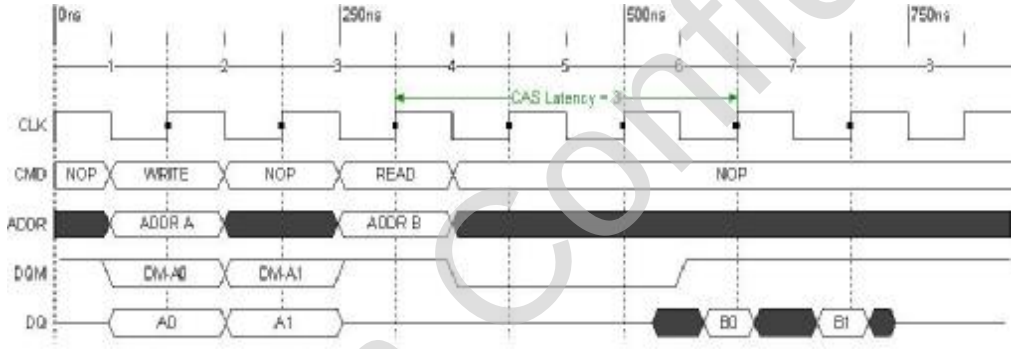


Figure 5.2-20 SDR-SDRAM write to read

I DDR-SDRAM Burst Read and Write

Single Read (CAS Latency = 2)

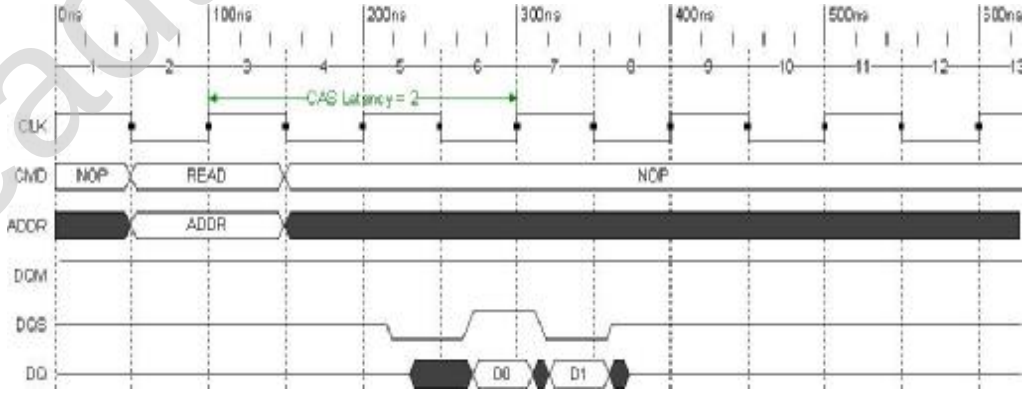


Figure 5.2-21 DDR-SDRAM read (CAS latency = 2)

Single Read (CAS Latency = 3)

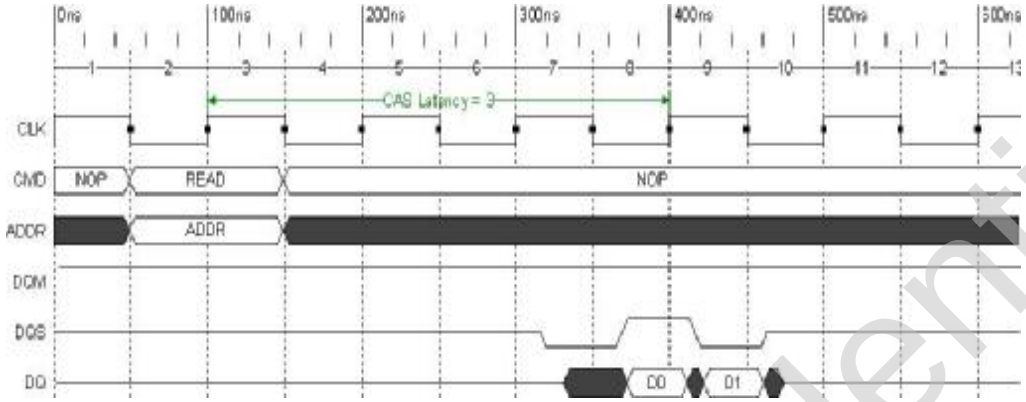


Figure 5.2-22 DDR-SDRAM read (CAS latency = 3)

Single Write

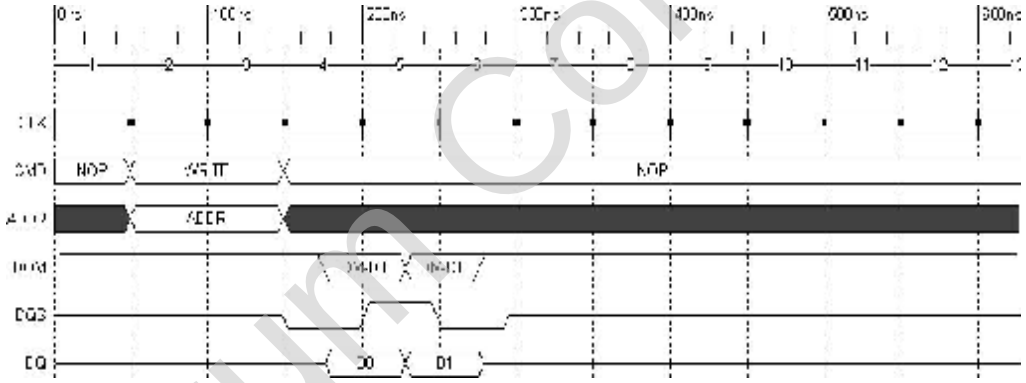


Figure 5.2-23 DDR-SDRAM write

Read to Read

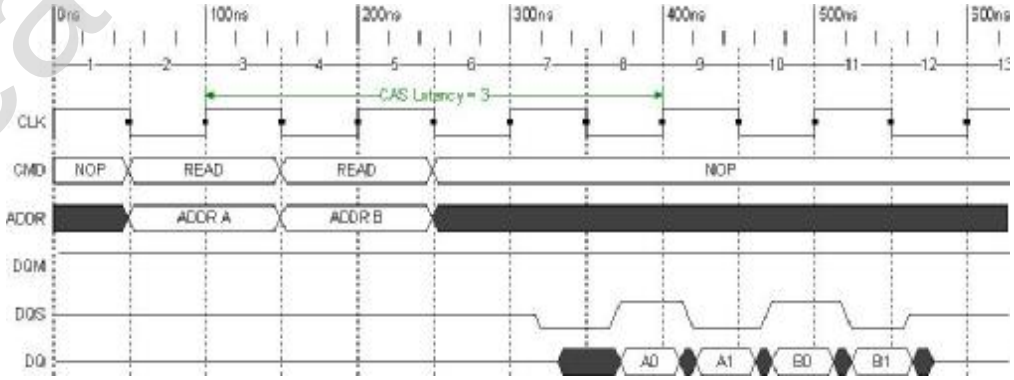


Figure 5.2-24 DDR-SDRAM read to read

Read to Write

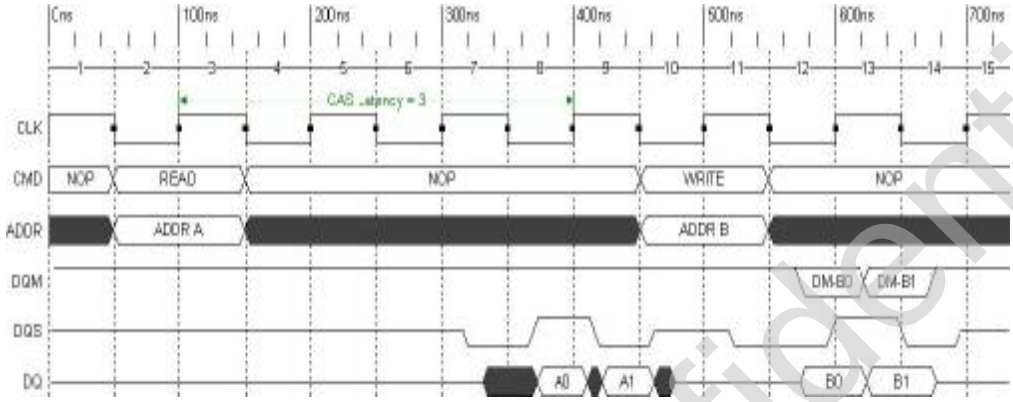


Figure 5.2-25 DDR-SDRAM read to write

Write to Write

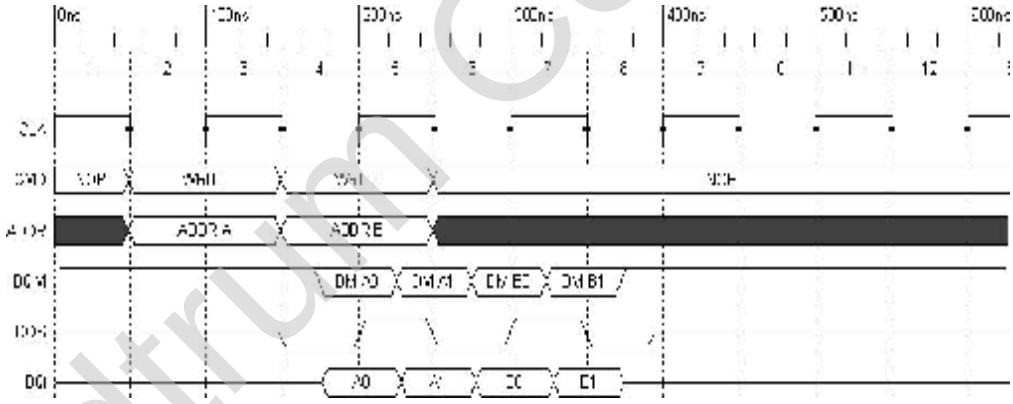


Figure 5.2-26 DDR-SDRAM write to write

Write to Read

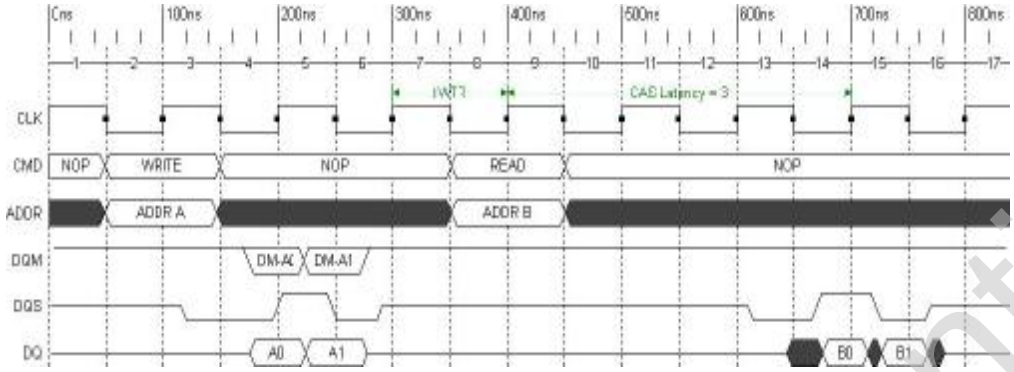


Figure 5.2-27 DDR-SDRAM write to read

5.2.4.5.4 EMC Main Command Control

DMEM controller is a two-burst SDR and DDR controller. The main control method is described as follows.

Introduction:

In order to improve performance, it's better for DMEM controller to see multiple bursts at the same time, because DMEM controller can plan and issue commands in different banks as parallel as possible.

This DMEM controller is designed to handle two bursts at the same time. It is not the best solution, but it's easier to implement.

The next issue is how to plan the two bursts. There are many methods for this issue, our method is to issue commands (PRECHARGE/ACTIVE/READ/WRITE) of two bursts in turn. The following specifies this method.

Firstly, we define one burst as current burst and the other as next burst.

State machine:

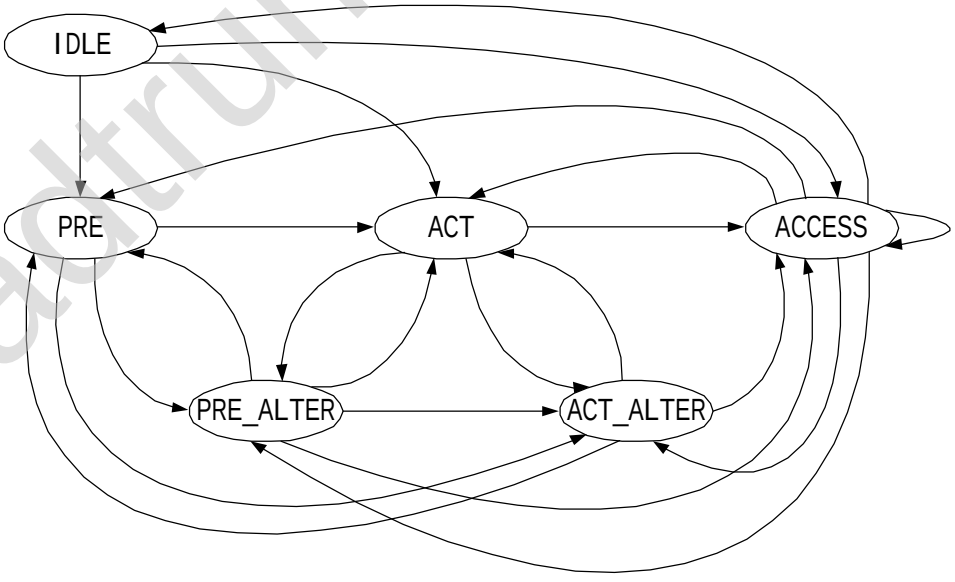
- IDLE: idle state
- PRE: precharge current burst bank
- ACT: active current burst row
- PRE_ALTER: precharge next burst bank
- ACT_ALTER: active next burst row
- ACCESS: access (read or write) current burst

State and command transfer description:

- In IDLE: after current burst is issued, if current row is active, access current burst and enters ACCESS; or if current bank is idle, active current row and enters ACT; or precharge current bank and enters PRE.
- In PRE: If next burst issued and bank is difference and next bank is idle, active next row and enters ACT_ALTER; or if next burst issued and bank is difference and next row is not active, precharge next bank and enters PRE_ALTER; or active current row and enters ACT.

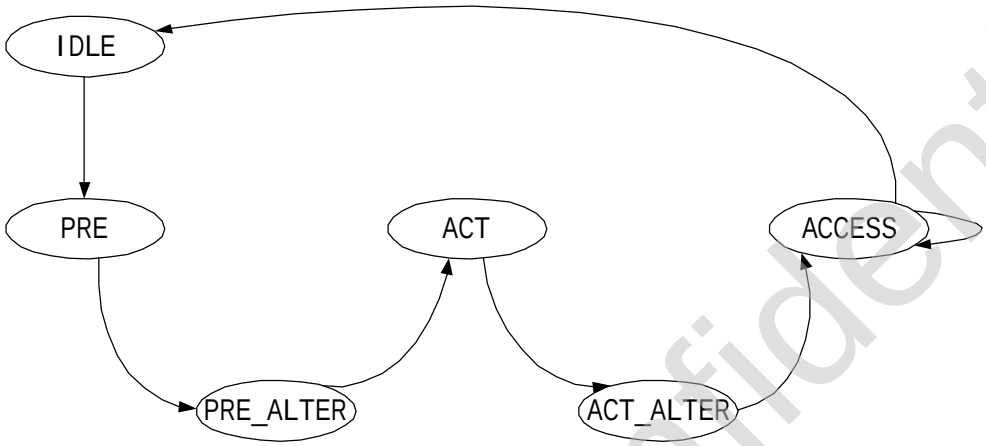
- In ACT: If next burst issued and bank is difference and next bank is idle, active next row and enters ACT_ALTER; or if next burst issued and bank is difference and next row is not active, precharge next bank and enters PRE_ALTER; or access current burst and enters ACCESS.
- In ACCESS: If not burst done and next burst issued and bank is difference and next bank is idle, active next row and enters ACT_ALTER; or if not burst done and next burst issued and bank is difference and next row is not active, precharge next bank and enters PRE_ALTER; or if burst done and next burst is not issued, enters IDLE; or if burst done and next burst is issued and next row is active, accesses next burst and enters ACCESS; or if burst done and next burst is issued and next bank is idle, active next row and enters ACT; or if burst done and next burst is issued and next row is not active, precharge next bank and enters PRE.
- In PRE_ALTER: If current burst is being executing and burst done and next bank is idle, active next row and enters ACT; or if current burst is being executing and burst done and the timing condition of active next row is not met, enters PRE; or if current burst is being executing and burst not done and next bank is idle, active next row and enters ACT_ALTER; or if current burst isn't being executing and current row is active, access current burst and enters ACCESS; or if current burst isn't being executing and current bank is idle, active current row and enters ACT; or if current burst isn't being executing and current row is not active, precharge current bank and enters PRE.
- In ACT_ALTER: If current burst is being executing and burst done and next row is active, access next burst and enters ACCESS; or if current burst is being executing and burst done and the timing condition of access next burst is not met, enters ACT; or if current burst isn't being executing and current row is active, access current burst and enters ACCESS; or if current burst isn't being executing and current bank is idle, active current row and enters ACT; or if current burst isn't being executing and current row is not active, precharge current bank and enters PRE.

State and command transfer diagram:



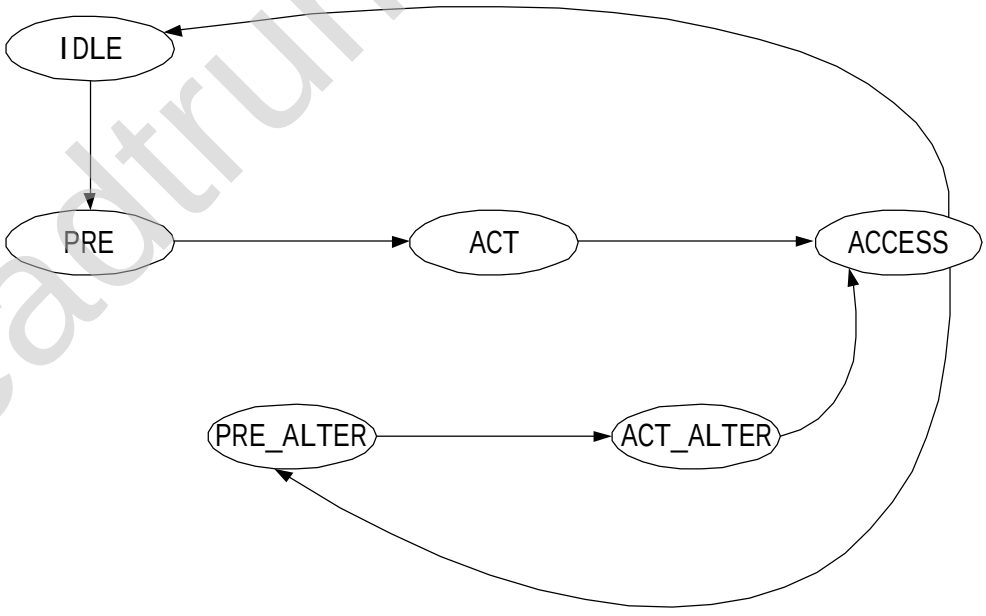
DMEM controller state tranfer

Figure 5.2-28 DMEM controller state transfer - 1



example 1:
two bursts and both need precharging

Figure 5.2-29 DMEM controller state transfer - 2



example 2:
two bursts and both need precharging

Figure 5.2-30 DMEM controller state transfer - 3

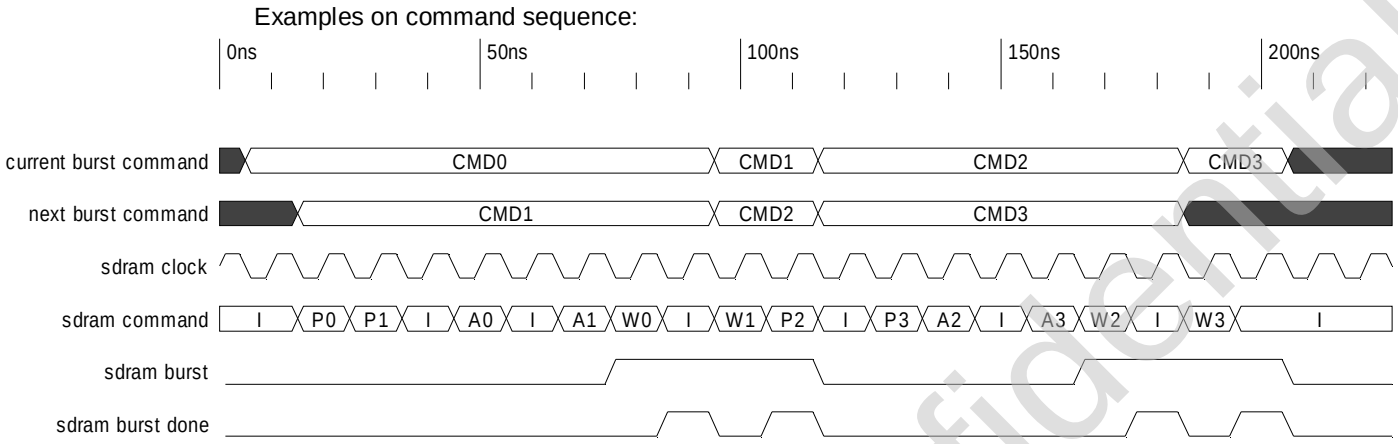


Figure 5.2-31 DMEM controller state transfer - 4

Note:

1, CMD0, CMD1, CMD2, CMD3: burst 0/1/2/3 command

I: Idle

P0, P1, P2, P3: burst 0/1/2/3 precharge

A0, A1, A2, A3: burst 0/1/2/3 active

W0, W1, W2, W3: burst 0/1/2/3 write (or read)

2, Suppose that tRP, tRCD and tRRD are 3-cycle.

Main command path mode control register:

- **drf_rowhit_en** : Row-hit access enable
- **drf_alternative_mode0_en** : Alternative-bank access mode 0 enable
- **drf_alternative_mode1_en** : Alternative-bank access mode 1 enable

Above three bits should always be set to improve efficiency.

Notes:

- Not support any burst is terminated/interrupted by any command before it completes. For example, it isn't supported that one burst is terminated by BURST TERMINATE cmmand, or by new READ / WRITE, or by PRECHARGE, etc.
- Not support CONCURRENT AUTO PRECHARGE.
- Not support BURST READ / SINGLE WRITE mode.

5.2.4.5.5 Refresh Control

Auto-refresh functions:

- Support hardware-automatically auto-refresh. This function can be enabled or disabled.
- Support configurable auto-refresh interval.
- Support two options for auto-refresh, chip by chip refresh mode, and all chips at the same time mode. The option select depends on LDO driving strength.

EMC provides the following registers to control external memory auto-refresh.

drf_auto_ref_en is used to enable automatic hardware AUTO-REFRESH.

Remember: This bit must be set if DMEM is not in self-refresh mode. Otherwise, data in DMEM may be lost.

drf_auto_ref_allcs is enable bit for that all CSs are auto-refreshed at the same time.

For stacked multi-chip SDRAM, we need auto-refresh more than one chip. There are two ways to do it, one is to handle one chip by one chip and the other is to handle all chips at the same time.

For the first solution, **drf_auto_ref_allcs** should be cleared. And For the second solution,

drf_auto_ref_allcs is set.

Obviously, the second solution is more efficient. However, we MUST guarantee our chip can supply so much current when all chips are operated at the same time.

5.2.4.5.6 Sleep Control

EMC should guarantee two conditions to make DMEM sleep or wakeup. One is that EMC should issue self-refresh or resume command to make DMEM sleep or wakeup. The other is that EMC should guarantee one burst completed before issuing self-refresh.

DMEM Sleep and wakeup functions:

- Support software-issued sleep and wakeup. And each CS can be controlled separately. Software should guarantee burst completed and issue self-refresh and resume manually.
- Support hardware-automatically sleep and wakeup. EMC guarantee burst completed and issue self-refresh and resume automatically.

For manually sleep mode:

- Software should guarantee there is no new burst requests for external memory, and check **rfemc_idle_sync** to make sure last bursts completed.
- Software should close auto-refresh before issuing self-refresh and open auto-refresh after issuing resume.

For automatically sleep mode:

- Support two modes for auto-sleep, mode 0 and mode 1.
- For mode 0, if received sleep requests, DMEM controller waits for current channel burst completing firstly, then DMEM controller issues precharge all banks and self-refresh automatically. At last, DMEM controller feeds back sleep signal. If received wakeup, DMEM controller resumes device automatically.
- For mode 1, if received sleep requests, DMEM controller waits for current channel burst completing firstly, then DMEM controller doesn't issue precharge all banks and

self-refresh immediately, but it makes use of one auto-refresh counter to guarantee all rows are refreshed at least one time during this wakeup period, if there are some row left not refreshed, DMEM controller refreshes these rows at first, then DMEM controller issues precharge all banks and self-refresh automatically. At last, DMEM controller feeds back sleep signal. If received wakeup, DMEM controller resumes device automatically and auto refresh counter should be cleared by software.

EMC provides the following registers to control sleep.

- auto-sleep control:

rf_auto_sleep_en is used to enable EMC auto-sleep and auto-resume.

1: enable

0: disable

drf_auto_sleep_mode is EMC auto-sleep/resume mode.

1: EMC guarantees all rows are refreshed before sleep.

0: EMC doesn't check whether some rows are still not refreshed.

cmd_chip_sleep is sleep status for each CS.

- auto-refresh control before sleep:

Auto-refresh can be issued in two mode, normal mode auto-refresh and sleep mode auto-refresh.

Sleep mode auto-refresh is issued before sleep to guarantee all rows are refreshed. In this mode, the only operation of EMC is auto-refresh. The following registers are used in sleep mode auto-refresh, and **drf_auto_sleep_mode** should be set.

drf_auto_sleep_t_ref is auto-refresh interval time before sleeping, and it can be configured to a small value to speed up auto-refresh. Relatively, **drf_t_ref** is used in normal mode, and it is always configured according to device data sheet.

drf_ref_cnt_thr is used to inform hardware how many times auto-refresh should be issued before sleep. In general, this value is configured as row number.

ref_cnt_done is a status indicating required refresh number is completed.

drf_ref_cnt_rst is used to reset refresh counter.

- Idle status before sleep:

rfemc_idle_sync is a status indicating EMC enters IDLE state and last bursts completed.

5.2.4.5.7 Software Commands

Software direct command functions:

- Support the following software direct command list for SDRAM:
  - Pre-charge all banks
  - Auto-refresh
  - Load mode register and extended mode register
  - Self-refresh
  - Resume
- For each command, there is one bit to check done status.
- Support two options for software commands, one command for one chip, and one command for all chips. The option select depends on LDO driving strength.

Notes:

- Not support SDRAM POWER DOWN AND DEEP POWER DOWN mode.
- Not support CLOCK SUSPEND mode.

EMC provide the following registers to issue software commands.

- **dsoft_pre_all**: Issue one PRECHARGE all banks command
- **dsoft_auto_ref**: Issue one AUTO-REFRESH command
- **dsoft_ld_mdreg**: Issue one LOAD MODE REGISTER command. Mode register value should be configured in drf_mode_reg before issuing this command.
- **dsoft_self_ref**: Enter SELF-REFRESH
- **dsoft_resume**: Exit SELF-REFRESH

drf_mode_reg[15:14] is mapped to BA[1:0].

drf_mode_reg[13:0] is mapped to A[13:0].

For stacked SDRAMs, when software commands are issued, two options are provided for chip select. If **dsoft_cmd_allcs** is set, the command is active on all CS at the same time. If it is cleared, the **dsoft_cs** is used to select which CS is active.

5.2.4.5.8 Data Path Control

The main function of DMEM data path logic is to handle data, DM and DQS.

Through several stage-configurable shift registers, burst commands and related information are transmitted from command path to data path. Data path should:

- Adjust the timing of data, DM and DQS, which are described in following chapter.
- Request and receive write data from each channel
- Translate write data format and sequence according to SDR/DDR and 16-bit/32-bit.
- Transmit write data on external memory bus, and the specific circuit is described in EMC PHY Specifications
- Receive and sample read data from external memory bus, and the specific circuit is described in EMC PHY Specifications, and the function is described in following chapter.
- Translate read data format and sequence according to SDR/DDR and 16-bit/32-bit.
- Transmit read data to each channel.

The detailed features in each task are as follows.

Data path adjust the timing of data, DM and DQS

- This function is described in following chapter

Data path requests and receives write data from each channel

- Channel information is got from the shift registers.

Data path translates write data format and sequence according to SDR/DDR and 16-bit/32-bit

- For 16-bit DMEM, higher 16-bit of 32-bit data is executed firstly and is written into the column address that LSB is 0, and lower 16-bit of 32-bit data is executed secondly and is written into the column address that LSB is 1.
- For 16-bit SDR, the maximum EMC core data rate is as four times as external memory data rate, so data rate need be matched.
- For 32-bit SDR, the maximum EMC core data rate is as twice as external memory data rate, so data rate need be matched.
- For 16-bit DDR, the maximum EMC core data rate is as twice as external memory data rate, so data rate need be matched.
- For 32-bit DDR, the maximum EMC core data rate is the same as external memory data rate.

Data path transmits write data on external memory bus.

- For SDR, write data and DM is latched output trigged by clk_emc
- For DDR, write data and DM is latched output trigged by clk_em_wr, which is generated from clk_emc through a delay line. Through coarse and fine timing adjustment, write data and DM need delay about 0.75 DMEM clock cycle (generally, coarse adjustment achieves 0.5 and delay line achieve about 0.25).

Data path receives and samples read data from external memory bus

- This function is described in following chapter

Data path translates read data format and sequence according to SDR/DDR and 16-bit/32-bit.

- For 16-bit DMEM, to consecutive two receiving data, the first one is stored in higher 16-bit of 32-bit data, and the second is stored in lower 16-bit of 32-bit data.
- For 16-bit SDR, the maximum EMC core data rate is as four times as external memory data rate, so data rate need be matched.
- For 32-bit SDR, the maximum EMC core data rate is as twice as external memory data rate, so data rate need be matched.
- For 16-bit DDR, the maximum EMC core data rate is as twice as external memory data rate, so data rate need be matched.
- For 32-bit DDR, the maximum EMC core data rate is the same as external memory data rate

Data path transmits read data to each channel.

- Channel information is got from the shift registers.

5.2.4.6 DMEM Timing Descriptions

Timing control registers are divided into two groups, one is used to control cycle-based command timing sequence, and the other is used to adjust data path and sampling timing.

5.2.4.6.1 Timing Diagrams

SDRAM is configured that CAS Latency is 3 and Burst Length is 2.

SDRAM Initialize

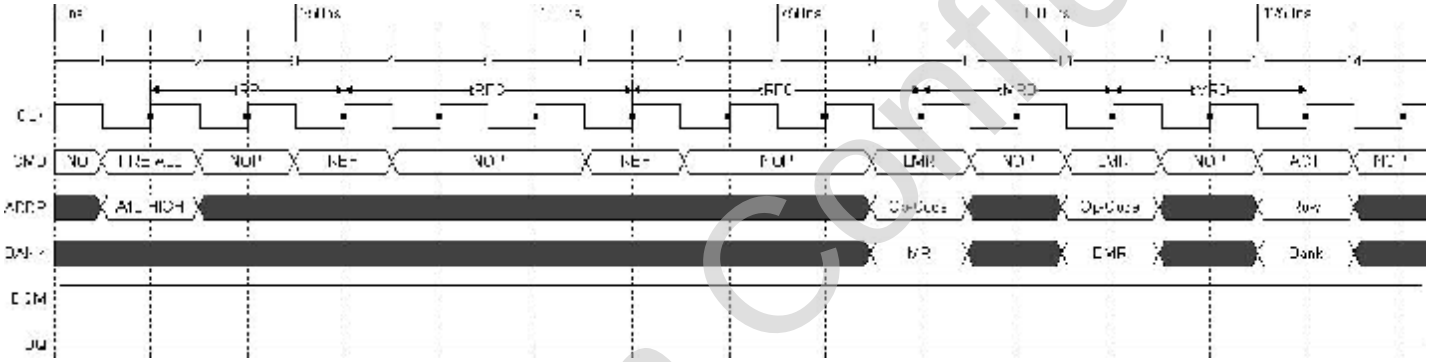


Figure 5.2-32 SDRAM initialize timing diagram

SDRAM Auto-Refresh

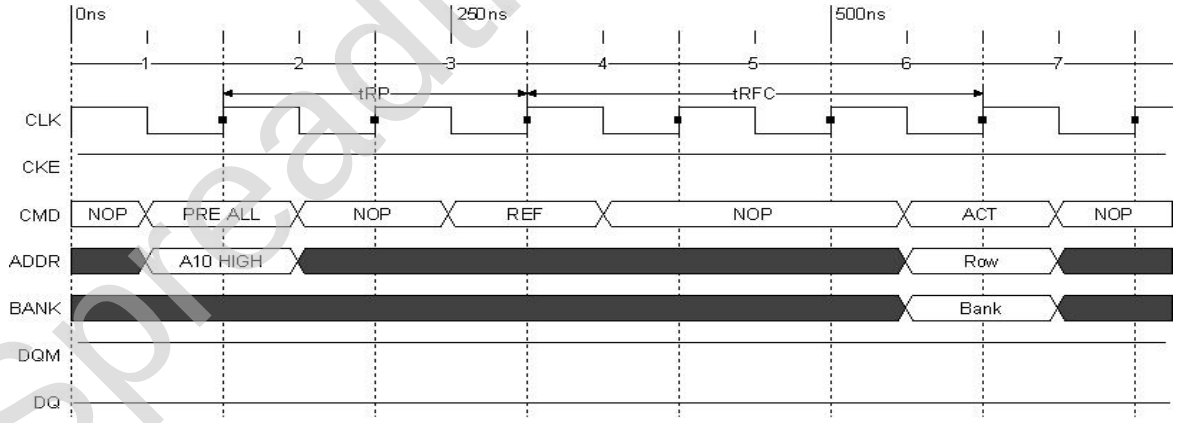


Figure 5.2-33 SDRAM auto-refresh timing diagram

SDRAM Self-Refresh

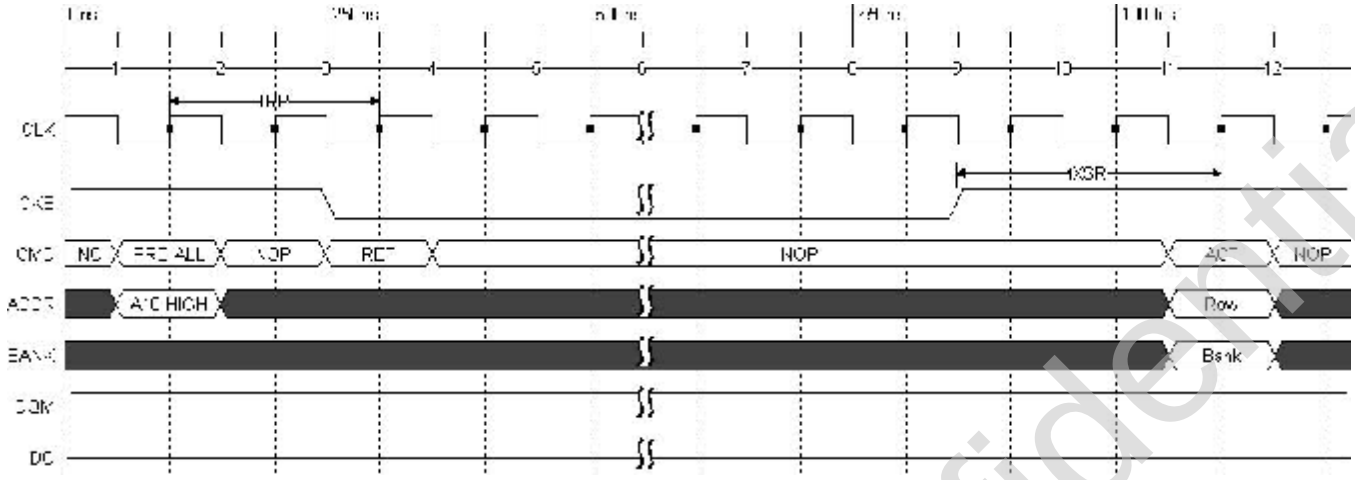


Figure 5.2-34 SDRAM self-refresh timing diagram

SDR-SDRAM Read

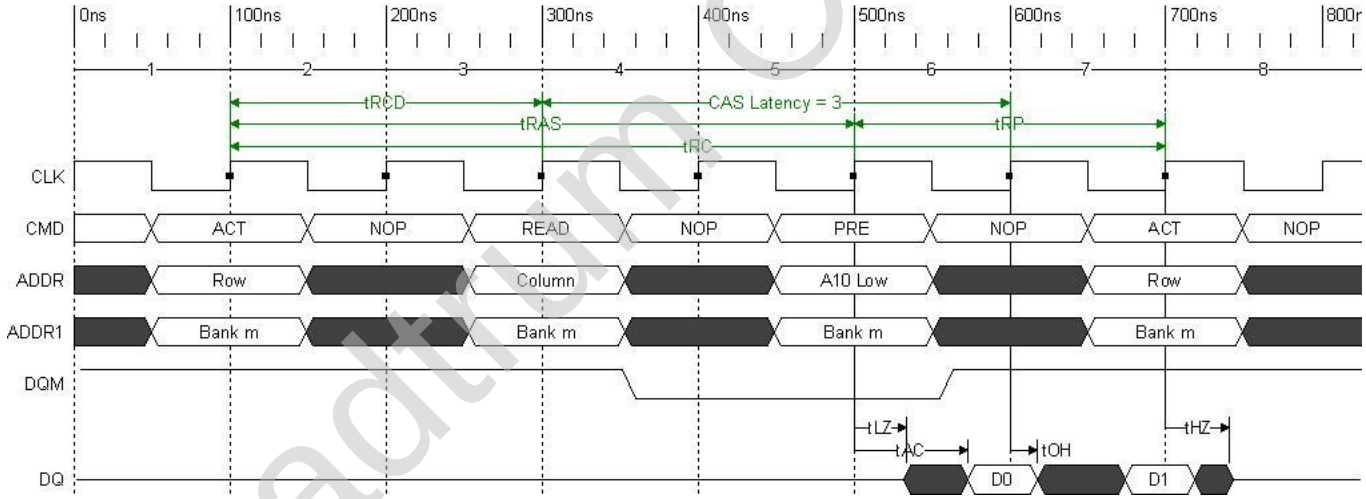


Figure 5.2-35 SDR-SDRAM read timing diagram

SDR-SDRAM alternative-bank Read

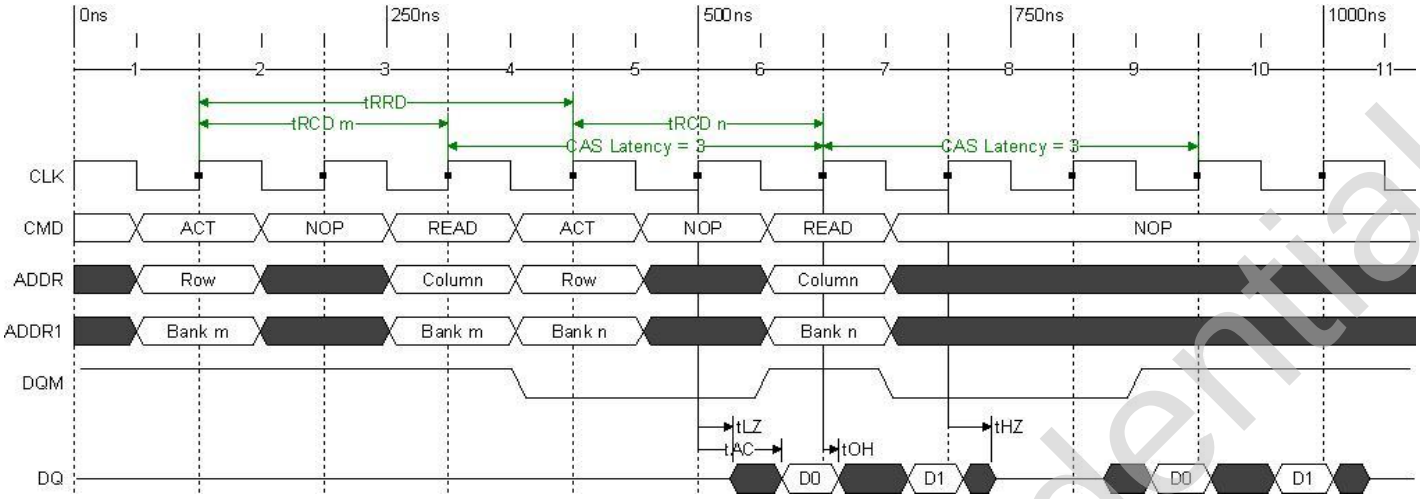


Figure 5.2-36 SDR-SDRAM alternative-bank read timing diagram

SDR-SDRAM Write

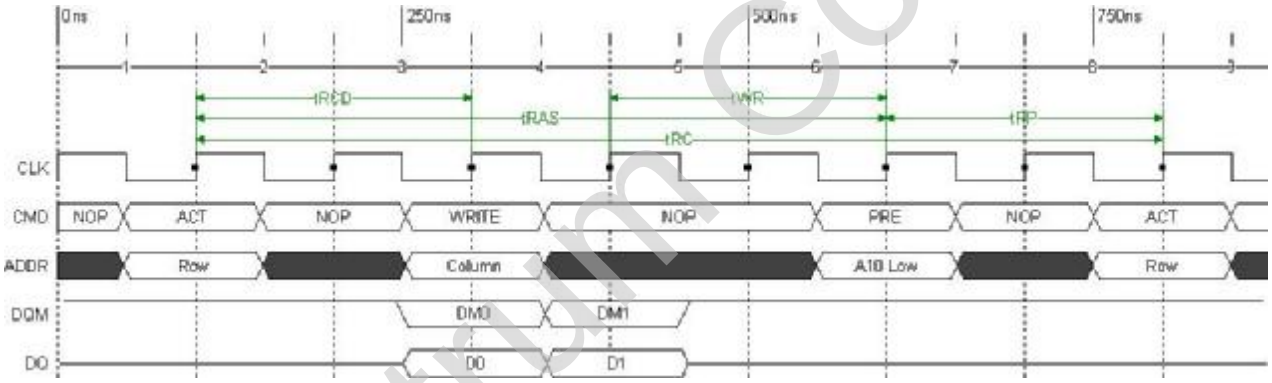


Figure 5.2-37 SDR-SDRAM write timing diagram

SDR-SDRAM alternative-bank Write

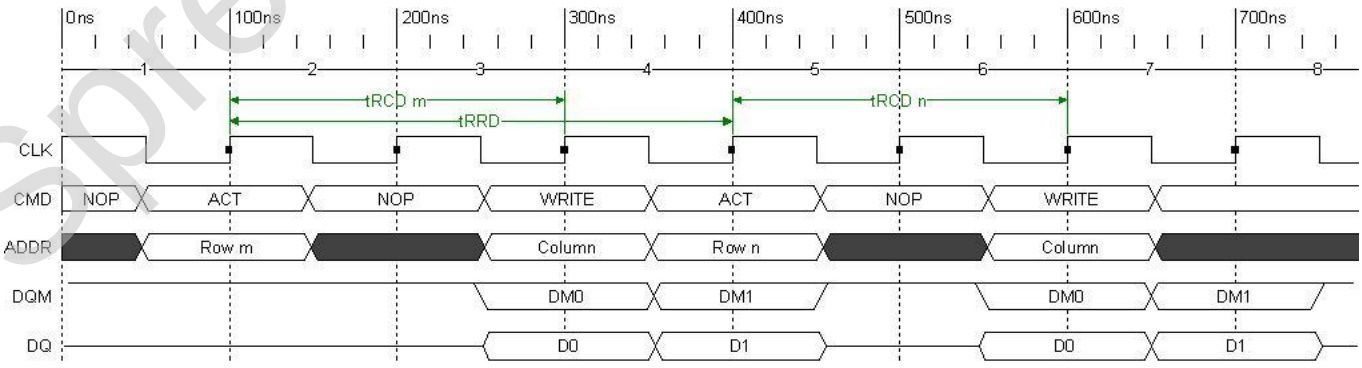


Figure 5.2-38 SDR-SDRAM alternative-bank write timing diagram

SDR-SDRAM Read-Write-Read turn-around

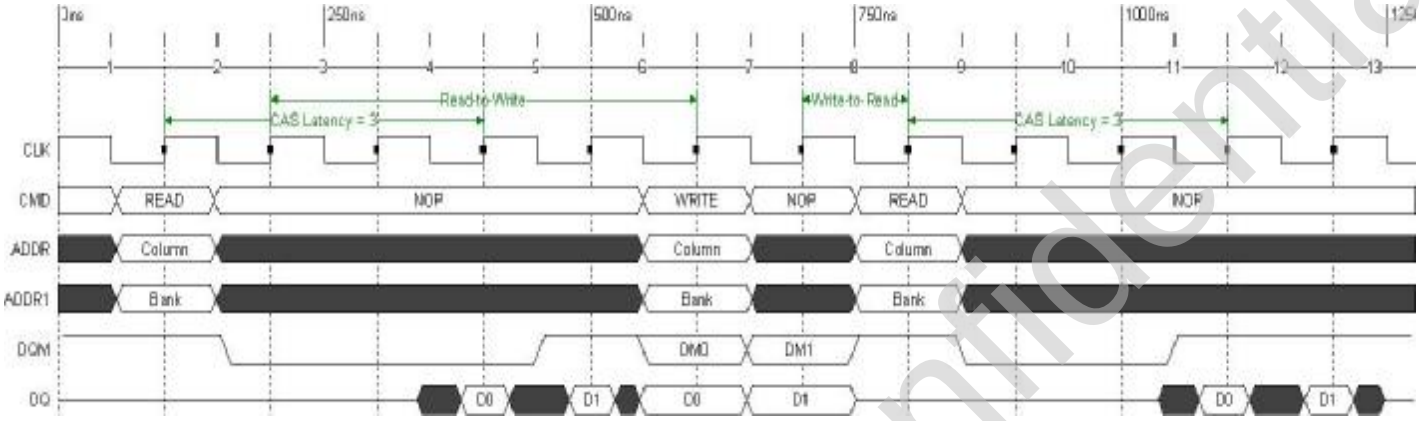


Figure 5.2-39 SDR-SDRAM read-write turn-around timing diagram

DDR-SDRAM Read

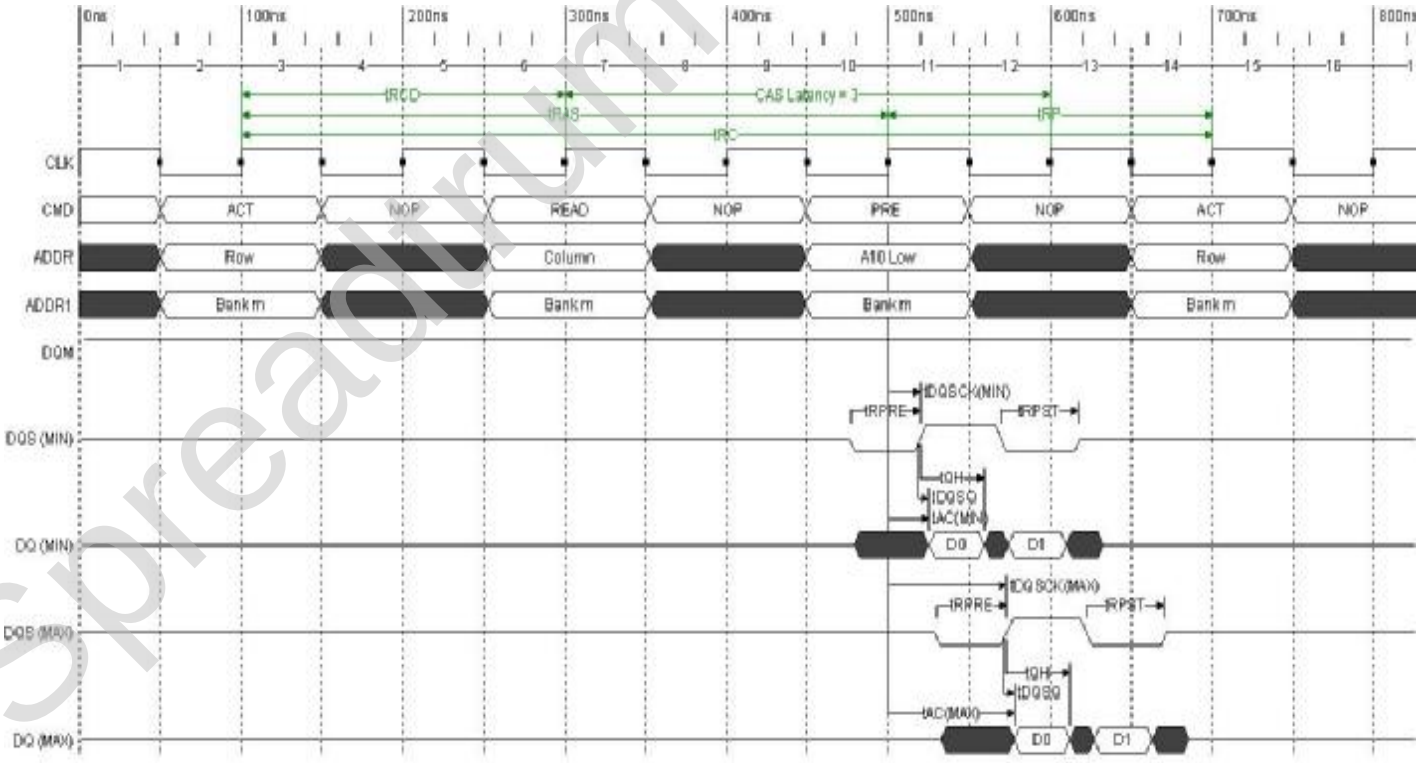


Figure 5.2-40 DDR-SDRAM read timing diagram

DDR-SDRAM Write

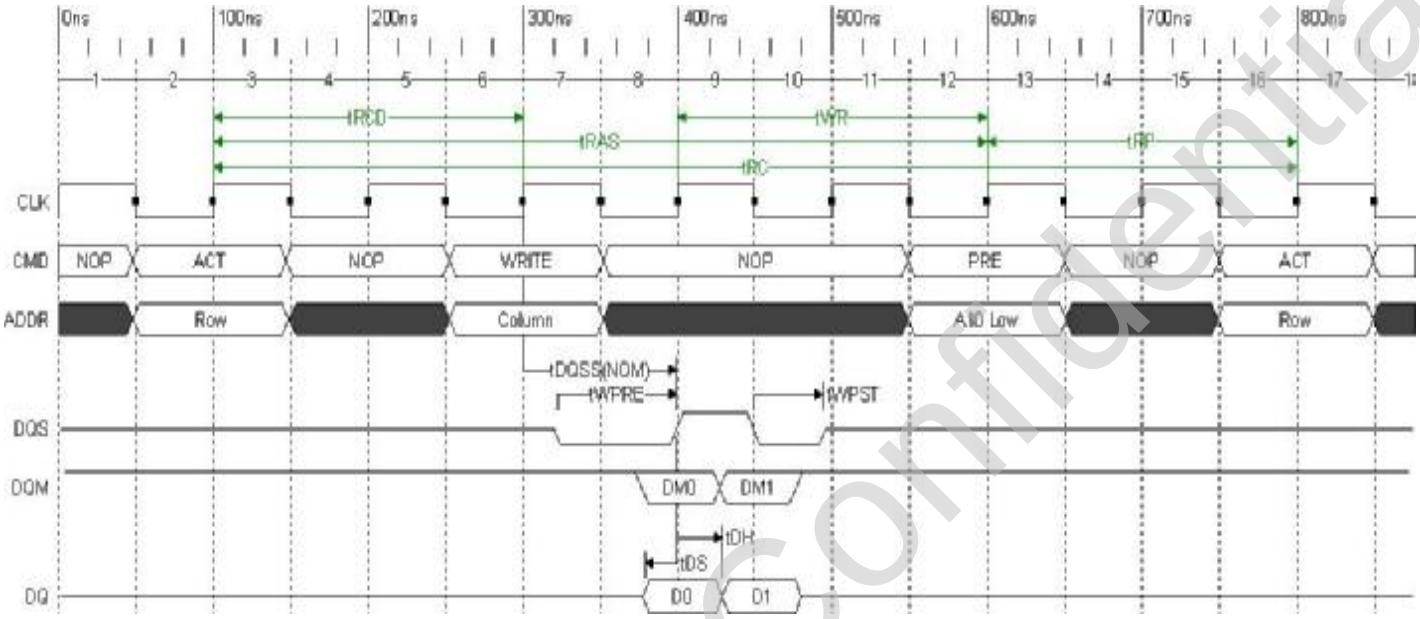


Figure 5.2-41 DDR-SDRAM write timing diagram

DDR-SDRAM Read-Write-Read turn-around

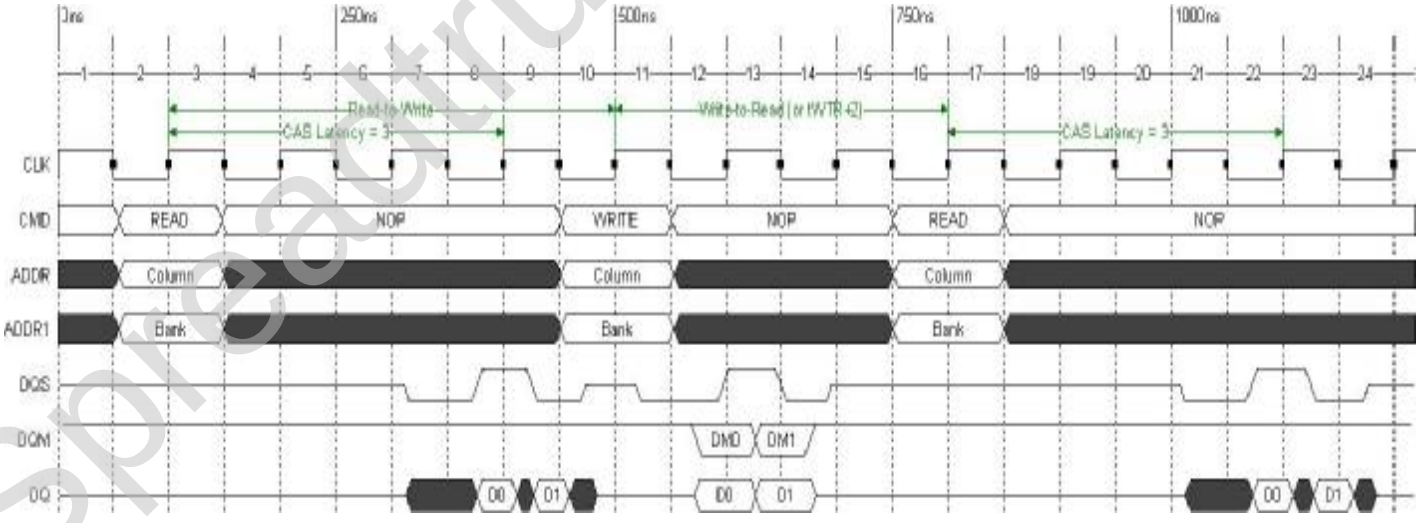


Figure 5.2-42 DDR-SDRAM read-write turn-around timing diagram

DDR-SDRAM alternative-CS Read-Read turn-around

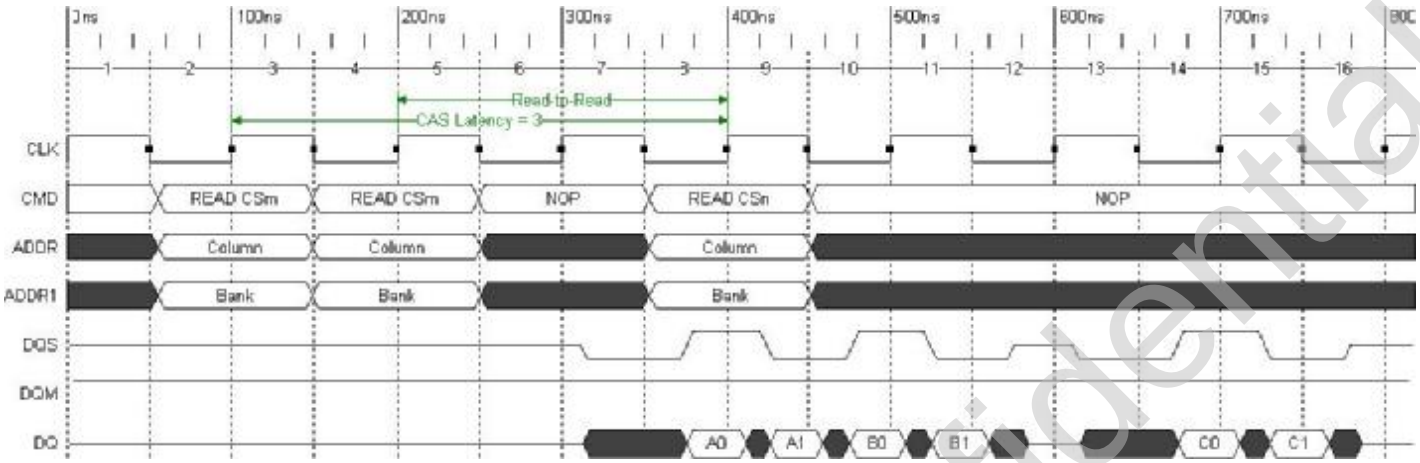


Figure 5.2-43 DDR-SDRAM alternative-CS read-read turn-around timing diagram

5.2.4.6.2 Output Clock Timing Control

- **drf_clkdmem_out_en** is used to enable DMEM output clock.
  1: enable
  0: disable

- **drf_clkdmem_out_sel** is used to adjust DMEM output clock phase. One step is one clk_emc cycle, or 1/2 DMEM clock cycle.

- **rf_clkdmem_out_dl_sel** and **rf_clkdmem_out_dl_inv** is used for related delay line to adjust DMEM output clock timing.

5.2.4.6.3 Command Timing Control

All timing parameters of SDR-SDRAM and DDR-SDRAM can be met by controlling DMEM configuration registers.

Note, the real wait cycles is (**drf_t_x** register value + 1), for example, if 3 cycles are needed for **Trcd** in data sheet, **drf_t_rcd** should be set to 2.

The following is detailed manual to guarantee the DMEM timing parameters.
T is DMEM clock cycle time, or clk_emc/2 clock cycle.
Tref is clk_emc_ref clock cycle.

- Minimum PRECHARGE command period time (or tRP):

We should use **drf_t_rp** to guarantee it. That is, (**drf_t_rp**+1)*T >= tRP.

- Minimum ACTIVE to READ or WRITE delay (or minimum RAS to CAS delay, or tRCD):

  We should use **drf_t_rcd** to guarantee it. That is, (**drf_t_rcd**+1)*T >= tRCD.

- Minimum ACTIVE to PRECHARGE time (or minimum row active time, or tRAS-MIN):

  We should use **drf_t_ras** to guarantee it. That is, (**drf_t_ras**+1)*T >= tRAS-MIN.

- Maximum ACTIVE to PRECHARGE time (or minimum row active time, or tRAS-MAX):

  We should use **drf_t_ref** to guarantee it because all banks are pre-charged before auto-refresh. That is, (**drf_t_ref**+1)*Tref <= tRAS-MAX. In general, this condition is met.

- Minimum ACTIVE(m) to ACTIVE(n) (in different bank) time (or tRRD):

  We should use **drf_t_rrd** to guarantee it. That is, (**drf_t_rrd**+1)*T >= tRRD.

- Minimum ACTIVE(m) to ACTIVE(m) (in same bank) time (or tRC):

  a. Because in the same bank there is a PRECHARGE in two ACTIVE in normal Read/Write, so we should also use **drf_t_ras** to guarantee tRC. That is, (**drf_t_ras**+**drf_t_rp**+2)*T >= tRC.

  b. There are only two cases that there isn't PRECHARGE, one is auto-refresh progress is in two ACTIVE. That is, (**drf_t_rp**+**drf_t_rfc**+3)*T >= tRC. In general, this condition is always met.

  c. The other is software-issued PRECHARGE ALL BANK command is in two ACTIVE. That is, software should guarantee PRECHARGE ALL BANK period is more than tRC. In general, this condition is always met.

- Minimum Write recovery time (or minimum last data-in to PRECHARGE time, or tWR, or tDPL, or tRDL):

  We should use **drf_t_wr** to guarantee it.

  For SDR, (**drf_t_wr**+1)*T >= tWR

  For DDR, (**drf_t_wr** -1)*T >= tWR

  (Because EMC is designed for both SDR and DDR, there are fixed 2 cycle difference between them)

- Maximum Refresh period (or tREF):

  We should use **drf_t_ref** to guarantee it. That is, (**drf_t_ref**+1)*Tref*(row number) <= tREF

- Minimum AUTO-REFRESH period (or tRFC):

  We should use **drf_t_rfc** to guarantee it. That is, (**drf_t_rfc**+2)*T >= tRFC

- Minimum SELF-REFRESH time (tRAS for Micron, Samsung, etc):

  We should use **drf_t_xsr** to guarantee it. That is, (**drf_t_xsr**+2)*T >= this minimum time

- Minimum RESUME time (or exit SELF-REFRESH to ACTIVE or AUTO-REFRESH delay, or tXSR for Micron, or tRC for Samsung, etc):

We should use **drf_t_xsr** to quarantee it. That is, (**drf_t_xsr**+2)*T >= this minimum time

- Minimum LOAD MODE REGISTER to ACTIVE or REFRESH delay (or tMRD):
  We should use **drf_t_mrd** to guarantee it. That is, (**drf_t_mrd**+2)*T >= tMRD

- **drf_t_rtw** is read-to-write turn-around time, used to prevent data bus conflict. It's from the last read in command stage to the next write in command stage.
  For SDR and DDR, normally, it should be configure to 2 (3 cycles) for CAS latency 2, or 3 (4 cycles) for CAS latency 3.

- **drf_t_wtr** is write-to-read turn-around time. It's from the last write in command stage to the next read in command stage. And this register is used to guarantee tWTR for DDR. However, unlike other parameters, this register has the different physical definitions with tWTR.
  For SDR, it should always be configured to 0 (1 cycle).
  For DDR, (**drf_t_wtr**+1)*T >= tWTR+2

- **drf_t_rtr** is read-to-read turn-around time between different CSs, used to prevent two DDR-SDRAM DQS conflict. It's from the last read in command stage on CSn to the next read in command stage on CSm.
  For SDR, it should always be configured to 0 (1 cycle).
  For DDR, it should be configured to 0 (1 cycle) for only supporting one CS, or 1(2 cycle) for supporting two or above.

5.2.4.6.4 Write Data Path Timing Control

- Support independent and configurable write data latency. For SDR, it's zero. For DDR, it should be adjusted. This adjustment includes coarse adjustment and fine adjustment.
  - ü For coarse adjustment, supporting 0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5 DMEM clock cycles delay
  - ü For fine adjustment, support one delay line to control delay value. This delay line is also used for write DQM delay control.

  drf_wdata_latency is used to adjust write data latency. One step is one clk_emc cycle.
  rf_clkwr_dl_sel and **rf_clkwr_dl_inv** is used for related delay line to adjust write data latency.

- Support independent and configurable data pad OE timing. It's used for SDR and DDR, and only coarse adjustment is on this signal and no delay line for fine adjustment.
  - ü For coarse adjustment, support configurable delay of 0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5 DMEM clock cycles, and support configurable period of one DMEM burst cycles, one DMEM burst cycles + 0.5 DMEM clock cycles, one DMEM burst cycles + 1 DMEM clock cycles, …, one DMEM burst cycles + 3.5 DMEM clock cycles.

  drf_data_oe_sel is used to adjust data PAD OE timing. One bit is one range, and the delay between two consecutive ranges is one clk_emc cycle. Then all selected ranges are OR output.

- Support independent and configurable write DQM latency. For SDR, it's zero. For DDR, it should be adjusted. This adjustment includes coarse adjustment and fine adjustment.
  - For coarse adjustment, supporting 0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5 DMEM clock cycles delay
  - For fine adjustment, support one delay line to control delay value. This delay line is also used for write data delay control.

  drf_wdm_latency is used to adjust write DM latency. One step is one clk_emc cycle.

  rf_clkwr_dl_sel and **rf_clkwr_dl_inv** is used for related delay line to adjust write DQM latency.

- Support independent and configurable output DQS timing. It's only used for DDR, and this adjustment includes coarse adjustment and fine adjustment.
  - For coarse adjustment, supporting 0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5 DMEM clock cycles delay
  - For fine adjustment, support one delay line to control delay value.

  drf_dqs_out_sel is used to adjust DQS output latency. One step is one clk_emc cycle.

  rf_dqs_out_dl_sel and **rf_dqs_out_dl_inv** is used for related delay line to adjust output DQS.

- Support independent and configurable DQS pad OE timing. It's only used for DDR, and only coarse adjustment is on this signal and no delay line for fine adjustment.
  - For coarse adjustment, support configurable delay of 0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5 DMEM clock cycles, and support configurable period of one DMEM burst cycles, one DMEM burst cycles + 0.5 DMEM clock cycles, one DMEM burst cycles + 1 DMEM clock cycles, …, one DMEM burst cycles + 3.5 DMEM clock cycles.

  drf_dqs_oe_sel is used to adjust DQS PAD OE timing. One bit is one range, and the delay between two consecutive ranges is one clk_emc cycle. Then all selected ranges are OR output.

5.2.4.6.5 Read Data Path Timing Control

- Support independent and configurable sampling clock timing. It's only used for SDR, and this adjustment includes coarse adjustment and fine adjustment.
  - For coarse adjustment, supporting 0, 0.5, 1, 1.5, …, 7, 7.5 DMEM clock cycles delay
  - For fine adjustment, support four delay lines to control delay value, and each delay line controls one byte data sampling clock. These delay lines are shared with DQS input control.

  drf_clkdmem_in_sel is used to adjust sample clock phase. One step is one clk_emc cycle.

  rf_dqs_in_pos_dl_0_sel and **rf_dqs_in_pos_dl_0_inv** is used for related delay line to adjust sampling clock positive edge timing.

  rf_dqs_in_pos_dl_1_sel and **rf_dqs_in_pos_dl_1_inv** is used for related delay line to adjust sampling clock positive edge timing.

  rf_dqs_in_pos_dl_2_sel and **rf_dqs_in_pos_dl_2_inv** is used for related delay line to adjust sampling clock positive edge timing.

  rf_dqs_in_pos_dl_3_sel and **rf_dqs_in_pos_dl_3_inv** is used for related delay line to adjust sampling clock positive edge timing.

rf_dqs_in_neg_dl_0_sel and **rf_dqs_in_neg_dl_0_inv** is used for related delay line to adjust sampling clock negative edge timing.

rf_dqs_in_neg_dl_1_sel and **rf_dqs_in_neg_dl_1_inv** is used for related delay line to adjust sampling clock negative edge timing.

rf_dqs_in_neg_dl_2_sel and **rf_dqs_in_neg_dl_2_inv** is used for related delay line to adjust sampling clock negative edge timing.

rf_dqs_in_neg_dl_3_sel and **rf_dqs_in_neg_dl_3_inv** is used for related delay line to adjust sampling clock negative edge timing.

- Support independent and configurable read data latency. It's used for SDR and DDR, and only coarse adjustment is on this signal and no delay line for fine adjustment.
  - For coarse adjustment, supporting 0, 0.5, 1, 1.5, …, 7, 7.5 DMEM clock cycles delay

drf_rdata_latency is used to adjust read data latency. One step is one clk_emc cycle.

- Support independent and configurable data pad IE timing. It's used for SDR and DDR, and only coarse adjustment is on this signal and no delay line for fine adjustment.
  - For coarse adjustment, support configurable delay of 0, 0.5, 1, 1.5, …, 7, 7.5 DMEM clock cycles, and support configurable period of one DMEM burst cycles, one DMEM burst cycles + 0.5 DMEM clock cycles, one DMEM burst cycles + 1 DMEM clock cycles, …, one DMEM burst cycles + 7.5 DMEM clock cycles.

drf_data_ie_sel is used to adjust data PAD IE timing. One bit is one range, and the delay between two consecutive ranges is one clk_emc cycle. Then all selected ranges are OR output.

- Support independent and configurable read DQM latency. For SDR, it's should be adjusted. For DDR, it's DON'T CARE. This adjustment only includes coarse adjustment.
  - For coarse adjustment, supporting 0, 0.5, 1, 1.5, 2, 2.5, 3 DMEM clock cycles delay (the last option is disabled)

drf_rdm_latency is used to adjust read DM latency. One step is one clk_emc cycle.

- Support independent and configurable DQS input timing. It's only used for DDR, and this adjustment only includes fine adjustment.
  - For fine adjustment, support four delay lines to control delay value, and each delay line controls one byte DQS input. These delay lines are shared with SDR sampling clock control.

- Support independent and configurable input DQS gate timing. It's only used for DDR, and this adjustment includes coarse adjustment and fine adjustment.
  - For coarse adjustment, support configurable delay of 0, 0.5, 1, 1.5, …, 7, 7.5 DMEM clock cycles, and support configurable period of one DMEM burst cycles, one DMEM burst cycles + 0.5 DMEM clock cycles, one DMEM burst cycles + 1 DMEM clock cycles, …, one DMEM burst cycles + 7.5 DMEM clock cycles.
  - For fine adjustment, support four delay lines to control delay value, and each delay controls one byte data DQS gate.

drf_dqs_gate_pre_sel and **drf_dqs_gate_pst_sel** is used to adjust DQS input mask timing. One bit is one range, and the delay between two consecutive ranges is one clk_emc cycle. Then all selected ranges are OR output.

rf_dqs_gate_pre_dl_0_sel and **rf_dqs_gate_pre_dl_0_inv** is used for related delay line to adjust DQS gate timing.

rf_dqs_gate_pre_dl_1_sel and **rf_dqs_gate_pre_dl_1_inv** is used for related delay line to adjust DQS gate timing.

rf_dqs_gate_pre_dl_2_sel and **rf_dqs_gate_pre_dl_2_inv** is used for related delay line to adjust DQS gate timing.

rf_dqs_gate_pre_dl_3_sel and **rf_dqs_gate_pre_dl_3_inv** is used for related delay line to adjust DQS gate timing.

rf_dqs_gate_pst_dl_0_sel and **rf_dqs_gate_pst_dl_0_inv** is used for related delay line to adjust DQS gate timing.

rf_dqs_gate_pst_dl_1_sel and **rf_dqs_gate_pst_dl_1_inv** is used for related delay line to adjust DQS gate timing.

rf_dqs_gate_pst_dl_2_sel and **rf_dqs_gate_pst_dl_2_inv** is used for related delay line to adjust DQS gate timing.

rf_dqs_gate_pst_dl_3_sel and **rf_dqs_gate_pst_dl_3_inv** is used for related delay line to adjust DQS gate timing.

- Support independent and configurable DQS pad IE timing. It's only used for DDR, and this adjustment includes coarse adjustment and fine adjustment.
  - For coarse adjustment, support configurable delay of 0, 0.5, 1, 1.5, …, 7, 7.5 DMEM clock cycles, and support configurable period of one DMEM burst cycles, one DMEM burst cycles + 0.5 DMEM clock cycles, one DMEM burst cycles + 1 DMEM clock cycles, …, one DMEM burst cycles + 7.5 DMEM clock cycles.
  - For fine adjustment, support one delay lines to control delay value.

drf_dqs_ie_sel is used to adjust DQS PAD IE timing. One bit is one range, and the delay between two consecutive ranges is one clk_emc cycle. Then all selected ranges are OR output.

rf_dqs_ie_dl_sel and **rf_dqs_ie_dl_inv** is used for related delay line to adjust DQS pad IE timing.

5.2.4.6.6 Sampling Control

Refer to EMC PHY specification for detailed circuit.

The base theory is described here:

Four dedicated sample clocks (each for one byte data) are used to sample data on external memory bus. These sample clocks have the same frequency as DMEM clock, but the phase is different. We guarantee the stability of sampling data by adjusting this phase.

Then the sampled data is written to FIFOs, and the async clock domains are passed through these FIFOs.

At last the output data from FIFOs is transmitted to DMEM controller.

SDR sampling clock features:

- For SDR, sampling clock is generated in DMEM controller. It's only active during burst data active, one cycle for one read data. Then this clock passes four delay lines to adjust sampling timing, and each delay line is related to one byte data. At last, the four clocks output from four delay lines are used for DFFs in sampling FIFO as trigging clocks.
- For SDR, support sample clock out-of-chip loop mode, and this function can be enabled or disabled. After sample clock is generated from DMEM controller, if this function is disabled, sample clock is connected to delay line directly, otherwise, sample clock output out of chip through CS3 pin firstly and then input through DQS pins to delay line.

- Note, if this function is used, CS3 pin is used as sample clock output, and related CS function is disabled.

DDR sampling clock features:

- For DDR, sampling clock is from four DQS signals (one DQS for one byte data), which is generated by DDR device. And also, this clock is only active during burst data active, one cycle for one data. After input from DQS pads, sampling clocks MUST be gated by DQS gate signals to remove unstable state, because DQS lines are high-Z state if no bursts issued. Then sampling clocks passes four delay lines to adjust sampling timing, and these delay lines are shared for SDR. At last, the four clocks output from four delay lines are used for DFFs in pose-edge sampling FIFO as trigging clocks, and at the same time, this four clocks are inverted to used for DFFs in negative-edge sampling FIFO as trigging clocks.
- From above description, the DQS gate signals are very important to guarantee sampling correction. The source of these DQS gate signals is generated in DMEM controller and only active during burst data active. Then it passes two groups of delay lines to adjust timing, and each group has four delay lines and each delay line is related to one DQS. There are two modes for the function of these two groups of delay lines. For mode 0, one group is used to meet fast-case rising edge timing and the other is used to meet slow-case rising edge timing, and the falling edge of DQS gate is generated automatically. For mode 1, one group is used to adjust DQS gate rising edge timing and the other is used to adjust falling edge timing. At last, the four DQS gate signals output from these delay lines are used for gating DQS.
- For DDR, support DQS gate signal out-of-chip loop mode, and this function can be enabled or disabled. DQS gate is generated from internal logic, and if this function is disabled, DQS gate is connected to delay line directly, otherwise, DQS gate output out of chip through CS3 pin firstly and then input through CKE1 pin to delay line.
- Note, if this function is used, CS3 and CKE1 pin are used as DQS gate output and input, and related CS and CKE function is disabled.

SDR sampling FIFOs features:

- One FIFO is used for one data and totally there are 32 FIFOs for SDR.
- All FIFOs have the same structure: 3-entry asynchronous FIFO.
- The writing clock is sampling clock
- The reading clock is clk_emc
- The writing pointer is generated in PHY
- The reading pointer is generated from DMEM controller.
- Because the frequency of sampling clock is the half of clk_emc and there is no accumulated error, so full and empty information is not needed, and we can guarantee data is valid in FIFO by adjusting read pointer delay timing (that is, read data latency described above).

DDR sampling FIFOs features:

- One pose-edge sampling FIFO and one neg-edge sampling FIFO are used for one data and totally there are 64 FIFOs for DDR. The 32 pose-edge sampling FIFO is shared for SDR.
- Both pose-edge sampling FIFO and neg-edge FIFO have the same structure: 3-entry asynchronous FIFO.
- The writing clock of pose-edge sampling FIFO is pose-edge sampling clock and the writing clock of neg-edge sampling FIFO is neg-edge sampling clock.
- The reading clock of both is clk_emc.
- The writing pointers of both are generated in PHY. One is trigged by pose-edge sampling clock and the other is trigged by neg-edge sampling clock.
- The reading pointers of both are the same one, and it is generated from DMEM controller.
- Because the frequency of both sampling clock is the half of clk_emc and there is no accumulated error, so full and empty information of both is not needed, and we can

guarantee data is valid in both FIFO by adjusting read pointer delay timing (that is, read data latency described above).

Sample FIFO Reset:

- **drf_sample_rst** is used to reset DMEM sample FIFO by software.
- **drf_sample_auto_rst_en** is used to enable resetting DMEM sample FIFO automatically during each auto-refresh and resume.

5.2.4.7 PHY Descriptions

All constraints described as follows should be checked in FF, TT and SS cases.

5.2.4.7.1 SDR Sampling Circuit Timing Budget

Sampling circuit is described as follows.

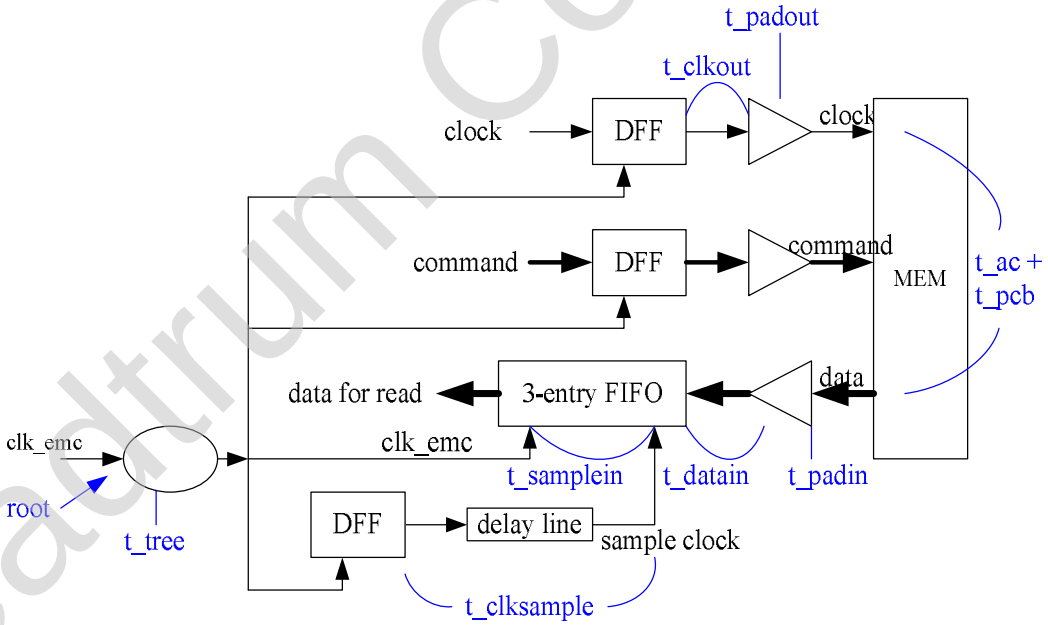


Figure 5.2-44 SDR sampling circuit

In order to make sampling stable, EMC should guarantee some timing:

- Data sample setup stable:

  (t_clkout + t_padout + t_AC + t_pcb + t_padin + t_datain + DFF setup time + clock tree skew) < (t_clksample + 2 * clk_emc cycle time)
- Data sample hold stable:

(t_clkout + t_padout + 2 * clk_emc cycle time + t_OH + t_pcb + t_padin + t_datain + DFF setup time - clock tree skew) > (t_clksample + 2 * clk_emc cycle time)

- Sample FIFO reading stable:

  (t_clksample + DFF output delay + t_samplein + DFF setup time + clock tree skew) < (1 * clk_emc cycle time)

5.2.4.7.2 DDR Output Data Timing Budget

Output data circuit is described as follows.

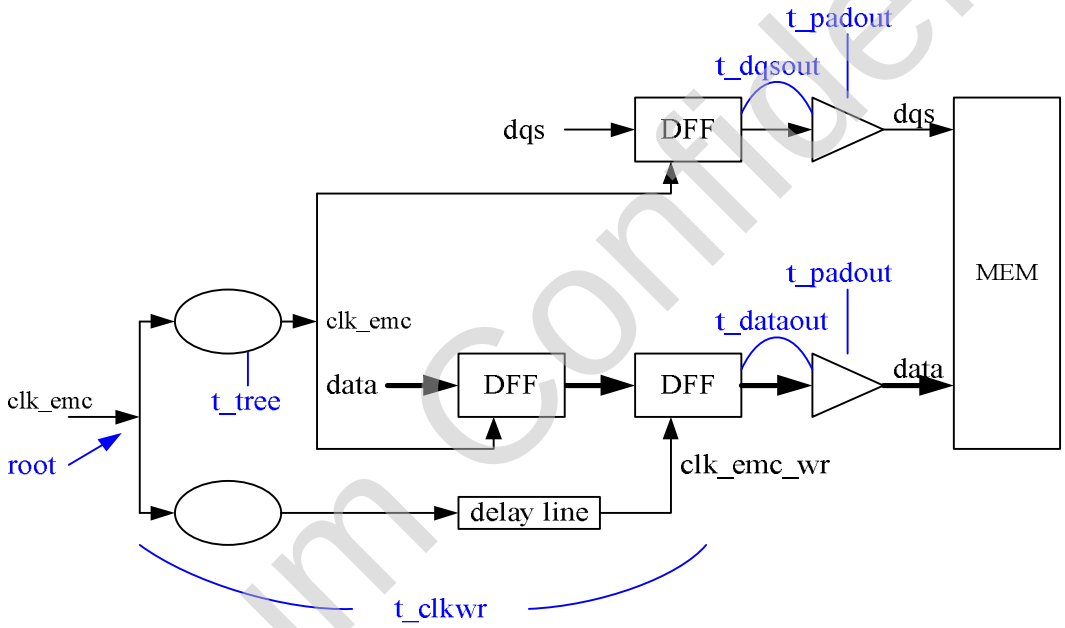


Figure 5.2-45 DDR sampling circuit

- clk_emc_wr DFF setup:

  (t_tree + DFF output delay + DFF setup time) < t_clkwr
- output data setup to DQS:

  (t_clkwr + DFF output delay + t_dataout + t_padout + data skew + t_DS) < (t_tree + DFF output delay + t_dqsout + t_padout)
- output data hold to DQS:

  (t_clkwr + DFF output delay + t_dataout + t_padout - data skew + 1 * clk_emc cycle time - t_DH) > (t_tree + DFF output delay + t_dqsout + t_padout)

5.2.4.7.3 DDR Sampling Circuit Timing Budget

Sampling circuit is described as follows.

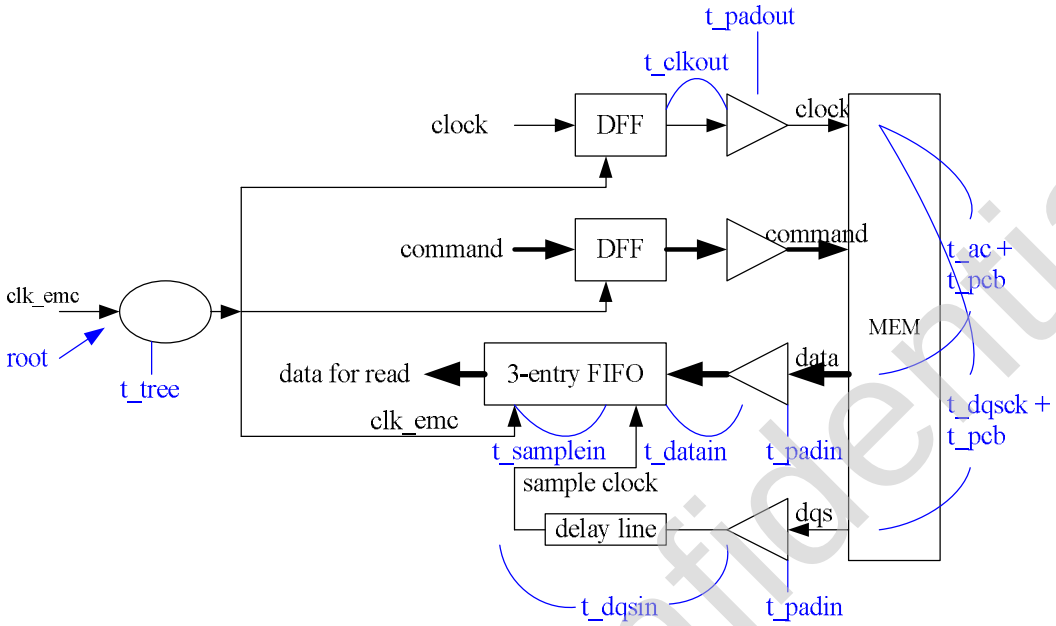


Figure 5.2-46 DDR sampling circuit

- Data sample setup stable:
  (t_padin + t_datain + DFF setup time + data skew) < (t_padin + t_dqsin - t_DQSQ)
- Data sample hold stable:
  (t_padin + t_datain + DFF setup time - data skew + data valid window) > (t_padin + t_dqsin - t_DQSQ)
  Or (t_padin + t_datain + DFF setup time - data skew) > (t_padin + t_dqsin - t_QH)
- Sample FIFO reading stable:
  (DFF output delay + t_clkout + t_padout + t_DQSCK_MAX + t_pcb + t_padin + t_dqsin + DFF output delay + t_samplein + DFF setup time) < (3 * clk_emc cycle time)

5.2.4.7.4 DDR DQS gating Circuit Timing Budget

DQS gating circuit is described as follows.

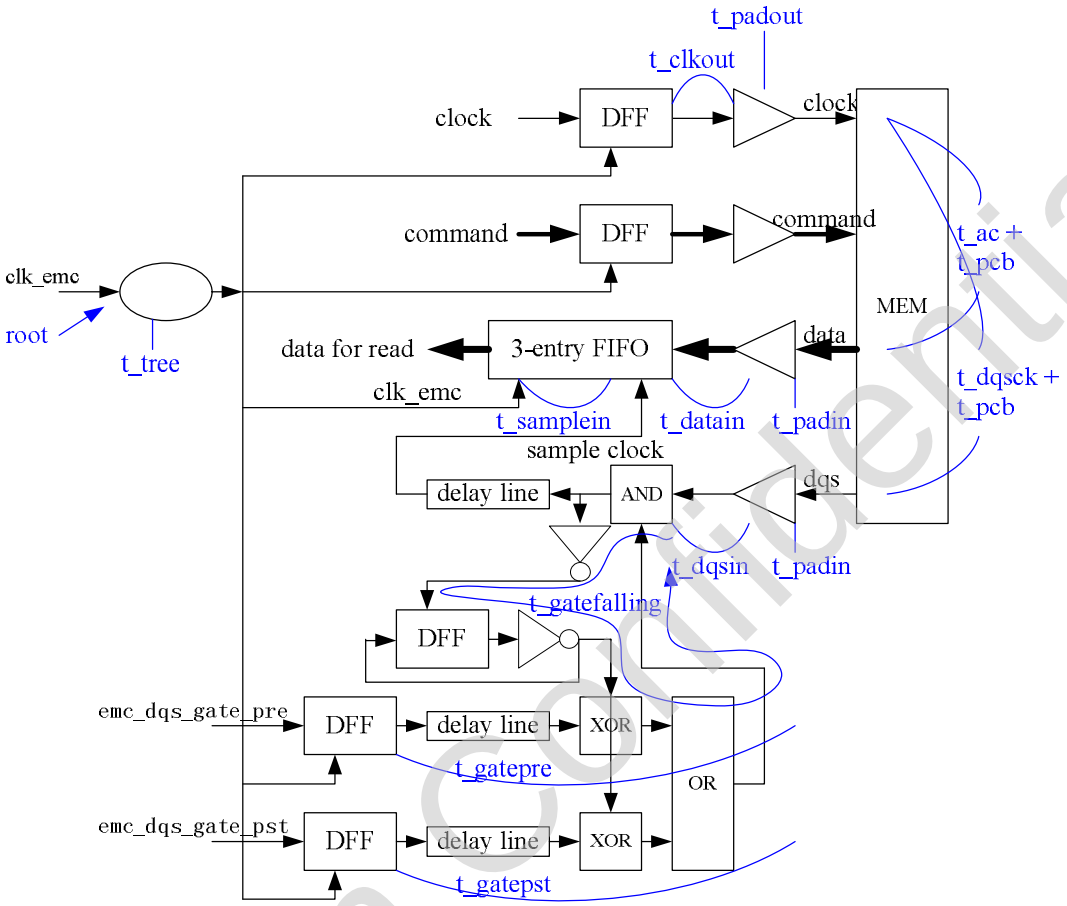


Figure 5.2-47 DDR gate circuit

DQS gating timing diagram is described as follows.

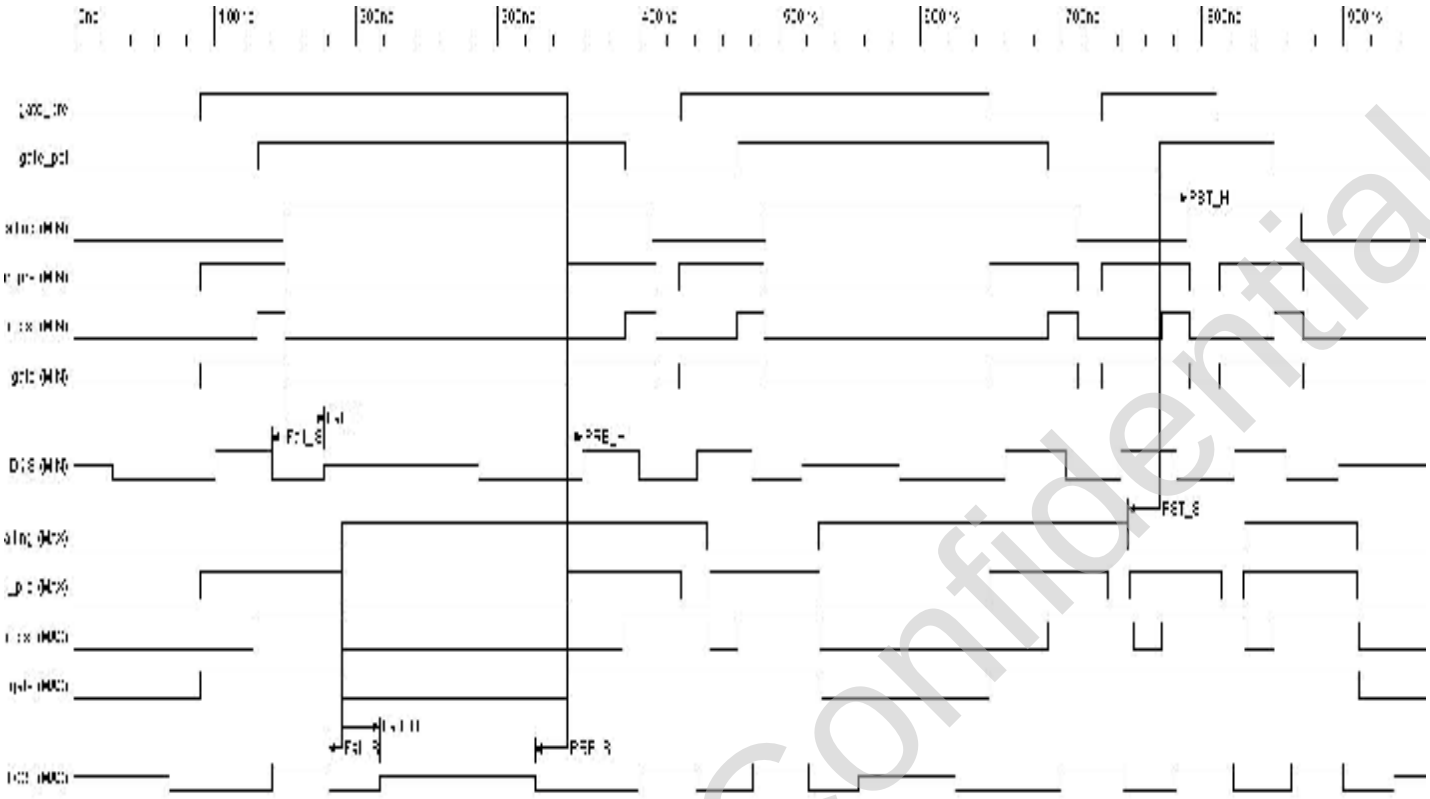


Figure 5.2-48 DDR gate timing diagram

- Gating signal falling edge delay constraint:
  Refer to Fall_S and Fall_H in above diagram
  t_gatefalling > 0
  t_gatefalling < 1 * clk_emc cycle time
  t_gatefalling < t_RPST
- DQSCK MAX guarantee from dqs_gate_pre:
  Refer to PRE_S in above diagram
  (DFF output delay + t_clkout + t_padout + t_DQSCK_MAX – t_RPRE + t_pcb + t_padin + t_dqsin) < (DFF output delay + t_gate_pre)
- DQSCK MIN guarantee from dqs_gate_pre:
  Refer to PRE_H in above diagram
  (DFF output delay + t_clkout + t_padout + t_DQSCK_MIN + t_pcb + t_padin + t_dqsin) > (DFF output delay + t_gate_pre)
- DQSCK MAX guarantee from dqs_gate_pst:
  Refer to PST_S in above diagram
  (DFF output delay + t_clkout + t_padout + t_DQSCK_MAX + t_pcb + t_padin + t_dqsin + t_gatefalling 1 * clk_emc cycle time) < (DFF output delay + t_gate_pst + 3 * clk_emc cycle time)
- DQSCK MIN guarantee from dqs_gate_pst:
  Refer to PST_H in above diagram
  (DFF output delay + t_clkout + t_padout + t_DQSCK_MIN + t_pcb + t_padin + t_dqsin + t_gatefalling 3 * clk_emc cycle time) > (DFF output delay + t_gate_pst + 3 * clk_emc cycle time)

5.2.4.8 DLL Descriptions

5.2.4.8.1 DLL Control

Memory controller includes a DLL to compensate delay line.

- **rf_dll_en**, **rf_dll_clr**, **rf_dll_init** and **rf_dll_auto_clr_en** are used to control DLL.
  If **rf_dll_clr** is set, DLL is reset and kept in idle. After system reset, **rf_dll_clr** is set.
  When **rf_dll_clr** is cleared, DLL starts to search LOCK point automatically.
  If LOCK point is found, DLL enters LOCKED state and continues to track this point.

  rf_dll_en is used to enable DLL function.

  rf_dll_init is used to configure DLL searching start value.

  During sleep, if **rf_dll_auto_clr_en** is set, DLL is reset automatically and memory controller waits for LOCKED automatically. It's recommended to set this bit.

- **rfdll_locked**, **rfdll_error** are used by software to monitor DLL status.

  rfdll_locked:
  1: DLL LOCKED
  0: DLL UNLOCKED

  rfdll_error is set if DLL error happens, and is cleared by software to write 1 to this bit. **rf_dll_err_clr** is used to clear the error bit.

5.2.4.8.2 Delay Line Control

There are twenty delay lines used in memory controller to delay clocks or control signals. All delay lines can be controlled independently.

Each delay line can be controlled in two ways.
The first is software-directly configuring.
The second is DLL-automatically compensating.

- All delay lines share a group of DLL-compensating configuration registers, **rf_dl_cpst_thr**, **rf_dl_cpst_group**, **rf_dl_cpst_en**, **rd_dl_cpst_start**, and **rfdl_cpst_st_idle**.

  rf_dl_cpst_en must be set if any delay line is compensated automatically by DLL. If all delay lines are controlled directly by software, this bit is cleared.

  rf_dl_cpst_group is DLL-compensating group mode.
  0: DMEM is hold during all clkwr_dl, dqs_in_pos_dl_x, dqs_in_neg_dl_x delay lines compensating.

1: DMEM is hold during all clkwr_dl, dqs_in_pos_dl_x, dqs_in_neg_dl_x, dqs_gate_pre_dl_x, dqs_gate_pst_dl_x delay lines compensating.

2: DMEM is hold during all clkwr_dl, dqs_in_pos_dl_x, dqs_in_neg_dl_x, dqs_gate_pre_dl_x, dqs_gate_pst_dl_x, dqs_ie_dl delay lines compensating.

3: DMEM is hold only during all delay lines compensating.

rf_dl_cpst_thr is threshold to start one compensation. That is, only if the DLL change value from last compensation is more than threshold, a new compensation is started. This value is used to prevent delay lines from compensating too frequently.

rf_dl_cpst_start is used to start DLL-compensating.

rfdl_cpst_st_idle is an indicator of compensation state machine idle.

- Each delay line has a separate group of configuration registers, **rf_xxx_dl_sel**, **rf_xxx_dl_inv**, **rfdl_xxx_cnt**, and **rf_xxx_cpst_en**.

  rf_xxx_cpst_en is used to select control modes.

  1: related delay line is compensated by DLL.

  0: related delay line can be configured only by software.

  rf_xxx_dl_sel has different functions in different configuring ways.

  If **rf_xxx_cpst_en** is set, this value means delay phase.

  Otherwise, it means delay line number.

  rf_xxx_dl_inv provides an inverting option for signal through delay line.

  rfdl_xxx_cnt is a read-back delay line value.

- Configuring flow is described as follows

  For **Software-directly control:**

  Related **rf_xxx_cpst_en** should be cleared.

  rf_xxx_sel is configured to new delay line number.

  For **DLL-automatically compensating:**

  rf_dll_en is set, **rf_dl_cpst_group** and **rf_dl_cpst_thr** are configured firstly.

  rf_xxx_sel is counted and configured.

  Then related **rf_xxx_cpst_en** is set.

  At last, **rf_dl_cpst_en** is set.

5.2.5 Control Registers

5.2.5.1 Memory map

ARM base address: 0x2000_0000

General Control Registers:

Offset Address	Name	Description
0x0000	EMC_CFG0	EMC general control register
0x0004	EMC_CFG1	EMC PHY control register
0x0008 – 0x000C	Reserved	
0x0010	EMC_CFG0_CS0	EMC CS0 device configuration register
0x0014	EMC_CFG0_CS1	EMC CS1 device configuration register
0x0018 – 0x001C	Reserved	
0x0020	EMC_CFG0_ACH0	EMC AXI channel 0 configuration register
0x0024	EMC_CFG1_ACH0	EMC AXI channel 0 configuration register
0x0028	EMC_CFG0_ACH1	EMC AXI channel 1 configuration register
0x002C	EMC_CFG1_ACH1	EMC AXI channel 1 configuration register
0x0030	EMC_CFG0_HCH2	EMC AHB channel 2 configuration register
0x0034	EMC_CFG1_HCH2	EMC AHB channel 2 configuration register
0x0038	EMC_CFG0_HCH3	EMC AHB channel 2 configuration register
0x003C	EMC_CFG1_HCH3	EMC AHB channel 3 configuration register
0x0040	EMC_CFG0_HCH4	EMC AHB channel 4 configuration register
0x0044	EMC_CFG1_HCH4	EMC AHB channel 4 configuration register
0x0048	EMC_CFG0_HCH5	EMC AHB channel 5 configuration register
0x004C	EMC_CFG1_HCH5	EMC AHB channel 5 configuration register
0x0050	EMC_CFG0_HCH6	EMC AHB channel 6 configuration register
0x0054	EMC_CFG1_HCH6	EMC AHB channel 6 configuration register
0x0058	EMC_CFG0_HCH7	EMC AHB channel 7 configuration register
0x005C	EMC_CFG1_HCH7	EMC AHB channel 7 configuration register
0x0060	EMC_CFG0_HCH8	EMC AHB channel 8 configuration register
0x0064	EMC_CFG1_HCH8	EMC AHB channel 8 configuration register
0x0068 – 0x009C	Reserved	
0x00A0	EMC_STS0	EMC status
0x00A4	EMC_STS1	EMC status
0x00A8	EMC_STS2	EMC status
0x00AC	EMC_STS3	EMC status
0x00B0 – 0x00BC	Reserved	
0x00C0	EMC_STS0_ACH0	EMC AXI channel 0 status
0x00C4	EMC_STS0_ACH1	EMC AXI channel 1 status

0x00C8	EMC_STS0_HCH2	EMC AHB channel 2 status
0x00CC	EMC_STS0_HCH3	EMC AHB channel 3 status
0x00D0	EMC_STS0_HCH4	EMC AHB channel 4 status
0x00D4	EMC_STS0_HCH5	EMC AHB channel 5 status
0x00D8	EMC_STS0_HCH6	EMC AHB channel 6 status
0x00DC	EMC_STS0_HCH7	EMC AHB channel 7 status
0x00E0	EMC_STS0_HCH8	EMC AHB channel 8 status
0x00E4 – 0x00FC	Reserved	

Delay Line Control Registers:

Offset Address	Name	Description
0x0100	EMC_DMEM_DL0	EMC delay line control register for clkdmem_out_dl
0x0104	EMC_DMEM_DL1	EMC delay line control register for dqs_ie_dl
0x0108	EMC_DMEM_DL2	EMC delay line control register for dqs_out_dl
0x010C	EMC_DMEM_DL3	EMC delay line control register for clkwr_dl
0x0110	EMC_DMEM_DL4	EMC delay line control register for dqs_gate_pre_dl_0
0x0114	EMC_DMEM_DL5	EMC delay line control register for dqs_gate_pre_dl_1
0x0118	EMC_DMEM_DL6	EMC delay line control register for dqs_gate_pre_dl_2
0x011C	EMC_DMEM_DL7	EMC delay line control register for dqs_gate_pre_dl_3
0x0120	EMC_DMEM_DL8	EMC delay line control register for dqs_gate_pst_dl_0
0x0124	EMC_DMEM_DL9	EMC delay line control register for dqs_gate_pst_dl_1
0x0128	EMC_DMEM_DL10	EMC delay line control register for dqs_gate_pst_dl_2
0x012C	EMC_DMEM_DL11	EMC delay line control register for dqs_gate_pst_dl_3
0x0130	EMC_DMEM_DL12	EMC delay line control register for dqs_in_pos_dl_0
0x0134	EMC_DMEM_DL13	EMC delay line control register for dqs_in_pos_dl_1

0x0138	EMC_DMEM_DL14	EMC delay line control register for dqs_in_pos_dl_2
0x013C	EMC_DMEM_DL15	EMC delay line control register for dqs_in_pos_dl_3
0x0140	EMC_DMEM_DL16	EMC delay line control register for dqs_in_neg_dl_0
0x0144	EMC_DMEM_DL17	EMC delay line control register for dqs_in_neg_dl_1
0x0148	EMC_DMEM_DL18	EMC delay line control register for dqs_in_neg_dl_2
0x014C	EMC_DMEM_DL19	EMC delay line control register for dqs_in_neg_dl_3
0x0150 – 0x016C	Reserved	
0x0170	EMC_CFG0_DLL	EMC DLL configuration register
0x0174	EMC_STS0_DLL	EMC DLL status
0x0178 – 0x017C	Reserved	

DMEM Control Registers:

Offset Address	Name	Description
0x0180	EMC_DCFG0	EMC DMEM control registers
0x0184	EMC_DCFG1	EMC DMEM control registers
0x0188	EMC_DCFG2	EMC DMEM control registers
0x018C	EMC_DCFG3	EMC DMEM control registers
0x0190	EMC_DCFG4	EMC DMEM control registers
0x0194	EMC_DCFG5	EMC DMEM control registers
0x0198	EMC_DCFG6	EMC DMEM control registers
0x019C	EMC_DCFG7	EMC DMEM control registers
0x01A0	EMC_DCFG8	EMC DMEM control registers
0x01A4 – 0x01FC	Reserved	

5.2.5.2 Register Descriptions

5.2.5.2.1 EMC_CFG0

Description: EMC general control register

This register is EMC general control register, shared by all external memories.

0x0000			EMC general control register (Reset 0x00000C45)													EMC_CFG0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	rf_lock_b	rf_lock_a	Reserved						rf_req_timeout_unit							
Type	RW	RW	RO						RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		rf_req_timeout_en	rf_dvc_endian	rf_auto_gate_en	rf_auto_sleep_en	Reserved		rf_cmd_queue_mode		Reserved	rf_cs_mode		rf_cs_position		
Type	RO		RW	RW	RW	RW	RO		RW		RO	RW		RW		
Reset	0	0	0	0	1	1	0	0	0	1	0	0	0	1	1	0

Field Name	Bit	Type	Reset Value	Description
rf_lock_b	[31]	R/W	1'h0	This field provides a semaphore for two independent CPUs. Semaphore signal with rf_lock_a
rf_lock_a	[30]	R/W	1'h0	This field provides a semaphore for two independent CPUs. Semaphore signal with rf_lock_b
	[29:24]	RO	0	Reserved
rf_req_timeout_unit	[23:16]	R/W	8'h0	
	[15:14]	RO	0	Reserved
rf_req_timeout_en	[13]	R/W	1'h0	This field enables request timeout functionality 0: request timeout is disabled 1: request timeout is enabled
rf_dvc_endian	[12]	R/W	1'h0	This field indicates external memory data endian format. 0: little-endian 1: big-endian This bit is only used to select external memory organizing format, not indicates bus endian and software endian. That is, software can execute correctly even if this bit is different with software

Field Name	Bit	Type	Reset Value	Description
				system endian. This bit is recommended to be configured as the same as ARM system endian.
rf_auto_gate_en	[11]	R/W	1'h1	This field enables auto-gate mode for power saving. 0: auto-gate mode is disabled 1: auto-gate mode is enabled This bit is recommended to be set.
rf_auto_sleep_en	[10]	R/W	1'h1	This field enables auto-sleep mode 0: automatically sleep mode is disabled, and software should make EMC sleep and wakeup manually 1: automatically sleep mode is enabled, and EMC can enter sleep by itself This bit is recommended to be set.
	[9:8]	RO	0	Reserved
rf_cmd_queue_mode	[7:6]	R/W	2'h1	This field select command queue operating mode. 0: 2-stage device burst 1: 2-stage device burst and 1-stage channel burst 2: 2-stage device burst and 2-stage channel burst 3: reserved In normal cases, mode-1 is better to balance performance and delay.
	[5]	RO	0	Reserved
rf_cs_mode	[4:3]	R/W	2'h0	This field selects the modes to merge CS to enlarge one CS space. Bit[0]: if set, the address space of CS0 and CS1 are merged to CS0 Bit[1]: if set, the address space of CS0 and CS1 are merged to CS1
rf_cs_position	[2:0]	R/W	3'h5	This field indicates one software address range is mapped to which external memory. 0: CS mapping to HADDR[22] 1: CS mapping to HADDR[23] 2: CS mapping to HADDR[24] 3: CS mapping to HADDR[25] 4: CS mapping to HADDR[26]

Field Name	Bit	Type	Reset Value	Description
				5: CS mapping to HADDR[27] 6: CS mapping to HADDR[28] 7: CS mapping to HADDR[29] Note: HADDR is software address.

5.2.5.2.2 EMC_CFG1

Description: EMC PHY control register

This register is EMC PHY control register, shared by all external memories.

0x0004	EMC PHY control register (Reset 0x00000000)	EMC_CFG1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0			0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	rf_cke_sel		Reserved				rf_phy_dqs_gate_loop_sel		rf_phy_dqs_gate_sel	rf_phy_data_out_sel	rf_phy_dqs_out_sel	rf_phy_dqs_ie_sel	rf_phy_clkdmem_in_sel	rf_phy_clkdmem_out_sel	rf_phy_clkdmem_loop_sel	rf_ddr_mode_en
Type	RW		RO				RW		RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	0	Reserved
rf_cke_sel	[15:14]	R/W	2'h0	This field selects DMEM CKE PAD output mode. 0: DMEM CKE output mode 0 (normal mode for only CS[0] used) CKE mapping for CS[0], mode 0 is used when only one DMEM on CS 0. 1: DMEM CKE output mode 1 (special mode for CS[1] used) CKE mapping for CS[1], mode 1 is used when only one DMEM on CS[1]. 2: DMEM CKE output mode 2 (special mode for CS[1] used) CKE mapping for all CSs, mode 2 is used when more

Field Name	Bit	Type	Reset Value	Description
				than one DMEM on bus. 3: reserved In normal cases, only one CKE is output to save PAD number, even if more than one DMEM are connected on bus. All DMEM share one CKE, so above options are provided for this sharing.
	[13:10]	RO	0	Reserved
rf_phy_dqs_gate_loop_sel	[9:8]	R/W	2'h0	This filed select DMEM DDR DQS gate signal loop back mode 0: DMEM DQS gate has only delay line delay 1: DMEM DQS gate has delay line delay and loop back delay 2, 3: DMEM DQS gate has only loop back delay
rf_phy_dqs_gate_sel	[7]	R/W	1'h0	This filed select DMEM DDR DQS gate signal mode. 0: DMEM DQS gate generating mode 0 (normal mode) 1: DMEM DQS gate generating mode 1 (debug mode) In normal cases, if the maximum frequency targets to about 200MHz or above, mode-0 is recommended to cover MIN tDQSCK and MAX tDQSCK . If the maximum frequency is less than 160MHz, both modes works.
rf_phy_data_out_sel	[6]	R/W	1'h0	This filed select DMEM data output mode. 0: DMEM data directly DFF output 1: DMEM data delay line controlled output In normal cases, mode-0 is recommended for SDR, and mode-1 is recommended for DDR.
rf_phy_dqs_out_sel	[5]	R/W	1'h0	This field selects DMEM DDR DQS output mode. 0: DMEM DQS[3:0] output is DFF output. 1: DMEM DQS[3:0] output is delay line output
rf_phy_dqs_ie_sel	[4]	R/W	1'h0	This field selects DMEM DDR DQS PAD IE mode. 0: DMEM EMDQS[3:0] pad input enable signal is from DFF output. 1: DMEM EMDQS[3:0] pad input enable signal is from delay line output
rf_phy_clkdmem_in_sel	[3]	R/W	1'h0	This field selects DMEM sample clock mode.

Field Name	Bit	Type	Reset Value	Description
				0: DMEM sample clock is from internal logic 1: DMEM sample clock is from out-of-chip (EMDQS[3:0] pad input) This field is only used by SDR to generate sample clock. For DDR, sample clock is from DQS.
rf_phy_clkdmem_out_sel	[2]	R/W	1'h0	This field selects DMEM output clock mode. 0: DMEM CK/CK# output is DFF output 1: DMEM CK/CK# output is delay line output This field is used for both SDR and DDR, and mode-0 is recommended for them.
rf_phy_clkdmem_loop_sel	[1]	R/W	1'h0	This field selects DMEM clock loopback mode. 0: DMEM READ strobe clock loopback disable 1: DMEM READ strobe clock loopback enable This field is only used for SDR
rf_ddr_mode_en	[0]	R/W	1'h0	This field enables DDR mode for DMEM. 0: SDR-SDRAM mode for DMEM 1: DDR-SDRAM mode for DMEM

5.2.5.2.3 EMC_CFG0_CSx

Description: EMC CSx device configuration register

This register is used to configure device information on CSx for DMEM.

Each CS has an independent registers.

0x0010 0x0014			EMC CS0 device configuration register (Reset 0x00000113) EMC CS1 device configuration register (Reset 0x00000113)										EMC_CFG0_CS0 EMC_CFG0_CS1			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved					rf_dburst_wlength_csx			Reserved	rf_dburst_rlength_csx			Reserved		rf_hburst_wen_csx	rf_hburst_ren_csx
Type	RO					RW			RO	RW			RO		RW	RW
Reset	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:11]	RO	0	Reserved
rf_dburst_wlength_csx	[10:8]	R/W	3'h1	This field indicates external device writing burst length 0: burst of 1 32-bit (NOT supported on 32-bit DDR) 1: burst of 2 32-bit 2: burst of 4 32-bit 3: burst of 8 32-bit 4: burst of 16 32-bit 5: reserved 6: reserved 7: reserved For DMEM, this field indicates device burst length for writing operation.
	[7]	RO	0	Reserved
rf_dburst_rlength_csx	[6:4]	R/W	3'h1	This field indicates external device reading burst length 0: burst of 1 32-bit (NOT supported on 32-bit DDR) 1: burst of 2 32-bit 2: burst of 4 32-bit 3: burst of 8 32-bit 4: burst of 16 32-bit 5: reserved 6: reserved 7: reserved For DMEM, this field indicates device burst length for reading operation.

Field Name	Bit	Type	Reset Value	Description
	[3:2]	RO	0	Reserved
rf_hburst_wen_csx	[1]	R/W	1'h1	This filed indicates AHB write operations mode 0: one AHB burst is divided into several single accesses 1: burst access This bit is cleared only if SW issues commands on pSRAM or NOR-Flash. Otherwise, it should be set to improve efficiency.
rf_hburst_ren_csx	[0]	R/W	1'h1	This filed indicates AHB read operations mode 0: one AHB burst is divided into several single accesses 1: burst access This bit is cleared only if SW issues commands on pSRAM or NOR-Flash. Otherwise, it should be set to improve efficiency.

5.2.5.2.4 EMC_CFG0_ACHx

Description: EMC AXI channel x configuration register
This register is used to configure AXI channel x information.
Each AXI channel has an independent registers.

0x0020 0x0028	EMC AXI CH0 configuration register (Reset 0x0000007C) EMC AXI CH1 configuration register (Reset 0x0000007C)	EMC_CFG0_ACH0 EMC_CFG0_ACH1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved						rf_address_offset_chx									
Type	RO						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rf_req_timeout_en_wr_chx	rf_req_timeout_thr_wr_chx							rf_auto_sleep_en_chx	rf_ch_en_chx	rf_endian_swt_chx		rf_req_level_wr_chx		rf_pri_wr_chx	
Type	RW	RW							RW	RW	RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0

Field Name	Bit	Type	Reset Value	Description

Field Name	Bit	Type	Reset Value	Description
	[31:11]	RO	0	Reserved
rf_address_offset_chx	[25:16]	R/W	10'h0	
rf_req_timeout_en_wr_chx	[15]	R/W	1'h0	This field enables request timeout function for each axi write channel
rf_req_timeout_thr_wr_chx	[14:8]	R/W	7'0	This field is used to set request timeout threshold value for each axi write channel.
rf_auto_sleep_en_chx	[7]	R/W	1'h0	This field enables auto-sleep mode for each channel 0: automatically sleep mode is disabled, and software should make the channel sleep and wakeup manually 1: automatically sleep mode is enabled, and the channel can enter sleep by itself This bit is recommended to be set.
rf_ch_en_chx	[6]	R/W	1'h1	This field enables the channel. 0: the channel is disabled 1: the channel is enabled
rf_endian_swt_chx	[5:4]	R/W	2'h3	This field selects switching mode for data endian Endian switching mode 0: byte switch 1: half switch 2: word switch (only for 64-bit AHB interface) 3: no switch Data endian switching function is provided for software in different endian domain. Data endian is different with AHB protocol endian, AHB endian is handled by hardware automatically. But data endian should be configured according to software requirement.
rf_req_level_wr_chx	[3:2]	R/W	2'h3	This field indicates the write command request level in AXI channel. The higher the level, the better the performance of AXI channel. 0 is the lowest priority and 3 is the highest priority
rf_pri_wr_chx	[1:0]	R/W	2'h0	This field indicates write channel priority. 0 is the lowest priority and 3 is the highest priority

5.2.5.2.5 EMC_CFG1_ACHx

Description: EMC AXI channel x configuration register

This register is used to configure AXI channel x information.

Each AXI channel has an independent registers.

0x0024 0x002C			EMC AXI CH0 configuration register (Reset 0x0000000C) EMC AXI CH1 configuration register (Reset 0x0000000C)										EMC_CFG1_ACH0 EMC_CFG1_ACH1			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	rf_req_timeout_en_rd_chx	rf_req_timeout_thr_rd_chx							Reserved	rf_bresp_mode_chx	rf_fifo_clr_chx	rf_sync_sel_chx	rf_req_level_rd_chx		rf_pri_rd_chx	
Type	RW	RW							RO	RW	RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	0	Reserved
rf_req_timeout_en_rd_chx	[15]	R/W	1'h0	This field enables request timeout function for each axi read channel
rf_req_timeout_thr_rd_chx	[14:8]	R/W	7'h0	This field is used to set request timeout threshold value for each axi read channel.
	[7]	RO	0	Reserved
rf_bresp_mode_ch	[6]	R/W	0	This filed indicates which mode is selected on issuing write response channel signals. 0: After WLAST signal 1: After the time data really write to DRAM
rf_fifo_clr_ch	[5]	R/W	0	This field is used to clear all FIFOs within this channel, when write 1 to this bit
rf_sync_sel_chx	[4]	R/W	1'h0	This field indicates the AXI clock for this channel is asynchronous with EMC clock or synchronous with EMC clock. 0: Asynchronous 1: Synchronous All channels can be configured to asynchronous mode, but only some of them can be configured to synchronous mode. Please refer to chip architecture document and clock document for synchronous clock group information.
rf_req_level_rd	[3:2]	R/W	2'h3	This field indicates the read command request level in

Field Name	Bit	Type	Reset Value	Description
_chx				AXI channel. The higher the level, the better the performance of AXI channel.
rf_pri_rd_chx	[1:0]	R/W	2'h0	This field indicates read channel priority. 0 is the lowest priority and 3 is the highest priority

5.2.5.2.6 EMC_CFG0_HCHx

Description: EMC AHB channel x configuration register

This register is used to configure AHB channel x information.

Each AHB channel has an independent registers.

0x0030	EMC AHB CH2 configuration register (Reset 0x0001C31C)	EMC_CFG0_HCH2
0x0038	EMC AHB CH3 configuration register (Reset 0x0001C31C)	EMC_CFG0_HCH3
0x0040	EMC AHB CH4 configuration register (Reset 0x0001C31C)	EMC_CFG0_HCH4
0x0048	EMC AHB CH5 configuration register (Reset 0x0001C31C)	EMC_CFG0_HCH5
0x0050	EMC AHB CH6 configuration register (Reset 0x0001C31C)	EMC_CFG0_HCH6
0x0058	EMC AHB CH7 configuration register (Reset 0x0001C31C)	EMC_CFG0_HCH7
0x0060	EMC AHB CH8 configuration register (Reset 0x0001C31C)	EMC_CFG0_HCH8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved														rf_auto_sleep_en_chx	rf_ch_en_chx
Type	RO														RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rf_rbuf_mode_chx	rf_wbuf_mode_chx	rf_sync_sel_chx	rf_hburst_timeout_en_chx	Reserved	rf_hburst_wlength_incr_chx			Reserved	rf_hburst_rlength_incr_chx			rf_endian_swt_chx		rf_pri_chx	
Type	RW	RW	RW	RW	RO	RW			RO	RW			RW		RW	
Reset	1	1	0	0	0	0	1	1	0	0	0	1	1	1	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:18]	RO	0	Reserved
rf_auto_sleep_en_chx	[17]	R/W	1'h0	This field enables auto-sleep mode for each channel 0: automatically sleep mode is disabled, and software should make the channel sleep and wakeup manually 1: automatically sleep mode is enabled, and the

Field Name	Bit	Type	Reset Value	Description
				channel can enter sleep by itself This bit is recommended to be set.
rf_ch_en_chx	[16]	R/W	1'h1	This field enables the channel. 0: the channel is disabled 1: the channel is enabled
rf_rbuf_mode_chx	[15]	R/W	1'h1	This filed indicates which operation mode is selected on read bursts. 0: Single operation mode 1: Pipeline operation mode Pipeline operation can achieve better write performance, so this mode is preferred in normal case.
rf_wbuf_mode_chx	[14]	R/W	1'h1	This filed indicates single-buffer or double-buffer is used on write bursts, and also indicates which operation mode is selected 0: Single buffer and single operation mode 1: Double buffer and pipeline operation mode Double buffer and pipeline mode can achieve better write performance, so this mode is preferred in normal case, especially for mass data transfers. Single buffer is used in some special cases, mainly for CPU, because: - double-buffer may lead to larger latency between CPU transfer done and external memory transfer done - double-buffer may lead to larger wait time for consecutive read operation.
rf_sync_sel_chx	[13]	R/W	1'h0	This field indicates the AHB clock for this channel is asynchronous with EMC clock or synchronous with EMC clock. 0: Asynchronous 1: Synchronous All channels can be configured to asynchronous mode, but only some of them can be configured to synchronous mode. Please refer to chip architecture document and clock document for synchronous clock group information.
rf_hburst_timeout_en_chx	[12]	R/W	1'h0	This field enable a timeout engine for debugging. This timeout engine is only used for AHB read operations. And in normal using, this be should be kept low.

Field Name	Bit	Type	Reset Value	Description
	[11]	RO	0	Reserved
rf_hburst_wlength_incr_chx	[10:8]	R/W	3'h3	This filed indicates how to divide AHB INCR writing burst. If a AHB write burst is INCR and HLENGTH is 0, the AHB burst is divided into several sub-bursts, and the sub-burst length is defined by this register. 0: 2 32-bit 1: 4 32-bit 2: 6 32-bit 3: 8 32-bit 4: 10 32-bit 5: 12 32-bit 6: 14 32-bit 7: 16 32-bit
	[7]	RO	0	Reserved
rf_hburst_rlength_incr_chx	[6:4]	R/W	3'h1	This filed indicates how to divide AHB INCR reading burst. If a AHB read burst is INCR and HLENGTH is 0, the AHB burst is divided into several sub-bursts, and the sub-burst length is defined by this register. 0: 2 32-bit 1: 4 32-bit 2: 6 32-bit 3: 8 32-bit 4: 10 32-bit 5: 12 32-bit 6: 14 32-bit 7: 16 32-bit
rf_endian_swt_chx	[3:2]	R/W	2'h3	This field selects switching mode for data endian Endian switching mode 0: byte switch 1: half switch 2: word switch (only for 64-bit AHB interface) 3: no switch Data endian switching function is provided for software in different endian domain. Data endian is different with AHB protocol endian, AHB endian is handled by hardware automatically. But data endian should be configured according to software requirement.
rf_pri_chx	[1:0]	R/W	2'h0	This field indicates channel priority.

Field Name	Bit	Type	Reset Value	Description
				0 is the lowest priority and 3 is the highest priority

5.2.5.2.7 EMC_CFG1_HCHx

Description: EMC AHB channel x configuration register

This register is used to configure AHB channel x information.

Each AHB channel has an independent registers.

0x0034 0x003C 0x0044 0x004C 0x0054 0x005C 0x0064	EMC AHB CH2 configuration register (Reset 0x00000000) EMC AHB CH3 configuration register (Reset 0x00000000) EMC AHB CH4 configuration register (Reset 0x00000000) EMC AHB CH5 configuration register (Reset 0x00000000) EMC AHB CH6 configuration register (Reset 0x00000000) EMC AHB CH7 configuration register (Reset 0x00000000) EMC AHB CH8 configuration register (Reset 0x00000000)															EMC_CFG1_HCH2 EMC_CFG1_HCH3 EMC_CFG1_HCH4 EMC_CFG1_HCH5 EMC_CFG1_HCH6 EMC_CFG1_HCH7 EMC_CFG1_HCH8
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**210**	**20**	**19**	**18**	**17**	**16**
Name	Reserved						rf_address_offset_chx									
Type	RO						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								rf_req_timeout_en_chx	rf_req_timeout_thr_chx						
Type	RO								RW	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:26]	RO	0	Reserved
rf_address_offset_chx	[25:16]	R/W	10'h0	
	[15:8]	RO	0	Reserved
rf_req_timeout_en	[7]	R/W	1'h0	This field enables request timeout function for each channel
rf_req_timeout_thr_chx	[6:0]	R/W	7'h0	This field is used to set request timeout threshold value for each channel.

5.2.5.2.8 EMC_STS3

Description: EMC status

This register indicates EMC status.

0x00AC			EMC status (Reset 0x8007FFFF)											EMC_STS3		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	rfemc_idle_sync	Reserved												rfdl_cpst_idle_sync	rfdmem_idle_sync	rfsel_idle_sync
Type	RO	RO												RO	RO	RO
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	rfahb_idle_ch15_sync	rfahb_idle_ch14_sync	rfahb_idle_ch13_sync	rfahb_idle_ch12_sync	rfahb_idle_ch11_sync	rfahb_idle_ch10_sync	rfahb_idle_ch9_sync	rfahb_idle_ch8_sync	rfahb_idle_ch7_sync	rfahb_idle_ch6_sync	rfahb_idle_ch5_sync	rfahb_idle_ch4_sync	rfahb_idle_ch3_sync	rfahb_idle_ch2_sync	rfahb_idle_ch1_sync	rfahb_idle_ch0_sync
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
rfemc_idle_sync	[31]	RO	1'h1	This bit indicates EMC is in IDLE status.
	[30:19]	RO	0	Reserved
rfdl_cpst_idle_sync	[18]	RO	1'h1	This bit indicates delay line compensation is in IDLE status.
rfdmem_idle_sync	[17]	RO	1'h1	This bit indicates DMEM is in IDLE status.
rfsel_idle_sync	[16]	RO	1'h1	This bit indicates CH MUX is in IDLE status.
rfahb_idle_ch15_sync	[15]	RO	1'h1	This bit indicates CH15 is in IDLE status.
rfahb_idle_ch14_sync	[14]	RO	1'h1	This bit indicates CH14 is in IDLE status.
rfahb_idle_ch13_sync	[13]	RO	1'h1	This bit indicates CH13 is in IDLE status.
rfahb_idle_ch12_sync	[12]	RO	1'h1	This bit indicates CH12 is in IDLE status.
rfahb_idle_ch11_sync	[11]	RO	1'h1	This bit indicates CH11 is in IDLE status.
rfahb_idle_ch10_sync	[10]	RO	1'h1	This bit indicates CH10 is in IDLE status.

Field Name	Bit	Type	Reset Value	Description
rfahb_idle_ch9_sync	[9]	RO	1'h1	This bit indicates CH9 is in IDLE status.
rfahb_idle_ch8_sync	[8]	RO	1'h1	This bit indicates CH8 is in IDLE status.
rfahb_idle_ch7_sync	[7]	RO	1'h1	This bit indicates CH7 is in IDLE status.
rfahb_idle_ch6_sync	[6]	RO	1'h1	This bit indicates CH6 is in IDLE status.
rfahb_idle_ch5_sync	[5]	RO	1'h1	This bit indicates CH5 is in IDLE status.
rfahb_idle_ch4_sync	[4]	RO	1'h1	This bit indicates CH4 is in IDLE status.
rfahb_idle_ch3_sync	[3]	RO	1'h1	This bit indicates CH3 is in IDLE status.
rfahb_idle_ch2_sync	[2]	RO	1'h1	This bit indicates CH2 is in IDLE status.
rfahb_idle_ch1_sync	[1]	RO	1'h1	This bit indicates CH1 is in IDLE status.
rfahb_idle_ch0_sync	[0]	RO	1'h1	This bit indicates CH0 is in IDLE status.

5.2.5.2.9 EMC_DMEM_DLx

Description: EMC delay line control register

These registers are used to configure the DMEM delay lines in EMC PHY.

EMC_DMEM_DL0	0x0100	clkdmem_out_dl.
EMC_DMEM_DL1	0x0104	dqs_ie_dl.
EMC_DMEM_DL2	0x0108	dqs_out_dl.
EMC_DMEM_DL3	0x010C	clkwr_dl.
EMC_DMEM_DL4	0x0110	dqs_gate_pre_dl_0.
EMC_DMEM_DL5	0x0114	dqs_gate_pre_dl_1.
EMC_DMEM_DL6	0x0118	dqs_gate_pre_dl_2.
EMC_DMEM_DL7	0x011C	dqs_gate_pre_dl_3.
EMC_DMEM_DL8	0x0120	dqs_gate_pst_dl_0.
EMC_DMEM_DL9	0x0124	dqs_gate_pst_dl_1.
EMC_DMEM_DL10	0x0128	dqs_gate_pst_dl_2.
EMC_DMEM_DL11	0x012C	dqs_gate_pst_dl_3.
EMC_DMEM_DL12	0x0130	dqs_in_pos_dl_0.
EMC_DMEM_DL13	0x0134	dqs_in_pos_dl_1.
EMC_DMEM_DL14	0x0138	dqs_in_pos_dl_2.

EMC_DMEM_DL15	0x013C	dqs_in_pos_dl_3
EMC_DMEM_DL16	0x0140	dqs_in_neg_dl_0
EMC_DMEM_DL17	0x0144	dqs_in_neg_dl_1
EMC_DMEM_DL18	0x0148	dqs_in_neg_dl_2
EMC_DMEM_DL19	0x014C	dqs_in_neg_dl_3

0x0100	**EMC delay line DL0 control register (Reset 0x00000000)**	**EMC_DMEM_DL0**
0x0104	**EMC delay line DL1 control register (Reset 0x00000000)**	**EMC_DMEM_DL1**
0x0108	**EMC delay line DL2 control register (Reset 0x00000000)**	**EMC_DMEM_DL2**
0x010C	**EMC delay line DL3 control register (Reset 0x00000000)**	**EMC_DMEM_DL3**
0x0110	**EMC delay line DL4 control register (Reset 0x00000000)**	**EMC_DMEM_DL4**
0x0114	**EMC delay line DL5 control register (Reset 0x00000000)**	**EMC_DMEM_DL5**
0x0118	**EMC delay line DL6 control register (Reset 0x00000000)**	**EMC_DMEM_DL6**
0x011C	**EMC delay line DL7 control register (Reset 0x00000000)**	**EMC_DMEM_DL7**
0x0120	**EMC delay line DL8 control register (Reset 0x00000000)**	**EMC_DMEM_DL8**
0x0124	**EMC delay line DL9 control register (Reset 0x00000000)**	**EMC_DMEM_DL9**
0x0128	**EMC delay line DL10 control register (Reset 0x00000000)**	**EMC_DMEM_DL10**
0x012C	**EMC delay line DL11 control register (Reset 0x00000000)**	**EMC_DMEM_DL11**
0x0130	**EMC delay line DL12 control register (Reset 0x00000000)**	**EMC_DMEM_DL12**
0x0134	**EMC delay line DL13 control register (Reset 0x00000000)**	**EMC_DMEM_DL13**
0x0138	**EMC delay line DL14 control register (Reset 0x00000000)**	**EMC_DMEM_DL14**
0x013C	**EMC delay line DL15 control register (Reset 0x00000000)**	**EMC_DMEM_DL15**
0x0140	**EMC delay line DL16 control register (Reset 0x00000000)**	**EMC_DMEM_DL16**
0x0144	**EMC delay line DL17 control register (Reset 0x00000000)**	**EMC_DMEM_DL17**
0x0148	**EMC delay line DL18 control register (Reset 0x00000000)**	**EMC_DMEM_DL18**
0x014C	**EMC delay line DL19 control register (Reset 0x00000000)**	**EMC_DMEM_DL19**

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	rf_xxx_cpst_en	rfdl_xxx_cnt							rf_xxx_dl_inv	rf_xxx_dl_sel						
Type	RW	RO							RW	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:6]	RO	0	Reserved
rf_xxx_cpst_en	[15]	R/W	1'h0	This field enables the delay line to be compensated automatically by DLL
rfdl_xxx_cnt	[14:8]	RO	7'h00	This field indicate the count of delay
rf_xxx_dl_inv	[7]	R/W	1'h0	This field provides an inverting option for signal through delay line. 0: no inverting 1: inverting

Field Name	Bit	Type	Reset Value	Description
rf_xxx_dl_sel	[6:0]	R/W	7'h00	This field controls delay value of delay line

5.2.5.2.10 EMC_CFG0_DLL

Description: EMC DLL configuration register

This register is used to configure DLL information.

0x0170			EMC DLL configuration register (Reset 0x00000000)													EMC_CFG0_DLL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved											rf_dll_err_clr	rf_dl_cpst_thr			
Type	RO											W	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	rfdll_error	rfdll_locked	rf_dl_cpst_group		rf_dl_cpst_start	rf_dl_cpst_en	rf_dll_auto_clr_en	rf_dll_clr	rf_dll_en	rf_dll_init						
Type	RO	RO	RW		RW	RW	RW	RW	RW	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:20]	RO	0	Reserved
rf_dll_err_clr	[20]	W	1'h0	This field is used to clear DLL error in bit[15], when write 1 to this bit
rf_dl_cpst_thr	[19:16]	R/W	4'h0	This field is the threshold to start one compensation
rfdll_error	[15]	RO	1'h0	This field is set if DLL error happens
rfdll_locked	[14]	RO	1'h0	This field indicates DLL is locked or not 1: DLL LOCKED 0: DLL UNLOCKED
rf_dl_cpst_group	[13:12]	R/W	2'h0	This field enables the group of delay lines to be compensated.
rf_dl_cpst_start	[11]	R/W	1'h0	This field is used to start one compensation.
rf_dl_cpst_en	[10]	R/W	1'h0	This field enables the DLL compensation. 0: the DLL compensation is disabled 1: the DLL compensation is enabled

Field Name	Bit	Type	Reset Value	Description
rf_dll_auto_clr_en	[9]	R/W	1'h0	This field enables automatically reset DLL
rf_dll_clr	[8]	R/W	1'h0	This field is to reset DLL
rf_dll_en	[7]	R/W	1'h0	This field enables the DLL. 0: the DLL is disabled 1: the DLL is enabled
rf_dll_init	[6:0]	R/W	7'h0	This field is used to configure DLL searching start value

5.2.5.2.11 EMC_DCFG0

Description: EMC DMEM control registers

This register is used to configure external DMEM.

0x0180	EMC DMEM control register (Reset 0x0000BF13)															EMC_DCFG0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	drf_auto_ref_allcs	drf_auto_ref_en	drf_alternative_mode1_en	drf_alternative_mode0_en	drf_clkdm_em_out_sel	drf_clkdm_em_out_en	drf_rowhit_en	drf_data_width	Reserved	drf_column_mode			drf_auto_pre_position		drf_row_mode	
Type	RW	RW	RW	RW	RW	RW	RW	RW	RO	RW			RW		RW	
Reset	1	0	1	1	1	1	1	1	0	0	0	1	0	0	1	1

Field Name	Bit	R/W	Default Value	Description
	[31:16]	RO	0	Reserved
drf_auto_ref_allcs	[15]	R/W	1'h1	This bit indicates auto-refresh mode for multi-DRAM on bus. 0: CSs are auto-refresh one by one 1: CSs are auto-refresh at the same time If there is no refresh current issues, mode-1 is recommended.

Field Name	Bit	R/W	Default Value	Description
drf_auto_ref_en	[14]	R/W	1'h0	This bit opens auto-refresh functions for both SDR and DDR. 0: hardware auto-refresh function is disabled 1: hardware auto-refresh function is enabled During device initialization or re-configuration, this bit should be cleared, and in other cases, this bit MUST be kept opened to guarantee data in device is correctly retained.
drf_alternative_mode1_en	[13]	R/W	1'h1	This bit enables alternative bank pre-charge or active during pre-charge or active 0: disabled 1: enabled This bit should be always set to improve efficiency.
drf_alternative_mode0_en	[12]	R/W	1'h1	This bit enables alternative bank pre-charge or active during access 0: disabled 1: enabled This bit should be always set to improve efficiency.
drf_clkdmem_out_sel	[11]	R/W	1'h1	This bit select DMEM output clock phase.
drf_clkdmem_out_en	[10]	R/W	1'h1	This bit enable DMEM output clock on EMCLKDP and EMCLKDM. 0: DMEM clock output is closed 1: DMEM clock output is opened
drf_rowhit_en	[9]	R/W	1'h1	This bit enables row-hit detect logic to remove redundant pre-charge and active operations. 0: row-hit detecting function is disabled 1: row-hit detecting function is enabled This bit should be always set to improve efficiency.
drf_data_width	[8]	R/W	1'h1	This bit selects device data bus width 0: 16-bit 1: 32-bit
	[7]	RO	0	Reserved
drf_column_mode	[6:4]	R/W	3'h1	This field indicates device column mode:

Field Name	Bit	R/W	Default Value	Description
				0: 8-bit 1: 9-bit 2: 10-bit 3: 11-bit 4: 12-bit 5: reserved 6: reserved 7: reserved This field should be configured according to device type.
drf_auto_pre_position	[3:2]	R/W	2'h0	This field indicates auto pre-charge and pre-charge all bank bit position. 0: A[10] 1: A[11] 2: A[12] 3: A[13] This field should be configured according to device type.
drf_row_mode	[1:0]	R/W	2'h3	This field indicates device row mode: 0: 11-bit 1: 12-bit 2: 13-bit 3: 14-bit This field should be configured according to device type.

5.2.5.2.12 EMC_DCFG1

Description: EMC DMEM control registers

This register is used to configure external DMEM.

0x0184			EMC DMEM control register (Reset 0x03382434)													EMC_DCFG1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	drf_t_rtr				drf_t_wtr				drf_t_rtw				drf_t_ras			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	drf_t_rrd				drf_t_wr				drf_t_rcd				drf_t_rp			
Type	RW				RW				RW				RW			
Reset	0	0	1	0	0	1	0	0	0	0	1	1	0	1	0	0

Field Name	Bit	Type	Reset Value	Description
drf_t_rtr	[31:28]	R/W	4'h0	Timing parameter: read-to-read turn-around time between different CSs T is clk_emc/2 cycle, that is, external memory clock cycle.
drf_t_wtr	[27:24]	R/W	4'h3	Timing parameter: write-to-read turn-around time T is clk_emc/2 cycle, that is, external memory clock cycle.
drf_t_rtw	[23:20]	R/W	4'h3	Timing parameter: read-to-write turn-around time T is clk_emc/2 cycle, that is, external memory clock cycle.
drf_t_ras	[19:16]	R/W	4'h8	Timing parameter: tRAS-MIN (drf_t_ras+1)*T >= tRAS-MIN T is clk_emc/2 cycle, that is, external memory clock cycle.
drf_t_rrd	[15:12]	R/W	4'h2	Timing parameter: tRRD (drf_t_rrd+1)*T >= tRRD T is clk_emc/2 cycle, that is, external memory clock cycle.
drf_t_wr	[11:8]	R/W	4'h4	Timing parameter: tWR For SDR, (drf_t_wr+1)*T >= tWR For DDR, (drf_t_wr -1)*T >= tWR T is clk_emc/2 cycle, that is, external memory clock cycle.
drf_t_rcd	[7:4]	R/W	4'h3	Timing parameter: tRCD (drf_t_rcd+1)*T >= tRCD T is clk_emc/2 cycle, that is, external memory clock cycle.
drf_t_rp	[3:0]	R/W	4'h4	Timing parameter: tRP (drf_t_rp+1)*T >= tRP T is clk_emc/2 cycle, that is, external memory clock cycle.

5.2.5.2.13 EMC_DCFG2

Description: EMC DMEM control registers

This register is used to configure external DMEM.

0x0188			EMC DMEM control register (Reset 0x1A261000)										EMC_DCFG2			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved		drf_t_rfc						drf_t_xsr							
Type	RO		RW						RW							
Reset	0	0	0	1	1	0	1	0	0	0	1	0	0	1	1	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	drf_t_ref												drf_t_mrd			
Type	RW												RW			
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:30]	RO	0	Reserved
drf_t_rfc	[29:24]	R/W	6'h1A	Timing parameter: tRFC (drf_t_rfc+2)*T >= tRFC T is clk_emc/2 cycle, that is, external memory clock cycle.
drf_t_xsr	[23:16]	R/W	8'h26	Timing parameter: tXSR (drf_t_xsr+2)*T >= tXSR T is clk_emc/2 cycle, that is, external memory clock cycle.
drf_t_ref	[15:4]	R/W	12'h100	Auto-refresh interval time (drf_t_ref+1)*Tref*(row number) <= tREF Tref is clk_emc_ref cycle.
drf_t_mrd	[3:0]	R/W	4'h0	Timing parameter: tMRD (drf_t_mrd+2)*T >= tMRD T is clk_emc/2 cycle, that is, external memory clock cycle.

5.2.5.2.14 EMC_DCFG3

Description: EMC DMEM control registers

This register is used to configure external DMEM.

0x018C			EMC DMEM control register (Reset 0x003FBFFF)													EMC_DCFG3
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved						drf_sample_auto_rst_en	drf_sample_rst	Reserved	drf_auto_sleep_mode	drf_auto_sleep_t_ref					
Type	RO						RW	RW	RO	RW	RW					
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	drf_ref_cnt_rst	ref_cnt_done	drf_ref_cnt_thr													
Type	RW	RO	RW													
Reset	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:26]	RO	0	Reserved
drf_sample_auto_rst_en	[25]	R/W	1'h0	This bit enables an auto-reset function for sampling logic. 0: read data FIFO cannot be reset automatically 1: read data FIFO is reset automatically during auto-refresh or resume
drf_sample_rst	[24]	R/W	1'h0	This bit is used to reset DMEM sample FIFO pointer. Active high. 0: read data FIFO is released to work 1: read data FIFO is held and reset This bit is a debugging bit, and should not be used in normal condition. Because this bit cannot be cleared automatically. To reset sample FIFO pointer, software should set this bit, and then clear this bit.
	[23]	RO	0	Reserved
drf_auto_sleep_mode	[22]	R/W	1'h0	This bit selects auto-sleep mode 0: normal mode 1: all rows are guarantee to refresh at least one time before sleep In normal cases, mode-0 is recommended and this bit is cleared to 0.

Field Name	Bit	Type	Reset Value	Description
				This bit is valid only if rf_auto_sleep_en is set.
drf_auto_sleep_t_ref	[21:16]	R/W	6'h3F	If drf_auto_sleep_mode is set to 1, this field indicates auto-refresh interval in special refresh mode before sleep. If drf_auto_sleep_mode is cleared to 0, this field is DON'T CARE.
drf_ref_cnt_rst	[15]	R/W	1'h1	This bit is used to reset and hold refresh counter. 0: refresh counter is released to count 1: refresh counter is held and reset If drf_auto_sleep_mode is cleared to 0, this bit should be kept high.
ref_cnt_done	[14]	RO	1'h0	This bit indicates refresh counter done status
drf_ref_cnt_thr	[13:0]	R/W	14'h3FFF	If drf_auto_sleep_mode is set to 1, this field is refresh counter threshold. The number should be configured to (row number – 1). If drf_auto_sleep_mode is cleared to 0, this field is DON'T CARE.

5.2.5.2.15 EMC_DCFG4

Description: EMC DMEM control registers

This register is used to configure external DMEM.

0x0190	EMC DMEM control register (Reset 0x00000000)															EMC_DCFG4
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved	dsoft_cmd_allcs	Reserved	dsoft_cs	cmd_chip_sleep		Reserved					dsoft_resume	dsoft_self_ref	dsoft_ld_mdreg	dsoft_auto_ref	dsoft_pre_all
Type	RO	RW	RO	RW	RO		RO					RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	drf_mode_reg															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31]	RO	0	Reserved
dsoft_cmd_allcs	[30]	R/W	1'h0	This bit select software command issued mode for multi-DRAM on bus.

Field Name	Bit	Type	Reset Value	Description
				If cleared, software command is issued one CS at one time, the CS number is dsoft_cs. If set, software command is issued on all CSs at the same time, and the dsoft_cs is DON'T CARE.
	[29]	RO	0	Reserved
dsoft_cs	[28]	R/W	1'h0	Only if dsoft_cmd_allcs is cleared, this register is used. 1'h0: software command is issued on CS0 1'h1: software command is issued on CS1
cmd_chip_sleep	[27:26]	RO	2'h0	Sleep status for each CS. [0]: CS0 [1]: CS1 If one CS sleeps, the related bit is set. If one CS is resumed, the related bit is cleared.
	[25:21]	RO	0	Reserved
dsoft_resume	[20]	R/W	1'h0	Software-issued EXIT SELF REFRESH (RESUME) command Write: start RESUME command Read: RESUME command status
dsoft_self_ref	[19]	R/W	1'h0	Software-issued SELF REFRESH command Write: start SELF REFRESH command Read: SELF REFRESH command status
dsoft_ld_mdreg	[18]	R/W	1'h0	Software-issued LOAD MODE REGISTER command Write: start LOAD MODE REGISTER command Read: LOAD MODE REGISTER command status
dsoft_auto_ref	[17]	R/W	1'h0	Software-issued AUTO REFRESH command Write: start AUTO REFRESH command Read: AUTO REFRESH command status
dsoft_pre_all	[16]	R/W	1'h0	Software-issued PRECHARGE ALL BANK command Write: start PRECHARGE ALL BANK command Read: PRECHARGE ALL BANK command status
drf_mode_reg	[15:0]	R/W	16'h0	SDRAM mode register. This value is loaded into SDRAM during write 1 to dsoft_ld_mdreg. And this value isn't used by controller. Bit[15:14]: mode register select (mapping to bank) Bit[13: 0]: mode register value (mapping to address)

5.2.5.2.16 EMC_DCFG5

Description: EMC DMEM control registers

This register is used to configure external DMEM.

0x0194	EMC DMEM control register (Reset 0x00620208)															EMC_DCFG5
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved								drf_clkdmem_in_sel				Reserved	drf_dqs_out_sel		
Type	RO								RW				RO	RW		
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	drf_wdm_latency			Reserved	drf_rdm_latency			Reserved	drf_wdata_latency			drf_rdata_latency			
Type	RO	RW			RO	RW			RO	RW			RW			
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:24]	RO	0	Reserved
drf_clkdmem_in_sel	[23:20]	R/W	4'h6	Timing adjustment: sample clock latency The unit is clk_emc cycle.
	[19]	RO	0	Reserved
drf_dqs_out_sel	[18:16]	R/W	3'h2	Timing adjustment: DQS output latency The unit is clk_emc cycle.
	[15]	RO	0	Reserved
drf_wdm_latency	[14:12]	R/W	3'h0	Timing adjustment: write DM latency The unit is clk_emc cycle.
	[11]	RO	0	Reserved
drf_rdm_latency	[10:8]	R/W	3'h2	Timing adjustment: read DM latency The unit is clk_emc cycle. IMPORTANT: if drf_rdm_latency is configured to 7, DM is kept high in whole read burst instead of 7-cycle-delay. This option is used for DDR because DM is DON'T CARE during read bursts.
	[7]	RO	0	Reserved
drf_wdata_latency	[6:4]	R/W	3'h0	Timing adjustment: write data latency The unit is clk_emc cycle.
drf_rdata_latency	[3:0]	R/W	4'h8	Timing adjustment: read data latency The unit is clk_emc cycle.

5.2.5.2.17 EMC_DCFG6

Description: EMC DMEM control registers

This register is used to configure external DMEM.

0x0198			EMC DMEM control register (Reset 0x00400020)										EMC_DCFG6			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	drf_dqs_gate_pst_sel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	drf_dqs_gate_pre_sel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
drf_dqs_gate_pst_sel	[31:16]	R/W	16'h40	Timing adjustment: DQS gate pst signal delay select The unit is clk_emc cycle.
drf_dqs_gate_pre_sel	[15:0]	R/W	16'h20	Timing adjustment: DQS gate pre signal delay select The unit is clk_emc cycle.

5.2.5.2.18 EMC_DCFG7

Description: EMC DMEM control registers

This register is used to configure external DMEM.

0x019C			EMC DMEM control register (Reset 0x00F0000E)										EMC_DCFG7			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	drf_dqs_ie_sel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								drf_dqs_oe_sel							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Field Name	Bit	Type	Reset Value	Description
drf_dqs_ie_sel	[31:16]	R/W	16'hF0	Timing adjustment: DQS PAD IE signal delay select The unit is clk_emc cycle.
	[15:8]	RO	0	Reserved
drf_dqs_oe_sel	[7:0]	R/W	8'h0E	Timing adjustment: DQS PAD OE signal delay select The unit is clk_emc cycle.

5.2.5.2.19 EMC_DCFG8

Description: EMC DMEM control registers

This register is used to configure external DMEM.

0x01A0	EMC DMEM control register (Reset 0x00400001)															EMC_DCFG8
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	drf_data_ie_sel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								drf_data_oe_sel							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Field Name	Bit	Type	Reset Value	Description
drf_data_ie_sel	[31:16]	R/W	16'h40	Timing adjustment: data PAD IE signal delay select The unit is clk_emc cycle.
	[15:8]	RO	0	Reserved
drf_data_oe_sel	[7:0]	R/W	8'h01	Timing adjustment: data PAD OE signal delay select The unit is clk_emc cycle.

5.2.6 Application Notes

5.2.6.1 Application Notes

5.2.6.1.1 16-Bit SDR-SDRAM Configuration 1

Condition:

- CAS Latency is 2
- Burst Length is 2 16-bit
- DLL OFF

Configure EMC:

(Suppose SDR-SDRAM is connected on CS0)

- 0x0000 -- 0x00000C45 (Default)
- 0x0004 -- 0x00000002 (Default)
- 0x0010 -- 0x00000003
- 0x0020 -- 0x000000FC (Default)
- 0x0024 -- 0x0000000C + (rf_sync_sel_ch0<<4)

…

- 0x0030 -- 0x0003C31C + (rf_sync_sel_ch2<<13)
- 0x0034 -- 0x00000000 (Default)

…

- 0x0180 -- 0x0000BE00 + (drf_row_mode<<0)
  + (drf_column_mode<<4)
- 0x0184 -- 0x00000000 + (drf_t_rp<<0)
  + (drf_t_rcd<<4)
  + (drf_t_wr<<8)
  + (drf_t_rrd<<12)
  + (drf_t_ras<<16)
  + (drf_t_rtw<<20)
  + (drf_t_wtr<<24)
  + (drf_t_rtr<<28)
- 0x0188 -- 0x00000000 + (drf_t_wrd<<0)
  + (drf_t_ref<<4)
  + (drf_t_xsr<<16)
  + (drf_t_rfc<<24)
- 0x0194 -- 0x00400007
- 0x01A0 -- 0x00100001

Initialize external memory after configuring EMC:

- 0x0190 -- 0x40010000
- Wait until bit-16 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_ext_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared

Open auto-refresh after initializing external memory:

- Set 1 to bit 14 of 0x0180

Description:

- rf_sync_sel_chx: if the HCLK of this channel is synchronous with clk_emc, this bit can be set to improve performance.

- drf_row_mode: row address bit select. See memory device specifications for this information.
- drf_column_mode: column address bit select. See memory device specifications for this information.
- drf_t_ref: Maximum Refresh period (or tREF).

  (drf_t_ref+1)*T_cycle*(row number) <= tREF. T_cycle is clk_emc_ref cycle time.

  It's important that clk_emc_ref is different with clk_emc. Normally, clk_emc_ref is a fixed-frequency clock with low frequency.
- drf_t_rfc: Minimum AUTO-REFRESH period (or tRFC).

  (drf_t_rfc+2)*T_cycle >= tRFC.
- drf_t_rp: Minimum PRECHARGE command period time (or tRP).

  (drf_t_rp+1)*T_cycle >= tRP.
- drf_t_rcd: Minimum ACTIVE to READ or WRITE delay (or minimum RAS to CAS delay, or tRCD).

  (drf_t_rcd+1)*T_cycle >= tRCD.
- drf_t_rrd: Minimum ACTIVE to ACTIVE (in different bank) time (or tRRD).

  (drf_t_rrd+1)*T_cycle >= tRRD.
- drf_t_wr: Minimum Write recovery time (or minimum last data-in to PRECHARGE time, or tWR, or tDPL, or tRDL).

  (drf_t_wr+1)*T_cycle >= tWR.
- drf_t_xsr: Minimum SELF-REFRESH time (tRAS for Micron, Samsung, etc).

  (drf_t_xsr+1)*T_cyle >= this minimum time.
- drf_t_ras: Minimum ACTIVE to PRECHARGE time (or minimum row active time, or tRAS-MIN).

  (drf_t_ras+1)*T_cyle >= tRAS-MIN.
- drf_t_mrd: Minimum LOAD MODE REGISTER to ACTIVE or REFRESH delay (or tMRD).

  (drf_t_mrd+2)*T_cycle >= tMRD.
- drf_mode_reg: Mode Register. drf_mode_reg[13:0] is mapped to A[13:0] and drf_mode_reg[15:14] is mapped to BA[1:0]. It's IMPORTANT that CAS Latency MUST be configured to 2 and Burst Length MUST be configured to 2 16-bit.
- drf_ext_mode_reg: Extended Mode Register

5.2.6.1.2 16-Bit SDR-SDRAM Configuration 2

Condition:

- CAS Latency is 3
- Burst Length is 2 16-bit

Configure EMC:

(Suppose SDR-SDRAM is connected on CS0)

- 0x0000 -- 0x00000C45 (Default)
- 0x0004 -- 0x00000002 (Default)
- 0x0010 -- 0x00000003
- 0x0020 -- 0x000000FC (Default)
- 0x0024 -- 0x0000000C + (rf_sync_sel_ch0<<4)

…

- 0x0030 -- 0x0003C31C + (rf_sync_sel_ch2<<13)
- 0x0034 -- 0x00000000 (Default)

…

- 0x0180 -- 0x0000BE00 + (drf_row_mode<<0)
  + (drf_column_mode<<4)

- 0x0184 -- 0x00000000 + (drf_t_rp<<0)
  + (drf_t_rcd<<4)
  + (drf_t_wr<<8)
  + (drf_t_rrd<<12)
  + (drf_t_ras<<16)
  + (drf_t_rtw<<20)
  + (drf_t_wtr<<24)
  + (drf_t_rtr<<28)
- 0x0188 -- 0x00000000 + (drf_t_wrd<<0)
  + (drf_t_ref<<4)
  + (drf_t_xsr<<16)
  + (drf_t_rfc<<24)
- 0x0194 -- 0x00600209
- 0x01A0 -- 0x00400001

Initialize external memory after configuring EMC:

- 0x0190 -- 0x40010000
- Wait until bit-16 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_ext_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared

Open auto-refresh after initializing external memory:

- Set 1 to bit-14 of 0x0180

Description:

- rf_sync_sel_chx: if the HCLK of this channel is synchronous with clk_emc, this bit can be set to improve performance.
- drf_row_mode: row address bit select. See memory device specifications for this information.
- drf_column_mode: column address bit select. See memory device specifications for this information.
- drf_t_ref: Maximum Refresh period (or tREF).

  (drf_t_ref+1)*T_cycle*(row number) <= tREF. T_cycle is clk_emc_ref cycle time.

  It's important that clk_emc_ref is different with clk_emc. Normally, clk_emc_ref is a fixed-frequency clock with low frequency.
- drf_t_rfc: Minimum AUTO-REFRESH period (or tRFC).

  (drf_t_rfc+2)*T_cycle >= tRFC.
- drf_t_rp: Minimum PRECHARGE command period time (or tRP).

  (drf_t_rp+1)*T_cycle >= tRP.
- drf_t_rcd: Minimum ACTIVE to READ or WRITE delay (or minimum RAS to CAS delay, or tRCD).

  (drf_t_rcd+1)*T_cycle >= tRCD.
- drf_t_rrd: Minimum ACTIVE to ACTIVE (in different bank) time (or tRRD).

  (drf_t_rrd+1)*T_cycle >= tRRD.
- drf_t_wr: Minimum Write recovery time (or minimum last data-in to PRECHARGE time, or tWR, or tDPL, or tRDL).

(drf_t_wr+1)*T_cycle >= tWR.

- drf_t_xsr: Minimum SELF-REFRESH time (tRAS for Micron, Samsung, etc).
  (drf_t_xsr+1)*T_cyle >= this minimum time.
- drf_t_ras: Minimum ACTIVE to PRECHARGE time (or minimum row active time, or tRAS-MIN).
  (drf_t_ras+1)*T_cyle >= tRAS-MIN.
- drf_t_mrd: Minimum LOAD MODE REGISTER to ACTIVE or REFRESH delay (or tMRD).
  (drf_t_mrd+2)*T_cycle >= tMRD.
- drf_mode_reg: Mode Register. drf_mode_reg[13:0] is mapped to A[13:0] and drf_mode_reg[15:14] is mapped to BA[1:0]. It's IMPORTANT that CAS Latency MUST be configured to 3 and Burst Length MUST be configured to 2 16-bit.
- drf_ext_mode_reg: Extended Mode Register

5.2.6.1.3 32-Bit SDR-SDRAM Configuration 1

Condition:

- CAS Latency is 2
- Burst Length is 1 32-bit or 2 32-bit

Configure EMC:

(Suppose SDR-SDRAM is connected on CS0)

- 0x0000 -- 0x00000C45 (Default)
- 0x0004 -- 0x00000002 (Default)
- 0x0010 -- 0x00000003 if Burst Length is 1 32-bit
- (0x0010 -- 0x00000113 if Burst Length is 2 32-bit) (Default)
- 0x0020 -- 0x000000FC (Default)
- 0x0024 -- 0x0000000C + (rf_sync_sel_ch0<<4)

…

- 0x0030 -- 0x0003C31C + (rf_sync_sel_ch2<<13)
- 0x0034 -- 0x00000000 (Default)

…

- 0x0180 -- 0x0000BF00 + (drf_row_mode<<0)
  + (drf_column_mode<<4)
- 0x0184 -- 0x00000000 + (drf_t_rp<<0)
  + (drf_t_rcd<<4)
  + (drf_t_wr<<8)
  + (drf_t_rrd<<12)
  + (drf_t_ras<<16)
  + (drf_t_rtw<<20)
  + (drf_t_wtr<<24)
  + (drf_t_rtr<<28)
- 0x0188 -- 0x00000000 + (drf_t_wrd<<0)
  + (drf_t_ref<<4)
  + (drf_t_xsr<<16)
  + (drf_t_rfc<<24)
- 0x0194 -- 0x00400007
- 0x01A0 -- 0x00100001

Initialize external memory after configuring EMC:

- 0x0190 -- 0x40010000

- Wait until bit-16 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_ext_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared

Open auto-refresh after initializing external memory:

- Set 1 to bit 14 of 0x0180

Description:

- rf_sync_sel_chx: if the HCLK of this channel is synchronous with clk_emc, this bit can be set to improve performance.
- drf_row_mode: row address bit select. See memory device specifications for this information.
- drf_column_mode: column address bit select. See memory device specifications for this information.
- drf_t_ref: Maximum Refresh period (or tREF).

  (drf_t_ref+1)*T_cycle*(row number) <= tREF. T_cycle is clk_emc_ref cycle time.

  It's important that clk_emc_ref is different with clk_emc. Normally, clk_emc_ref is a fixed-frequency clock with low frequency.
- drf_t_rfc: Minimum AUTO-REFRESH period (or tRFC).

  (drf_t_rfc+2)*T_cycle >= tRFC.
- drf_t_rp: Minimum PRECHARGE command period time (or tRP).

  (drf_t_rp+1)*T_cycle >= tRP.
- drf_t_rcd: Minimum ACTIVE to READ or WRITE delay (or minimum RAS to CAS delay, or tRCD).

  (drf_t_rcd+1)*T_cycle >= tRCD.
- drf_t_rrd: Minimum ACTIVE to ACTIVE (in different bank) time (or tRRD).

  (drf_t_rrd+1)*T_cycle >= tRRD.
- drf_t_wr: Minimum Write recovery time (or minimum last data-in to PRECHARGE time, or tWR, or tDPL, or tRDL).

  (drf_t_wr+1)*T_cycle >= tWR.
- drf_t_xsr: Minimum SELF-REFRESH time (tRAS for Micron, Samsung, etc).

  (drf_t_xsr+1)*T_cyle >= this minimum time.
- drf_t_ras: Minimum ACTIVE to PRECHARGE time (or minimum row active time, or tRAS-MIN).

  (drf_t_ras+1)*T_cyle >= tRAS-MIN.
- drf_t_mrd: Minimum LOAD MODE REGISTER to ACTIVE or REFRESH delay (or tMRD).

  (drf_t_mrd+2)*T_cycle >= tMRD.
- drf_mode_reg: Mode Register. drf_mode_reg[13:0] is mapped to A[13:0] and drf_mode_reg[15:14] is mapped to BA[1:0]. It's IMPORTANT that CAS Latency MUST be configured to 2 and Burst Length MUST be configured to 1 32-bit or 2 32-bit.
- drf_ext_mode_reg: Extended Mode Register

5.2.6.1.4 32-Bit SDR-SDRAM Configuration 2

Condition:

- CAS Latency is 3
- Burst Length is 1 32-bit or 2 32-bit

Configure EMC:

(Suppose SDR-SDRAM is connected on CS0)

- 0x0000 -- 0x00000C45 (Default)
- 0x0004 -- 0x00000002 (Default)
- 0x0010 -- 0x00000003 if Burst Length is 1 32-bit
- (0x0010 -- 0x00000113 if Burst Length is 2 32-bit)
- 0x0020 -- 0x000000FC (Default)
- 0x0024 -- 0x0000000C + (rf_sync_sel_ch0<<4)

…

- 0x0030 -- 0x0003C31C + (rf_sync_sel_ch2<<13)
- 0x0034 -- 0x00000000 (Default)

…

- 0x0180 -- 0x0000BF00 + (drf_row_mode<<0)
  + (drf_column_mode<<4)
- 0x0184 -- 0x00000000 + (drf_t_rp<<0)
  + (drf_t_rcd<<4)
  + (drf_t_wr<<8)
  + (drf_t_rrd<<12)
  + (drf_t_ras<<16)
  + (drf_t_rtw<<20)
  + (drf_t_wtr<<24)
  + (drf_t_rtr<<28)
- 0x0188 -- 0x00000000 + (drf_t_wrd<<0)
  + (drf_t_ref<<4)
  + (drf_t_xsr<<16)
  + (drf_t_rfc<<24)
- 0x0194 -- 0x00600209 (Default)
- 0x01A0 -- 0x00400001

Initialize external memory after configuring EMC:

- 0x0190 -- 0x40010000
- Wait until bit-16 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_ext_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared

Open auto-refresh after initializing external memory:

- Set 1 to bit 14 of 0x0180

Description:

- rf_sync_sel_chx: if the HCLK of this channel is synchronous with clk_emc, this bit can be set to improve performance.
- drf_row_mode: row address bit select. See memory device specifications for this information.

- drf_column_mode: column address bit select. See memory device specifications for this information.
- drf_t_ref: Maximum Refresh period (or tREF).
  (drf_t_ref+1)*T_cycle*(row number) <= tREF. T_cycle is clk_emc_ref cycle time.
  It's important that clk_emc_ref is different with clk_emc. Normally, clk_emc_ref is a fixed-frequency clock with low frequency.
- drf_t_rfc: Minimum AUTO-REFRESH period (or tRFC).
  (drf_t_rfc+2)*T_cycle >= tRFC.
- drf_t_rp: Minimum PRECHARGE command period time (or tRP).
  (drf_t_rp+1)*T_cycle >= tRP.
- drf_t_rcd: Minimum ACTIVE to READ or WRITE delay (or minimum RAS to CAS delay, or tRCD).
  (drf_t_rcd+1)*T_cycle >= tRCD.
- drf_t_rrd: Minimum ACTIVE to ACTIVE (in different bank) time (or tRRD).
  (drf_t_rrd+1)*T_cycle >= tRRD.
- drf_t_wr: Minimum Write recovery time (or minimum last data-in to PRECHARGE time, or tWR, or tDPL, or tRDL).
  (drf_t_wr+1)*T_cycle >= tWR.
- drf_t_xsr: Minimum SELF-REFRESH time (tRAS for Micron, Samsung, etc).
  (drf_t_xsr+1)*T_cyle >= this minimum time.
- drf_t_ras: Minimum ACTIVE to PRECHARGE time (or minimum row active time, or tRAS-MIN).
  (drf_t_ras+1)*T_cyle >= tRAS-MIN.
- drf_t_mrd: Minimum LOAD MODE REGISTER to ACTIVE or REFRESH delay (or tMRD).
  (drf_t_mrd+2)*T_cycle >= tMRD.
- drf_mode_reg: Mode Register. drf_mode_reg[13:0] is mapped to A[13:0] and drf_mode_reg[15:14] is mapped to BA[1:0]. It's IMPORTANT that CAS Latency MUST be configured to 3 and Burst Length MUST be configured to 1 32-bit or 2 32-bit.
- drf_ext_mode_reg: Extended Mode Register

5.2.6.1.5 16-Bit DDR-SDRAM Configuration 1

Condition:

- CAS Latency is 2
- Burst Length is 2 16-bit

Configure EMC:

(Suppose DDR-SDRAM is connected on CS0)

- 0x0000 -- 0x00000C45 (Default)
- 0x0004 -- 0x00000049
- 0x0010 -- 0x00000003
- 0x0020 -- 0x000000FC (Default)
- 0x0024 -- 0x0000000C + (rf_sync_sel_ch0<<4)

…

- 0x0030 -- 0x0003C31C + (rf_sync_sel_ch2<<13)
- 0x0034 -- 0x00000000 (Default)

…

- 0x0180 -- 0x0000BE00 + (drf_row_mode<<0)
  + (drf_column_mode<<4)
- 0x0184 -- 0x00000000 + (drf_t_rp<<0)

+ (drf_t_rcd<<4)
+ (drf_t_wr<<8)
+ (drf_t_rrd<<12)
+ (drf_t_ras<<16)
+ (drf_t_rtw<<20)
+ (drf_t_wtr<<24)
+ (drf_t_rtr<<28)

- 0x0188 -- 0x00000000 + (drf_t_wrd<<0)
  + (drf_t_ref<<4)
  + (drf_t_xsr<<16)
  + (drf_t_rfc<<24)
- 0x0194 -- 0x00622728
- 0x0198 -- 0x00080004
- 0x019C -- 0x00F0000E
- 0x01A0 -- 0x00F0000E

Configure delay lines:

DLL OFF:

clk_emc: 200MHz

- 0x010C -- 0x00000018
- 0x0110 -- 0x0000000C
- 0x0114 -- 0x0000000C
- 0x0118 -- 0x0000000C
- 0x011C -- 0x0000000C
- 0x0120 -- 0x0000000C
- 0x0124 -- 0x0000000C
- 0x0128 -- 0x0000000C
- 0x012C -- 0x0000000C
- 0x0130 -- 0x00000018
- 0x0134 -- 0x00000018
- 0x0138 -- 0x00000018
- 0x013C -- 0x00000018
- 0x0140 -- 0x00000018
- 0x0144 -- 0x00000018
- 0x0148 -- 0x00000018
- 0x014C -- 0x00000018

clk_emc: 400MHz

- 0x010C -- 0x0000000C
- 0x0110 -- 0x00000006
- 0x0114 -- 0x00000006
- 0x0118 -- 0x00000006
- 0x011C -- 0x00000006
- 0x0120 -- 0x00000006
- 0x0124 -- 0x00000006
- 0x0128 -- 0x00000006
- 0x012C -- 0x00000006
- 0x0130 -- 0x0000000C
- 0x0134 -- 0x0000000C
- 0x0138 -- 0x0000000C
- 0x013C -- 0x0000000C
- 0x0140 -- 0x0000000C
- 0x0144 -- 0x0000000C
- 0x0148 -- 0x0000000C
- 0x014C -- 0x0000000C

DLL ON:

- 0x0170 -- 0x00011080
- 0x010C -- 0x00008040
- 0x0110 -- 0x00008020
- 0x0114 -- 0x00008020
- 0x0118 -- 0x00008020
- 0x011C -- 0x00008020
- 0x0120 -- 0x00008020
- 0x0124 -- 0x00008020
- 0x0128 -- 0x00008020
- 0x012C -- 0x00008020
- 0x0130 -- 0x00008040
- 0x0134 -- 0x00008040
- 0x0138 -- 0x00008040
- 0x013C -- 0x00008040
- 0x0140 -- 0x00008040
- 0x0144 -- 0x00008040
- 0x0148 -- 0x00008040
- 0x014C -- 0x00008040
- 0x0170 -- 0x00011480

Initialize external memory after configuring EMC:

- 0x0190 -- 0x40010000
- Wait until bit-16 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_ext_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared

Open auto-refresh after initializing external memory:

- Set 1 to bit 14 of 0x0180

Description:

- rf_sync_sel_chx: if the HCLK of this channel is synchronous with clk_emc, this bit can be set to improve performance.
- drf_row_mode: row address bit select. See memory device specifications for this information.
- drf_column_mode: column address bit select. See memory device specifications for this information.
- drf_t_ref: Maximum Refresh period (or tREF).

  (drf_t_ref+1)*T_cycle*(row number) <= tREF. T_cycle is clk_emc_ref cycle time.

  It's important that clk_emc_ref is different with clk_emc. Normally, clk_emc_ref is a fixed-frequency clock with low frequency.
- drf_t_rfc: Minimum AUTO-REFRESH period (or tRFC).

  (drf_t_rfc+2)*T_cycle >= tRFC.
- drf_t_rp: Minimum PRECHARGE command period time (or tRP).

  (drf_t_rp+1)*T_cycle >= tRP.
- drf_t_rcd: Minimum ACTIVE to READ or WRITE delay (or minimum RAS to CAS delay, or tRCD).

(drf_t_rcd+1)*T_cycle >= tRCD.

- drf_t_rrd: Minimum ACTIVE to ACTIVE (in different bank) time (or tRRD).
  (drf_t_rrd+1)*T_cycle >= tRRD.
- drf_t_wr: Minimum Write recovery time (or minimum last data-in to PRECHARGE time, or tWR, or tDPL, or tRDL).
  (drf_t_wr -1)*T_cycle >= tWR.
- drf_t_xsr: Minimum SELF-REFRESH time (tRAS for Micron, Samsung, etc).
  (drf_t_xsr+1)*T_cyle >= this minimum time.
- drf_t_ras: Minimum ACTIVE to PRECHARGE time (or minimum row active time, or tRAS-MIN).
  (drf_t_ras+1)*T_cyle >= tRAS-MIN.
- drf_t_wtr: Minimum WRITE-to-READ turn-around time.
  (drf_t_wtr+1)*T_cycle >= tWTR+2.
- drf_t_mrd: Minimum LOAD MODE REGISTER to ACTIVE or REFRESH delay (or tMRD).
  (drf_t_mrd+2)*T_cycle >= tMRD.
- drf_mode_reg: Mode Register. drf_mode_reg[13:0] is mapped to A[13:0] and drf_mode_reg[15:14] is mapped to BA[1:0]. It's IMPORTANT that CAS Latency MUST be configured to 2 and Burst Length MUST be configured to 2 16-bit.
- drf_ext_mode_reg: Extended Mode Register

5.2.6.1.6 16-Bit DDR-SDRAM Configuration 2

Condition:

- CAS Latency is 3
- Burst Length is 2 16-bit

Configure EMC:

(Suppose DDR-SDRAM is connected on CS0)

- 0x0000 -- 0x00000C45 (Default)
- 0x0004 -- 0x00000049
- 0x0010 -- 0x00000003
- 0x0020 -- 0x000000FC (Default)
- 0x0024 -- 0x0000000C + (rf_sync_sel_ch0<<4)

…

- 0x0030 -- 0x0003C31C + (rf_sync_sel_ch2<<13)
- 0x0034 -- 0x00000000 (Default)

…

- 0x0180 -- 0x0000BE00 + (drf_row_mode<<0)
  + (drf_column_mode<<4)
- 0x0184 -- 0x00000000 + (drf_t_rp<<0)
  + (drf_t_rcd<<4)
  + (drf_t_wr<<8)
  + (drf_t_rrd<<12)
  + (drf_t_ras<<16)
  + (drf_t_rtw<<20)
  + (drf_t_wtr<<24)
  + (drf_t_rtr<<28)
- 0x0188 -- 0x00000000 + (drf_t_wrd<<0)
  + (drf_t_ref<<4)
  + (drf_t_xsr<<16)

+ (drf_t_rfc<<24)

- 0x0194 -- 0x0062272A
- 0x0198 -- 0x00200010
- 0x019C -- 0x00F0000E
- 0x01A0 -- 0x00F0000E

Configure delay lines:

DLL OFF:

clk_emc: 200MHz

- 0x010C -- 0x00000018
- 0x0110 -- 0x0000000C
- 0x0114 -- 0x0000000C
- 0x0118 -- 0x0000000C
- 0x011C -- 0x0000000C
- 0x0120 -- 0x0000000C
- 0x0124 -- 0x0000000C
- 0x0128 -- 0x0000000C
- 0x012C -- 0x0000000C
- 0x0130 -- 0x00000018
- 0x0134 -- 0x00000018
- 0x0138 -- 0x00000018
- 0x013C -- 0x00000018
- 0x0140 -- 0x00000018
- 0x0144 -- 0x00000018
- 0x0148 -- 0x00000018
- 0x014C -- 0x00000018

clk_emc: 400MHz

- 0x010C -- 0x0000000C
- 0x0110 -- 0x00000006
- 0x0114 -- 0x00000006
- 0x0118 -- 0x00000006
- 0x011C -- 0x00000006
- 0x0120 -- 0x00000006
- 0x0124 -- 0x00000006
- 0x0128 -- 0x00000006
- 0x012C -- 0x00000006
- 0x0130 -- 0x0000000C
- 0x0134 -- 0x0000000C
- 0x0138 -- 0x0000000C
- 0x013C -- 0x0000000C
- 0x0140 -- 0x0000000C
- 0x0144 -- 0x0000000C
- 0x0148 -- 0x0000000C
- 0x014C -- 0x0000000C

DLL ON:

- 0x0170 -- 0x00011080
- 0x010C -- 0x00008040
- 0x0110 -- 0x00008020
- 0x0114 -- 0x00008020
- 0x0118 -- 0x00008020
- 0x011C -- 0x00008020
- 0x0120 -- 0x00008020
- 0x0124 -- 0x00008020
- 0x0128 -- 0x00008020

- 0x012C -- 0x00008020
- 0x0130 -- 0x00008040
- 0x0134 -- 0x00008040
- 0x0138 -- 0x00008040
- 0x013C -- 0x00008040
- 0x0140 -- 0x00008040
- 0x0144 -- 0x00008040
- 0x0148 -- 0x00008040
- 0x014C -- 0x00008040
- 0x0170 -- 0x00011480

Initialize external memory after configuring EMC:

- 0x0190 -- 0x40010000
- Wait until bit-16 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_ext_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared

Open auto-refresh after initializing external memory:

- Set 1 to bit 14 of 0x0180

Description:

- rf_sync_sel_chx: if the HCLK of this channel is synchronous with clk_emc, this bit can be set to improve performance.
- drf_row_mode: row address bit select. See memory device specifications for this information.
- drf_column_mode: column address bit select. See memory device specifications for this information.
- drf_t_ref: Maximum Refresh period (or tREF).

  (drf_t_ref+1)*T_cycle*(row number) <= tREF. T_cycle is clk_emc_ref cycle time.

  It's important that clk_emc_ref is different with clk_emc. Normally, clk_emc_ref is a fixed-frequency clock with low frequency.
- drf_t_rfc: Minimum AUTO-REFRESH period (or tRFC).

  (drf_t_rfc+2)*T_cycle >= tRFC.
- drf_t_rp: Minimum PRECHARGE command period time (or tRP).

  (drf_t_rp+1)*T_cycle >= tRP.
- drf_t_rcd: Minimum ACTIVE to READ or WRITE delay (or minimum RAS to CAS delay, or tRCD).

  (drf_t_rcd+1)*T_cycle >= tRCD.
- drf_t_rrd: Minimum ACTIVE to ACTIVE (in different bank) time (or tRRD).

  (drf_t_rrd+1)*T_cycle >= tRRD.
- drf_t_wr: Minimum Write recovery time (or minimum last data-in to PRECHARGE time, or tWR, or tDPL, or tRDL).

  (drf_t_wr -1)*T_cycle >= tWR.
- drf_t_xsr: Minimum SELF-REFRESH time (tRAS for Micron, Samsung, etc).

  (drf_t_xsr+1)*T_cyle >= this minimum time.
- drf_t_ras: Minimum ACTIVE to PRECHARGE time (or minimum row active time, or tRAS-MIN).

  (drf_t_ras+1)*T_cyle >= tRAS-MIN.

- drf_t_wtr: Minimum WRITE-to-READ turn-around time.
  (drf_t_wtr+1)*T_cycle >= tWTR+2.
- drf_t_mrd: Minimum LOAD MODE REGISTER to ACTIVE or REFRESH delay (or tMRD).
  (drf_t_mrd+2)*T_cycle >= tMRD.
- drf_mode_reg: Mode Register. drf_mode_reg[13:0] is mapped to A[13:0] and drf_mode_reg[15:14] is mapped to BA[1:0]. It's IMPORTANT that CAS Latency MUST be configured to 2 and Burst Length MUST be configured to 2 16-bit.
- drf_ext_mode_reg: Extended Mode Register

5.2.6.1.7 32-Bit DDR-SDRAM Configuration 1

Condition:

- CAS Latency is 2
- Burst Length is 2 32-bit

Configure EMC:

(Suppose SDR-SDRAM is connected on CS0)

- 0x0000 -- 0x00000C45 (Default)
- 0x0004 -- 0x00000049
- 0x0010 -- 0x00000113 (Default)
- 0x0020 -- 0x000000FC (Default)
- 0x0024 -- 0x0000000C + (rf_sync_sel_ch0<<4)

…

- 0x0030 -- 0x0003C31C + (rf_sync_sel_ch2<<13)
- 0x0034 -- 0x00000000 (Default)

…

- 0x0180 -- 0x0000BF00 + (drf_row_mode<<0)
  + (drf_column_mode<<4)
- 0x0184 -- 0x00000000 + (drf_t_rp<<0)
  + (drf_t_rcd<<4)
  + (drf_t_wr<<8)
  + (drf_t_rrd<<12)
  + (drf_t_ras<<16)
  + (drf_t_rtw<<20)
  + (drf_t_wtr<<24)
  + (drf_t_rtr<<28)
- 0x0188 -- 0x00000000 + (drf_t_wrd<<0)
  + (drf_t_ref<<4)
  + (drf_t_xsr<<16)
  + (drf_t_rfc<<24)
- 0x0194 -- 0x00622728
- 0x0198 -- 0x00200010
- 0x019C -- 0x00F0000E
- 0x01A0 -- 0x00F0000E

Configure delay lines:

DLL OFF:

clk_emc: 200MHz

- 0x010C -- 0x00000018
- 0x0110 -- 0x0000000C

- 0x0114 -- 0x0000000C
- 0x0118 -- 0x0000000C
- 0x011C -- 0x0000000C
- 0x0120 -- 0x0000000C
- 0x0124 -- 0x0000000C
- 0x0128 -- 0x0000000C
- 0x012C -- 0x0000000C
- 0x0130 -- 0x00000018
- 0x0134 -- 0x00000018
- 0x0138 -- 0x00000018
- 0x013C -- 0x00000018
- 0x0140 -- 0x00000018
- 0x0144 -- 0x00000018
- 0x0148 -- 0x00000018
- 0x014C -- 0x00000018

clk_emc: 400MHz

- 0x010C -- 0x0000000C
- 0x0110 -- 0x00000006
- 0x0114 -- 0x00000006
- 0x0118 -- 0x00000006
- 0x011C -- 0x00000006
- 0x0120 -- 0x00000006
- 0x0124 -- 0x00000006
- 0x0128 -- 0x00000006
- 0x012C -- 0x00000006
- 0x0130 -- 0x0000000C
- 0x0134 -- 0x0000000C
- 0x0138 -- 0x0000000C
- 0x013C -- 0x0000000C
- 0x0140 -- 0x0000000C
- 0x0144 -- 0x0000000C
- 0x0148 -- 0x0000000C
- 0x014C -- 0x0000000C

DLL ON:

- 0x0170 -- 0x00011080
- 0x010C -- 0x00008040
- 0x0110 -- 0x00008020
- 0x0114 -- 0x00008020
- 0x0118 -- 0x00008020
- 0x011C -- 0x00008020
- 0x0120 -- 0x00008020
- 0x0124 -- 0x00008020
- 0x0128 -- 0x00008020
- 0x012C -- 0x00008020
- 0x0130 -- 0x00008040
- 0x0134 -- 0x00008040
- 0x0138 -- 0x00008040
- 0x013C -- 0x00008040
- 0x0140 -- 0x00008040
- 0x0144 -- 0x00008040
- 0x0148 -- 0x00008040
- 0x014C -- 0x00008040
- 0x0170 -- 0x00011480

Initialize external memory after configuring EMC:

- 0x0190 -- 0x40010000
- Wait until bit-16 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_ext_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared

Open auto-refresh after initializing external memory:

- Set 1 to bit 14 of 0x0180

Description:

- rf_sync_sel_chx: if the HCLK of this channel is synchronous with clk_emc, this bit can be set to improve performance.
- drf_row_mode: row address bit select. See memory device specifications for this information.
- drf_column_mode: column address bit select. See memory device specifications for this information.
- drf_t_ref: Maximum Refresh period (or tREF).

  (drf_t_ref+1)*T_cycle*(row number) <= tREF. T_cycle is clk_emc_ref cycle time.

  It's important that clk_emc_ref is different with clk_emc. Normally, clk_emc_ref is a fixed-frequency clock with low frequency.
- drf_t_rfc: Minimum AUTO-REFRESH period (or tRFC).

  (drf_t_rfc+2)*T_cycle >= tRFC.
- drf_t_rp: Minimum PRECHARGE command period time (or tRP).

  (drf_t_rp+1)*T_cycle >= tRP.
- drf_t_rcd: Minimum ACTIVE to READ or WRITE delay (or minimum RAS to CAS delay, or tRCD).

  (drf_t_rcd+1)*T_cycle >= tRCD.
- drf_t_rrd: Minimum ACTIVE to ACTIVE (in different bank) time (or tRRD).

  (drf_t_rrd+1)*T_cycle >= tRRD.
- drf_t_wr: Minimum Write recovery time (or minimum last data-in to PRECHARGE time, or tWR, or tDPL, or tRDL).

  (drf_t_wr -1)*T_cycle >= tWR.
- drf_t_xsr: Minimum SELF-REFRESH time (tRAS for Micron, Samsung, etc).

  (drf_t_xsr+1)*T_cyle >= this minimum time.
- drf_t_ras: Minimum ACTIVE to PRECHARGE time (or minimum row active time, or tRAS-MIN).

  (drf_t_ras+1)*T_cyle >= tRAS-MIN.
- drf_t_wtr: Minimum WRITE-to-READ turn-around time.

  (drf_t_wtr+1)*T_cycle >= tWTR+2.
- drf_t_mrd: Minimum LOAD MODE REGISTER to ACTIVE or REFRESH delay (or tMRD).

  (drf_t_mrd+2)*T_cycle >= tMRD.
- drf_mode_reg: Mode Register. drf_mode_reg[13:0] is mapped to A[13:0] and drf_mode_reg[15:14] is mapped to BA[1:0]. It's IMPORTANT that CAS Latency MUST be configured to 2 and Burst Length MUST be configured to 2 16-bit.
- drf_ext_mode_reg: Extended Mode Register

5.2.6.1.8 32-Bit DDR-SDRAM Configuration 2

Condition:

- CAS Latency is 3
- Burst Length is 2 32-bit

Configure EMC:

(Suppose SDR-SDRAM is connected on CS0)

- 0x0000 -- 0x00000C45 (Default)
- 0x0004 -- 0x00000049
- 0x0010 -- 0x00000113 (Default)
- 0x0020 -- 0x000000FC (Default)
- 0x0024 -- 0x0000000C + (rf_sync_sel_ch0<<4)

…

- 0x0030 -- 0x0003C31C + (rf_sync_sel_ch2<<13)
- 0x0034 -- 0x00000000 (Default)

…

- 0x0180 -- 0x0000BF00 + (drf_row_mode<<0)
  + (drf_column_mode<<4)
- 0x0184 -- 0x00000000 + (drf_t_rp<<0)
  + (drf_t_rcd<<4)
  + (drf_t_wr<<8)
  + (drf_t_rrd<<12)
  + (drf_t_ras<<16)
  + (drf_t_rtw<<20)
  + (drf_t_wtr<<24)
  + (drf_t_rtr<<28)
- 0x0188 -- 0x00000000 + (drf_t_wrd<<0)
  + (drf_t_ref<<4)
  + (drf_t_xsr<<16)
  + (drf_t_rfc<<24)
- 0x0194 -- 0x0062272A
- 0x0198 -- 0x00400020 (Default)
- 0x019C -- 0x00F0000E
- 0x01A0 -- 0x00F0000E

Configure delay lines:

DLL OFF:

clk_emc: 200MHz

- 0x010C -- 0x00000018
- 0x0110 -- 0x0000000C
- 0x0114 -- 0x0000000C
- 0x0118 -- 0x0000000C
- 0x011C -- 0x0000000C
- 0x0120 -- 0x0000000C
- 0x0124 -- 0x0000000C
- 0x0128 -- 0x0000000C
- 0x012C -- 0x0000000C
- 0x0130 -- 0x00000018
- 0x0134 -- 0x00000018
- 0x0138 -- 0x00000018
- 0x013C -- 0x00000018
- 0x0140 -- 0x00000018
- 0x0144 -- 0x00000018
- 0x0148 -- 0x00000018

- 0x014C -- 0x00000018

clk_emc: 400MHz

- 0x010C -- 0x0000000C
- 0x0110 -- 0x00000006
- 0x0114 -- 0x00000006
- 0x0118 -- 0x00000006
- 0x011C -- 0x00000006
- 0x0120 -- 0x00000006
- 0x0124 -- 0x00000006
- 0x0128 -- 0x00000006
- 0x012C -- 0x00000006
- 0x0130 -- 0x0000000C
- 0x0134 -- 0x0000000C
- 0x0138 -- 0x0000000C
- 0x013C -- 0x0000000C
- 0x0140 -- 0x0000000C
- 0x0144 -- 0x0000000C
- 0x0148 -- 0x0000000C
- 0x014C -- 0x0000000C

DLL ON:

- 0x0170 -- 0x00011080
- 0x010C -- 0x00008040
- 0x0110 -- 0x00008020
- 0x0114 -- 0x00008020
- 0x0118 -- 0x00008020
- 0x011C -- 0x00008020
- 0x0120 -- 0x00008020
- 0x0124 -- 0x00008020
- 0x0128 -- 0x00008020
- 0x012C -- 0x00008020
- 0x0130 -- 0x00008040
- 0x0134 -- 0x00008040
- 0x0138 -- 0x00008040
- 0x013C -- 0x00008040
- 0x0140 -- 0x00008040
- 0x0144 -- 0x00008040
- 0x0148 -- 0x00008040
- 0x014C -- 0x00008040
- 0x0170 -- 0x00011480

Initialize external memory after configuring EMC:

- 0x0190 -- 0x40010000
- Wait until bit-16 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40020000
- Wait until bit-17 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared
- 0x0190 -- 0x40040000 + (drf_ext_mode_reg<<0)
- Wait until bit-18 of 0x0190 is cleared

Open auto-refresh after initializing external memory:

- Set 1 to bit 14 of 0x0180

Description:

- rf_sync_sel_chx: if the HCLK of this channel is synchronous with clk_emc, this bit can be set to improve performance.
- drf_row_mode: row address bit select. See memory device specifications for this information.
- drf_column_mode: column address bit select. See memory device specifications for this information.
- drf_t_ref: Maximum Refresh period (or tREF).

  (drf_t_ref+1)*T_cycle*(row number) <= tREF. T_cycle is clk_emc_ref cycle time.

  It's important that clk_emc_ref is different with clk_emc. Normally, clk_emc_ref is a fixed-frequency clock with low frequency.
- drf_t_rfc: Minimum AUTO-REFRESH period (or tRFC).

  (drf_t_rfc+2)*T_cycle >= tRFC.
- drf_t_rp: Minimum PRECHARGE command period time (or tRP).

  (drf_t_rp+1)*T_cycle >= tRP.
- drf_t_rcd: Minimum ACTIVE to READ or WRITE delay (or minimum RAS to CAS delay, or tRCD).

  (drf_t_rcd+1)*T_cycle >= tRCD.
- drf_t_rrd: Minimum ACTIVE to ACTIVE (in different bank) time (or tRRD).

  (drf_t_rrd+1)*T_cycle >= tRRD.
- drf_t_wr: Minimum Write recovery time (or minimum last data-in to PRECHARGE time, or tWR, or tDPL, or tRDL).

  (drf_t_wr -1)*T_cycle >= tWR.
- drf_t_xsr: Minimum SELF-REFRESH time (tRAS for Micron, Samsung, etc).

  (drf_t_xsr+1)*T_cyle >= this minimum time.
- drf_t_ras: Minimum ACTIVE to PRECHARGE time (or minimum row active time, or tRAS-MIN).

  (drf_t_ras+1)*T_cyle >= tRAS-MIN.
- drf_t_wtr: Minimum WRITE-to-READ turn-around time.

  (drf_t_wtr+1)*T_cycle >= tWTR+2.
- drf_t_mrd: Minimum LOAD MODE REGISTER to ACTIVE or REFRESH delay (or tMRD).

  (drf_t_mrd+2)*T_cycle >= tMRD.
- drf_mode_reg: Mode Register. drf_mode_reg[13:0] is mapped to A[13:0] and drf_mode_reg[15:14] is mapped to BA[1:0]. It's IMPORTANT that CAS Latency MUST be configured to 2 and Burst Length MUST be configured to 2 16-bit.
- drf_ext_mode_reg: Extended Mode Register

5.2.6.1.9 Software-Controlled Sleep

EMC supports software-controlled manual-sleep. The sleep and wakeup tasks must run in on-chip memory, and software must guarantee no new access issued and check current access completed.

DMEM Sleep task:

Step1: Software program jumps to on-chip memory and guarantee no new access issued on DMEM.

Step2: Clear **drf_auto_ref_en** to disable AUTO-REFRESH function

Step3: Polling **rfemc_idle_sync** in EMC_STS3 until it's set, and then waiting for at least 50 EMC cycles.

Step4: Set **dsoft_pre_all**, then polling this bit until it's cleared.

Step5: Set **dsoft_self_ref**, then polling this bit until it's cleared.

Step6: Clear **drf_clkdmem_out_en** to close DMEM output clock (optional).

Step7: Software can close EMC core clock and sleep.

DMEM Wakeup task:

Step1: Set **drf_clkdmem_out_en** to open DMEM output clock after software wakes up on on-chip RAM.

Step2: Set **dsoft_resume**, then polling this bit until it's cleared.

Step3: Set **drf_auto_ref_en** to enable AUTO-REFRESH function.

Step4: Software can jump to DMEM to run.

5.2.6.1.10 Hardware-Controlled Auto-Sleep

EMC supports hardware-controlled auto-sleep. To enable this function, software need do the following configuring.

- set **rf_auto_sleep_en** to 1
- set all **rf_auto_sleep_en_chx** to 1 (optional, but recommended)
- clear **drf_auto_sleep_mode** to 0
- keep **drf_ref_cnt_rst** to 1

5.2.6.2 Limitation Summary

- **SDR Maximum Speed Limitation:**

In many cases, out-of-chip loop mode isn't used for SDR to save PADs, it leads to impact on maximum speed. From timing budget analysis, the key issue of SDR speed is that it is difficult to reduce delay from clock output to sample DFFs. So we have to balance this delay by delaying sample clock as possible, but if sample clock delay is too big, the skew between FF and SS cannot be controlled very well. As a result, to some (-8) SDR, tAC is 7ns, same as the (-10) SDR, EMC has to support 100MHz even if SDR itself can work on 125MHz. Out-of-chip loop mode can improve this performance because of similar path between output clock and sample clock.

- **WRAP-Mode AHB Burst Issues:**

WRAP-mode bursts can keep WRAP feature during AHB bursts mapping to channel bursts. But this feature cannot be kept during channel bursts mapping to device bursts to simplify hardware design, even if external memory is also in wrap mode. In order to reduce performance impacts, for SMEM, INCR mode is recommended. And for DMEM, short burst length is recommended.

- **DMEM Chip Select Limitation:**

Unlike SMEM, DMEM only supports up to 2 chip selects at the same time. And the 2 chip selects MUST follow the rules:

- If one chip select is used for DMEM, any of CS0, CS1 can be chosen.

5.3 NFC

5.3.1 Overview

The module implements a flexible controller for NAND flash memory. It manages the read/write interactions between a master host system and the external NAND Flash memory units. Master configures the NFC and initiates it to start the memory operation. For read/write access, NFC exchanges data with both internal data memory and spare memory through external AHB interface. Configurable features and internal configuration registers make it easy to adapt a variety memory device types.

NFC has an 8-bit/16-bit wide bus. And support page size of 512 / 1k / 2k / 4k /8k bytes. Moreover an internal hardware ECC encoder and decoder are provided and the external master can acquire the ECC by accessing adequate internal register.

5.3.2 Features

- Compatible to ONFI V1.0
- Support bus width of **8/16** bits
- Support Page size of **512/1K/2K/4K/8K** Bytes.
- Support Address Cycle of **3/4/5**
- Support at most 8-page consecutive read for memories with 512 bytes page.
- Support SuperAND Flash memory;
- Support NAND access with both micro-code and fixed-sequence command;
- Support data order switch between NFC_DMEM and NAND Flash device;
- Support Hardware ECC encoder and decoder
- Support ECC of **1/2/4/8/12/16/24** bits with info length 1~1024 Bytes
- Support Hardware DMA transfer mode.

5.3.3 Signal Description

NAND Flash controller includes below signals.

Table 5.3-1 NAND Flash Controller PIN List

Pin Name	I/O	Width	Description
nfc_cen	O	1	Chip enable, active low, work as CS0.
nfc_cle	O	1	Command latch enable, active high.
nfc_ale	O	1	Address latch enable, active high.
nfc_ren	O	1	Read enable, active low.
nfc_wen	O	1	Write enable, active low.
nfc_data_oe	O	1	Data output enable
nfc_data_out	O	16	Data output
nfc_data_in	I	16	Data input
nfc_rbn	I	1	Ready/busy output, high for ready, low for busy.
clk_nfc	I	1	Nand Flash clock signals
nfc_rst_n	I	1	Nand Flash reset signals
nfc_wpn	O	1	Write protect, active low.
nfc_bigend_en	I	1	Nand Flash endian signals
ptest_icg_mode	I	1	Nand ptest mode select

Pin Name	I/O	Width	Description
Int_req_nfc	O	1	Nand Flash interrupt signals
nfc_dmem_clk	O	1	Nand flash main data memory clock
nfc_dmem_cen	O	1	Nand flash main data memory chip enable
nfc_dmem_wen	O	4	Nand flash main data memory write enable
nfc_dmem_addr	O	11	Nand flash main data memory address
nfc_dmem_wdata	O	32	Nand flash main data memory write data
nfc_dmem_rdata	I	32	Nand flash main data memory read data
nfc_smem_clk	O	1	Nand flash spare data memory clock
nfc_smem_cen	O	1	Nand flash spare data memory chip enable
nfc_smem_wen	O	4	Nand flash spare data memory write enable
nfc_smem_addr	O	7	Nand flash spare data memory address
nfc_smem_wdata	O	32	Nand flash spare data memory write data
nfc_smem_rdata	I	32	Nand flash spare data memory read data
dma_req_nfc_tx	O	1	DMA Request for write data
dma_req_nfc_rx	O	1	DMA Request for read data
dma_ack_nfc_tx	I	1	DMA Acknowledge to Write
dma_ack_nfc_rx	I	1	DMA Acknowledge to read
AHB Signals Set			Nand Flash AHB signals set

5.3.4 Function Description

5.3.4.1 Function abstract

The NFC's application is as below.

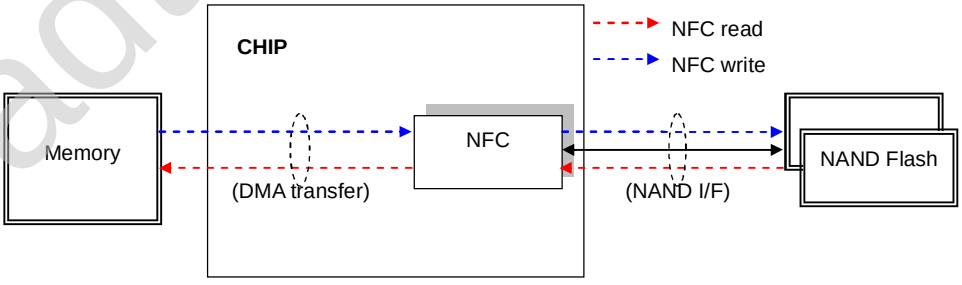


Figure 5.3-1 NFC Application

The NFC can read or write external NAND Flash memory, it supports up to 2 devices. When read, NFC gets data from extern NAND Flash memory and saves to internal memory, then transfers them to external memory through DMA channel; when write, work data may be transferred to internal memory through DMA channel, then NFC send them to extern NAND Flash memory.

NFC exchange NAND Flash memory data and other memory data with a specified NAND Flash memory interface. Its block diagram is shown in below.

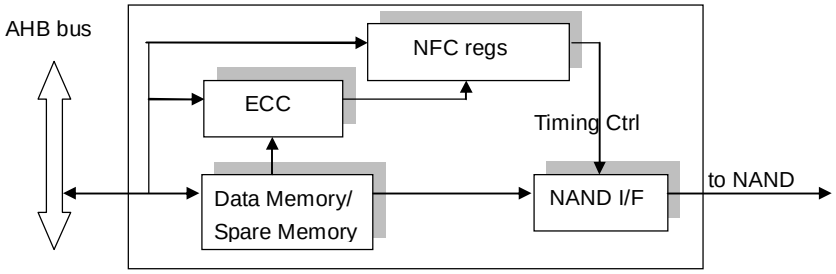


Figure 5.3-2 NFC Block Diagram

5.3.4.2 Memory Start/End Address Register

To support at most 4-page consecutive program/erase, the controller has 4 start address registers. For read operation, if the block number is more than one page, it will equal to one read batch operation.

Sequential operation will not be supported, that is, the start address and end address should be in the same page.

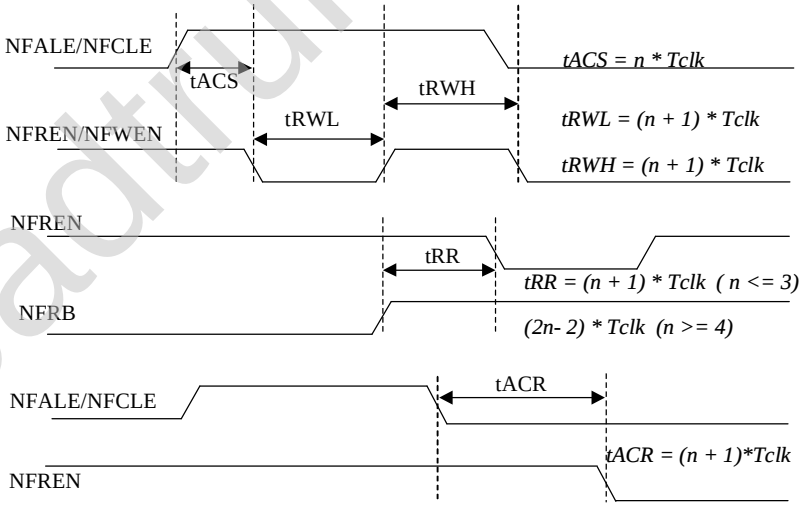
For large page NAND, the read batch and multi-plan operations are forbidden. Only the access for the first page can be processed, the other page process will be ignored.

During read operation, multi-page read means read “batch” command. For example, supposed that block_num is 4, and read data from NAND, the controller will continuously read 4 times.

Besides, if the M_END_ADDR n is 32’hFFFF_FFFF, it means the rest of current page specified by the M_END_ADDR n will be read out.

5.3.4.3 Timing Parameter Register

The read/write timing is shown in fellow.

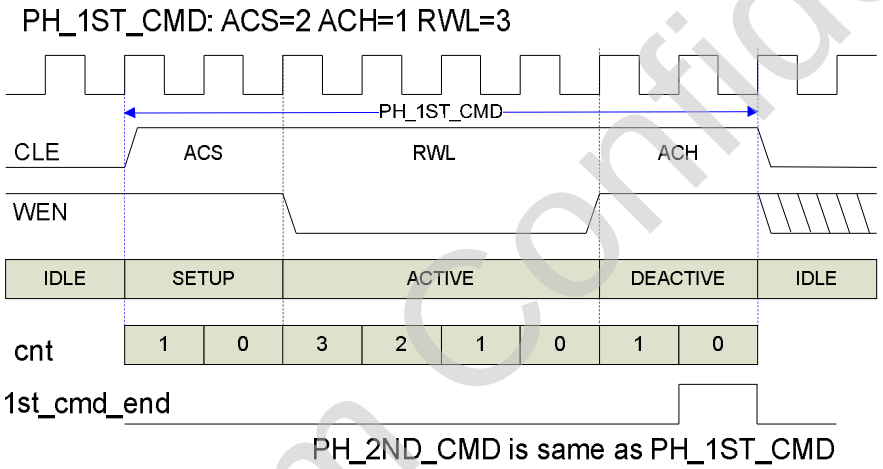


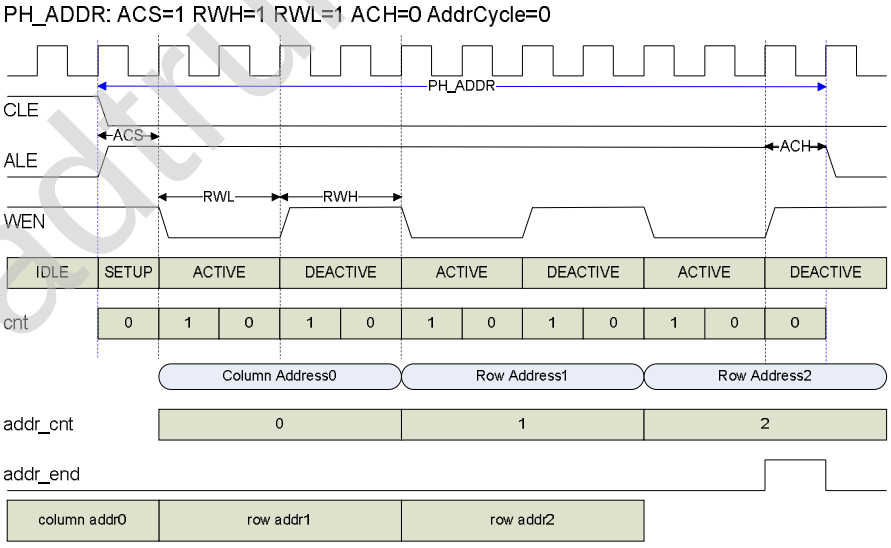
Description of these parameters

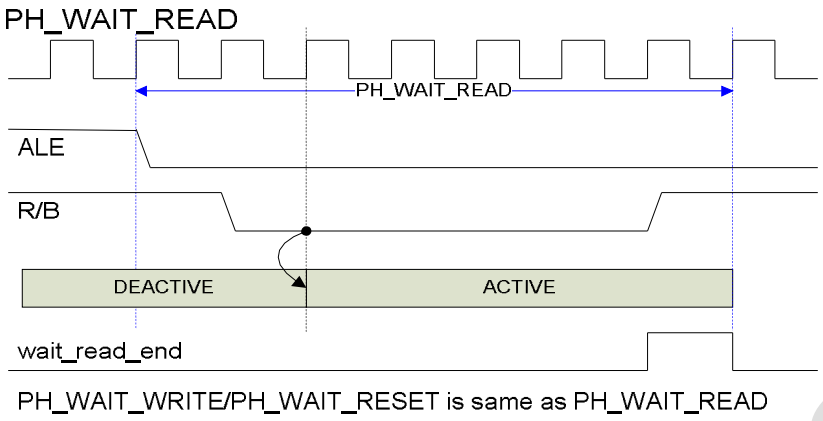
Parameter	Default	Description
ACS	1	Setup time for both ALE and CLE. tACS = n * Tclk
RWL	7	Active low pulse width for both RE and WE. tRWH = (n + 1) * Tclk

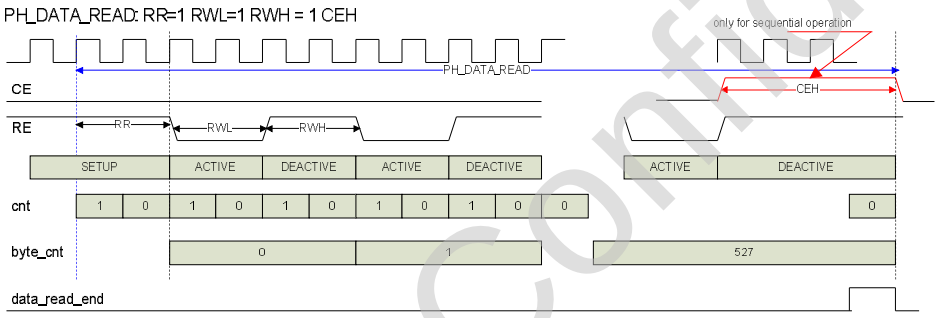
Parameter	Default	Description
RWH	1	Hold time for both RE and WE. tRWL = (n + 1) * Tclk
RR	3	Ready to RE low. When n <= 3, tRR = (n + 1) * Tclk. Otherwise tRR = (2n – 2) * Tclk
ACR	5	CLE to RE ready. ALE to RE ready. tACR = (n + 1) * Tclk
CEH	7	To terminate a Sequential Row Read operation set the Chip Enable signal to High for more than tCEH. tCEH=n * Tclk. For Flash without Sequential Read operation, this field must be set to 4'h0

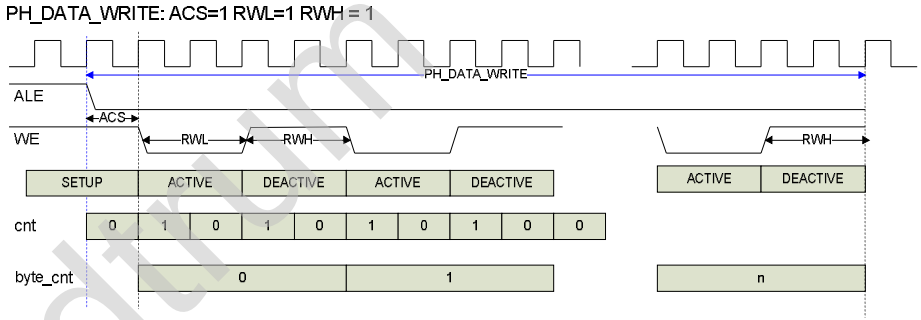
The following describes the cycles for some states

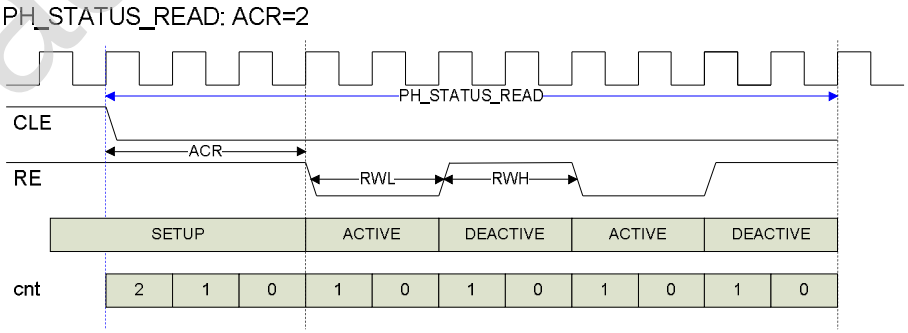












5.3.4.4 FSM in Fixed-Sequence Command

The following picture depicts the State Machine for NAND access.

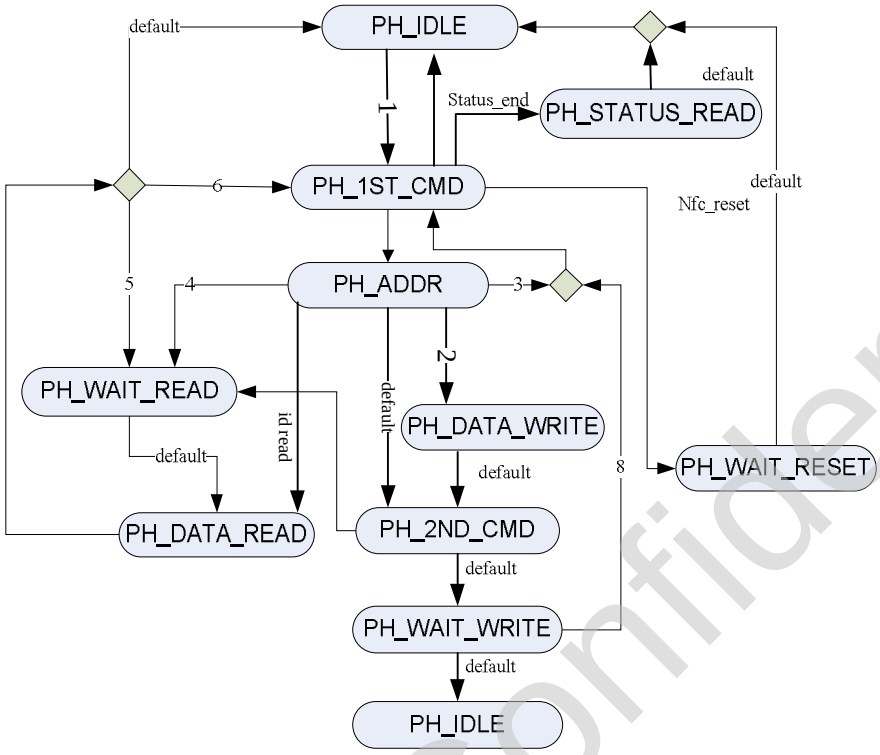


Figure 5.3-3 NFC Main FSM

1. (nfc_reset | nfc_rb_syn3) & nfc_start0
2. sp_program | mp_program
3. mp_erase & !mp_last_page
4. read & !addvance
   read = (sp_read | mp_read | id_read | seq_read)
5. seq_read & !mp_last_page
6. mp_read & !mp_last_page
7. read
8. mp_program & !mp_last_page

5.3.4.5 Modified FSM for Sub-Command

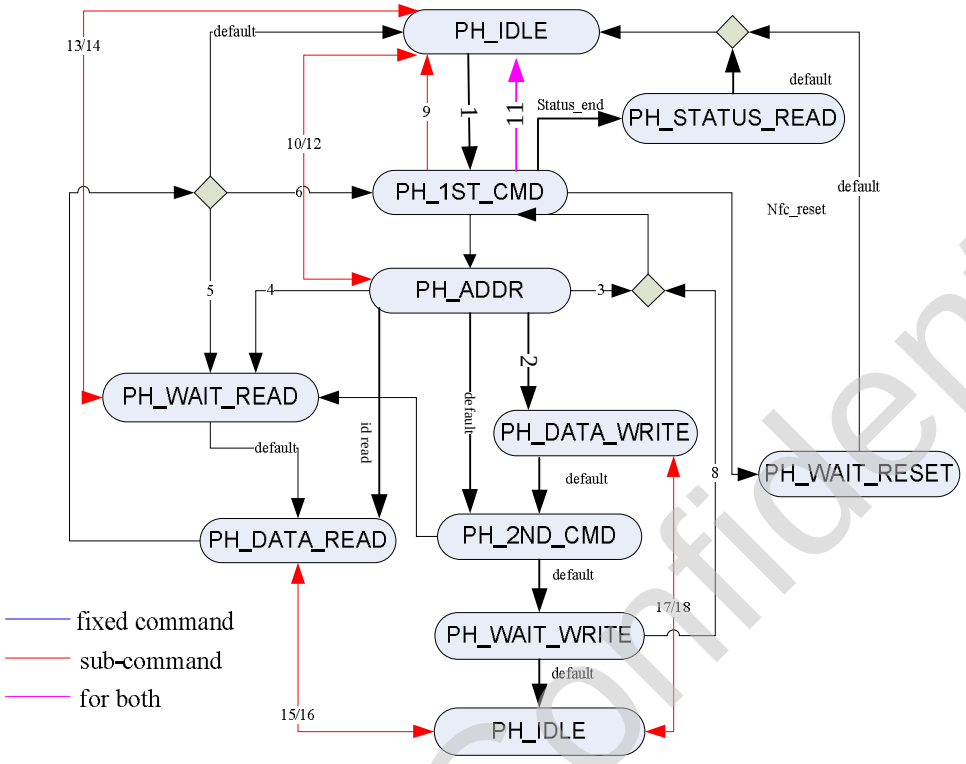


Figure 5.3-4 NFC Sub FSM

1. (nfc_reset | nfc_rb_syn3) & nfc_start0
2. sp_program | mp_program
3. mp_erase & !mp_last_page
4. read & !addvance
   read = (sp_read | mp_read | id_read | seq_read)
5. seq_read & !mp_last_page
6. mp_read & !mp_last_page
7. read
8. mp_program & !mp_last_page
9. for command sub-command

10/12. for address sub-command

11. pt_turn | cmd_mode

13/14 for waitRB sub-command

15/16. for read sub-command

17/18. for write sub-command

5.3.5 Micro-Instruction

5.3.5.1 Instruction Abstract

Instruction	Code	Description
Command	0xFD	Send one command to NAND Flash. Command supported by all kinds of NAND Flash, e.g.

Instruction	Code	Description
		0x50, 0x60 etc
Address	0xF1	Address specified in address input cycle. E.g. 0xA5F1: send 0xA5 to NAND as one input address. Active one address latch cycle.
WaitRB	0xF2	Wait for the end of NAND busy, that is, to detect one positive edge of R/B input signal.
ReadWord	0xF3	Word number (0 ~255). E.g. 0xFFF3: Read 256 words from NAND Flash. Initiate one or more read cycle When BusSize = 8, the “Word” indicate 8bits When BusSize = 16, the “Word” indicate 16bits
ReadBlock	0xF4	Block number. Number of Block (one block = 256 words). E.g. 0x00F4: Read 1 blocks 256 words from NAND When BusSize = 8, the “Word” indicate 8bits When BusSize = 16, the “Word” indicate 16bits
WriteWord	0xF6	Word number. (0~255) E.g. 0x10F6: Write 17 words into NAND Flash. Initiate one or more write cycle, including data, ID and status When BusSize = 8, the “Word” indicate 8bits When BusSize = 16, the “Word” indicate 16bits
WriteBlock	0xF7	Block number. Number of Block (one block = 256 words). E.g. 0x02F4: Write 3 blocks (768 words) into NAND When BusSize = 8, the “Word” indicate 8bits When BusSize = 16, the “Word” indicate 16bits
DeactiveCS	0xF9	Number of idle cycle. At most 16 cycles once. This instruction is used to stop sequential access.
Nop	0xFA	Wait for some idle clock cycles. At most 16 cycle once.

5.3.5.2 Instruction Format

Bits	15 ~ 8	7 ~ 0
Context	Parameters	Codes

5.3.5.3 Instruction FIFO

Software can issue at most 33 instructions once. And the number of one command batch can be specified by the INST_NUM. The real number of instruction is INST_NUM + 2. For example, if INST_NUM = 5’hE, that means there are 16 instructions waiting to execute in Instruction FIFO. The INST_NUM field should not larger than 5’h1E which indicate the number of 33.

No.	Instruction Address	Inst. Entry Name

No.	Instruction Address	Inst. Entry Name
0	0x0060	M_START_ADDR0
1	0x0064	M_START_ADDR1
2	0x0068	M_START_ADDR2
3	0x006C	M_START_ADDR3
4	0x0070	M_START_ADDR4
5	0x0074	M_START_ADDR5
6	0x0078	M_START_ADDR6
7	0x007C	M_START_ADDR7
8	0x0080	M_END_ADDR0
9	0x0084	M_END_ADDR1
10	0x0088	M_END_ADDR2
11	0x008C	M_END_ADDR3
12	0x0090	M_END_ADDR4
13	0x0094	M_END_ADDR5
14	0x0098	M_END_ADDR6
15	0x009C	M_END_ADDR7

Note: when in micro-instruction mode, the structure of NFC_CMD register will be different from when it in fix command mode. Please refer to the NFC_CMD registers description for details.

NFC will execute instructions as the following sequence:

Sequence	Executed CMD Position	Sequence	Executed CMD Position
0	NFC_CMD[15:0]	17	M_END_ADDR0[15:0]
1	M_START_ADDR0[15:0]	18	M_END_ADDR0[31:16]
2	M_START_ADDR0[31:16]	19	M_END_ADDR1[15:0]
3	M_START_ADDR1[15:0]	20	M_END_ADDR1[31:16]
4	M_START_ADDR1[31:16]	21	M_END_ADDR2[15:0]
5	M_START_ADDR2[15:0]	22	M_END_ADDR2[31:16]
6	M_START_ADDR2[31:16]	23	M_END_ADDR3[15:0]
7	M_START_ADDR3[15:0]	24	M_END_ADDR3[31:16]
8	M_START_ADDR3[31:16]	25	M_END_ADDR4[15:0]
9	M_START_ADDR4[15:0]	26	M_END_ADDR4[31:16]
10	M_START_ADDR4[31:16]	27	M_END_ADDR5[15:0]
11	M_START_ADDR5[15:0]	28	M_END_ADDR5[31:16]
12	M_START_ADDR5[31:16]	29	M_END_ADDR6[15:0]
13	M_START_ADDR6[15:0]	30	M_END_ADDR6[31:16]
14	M_START_ADDR6[31:16]	31	M_END_ADDR7[15:0]

Sequence	Executed CMD Position	Sequence	Executed CMD Position
15	M_START_ADDR7[15:0]	32	M_END_ADDR7[31:16]
16	M_START_ADDR7[31:16]		

5.3.5.4 Instruction Examples

This section will illustrate how to use the above instructions when accessing one type of NAND Flash. As to K9F1208D0A, please refer to the following table..

Example.1 Read one page with 528 bytes from No. 32 Page

Instruction List		Program Mask Code
0x00FD	//CMD 00	NFC_CMD [15:00] = 0x00FD
0x00F1	//ADDR 00	M_START_ADDR0 [15:00] = 0x00F1
0x00F1	//ADDR 00	M_START_ADDR0 [31:16] = 0x00F1
0x20F1	//ADDR 20	M_START_ADDR1 [15:00] = 0x20F1
0x00F1	//ADDR 00	M_START_ADDR1 [31:16] = 0x20F1
0x00F2	//WAIT RB	M_START_ADDR2 [15:00] = 0x00F2
0x01F4	//Read 2 blocks	M_START_ADDR2 [31:16] = 0x01F4
//Run the command		NFC_CMD [31:00] = 0x8005_00FD

Example.2 Three Plane Block Erase

Instruction List		Program Mask Code
0x60FD	//CMD 60	NFC_CMD [15:00] = 0x60FD
0x00F1	//ADDR 00	M_START_ADDR0 [15:00] = 0x00F1
0x00F1	//ADDR 00	M_START_ADDR0 [31:16] = 0x00F1
0x00F1	//ADDR 00	M_START_ADDR1 [15:00] = 0x00F1
0x60FD	//CMD 60	M_START_ADDR1 [31:16] = 0x60FD
0x00F1	//ADDR 00	M_START_ADDR2 [15:00] = 0x00F1
0x01F1	//ADDR 01	M_START_ADDR2 [31:16] = 0x01F1
0x00F1	//ADDR 00	M_START_ADDR3 [15:00] = 0x00F1
0x60FD	//CMD 60	M_START_ADDR3 [31:16] = 0x60FD
0x00F1	//ADDR 00	M_START_ADDR 4 [15:00] = 0x00F1
//Run the command		NFC_CMD [31:00] = 0x8008_60FD

Example.3 SUPERAND read one page

Instruction List	Program Mask Code

0x00FD	//CMD 00	NFC_CMD [15:00] = 0x00FD
0x00F1	//ADDR 00	M_START_ADDR0 [15:00] = 0x00F1
0x00F1	//ADDR 00	M_START_ADDR0 [31:16] = 0x00F1
0x20F1	//ADDR 20	M_START_ADDR1 [15:00] = 0x20F1
0x00F1	//ADDR 00	M_START_ADDR1 [31:16] = 0x00F1
0x00F2	//WAITRB	M_START_ADDR2 [15:00] = 0x00F2
0x00F4	//read one block	M_START_ADDR2 [31:16] = 0x00F4
0xF0FD	//stop command	M_START_ADDR3 [15:00] = 0xF0FD
//Run the command		NFC_CMD [31:00] = 0x8006_00FD

Note:

1. Two consequence micro-instructions have one clock turn-around time.
2. The tRR should be controlled by inside one or more NOP instructions.

5.3.6 Control Registers

5.3.6.1 Memory map

ARM base address: 0x6000_0000

Offset Address	Name	Description
0x0000	NFC_CMD	NAND operation command
0x0004	NFC_CFG0	NAND operation configuration 0
0x0008	NFC_CFG1	NAND operation configuration 1
0x000C	Reserved	
0x0010	NFC_TIMING	NAND operation timings
0x0014	NFC_TIMEOUT	NAND timeout configuration
0x0018	NFC_ID_STS	ID or status read result
0x001C	Reserved	
0x0020	NFC_INT_STS_EN	Interrupt source
0x0024	NFC_INT_CLR_RAW	Interrupt source enable
0x0028 ~ 0x002C	Reserved	
0x0030	NFC_ECC_CFG0	Configure ECC0
0x0034	NFC_ECC_CFG1	Configure ECC1
0x0038 ~ 0x003C	Reserved	
0x0040	NFC_ECC_STS0	ECC Status0
0x0044	NFC_ECC_STS1	ECC Status1
0x0048	NFC_ECC_STS2	ECC Status2
0x004C	NFC_ECC_STS3	ECC Status3
0x0050 ~ 0x005C	Reserved	

Offset Address	Name	Description
0x0060	M_START_ADDR0	Memory start address 0
0x0064	M_START_ADDR1	Memory start address 1
0x0068	M_START_ADDR2	Memory start address 2
0x006C	M_START_ADDR3	Memory start address 3
0x0070	M_START_ADDR4	Memory start address 4
0x0074	M_START_ADDR5	Memory start address 5
0x0078	M_START_ADDR6	Memory start address 6
0x007C	M_START_ADDR7	Memory start address 7
0x0080	M_END_ADDR0	Memory end address 0
0x0084	M_END_ADDR1	Memory end address 1
0x0088	M_END_ADDR2	Memory end address 2
0x008C	M_END_ADDR3	Memory end address 3
0x0090	M_END_ADDR4	Memory end address 4
0x0094	M_END_ADDR5	Memory end address 5
0x0098	M_END_ADDR6	Memory end address 6
0x009C	M_END_ADDR7	Memory end address 7
NFC Internal Memory		
0x2000~0x3FFF	NFC_DMEM	Can be accessed through DMA software channel.
0x4000~0x43FF	NFC_SMEM	Can be accessed through DMA software channel.

5.3.6.2 Register Descriptions

5.3.6.2.1 NFC_CMD

Description: NAND operation command.

0x0000	NAND operation command (for fixed sequence command)															NFC_CMD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	VALID	Reserved												BLK_NUM		
Type	R/W	RO												R/W		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CMD															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

VALID	[31]	R/W	1'h0	Write '1' to indicate a valid command, it will be cleared by HW after complete the command.
	[30:19]	RO	12'h0	Reserved
BLK_NUM	[18:16]	R/W	3'h0	Block number. Number of consecutive page/plane operations. 0: 1-page operation 1: 2-page operation ... 7: 8-page operation When accessing the device with 4k bytes of one page, this field will be ignored. Only one page can be accessed once. For multi-plane operations, if this field is zero, it will be the same as a single-page operation.
CMD	[15:0]	R/W	16'h0	Commands supported by most of NAND Flash. They are 00/50/90/FF/80/60/70/71/FD. For large page (2112 bytes per page), only 00h is supported in read command. For small page (512 bytes per page), either 00h or 01h is determined by the tenth address bit. In case of multi-plane operations, it is indicated by BLK_NO field in Command register. Moreover, all control signals can be directly assigned by MCU programming. Here, all output signals can be used as GPIO. When Command [7:0] is 8'h5A, {rd,cle,ale,cen,wen,ren,wpn,data_oen} = Command[15:8]. If rd is 1 and data_oen is 0, the DATA will be stored into DATA_BUF register, otherwise, wdata will be driven by DATA register. For advance device, the second cycle command will be 30h. For area switching, area pointer is specified by command[15:8]. For example, command[15:0] = 16'h50fd, it means changing point to spare area. Moreover, this command is invalid for this kind of device with 2k bytes per page.

0x0000	NAND operation command (for micro-code way)															NFC_CMD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	VALID	Reserved										INST_NUM				
Type	R/W	RO										R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CMD															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

			Value	
VALID	[31]	R/W	1'h0	Write '1' to indicate a valid command, it will be cleared by HW after complete the command.
	[30:21]	RO	10'h0	Reserved
INST_NUM	[20:16]	R/W	5'h0	The number of micro-instructions is INST_NUM + 1.
CMD	[15:0]	R/W	16'h0	The first micro-code

The commands support most of NAND Flash. All commands are listed below.

Table xx NAND Command List

Command	Encode	Command Sequence	
		1st. Cycle	2nd. Cycle
Read	00h	00h	
		01h	
Read C	50h	50h	
Read ID	90h	90h	
Reset	FFh	FFh	
Page Program(True)	80h	80h	10h
Page Program(Dummy)		80h	11h
Block Erase	60h	60h	D0h
Multi-Plane Block Erase		60h—60h	D0h
Read Status	70h	70h	
Read Multi-Plane Status	71h	71h	
GPIO	FEh		
Area switch	FDh		

For large page (2112 byte per page), only 00h is supported in read command. For small page (512byte per page), either 00h or 01h is determined by the tenth address bit.

In case of multi-plane operations, it is indicated by Block Number field in Command register.

Moreover, all control signals can be directly assigned by MCU programming. Here, all output signals can be used as GPIO. When Command [7:0] is 8'h5A, {rd,cle,ale,cen,wen,ren,wpn,data_oen} = Command[15:8]. If rd is 1 and data_oen is 0, the DATA will be stored into DataBuf register; otherwise, wdata will be driven by DATA register.

For advance device, the second cycle command will be 30h.

For area witching, area pointer is specified by command [15:8]. For example, command [15:0] =16'h50fd, it means changing point to spare area. Moreover, this command is invalid for this kind of device with 2kbyte per page.

5.3.6.2.2 NFC_CFG0

Description: NFC Configuration 0

0x0004			NFC configuration (reset 0x01)													NFC_CFG0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved						NFC_SP_SIZE									
Type	RO						R/W									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	NFC_CMD_SET	ADVANCE	ADD_CYCLE		PAGE_TYPE			Reserved		CS_SEL	DEV_BUS_SIZE	NFC_MEM_SWITCH	MEM_NFC_SWITCH	NFC_WPN	NFC_CMD_CLR	NFC_RBN
Type	R/W	R/W	R/W		R/W			RO		R/W	R/W	R/W	R/W	R/W	WO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Field Name	Bit	Type	Reset Value	Description
	[31:26]	RO	6'h0	Reserved
NFC_SP_SIZE	[25:16]	R/W	10'h00	For SLC, the spare area is relatively fixed value for every 512Bytes main area data. For MLC, the spare area is not integral multiple of 16bytes for every 512Bytes main area data, and then software should specify the spare area size. To simple the software configuration, there are some default values which are used more frequently for different PageSize will be set. The special value of 10'h00 will do this function. When "NFC_SP_SIZE" == 10'h0, the real Spare area size will be set to following value, but not 0. PageSize == 512Bytes: spare size is **16**Bytes. PageSize == 1K Bytes: spare size is **32** Bytes PageSize == 2K Bytes: spare size is **64** Bytes PageSize == 4K Bytes: spare size is **224** Bytes PageSize == 8K Bytes spare size is **448** Bytes. When "NFC_SP_SIZE != 10'h0", the real Spare area size will be set to the set value add 1, and the default value will be invalided. E.g. 0x001, indicate 2 bytes 0x07F, indicate 128 bytes 0x0FF, indicate 256 bytes 0x3FF, indicate 1024 bytes
NFC_CMD_SET	[15]	R/W	1'h0	CMD Set mode 0: Signal Command operation; 1: Micro-Instruction operation. It is auto clear to 0 after this process is done.
ADVANCE	[14]	R/W	1'h0	Advance. Flash memory has 2nd cycle read command (30h). Active high.

				(If NFC_CMD_SET = 1, this bit is ignored)
ADDR_CYCLE	[13:12]	R/W	2'h0	Address cycles of NAND flash memory, work with ADV flag as follows. 00 : 3 address cycles 01 : 4 address cycles 10 : 5 address cycles 11 : Reserved (If NFC_CMD_SET = 1, these bits are ignored)
PAGE_TYPE	[11:9]	R/W	3'h0	Page type 000: 512 Bytes / Page 001: 1K Bytes / Page 010: 2K Byte / Page 011: 4K Byte / Page 100: 8K Byte / Page Others: Reserved (If NFC_CMD_SET = 1, these bits are ignored)
	[8:7]	RO	2'h0	Reserved
CS_SEL	[6]	R/W	1'h0	CS select 0: CS0 is valid, CS1 is invalid 1: CS1 is valid, CS0 is invalid
DEV_BUS_SIZE	[5]	R/W	1'h0	Device bus size 0: x8 device 1: x16 device
NFC_MEM_SWITCH	[4]	R/W	1'h0	NFC to memory endian switch
MEM_NFC_SWITCH	[3]	R/W	1'h0	Memory to NFC endian switch
NFC_WPN	[2]	R/W	1'h0	Nand write protection. Active low. 0: Protection. 1: Not Protection
NFC_CMD_CLR	[1]	WO	1'h0	Write 1 to this bit to clear the controller command
NFC_RBN	[0]	RO	1'h1	Whether Nand Flash is busy. 0: Busy 1: Not Busy

5.3.6.2.3 NFC_CFG1

Description: NFC configuration 1

0x0008			NFC configuration (reset 0x00)													NFC_CFG1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														DMA_RX_EN	DMA_TX_EN
Type	RO														R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:2]	RO	30'h0	Reserved
DMA_RX_EN	[1]	R/W	1'h0	NFC DMA RX mode enable
DMA_TX_EN	[0]	R/W	1'h0	NFC DMA TX mode enable

5.3.6.2.4 NFC_TIMING

Description: NAND operation timing parameters.

0x0010			NAND operation timing (reset 0x1C65_1C21)													NFC_TIMING
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	CEH						RR						ACR			
Type	R/W						R/W						R/W			
Reset	0	0	0	1	1	1	0	0	0	1	1	0	0	1	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RWL						RWH						ACS			
Type	R/W						R/W						R/W			
Reset	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0	1

Field Name	Bit	Type	Reset Value	Description
CEH	[31:26]	R/W	6'h7	To terminate a Sequential Row Read operation set the Chip Enable signal to High for more than tCEH. tCEH = n * Tclk For Flash without Sequential Read operation, this field must be set to 0.
RR	[25:21]	R/W	5'h3	Ready to RE low tRR = (n + 1) * Tclk, when n <= 3 tRR = (2n – 2) * Tclk, otherwise
ACR	[20:16]	R/W	5'h5	CLE to RE ready, ALE to RE ready

				tACR = (n + 1) * Tclk
RWL	[15:10]	R/W	6'h7	Active low pulse width for both RE and WE tRWL = (n + 1) * Tclk
RWH	[9:5]	R/W	5'h1	Hold time for both RE and WE tRWH = (n + 1) * Tclk
ACS	[4:0]	R/W	5'h1	Setup time for both ALE and CLE tACS = n * Tclk

All these parameters make up of NAND read/write timing control, their definitions and relations are shown in Figure xx.

5.3.6.2.5 NFC_TIMEOUT

Description: Timeout to detect NAND R/B busy period.

0x0014			Timeout to detect NAND R/B busy period (reset 0x3fffff)											NFC_TIMEOUT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	TIMEOUT															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TIMEOUT															
Type	R/W															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
TIMEOUT	[31:0]	R/W	32'h3fffff	Timeout to detect NAND R/B busy period.

5.3.6.2.6 NFC_ID_STATUS

Description: NFC ID or status result.

0x0018			NFC ID or status result													NFC_ID_STATUS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	ID_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ID_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
ID_STATUS	[31:0]	RO	32'h0	The result of either ID read or status read operation is stored in this register.

5.3.6.2.7 NFC_INT_STS_EN

Description: NFC interrupts status and enables signals

0x0020			NFC interrupt status and enable													NFC_INT_STS_EN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved											INT_TO_STS	INT_WP_STS	INT_ERR_STS	INT_ECC_DONE_STS	INT_NFC_DONE_STS
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											INT_TO_EN	INT_WP_EN	INT_ERR_EN	INT_ECC_DONE_EN	INT_NFC_DONE_EN
Type	RO											R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:21]	RO	11'h0	Reserved
INT_TO_STS	[20]	RO	1'h0	Masked INT_TO interrupt.
INT_WP_STS	[19]	RO	1'h0	Masked INT_WP interrupt.
INT_ERR_STS	[18]	RO	1'h0	Masked INT_ERR interrupt.
INT_ECC_ DONE_STS	[17]	RO	1'h0	Masked INT_ECC_DONE interrupt.

INT_NFC_ DONE_STS	[16]	RO	1'h0	Masked INT_NFC_DONE interrupt.
	[15:5]	RO	11'h0	Reserved
INT_TO_EN	[4]	R/W	1'h0	Interrupt when NAND access timeout. Set '1' to enable this interrupt.
INT_WP_EN	[3]	R/W	1'h0	Interrupt when programming or erasing NAND in write-protection mode. Set '1' to enable this interrupt.
INT_ERR_EN	[2]	R/W	1'h0	Interrupt when AHB tries to modify some configuration when NAND is in processing. Set '1' to enable this interrupt.
INT_ECC_ DONE_EN	[1]	R/W	1'h0	Interrupt when ECC calculation is done. Set '1' to enable this interrupt.
INT_NFC_ DONE_EN	[0]	R/W	1'h0	Interrupt when NAND operation finishing. Set '1' to enable this interrupt.

Note:

When writing (ECC encode) NAND Flash, the INT_ECC_DONE interrupt is occurred before INT_NFC_DONE interrupt;

When reading (ECC decode) NAND Flash, the INT_ECC_DONE interrupt is occurred after INT_NFC_DONE interrupt.

5.3.6.2.8 NFC_INT_CLR_RAW

Description: NFC interrupts clear and raw status

0x0024	NFC interrupt clear and raw														NFC_INT_CLR_RAW	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved											INT_TO_CLR	INT_WP_CLR	INT_ERR_CLR	INT_ECC_DONE_CLR	INT_NFC_DONE_CLR
Type	RO											R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											INT_TO_RAW	INT_WP_RAW	INT_ERR_RAW	INT_ECC_DONE_RAW	INT_NFC_DONE_RAW
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:21]	RO	11'h0	Reserved
INT_TO_CLR	[20]	R/W	1'h0	Clear INT_TO interrupt.

INT_WP_CLR	[19]	R/W	1'h0	Clear INT_WP interrupt.
INT_ERR_CLR	[18]	R/W	1'h0	Clear INT_ERR interrupt.
INT_ECC_ DONE_CLR	[17]	R/W	1'h0	Clear INT_ECC_DONE interrupt.
INT_NFC_ DONE_CLR	[16]	R/W	1'h0	Clear INT_NFC_DONE interrupt.
	[15:5]	RO	11'h0	Reserved
INT_TO_RAW	[4]	RO	1'h0	Raw INT_TO interrupt.
INT_WP_RAW	[3]	RO	1'h0	Raw INT_WP interrupt.
INT_ERR_RAW	[2]	RO	1'h0	Raw INT_ERR interrupt.
INT_ECC_ DONE_RAW	[1]	RO	1'h0	Raw INT_ECC_DONE interrupt.
INT_NFC_ DONE_RAW	[0]	RO	1'h0	Raw INT_NFC_DONE interrupt.

5.3.6.2.9 NFC_ECC_CFG0

Description: ECC Configure 0.

0x0030	ECC Configure (Reset 32'hF0000)												NFC_ECC_CFG0			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	ECC_SEC_POS								ECC_SEC_SIZE							
Type	R/W								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				ECC_NUM				Reserved	ECC_MODE			ECC_SP_EN DIAN	ECC_DE CODE	ECC_AU TO_EN	ECC_AC T IVE
Type	RO				R/W				RO	R/W			R/W	R/W	R/W	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
ECC_SEC_POS	[31:24]	R/W	8'h0	ECC sector position of read or write data when ECC is enabled.
ECC_SEC_SIZE	[23:16]	R/W	8'hf	Spare sector area size, not the whole spare area size. E.g. 8'h0, size is 1 byte 8'h1, size is 2 byte

				8'hFF, size is 256 Bytes (Default is 16 bytes)
	[15:12]	RO	5'h0	Reserved
ECC_NUM	[11:8]	R/W	4'h0	The times to evaluate ECC. E.g. 4'h0, number is 1 4'h3, number is 4 4'h7, number is 8
	[7]	RO	1'h0	Reserved
ECC_MODE	[6:4]	R/W	3'b0	ECC mode. 000: 1 Bits 001: 2 Bits. 010: 4 Bits 011: 8 Bits 100: 12 Bits 101: 16 Bits 110: 24 Bits 111: Reserved
ECC_SP_ENDIAN	[3]	R/W	1'h0	ECC spare memory endian.
ECC_DECODE	[2]	R/W	1'h0	This bit indicated whether the ECC act as encoder or decoder. 0: encoder 1: decoder
ECC_AUTO_EN	[1]	R/W	1'h0	If set this bit 1'b1, then the ECC function will be active in auto mode, and the ECC_ACTIVE will be ignored. (It is not auto cleared, and SW should write 0 to clear it)
ECC_ACTIVE	[0]	WO	1'b0	Software writes this bit active the start ECC for encoding or decoding. (If ECC_AUTO_EN =1, it is no used) (It is auto cleared to 0 after write 1)

5.3.6.2.10 NFC_ECC_CFG1

Description: ECC Configure 1.

0x0034			ECC Configure (Reset 32'h1FF)												NFC_ECC_CFG1	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved					ECC_MAIN_ADDR										
Type	RO					R/W										
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ECC_LOCATION	Reserved					ECC_INFO_SIZE									
Type	R/W	RO					R/W									
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:27]	RO	5'h0	Reserved
ECC_MAIN_ADDR	[26:16]	R/W	11'h0	ECC_MAIN_ADDR (Unit Words) Then, this register indicates the beginning address of the ECC parity in the main area when the ECC_LOCATION is 1, while the micro-code operation is processed. Note, the ECC_MAIN_ADDR may not nearly follow the valid main data; it can be located at any address in the main area. The unit is words, not bytes. Eg. 11'h0: address = 0 word (0 byte) 11'h80: address = 128 words (512 bytes) (equal to one small page) 11'h200: address = 512 words (2K bytes) (equal one large page) Please see below domestication of this register indicated.
ECC_LOCATION	[15]	R/W	1'b0	This register indicates where the ECC bits located. 0: ECC is located in the spare memory buffer 1: ECC is located in the main memory buffer
	[14:10]	RO	5'h0	Reserved
ECC_INFO_SIZE	[9:0]	R/W	10'h1FF	ECC_INFO_SIZE (Unit Bytes) This register indicates the ECC information bytes; the ECC will be encoded or decoded based on these data. it ranges from 1 Byte to 1K Bytes. The real size is the set value adds 1. e.g. 10'h0 : 1 Bytes 10'h1FF: 512Bytes (default) 10'h3FF: 1K Bytes Note:

				In following two cases, the ECC_INFO_SIZE should be configured to word (32bits) aligned. 1) ECC_LOCATION = 1 2) (ECC_LOCATION = 0) & (ECC_NUM != 4'h0);

Demonstration of the ECC parameters indicated.

Figure 1

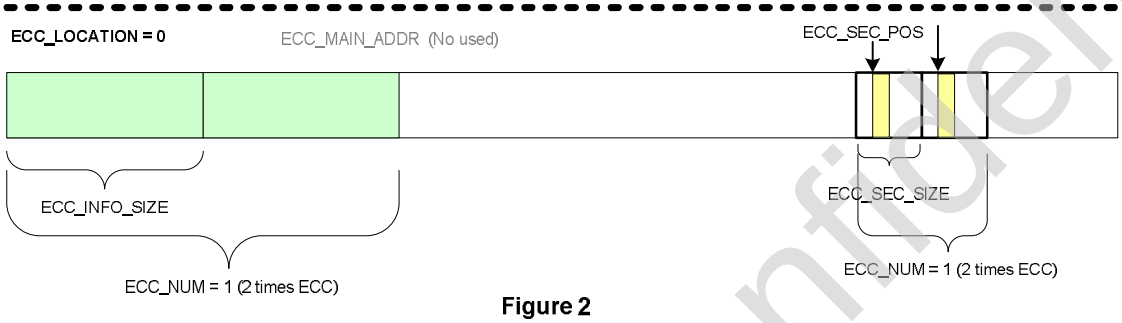


Figure 2

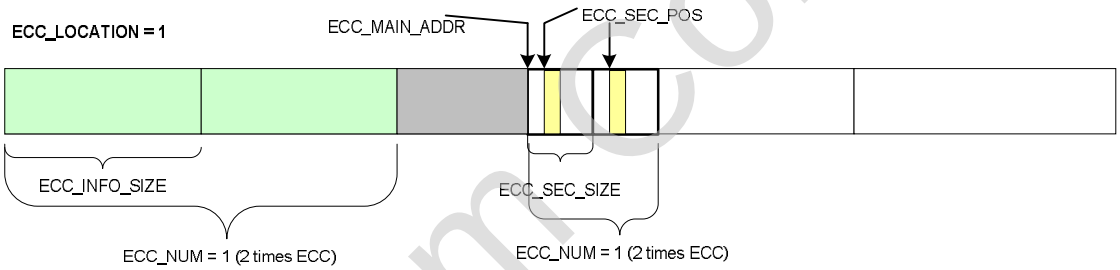


Figure 3

Figure 1 is a reference of main and spare buffer.

Figure 2 is when the ECC_LOCATION = 0, where the ECC parity is located in the spare area.

ECC_INFO_SIZE indicates the ECC information data size.

ECC_SEC_SIZE indicates every sector's bytes size in the spare area;

ECC_SEC_POS indicates the beginning address of parity in each sector,

ECC_NUM indicates the times to calculate the ECC, here 2 times will be calculated.

Figure 3 is when the ECC_LOCATION = 1, where the ECC parity is located after the information data in the main area.

MAIN_AREA_DATA_SIZE indicates the main data information size, which may be bigger or equal to the ECC_INFO_SIZE * (ECC_NUM + 1)

5.3.6.2.11 NFC_ECC_STS0

Description: ECC result.

0x0040			ECC Status											NFC_ECC_STS0		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	RSV	ECC_ERR_STS3		ECC_ERR_NUM3					RSV	ECC_ERR_STS2		ECC_ERR_NUM2				
Type	RO	RO		RO					RO	RO		RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RSV	ECC_ERR_STS1		ECC_ERR_NUM1					RSV	ECC_ERR_STS0		ECC_ERR_NUM0				
Type	RO	RO		RO					RO	RO		RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31]	RO	1'h0	Reserved
ECC_ERR_STS3	[22:21]	RO	2'h0	It indicates the 3rd ECC Error Status
ECC_ERR_NUM3	[28:24]	RO	5'h0	It indicates the 3rd ECC Error Numbers.
	[23]	RO	1'h0	Reserved
ECC_ERR_STS2	[22:21]	RO	2'h0	It indicates the 2nd ECC Error Status
ECC_ERR_NUM2	[20:16]	RO	5'h0	It indicates the 2nd ECC Error Numbers.
	[15]	RO	1'h0	Reserved
ECC_ERR_STS1	[14:13]	RO	2'h0	It indicates the 1st ECC Error Status
ECC_ERR_NUM1	[12:8]	RO	5'h0	It indicates the 1st ECC Error Numbers.
	[7]	RO	1'h0	Reserved
ECC_ERR_STS0	[6:5]	RO	2'h0	It indicates the 0th ECC Error Status **2'b00:** indicate jump out from SS step. (NO Error) **2'b01:** indicate jump from search done in internal CHIEN. (Errors can be corrected) **2'b10:** indicate jump from search done in last CHIEN. (Errors maybe not corrected) **2'b11:** indicate jump from ELP step.(Errors can't be corrected)
ECC_ERR_NUM0	[4:0]	RO	5'h0	It indicates the 0th ECC Error Numbers. **5'h0:** indicate no error **5'h1F:** indicate more errors that can't be correted. **>5'h0 and < 5'h1F:** indicate the error numbers.

Note:

When the ECC_ERR_NUM value is 0x00, then it means the corresponding sector's ECC is not decoded or there is no error occurred;

When the ECC_ERR_NUM is all 0x1F, then it means the corresponding sector's ECC is decoded and the error number is out of the capacity of the decoder.

When the ECC_ERR_NUM and ECC_ERR_STS registers are arranged in pairs, it have the different meanings: (suppose the ECC correct capacity is "t", and error number is "r")

ECC_ERR_STS	ECC_ERR_NUM	Status	Note
00	0	**No error**	When there are large amount errors, maybe this situation.
01	0 < r < t	**Errors in capacity**	
	= = t	Errors but not sure (in or out of capacity)	Not sure (especially for ECC mode0)
10	0 < r < t	**Errors in capacity**	
	= = t	Errors but not sure (in or out of capacity)	Not sure (especially for ECC mode1)
	= = 5'h1F	**Errors out of capacity**	
11	= = 5'h1F	**Errors out of capacity**	

5.3.6.2.12 NFC_ECC_STS1

Description: ECC result.

0x0044	ECC Status													NFC_ECC_STS1			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	RSV	ECC_ERR_STS7		ECC_ERR_NUM7					RSV	ECC_ERR_STS6		ECC_ERR_NUM6				
Type	RO	RO		RO					RO	RO		RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RSV	ECC_ERR_STS5		ECC_ERR_NUM5					RSV	ECC_ERR_STS4		ECC_ERR_NUM4				
Type	RO	RO		RO					RO	RO		RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31]	RO	1'h0	Reserved
ECC_ERR_STS7	[22:21]	RO	2'h0	It indicates the 7th ECC Error Status
ECC_ERR_NUM7	[28:24]	RO	5'h0	It indicates the 7th ECC Error Numbers.
	[23]	RO	1'h0	Reserved
ECC_ERR_STS6	[22:21]	RO	2'h0	It indicates the 6th ECC Error Status
ECC_ERR_NUM6	[20:16]	RO	5'h0	It indicates the 6th ECC Error Numbers.
	[15]	RO	1'h0	Reserved
ECC_ERR_STS5	[14:13]	RO	2'h0	It indicates the 5th ECC Error Status
ECC_ERR_NUM5	[12:8]	RO	5'h0	It indicates the 5th ECC Error Numbers.
	[7]	RO	1'h0	Reserved
ECC_ERR_STS4	[6:5]	RO	2'h0	It indicates the 4th ECC Error Status **2'b00:** indicate jump out from SS step. (NO Error)

				2'b01: indicate jump from search done in internal CHIEN. (Errors can be corrected) **2'b10:** indicate jump from search done in last CHIEN. (Errors maybe not corrected) **2'b11:** indicate jump from ELP step.(Errors can't be corrected)
ECC_ERR_NUM4	[4:0]	RO	5'h0	It indicates the 4th ECC Error Numbers. **5'h0:** indicate no error **5'h1F:** indicate more errors that can't be correted. **>5'h0 and < 5'h1F:** indicate the error numbers.

5.3.6.2.13 NFC_ECC_STS2

Description: ECC result.

0x0048	ECC Status															NFC_ECC_STS1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	RSV	ECC_ERR_STS11		ECC_ERR_NUM11					RSV	ECC_ERR_STS10		ECC_ERR_NUM10				
Type	RO	RO		RO					RO	RO		RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RSV	ECC_ERR_STS9		ECC_ERR_NUM9					RSV	ECC_ERR_STS8		ECC_ERR_NUM8				
Type	RO	RO		RO					RO	RO		RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31]	RO	1'h0	Reserved
ECC_ERR_STS11	[22:21]	RO	2'h0	It indicates the 11th ECC Error Status
ECC_ERR_NUM11	[28:24]	RO	5'h0	It indicates the 11th ECC Error Numbers.
	[23]	RO	1'h0	Reserved
ECC_ERR_STS10	[22:21]	RO	2'h0	It indicates the 10th ECC Error Status
ECC_ERR_NUM10	[20:16]	RO	5'h0	It indicates the 10th ECC Error Numbers.
	[15]	RO	1'h0	Reserved
ECC_ERR_STS9	[14:13]	RO	2'h0	It indicates the 9th ECC Error Status
ECC_ERR_NUM9	[12:8]	RO	5'h0	It indicates the 9th ECC Error Numbers.
	[7]	RO	1'h0	Reserved
ECC_ERR_STS8	[6:5]	RO	2'h0	It indicates the 8th ECC Error Status **2'b00:** indicate jump out from SS step. (NO Error) **2'b01:** indicate jump from search done in internal CHIEN. (Errors can be corrected) **2'b10:** indicate jump from search done in last CHIEN. (Errors maybe not corrected)

				2'b11: indicate jump from ELP step.(Errors can't be corrected)
ECC_ERR_NUM8	[4:0]	RO	5'h0	It indicates the 8th ECC Error Numbers. **5'h0:** indicate no error **5'h1F:** indicate more errors that can't be correted. **>5'h0 and < 5'h1F:** indicate the error numbers.

5.3.6.2.14 NFC_ECC_STS3

Description: ECC result.

0x004C			ECC Status										NFC_ECC_STS1			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	RSV	ECC_ERR_STS15		ECC_ERR_NUM15					RSV	ECC_ERR_STS14		ECC_ERR_NUM14				
Type	RO	RO		RO					RO	RO		RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RSV	ECC_ERR_STS13		ECC_ERR_NUM13					RSV	ECC_ERR_STS12		ECC_ERR_NUM12				
Type	RO	RO		RO					RO	RO		RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31]	RO	1'h0	Reserved
ECC_ERR_STS15	[22:21]	RO	2'h0	It indicates the 15th ECC Error Status
ECC_ERR_NUM15	[28:24]	RO	5'h0	It indicates the 15th ECC Error Numbers.
	[23]	RO	1'h0	Reserved
ECC_ERR_STS14	[22:21]	RO	2'h0	It indicates the 14th ECC Error Status
ECC_ERR_NUM14	[20:16]	RO	5'h0	It indicates the 14th ECC Error Numbers.
	[15]	RO	1'h0	Reserved
ECC_ERR_STS13	[14:13]	RO	2'h0	It indicates the 13th ECC Error Status
ECC_ERR_NUM13	[12:8]	RO	5'h0	It indicates the 13th ECC Error Numbers.
	[7]	RO	1'h0	Reserved
ECC_ERR_STS12	[6:5]	RO	2'h0	It indicates the 12th ECC Error Status **2'b00:** indicate jump out from SS step. (NO Error) **2'b01:** indicate jump from search done in internal CHIEN. (Errors can be corrected) **2'b10:** indicate jump from search done in last CHIEN. (Errors maybe not corrected) **2'b11:** indicate jump from ELP step.(Errors can't be corrected)

ECC_ERR_NUM12	[4:0]	RO	5'h0	It indicates the 12th ECC Error Numbers. **5'h0:** indicate no error **5'h1F:** indicate more errors that can't be correted. **>5'h0 and < 5'h1F:** indicate the error numbers.

5.3.6.2.15 NFC_START_ADDRx

Description: Start address for the x(0~7) page operation

0x0060	**Start address for the 0th page operation / Micro-Instruction Registers 0**	**NFC_START_ADDR0**
0x0064	**Start address for the 1st page operation / Micro-Instruction Registers 1**	**NFC_START_ADDR1**
0x0068	**Start address for the 2nd page operation / Micro-Instruction Registers 2**	**NFC_START_ADDR2**
0x006C	**Start address for the 3rd page operation / Micro-Instruction Registers 3**	**NFC_START_ADDR3**
0x0070	**Start address for the 4th page operation / Micro-Instruction Registers 4**	**NFC_START_ADDR4**
0x0074	**Start address for the 5th page operation / Micro-Instruction Registers 5**	**NFC_START_ADDR5**
0x0078	**Start address for the 6th page operation / Micro-Instruction Registers 6**	**NFC_START_ADDR6**
0x007C	**Start address for the 7th page operation / Micro-Instruction Registers 7**	**NFC_START_ADDR7**

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	START_ADDRx															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	START_ADDRx															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
START_ADDRx	[31:0]	R/W	32'h0	Start address for the x(0~7) page operation, or the Micro-Instruction Register x(0~7)

5.3.6.2.16 NFC_END_ADDRx

Description: End address for the x(0~7) page operation

0x0080			**End address for the 0th page operation / Micro-Instruction Registers 8**												**NFC_END_ADDR0**	
0x0084			**End address for the 1st page operation / Micro-Instruction Registers 9**												**NFC_END_ADDR1**	
0x0088			**End address for the 2nd page operation / Micro-Instruction Registers 10**												**NFC_END_ADDR2**	
0x008C			**End address for the 3rd page operation / Micro-Instruction Registers 11**												**NFC_END_ADDR3**	
0x0090			**End address for the 4th page operation / Micro-Instruction Registers 12**												**NFC_END_ADDR4**	
0x0094			**End address for the 5th page operation / Micro-Instruction Registers 13**												**NFC_END_ADDR5**	
0x0098			**End address for the 6th page operation / Micro-Instruction Registers 14**												**NFC_END_ADDR6**	
0x009C			**End address for the 7th page operation / Micro-Instruction Registers 15**												**NFC_END_ADDR7**	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	END_ADDRx															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	END_ADDRx															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
END_ADDRx	[31:0]	R/W	32'h0	End address for the x(0~7) page operation or the Micro-Instruction Register x(8~15)

5.3.7 ECC

SC6820 NAND Flash Controller consist one powerful internal error checking and correcting module. It supports configurations of different parameters including coding size, redundancy size, and correct capacity.

Main function is to checking and correcting errors when read and write nand flash. When write (or program) nand flash, starting this module to encode the written data and save the encode data to the spare area; when read nand flash, starting this module to decode the read data and correct the error data.

In this module, the ECC support 1~ 1K bytes information bits ECC encoder and decoder. The supported information and redundancies configuration as following:

ECC MODE	Correct-capacity	Redundancies bits	Notes
0	1 bits	14	Info size 1 ~ 1K Bytes
1	2 bits	28	Info size 1 ~ 1K Bytes
2	4 bits	56	Info size 1 ~ 1K Bytes
3	8 bits	112	Info size 1 ~ 1K Bytes
4	12 bits	168	Info size 1 ~ 1K Bytes
5	16 bits	224	Info size 1 ~ 1K Bytes
6	24 bits	336	Info size 1 ~ 1K Bytes

For detail information about ECC module, please refer to *"SC6820 ECC Module Design Specification"*

5.3.8 Application Notes

Before configure module, set some global parameters,

Set bit[8] of 0x2090_0200 to enable NFC clock;

Set or reset bit[5] of 0x2090_0210 to reset NFC module;

5.3.8.1 Non-DMA fixed-sequence Program Flow

For programming:

1. Software write data to the internal main buffer (0x6000_2000) and spare buffer (0x6000_4000).
2. Set **NFC_CFG0** for basic parameters including: MEM_NFC_SWITCH, DEV_BUS_SIZE, CS_SEL, PAGE_TYPE, ADD_CYCLE, ADVANCE, NFC_CMD_SET = 0, NFC_SP_SIZE. Also NFC_WPN should be set 1 to un-protect the Nand
3. For different NAND, the timing parameters are different, the **NFC_TIMING** register should be set relatively
4. Set **NFC_START_ADDR**0 ~ 7 and **NFC_END_ADDR**0~7 to indicate the start and end address which will be write to.
5. If ECC function is used, the **NFC_ECC_CFG0** and **NFC_ECC_CFG1** should be set to configure the ECC parameters including: ECC_DECODE, ECC_SP_ENDIAN, ECC_MODE, ECC_NUM, ECC_SEC_SIZE, ECC_SEC_POS and ECC_INFO_SIZE. if the automatic way is selected, the ECC_AUTO_EN register should be set to 1. The ECC_ACTIVE_EN will used if one manual calculate the ECC and used this function independly.
6. Set **NFC_INT_STS_EN** register, for basic function, the INT_NFC_DONE_EN should set 1. The INT_ECC_DONE_EN can be omitted either the ECC function is used or not in programming nand process.
7. Write **NFC_CMD** register to start the programming process with BLK_NUM inside.
8. After the INT_NFC_DONE interrupt is occurred, the programming is done.

5.3.8.2 Non-DMA fixed-sequence read Flow

For reading:

1. Set **NFC_CFG0** for basic parameters including: MEM_NFC_SWITCH, DEV_BUS_SIZE, CS_SEL, PAGE_TYPE, ADD_CYCLE, ADVANCE, NFC_CMD_SET = 0, NFC_SP_SIZE. Also NFC_WPN should be set 1 to un-protect the Nand
2. For different NAND, the timing parameters are different, the **NFC_TIMING** register should be set relatively
3. Set **NFC_START_ADDR**0 ~ 7 and **NFC_END_ADDR**0~7 to indicate the start and end address which will be write to.
4. If ECC function is used, the **NFC_ECC_CFG0** and **NFC_ECC_CFG1** should be set to configure the ECC parameters including: ECC_DECODE, ECC_SP_ENDIAN, ECC_MODE, ECC_NUM, ECC_SEC_SIZE, ECC_SEC_POS and ECC_INFO_SIZE. if the automatic way is selected, the ECC_AUTO_EN register should be set to 1. The ECC_ACTIVE_EN will used if one manual calculate the ECC and used this function independly.
5. Set **NFC_INT_STS_EN** register, for basic function, the INT_NFC_DONE_EN should set 1. If ECC is used , the INT_ECC_DONE_EN should be set
6. Write **NFC_CMD** register to start the programming process with BLK_NUM inside.
7. If ECC_AUTO_EN is set, after the INT_ECC_DONE interrupt is occurred, the read is done; then after the INT_NFC_DONE interrupt is occurred , the read is done.
8. Software read data from the internal main buffer (0x6000_2000) and spare buffer (0x6000_4000).

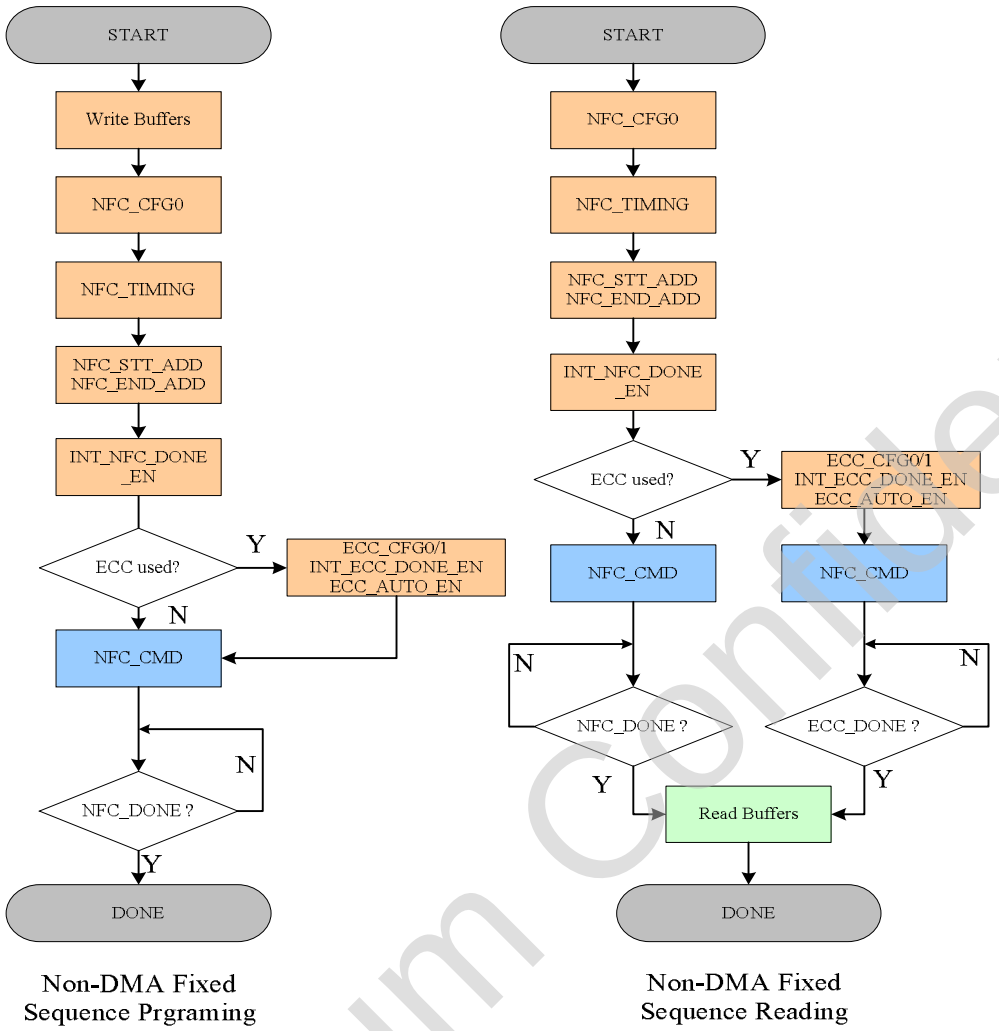


Figure 5.3-5 NFC Non-DMA Fixed Sequence

5.3.8.3 Non-DMA Micro- Code Programming Flow

For programming:

1. Software write data to the internal main buffer (0x6000_2000) and spare buffer (0x6000_4000).
2. If ECC function is used, the **NFC_ECC_CFG0** and **NFC_ECC_CFG1** should be set to configure the ECC parameters including: ECC_DECODE, ECC_SP_ENDIAN, ECC_MODE, ECC_NUM, ECC_SEC_SIZE, ECC_SEC_POS and ECC_INFO_SIZE. In micro-code mode, the ECC automatically way cannot be used. Software should write ECC_ACTIVE_EN to manually start the ECC function.
3. After the ECC is done, software should copy the spare buffer data to the heel of data of main buffer.
4. Set **NFC_CFG0** for basic parameters including: MEM_NFC_SWITCH, DEV_BUS_SIZE, CS_SEL, ~~PAGE_TYPE~~, ~~ADD_CYCLE~~, ~~ADVANCE~~, NFC_CMD_SET = 1, ~~NFC_SP_SIZE~~. Also NFC_WPN should be set 1 to un-protect the Nand
5. For different NAND, the timing parameters are different, the **NFC_TIMING** register should be set relatively

6. For Micro-code mode, the address registers are act as Micro-Instruction Registers, Software write these registers based on the selected NAND command/address/data sequence, the code number will be set on the **NFC_CMD** registers
7. Set **NFC_INT_STS_EN** register, for basic function, the INT_NFC_DONE_EN should set 1.
8. Write **NFC_CMD** register to start the programming process with INST_NUM inside.
9. After the INT_NFC_DONE interrupt is occurred, the programming is done.

5.3.8.4 Non-DMA Micro- Code Reading Flow

For reading:

1. Set **NFC_CFG0** for basic parameters including: MEM_NFC_SWITCH, DEV_BUS_SIZE, CS_SEL, ~~PAGE_TYPE~~, ~~ADD_CYCLE~~, ~~ADVANCE~~, NFC_CMD_SET = 1, ~~NFC_SP_SIZE~~.
2. For different NAND, the timing parameters are different, the **NFC_TIMING** register should be set relatively
3. For Micro-code mode, the address registers are act as Micro-Instruction Registers, Software write these registers based on the selected NAND command/address/data sequence, the code number will be set on the **NFC_CMD** registers
4. Set **NFC_INT_STS_EN** register, for basic function, the INT_NFC_DONE_EN should set 1.
5. Write **NFC_CMD** register to start the programming process with INST_NUM inside.
6. Wait the ECC is done
7. If ECC is used,software should copy the heel date of main buffer to spare buffer.
8. If ECC function is used, the **NFC_ECC_CFG0** and **NFC_ECC_CFG1** should be set to configure the ECC parameters including: ECC_DECODE, ECC_SP_ENDIAN, ECC_MODE, ECC_NUM, ECC_SEC_SIZE, ECC_SEC_POS and ECC_INFO_SIZE. In micro-code mode, the ECC automatically way cannot be used. Software should write ECC_ACTIVE_EN to manually start the ECC function.
9. After the INT_NFC_DONE interrupt is occurred, the reading is done.
10. Software read data from the internal main buffer (0x6000_2000) and spare buffer (0x6000_4000).

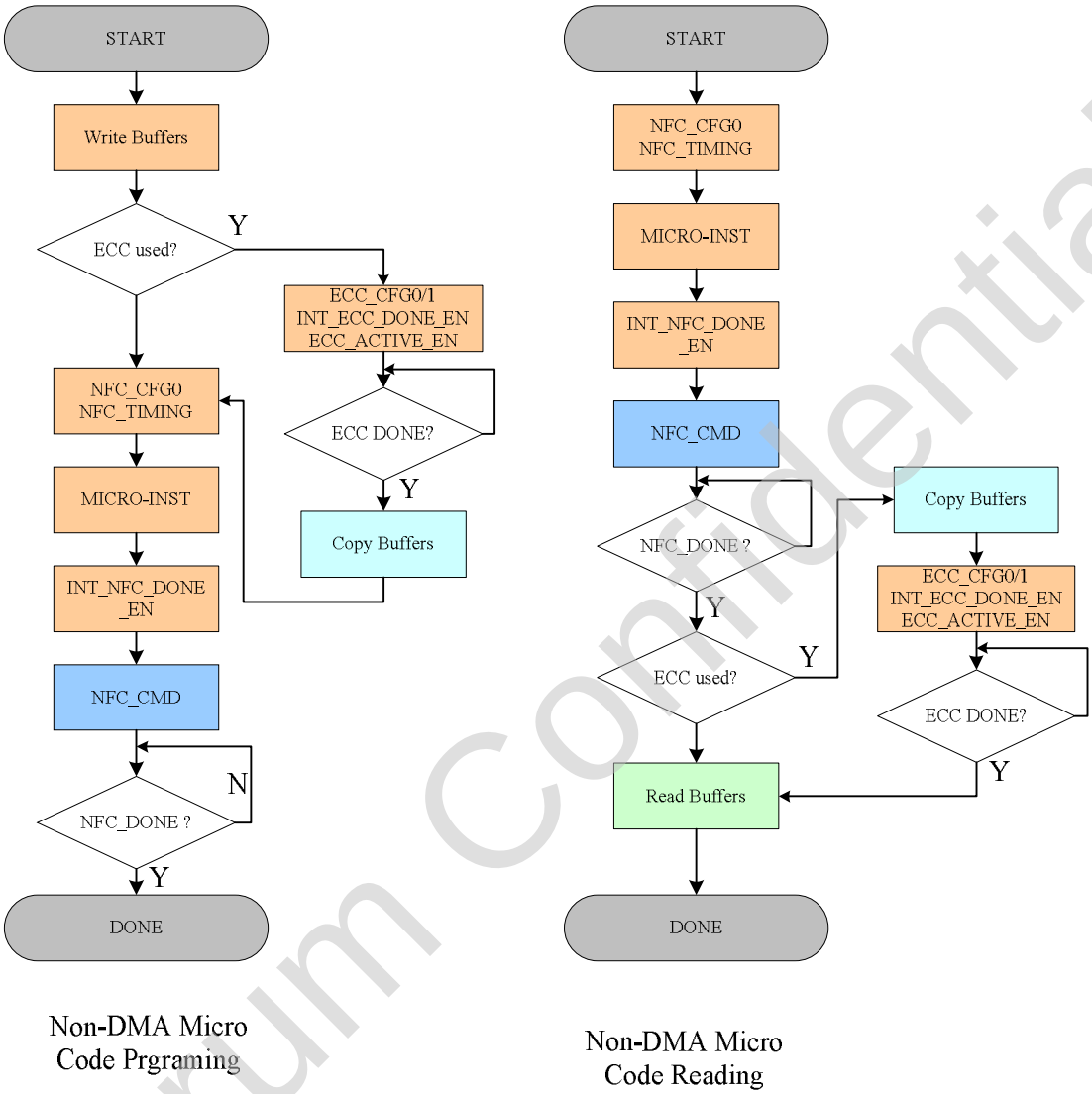


Figure 5.3-6 NFC Non-DMA Micro Code

5.3.8.5 DMA fixed-sequence Program Flow

For programming:

1. Configure the DMA channel parameters, where the DMA target address is 0x6000_2000 and linked target address is 0x6000_4000
2. Set **NFC_CFG0** for basic parameters including: MEM_NFC_SWITCH, DEV_BUS_SIZE, CS_SEL, PAGE_TYPE, ADD_CYCLE, ADVANCE, NFC_CMD_SET = 0, NFC_SP_SIZE. Also NFC_WPN should be set 1 to un-protect the Nand
3. Set DMA_TX_EN of **NFC_CFG1** to enable the hardware DMA transfer.
4. For different NAND, the timing parameters are different, the **NFC_TIMING** register should be set relatively
5. Set **NFC_START_ADDR**0 ~ 7 and **NFC_END_ADDR**0~7 to indicate the start and end address which will be write to.

6. If ECC function is used, the **NFC_ECC_CFG0** and **NFC_ECC_CFG1** should be set to configure the ECC parameters including: ECC_DECODE, ECC_SP_ENDIAN, ECC_MODE, ECC_NUM, ECC_SEC_SIZE, ECC_SEC_POS and ECC_INFO_SIZE. if the automatic way is selected, the ECC_AUTO_EN register should be set to 1. The ECC_ACTIVE_EN will used if one manual calculate the ECC and used this function independly.
7. Set **NFC_INT_STS_EN** register, for basic function, the INT_NFC_DONE_EN should set 1. The INT_ECC_DONE_EN can be omitted either the ECC function is used or not in programming nand process.
8. Write **NFC_CMD** register to start the programming process with BLK_NUM inside.
9. After the INT_NFC_DONE interrupt is occurred, the programming is done.

5.3.8.6 DMA fixed-sequence read Flow

For reading:

1. Configure the DMA channel parameters, where the DMA source address is 0x6000_2000 and linked source address is 0x6000_4000
2. Set **NFC_CFG0** for basic parameters including: MEM_NFC_SWITCH, DEV_BUS_SIZE, CS_SEL, PAGE_TYPE, ADD_CYCLE, ADVANCE, NFC_CMD_SET = 0, NFC_SP_SIZE. Also NFC_WPN should be set 1 to un-protect the Nand
3. Set DMA_RX_EN of **NFC_CFG1** to enable the hardware DMA receiving.
4. For different NAND, the timing parameters are different, the **NFC_TIMING** register should be set relatively
5. Set **NFC_START_ADDR**0 ~ 7 and **NFC_END_ADDR**0~7 to indicate the start and end address which will be write to.
6. If ECC function is used, the **NFC_ECC_CFG0** and **NFC_ECC_CFG1** should be set to configure the ECC parameters including: ECC_DECODE, ECC_SP_ENDIAN, ECC_MODE, ECC_NUM, ECC_SEC_SIZE, ECC_SEC_POS and ECC_INFO_SIZE. if the automatic way is selected, the ECC_AUTO_EN register should be set to 1. The ECC_ACTIVE_EN will used if one manual calculate the ECC and used this function independly.
7. Set **NFC_INT_STS_EN** register, for basic function, the INT_NFC_DONE_EN should set 1. If ECC is used , the INT_ECC_DONE_EN should be set
8. Write **NFC_CMD** register to start the programming process with BLK_NUM inside.
9. After the DMA_DONE is occurred, then the reading process is done.

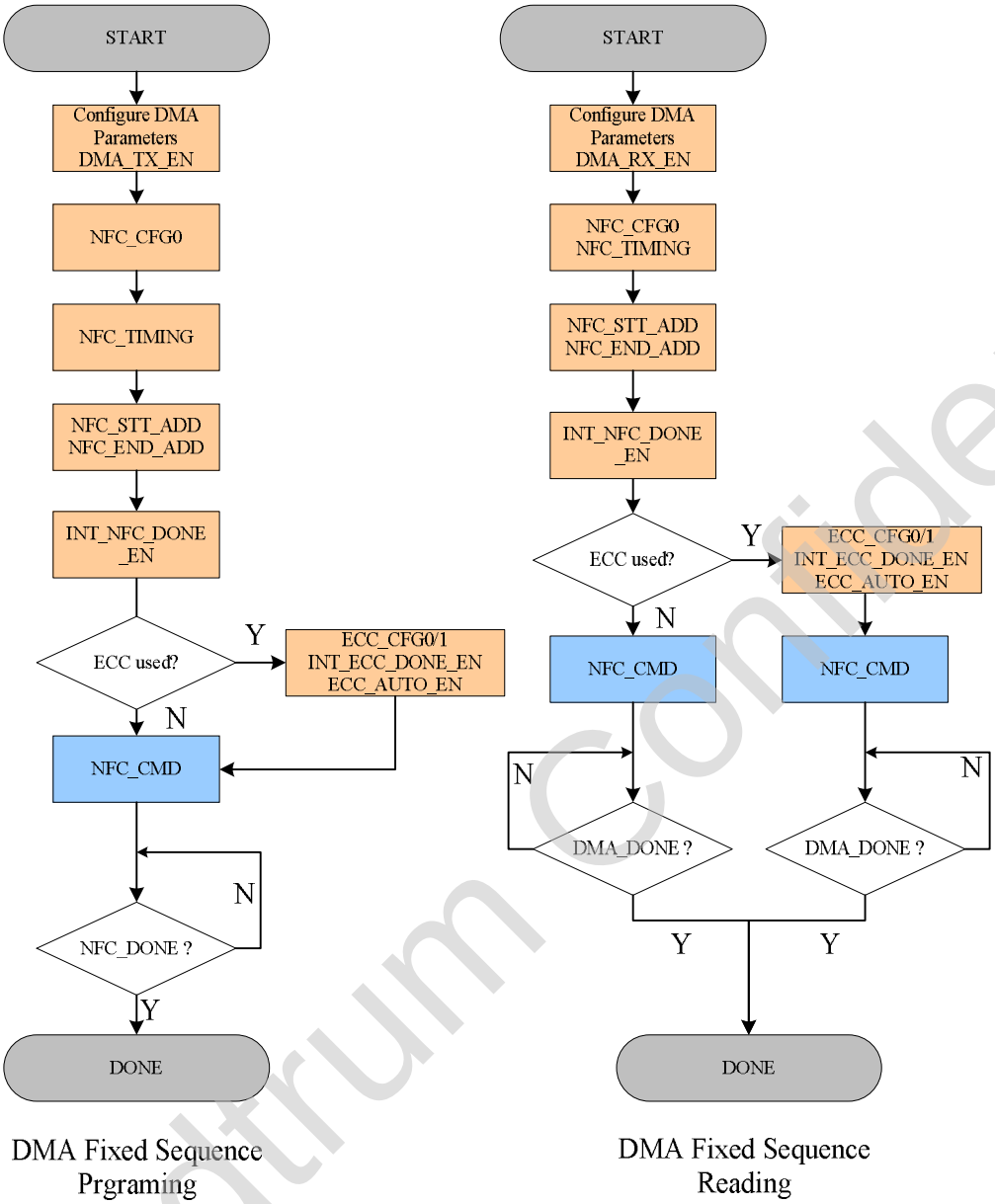


Figure 5.3-7 NFC DMA Fixed Sequence

5.3.8.7 DMA Micro- Code Programming Flow

For programming:

1. Configure the DMA channel parameters, where the DMA target address is 0x6000_2000
2. Set DMA_TX_EN of **NFC_CFG1** to enable the hardware DMA transfer and start DMA.
3. Wait for the DMA_DONE interrupt.
4. If ECC function is used, the **NFC_ECC_CFG0** and **NFC_ECC_CFG1** should be set to configure the ECC parameters including: ECC_DECODE, ECC_SP_ENDIAN, ECC_MODE, ECC_NUM, ECC_SEC_SIZE, ECC_SEC_POS and ECC_INFO_SIZE. In micro-code mode, the ECC

automatically way cannot be used. Software should write ECC_ACTIVE_EN to manually start the ECC function.

5. After the ECC is done, software should copy the spare buffer data to the heel of data of main buffer.
6. Set **NFC_CFG0** for basic parameters including: MEM_NFC_SWITCH, DEV_BUS_SIZE, CS_SEL, ~~PAGE_TYPE~~, ~~ADD_CYCLE~~, ~~ADVANCE~~, NFC_CMD_SET = 1, ~~NFC_SP_SIZE~~. Also NFC_WPN should be set 1 to un-protect the Nand
7. For different NAND, the timing parameters are different, the **NFC_TIMING** register should be set relatively
8. For Micro-code mode, the address registers are act as Micro-Instruction Registers, Software write these registers based on the selected NAND command/address/data sequence, the code number will be set on the **NFC_CMD** registers
9. Set **NFC_INT_STS_EN** register, for basic function, the INT_NFC_DONE_EN should set 1.
10. Write **NFC_CMD** register to start the programming process with INST_NUM inside.
11. After the INT_NFC_DONE interrupt is occurred, the programming is done.

5.3.8.8 DMA Micro-Code Reading Flow

For reading:

1. Configure the DMA channel parameters, where the DMA source address is 0x6000_2000 and linked source address is 0x6000_4000
2. Set DMA_RX_EN of **NFC_CFG1** to enable the hardware DMA receiving
3. Set **NFC_CFG0** for basic parameters including: MEM_NFC_SWITCH, DEV_BUS_SIZE, CS_SEL, ~~PAGE_TYPE~~, ~~ADD_CYCLE~~, ~~ADVANCE~~, NFC_CMD_SET = 1, ~~NFC_SP_SIZE~~.
4. For different NAND, the timing parameters are different, the **NFC_TIMING** register should be set relatively
5. For Micro-code mode, the address registers are act as Micro-Instruction Registers, Software write these registers based on the selected NAND command/address/data sequence, the code number will be set on the **NFC_CMD** registers
6. Set **NFC_INT_STS_EN** register, for basic function, the INT_NFC_DONE_EN should set 1.
7. Write **NFC_CMD** register to start the programming process with INST_NUM inside.
8. Wait the ECC is done
9. If ECC is used,software should copy the heel date of main buffer to spare buffer.
10. If ECC function is used, the **NFC_ECC_CFG0** and **NFC_ECC_CFG1** should be set to configure the ECC parameters including: ECC_DECODE, ECC_SP_ENDIAN, ECC_MODE, ECC_NUM, ECC_SEC_SIZE, ECC_SEC_POS and ECC_INFO_SIZE. In micro-code mode, the ECC automatically way cannot be used. Software should write ECC_ACTIVE_EN to manually start the ECC function.
11. After the INT_NFC_DONE interrupt is occurred, the reading is done.
12. Start DMA
13. Wait for the DMA_DONE interrupt.

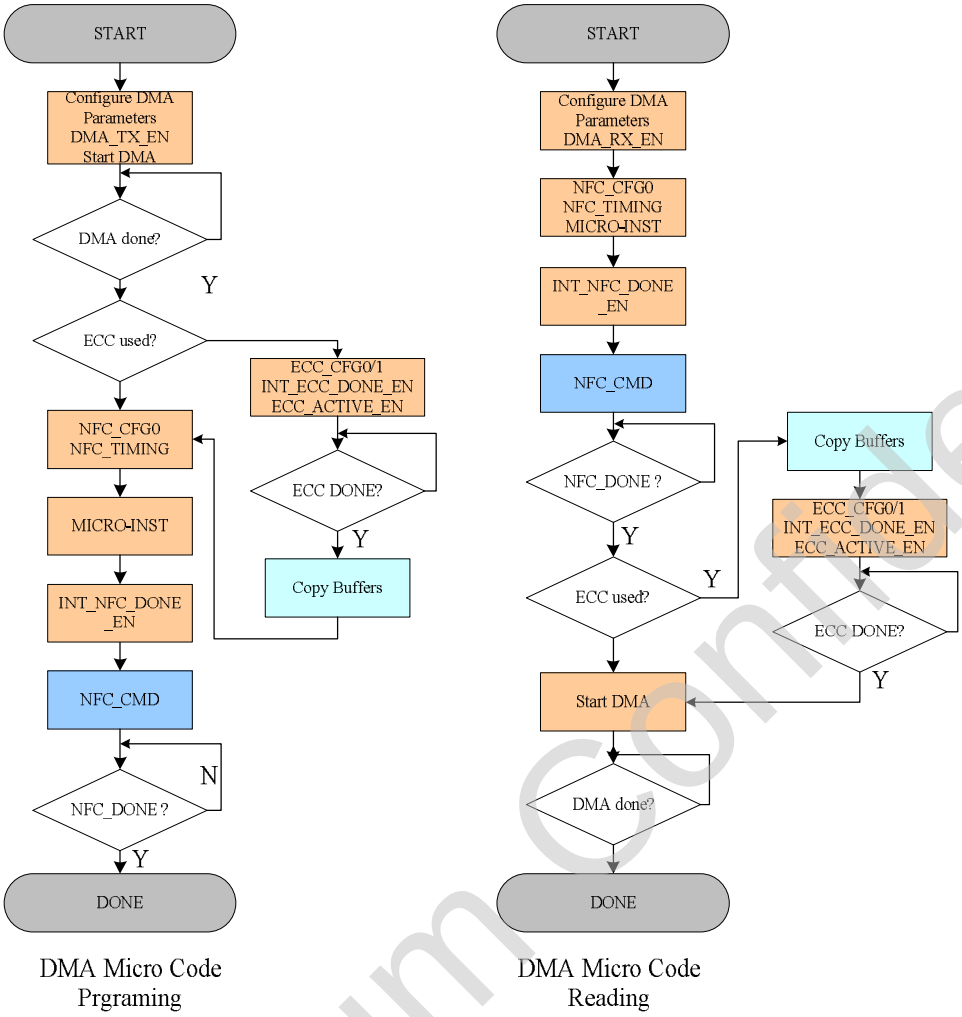


Figure 5.3-8 NFC DMA Micro Code

5.4 DMA Controller

5.4.1 Overview

The Direct Memory Access (DMA) controller is used to accelerate data transfer between different peripherals and memories without processor core's intervention. 32-channel AHB-based DMA controller improves data transfer efficiency.

This controller can also support several work modes. The DMA controller support a 2-D transfer which means a total transfer is divided into several blocks and each request only responded with one block transfer.

5.4.2 Features

- 32 channels. Each channel can be enabled and configured independently
- 4-level priority. Priority can be configured independently for each channel. The channels with the same priority are selected with robin-round algorithm
- Configurable block wait time

- 28 channels are used by hardware, and the other 4 channels can be used dedicatedly as software request
- Each channel can be configured as whole transfer executed after one request or one block executed after one request
- Each channel can be configured in normal mode
- Each channel can be configured in linked list mode
- Each channel can be configured in infinite burst mode
- The transfer support both byte (8 bit), half-word (16 bit) and word (32 bit). If in word format, a user can re-arrange the byte sequence beyond a word to adapt for different system requirement
- Each channel can be programmed to allocate a channel user identity (UID), which can be used to calculate this user's "channel control register" base-address.

5.4.3 Function Description

The Direct Memory Access （DMA） is essential part of both DSP platform and ARM processor platform, and in both platform it is used to accelerate data transfer between the different peripherals and memories, without any DSP/ARM core intervention.

DMA transfer is carried out in either an untouched data format or in a restructured data format, depending on the requirements of the particular applications.

DMA controller has two masters, one is dedicated for read operation and the other is dedicated for write, supporting reading and writing data simultaneously on differently layers.

5.4.3.1 DMA Channel Description

The DMA controller supports 32 logic channels and each channel can be enabled and configured independently.

For hardware-request, the sources are from different clock domains, the synchronization logic for requests and acknowledges are implemented in the DMA controller.

5.4.3.2 DMA Work Modes

The DMA contains 32 independent programmable logic channels that support 32 different applications at the same time. Besides, for each channel, it can work in normal mode, linked list mode or soft list mode according to the applications.

"Normal Mode". In Normal mode, the channel will be initialized, configured and enabled by software. After receiving request from hardware or software, DMA begin to transfer a block, or the total data according to the configuration information.

"Linked List Mode". In Linked List mode, the channel will be initialized and enabled by software. While in the selected channel, nothing but an address pointer is valid. Base on the linked list pointer, DMA can load the channel configuratoin information by itself, and begin to transfer according to the newly loaded configuration. If the newly loaded configuration information has the "LLEnd" bit active, then this means that it is the last node of the linked list. And if "LLEnd" is set active, the bit "DMAChnLLPtr" is invalid.

"Soft List Mode". In Soft List mode, the channel will be initialized and enable by software. Besides, software also needs to maintain a list out side of DMA. Each node

of the list contains 8-word full channel configuration information. Software will let DMA know the list base address and the list size and how many nodes are there in the list. DMA will automatically load the channel configuration information as long as the list counter is nonzero.

5.4.3.3 Two-Dimensional Transfer

A 2-Dimension transfer divides a whole transfer length into several transfer blocks. One block will be transferred after one request. The transfer block also composed of several elements. An “element” is an atomic unit of a burst transfer, which can be byte, half-word or word. A user can place a gap between the boundary of elements or blocks, which means an address leap is supported during burst transfer.

5.4.3.4 Channel Arbitration

The DMA controller provides configurable 4-level priority for each channel in register DMA_PRIORITY0 or DMA_PRIORITY1, and each channel can be configured independently in one of the four priority levels.

The channel with higher priority is always granted more early than the channel with lower priority – 3 > 2 > 1 > 0.

The channels with the same priority are granted by robin-round rule.

5.4.3.5 DMA Interrupt Description

For each channel, there are two interrupt sources: the whole transfer completed interrupt and one burst completed interrupt. Each interrupt source can be enabled or disabled. The masked and raw interrupt status can be read and cleared through AHB.

For linked list mode, the whole transfer completed interrupt indicates all linked list nodes are completed.

5.4.4 DMA Logic Request Channels

There are totally 32 logic request channels in arm side, 16 logic request channels in dsp side. Once a channel is allocated with a UID, then the base-address of “channel control register” can be calculated as follows (n is channel number).

0x2010_0400 + 0x0020*n,

Table 5-2 DMA logci request channels

UID	Channel User	Description
1	UART0 TX	UART0 TX request
2	UART0 RX	UART0 RX request
3	UART1 TX	UART1 TX request
4	UART1 RX	UART1 RX request
5	UART2 TX	UART2 TX request
6	UART2 RX	UART2 RX request
7	IIS0 TX	IIS0 TX request
8	IIS0 RX	IIS0 RX request
9	EPT_RX	EPT RX request

UID	Channel User	Description
10	EPT_TX	EPT TX request
11	VB DA0	VBC DAC0 TX request
12	VB DA1	VBC DAC1 TX request
13	VB AD0	VBC ADC0 TX request
14	VB AD1	VBC ADC1 TX request
15	SIM0 TX	SIM 0 TX request
16	SIM0 RX	SIM 0 RX request
17	SIM1 TX	SIM 1 TX request
18	SIM1 RX	SIM 1 RX request
19	SPI0 TX	SPI0 TX request
20	SPI0 RX	SPI0 RX request
21	ROT	Rotation request
22	SPI1 TX	SPI1 TX request
23	SPI1 RX	SPI1 RX request
24	IIS1 TX	IIS1 TX request
25	IIS1 RX	IIS1 RX request
26	NFC TX	NFC TX request
27	NFC RX	NFC RX request
28		
29	DRM RAW	DRM raw request
30	DRM CPT	DRM cpt request
31		
32		

Note:

The UID is fixed by AISC, while the Channel User is configurable; Each UID can be configured to complete anyone of the 32 Channel User's function.

5.4.5 Control Registers

5.4.5.1 Memory map

ARM base address: 0x2010_0000

Offset Addr	Register Name	Register Description
0x0000	DMA_BLK_WAIT	Block Wait time register
0x0004	DMA_CHN_EN_STATUS	Channel enable register
0x0008	DMA_LINK_LIST_EN	Link List Mode enable register

Offset Addr	Register Name	Register Description
0x000C	DMA_SOFT_LIST_EN	Soft List Mode enable register
0x0010	DMA_SOFT_LIST_SIZE	Soft List size register
0x0014	DMA_SOFT_LIST_CMD	Soft list command register
0x0018	DMA_SOFT_LIST_STATUS	Soft list mode status register
0x001C	DMA_SOFT_LIST_BADDR	Base address register of soft list mode
0x0020	DMA_PRI_CFG0	Channel Priority register
0x0024	DMA_PRI_CFG1	Channel Priority register
0x0028	Reserved.	
0x002C	Reserved.	
0x0030	DMA_INT_MASK_STATUS	DMA Masked interrupt status register
0x0034	DMA_INT_RAW_STATUS	DMA Raw interrupt status register
0x0038	Reserved.	
0x003C	Reserved.	
0x0040	DMA_LLIST_DONE_INT_EN	Interrupt enable register of Link list done.
0x0044	DMA_BLOCK_DONE_INT_EN	Interrupt enable register of Burst done
0x0048	DMA_TRANS_DONE_INT_EN	Interrupt enable register of Transaction done
0x004C	Reserved.	
0x0050	DMA_LLIST_DONE_ INT_ MASK_STATUS	Masked status of Link list done interrupt.
0x0054	DMA_BLOCK_DONE_INT_MASK_STATUS	Masked status of block done interrupt.
0x0058	DMA_TRANS_DONE_INT_MASK_STATUS	Masked status of Transaction done interrupt
0x005C	Reserved.	
0x0060	DMA_LLIST_DONE_ INT_ RAW_STATUS	Raw status of Link List done interrupt.
0x0064	DMA_BLOCK_DONE_INT_ RAW _STATUS	Raw status of BLock done interrupt.
0x0068	DMA_TRANS_DONE_INT_ RAW _STATUS	Raw status of Transaction done interrupt.

Offset Addr	Register Name	Register Description
0x006C	Reserved.	
0x0070	DMA_LLIST_DONE_ INT_ CLR	Clear interrupt of Link List done
0x0074	DMA_BURST_DONE_INT_ CLR	Clear interrupt of Burst done.
0x0078	DMA_TRANS_DONE_INT_ CLR	Clear interrupt of Transaction done.
0x007C	Reserved.	
0x0080	DMA_SOFT_REQ	Soft channel request
0x0084	DMA_STATUS	DMA Status
0x0088	DMA_REQ_PEND	Pending request status.
0x008C	Reserved.	
0x0090	DMA_WRAP_START_ADDR	Start address of WRAP mode.
0x0094	DMA_WRAP_END_ADDR	End address of WRAP mode.
0x0098	DMA_CHN_UID_CFG0	User ID of channels
0x009C	DMA_CHN_UID_CFG1	User ID of channels
0x00A0	DMA_CHN_UID_CFG2	User ID of channels
0x00A4	DMA_CHN_UID_CFG3	User ID of channels
0x00A8	DMA_CHN_UID_CFG4	User ID of channels
0x00AC	DMA_CHN_UID_CFG5	User ID of channels
0x00B0	DMA_CHN_UID_CFG6	User ID of channels
0x00B4	Reserved.	
0x00B8	Reserved.	
0x00BC	Reserved.	
0x00C0	DMA_CHN_EN_SET	User ID of channels
0x00C4	DMA_CHN_EN_CLR	User ID of channels
0x00C8-0x0400	Reserved.	
0x0400	CHN0_CFG	Channel 0 configure register
0x0404	CHN0_TOTAL_LEN	Channel 0 total length
0x0408	CHN0_SRC_ADDR	Channel 0 Source Address
0x040C	CHN0_DEST_ADDR	Channel 0 Destination Address
0x0410	CHN0_LLIST_PTR	Channel 0 Link list pointer address

Offset Addr	Register Name	Register Description
0x0414	CHN0_ELEM_POSTM	Channel 0 Element post-modification
0x0418	CHN0_SRC_BLOCK_POSTM	Channel 0 Source Block post-modification
0x041C	CHN0_DEST_BLOCK_POSTM	Channel 0 Destination Block post-modification
0x0420-0x043C	Channel 1 configure register, definition as channel 0.	
0x0440-0x045C	Channel 2 configure register, definition as channel 0.	
0x0460-0x047C	Channel 3 configure register, definition as channel 0.	
0x0480-0x049C	Channel 4 configure register, definition as channel 0.	
0x0480-0x049C	Channel 4 configure register, definition as channel 0.	
0x04A0-0x04BC	Channel 5 configure register, definition as channel 0.	
0x04C0-0x04DC	Channel 6 configure register, definition as channel 0.	
0x04E0-0x04FC	Channel 7 configures register, definition as channel 0.	
0x0500-0x051C	Channel 8 configure register, definition as channel 0.	
0x0520-0x053C	Channel 9 configure register, definition as channel 0.	
0x0540-0x055C	Channel 10 configure register, definition as channel 0.	
0x0560-0x057C	Channel 11 configure register, definition as channel 0.	
0x0580-0x059C	Channel 12 configure register, definition as channel 0.	
0x05A0-0x05BC	Channel 13 configure register, definition as channel 0.	
0x05C0-0x05DC	Channel 14 configure register, definition as channel 0.	
0x05E0-0x05FC	Channel 15 configure register, definition as channel 0.	
0x0600-0x061C	Channel 16 configure register, definition as channel 0.	
0x0620-	Channel 17 configure register, definition as	

Offset Addr	Register Name	Register Description
0x063C	channel 0.	
0x0640-0x065C	Channel 18 configure register, definition as channel 0.	
0x0660-0x067C	Channel 19 configure register, definition as channel 0.	
0x0680-0x069C	Channel 20 configure register, definition as channel 0.	
0x06A0-0x06BC	Channel 21 configure register, definition as channel 0.	
0x06C0-0x06DC	Channel 22 configure register, definition as channel 0.	
0x06E0-0x06FC	Channel 23 configure register, definition as channel 0.	
0x0700-0x071C	Channel 24 configure register, definition as channel 0.	
0x0720-0x073C	Channel 25 configure register, definition as channel 0.	
0x0740-0x075C	Channel 26 configure register, definition as channel 0.	
0x0760-0x077C	Channel 27 configure register, definition as channel 0.	
0x0780-0x079C	Channel 28 configure register, definition as channel 0.	
0x07A0-0x07BC	Channel 29 configure register, definition as channel 0.	
0x07C0-0x07DC	Channel 30 configure register, definition as channel 0.	
0x07E0-0x07FC	Channel 31 configure register, definition as channel 0.	

5.4.5.2 Register Descriptions

5.4.5.2.1 DMA_BLK_WAIT

Description： Block Wait time register

0x0000			Block Wait time register (reset 0x0000_0000)										DMA_BLK_WAIT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SOFT_BLOCK_WAIT															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							PAUSE_REQ	HARD_BLOCK_WAIT							
Type	RO							R/W	R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
SOFT_BLOCK_WAIT	[31:16]	R/W	16'h0	The software channel waiting time between the data transfer burst. The unit is HCLK cycle.
	[15:9]	RO	7'h0	Reserved
PAUSE_REQ	[8]	R/W	1'h0	Active high, Request to pause DMA;
HARD_BLOCK_WAIT	[7:0]	R/W	8'h0	The hardware channel waiting time between the data transfer burst. The unit is HCLK cycle

5.4.5.2.2 DMA_CHN_EN_STATUS

Description： Channels enable status register

0x0004			Channel enable status register (reset 0x0000_0000)										DMA_CHN_EN_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	CHN_EN_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHN_EN_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
CHN_EN_STATUS	[31:0]	RO	32'h0	Status of Channel Enable, Active high

5.4.5.2.3 DMA_LINK_LIST_EN

Description： Link List Mode enable register

0x0008			Link List Mode enable register (reset 0x0000_0000)										DMA_LINK_LIST_EN			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	LINK_LIST_EN															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LINK_LIST_EN															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
LINK_LIST_EN	[31:0]	R/W	32'h0	Channel Link List Mode Enable, Active high

5.4.5.2.4 DMA_SOFT_LIST_EN

Description：Soft List Mode enable register

0x000C			Soft List Mode enable register (reset 0x0000_0000)										DMA_SOFT_LIST_EN			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SOFT_LIST_EN															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SOFT_LIST_EN															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
SOFT_LIST_EN	[31:0]	R/W	32'h0	Channel Soft List Mode Enable, Active high

5.4.5.2.5 DMA_SOFT_LIST_SIZE

Description：Soft List size register

0x0010			Soft List size register (reset 0x0000_0000)										DMA_SOFT_LIST_SIZE			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SOFT_LIST_SIZE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
SOFT_LIST_SIZE	[15:0]	R/W	16'h0	The size of the request list. When the DMA reaches the end of list, it starts from the beginning again. For example, if SOFT_LIST_SIZE is equal to 5, then SW can set maximum (N) 5 requests to DMA. And if SOFT_LIST_EN is active, this value can't be zero.

5.4.5.2.6 DMA_SOFT_LIST_CMD

Description：Soft list command register

0x0014			Soft list command register (reset 0x0000_0000)										DMA_SOFT_LIST_CMD			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SOFT_LIST_CNT_INCR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
SOFT_LIST_CNT_INCR	[15:0]	WO	16'h0	Soft List Counter Increase, Write Only. It counts the number of pending SW request in the list. Every time the SW adds new requests to the list, SW must increase the counter by writing to this register. And when DMA completes one request, DMA decrease the counter.

				Note: Since the Soft List Counter is 16 bits, the SW must ensure that overflow can't happen.

5.4.5.2.7 DMA_SOFT_LIST_STATUS

Description：Soft list mode status register

0x0018			**Soft list mode status register (reset 0x0000_0000)**										**DMA_SOFT_LIST_STATUS**			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SOFT_LIST_REQ_PTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SOFT_LIST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
SOFT_LIST_REQ_PTR	[31:16]	RO	16'h0	Indicating which request DMA is going to serving. And corresponding SoftListSize, SW can know the situation of the request list and replace new requests to the old ones. This method can make SW and DMA synchronized.
SOFT_LIST_CNT	[15:0]	RO	16'h0	Counter value, maximum number of pending request is 2^{16}. Note: When in Soft List Mode, no request and acknowledge will occur, the condition {SOFT_LIST_CNT != 0} means request and SW regards the condition {SOFT_LIST_CNT = 0} as acknowledge. In this case, SW can only focus on the request list and don't care when these requests are completed.

5.4.5.2.8 DMA_SOFT_LIST_BADDR

Description：Base address register of soft list mode

0x001C			Base address register of soft list mode (reset 0x0000_0000)										DMA_SOFT_LIST_BADDR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SOFT_LIST_BASE_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SOFT_LIST_BASE_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
SOFT_LIST_BASE_ADDR	[31:0]	R/W	32'h0	Pointing the beginning address of Soft List Request. The lowest 2 bits must be "00", and can't be changed.

5.4.5.2.9 DMA_PRI_CFG0

Description：Channel Priority register

0x0020			Channel Priority register (reset 0x0000_0000)										DMA_PRI_CFG0			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	CHN15_PRI		CHN14_PRI		CHN13_PRI		CHN12_PRI		CHN11_PRI		CHN10_PRI		CHN9_PRI		CHN8_PRI	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHN7_PRI		CHN6_PRI		CHN5_PRI		CHN4_PRI		CHN3_PRI		CHN2_PRI		CHN1_PRI		CHN0_PRI	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
CHN15_PRI	[31:30]	R/W	2'h0	Channel 15 Priority
CHN14_PRI	[29:28]	R/W	2'h0	Channel 14 Priority
CHN13_PRI	[27:26]	R/W	2'h0	Channel 13 Priority
CHN12_PRI	[25:24]	R/W	2'h0	Channel 12 Priority
CHN11_PRI	[23:22]	R/W	2'h0	Channel 11 Priority
CHN10_PRI	[21:20]	R/W	2'h0	Channel 10 Priority
CHN19_PRI	[19:18]	R/W	2'h0	Channel 9 Priority
CHN8_PRI	[17:16]	R/W	2'h0	Channel 8 Priority

CHN7_PRI	[15:14]	R/W	2'h0	Channel 7 Priority
CHN6_PRI	[13:12]	R/W	2'h0	Channel 6 Priority
CHN5_PRI	[11:10]	R/W	2'h0	Channel 5 Priority
CHN4_PRI	[9:8]	R/W	2'h0	Channel 4 Priority
CHN3_PRI	[7:6]	R/W	2'h0	Channel 3 Priority
CHN2_PRI	[5:4]	R/W	2'h0	Channel 2 Priority
CHN1_PRI	[3:2]	R/W	2'h0	Channel 1 Priority
CHN0_PRI	[1:0]	R/W	2'h0	Channel 0 Priority, 2'b00 means lowest priority, and 2'b11 means highest priority.

5.4.5.2.10 DMA_PRI_CFG1

Description：Channel Priority register

0x0024			Channel Priority register (reset 0x0000_0000)													DMA_PRI_CFG1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	CHN31_PRI		CHN30_PRI		CHN29_PRI		CHN28_PRI		CHN27_PRI		CHN26_PRI		CHN25_PRI		CHN24_PRI	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHN23_PRI		CHN22_PRI		CHN21_PRI		CHN20_PRI		CHN19_PRI		CHN18_PRI		CHN17_PRI		CHN16_PRI	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
CHN31_PRI	[31:30]	R/W	2'h0	Channel 31 priority
CHN30_PRI	[29:28]	R/W	2'h0	Channel 30 priority
CHN29_PRI	[27:26]	R/W	2'h0	Channel 29 Priority
CHN28_PRI	[25:24]	R/W	2'h0	Channel 28 Priority
CHN27_PRI	[23:22]	R/W	2'h0	Channel 27 Priority
CHN26_PRI	[21:20]	R/W	2'h0	Channel 26 Priority
CHN25_PRI	[19:18]	R/W	2'h0	Channel 25 Priority
CHN24_PRI	[17:16]	R/W	2'h0	Channel 24 Priority
CHN23_PRI	[15:14]	R/W	2'h0	Channel 23 priority
CHN22_PRI	[13:12]	R/W	2'h0	Channel 22 priority
CHN21_PRI	[11:10]	R/W	2'h0	Channel 21 Priority
CHN20_PRI	[9:8]	R/W	2'h0	Channel 20 Priority
CHN19_PRI	[7:6]	R/W	2'h0	Channel 19 Priority

CHN18_PRI	[5:4]	R/W	2'h0	Channel 18 Priority
CHN17_PRI	[3:2]	R/W	2'h0	Channel 17 Priority
CHN16_PRI	[1:0]	R/W	2'h0	Channel 16 Priority

5.4.5.2.11 DMA_INT_MASK_STATUS

Description：DMA Masked interrupt status register

0x0030			DMA Masked interrupt status register (reset 0x0000_0000)										DMA_INT_MASK_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_MASK_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_MASK_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_MASK_STATUS	[31:0]	RO	32'h0	Channel31 to channel0 interrupt mask status. Int_mask_status = Trans_done_int_mask_stauts | Burst_done_int_mask_status | LList_done_int_mask_status ;

5.4.5.2.12 DMA_INT_RAW_STATUS

Description：DMA Raw interrupt status register

0x0034			DMA Raw interrupt status register (reset 0x0000_0000)										DMA_INT_RAW_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_RAW_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_RAW_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_RAW_STATUS	[31:0]	RO	32'h0	Channel31 to channel0 interrupt raw status. Int_mask_status = Trans_done_int_raw_stauts |

				Burst_done_int_raw_status | LList_done_int_raw_status ;

5.4.5.2.13 DMA_LLIST_DONE_INT_EN

Description：Interrupt enable register of Link list done

0x0040			Interrupt enable register of Link list done (reset 0x0000_0000)										DMA_LLIST_DONE_INT_EN			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	LLIST_DONE_INT_EN															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LLIST_DONE_INT_EN															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
LLIST_DONE_INT_EN	[31:0]	R/W	32'h0	Channel31 to channel0 all link list done interrupt enable.

5.4.5.2.14 DMA_BLOCK_DONE_INT_EN

Description：Interrupt enable register of block done

0x0044			Interrupt enable register of block done (reset 0x0000_0000)										DMA_BLOCK_DONE_INT_EN			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	BLOCK_DONE_INT_EN															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BLOCK_DONE_INT_EN															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
BLOCK_DONE_INT_EN	[31:0]	R/W	32'h0	Channel31 to channel0 one burst done interrupt enable.

5.4.5.2.15 DMA_TRANS_DONE_INT_EN

Description：Interrupt enable register of transaction done

0x0048			Interrupt enable register of transaction done (reset 0x0000_0000)										DMA_TRANS_DONE_INT_EN			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	TRANS_DONE_INT_EN															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TRANS_DONE_INT_EN															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
TRANS_DONE_INT_EN	[31:0]	R/W	32'h0	Channel31 to channel0 transaction or one node in link list mode done interrupt enable.

5.4.5.2.16 DMA_LLIST_DONE_INT_ MASK_STATUS

Description：Masked status of Link list done interrupt

0x0050			Masked status of Link list done interrupt (reset 0x0000_0000)										DMA_LLIST_DONE_INT_ MASK_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	LLIST_DONE_ INT_ MASK_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LLIST_DONE_ INT_ MASK_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
LLIST_DONE_ INT_ MASK_STATUS	[31:0]	RO	32'h0	Channel31 to channel0 link list done interrupt mask status.

5.4.5.2.17 DMA_BLOCK_DONE_INT_MASK_STATUS

Description：Masked status of block done interrupt

0x0054			Masked status of block done interrupt (reset 0x0000_0000)										DMA_BLOCK_DONE_INT_ MASK_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	BLOCK_DONE_ INT_ MASK_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BLOCK_DONE_ INT_ MASK_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
BLOCK_DONE_ INT_ MASK_STATUS	[31:0]	RO	32'h0	Channel31 to channel0 one block done interrupt mask status. block_done_int_mask_status = block_done_int_raw_status & block_done_int_en block done interrupt is import in infinite mode, sine total length of transaction is unknown, and a burst will be executed after every DMA request. DMA will not clear any interrupt status by itself.

5.4.5.2.18 DMA_TRANS_DONE_INT_MASK_STATUS

Description：Masked status of transaction done interrupt

0x0058			Masked status of transaction done interrupt (reset 0x0000_0000)										DMA_TRANS_DONE_INT_ MASK_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	TRANS_DONE_ INT_ MASK_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TRANS_DONE_ INT_ MASK_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
TRANS_DONE_ INT_ MASK_STATUS	[31:0]	RO	32'h0	Channel31 to channel0 one transaction or a node of link list done interrupt mask status. Trans_done_int_mask_status = Trans_done_int_raw_status & Trans_done_int_en

5.4.5.2.19 DMA_LLIST_DONE_INT_RAW_STATUS

Description：RAW status of Link list done interrupt

0x0060			RAW status of Link list done interrupt (reset 0x0000_0000)										DMA_LLIST_DONE_INT_RAW_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	LLIST_DONE_ INT_ RAW _STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LLIST_DONE_ INT_ RAW _STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
LLIST_DONE_ INT_ RAW _STATUS	[31:0]	RO	32'h0	Channel31 to channel0 all link list done interrupt raw status.

5.4.5.2.20 DMA_BLOCK_DONE_INT_RAW_STATUS

Description：RAW status of block done interrupt

0x0064			RAW status of block done interrupt (reset 0x0000_0000)										DMA_BLOCK_DONE_INT_RAW_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	BLOCK_DONE_ INT_ RAW _STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BLOCK_DONE_ INT_ RAW _STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
BLOCK_DONE_ INT_ RAW _STATUS	[31:0]	RO	32'h0	Channel31 to channel0 one block done interrupt RAW status.

5.4.5.2.21 DMA_TRANS_DONE_INT_RAW_STATUS

Description：RAW status of Transaction done interrupt

0x0068			RAW status of Transaction done interrupt (reset 0x0000_0000)										DMA_TRANS_DONE_INT_RAW _STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	TRANS_DONE_ INT_ RAW _STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TRANS_DONE_ INT_ RAW _STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
TRANS_DONE_INT_RAW _STATUS	[31:0]	RO	32'h0	Channel31 to channel0 one transaction or a node of link list done interrupt RAW status.

5.4.5.2.22 DMA_LLIST_DONE_INT_CLR

Description：Clear interrupt of Link List done

0x0070			Clear interrupt of Link List done (reset 0x0000_0000)										DMA_LLIST_DONE_INT_CLR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	LLIST_DONE_ INT_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LLIST_DONE_ INT_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
LLIST_DONE_INT_CLR	[31:0]	WO	32'h0	Channel31 to channel0 all link_list_done interrupt clear.

5.4.5.2.23 DMA_BLOCK_DONE_INT_CLR

Description：Clear interrupt of Block done

0x0074			Clear interrupt of Block done (reset 0x0000_0000)										DMA_BLOCK_DONE_INT_CLR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	BLOCK_DONE_ INT_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BLOCK_DONE_ INT_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
BLOCK_DONE_INT_CLR	[31:0]	WO	32'h0	Channel31 to channel0 Block Done interrupt clear.

5.4.5.2.24 DMA_TRANS_DONE_INT_CLR

Description： Clear interrupt of Transaction done

0x0078			Clear interrupt of Transaction done (reset 0x0000_0000)										DMA_TRANS_DONE_INT_CLR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	TRANS_DONE_ INT_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TRANS_DONE_ INT_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
TRANS_DONE_INT_CLR	[31:0]	WO	32'h0	Channel31 to channel0 transaction or a node of link list done interrupt clear.

5.4.5.2.25 DMA_SOFT_REQ

Description：Soft channel request

0x0080	Soft channel request (reset 0x0000_0000)													DMA_SOFT_REQ			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SOFT_REQ															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SOFT_REQ															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
SOFT_REQ	[31:0]	WO	32'h0	Active high, Channel31 to channel0 software request. In software request mode, this signal starts the transfer.

5.4.5.2.26 DMA_STATUS

Description：DMA Status

0x0084	DMA Status (Reset to 0x0000_E000)														DMA_STATUS	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DMA_BUSY	DMA_PAUSE	Reserved.													
Type	RO	RO	RO													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	HREADY_DMAS	HREADY_DMAW	HREADY_DMAR	MFSM_STATUS					SFSM_STATUS				DFSM_STATUS			
Type	RO	RO	RO	RO					RO				RO			
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
DMA_BUSY	[31]	RO	1'h0	1'b1: DMA is busy. 1'b0: Main FSM is in IDLE state, and no request pending
DMA_PAUSE	[30]	RO	1'h0	1'b1: DMA in pause state 1'b0: DMA is not in Pause Status
	[28:16]	RO	14'h0	Reserved.
HREADY_DMAS	[15]	RO	1'h1	DMA AHB slave side HREADY signal
HREADY_DMAW	[14]	RO	1'h1	DMA AHB destination master side HREADY signal

HREADY_DMAR	[13]	RO	1'h1	DMA AHB source master side HREADY signal
MFSM_STATUS	[12:8]	RO	5'h0	DMA AHB main FSM current state
SFSM_STATUS	[7:4]	RO	4'h0	DMA AHB source FSM current state
DFSM_STATUS	[3:0]	RO	4'h0	DMA AHB destination FSM current state

5.4.5.2.27 DMA_REQ_PEND

Description：Pending request status.

0x0088			Pending request status. (Reset to 0x0000_0000)										DMA_REQ_PEND			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	REQ_PEND															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	REQ_PEND															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
REQ_PEND	[31:0]	RO	0	DMA pending request.

5.4.5.2.28 DMA_WRAP_START_ADDR

Description：Start address of WRAP mode

0x0090			Start address of WRAP mode (reset 0x0000_0000)										DMA_WRAP_START_ADDR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				WRAP_START_ADDR											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	WRAP_START_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
WRAP_START_ADDR	[27:0]	R/W	28'h0	DMA Start Address in wrap mode

5.4.5.2.29 DMA_WRAP_END_ADDR

Description：End address of WRAP mode

0x0094			End address of WRAP mode (reset 0x0000_0000)										DMA_WRAP_END_ADDR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				WRAP_END_ADDR											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	WRAP_END_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
WRAP_END_ADDR	[27:0]	R/W	28'h0	DMA End Address in wrap mode

5.4.5.2.30 DMA_CHN_UID_CFG0

Description：User ID of channels

0x0098			User ID of channels (reset 0x0000_0000)										DMA_CHN_UID_CFG0			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved			CHN3_UID					Reserved			CHN2_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			CHN1_UID					Reserved			CHN0_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:29]	RO	3'h0	Reserved.
CHN3_UID	[28:24]	R/W	5'h0	Channel 3 User ID number; Each DMA user, that may trigger DMA, has a unique ID number, and SW may assign a DMA channel to any one of them, no matter APB or AHB module;
	[23:21]	RO	3'h0	Reserved.
CHN2_UID	[20:16]	R/W	5'h0	Channel 2 User ID number;
	[15:13]	RO	3'h0	Reserved.

CHN1_UID	[12:8]	R/W	5'h0	Channel 1 User ID number;
	[7:5]	RO	3'h0	Reserved.
CHN0_UID	[4:0]	R/W	5'h0	Channel 0 User ID number;

5.4.5.2.31 DMA_CHN_UID_CFG1

Description：User ID of channels

0x009C			User ID of channels (reset 0x0000_0000)										DMA_CHN_UID_CFG1			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved			CHN7_UID					Reserved			CHN6_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			CHN5_UID					Reserved			CHN4_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:29]	RO	3'h0	Reserved.
CHN7_UID	[28:24]	R/W	5'h0	Channel 7 User ID number; Each DMA user, that may trigger DMA, has a unique ID number, and SW may assign a DMA channel to any one of them, no matter APB or AHB module;
	[23:21]	RO	3'h0	Reserved.
CHN6_UID	[20:16]	R/W	5'h0	Channel 6 User ID number;
	[15:13]	RO	3'h0	Reserved.
CHN5_UID	[12:8]	R/W	5'h0	Channel 5 User ID number;
	[7:5]	RO	3'h0	Reserved.
CHN4_UID	[4:0]	R/W	5'h0	Channel 4 User ID number;

5.4.5.2.32 DMA_CHN_UID_CFG2

Description：User ID of channels

0x00A0	User ID of channels (reset 0x0000_0000)												DMA_CHN_UID_CFG2			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved			CHN11_UID					Reserved			CHN10_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			CHN9_UID					Reserved			CHN8_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:29]	RO	3'h0	Reserved.
CHN11_UID	[28:24]	R/W	5'h0	Channel 11 User ID number; Each DMA user, that may trigger DMA, has a unique ID number, and SW may assign a DMA channel to any one of them, no matter APB or AHB module;
	[23:21]	RO	3'h0	Reserved.
CHN10_UID	[20:16]	R/W	5'h0	Channel 10 User ID number;
	[15:13]	RO	3'h0	Reserved.
CHN9_UID	[12:8]	R/W	5'h0	Channel 9 User ID number;
	[7:5]	RO	3'h0	Reserved.
CHN8_UID	[4:0]	R/W	5'h0	Channel 8 User ID number;

5.4.5.2.33 DMA_CHN_UID_CFG3

Description：User ID of channels

0x00A4	User ID of channels (reset 0x0000_0000)												DMA_CHN_UID_CFG3			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved			CHN15_UID					Reserved			CHN14_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			CHN13_UID					Reserved			CHN12_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:29]	RO	3'h0	Reserved.
CHN15_UID	[28:24]	R/W	5'h0	Channel 15 User ID number; Each DMA user, that

				may trigger DMA, has a unique ID number, and SW may assign a DMA channel to any one of them, no matter APB or AHB module;
	[23:21]	RO	3'h0	Reserved.
CHN14_UID	[20:16]	R/W	5'h0	Channel 14 User ID number;
	[15:13]	RO	3'h0	Reserved.
CHN13_UID	[12:8]	R/W	5'h0	Channel 13 User ID number;
	[7:5]	RO	3'h0	Reserved.
CHN12_UID	[4:0]	R/W	5'h0	Channel 12 User ID number;

5.4.5.2.34 DMA_CHN_UID_CFG4

Description：User ID of channels

0x00A8			User ID of channels (reset 0x0000_0000)													DMA_CHN_UID_CFG4
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved			CHN19_UID					Reserved			CHN18_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			CHN17_UID					Reserved			CHN16_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:29]	RO	3'h0	Reserved.
CHN19_UID	[28:24]	R/W	5'h0	Channel 19 User ID number; Each DMA user, that may trigger DMA, has a unique ID number, and SW may assign a DMA channel to any one of them, no matter APB or AHB module;
	[23:21]	RO	3'h0	Reserved.
CHN18_UID	[20:16]	R/W	5'h0	Channel 18 User ID number;
	[15:13]	RO	3'h0	Reserved.
CHN17_UID	[12:8]	R/W	5'h0	Channel 17 User ID number;
	[7:5]	RO	3'h0	Reserved.
CHN16_UID	[4:0]	R/W	5'h0	Channel 16 User ID number;

5.4.5.2.35 DMA_CHN_UID_CFG5

Description：User ID of channels

0x00AC			User ID of channels (reset 0x0000_0000)										DMA_CHN_UID_CFG5			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved			CHN23_UID					Reserved			CHN22_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			CHN21_UID					Reserved			CHN20_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:29]	RO	3'h0	Reserved.
CHN23_UID	[28:24]	R/W	5'h0	Channel 23 User ID number; Each DMA user, that may trigger DMA, has a unique ID number, and SW may assign a DMA channel to any one of them, no matter APB or AHB module;
	[23:21]	RO	3'h0	Reserved.
CHN22_UID	[20:16]	R/W	5'h0	Channel 22 User ID number;
	[15:13]	RO	3'h0	Reserved.
CHN21_UID	[12:8]	R/W	5'h0	Channel 21 User ID number;
	[7:5]	RO	3'h0	Reserved.
CHN20_UID	[4:0]	R/W	5'h0	Channel 20 User ID number;

5.4.5.2.36 DMA_CHN_UID_CFG6

Description：User ID of channels

0x00B0			User ID of channels (reset 0x0000_0000)										DMA_CHN_UID_CFG6			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved			CHN27_UID					Reserved			CHN26_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			CHN25_UID					Reserved			CHN24_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:29]	RO	3'h0	Reserved.
CHN27_UID	[28:24]	R/W	5'h0	Channel 27 User ID number; Each DMA user, that

				may trigger DMA, has a unique ID number, and SW may assign a DMA channel to any one of them, no matter APB or AHB module;
	[23:21]	RO	3'h0	Reserved.
CHN26_UID	[20:16]	R/W	5'h0	Channel 26 User ID number;
	[15:13]	RO	3'h0	Reserved.
CHN25_UID	[12:8]	R/W	5'h0	Channel 25 User ID number;
	[7:5]	RO	3'h0	Reserved.
CHN24_UID	[4:0]	R/W	5'h0	Channel 24 User ID number;

5.4.5.2.37 DMA_CHN_UID_CFG7

Description：User ID of channels

0x00B4			User ID of channels (reset 0x0000_0000)										DMA_CHN_UID_CFG7			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved			CHN31_UID					Reserved			CHN30_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			CHN29_UID					Reserved			CHN28_UID				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:29]	RO	3'h0	Reserved.
CHN31_UID	[28:24]	R/W	5'h0	Channel 31 User ID number; Each DMA user, that may trigger DMA, has a unique ID number, and SW may assign a DMA channel to any one of them, no matter APB or AHB module;
	[23:21]	RO	3'h0	Reserved.
CHN30_UID	[20:16]	R/W	5'h0	Channel 30 User ID number;
	[15:13]	RO	3'h0	Reserved.
CHN29_UID	[12:8]	R/W	5'h0	Channel 29 User ID number;
	[7:5]	RO	3'h0	Reserved.
CHN28_UID	[4:0]	R/W	5'h0	Channel 28 User ID number;

5.4.5.2.38 DMA_CHN_EN_SET

Description： Set Channels enable register

0x00C0	Set Channel enable register (reset 0x0000_0000)													DMA_CHN_EN_SET			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	CHN_EN_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHN_EN_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
CHN_EN_SET	[31:0]	WO	32'h0	Set Channel Enable, Active high

5.4.5.2.39 DMA_CHN_EN_CLR

Description： Clear Channels enable register

0x00C4	Clear Channel enable register (reset 0x0000_0000)													DMA_CHN_EN_CLR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	CHN_EN_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHN_EN_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
CHN_EN_CLR	[31:0]	WO	32'h0	Clear Channel Enable, Active high

5.4.5.2.40 CHNX_CFG

Description：Channel X configure register, X = 0, 1, 2 ….31

0x0400 + 0x20*X	Channel X configure register (reset 0xXXXX_XXXX)															CHNX_CFG
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	LLIST_END	Reserved	SWT_MODE_SEL		SRC_DATA_WIDTH		DEST_DATA_WIDTH		REQ_MODE_SEL		SRC_WRAP_EN	DEST_WRAP_EN	Reserved		NO_AUTO_CLOSE	Reserved
Type	R/W	R/W	R/W		R/W		R/W		R/W		R/W	R/W	RO		R/W	RO
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BLOCK_LENGTH															
Type	R/W															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Field Name	Bit	Type	Reset Value	Description
LLIST_END	[31]	R/W	1'hx	Active high, Link list end flag means this is the last one of the link list. When LLEnd is active, LLPtr means nothing.
	[30]	R/W	1'hx	Reserved.
SWT_MODE_SEL	[29:28]	R/W	2'hx	DMA supports 4 kinds of Switch mode, they are: 2'b00: Un-switch Mode; 2'b01: Full Switch Mode, All the bytes within a word reversed; 2'b10: Switch Mode 0, In a word, the two bytes within each half-word reversed, and the position of the tow Half-words keep un-touched. 2'b11: Switch Mode 1, In a word, the two Half-words reversed, and the bytes within each Half-word keep un-touched. For example: if DMA receives a word "0xABCD", and the result of endian switch is showed below: 2'b00: 0xABCD => 0xABCD 2'b01: 0xABCD => 0xDCBA 2'b10: 0xABCD => 0xBADC 2'b11: 0xABCD => 0xCDAB Note: In any switch mode, Full switch, switch mode0 or switch mode1, both the total length and block length MUST be WORD boundary, and if not, data may be lost in transfer.
SRC_DATA_WIDTH	[27:26]	R/W	2'hx	Source data width. 00: byte. 01: half-word. 10: word.
DEST_DATA_WIDTH	[25:24]	R/W	2'hx	Destination data width. 00: byte. 01: half-word. 10: word.
REQ_MODE_SEL	[23:22]	R/W	2'hx	Channel request mode selection signals 2'b00: Normal mode, one request for one block. 2'b01: Transaction mode, one request for the total length of one transaction. 2'b10: List mode, one request for the whole link

				list. In soft List mode, DMA will execute transfer whenever the “counter” is unequal to zero; 2’b11: Infinite mode, the total length of the current channel is unknown, while block length is configured fixed. So DMA will always transfer a fixed length block whenever a corresponding dma_req is active. Note: 1. In SoftList mode, “ReqModeSel” must be set to “2’b10”, that is, one request for the whole list. In Infinite mode, NoAutoClose should be set;
SRC_WRAP_EN	[21]	R/W	1’hx	Active high, Source Address Wrapping Enable
DEST_WRAP_EN	[20]	R/W	1’hx	Active high, Destination Address Wrapping Enable
	[19:18]	RO	2’hx	Reserved.
NO_AUTO_CLOSE	[17]	R/W	1’hx	Channel No Auto-Close 0: ChnEn is set by ARM and cleared automatically after transferring the whole link list in link list mode, or the whole transaction in normal mode. 1: ChnEn is set and cleared only by ARM. Note: in Soft list mode, this register value will be ignored.
	[16]	RO	1’hx	Reserved.
BLOCK_LENGTH	[15:0]	R/W	16’hx	BlockLength The unit is BYTE. **Note:** burst_length should be on maxium value of src_data_width and dest_data_width boundary;

5.4.5.2.41 CHNX_ TOTAL_LEN

Description：Channel X total length, X = 0, 1, 2 ….31

0x0404 + 0x20*X	Channel X total length (reset 0xXXXX_XXXX)												CHNX_ TOTAL_LEN			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved							TOTAL_LEN								
Type	RO							R/W								
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TOTAL_LEN															
Type	R/W															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Field Name	Bit	Type	Reset Value	Description
	[31:25]	RO	7’hx	Reserved
TOTAL_LEN	[24:0]	R/W	25’hx	Total transfers length.

				The unit is BYTE. Note: total length can be any value without concerning about Burst length.

5.4.5.2.42 CHNX_SRC_ADDR

Description：Channel X Source Address, X = 0, 1, 2 ….31

0x0408 + 0x20*X	Channel X Source Address (reset 0xXXXX_XXXX)												CHNX_SRC_ADDR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SRC_ADDR															
Type	R/W															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SRC_ADDR															
Type	R/W															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Field Name	Bit	Type	Reset Value	Description
SRC_ADDR	[31:0]	R/W	32’hx	Source address.

5.4.5.2.43 CHNX_DEST_ADDR

Description：Channel X Destination Address, X = 0, 1, 2 ….31

0x040C + 0x20*X	Channel X Source Address (reset 0xXXXX_XXXX)												CHNX_DEST_ADDR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DEST_ADDR															
Type	R/W															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DEST_ADDR															
Type	R/W															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Field Name	Bit	Type	Reset Value	Description
DEST_ADDR	[31:0]	R/W	32’hx	Destination address.

5.4.5.2.44 CHNX_LLIST_PTR

Description：Channel X Link list pointer address, X = 0, 1, 2 ….31

0x0410 + 0x20*X			Channel X Link list pointer address (reset 0xXXXX_XXXX)										CHNX_LLIST_PTR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	LLIST_PTR															
Type	R/W															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LLIST_PTR															
Type	R/W															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Field Name	Bit	Type	Reset Value	Description
LLIST_PTR	[31:0]	R/W	32'hx	Link list pointer to the next node address. MUST be on 8-word boundary. So when writing, bit [4:0] is omitted; When reading, bit [4:0] is 0. If LLEnd is set, indicating the current transaction is last one of the list, LLPtr is unused.

5.4.5.2.45 CHNX_ELEM_POSTM

Description：Channel X Element post-modification, X = 0, 1, 2 ….31

0x0414 + 0x20*X			Channel X Element post-modification (reset 0xXXXX_XXXX)										CHNX_ELEM_POSTM			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SRC_ELEM_POSTM															
Type	R/W															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DEST_ELEM_POSTM															
Type	R/W															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Field Name	Bit	Type	Reset Value	Description
SRC_ELEM_POSTM	[31:16]	R/W	16'hx	Sets the post-modification value of the source's current address during a block transfer. The value is in 2's complement format, which means that both positive and negative values are supported. The post-modification value is summed with the source current address following an element Read transfer. **Note:** The value must be set to an integer multiple of the Source data width, setting it to a different value may yield unexpected behaviors. When DMA source master working in BURST,

				this register “src_elem_postm” is automatically set to “don’t care”, and DMA will manage HADDRdmar according to src_data_width;
DEST_ELEM_POSTM	[15:0]	R/W	16’hx	Sets the post-modification value of the destination's current address during a block transfer. The value is in 2’s complement format, which means that both positive and negative values are supported. The post-modification value is summed with the destination current address following an element Write transfer. **Note:** The value must be set to an integer multiple of the Destination data width; setting it to a different value may yield unexpected behavior. When DMA destination master working in BURST, this register “dest_elem_postm” is automatically set to “don’t care”, and DMA will manage HADDRdmaw according to src_data_width;

5.4.5.2.46 CHNX_SRC_BLOCK_POSTM

Description：Channel X Source Block post-modification, X = 0, 1, 2 ….31

0x0418 + 0x20*X			Channel X Source Block post-modification (reset 0xXXXX_XXXX)										CHNX_SRC_BLOCK_POSTM			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved	SRC_BURST_MODE			Reserved		SRC_BLOCK_POSTM									
Type	RO	R/W			RO		R/W									
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SRC_BLOCK_POSTM															
Type	R/W															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Field Name	Bit	Type	Reset Value	Description
	[31]	RO	1’hx	Reserved.
SRC_BURST_MODE	[30:28]	R/W	3’hx	000 – Single Transfer; NSEQ for each transfer; 001 – INCR for unspecified length 011 – INCR4; 101 – INCR8; 111 – INCR16; No wrap burst is supported.
	[27:26]	RO	2’hx	Reserved.
SRC_BLOCK_POSTM	[25:0]	R/W	26’hx	Sets the post-modification value of the source’s current address, between the Read transfer of the

				last element in a source block to the first element of the next block during a cluster transfer. The value is in 2's complement, which means that both positive and negative values are supported. The post-modification value is summed with the source current address following a block Read transfer. **Note:** The value must be set to an integer multiple of the data width; setting it to a different value may yield unexpected behavior.

5.4.5.2.47 CHNX_DEST_BLOCK_POSTM

Description：Channel X Destination Block post-modification, X = 0, 1, 2 ….31

0x041C + 0x20*X			Channel X Destination Block post-modification (reset 0xXXXX_XXXX)										CHNX_DEST_BLOCK_POSTM			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved	DEST_BURST_MODE			Reserved		DEST_BLOCK_POSTM									
Type	RO	R/W			RO		R/W									
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DEST_BLOCK_POSTM															
Type	R/W															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Field Name	Bit	Type	Reset Value	Description
	[31]	RO	1'hx	Reserved.
DEST_BURST_MODE	[30:28]	R/W	3'hx	000 – Single Transfer; NSEQ for each transfer; 001 – INCR for unspecified length 011 – INCR4; 101 – INCR8; 111 – INCR16; No wrap burst is supported.
	[27:26]	RO	2'hx	Reserved.
DEST_BLOCK_POSTM	[25:0]	R/W	26'hx	Sets the post-modification value of the destination's current address, between the Read transfers of the last element in a current block to the first element of the next block during a cluster transfer. The value is in 2's Complement, which means that both positive and negative values are supported. The post-modification value is summed with the destination current address following a block Write transfer. **Note:** The value bit must be set to a fixed multiple of the data width in bytes; setting it to a different value may yield unexpected behavior.

5.4.6 Application Notes

In link list mode, each link list pointer address MUST be on WORD boundary. DMA will read successive 8 words (from pointer to [pointer + 0x1C]) into DMA internal channel registers.

Data width on DMA slave port MUST be WORD. Reading or writing BYTE or HALF-WORD width data on DMA SLAVE port will cause error.

In present DMA design, total_length can be any value without concerning about src/dest_data_width. But Block_length should be on maxium value of src_data_width and dest_data_width boundary, for example, if src_data_width is WORD and dest_data_width is BYTE, then block_length should be on WORD boundary. If total_length is not on src/dest_data_width boundary, the last element of the last block may contain some redundancy bits which are not desired

5.5 MCU Interrupt Controller

5.5.1 Overview

SC6820 provides a 32-channel interrupt controller to collect all interrupts from different modules to generate FIQ and IRQ to MCU.

5.5.2 Features

- Provide 30 hardware IRQ interrupt from channels 2 to channel 31
- Provide 30 hardware FIQ interrupt from channels 2 to channel 31
- Provide one software-trigged IRQ interrupt from channel 1
- Provide one software-trigged FIQ interrupt from channel 1
- Provide one special IRQ interrupt from channel 0
- Provide one special FIQ interrupt from channel 0
- Provide one interrupt sent to DSP, which is generated by all IRQ channel interrupt raw status OR bit by bit, with each channel enabled separately.
-
- Each IRQ or FIQ channel can be enabled or disabled independently
- Provide raw status for each IRQ or FIQ channel
- Provide masked status for each IRQ or FIQ channel
- Special IRQ or FIQ interrupt on channel 0 is used to latch some input signal status and trigger IRQ or FIQ interrupt by level detecting (not edge detecting)
- Special IRQ or FIQ interrupt on channel 0 is multiplexed from four independent input sources
- Provide raw status for each of four input sources on special channel
- Provide polarity control bit for each of four input sources on special channel
- Provide only one clear bit to clear all latches on special channel
- Each input source can be enabled or disabled independently on special channel

5.5.3 Function Description

SC6820 interrupt controller provides four different functions – thirty channels of hardware-trigged IRQ and FIQ interrupts, one channel of software-trigged IRQ and FIQ interrupts, and five special latch channels, and one interrupt sent to DSP

5.5.3.1 Hardware-Trigged Channels

Thirty channels are used as hardware-trigged channels, which are from channels 2 to channel 31, and their sources are specified in the above table.

The hardware-trigged function is the main function provided by the interrupt controller. The controller collects interrupt trigger signals from different hardware modules,

applies mask on them and generates MCU FIQ and IRQ. The controller only supports level trigging, and trigging level is high active. There is no DFF or latch to keep status on the hardware-trigged channel path. So this controller can be used to wakeup MCU sub-system during sleep with no working clock, but it needs each source latches the interrupt status.

The circuit is very simple on hardware-trigged channels, shown as follows.

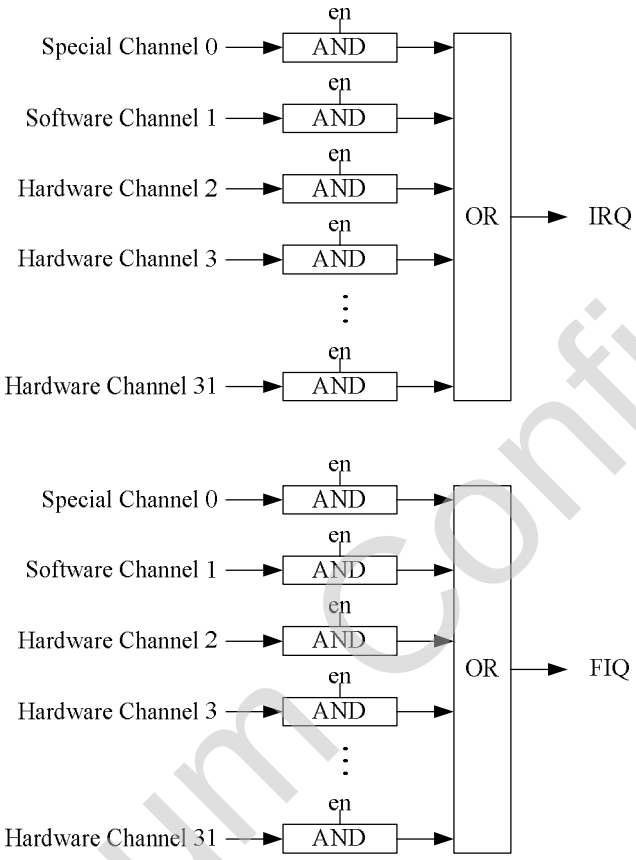


Figure 5-9 Hardware-Trigged channels diagram

5.5.3.2 Software-Trigged Channels

Software-trigged interrupt is assigned to channel 1, and the function is similar to other hardware interrupts. The difference between them is that the software-trigged interrupt is issued in interrupt controller by setting one bit. Similarly, this interrupt can be cleared by just clearing this bit. This interrupt cannot wake up the system.

5.5.3.3 Special Latch Channels

There is one special IRQ channel and FIQ channel, assigned on IRQ channel 0 and FIQ channel 0. These two channels are special because they are connected with off-chip interrupt to wakeup MCU sub-system. However inside the Interrupt Controller they are the same priority and function with other channels.

5.5.3.4 Interrupt sent to DSP

Interrupt sent to DSP is generated by all IRQ channel interrupt raw status OR bit by bit, with each channel enabled separately by register INT2DSP_ENABLE.

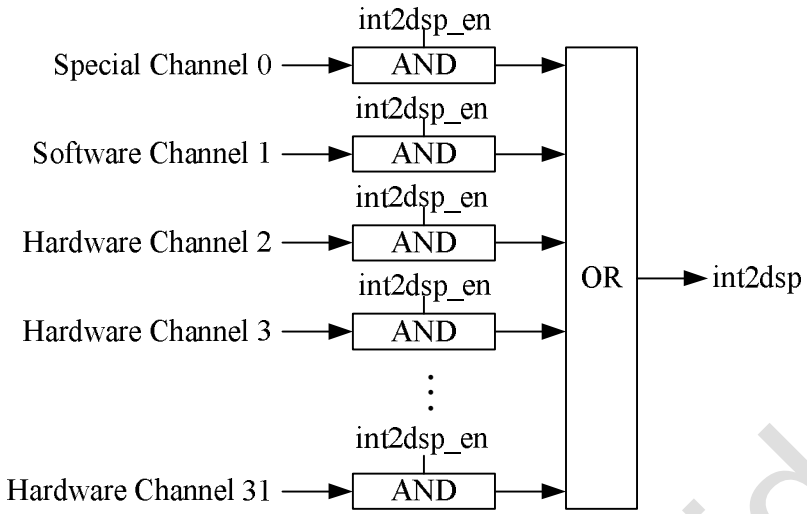


Figure 5-10 Interrupts to DSP diagram

5.5.4 Interrupt Channel Assignment

The following table shows the detailed channel assignment for both IRQ and FIQ.

Table 5-3 Interrupt channel assignment table

Channel Number	Source		Description
0	Special latch channel	0: UART0 RXD	
		1: UART0 CTSN	
		2: UART1 RXD	
		3: UART2 RXD	
		4: USB Input SE0	
		5: UART2 CTSN	
		6:csyspwrupreq	
1	Software-trigged channel		
2	UART0 Interrupt		
3	UART1 Interrupt | CA5_L2CC_INT | CA5_PMU_INT|CA5_NCT_INT		
4	UART2 Interrupt		
5	Generic Timer 0 Interrupt		
6	Generic Timer 1 Interrupt		
7	Generic Timer 2 Interrupt | COMMTX		
8	GPIO Combined Interrupt | EIC		
9	SPI0 Interrupt | SPI1 Interrupt		
10	Keypad Interrupt		
11	I2C0 | I2C1 Interrupt		

12	SIM0 Interrupt | SIM1 Interrupt	
13	PIU_SER_INT	Semaphore interrupts from DSP side; there are 3 interrupts and they are logically OR'ed together
14	PIU_CR_HINT | I2C2 | I2C3	Command/reply interrupt from DSP to MCU
15	DSP IRQ0	
16	DSP IRQ1	
17	System Timer Interrupt0	
18	EPT Interrupt	
19	IIS0 Interrupt | IIS1 Interrupt	
20	DSP INT OR	All the DSP interrupt
21	DMA Interrupt	
22	VBC Interrupt	
23	VSP Interrupt	
24	Ana_ irq	
25	ADI module Interrupt | GPU Interrupt	
26	USB Interrupt	
27	DCAM Interrupt	
28	NFC	
29	LCDC Interrupt	
30	DRM Interrupt | SDIO0 Interrupt	
31	Bus_mon0 | bus_mon1 | SDIO1 interrupt | AXI_bus_mon0|AXI_bus_mon1	

5.5.5 Control Registers

5.5.5.1 Memory map

ARM base address: 0x8000_3000

Offset Address	Name	Description
0x0000	INT_IRQ_MASK_STS	IRQ masked status
0x0004	INT_IRQ_RAW_STS	IRQ raw status
0x0008	INT_IRQ_ENABLE	IRQ enable control
0x000C	INT_IRQ_DISABLE	IRQ disable control
0x0010	INT_IRQ_SOFT	IRQ software interrupt trig
0x0014	INT_IRQ_TEST_SRC	IRQ test source generating
0x0018	INT_IRQ_TEST_SEL	IRQ test select
0x0020	INT_FIQ_MASK_STS	FIQ masked status

0x0024	INT_ FIQ_RAW_STS	FIQ raw status
0x0028	INT_ FIQ_ENABLE	FIQ enable control
0x002C	INT_ FIQ_DISABLE	FIQ disable control
0x0030	INT_ FIQ_SOFT	FIQ software interrupt trig
0x0034	INT_ FIQ_TEST_SRC	FIQ test source generating
0x0038	INT_ FIQ_TEST_SEL	FIQ test select

5.5.5.2 Register Descriptions

5.5.5.2.1 INT_IRQ_MASK_STS

Description：IRQ masked status

0x0000			IRQ masked status (reset 0x0)										INT_IRQ_MASK_STS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_IRQ_MASK_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_IRQ_MASK_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_IRQ_MASK_STS	[31:0]	RO	32'h0	IRQ interrupt channel masked status One bit for one channel Active high

5.5.5.2.2 INT_IRQ_RAW_STS

Description：IRQ raw status

0x0004			IRQ raw status (reset 0x0)										INT_IRQ_RAW_STS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_IRQ_RAW_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_IRQ_RAW_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_IRQ_RAW_STS	[31:0]	RO	32'h0	IRQ interrupt channel raw status One bit for one channel Active high

5.5.5.2.3 INT_IRQ_ENABLE

Description：IRQ enable control

0x0008	IRQ enable control (reset 0x0)												INT_IRQ_ENABLE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_IRQ_ENABLE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_IRQ_ENABLE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_IRQ_ENABLE	[31:0]	R/W	32'h0	IRQ interrupt channel enable One bit for one channel Write 1 to corresponding bit to enable the corresponding interrupt channel. Write 0 to any bit is DO NOT CARE. Write 1 to corresponding bit in **INT_IRQ_DISABLE** to clear enable bit. Read status: 0: related channel is disabled 1: related channel is enabled

5.5.5.2.4 INT_IRQ_DISABLE

Description：IRQ disable control

0x000c			IRQ disable control (reset 0x0)										INT_IRQ_DISABLE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_IRQ_DISABLE															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_IRQ_DISABLE															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_IRQ_DISABLE	[31:0]	WO	32'h0	IRQ interrupt channel disable One bit for one channel Write 1 to corresponding bit to disable the corresponding interrupt channel. Write 0 to any bit is DO NOT CARE.

5.5.5.2.5 INT_IRQ_SOFT

Description：IRQ software interrupt

0x0010			IRQ software interrupt (reset 0x0)												INT_IRQ_SOFT	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														INT_IRQ_SOFT	Reserved
Type	RO														WO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:2]	RO	30'h0	Reserved
INT_IRQ_SOFT	[1]	WO	1'h0	IRQ software interrupt Write 1 to active the software interrupt. Write 0 to clear the software interrupt.
	[0]	RO	1'h0	Reserved

5.5.5.2.6 INT_IRQ_TEST_SRC

Description：Test mode control: source generating

0x0014	IRQ test source generating (reset 0x0)												INT_IRQ_TEST_SRC			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_IRQ_TEST_SRC															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_IRQ_TEST_SRC														Reserved	INT_IRQ_TEST_SRC
Type	R/W														RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_IRQ_TEST_SRC	[31:0]	R/W	32'h0	IRQ test mode control for source generating One bit for one channel, the bit[1] is reserved. This register is only used in test mode. When INT_IRQ_TEST_SEL is 1, Write 1 to corresponding bit to generate INT_IRQ_RAW_STS. If the corresponding channel is enabled, IRQ to MCU and INT_IRQ_MASK_STS is also generated.

5.5.5.2.7 INT_IRQ_TEST_SEL

Description：Test mode control: test select

0x0018	IRQ test select (reset 0x0)												INT_IRQ_TEST_SEL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															INT_IRQ_TEST_SEL
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:1]	RO	31'h0	Reserved

INT_IRQ_TEST_SEL	[0]	R/W	1'h0	IRQ test mode enable Write 1 to enter test mode. In normal condition, this register MUST be configured to 0.

5.5.5.2.8 INT_FIQ_MASK_STS

Description：FIQ masked status

0x0020	FIQ masked status (reset 0x0)												INT_FIQ_MASK_STS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_FIQ_MASK_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_FIQ_MASK_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_FIQ_MASK_STS	[31:0]	RO	32'h0	FIQ interrupt channel masked status One bit for one channel Active high

5.5.5.2.9 INT_FIQ_RAW_STS

Description：FIQ raw status

0x0024	FIQ raw status (reset 0x0)												INT_FIQ_RAW_STS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_FIQ_RAW_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_FIQ_RAW_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_FIQ_RAW_STS	[31:0]	RO	32'h0	FIQ interrupt channel raw status One bit for one channel

				Active high

5.5.5.2.10 INT_FIQ_ENABLE

Description：FIQ enable control

0x0028	FIQ enable control (reset 0x0)												INT_FIQ_ENABLE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_FIQ_ENABLE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_FIQ_ENABLE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_FIQ_ENABLE	[31:0]	R/W	32'h0	FIQ interrupt channel enable One bit for one channel Write 1 to corresponding bit to enable the corresponding interrupt channel. Write 0 to any bit is DO NOT CARE. Write 1 to corresponding bit in **INT_FIQ_DISABLE** to clear enable bit. Read status: 0: related channel is disabled 1: related channel is enabled

5.5.5.2.11 INT_FIQ_DISABLE

Description：FIQ disable control

0x002c			FIQ disable control (reset 0x0)													INT_FIQ_DISABLE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_FIQ_DISABLE															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_FIQ_DISABLE															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_FIQ_DISABLE	[31:0]	WO	32'h0	FIQ interrupt channel disable One bit for one channel Write 1 to corresponding bit to disable the corresponding interrupt channel. Write 0 to any bit is DO NOT CARE.

5.5.5.2.12 INT_FIQ_SOFT

Description：FIQ software interrupt

0x0030			FIQ software interrupt (reset 0x0)													INT_FIQ_SOFT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														INT_FIQ_SOFT	Reserved
Type	RO														WO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:2]	RO	30'h0	Reserved
INT_FIQ_SOFT	[1]	WO	1'h0	FIQ software interrupt Write 1 to active the software interrupt. Write 0 to clear the software interrupt.
	[0]	RO	1'h0	Reserved

5.5.5.2.13 INT_FIQ_TEST_SRC

Description：Test mode control: source generating

0x0034	FIQ test source generating (reset 0x0)												INT_FIQ_TEST_SRC			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_FIQ_TEST_SRC															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_FIQ_TEST_SRC														Reserved	INT_FIQ_TEST_SRC
Type	R/W														RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_FIQ_TEST_SRC	[31:0]	R/W	32'h0	IRQ test mode control for source generating One bit for one channel, the bit[1] is reserved. This register is only used in test mode. When INT_FIQ_TEST_SEL is 1, Write 1 to corresponding bit to generate INT_FIQ_RAW_STS. If the corresponding channel is enabled, FIQ to MCU and INT_FIQ_MASK_STS is also generated.

5.5.5.2.14 INT_FIQ_TEST_SEL

Description：Test mode control: test select

0x0038	FIQ test select (reset 0x0)												INT_FIQ_TEST_SEL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															INT_FIQ_TEST_SEL
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

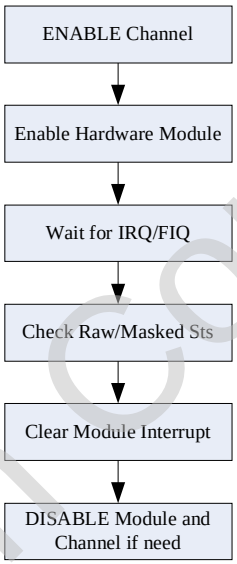
Field Name	Bit	Type	Reset Value	Description
	[31:1]	RO	31'h0	Reserved

INT_FIQ_TEST_SEL	[0]	R/W	1'h0	FIQ test mode enable Write 1 to enter test mode. In normal condition, this register MUST be configured to 0.

5.5.6 Application Notes

Interrupt Control's PCLK is open by default, so Software needs not to enable any bit and can access the register directly.

For IRQ and FIQ, the most important function is in the 30 hardware channel. They are connected to different hardware module. **Make sure that all the hardware modules' interrupt is level triggering, and triggering level is active high.** Once interrupt is generated, it should kept high until software clear it by setting interrupt clear bit in corresponding module. Following is the recommended flow for hardware channels.



5.6 AXI Bus Monitor

5.6.1 Overview

In SC6820, CPU and GPU access EMC through AXI interface. These two AXI interfaces share one bus monitor, we can set register to select one of them to monitor. Bus monitor could monitor the bus access on the AXI interface and provide the interrupts when a target reading from or writing to a target address. Only CHN_INT register(0x00) could be cleared after reset, other registers would not be effected by reset.

5.6.2 Features

SC6820 AXI bus monitor supports the following features:

- Support AMBA AXI bus Read and Write monitoring;
- Support AXI byte/half-word/word access monitoring;
- Support AXI ID monitoring;
- Support AXI burst type monitoring;
- Support AXI burst length monitoring;
- Support AXI WSTRB monitoring
- Support AXI 64-bit data bus monitoring, by 64-bit data mask;

- Support AXI 32-bit address space monitoring, for any address between minimal and maximum setting;
- Support interrupt raw/mask status and interrupt enable;
- Support triggered ADDR/DATA/SIZE/BURST/LEN/ID/WSTRB status.
- Support limited multiple outstanding as EMC, 4 for read and 8 for write

5.6.3 Signal Description

5.6.4 Function Description

5.6.5 Control Registers

5.6.5.1 Control Register Address Map

ARM base address: 0x20A0_0000

Offset Address	Register Name	Register Description
0x0~0x3	CHN_INT	Channel interrupt configure.
0x4~0x7	CHN_CFG	AXI feature configure
0x8~0xB	ADDR_MIN	Minimum address for monitoring.
0xC~0xF	ADDR_MAX	Maximum address for monitoring.
0x10~0x13	DATA_MIN_L32	Minimum data for monitoring, low 32bit
0x14~0x17	DATA_MAX_L32	Maximum data for monitoring. Low 32bit
0x18~0x1b	DATA_MASK_L32	Data mask for monitoring. Low 32bit
0x1C~0x1F	MATCH_ADDR	Matched address which triggered interrupt.
0x20~0x27	MATCH_DATA	Matched data which triggered interrupt.
0x28~0x2B	DATA_MIN_H32	Minimum data for monitoring, high 32bit
0x2C~0x2F	DATA_MAX_H32	Maximum data for monitoring. high 32bit
0x30~0x33	DATA_MASK_H32	Data mask for monitoring. high 32bit

5.6.5.2 Register Descriptions

5.6.5.2.1 CHN_INT

Description：

0x0000			. (Reset to 0x0000_0000)													CHN_INT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_MASK_STATUS	INT_RAW_STATUS	INT_CLR	INT_EN	Reserved.				Match_size		Match_burst		Match_len			
Type	RO	RO	WO	RW	RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Match_strb								Match_id						reserved	CHN_EN
Type	RO														RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_MASK_STATUS	[31]	RO	‘b0	Interrupt Mask status and should be cleared by asserting INT_CLR; Only would be active when INT_EN active high.
INT_RAW_STATUS	[30]	RO	‘b0	Interrupt raw status and should be cleared by asserting INT_CLR;
INT_CLR	[29]	WO	‘b0	Writing “1” to this bit will clear the interrupt raw status;
INT_EN	[28]	RW	‘b0	0 : By default, disable busmon interrupt; 1 : Enable busmon interrupt;
Reserved	[27:24]	RO	‘b0	Reserved.
MATCH_SIZE	[23:22]	RO	‘b0	AXI size of the matched transaction
MATCH_BURST	[21:20]	RO	‘b0	AXI Burst type of the matched transaction
MATCH_LEN	[19:16]	RO	‘b0	AXI Burst length of the matched transaction
MATCH_STRB	[15:8]	RO	‘b0	AXI Write strobe of the matched transaction
MATCH_ID	[7:2]	RO	‘b0	AXI transaction ID of the matched transaction
Reserved.	[1]	RO	‘b0	Reserved.
CHN_EN	[0]	RW	‘b0	Channel enable: 0: by default, disable bus monitor; 1: Enable bus monitor;

5.6.5.2.2 CHN_CFG

Description：

0x0004	. (Reset to 0x0000_0000)												CHN_CFG			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved.												BURST_CFG			BURST_EN
Type	RO												RW			RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MASTER_CFG				Reserved.			MASTER_EN	SIZE_CFG			SIZE_EN	Reserved		WRITE_CFG	WRITE_EN
Type	RW				RO			RW	RW			RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name / Bit	Bit	Type	Reset Value	Description
WSTRB_CFG	[31:24]	RW	‘b0	AXI WSTRB monitoring
LEN_CFG	[23:20]	RW	‘b0	AXI burst length monitoring
LEN_EN	[19]	RW	‘b0	AXI burst length monitoring enable 0: Disable ALEN monitoring 0: Enable ALEN monitoring
BURST_CFG	[18:17]	RW	‘b0	AXI BURST monitoring: 2’b00 : Fixed 2’b01 : INCR; 2’b10 : WRAP; 2;b11 : Reserved
BURST_EN	[16]	RW	‘b0	HBURST type monitoring enable: 0 : Disable BURST monitoring; 1 : Enable BURST monitoring;
ID_CFG	[15:10]	RW	‘b0	AXI ID monitoring
ID_EN	[9]	RW	‘b0	AXI ID monitoring enable
STRB_EN	[8]	RW	‘b0	AXI WSTRB monitoring enable
SIZE_CFG	[7:5]	RW	‘b0	AHB HSIZE monitoring: 000: Byte; 001: Half-word; 010: Word; Others: reserved.
SIZE_EN	[4]	RW	‘b0	HSIZE type monitoring enable; 0 : Disable HSIZE monitoring; 1 : Enable HSIZE monitoring;

Reserved	[3:2]	RW	‘b0	Reserved
WRITE_CFG	[1]	RW	‘b0	HWRITE for monitoring: 0 : HWRITE = 1’b0, read transaction; 1: HWRITE = 1’b1, write transaction;
WRITE_EN	[0]	RW	‘b0	HWRITE type monitoring enable; 0 : Dis-able HWRITE monitoring; 1 : Enable HWRITE monitoring;

5.6.5.2.3 ADDR_MIN

Description：

0x0008	. (Reset to 0x0000_0000)															ADDR_MIN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	ADDR_MIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ADDR_MIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
ADDR_MIN	[31: 0]	RW	‘b0	AHB minimal address for monitoring; Any access between Max and Min address space may trigger interrupt;

5.6.5.2.4 ADDR_MAX

Description：

0x000C	. (Reset to 0x0000_0000)															ADDR_MAX
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	ADDR_MAX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ADDR_MAX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

ADDR_MAX	[31: 0]	RW	‘b0	AHB maxium address for monitoring; Any access between Max and Min address space may trigger interrupt;

5.6.5.2.5 DATA_MIN_L32

Description：

0x0010			. (Reset to 0x0000_0000)										DATA_MIN			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DATA_MIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DATA_MIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
DATA_MIN_L32	[31: 0]	RW	‘b0	AHB minimal DATA for monitoring, low 32 bit Any access between Max and Min data space may trigger interrupt;

5.6.5.2.6 DATA_MAX_L32

Description：

0x0014			. (Reset to 0x0000_0000)										DATA_MAX			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DATA_MAX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DATA_MAX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
DATA_MAX_L32	[31: 0]	RW	‘b0	AHB maxium Data for monitoring, low 32 bit Any access between Max and Min Data space may trigger interrupt;

5.6.5.2.7 DATA_MASK_L32

Description：

0x0018	. (Reset to 0x0000_0000)												DATA_MASK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DATA_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DATA_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
DATA_MASK_L32	[31: 0]	RW	‘b0	Data_mask, active high makes the data of corresponding bits to be masked, and ignored during comparation. , low 32 bit

5.6.5.2.8 MATCH_ADDR

Description：

0x001C	. (Reset to 0x0000_0000)												MATCH_ADDR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	MATCH_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MATCH_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
MATCH_ADDR	[31: 0]	RO	‘b0	Captured Address, which triggered interrupt;

5.6.5.2.9 MATCH_DATA_L32

Description：

0x0020			. (Reset to 0x0000_0000)										MATCH_DATA			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	MATCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MATCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
MATCH_DATA_L32	[31: 0]	RO	‘b0	Captured Data, which triggered interrupt; low 32 bit

5.6.5.2.10 MATCH_DATA_H32

Description：

0x0024			. (Reset to 0x0000_0000)										BUSMON_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	MATCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MATCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
MATCH_DATA_H32	[31: 0]	RO	‘b0	Captured Data, which triggered interrupt; high 32 bit

5.6.5.2.11 DATA_MIN_H32

Description：

0x0010			. (Reset to 0x0000_0000)													DATA_MIN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DATA_MIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DATA_MIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
DATA_MIN_H32	[31: 0]	RW	‘b0	AHB minimal DATA for monitoring, high 32 bit Any access between Max and Min data space may trigger interrupt;

5.6.5.2.12 DATA_MAX_H32

Description：

0x0014			. (Reset to 0x0000_0000)													DATA_MAX
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DATA_MAX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DATA_MAX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
DATA_MAX_H32	[31: 0]	RW	‘b0	AHB maxium Data for monitoring, high 32 bit Any access between Max and Min Data space may trigger interrupt;

5.6.5.2.13 DATA_MASK_H32

Description：

0x0018			. (Reset to 0x0000_0000)										DATA_MASK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DATA_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DATA_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
DATA_MASK_H32	[31: 0]	RW	‘b0	Data_mask, active high makes the data of corresponding bits to be masked, and ignored during comparation. ,high 32 bit

5.6.6 Application Note

SW programming is almost the same as AHB bus monitor. The most important difference is that the bus monitor do not support dynamically on/off because AXI address and data is in separate channel and multiple outstanding is enabled. So the bus monitor should always be on if we want to monitor AXI transaction. The other thing is that we can set register axibusmon_sel(0x2090_020C, bit11) to select one of them to monitor. (1: select GPU, 0:select CPU).

5.7 AHB Bus Monitor

5.7.1 Overview

SC6820 contains multi-layer AHB bus, and each layer contains AHB masters and slaves. Bus monitors could monitor the bus access and provide the interrupts when a target data reading from or writing to a target address. Only CHN_INT register(0x00) could be cleared after reset, other registers would not be effected by reset.

Besides, bus monitors provide the bus usage to analyze system performance.

5.7.2 Features

SC6820 bus monitor supports the following features:

- Support AMBA AHB bus Read and Write monitoring;
- Support AHB byte/half-word/word access monitoring;
- Support AHB 32-bit data bus monitoring, by 32-bit data mask;
- Support AHB 32-bit address space monitoring, for any address between minimal and maximum setting;
- Support interrupt raw/mask status and interrupt enable;
- Support triggered HADDR/HDATA/HSIZE/HBURST status.

5.7.3 Bus Monitor Assignment

SC6820 contains 7 AHB masters and 2 ARM side bus monitors, that is, only 2 AHB masters can be monitored at a given time. The bus monitors assignment is illustrated below.

Table 5-4 Bus Monitor Assignment

Busmon Num	Busmon0/1_sel = 0	Busmon0/1/_sel = 1
Bus Monitor0	A5 AHB master	Empty
Bus Monitor1	DMAR/DMAW/SDIO/USB/CEVAX access to others	DMAR/DMAW/SDIO/USB/CEVAacess to EMC

5.7.4 Control Registers

5.7.4.1 Memory Map

ARM base address: 0x2040_0000 + 0x0000_1000 * N (N= 0, 1, Busmon Num)

Offset Address	Register Name	Register Description
0x0000	CHN_INT	Channel interrupt configure.
0x0004	CHN_CFG	AHB feature configure.
0x0008	ADDR_MIN	Minimum address for monitoring.
0x000C	ADDR_MAX	Maximum address for monitoring.
0x0010	DATA_MIN	Minimum data for monitoring.
0x0014	DATA_MAX	Maximum data for monitoring.
0x0018	DATA_MASK	Data mask for monitoring.
0x001C	MATCH_ADDR	Matched address which triggered interrupt.
0x0020	MATCH_DATA	Matched data which triggered interrupt.
0x0024	BUSMON_CNT	Performance counter.

5.7.4.2 Register Descriptions

5.7.4.2.1 CHN_INT

Description:

0x0000			. (Reset to 0x0000_0000)													CHN_INT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_MASK_STATUS	INT_RAW_STATUS	INT_CLR	INT_EN	Reserved.											
Type	RO	RO	WO	RW	RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved.										CNT_SEL		CNT_CLR	CNT_HOLD	CNT_EN	CHN_EN
Type	RO										RW		WO	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_MASK_STATUS	[31]	RO	‘b0	Interrupt Mask status and should be cleared by asserting INT_CLR; Only would be active when INT_EN active high.
INT_RAW_STATUS	[30]	RO	‘b0	Interrupt raw status and should be cleared by asserting INT_CLR;
INT_CLR	[29]	WO	‘b0	Writing “1” to this bit will clear the interrupt raw status;
INT_EN	[28]	RW	‘b0	0 : By default, disable busmon interrupt; 1 : Enable busmon interrupt;
	[27:6]	RO	‘b0	Reserved.
CNT_SEL	[5:4]	RW	‘b0	Counter type as following: 2’b00: Busmon Enable; 2’b01: AHB Transcation; 2’b10: AHB Transcation with HREADY; 2’b11: Data Size;
CNT_CLR	[3]	RW	‘b0	Busmon Cnt clear, writing “1” to this bit will clear busmon cnt to zero;
CNT_HOLD	[2]	RW	‘b0	Transaction Counter hold, active HIGH will hold the counter;
CNT_EN	[1]	RW	‘b0	Transaction Counter Enable; 0 : Disable counter; 1 : Enable counter;
CHN_EN	[0]	RW	‘b0	Channel enable: 0: by default, disable bus monitor; 1: Enable bus monitor;

5.7.4.2.2 CHN_CFG

Description：

0x0004	. (Reset to 0x0000_0000)												CHN_CFG			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved.												BURST_CFG			BURST_EN
Type	RO												RW			RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MASTER_CFG				Reserved.			MASTER_EN	SIZE_CFG			SIZE_EN	Reserved		WRITE_CFG	WRITE_EN
Type	RW				RO			RW	RW			RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:20]	RO	‘b0	Reserved.
BURST_CFG	[19:17]	RW	‘b0	AHB HBURST definition: 3’b000 : Single; 3’b001 : INCR; 3’b010 : WRAP4; 3;b011 : INCR4; 3’b100 : WRAP8; 3’b101 : INCR8; 3’b110 : WRAP16; 3’b111 : INCR16;
BURST_EN	[16]	RW	‘b0	HBURST type monitoring enable: 0 : Disable HBURST monitoring; 1 : Enable HBURST monitoring;
MASTER_CFG	[15:12]	RW	‘b0	HMASTER.
	[11:9]	RO	‘b0	Reserved.
MASTER_EN	[8]	RW	‘b0	AHB Hmaster enable, Must be set as default 0.
SIZE_CFG	[7:5]	RW	‘b0	AHB HSIZE monitoring: 000: Byte; 001: Half-word; 010: Word; Others: reserved.
SIZE_EN	[4]	RW	‘b0	HSIZE type monitoring enable; 0 : Disable HSIZE monitoring; 1 : Enable HSIZE monitoring;
	[3:2]	RW	‘b0	Reserved
WRITE_CFG	[1]	RW	‘b0	HWRITE for monitoring:

				0 : HWRITE = 1'b0, read transaction; 1: HWRITE = 1'b1, write transaction;
WRITE_EN	[0]	RW	'b0	HWRITE type monitoring enable; 0 : Dis-able HWRITE monitoring; 1 : Enable HWRITE monitoring;

5.7.4.2.3 ADDR_MIN

Description：

0x0008			. (Reset to 0x0000_0000)													ADDR_MIN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	ADDR_MIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ADDR_MIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
ADDR_MIN	[31: 0]	RW	'b0	AHB minimal address for monitoring; Any access between Max and Min address space may trigger interrupt;

5.7.4.2.4 ADDR_MAX

Description：

0x000C			. (Reset to 0x0000_0000)													ADDR_MAX
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	ADDR_MAX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ADDR_MAX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
ADDR_MAX	[31: 0]	RW	'b0	AHB maxium address for monitoring;

				Any access between Max and Min address space may trigger interrupt;

5.7.4.2.5 DATA_MIN

Description：

0x0010			. (Reset to 0x0000_0000)										DATA_MIN			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DATA_MIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DATA_MIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
DATA_MIN	[31: 0]	RW	‘b0	AHB minimal DATA for monitoring; Any access between Max and Min data space may trigger interrupt;

5.7.4.2.6 DATA_MAX

Description：

0x0014			. (Reset to 0x0000_0000)										DATA_MAX			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DATA_MAX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DATA_MAX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
DATA_MAX	[31: 0]	RW	‘b0	AHB maxium Data for monitoring; Any access between Max and Min Data space may trigger interrupt;

5.7.4.2.7 DATA_MASK

Description：

0x0018			. (Reset to 0x0000_0000)													DATA_MASK
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DATA_MASK															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DATA_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
DATA_MASK	[31: 0]	RW	‘b0	Data_mask

5.7.4.2.8 MATCH_ADDR

Description：

0x001C			. (Reset to 0x0000_0000)													MATCH_ADDR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	MATCH_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MATCH_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
MATCH_ADDR	[31: 0]	RO	‘b0	Captured Address, which triggered interrupt;

5.7.4.2.9 MATCH_DATA

Description：

0x0020			. (Reset to 0x0000_0000)										MATCH_DATA			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	MATCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MATCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
MATCH_DATA	[31: 0]	RO	‘b0	Captured Data, which triggered interrupt;

5.7.4.2.10 BUSMON_CNT

Description：

0x0024			. (Reset to 0x0000_0000)										BUSMON_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	BUSMON_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BUSMON_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
BUSMON_CNT	[31: 0]	RO	‘b0	Transaction counter;

5.8 RTC Timer

5.8.1 Overview

SC6820 provides an always-powered-on region to count second, minute, hour and day, and to perform alarm functions.

5.8.2 Features

Main feature list:

- Second counter: 0 – 59
- Minute counter: 0 – 59

- Hour counter: 0 – 23
- Day counter: 0 – 65535
- Second, minute, hour and day numbers can be changed by software
- Provide second interrupt, minute interrupt, hour interrupt and day interrupt
- Provide configurable alarm function
- All interrupts can be used to wakeup system from deep sleep
- Alarm interrupt can be used to power up system from power-down status
- RTCVDD is the power supply for second counter, minute counter, hour counter, day counter, and alarm function. And this power is always on.

5.8.3 Signal Description

5.8.4 Function Description

SC6820 provides a very small always-powered-on region supplied by RTCVDD. Second counter, minute counter, hour counter, day counter, and alarm function are put in this region, so these functions always work even if the base band chip enters power-down mode.

Second counter, minute counter, hour counter and day counter are used to count second, minute, hour and day values, and to issue second, minute, hour and day interrupts. The value of these four counters can be changed by software, but the changing time is very long, about 125 ms. In order to improve software efficiency, SC6820 provides four interrupts to inform software changing completion. The changes to four counters are independent, and it does not need waiting for first changing to complete before changing next one.

Alarm function is used to generate alarm interrupt to inform software, to wake up system, or to power up system. Alarm second, minute, hour and day values are stored in the RTCVDD power domain, and these four registers can be changed by software. It also takes long time to change these registers, and another set of four interrupts are provided for changing completion. Same as the above, the changes to the four registers are independent, and it does not need waiting for first changing to complete before changing next one.

Because RTC timers are in RTC clock domain, all interrupts can be used to wakeup system from deep sleep. Another important function is alarm interrupt can power up base band from power-down mode.

5.8.5 Control Registers

5.8.5.1 Memory map

ARM base address: 0x8200_0080

Address Offset	Register Name	Default Value
0x0000	RTC_SEC_CNT	-
0x0004	RTC_MIN_CNT	-
0x0008	RTC_HOUR_CNT	-
0x000C	RTC_DAY_CNT	-
0x0010	RTC_SEC_CNT_UPD	32’h00000000
0x0014	RTC_MIN_ CNT_UPD	32’h00000000

0x0018	RTC_HOUR_ CNT_UPD	32'h00000000
0x001C	RTC_DAY_ CNT_UPD	32'h00000000
0x0020	RTC_SEC_ALM_UPD	32'h00000000
0x0024	RTC_MIN_ALM_UPD	32'h00000000
0x0028	RTC_HOUR_ALM_UPD	32'h00000000
0x002C	RTC_DAY_ALM_UPD	32'h00000000
0x0030	RTC_INT_EN	32'h00000000
0x0034	RTC_INT_RAW_STS	32'h00000000
0x0038	RTC_INT_CLR	32'h00000000
0x003C	RTC_INT_MASK_STS	32'h00000000
0x0040	RTC_SEC_ALM_CNT	-
0x0044	RTC_MIN_ALM_CNT	-
0x0048	RTC_HRS_ALM_CNT	-
0x004C	RTC_DAY_ALM_CNT	-
0x0050	RTC_SPG_CNT	-
0x0054	RTC_SPG_CNT_UPD	32'h00000000

5.8.5.2 Register Descriptions

5.8.5.2.1 RTC_SEC_CNT

Description：Current second counter value

0x0000			RTC Second Counter													RTC_SEC_CNT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										RTC_SEC_CNT					
Type	RO										RO					
Reset	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-

Field Name	Bit	Type	Reset Value	Description
	[31:6]	RO	26'h0	Reserved
RTC_SEC_CNT	[5:0]	RO	-	Current second counter value

5.8.5.2.2 RTC_MIN_CNT

Description：Current minute counter value

0x0004	RTC Minute Counter														RTC_MIN_CNT	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										RTC_MIN_CNT					
Type	RO										RO					
Reset	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-

Field Name	Bit	Type	Reset Value	Description
	[31:6]	RO	26'h0	Reserved
RTC_MIN_CNT	[5:0]	RO	-	Current minute counter value

5.8.5.2.3 RTC_HRS_CNT

Description：Current hour counter value

0x0008	RTC Hour Counter														RTC_HRS_CNT	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											RTC_HRS_CNT				
Type	RO											RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-

Field Name	Bit	Type	Reset Value	Description
	[31:5]	RO	27'h0	Reserved
RTC_HRS_CNT	[4:0]	RO	-	Current hour counter value

5.8.5.2.4 RTC_DAY_CNT

Description：Current day counter value

0x000C			RTC Day Counter											RTC_DAY_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_CNT															
Type	RO															
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
RTC_DAY_CNT	[15:0]	RO	-	Current day counter value

5.8.5.2.5 RTC_SEC_CNT_UPD

Description：Current second counter update

0x0010			RTC Second Counter Update (reset 0x0000_0000)											RTC_SEC_CNT_UPD		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										RTC_SEC_CNT_UPD					
Type	RO										R/W					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:6]	RO	26'h0	Reserved
RTC_SEC_CNT_UPD	[5:0]	R/W	6'h0	Current second counter update Write new counter value to this register to start an second counter updating operation in RTCVDD domain. Reading this register can get recent updating value

5.8.5.2.6 RTC_MIN_CNT_UPD

Description：Current minute counter update

0x0014			RTC Minute Counter Update (reset 0x0000_0000)													RTC_MIN_CNT_UPD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										RTC_MIN_CNT_UPD					
Type	RO										R/W					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:6]	RO	26'h0	Reserved
RTC_MIN_CNT_UPD	[5:0]	R/W	6'h0	Current minute counter update Write new counter value to this register to start an minute counter updating operation in RTCVDD domain. Reading this register can get recent updating value

5.8.5.2.7 RTC_HRS_CNT_UPD

Description：Current hour counter update

0x0018			RTC Hour Counter Update (reset 0x0000_0000)													RTC_HRS_CNT_UPD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											RTC_HRS_CNT_UPD				
Type	RO											R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:5]	RO	27'h0	Reserved
RTC_MIN_CNT_UPD	[4:0]	R/W	5'h0	Current hour counter update Write new counter value to this register to start an hour counter updating operation in RTCVDD domain. Reading this register can get recent updating value

5.8.5.2.8 RTC_DAY_CNT_UPD

Description：Current day counter update

0x001C			RTC Day Counter Update (reset 0x0000_0000)										RTC_DAY_CNT_UPD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_CNT_UPD															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
RTC_MIN_CNT_UPD	[15:0]	R/W	16'h0	Current hour counter update Write new counter value to this register to start an day counter updating operation in RTCVDD domain. Reading this register can get recent updating value

5.8.5.2.9 RTC_SEC_ALM_UPD

Description：Current second alarm update

0x0020			RTC Second Alarm Update (reset 0x0000_0000)										RTC_SEC_ALM_UPD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										RTC_SEC_ALM_UPD					
Type	RO										R/W					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:6]	RO	26'h0	Reserved
RTC_SEC_ALM_UPD	[5:0]	R/W	6'h0	Current second alarm update

				Write new counter value to this register to start an second alarm updating operation in RTCVDD domain. Reading this register can get recent updating value

5.8.5.2.10 RTC_MIN_ALM_UPD

Description：Current minute alarm update

0x0024			RTC Minute Alarm Update (reset 0x0000_0000)													RTC_MIN_ALM_UPD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										RTC_MIN_ALM_UPD					
Type	RO										R/W					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:6]	RO	26'h0	Reserved
RTC_MIN_ALM_UPD	[5:0]	R/W	6'h0	Current minute alarm update Write new counter value to this register to start an minute alarm updating operation in RTCVDD domain. Reading this register can get recent updating value

5.8.5.2.11 RTC_HRS_ALM_UPD

Description：Current hour alarm update

0x0028			RTC Hour Alarm Update (reset 0x0000_0000)													RTC_HRS_ALM_UPD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											RTC_HRS_ALM_UPD				
Type	RO											R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

	[31:5]	RO	27'h0	Reserved
RTC_MIN_ALM_UPD	[4:0]	R/W	5'h0	Current hour alarm update Write new counter value to this register to start an hour alarm updating operation in RTCVDD domain. Reading this register can get recent updating value

5.8.5.2.12 RTC_DAY_ALM_UPD

Description：Current day alarm update

0x002C			RTC Day Alarm Update (reset 0x0000_0000)										RTC_DAY_ALM_UPD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_ALM_UPD															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name / Bit	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
RTC_MIN_ALM_UPD	[15:0]	R/W	16'h0	Current day alarm update Write new counter value to this register to start an day alarm updating operation in RTCVDD domain. Reading this register can get recent updating value

5.8.5.2.13 RTC_INT_EN

Description：Interrupt enable and hour format control

0x0030			RTC Day Counter													RTC_DAY_CNT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_ALM_UPD_INT_EN	RTC_HOUR_ALM_UPD_INT_EN	RTC_MIN_ALM_UPD_INT_EN	RTC_SEC_ALM_UPD_INT_EN	RTC_DAY_CNT_UPD_INT_EN	RTC_HOUR_CNT_UPD_INT_EN	RTC_MIN_CNT_UPD_INT_EN	RTC_SEC_CNT_UPD_INT_EN	RTC_SPG_CNT_UPD_INT_EN	Reserved	RTC_HOUR_FORMAT_SEL	RTC_ALM_INT_EN	RTC_DAY_INT_EN	RTC_HOUR_INT_EN	RTC_MIN_INT_EN	RTC_SEC_INT_EN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
RTC_DAY_ALM_UPD_INT_EN	[15]	RW	1'h0	Day alarm updating complete interrupt enable 0: disabled 1: enabled
RTC_HOUR_ALM_UPD_INT_EN	[14]	RW	1'h0	Hour alarm updating complete interrupt enable
RTC_MIN_ALM_UPD_INT_EN	[13]	RW	1'h0	Minute alarm updating complete interrupt enable
RTC_SEC_ALM_UPD_INT_EN	[12]	RW	1'h0	Second alarm updating complete interrupt enable
RTC_DAY_CNT_UPD_INT_EN	[11]	RW	1'h0	Day counter updating complete interrupt enable
RTC_HOUR_CNT_UPD_INT_EN	[10]	RW	1'h0	Hour counter updating complete interrupt enable
RTC_MIN_CNT_UPD_INT_EN	[9]	RW	1'h0	Minute counter updating complete interrupt enable
RTC_SEC_CNT_UPD_INT_EN	[8]	RW	1'h0	Second counter updating complete interrupt enable
RTC_SPG_CNT_UPD_INT_EN	[7]	RW	1'h0	Spg counter updating complete interrupt enable
	[6]	RO	1'h0	Reserved
	[5]	RW	1'h0	Hour format select 0: The read back hour count is formatted as 0 to 23. 1: The read back hour count is formatted as 0 to 11, and bit 4 represent AM or PM – AM is 0 and PM is 1.

RTC_ALM_INT_EN	[4]	RW	1'h0	alarm interrupt enable
RTC_DAY_INT_EN	[3]	RW	1'h0	day interrupt enable
RTC_HOUR_INT_EN	[2]	RW	1'h0	hour interrupt enable
RTC_MIN_INT_EN	[1]	RW	1'h0	minute interrupt enable
RTC_SEC_INT_EN	[0]	RW	1'h0	Second interrupt enable

5.8.5.2.14 RTC_INT_RAW_STS

Description：Interrupt raw status

0x0034			RTC Day Counter												RTC_DAY_CNT	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_ALM_UPD_INT_RAW_STS	RTC_HOUR_ALM_UPD_INT_RAW_STS	RTC_MIN_ALM_UPD_INT_RAW_STS	RTC_SEC_ALM_UPD_INT_RAW_STS	RTC_DAY_CNT_UPD_INT_RAW_STS	RTC_HOUR_CNT_UPD_INT_RAW_STS	RTC_MIN_CNT_UPD_INT_RAW_STS	RTC_SEC_CNT_UPD_INT_RAW_STS	RTC_SPG_CNT_UPD_INT_RAW_STS	Reserved	RTC_ALM_INT0_RAW_STS	RTC_ALM_INT_RAW_STS	RTC_DAY_INT_RAW_STS	RTC_HOUR_INT_RAW_STS	RTC_MIN_INT_RAW_STS	RTC_SEC_INT_RAW_STS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
RTC_DAY_ALM_UPD_INT_RAW_STS	[15]	RO	1'h0	Day alarm updating complete interrupt raw status
RTC_HOUR_ALM_UPD_INT_RAW_STS	[14]	RO	1'h0	Hour alarm updating complete interrupt raw status
RTC_MIN_ALM_UPD_INT_RAW_STS	[13]	RO	1'h0	Minute alarm updating complete interrupt raw status
RTC_SEC_ALM_UPD_INT_RAW_STS	[12]	RO	1'h0	Second alarm updating complete interrupt raw status
RTC_DAY_CNT_UPD_INT_RAW_STS	[11]	RO	1'h0	Day counter updating complete interrupt raw status
RTC_HOUR_CNT_UPD_INT_RAW_STS	[10]	RO	1'h0	Hour counter updating complete interrupt raw status
RTC_MIN_CNT_UPD_INT_RAW_STS	[9]	RO	1'h0	Minute counter updating complete interrupt raw status
RTC_SEC_CNT_UPD_INT_RAW_STS	[8]	RO	1'h0	Second counter updating

				complete interrupt raw status
RTC_SPG_CNT_UPD_INT_RAW_STS	[7]	RO	1'h0	Spg counter updating complete interrupt raw status
	[6]	RO	1'h0	Reserved
RTC_ALM_INT0_RAW_STS	[5]	RO	1'h0	alarm interrupt0 raw status
RTC_ALM_INT_RAW_STS	[4]	RO	1'h0	alarm interrupt raw status
RTC_DAY_INT_RAW_STS	[3]	RO	1'h0	day interrupt raw status
RTC_HOUR_INT_RAW_STS	[2]	RO	1'h0	hour interrupt raw status
RTC_MIN_INT_RAW_STS	[1]	RO	1'h0	minute interrupt raw status
RTC_SEC_INT_RAW_STS	[0]	RO	1'h0	Second interrupt raw status

5.8.5.2.15 RTC_INT_CLR

Description：Interrupt clear

0x0038	RTC Day Counter															RTC_DAY_CNT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_ALM_UPD_INT_CLR	RTC_HOUR_ALM_UPD_INT_CLR	RTC_MIN_ALM_UPD_INT_CLR	RTC_SEC_ALM_UPD_INT_CLR	RTC_DAY_CNT_UPD_INT_CLR	RTC_HOUR_CNT_UPD_INT_CLR	RTC_MIN_CNT_UPD_INT_CLR	RTC_SEC_CNT_UPD_INT_CLR	RTC_SPG_CNT_UPD_INT_CLR	Reserved		RTC_ALM_INT_CLR	RTC_DAY_INT_CLR	RTC_HOUR_INT_CLR	RTC_MIN_INT_CLR	RTC_SEC_INT_CLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	RO		WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
RTC_DAY_ALM_UPD_INT_CLR	[15]	WO	1'h0	Day alarm updating complete interrupt clear Write 1 to this bit to clear corresponding interrupt
RTC_HOUR_ALM_UPD_INT_CLR	[14]	WO	1'h0	Hour alarm updating complete interrupt clear
RTC_MIN_ALM_UPD_INT_CLR	[13]	WO	1'h0	Minute alarm updating complete interrupt clear
RTC_SEC_ALM_UPD_INT_CLR	[12]	WO	1'h0	Second alarm updating complete interrupt clear
RTC_DAY_CNT_UPD_INT_CLR	[11]	WO	1'h0	Day counter updating complete

				interrupt clear
RTC_HOUR_CNT_UPD_INT_CLR	[10]	WO	1'h0	Hour counter updating complete interrupt clear
RTC_MIN_CNT_UPD_INT_CLR	[9]	WO	1'h0	Minute counter updating complete interrupt clear
RTC_SEC_CNT_UPD_INT_CLR	[8]	WO	1'h0	Second counter updating complete interrupt clear
RTC_SPG_CNT_UPD_INT_CLR	[7]	WO	1'h0	Spg counter updating complete interrupt clear
	[6:5]	RO	2'h0	Reserved
RTC_ALM_INT_CLR	[4]	WO	1'h0	alarm interrupt clear
RTC_DAY_INT_CLR	[3]	WO	1'h0	day interrupt clear
RTC_HOUR_INT_CLR	[2]	WO	1'h0	hour interrupt clear
RTC_MIN_INT_CLR	[1]	WO	1'h0	minute interrupt clear
RTC_SEC_INT_CLR	[0]	WO	1'h0	Second interrupt clear

5.8.5.2.16 RTC_INT_MASK_STS

Description：Interrupt masked status

0x003C			RTC Day Counter										RTC_DAY_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_ALM_UPD_INT_MASK_STS	RTC_HOUR_ALM_UPD_INT_MASK_STS	RTC_MIN_ALM_UPD_INT_MASK_STS	RTC_SEC_ALM_UPD_INT_MASK_STS	RTC_DAY_CNT_UPD_INT_MASK_STS	RTC_HOUR_CNT_UPD_INT_MASK_STS	RTC_MIN_CNT_UPD_INT_MASK_STS	RTC_SEC_CNT_UPD_INT_MASK_STS	RTC_SPG_CNT_UPD_INT_MASK_STS	Reserved		RTC_ALM_INT_MASK_STS	RTC_DAY_INT_MASK_STS	RTC_HOUR_INT_MASK_STS	RTC_MIN_INT_MASK_STS	RTC_SEC_INT_MASK_STS
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO		R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
RTC_DAY_ALM_UPD_INT_MASK_STS	[15]	RW	1'h0	Day alarm updating complete interrupt masked status Write 1 to this bit to masked status corresponding interrupt
RTC_HOUR_ALM_UPD_INT_MASK_STS	[14]	RW	1'h0	Hour alarm updating complete

				interrupt masked status
RTC_MIN_ALM_UPD_INT_MASK_STS	[13]	RW	1'h0	Minute alarm updating complete interrupt masked status
RTC_SEC_ALM_UPD_INT_MASK_STS	[12]	RW	1'h0	Second alarm updating complete interrupt masked status
RTC_DAY_CNT_UPD_INT_MASK_STS	[11]	RW	1'h0	Day counter updating complete interrupt masked status
RTC_HOUR_CNT_UPD_INT_MASK_STS	[10]	RW	1'h0	Hour counter updating complete interrupt masked status
RTC_MIN_CNT_UPD_INT_MASK_STS	[9]	RW	1'h0	Minute counter updating complete interrupt masked status
RTC_SEC_CNT_UPD_INT_MASK_STS	[8]	RW	1'h0	Second counter updating complete interrupt masked status
RTC_SPG_CNT_UPD_INT_MASK_STS	[7]	RW	1'h0	Spg counter updating complete interrupt masked status
	[6:5]	RO	2'h0	Reserved
RTC_ALM_INT_MASK_STS	[4]	RW	1'h0	alarm interrupt masked status
RTC_DAY_INT_MASK_STS	[3]	RW	1'h0	day interrupt masked status
RTC_HOUR_INT_MASK_STS	[2]	RW	1'h0	hour interrupt masked status
RTC_MIN_INT_MASK_STS	[1]	RW	1'h0	minute interrupt masked status
RTC_SEC_INT_MASK_STS	[0]	RW	1'h0	Second interrupt masked status

5.8.5.2.17 RTC_SEC_ALM_CNT

Description：Current second alarm value

0x0040	RTC Second alarm												RTC_SEC_ALM_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										RTC_SEC_ALM_CNT					
Type	RO										RO					
Reset	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-

Field Name	Bit	Type	Reset Value	Description

	[31:6]	RO	26'h0	Reserved
RTC_SEC_ALM_CNT	[5:0]	RO	-	Current second alarm value

5.8.5.2.18 RTC_MIN_ALM_CNT

Description：Current minute alarm value

0x0044	RTC Minute alarm												RTC_MIN_ALM_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										RTC_MIN_ALM_CNT					
Type	RO										RO					
Reset	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-

Field Name	Bit	Type	Reset Value	Description
	[31:6]	RO	26'h0	Reserved
RTC_MIN_ALM_CNT	[5:0]	RO	-	Current minute alarm value

5.8.5.2.19 RTC_HRS_ALM_CNT

Description：Current hour alarm value

0x0048	RTC Hour Alarm												RTC_HRS_ALM_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											RTC_HRS_ALM_CNT				
Type	RO											RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-

Field Name	Bit	Type	Reset Value	Description
	[31:5]	RO	27'h0	Reserved
RTC_HRS_ALM_CNT	[4:0]	RO	-	Current hour alarm value

5.8.5.2.20 RTC_DAY_ALM_CNT

Description：Current day alarm value

0x004C			RTC Day Alarm										RTC_DAY_ALM_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_CNT															
Type	RO															
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
RTC_DAY_ALM_CNT	[15:0]	RO	-	Current day alarm value

5.8.5.2.21 RTC_SPG_CNT

Description：Current spg counter value

0x0050			RTC SPG Counter Value													RTC_SPG_CNT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								RTC_SPG_CNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
RTC_SPG_CNT	[7:0]	RO	-	Current spg counter value

5.8.5.2.22 RTC_SPG_CNT_UPD

Description：Current spg counter update

0x0054			RTC SPG Counter Update (reset 0x0000_0000)										RTC_SPG_CNT_UPD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								RTC_SPG_CNT_UPD							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
RTC_SPG_CNT_UPD	[7:0]	R/W	8'h0	Current spg counter update Write new counter value to this register to start an spgd counter updating operation in RTCVDD domain. Reading this register can get recent updating value

5.8.6 Application Notes

Second counter, minute counter, hour counter and day counter always run in RTCVDD domain. However, if software wants to access or control these functions, it should set rtc_eb and rtc_rtc_eb first.

After setting rtc_eb and rtc_rtc_eb, software can get second, minute, hour and day counter values by reading rtc_sec_cnt, rtc_min_cnt, rtc_hour_cnt and rtc_day_cnt. Double-reading method is still recommended, like the system timer reading.

RTC timers provide second interrupt, minute interrupt, hour interrupt and day interrupt. Software can enable these interrupts by setting 1 to rtc_sec_int_en, rtc_min_int_en, rtc_sec_hour_en and rtc_day_int_en, check status by reading rtc_sec_int_mask_sts, rtc_min_int_mask_sts, rtc_hour_int_mask_sts and rtc_day_int_mask_sts, and clear these interrupts by writing 1 to rtc_sec_int_clr, rtc_min_int_clr, rtc_hour_int_clr and rtc_day_int_clr.

Software can update the four counter values by writing new value to rtc_sec_cnt_upd, rtc_min_cnt_upd, rtc_hour_cnt_upd or rtc_day_cnt_upd. However, the changing time is very long, about 125 ms. In order to improve software efficiency, RTC timer provides four interrupts to inform software changing completion. Software can enable these interrupts by setting rtc_sec_cnt_upd_int_en, rtc_min_cnt_upd_int_en, rtc_hour_cnt_upd_int_en and rtc_day_cnt_upd_int_en, check status by reading rtc_sec_cnt_upd_int_mask_sts, rtc_min_cnt_upd_int_mask_sts, rtc_hour_cnt_upd_int_mask_sts and rtc_day_cnt_upd_int_mask_sts, and clear these interrupts by writing 1 to rtc_sec_cnt_upd_int_clr, rtc_min_cnt_upd_int_clr, rtc_cnt_upd_hour_int_clr and rtc_day_cnt_upd_int_clr. The changes to four counters are independent, and it does not need waiting for first changing to complete before changing next one.

RTC timer provides an alarm function. If an alarm occurs, alarm interrupt is issued. Software can enable this interrupt by setting rtc_alm_int_en, check status by reading rtc_alm_int_mask_sts, and clear these interrupts by writing 1 to rtc_alm_int_clr.

Alarm value can be configured by writing expected value to rtc_sec_alm_upd, rtc_min_alm_upd, rtc_hour_alm_upd and rtc_day_alm_upd. However, the changing time is very long, about 125 ms. In order to improve software efficiency, RTC timer provides four interrupts to inform software changing completion. Software can enable these interrupts by setting rtc_sec_alm_upd_int_en, rtc_min_alm_upd_int_en, rtc_hour_alm_upd_int_en and rtc_day_alm_upd_int_en, check status by reading rtc_sec_alm_upd_int_mask_sts, rtc_min_alm_upd_int_mask_sts, rtc_hour_alm_upd_int_mask_sts and rtc_day_alm_upd_int_mask_sts, and clear these interrupts by writing 1 to rtc_sec_alm_upd_int_clr, rtc_min_alm_upd_int_clr, rtc_alm_upd_hour_int_clr and rtc_day_alm_upd_int_clr. The changes to the four counters are independent, and it does not need waiting for first changing to complete before changing next one.

Because RTC timers are in RTC clock domain, all interrupts can be used to wakeup system from deep sleep. Another important function is alarm interrupt can power up base band chip from power-down mode.

5.9 General Purpose Timer

5.9.1 Overview

The module includes three general-purpose timers, two RTC-clock trigged asynchronous timers, and one PCLK trigged synchronous timer.

5.9.2 Features

RTC clock trigged timers:

- Two independent RTC clock trigged timers
- 32-bit decreasing counter
- Support one-time mode and period mode
- Support configurable counting value
- Can be used as wakeup source during deep sleep

PCLK clock trigged timer:

- One PCLK clock trigged timer
- 32-bit decreasing counter
- Support one-time mode and period mode
- Support configurable counting value
- Cannot be used as wakeup source during deep sleep

5.9.3 Signal Description

Null

5.9.4 Function Description

The MCU sub-system provides three general-purpose timers. Timer 0 and Timer 1 are trigged by RTC clock, which is 32.768KHz, and Timer 2 is trigged by PCLK, which is 26MHz. These three timers can be controlled independently.

5.9.4.1 RTC Clock Trigged Timers

Timer 0 and Timer 1 are trigged by RTC clock, which is 32.768KHz. So the counting step is about 30.5us.

Each timer has a 32-bit decreasing counter. This kind of timer provides two operating modes: one-time mode and period mode.

If the timer is configured in one-time mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued. The counter stays at 0 until software load it again.

If the timer is configured in period mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued, and counter is reloaded by setting value, and then counter continues to decrease from setting value.

Because trigging clock is RTC clock, these two timers can be used to wake up system during deep sleep.

5.9.4.2 PCLK Trigged Timers

Timer 2 is trigged by PCLK, which is 26MHz. So the counting step is about 38.5ns.

This timer has a 32-bit decreasing counter. This timer provides two operating modes: one-time mode and period mode.

If the timer is configured in one-time mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued. The counter stays at 0 until software load it again.

If the timer is configured in period mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued, and counter is reloaded by setting value, and then counter continues to decrease from setting value.

Because trigging clock is PCLK, this timer cannot be used to wake up system during deep sleep.

5.9.5 Control Registers

5.9.5.1 Memory map

ARM base address: 0x8100_0000

Timer0:

Offset Address	Name	Description
0x0000	TIMER0_LOAD	Timer0 load value
0x0004	TIMER0_VALUE	Timer0 counter value
0x0008	TIMER0_CTL	Timer0 control registers

Offset Address	Name	Description
0x000C	TIMER0_INT	Timer0 interrupt

Timer1:

Offset Address	Name	Description
0x0020	TIMER1_LOAD	Timer1 load value
0x0024	TIMER1_VALUE	Timer1 counter value
0x0028	TIMER1_CTL	Timer1 control registers
0x002C	TIMER1_INT	Timer1 interrupt

Timer2:

Offset Address	Name	Description
0x0040	TIMER2_LOAD	Timer2 load value
0x0044	TIMER2_VALUE	Timer2 counter value
0x0048	TIMER2_CTL	Timer2 control registers
0x004C	TIMER2_INT	Timer2 interrupt

5.9.5.2 Register Descriptions

5.9.5.2.1 TIMER0_LOAD

Description: Timer0 load value

0x0000		Timer0 load value (Reset 0x0000_0000)										TIMER0_LOAD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer0_load															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer0_load															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer0_load	[31:0]	RW	32'h0	Timer0 load value Write to this register will reload the timer with the new value. In one-time mode, this value is

Field Name	Bit	R/W	Reset Value	Description
				the first counting start number. In periodic mode, this value is each counting start number.

5.9.5.2.2 TIMER0_VALUE

Description: Timer0 counter value

0x0004	Timer0 counter value (Reset 0x0000_0000)												TIMER0_VALUE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer0_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer0_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer0_value	[31:0]	RO	32'h0	Timer0 counter value This read-only register indicates current counter value. It's not recommended to read this register in normal usage. Because the counter is in different clock domain with APB, software needs use double-reading method to read this value, like system timer.

5.9.5.2.3 TIMER0_CTL

Description: Timer0 control registers

0x0008			Timer0 control register (Reset 0x0000_0000)													TIMER0_CTL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								timer0_run	timer0_mode	Reserved					
Type	RO								RW	RW	RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:8]	RO	24'h0	Reserved
timer0_run	[7]	RW	1'h0	Timer0 open bit 0: timer stops 1: timer runs
timer0_mode	[6]	RW	1'h0	Timer0 mode select 0: one-time mode 1: period mode
	[5:0]	RO	6'h0	Reserved

5.9.5.2.4 TIMER0_INT

Description: Timer0 interrupt

0x000C			Timer0 interrupt (Reset 0x0000_0000)													TIMER0_INT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											timer0_ld_busy	timer0_int_clr	timer0_int_mask_sts	timer0_int_raw_sts	timer0_int_en
Type	RO											RO	WO	RO	RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:5]	RO	27'h0	Reserved
timer0_ld_busy	[4]	RO	1'h0	Timer0 load busy status

Field Name	Bit	R/W	Default Value	Description
				0: Timer is ready for new loading 1: Last loading is not completed Software must not load new value when this bit is busy, that is, this bit should be checked before any new loading. This bit is set after a new loading, and lasts two or three RTC clock cycles, about 60us - 92us.
timer0_int_clr	[3]	WO	1'h0	Timer0 Interrupt clear Write 1 to this bit to clear interrupt
timer0_int_mask_sts	[2]	RO	1'h0	Timer0 interrupt masked status
timer0_int_raw_sts	[1]	RO	1'h0	Timer0 interrupt raw status
timer0_int_en	[0]	RW	1'h0	Timer0 interrupt enable

5.9.5.2.5 TIMER1_LOAD

Description: Timer1 load value

0x0020	Timer1 load value (Reset 0x0000_0000)												TIMER1_LOAD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer1_load															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer1_load															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer1_load	[31:0]	RW	32'h0	Timer1 load value Write to this register will reload the timer with the new value. In one-time mode, this value is the first counting start number. In period mode, this value is each counting start number.

5.9.5.2.6 TIMER1_VALUE

Description: Timer1 counter value

0x0024	Timer1 counter value (Reset 0x0000_0000)												TIMER1_VALUE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer1_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer1_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer1_value	[31:0]	RO	32'h0	Timer1 counter value This read-only register indicates current counter value. It's not recommended to read this register in normal usage. Because the counter is in different clock domain with APB, software needs use double-reading method to read this value, like system timer.

5.9.5.2.7 TIMER1_CTL

Description: Timer1 control registers

0x0028	Timer1 control register (Reset 0x0000_0000)												TIMER1_CTL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								timer1_run	timer1_mode	Reserved					
Type	RO								RW	RW	RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:8]	RO	24'h0	Reserved
timer1_run	[7]	RW	1'h0	Timer1 open bit 0: timer stops 1: timer runs
timer1_mode	[6]	RW	1'h0	Timer1 mode select 0: one-time mode 1: period mode
	[5:0]	RO	6'h0	Reserved

5.9.5.2.8 TIMER1_INT

Description: Timer1 interrupt

0x002C		Timer1 interrupt (Reset 0x0000_0000)														TIMER1_INT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											timer1_ld_busy	timer1_int_clr	timer1_int_mask_sts	timer1_int_raw_sts	timer1_int_en
Type	RO											RO	WO	RO	RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:5]	RO	27'h0	Reserved
timer1_ld_busy	[4]	RO	1'h0	Timer1 load busy status 0: Timer is ready for new loading 1: Last loading is not completed Software must not load new value when this bit is busy, that is, this bit should be checked before any new loading. This bit is set after a new loading, and lasts two or three RTC clock cycles, about 60us - 92us.
timer1_int_clr	[3]	WO	1'h0	Timer1 Interrupt clear Write 1 to this bit to clear

Field Name	Bit	R/W	Default Value	Description
				interrupt
timer1_int_mask_sts	[2]	RO	1'h0	Timer1 interrupt masked status
timer1_int_raw_sts	[1]	RO	1'h0	Timer1 interrupt raw status
timer1_int_en	[0]	RW	1'h0	Timer1 interrupt enable

5.9.5.2.9 TIMER2_LOAD

Description: Timer2 load value

0x0040			Timer2 load value (Reset 0x0000_0000)										TIMER2_LOAD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer2_load															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer2_load															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer2_load	[31:0]	WO	32'h0	Timer2 load value Write to this register will reload the timer with the new value. In one-time mode, this value is the first counting start number. In period mode, this value is each counting start number.

5.9.5.2.10 TIMER2_VALUE

Description: Timer2 counter value

0x0044	Timer2 counter value (Reset 0x0000_0000)												TIMER2_VALUE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer2_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer2_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer2_value	[31:0]	RO	32'h0	Timer2 counter value This read-only register indicates current counter value.

5.9.5.2.11 TIMER2_CTL

Description: Timer2 control registers

0x0048	Timer2 control register (Reset 0x0000_0000)												TIMER2_CTL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								timer2_run	Timer2_mode	Reserved					
Type	RO								RW	RW	RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:8]	RO	24'h0	Reserved
timer2_run	[7]	RW	1'h0	Timer2 open bit 0: timer stops 1: timer runs
Timer2_mode	[6]	RW	1'h0	Timer2 mode select 0: one-time mode 1: period mode
	[5:0]	RO	6'h0	Reserved

5.9.5.2.12 TIMER2_INT

Description: Timer2 interrupt

0x004C			Timer2 interrupt (Reset 0x0000_0000)													TIMER2_INT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												timer2_int_clr	timer2_int_mask_sts	timer2_int_raw_sts	timer2_int_en
Type	RO												WO	RO	RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:4]	RO	28'h0	Reserved
timer2_int_clr	[3]	WO	1'h0	Timer2 Interrupt clear Write 1 to this bit to clear interrupt
timer2_int_mask_sts	[2]	RO	1'h0	Timer2 interrupt masked status
timer2_int_raw_sts	[1]	RO	1'h0	Timer2 interrupt raw status
timer2_int_en	[0]	RW	1'h0	Timer2 interrupt enable

5.9.6 Application Notes

5.9.6.1 RTC Clock Trigged Timers

When software uses RTC clock trigged timer, it should set tmr_eb bit and tmr_rtc_eb bit in global control register.

Before opening timer0_run or timer1_run, software should configure all control registers – timer0_load or timer1_load, timer0_mode or timer1_mode, timer0_int_en or timer1_int_en.

Then timer0_run or timer1_run is set to 1 to open corresponding timer.

After receiving interrupt issued by a timer, software can check interrupt status by reading timer0_int_mask_sts or timer1_int_mask_sts, and can clear interrupt by writing 1 to timer0_int_clr or timer1_int_clr.

When software completes using RTC clock trigged timer, it should disable timer0_run or timer1_run firstly, then it disable tmr_rtc_eb and tmr_eb in global control registers.

It's IMPORTANT that there are 2-3 RTC clock cycles delay from setting timer0_load or timer1_load to counter setting success because of different clock domains, that is, if N is configured in timer0_load or timer1_load, real counting number is N+2 or N+3.

And during this 2-3 RTC clock cycles loading time, any new loading operation is forbidden. Each Timer provides a bit, timer0_ld_busy or timer1_ld_busy, for software to indicate if timer is busy in last loading. And software should check this bit before any new loading.

It's not recommended to read counter value in normal usage. Because the counter is binary-code counter, not gray-code, and is in different clock domain with APB, software needs use double-reading method to read this value, like system timer.

If the timer is configured in one-time mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued. The counter stays at 0 until software load it again.

If the timer is configured in period mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued, and counter is reloaded by setting value, and then counter continues to decrease from setting value.

5.9.6.2 PCLK Trigged Timers

When software uses PCLK trigged timer, it should set tmr_eb bit in global control register.

Before opening timer2_run, software should configure all control registers – timer2_load, timer2_mode, timer2_int_en.

Then timer2_run is set to 1 to open the timer.

After receiving interrupt issued by a timer, software can check interrupt status by reading timer2_int_mask_sts, and can clear interrupt by writing 1 to timer2_int_clr.

When software completes using PCLK trigged timer, it should disable timer2_run firstly, and then it disable tmr_eb in global control registers.

If the timer is configured in one-time mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued. The counter stays at 0 until software load it again.

If the timer is configured in period mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued, and counter is reloaded by setting value, and then counter continues to decrease from setting value.

5.10 Watchdog Timer

5.10.1 Overview

Watchdog timer is a 32-bit decreasing timer with RTC-clock trigged, and this timer can be used to issue system reset.

5.10.2 Features

- RTC-clock trigged
- 32-bit decreasing timer
- Support 32-bit timer value loading
- Support reset mode for watchdog function
- Support interrupt mode for debug function and timer function

5.10.3 Signal Description

Null

5.10.4 Function Description

After hardware reset, watchdog timer is 32'hFFFF_FFFF.

And after enabled, watchdog timer decreases from the reset value or from software-loading value.

The counting step is one RTC clock cycle.

For reset mode, whenever watchdog timer gets to 0, system reset is issued. Then system reboots, and watchdog timer comes back to 32'hFFFF_FFFF, and all controlled registers and status also come back to reset value, except interrupt raw status. Interrupt raw status can be used to judge if or not system rebooting comes from watchdog reset.

For interrupt mode, watchdog timer runs as a periodic generic timer. If watchdog timer gets to 0, an interrupt is issued, and then the timer is reloaded automatically.

After enabled, watchdog timer can be loaded at any time, and software should guarantee the timer is loaded before it decreases to 0.

Reset mode is used as normal watchdog function. And interrupt mode is used as debug mode or as a generic periodic timer.

5.10.5 Control Registers

5.10.5.1 Memory map

ARM base address: 0x8200_0040

Offset Address	Name	Description
0x0000	WDG_LOAD_LOW	Low 16 bit of watchdog load value
0x0004	WDG_LOAD_HIGH	High16 bit of watchdog load value
0x0008	WDG_CTRL	Watchdog control
0x000C	WDG_INT_CLR	Watchdog interrupt clear
0x0010	WDG_INT_RAW	Watchdog interrupt raw status
0x0014	WDG_INT_MASK	Watchdog interrupt masked status
0x0018	WDG_CNT_LOW	Low 16 bit of watchdog counter value
0x001C	WDG_CNT_HIGH	High16 bit of watchdog counter value
0x0020	WDG_LOCK	Watchdog lock

5.10.5.2 Register Descriptions

5.10.5.2.1 WDG_LOAD_LOW

Description: Low 16 bit of watchdog load value

0x0000			Low 16 bit of watchdog load value (Reset 0x0000_FFFF)										WDG_LOAD_LOW			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdg_load_low															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
wdg_load_low	[15:0]	RW	16'hFFFF	wdg_load_low: low 16 bit of watchdog timer load value. Wdg_load_high: high 16 bit of watchdog timer load value. wdg_load_low and wdg_load_high are used together. Software should write

Field Name	Bit	R/W	Reset Value	Description
				wdg_load_high firstly, and then write wdg_load_low, because writing wdg_load_low can trig loading both wdg_load_low and wdg_load_high to watchdog counter, and writing wdg_load_high cannot trig this event. So software must guarantee wdg_load_high is ready when writing wdg_load_low. In reset mode, software should load new value before timer decrease to 0. In interrupt mode, this value is counting start number. The default value is about 8 seconds.

5.10.5.2.2 WDG_LOAD_HIGH

Description: High 16 bit of watchdog load value

0x0004			High 16 bit of watchdog load value (Reset 0x0000_0003)											WDG_LOAD_HIGH		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdg_load_high															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
wdg_load_high	[15:0]	RW	16'h0003	See wdg_load_low description

5.10.5.2.3 WDG_CTRL

Description: Watchdog control

0x0008			Watchdog control (Reset 0x0000_0000)												WDG_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														wdg_run	wdg_mode
Type	RO														RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:2]	RO	30'h0	Reserved
wdg_run	[1]	RW	1'h0	Watchdog counter open: 0: counter stops. 1: counter runs.
wdg_mode	[0]	RW	1'h0	Watchdog mode 0: reset mode 1: interrupt mode

5.10.5.2.4 WDG_INT_CLR

Description: Watchdog interrupt clear

0x000C			Watchdog interrupt clear (Reset 0x0000_0000)													WDG_INT_CLR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															wdg_int_clr
Type	RO															WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:1]	RO	31'h0	Reserved
wdg_int_clr	[0]	WO	1'h0	Watchdog interrupt clear Write 1 to this bit to clear interrupt

5.10.5.2.5 WDG_INT_RAW

Description: Watchdog interrupt raw status

0x0010	Watchdog interrupt raw status (Reset 0x0000_0000)	WDG_INT_RAW

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											wdg_ld_bus	Reserved			wdg_int_raw
Type	RO											RO	RO			RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:5]	RO	27'h0	Reserved
wdg_ld_busy	[4]	RO	1'h0	Watchdog load busy status 0: Watchdog is ready for new loading 1: Last loading is not completed Software must not load new value when this bit is busy, that is, this bit should be checked before any new loading. This bit is set after a new loading, and lasts two or three RTC clock cycles, about 60us - 92us.
	[3:1]	RO	3'h0	Reserved
wdg_int_raw	[0]	RO	1'h0	Watchdog interrupt raw status

5.10.5.2.6 WDG_INT_MASK

Description: Watchdog interrupt mask status

0x0014			Watchdog interrupt mask status (Reset 0x0000_0000)													WDG_INT_MASK
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															wdg_int_mask
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:1]	RO	31'h0	Reserved
wdg_int_mask	[0]	RO	1'h0	Watchdog interrupt masked status

5.10.5.2.7 WDG_CNT_LOW

Description: Low 16 bit of watchdog counter value

0x0018			Low 16 bit of watchdog counter value (Reset 0x0000_FFFF)													WDG_CNT_LOW
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdg_cnt_low															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
wdg_cnt_low	[15:0]	RO	16'hFFFF	wdg_cnt_low: Low 16 bit of watchdog timer counter value. wdg_cnt_high: High 16 bit of watchdog timer counter value. wdg_cnt_low and wdg_cnt_high are used together. This read-only register indicates current counter value.

Field Name	Bit	R/W	Reset Value	Description
				It's not recommended to read this register in normal usage. Because the counter is in different clock domain with APB, software needs use double-reading method to read this value, like system timer.

5.10.5.2.8 WDG_CNT_HIGH

Description: High 16 bit of watchdog counter value

0x001C			High 16bit of watchdog counter value (Reset 0x0000_FFFF)												WDG_CNT_HIGH	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdg_cnt_high															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
wdg_cnt_high	[15:0]	RO	16'hFFFF	See wdg_cnt_low description.

5.10.5.2.9 WDG_LOCK

Description: Watchdog lock control

0x0020			Watchdog lock control (Reset 0x0000_0000)													WDG_LOCK
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdg_lock															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
wdg_lock	[15:0]	RW	16'h0	Watchdog lock control Write 16'hE551 to this register to unlock watchdog. Write other value to this register to lock watchdog If reading this register, bit-0 is lock status, and other bits are reserved. If watchdog is locked, all control registers cannot be written by software.

5.10.6 Application Notes

When software uses watchdog, it should set wdg_eb bit and wdg_rtc_eb bit in global control register, and also should guarantee arch_rtc_eb is set.

Before configuring watchdog, software should write 16'hE551 to wdg_lock to unlock watchdog.

Then Software configures all control registers – wdg_load_low, wdg_load_high and wdg_mode.

IMPORTANT: wdg_load_high should always be configured before writing wdg_load_low.

Then wdg_run is set to 1 to open counter.

Reset mode is used as normal watchdog function. After enabled, watchdog timer can be loaded at any time, and software should guarantee the timer is reloaded before it decreases to 0.

Whenever watchdog timer gets to 0, system reset is issued. Then system reboots, and watchdog timer comes back to 32'hFFFF_FFFF, and all controlled registers and status also come back to reset value, except interrupt raw status. Interrupt raw status can be used to judge if or not system rebooting comes from watchdog reset.

For interrupt mode, watchdog timer runs as a periodic generic timer. If watchdog timer gets to 0, an interrupt is issued, and then the timer is reloaded automatically.

After receiving interrupt, software can check interrupt status by reading wdg_int_mask, and can clear interrupt by writing 1 to wdg_int_clr.

Interrupt mode is used as debug mode or as a generic periodic timer.

When software completes using watchdog, it should disable wdg_run firstly, then it disable wdg_rtc_eb and wdg_eb in global control registers.

It's IMPORTANT that only writing wdg_load_high cannot reload watchdog. Both wdg_load_low and wdg_load_high should be written if watchdog need reloaded. And software must write wdg_load_high firstly, then write wdg_load_low.

Another IMPORTANT thing is that there are 2-3 RTC clock cycles delay from setting wdg_load_low to counter setting success because of different clock domains, that is, if N is configured in {wdg_load_high,wdg_load_low}, real counting number is N+2 or N+3.

And during this 2-3 RTC clock cycles loading time, any new loading operation is forbidden. Watchdog provides a bit, wdg_ld_busy, for software to indicate if counter is busy in last loading. And software should check this bit before any new loading.

It's not recommended to read counter value in normal usage. Because the counter is binary-code counter, not gray-code, and is in different clock domain with APB, software needs use double-reading method to read this value, like system timer.

5.11 System Timer

5.11.1 Overview

System timer is a 32-bit free-running increasing timer with 1ms step.

5.11.2 Features

- RTC-clock trigged
- 32-bit free-running increasing timer
- 1ms step
- Support one configurable alarm, and support alarm interrupt generating
- Alarm interrupt can be used as wakeup source during deep sleep

5.11.3 Signal Description

Null

5.11.4 Function Description

After hardware reset, system timer is 0. And after enabled, system timer runs from 0 to the maximum, 2^32-1. if system timer gets to the maximum, it return to 0 again and then continue increasing. If no new hardware reset occurs and system timer is kept enabled, nothing can stop system timer.

The counting step is 1ms, that is, the timer increases by 1 per 1ms.

The timer value can be read by software. But double-reading method must be used because of different clock domains.

Based on system timer free running, it provides an alarm function. When system timer value is equal to alarm value, an interrupt is issued, and this interrupt can be used for system wakeup source during deep sleep.

5.11.5 Control Registers

5.11.5.1 Memory map

ARM base address: 0x8700_3000

Offset Address	Name	Description
0x0000	SYST_ALARM	System timer alarm
0x0004	SYST_VALUE	System timer value
0x0008	SYST_INT	System timer interrupt

5.11.5.2 Register Descriptions

5.11.5.2.1 SYST_ALARM

Description: System timer alarm

0x0000			System timer alarm (Reset 0x0000_FFFF)										SYST_ALARM			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	syst_alarm															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	syst_alarm															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
syst_alarm	[31:0]	RW	32'h0000FFFF	System timer alarm value: If system timer is equal to

Field Name	Bit	R/W	Reset Value	Description
				system alarm, one interrupt is issued.

5.11.5.2.2 SYST_VALUE

Description: System timer value

0x0004	System timer value (Reset 0x0000_0000)												SYST_VALUE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	syst_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	syst_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
syst_value	[31:0]	RO	32'h0	System timer value Double-reading method MUST be used to read this register.

5.11.5.2.3 SYST_INT

Description: System timer interrupt

0x000C	System timer interrupt (Reset 0x0000_0000)														SYST_INT	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											syst_int_pls_sts	syst_int_clr	syst_int_mask_sts	syst_int_raw_sts	syst_int_en
Type	RO											RO	WO	RO	RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description

Field Name	Bit	R/W	Default Value	Description
	[31:5]	RO	27'h0	Reserved
syst_int_pls_sts	[4]	RO	1'h0	System timer interrupt pulse status This bit is used only for debugging.
syst_int_clr	[3]	WO	1'h0	System timer Interrupt clear Write 1 to this bit to clear interrupt
syst_int_mask_sts	[2]	RO	1'h0	System timer interrupt masked status
syst_int_raw_sts	[1]	RO	1'h0	System timer interrupt raw status
syst_int_en	[0]	RW	1'h0	System timer interrupt enable

5.11.6 Application Notes

When software begins to use system timer, it should set sys_eb bit and sys_rtc_eb bit in global control register.

When software completes using system timer, it should disable sys_eb bit and sys_rtc_eb bit in global control registers.

When software uses alarm function, it should configure sys_alarm and sys_int_en.

After receiving interrupt issued by a system timer, software can check interrupt status by reading sys_int_mask_sts, and can clear interrupt by writing 1 to sys_int_clr.

IMPORTANT:

System timer is in RTC clock domain, and there is no shadow register for reading. So double-reading method MUST be used to read this register. When software wants to get system timer value, software needs read twice, and if twice numbers are the same, this value is correct, otherwise, software should repeat above operating – next twice reading and comparison.

5.12 MCU JTAG Interface

The MCU JTAG interface consists of the following pins.

- MTDO, test data output
- MTDI, test data input
- MTCK, test clock
- MTMS, test mode
- MTRST_N, test reset, active low

For JTAG timing parameters please see "JTAG Timing".

5.12.1 JTAG Timing

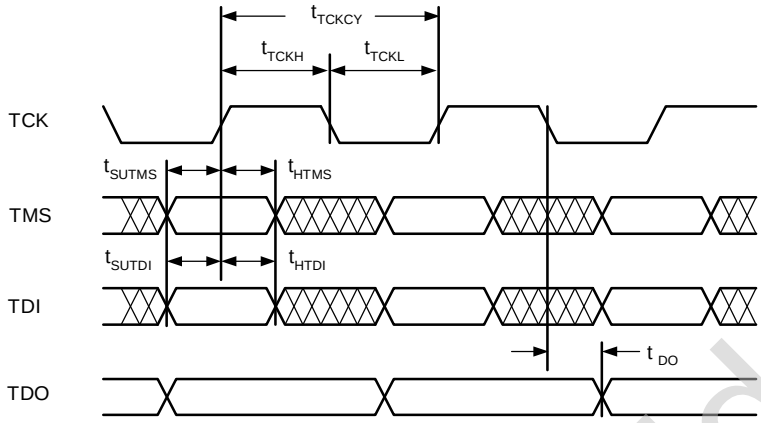


Figure 5-11 JTAG Interface Timing

Table 5-5 JTAG Interface Timing

Symbol	Parameter	Min	Typical	Max	Units
t_{TCKCY}	TCK period	100	200	1000000	ns
t_{TCKH}	TCK pulse width high	50	100	500000	ns
t_{TCKL}	TCK pulse width low	50	100	500000	ns
t_{SUTMS}	TMS Input Set-up Time	44	–	–	ns
t_{HTMS}	TMS Input Hold Time	6	–	–	ns
t_{SUTDI}	TDI Input Set-up Time	44	–	–	ns
t_{HTDI}	TDI Input Hold Time	15	–	–	ns
t_{DO}	TDO Data Output Delay	6	–	?	ns

6 Micro-Controller Unit Peripherals

6.1 USB Device Interface

6.1.1 Overview

The USB interface is a USB device-only controller, fully compliant with the USB 2.0 Specification. The USB 2.0 configurations support high-speed(HS, 480-Mbps), full-speed(FS,12-Mbps), and low-speed(LS, 1.5-Mps) transfers. USB core connects to the industry-standard AMBA High-Performance Bus (AHB) to communicate with the application and system memory, and is fully compliant with AMBA specification, Revision 2.0.

6.1.2 Features

6.1.2.1 General Features

- Supports different clocks for AHB and the PHY interfaces for ease of integration
- Uses the coreConsultant utility to configure the core to user requirements
- Includes USB power management features
- Supports packet-based, Dynamic FIFO memory allocation for endpoints for small FIFOs and flexible, efficient use of RAM
- Uses single-port RAM instead of dual-port RAM for smaller area and lower power.
- Provides support to change an endpoint's FIFO memory size
- Supports endpoint FIFO sizes that are not powers of 2, to allow the use of contiguous memory locations
- Supports the Keep-alive in Low-Speed mode and SOFs in High/Full-Speed modes
- Power-optimized design

6.1.2.2 Application Features

- Interfaces for the application via the AHB:
  - AHB Slave interface for accessing Control and Status Registers(CSRs),the Data FIFO, and queues
  - Optional AHB Master interface for Data FIFO access when Internal DMA is enabled
- Supports only 32-bits data on the AHB
- Supports Little or Big Endian mode(selectable by pin, In our case, the pin is tied to 1'b1 for Big Endian)
- Supports all AHB burst types in AHB Slave interface
- Supports Split, Retry, and Error AHB responses on the AHB Master interface; these are not generated on the AHB Slave interface(That means core itself will not generate split response, but as a master, it can handle split response as retry response. In our case, the AHB bus does not support split transfer, so there won't be any split response occurred.)
- Software-selectable AHB burst type on AHB Master interface
  - If INCR4 is chosen, core only uses INCR4.
  - If INCR8 is chosen, core normally uses INCR8, but at the beginning and at the end of a transfer, it can use INCR4, depending on the size of the transfer.
  - If INCR8 is chosen, core normally uses INCR8, but at the beginning and at the end of a transfer, it can use INCR4, depending on the size of the transfer.
  - If INCR16 is chosen, core normally uses INCR16, but at the beginning and at the end of a transfer, it can use INCR4/INCR8, depending on the size of the transfer.

- Handles the fixed burst address alignment. For example, INCR16 is used only when lower addresses [5:0] are all 0.
- Generates AHB Busy cycles on the AHB Master interface
- Takes care of the 1KB boundary breakup.
- Includes optional interface to an external DMA controller; data is transferred through the AHB Slave interface.

6.1.2.3 USB 2.0 Supported Features

- Complies with the On-The-Go Supplement to the USB 2.0 Specification (Revision 1.0a)
- Operates in High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps) modes
- Supports the UTMI+ Level 3 interface (Revision 1.0, February 25th, 2004). 8-, 16-, and 8/16-bit data buses are supported.
- Supports ULPI interface (Revision 1.1rc, September 1st, 2004) - 8-bit SDR, 4-bit DDR, 6-pin Serial, 3- pin Serial
- Includes automatic ping capabilities

6.1.2.4 Power Optimization Features

- AHB clock gating support during USB Suspend and Session-Off modes
- Data FIFO RAM chip-select deasserted when not active
- Data FIFO RAM clock-gating support

6.1.3 Signal Description

Table 6-1 USB interface pins

Ball No	Signal Name	Pin Name	Type	Power	Value During Reset	Value After Reset	Description
		DP	AIO	VDDUSB	NA	NA	USB data line, positive
		DM	AIO	VDDUSB	NA	NA	USB data line, negative
	tx_enable	LCD_D9	O	VDDUSB	NA	NA	TLL mode tx enable
	tx_dat	LCD_D10	O	VDDUSB	NA	NA	TLL mode tx data 1
	tx_se0	LCD_D11	O	VDDUSB	NA	NA	TLL mode tx data 0
	suspend_out	LCD_D8	O	VDDUSB	NA	NA	TLL mode suspend signal
	rx_rcv	LCD_D15	I	VDDUSB	NA	NA	TLL mode rx receive
	rx_dm	LCD_D14	I	VDDUSB	NA	NA	TLL mode rx data 0
	rx_dp	LCD_D13	I	VDDUSB	NA	NA	TLL mode rx data 1
	int	LCD_D12	I	VDDUSB	NA	NA	TLL mode interrupt

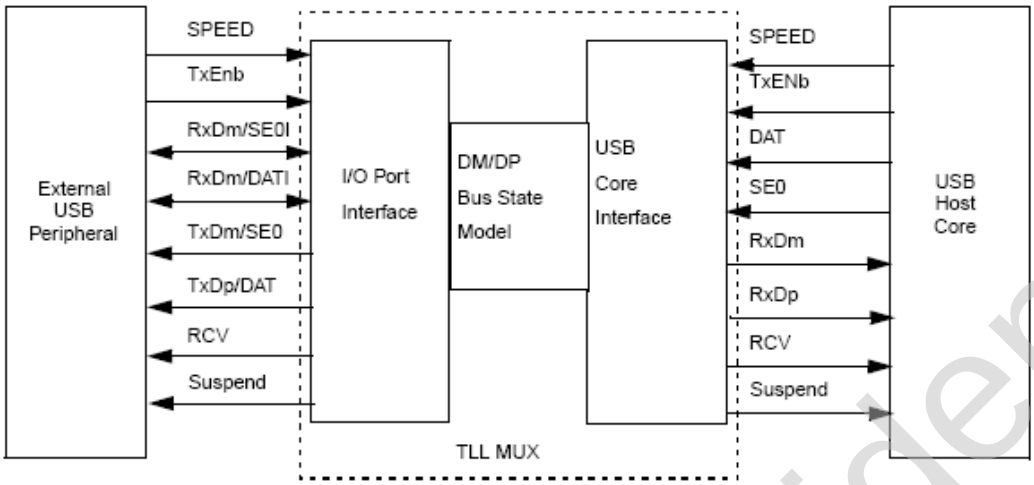


Figure 6-1 TLL mode connection

6.1.4 Function Description

The following figure shows the DWC_otg controller in a typical system. The core interfaces are summarized in the following subsections.

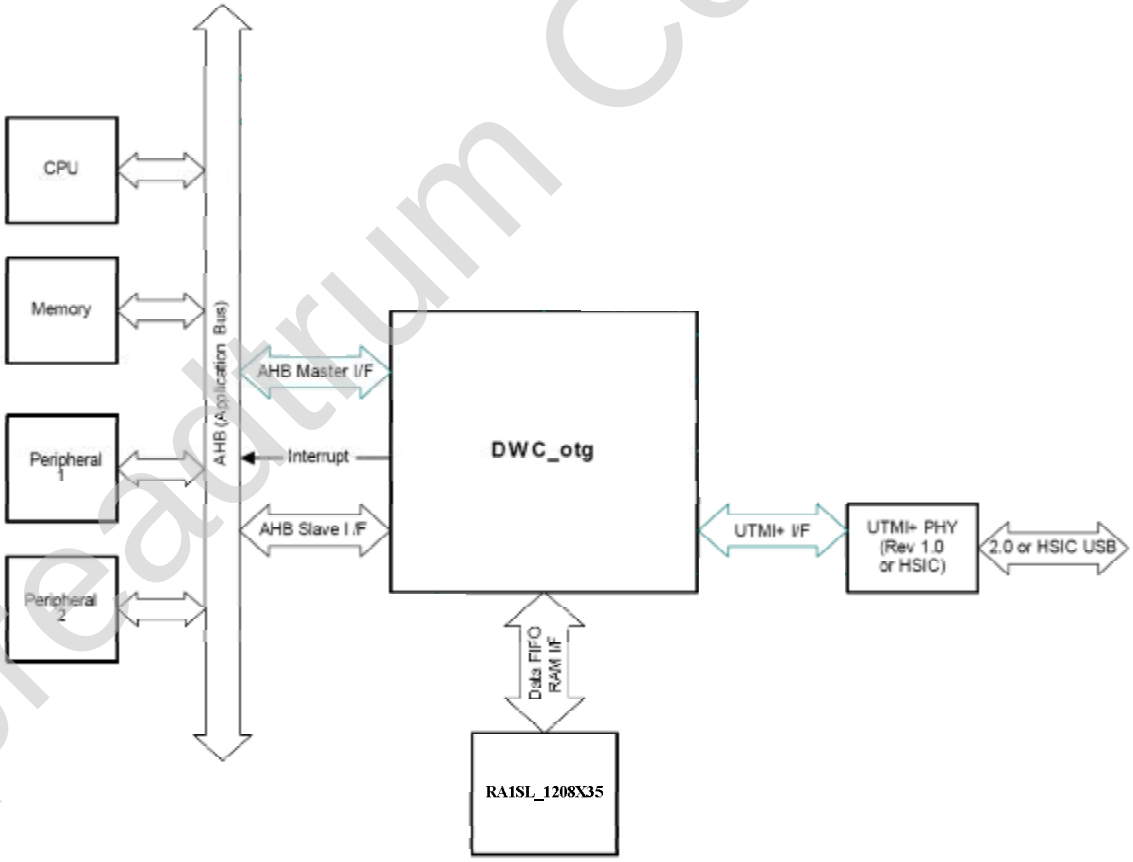


Figure 6-2 System-Level Block Diagram

6.1.5 Control Registers

By reading from and writing to the Control and Status Registers (CSRs) through the AHB Slave interface, your application controls the DWC_otg core. These registers are 32 bits wide, and the addresses are 32-bit block aligned.

Only the Core Global, Power and Clock Gating, Data FIFO Access, and Host Port registers can be accessed in both Host and Device modes. When the DWC_otg core is operating in one mode, either Device or Host, the application must not access registers from the other mode. If an illegal access occurs, a Mode Mismatch interrupt is generated and reflected in the Core Interrupt register (GINTSTS.ModeMis).

The CSR address map is fixed and does not depend on the core's configuration (for example, how many endpoints are implemented). Host and Device mode registers occupy different addresses. All registers are implemented in the AHB Clock domain.

6.1.5.1 Memory map

ARM base address: 0x2030_0000

Offset Address	Name	Description
0x0008	GAHBCFG	Global AHB Configure
0x000C	GUSBCFG	Global USB Configure
0x0010	GRSTCTL	Global Reset Contrl
0x0018	GINTMSK	Global Interrupt Mask
0x001C	GRXSTSR	Global RX Status Register
0x0020	GRXSTSP	Global RX Status POP
0x0024	GRXFSIZ	Global RX FIFO Size
0x0028	GNPTXFSIZ	Global NON-Periodic TX FIFO Size
0x002C	GNPTXSTS	Global NON-Periodic TX Status
0x0040	GSNPSID	Global Synopsys ID
0x0044	GHWCFG1	Global Hardware Configuration 1
0x0048	GHWCFG2	Global Hardware Configuration 2
0x004C	GHWCFG3	Global Hardware Configuration 3
0x0050	GHWCFG4	Global Hardware Configuration 4
0x0104+(n-1)*04	DPTXFSIZn	IN Endpoint Tx FIFO Size n
0x0800	DCFG	Device Configure
0x0804	DCTL	Device Contrl
0x0808	DSTS	Device Status
0x0810	DIEPMSK	Device In Endpoint Mask
0x0814	DOEPMSK	Device Out Endpoint Mask
0x0818	DAINT	Device All Interrupt
0x081C	DAINTMSK	Device All Interrupt Mask
0x0834	DIEPEMPMSK	Device In Endpoint Empty Mask
0x0900	DIEPCTL0	Device In Endpoint Control 0

Offset Address	Name	Description
0x0B00	DOEPCTL0	Device Out Endpoint Control 0
IN EP: 0x900+(n*20)	DIEPCTLn	Device In Endpoint Control n
OUT EP: 0xB00+(n*20)	DOEPCTLn	Device Out Endpoint Control n
IN EP: 0x908+(n*20)	DIEPINTn	Device In Endpoint Int n
OUT EP: 0xB08+(n*20)	DOEPINTn	Device Out Endpoint Int n
0x0910	DIEPTSIZ0	Device In Endpoint Transfer Size 0
0x0B10	DOEPTSIZ0	Device Out Endpoint Transfer Size 0
IN EP: 0x910+(n*20)	DIEPTSIZn	Device In Endpoint Transfer Size n
OUT EP: 0xB10+(n*20)	DOEPTSIZn	Device Out Endpoint Transfer Size n
IN EP: 0x914+(n*20)	DIEPDMAn	Device In Endpoint DMA n
OUT EP: 0xB14+(n*20)	DOEPDMAn	Device Out Endpoint DMA n
0x918h+(n*20h)	DTXFSTSn	Device TX FIFO Status n
0x0E00	PCGCCTL	Power and Clock Gating Control

6.1.5.2 Register Descriptions

6.1.5.2.1 GAHBCFG

Description：（Global AHB Configure）

0x0008		Global AHB Configure(reset 0x0000_0000)											GAHBCFG			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										DMAEN	HBSTLEN				GLBLINTRMSK
Type	RO										RW	RW				RW
Reset	0	0	0	0	0	0	0	0	0	0	0	4'b0				0

Field Name	Bit	Type	Reset Value	Description

DMAEN	[5]	RO	1'b0	• 1'b0: Core operates in Slave mode • 1'b1: Core operates in a DMA mode This bit is always 0 when Slave-Only mode has been selected for the Architecture in coreConsultant (parameter OTG_ARCHITECTURE = 0).
HBSTLEN	[4:1]	R/W	1'b0	Internal DMA Mode—AHB Master burst type: • 4'b0000 Single • 4'b0001 INCR • 4'b0011 INCR4 • 4'b0101 INCR8 • 4'b0111 INCR16 • Others: Reserved
GLBLINTRMSK	[0]	R/W	1'b0	The application uses this bit to mask or unmask the interrupt line assertion to itself. Irrespective of this bit's setting, the interrupt status registers are updated by the core. • 1'b0: Mask the interrupt assertion to the application. • 1'b1: Unmask the interrupt assertion to the application.

6.1.5.2.2 GUSBCFG

Description：（Global USB Configure）

0x000C			Global USB Configure (reset 0x0000_1400)										GUSBCFG			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	CORRUPT TX PACKET	FORCEDEVMODE	Reserved	TXENDDELAY	Reserved					Termseldlpulse	Reserved		ULPICLKSUSM	ULPIAUTORES	ULPIFSLS	Reserved
Type	RW	RW		RW						RW			RW	RW	RW	
Reset	0	0	0	0	5'b0					0	2'b0		0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PHYLPWRCLKSEL	Reserved	Usbtrdtim				Reserved		DDRSEL	PHYSEL	FSINTF	ULPI_UTMI_SEL	PHYIF	TOUTCAL		
Type	RW		RW						RW	RW	RW	RW	RW	RW		
Reset	0	0	4'h5				2'b0		0	0	0	0	0	3'b00		

Field Name	Bit	Type	Reset Value	Description
CORRUPT TX PACKET	[31]	R/W	1'b0	This bit is for debug purposes only. Never set this bit to 1.
FORCEDEVMODE	[30]	R/W	1'b0	Writing a 1 to this bit forces the core to device mode irrespective of utmiotg_iddig input pin. • 1'b0:

				Normal Mode • 1'b1: Force Device Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500 us is sufficient.
	[29]	RO	1'b0	Reserved
TXENDDELAY	[28]	R/W	1'b0	Writing a 1 to this bit enables the TxEndDelay timers in the core as per the section 4.1.5 on Opmode of the USB 2.0 Transceiver Macrocell Interface (UTMI) version 1.05. • 1'b0: Normal mode • 1'b1: Introduce Tx end delay timers
	[27:23]	RO	5'b0	Reserved
TERMSELDLPULSE	[22]	R/W	1'b0	This bit selects utmi_termselect to drive data line pulse during SRP. • 1'b0: Data line pulsing using utmi_txvalid (default). • 1'b1: Data line pulsing using utmi_termsel.
	[21:20]	RO	2'b00	Host only
ULPICLKSUSM	[19]	R/W	1'b0	This bit sets the ClockSuspendM bit in the Interface Control register on the ULPI PHY. This bit applies only in serial modes. • 1'b0: PHY powers down internal clock during suspend. • 1'b1: PHY does not power down internal clock.
ULPIAUTORES	[18]	R/W	1'b0	This bit sets the AutoResume bit in the Interface Control register on the ULPI PHY. 1'b0: PHY does not use AutoResume feature. 1'b1: PHY uses AutoResume feature.
ULPIFSLS	[17]	R/W	1'b0	The application uses this bit to select the FS/LS serial interface for the ULPI PHY. This bit is valid only when the FS serial transceiver is selected on the ULPI PHY. • 1'b0: ULPI interface • 1'b1: ULPI FS/LS serial interface
	[16]	RO	1'b0	Reserved
PHYLPWRCLKSEL	[15]	R/W	1'b0	Selects either 480-MHz or 48-MHz (low-power) PHY mode. In FS and LS modes, the PHY can usually operate on a 48-MHz clock to save power. • 1'b0: 480-MHz Internal PLL clock • 1'b1: 48-MHz External Clock In 480 MHz mode, the UTMI interface operates at either 60 or 30-MHz, depending upon whether 8- or 16-bit data width is selected. In 48-MHz mode, the UTMI interface operates at 48 MHz in FS and LS modes. This bit drives the utmi_fsls_low_power core output signal, and is valid only for UTMI+ PHYs.
	[14]	RO	1'b0	Reserved
USBTRDTIM	[13:10]	R/W	4'h5	Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to

				the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). This must be programmed to • 4'h5: When the MAC interface is 16-bit UTMI+. • 4'h9: When the MAC interface is 8-bit UTMI+.
	[9:8]	RO	2'b0	Reserved
DDRSEL	[7]	R/W	1'b0	The application uses this bit to select a Single Data Rate (SDR) or Double Data Rate (DDR) or ULPI interface. • 1'b0: Single Data Rate ULPI Interface, with 8-bit-wide data bus • 1'b1: Double Data Rate ULPI Interface, with 4-bit-wide data bus
PHYSEL	[6]	R/W	1'b0	The application uses this bit to select either a high-speed UTMI+ or ULPI PHY, or a full-speed transceiver. • 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY • 1'b1: USB 1.1 full-speed serial transceiver
FSINTF	[5]	R/W	1'b0	The application uses this bit to select either a unidirectional or bidirectional USB 1.1 full-speed serial transceiver interface. • 1'b0: 6-pin unidirectional full-speed serial interface • 1'b1: 3-pin bidirectional full-speed serial interface
ULPI_UTMI_SEL	[4]	R/W	1'b0	The application uses this bit to select either a UTMI+ interface or ULPI Interface .• 1'b0: UTMI+ Interface • 1'b1: ULPI Interface
PHYIF	[3]	R/W	1'b0	The application uses this bit to configure the core to support a UTMI+ PHY with an 8- or 16-bit interface. When a ULPI PHY is chosen, this must be set to 8-bit mode. • 1'b0: 8 bits • 1'b1: 16 bits
TOUTCAL	[2:0]	R/W	3'b0	The number of PHY clocks that the application programs in this field is added to the high-speed/full-speed interpacket timeout duration in the core to account for any additional delays introduced by the PHY. This can be required, because the delay introduced by the PHY in generating the line state condition can vary from one PHY to another. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this field based on the speed of enumeration. The number of bit times added per PHY clock are: High-speed operation: • One 30-MHz PHY clock = 16 bit times

				• One 60-MHz PHY clock = 8 bit times Full-speed operation: • One 30-MHz PHY clock = 0.4 bit times • One 60-MHz PHY clock = 0.2 bit times • One 48-MHz PHY clock = 0.25 bit times

6.1.5.2.3 GRSTCTL

Description：（Global USB Configure）

0x0010			Global Reset Contrl(reset 0x8000_0000)												GRSTCTL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	AHB IDLE	DMAREQ	Reserved													
Type	RO	RO	RO													
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved					TXFNUM					TXFFLSH	RXFFLSH	INTKNQFLSH	Reserved	HSFTRST	CSFTRST
Type	RO					RW					R_WS_SC	R_WS_SC	R_WS_SC	R0	R_WS_SC	R_WS_SC
Reset	0	0	0	0	0	5'b0					0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
AHBIDLE	[31]	RO	1'b0	Indicates that the AHB Master State Machine is in the IDLE condition.
DMAREQ	[30]	RO	1'b0	Indicates that the DMA request is in progress. Used for debug.
	[29:11]	RO	19'b0	Reserved
TXFNUM	[10:6]	R/W	5'b0	This is the FIFO number that must be flushed using the TxFIFO Flush bit. This field must not be changed until the core clears the TxFIFO Flush bit. • 5'h0: - Tx FIFO 0 flush in device mode when in dedicated FIFO mode • 5'h1: - TXFIFO 1 flush in device mode when in dedicated FIFO mode • 5'h2: - TXFIFO 2 flush in device mode when in dedicated FIFO mode ... • 5'hF:

				- TXFIFO 15 flush in device mode when in dedicated FIFO mode • 5'h10: Flush all the transmit FIFOs in device or host mode.
TXFFLSH	[5]	R_WS_SC	5'b0	This bit selectively flushes a single or all transmit FIFOs, but cannot do so if the core is in the midst of a transaction. The application must write this bit only after checking that the core is neither writing to the TxFIFO nor reading from the TxFIFO. Verify using these registers: • Read—NAK Effective Interrupt ensures the core is not reading from the FIFO • Write—GRSTCTL.AHBIdle ensures the core is not writing anything to the FIFO. Flushing is normally recommended when FIFOs are reconfigured or when switching between Shared FIFO and Dedicated Transmit FIFO operation. FIFO flushing is also recommended during device endpoint disable. The application must wait until the core clears this bit before performing any operations. This bit takes eight clocks to clear, using the slower clock of phy_clk or hclk.
RXFFLSH	[4]	R_WS_SC	1'b0	The application can flush the entire RxFIFO using this bit, but must first ensure that the core is not in the middle of a transaction. The application must only write to this bit after checking that the core is neither reading from the RxFIFO nor writing to the RxFIFO. The application must wait until the bit is cleared before performing any other operations. This bit requires 8 clocks (slowest of PHY or AHB clock) to clear.
INTKNQFLSH	[3]	R_WS_SC	1'b0	The application writes this bit to flush the IN Token Sequence Learning Queue.
	[2]	R/W	1'b0	Reserved
HSFTRST	[1]	R_WS_SC	1'b0	The application uses this bit to flush the control logic in the AHB Clock domain. Only AHB Clock Domain pipelines are reset. • FIFOs are not flushed with this bit. • All state machines in the AHB clock domain are reset to the Idle state after terminating the transactions on the AHB, following the protocol. • CSR control bits used by the AHB clock domain state machines are cleared. • To clear this interrupt, status mask bits that control the interrupt status and are generated by the AHB clock domain state machine are cleared. • Because interrupt status bits are not cleared, the application can get the status of any core events that occurred after it set this bit. This is a self-clearing bit that the core clears after all necessary logic is reset in the core. This can

				take several clocks, depending on the core's current state.
CSFTRST	[0]	R_WS_SC	1'b0	Resets the hclk and phy_clock domains as follows: • Clears the interrupts and all the CSR registers except the following register bits: - PCGCCTL.RstPdwnModule - PCGCCTL.GateHclk - PCGCCTL.PwrClmp -PCGCCTL.StopPPhyLPwrClkSelclk - GUSBCFG.PhyLPwrClkSel - GUSBCFG.DDRSel - GUSBCFG.PHYSel - GUSBCFG.FSIntf - GUSBCFG.ULPI_UTMI_Sel - GUSBCFG.PHYIf - HCFG.FSLSPclkSel - DCFG.DevSpd - GGPIO • All module state machines (except the AHB Slave Unit) are reset to the IDLE state, and all the transmit FIFOs and the receive FIFO are flushed. • Any transactions on the AHB Master are terminated as soon as possible, after gracefully completing the last data phase of an AHB transfer. Any transactions on the USB are terminated immediately. The application can write to this bit any time it wants to reset the core. This is a self-clearing bit and the core clears this bit after all the necessary logic is reset in the core, which can take several clocks, depending on the current state of the core. Once this bit is cleared software must wait at least 3 PHY clocks before doing any access to the PHY domain (synchronization delay). Software must also must check that bit 31 of this register is 1 (AHB Master is IDLE) before starting any operation. Typically software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain has to be reset for proper operation.

6.1.5.2.4 GINTSTS

Description：（Global Interrupt Status）

0x0014	Global Interrupt Status(reset 0x0000_0020)												GINTSTS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	WKUPINT	SESSREQINT	Reserved	CONIDSTSCHNG	Reserved				RESETDET	FETSUSP	INCOMPISOOUT	INCOMPISOIN	OEPINT	IEPINT	EPMIS	Reserved
Type	R_SS_WC	R_SS_WC		R_SS_WC					RW	R_SS_WC	R_SS_WC	R_SS_WC	RO	RO	RO	
Reset	0	0	0	0	4'b0				0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	EOPF	ISOOUTDROP	ENUMDONE	USBRST	USBSUSP	ERLYSUSP	Reserved		GOUTNAKEFF	GINNAKEFF	NPTXFEMP	RXFLV	SOF	OTGINT	MODEMIS	CURMOD
Type	R_SS_WC	R_SS_WC	R_SS_WC	R_SS_WC	R_SS_WC	R_SS_WC			RO	RO	RO	RO	R_SS_WC	R_SS_WC	R_SS_WC	RO
Reset	0	0	0	0	0	0	2'b0		0	0	1	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
WKUPINT	[31]	R_SS_WC	1'b0	The Wakeup bit is same for both L1 and normal wakeup, except that Partial Power-Down cannot be used in L1. In L1, this interrupt is asserted when a host-initiated resume or a device-initiated remote wakeup is detected on the USB in Host and Device modes. In Device mode, this interrupt is asserted when a resume is detected on the USB for normal suspend.
SESSREQINT	[30]	R_SS_WC	1'b0	device. In Device mode, this interrupt is asserted when theutmiotg_bvalid signal goes high.
	[29]		1'b0	Reserved
CONIDSTSCHNG	[28]	R_SS_WC	1'b0	The core sets this bit when there is a change in connector ID status.
	[27:24]	RO	4'h3	Reserved
RESETDET	[23]	R/W	1'b0	The core asserts this interrupt in Device mode when it detects a reset on the USB in Partial Power-Down mode when the device is in Suspend. This interrupt is not asserted in Host mode.
FETSUSP	[22]	R_SS_WC	1'b0	This interrupt is valid only in DMA mode. This interrupt indicates that the core has stopped fetching data for IN endpoints due to the unavailability of TxFIFO space or Request Queue space. This interrupt is used by the application for an endpoint mismatch algorithm. For example, after detecting an endpoint mismatch, the application:

				• Sets a global non-periodic IN NAK handshake • Disables In endpoints • Flushes the FIFO • Determines the token sequence from the IN Token Sequence Learning Queue • Re-enables the endpoints • Clears the global non-periodic IN NAK handshake If the global non-periodic IN NAK is cleared, the core has not yet fetched data for the IN endpoint, and the IN token is received: the core generates an “IN token received when FIFO empty” interrupt. The OTG then sends the host a NAK response. To avoid this scenario, the application can check the GINTSTS.FetSusp interrupt, which ensures that the FIFO is full before clearing a global NAK handshake. Alternatively, the application can mask the “IN token received when FIFO empty” interrupt when clearing a global IN NAK handshake.
INCOMPISOOUT	[21]	R_SS_WC	1’b0	The Device mode, the core sets this interrupt to indicate that there is at least one isochronous OUT endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register.
INCOMPISOIN	[20]	R_SS_WC	1’b0	The core sets this interrupt to indicate that there is at least one isochronous IN endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register.
OEPINT	[19]	RO	1’b0	The core sets this bit to indicate that an interrupt is pending on one of the OUT endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the OUT endpoint on which the interrupt occurred, and then read the corresponding Device OUT Endpoint-n Interrupt (DOEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DOEPINTn register to clear this bit.
IEPINT	[18]	RO	1’b0	The core sets this bit to indicate that an interrupt is pending on one of the IN endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the IN endpoint on which the interrupt occurred, and then read the corresponding Device IN Endpoint-n Interrupt (DIEPINTn) register to determine the exact

				cause of the interrupt. The application must clear the appropriate status bit in the corresponding DIEPINTn register to clear this bit.
	[17:16]	RO	2'b0	Reserved
EOPF	[15]	R_SS_WC	1'b0	Indicates that the period specified in the Periodic Frame Interval field of the Device Configuration register (DCFG.PerFrInt) has been reached in the current microframe.
ISOOUTDROP	[14]	R_SS_WC	1'b0	The core sets this bit when it fails to write an isochronous OUT packet into the RxFIFO because the RxFIFO does not have enough space to accommodate a maximum packet size packet for the isochronous OUT endpoint.
ENUMDONE	[13]	R_SS_WC	1'b0	The core sets this bit to indicate that speed enumeration is complete. The application must read the Device Status (DSTS) register to obtain the enumerated speed.
USBRST	[12]	R_SS_WC	1'b0	The core sets this bit to indicate that a reset is detected on the USB.
USBSUSP	[11]	R_SS_WC	1'b0	The core sets this bit to indicate that a suspend was detected on the USB. The core enters the Suspended state when there is no activity on the phy_line_state_i signal for an extended period of time.
ERLYSUSP	[10]	R_SS_WC	1'b0	The core sets this bit to indicate that an Idle state has been detected on the USB for 3 ms
	[9:8]			
GOUTNAKEFF	[7]	RO	1'b0	Indicates that the Set Global OUT NAK bit in the Device Control register (DCTL.SGOUTNak), set by the application, has taken effect in the core. This bit can be cleared by writing the Clear Global OUT NAK bit in the Device Control register (DCTL.CGOUTNak).
GINNAKEFF	[6]	RO	1'b0	Indicates that the Set Global Non-periodic IN NAK bit in the Device Control register (DCTL.SGNPInNak), set by the application, has taken effect in the core. That is, the core has sampled the Global IN NAK bit set by the application. This bit can be cleared by clearing the Clear Global Non-periodic IN NAK bit in the Device Control register (DCTL.CGNPInNak). This interrupt does not necessarily mean that a NAK handshake is sent out on the USB. The STALL bit takes precedence over the NAK bit.
NPTXFEMP	[5]	RO	1'b1	This interrupt is valid only when OTG_EN_DED_TX_FIFO = 0. This interrupt is asserted when the Non-periodic TxFIFO is either half or completely empty, and there is space for at least one entry to be written to the Non-periodic Transmit Request Queue. The half or completely empty status is determined by the Non-periodic TxFIFO Empty Level bit in

				the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl).
RXFLVL	[4]	RO	1'b0	Indicates that there is at least one packet pending to be read from the RxFIFO.
SOF	[3]	R_SS_WC	2'b0	In Device mode, in the core sets this bit to indicate that an SOF token has been received on the USB. The application can read the Device Status register to get the current (micro)frame number. This interrupt is seen only when the core is operating at either HS or FS.
OTGINT	[2]	R_SS_WC	1'b0	The core sets this bit to indicate an OTG protocol event. The application must read the OTG Interrupt Status (GOTGINT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the GOTGINT register to clear this bit.
MODEMIS	[1]	R_SS_WC	1'b0	The core sets this bit when the application is trying to access: • A Host mode register, when the core is operating in Device mode • A Device mode register, when the core is operating in Host mode The register access is completed on the AHB with an OKAY response, but is ignored by the core internally and does not affect the operation of the core.
CURMOD	[0]	RO	1'b1	Indicates the current mode. • 1'b0: Device mode • 1'b1: Host mode

6.1.5.2.5 GINTMSK

Description：（Global Interrupt Mask）

0x0018	Global Interrupt Mask(reset 0x0000_0000)												GINTMSK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	WKUPINTMSK	SESSREQINTMSK	Reserved	Conidstschngmsk	Reserved				RESETDETMSK	FETSUSPMSK	INCOMPISOOUTMSK	INCOMPISOINMSK	OEPINTMSK	IEPINTMSK	EPMISMSK	Reserved
Type	RW	RW		RW					RW	RW	RW	RW	RW	RW	RW	
Reset	0	0	0	0	4'b0				0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	EOPFMSK	ISOOUTDROPMSK	ENUMDONEMSK	USBRSTMSK	USBSUSPMSK	ERLYSUSPMSK	Reserved		GOUTNAKEFFMSK	GINNAKEFFMSK	NPTXFEMPMSK	RXFLVLMSK	SOFMSK	OTGINTMSK	MODEMISMSK	Reserved
Type	RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	2'b0		0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
WKUPINTMSK	[31]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
SESSREQINTMSK	[30]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
DISCONNINTMSK	[29]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
CONIDSTSCHNGMSK	[28]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
LPM_INTMSK	[27]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
PTXFEMPMSK	[26]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
HCHINTMSK	[25]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
PRTINTMSK	[24]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
RESETDETMSK	[23]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
FETSUSPMSK	[22]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
INCOMPISOOUTMSK	[21]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
INCOMPISOINMSK	[20]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt

OEPINTMSK	[19]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
EPINTMSK	[18]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
EPMISMSK	[17]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
	[16]	RO	1'b0	Reserved
EOPFMSK	[15]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
ISOOUTDROPMSK	[14]	R/W		1'b0: Mask Interrupt 1'b1: Unmask Interrupt
ENUMDONEMSK	[13]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
USBRSTMSK	[12]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
USBSUSPMSK	[11]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
ERLYSUSPMSK	[10]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
I2CINTMSK	[9]	R/W	1'b0	Reserved
ULPICKINTMsk	[8]	R/W	1'b0	Reserved
GOUTNAKEFFMSK	[7]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
GINNAKEFFMSK	[6]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
NPTXFEMPMSK	[5]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
RXFLVLMSK	[4]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
SOFMSK	[3]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
OTGINTMSK	[2]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
MODEMISMSK	[1]	R/W	1'b0	1'b0: Mask Interrupt 1'b1: Unmask Interrupt
	[0]			Reserved

6.1.5.2.6 GRXSTSR

Description：（Global Receive Status Register）

0x001C			Global RX Status Register(reset 0x0000_0000)													GRXSTSR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved							FN				PKTSTS				DPID
Type								RO				RO				RO
Reset	7'b0							4'h0				4'h0				2'b0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DPID	BCNT											EPNUM			
Type	RO	RO											RO			
Reset	2'b0	11'b0											3'b0			

Field Name	Bit	Type	Reset Value	Description
FN	[24:21]	RO	4'b0	This is the least significant 4 bits of the (micro)frame number in which the packet is received on the USB. This field is supported only when isochronous OUT endpoints are supported.
PKTSTS	[20:17]	RO	4'b0	Indicates the status of the received packet • 4'b0001: Global OUT NAK (triggers an interrupt) • 4'b0010: OUT data packet received • 4'b0011: OUT transfer completed (triggers an interrupt) • 4'b0100: SETUP transaction completed (triggers an interrupt) • 4'b0110: SETUP data packet received • Others: Reserved
DPID	[16:15]	RO	2'b0	Indicates the Data PID of the received OUT data packet • 2'b00: DATA0 • 2'b10: DATA1 • 2'b01: DATA2 • 2'b11: MDATA
BCNT	[14:4]	RO	11'b0	Indicates the byte count of the received data packet.
EPNUM	[3:0]	RO	4'b0	Indicates the endpoint number to which the current received packet belongs.

6.1.5.2.7 GRXSTSP

Description：（Global Receive Status Pop）

0x001C			Global RX Status Register(reset 0x0000_0000)													GRXSTSR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved							FN				PKTSTS				DPID
Type								RO				RO				RO
Reset	7'b0							4'h0				4'h0				2'b0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DPID	BCNT											EPNUM			
Type	RO	RO											RO			
Reset	2'b0	11'b0											3'b0			

Field Name	Bit	Type	Reset Value	Description
FN	[24:21]	RO	4'b0	This is the least significant 4 bits of the (micro)frame number in which the packet is received on the USB. This field is supported only when isochronous OUT endpoints are supported.
PKTSTS	[20:17]	RO	4'b0	Indicates the status of the received packet • 4'b0001: Global OUT NAK (triggers an interrupt) • 4'b0010: OUT data packet received • 4'b0011: OUT transfer completed (triggers an interrupt) • 4'b0100: SETUP transaction completed (triggers an interrupt) • 4'b0110: SETUP data packet received • Others: Reserved
DPID	[16:15]	RO	2'b0	Indicates the Data PID of the received OUT data packet • 2'b00: DATA0 • 2'b10: DATA1 • 2'b01: DATA2 • 2'b11: MDATA
BCNT	[14:4]	RO	11'b0	Indicates the byte count of the received data packet.
EPNUM	[3:0]	RO	4'b0	Indicates the endpoint number to which the current received packet belongs.

6.1.5.2.8 GRXFSIZ

Description：（Global Receive FIFO Size）

0x0024	Global RX FIFO Size(reset 0x0000_0215)												GRXFSIZ			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type																
Reset	15'b0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RxFIFO Depth															
Type	RW															
Reset	16'd533															

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	0	Reserved
RXFDEP	[15:0]	RO	15'b215	This value is in terms of 32-bit words. • Minimum value is 16 • Maximum value is 32,768 The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth (parameter OTG_RX_DFIFO_DEPTH) during coreConsultant configuration. If Enable Dynamic FIFO Sizing? was selected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. You can write a new value in this field. Programmed values must not exceed the power-on value set in coreConsultant.

6.1.5.2.9 GNPTXFSIZ

Description：（Global Non-Periodic Transmit FIFO Size）

0x0028	Global NON-Periodic TX FIFO Size(reset 0x0100_0100)												GNPTXFSIZ			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	NPTXFDEP															
Type	RW															
Reset	16'h100															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	NPTXFSTADDR															
Type	RW															
Reset	16'd100															

Field Name	Bit	Type	Reset Value	Description
NPTXFDEP	[31:16]	RW	16'h100	INEPTxF0Dep)This field is valid only for Device mode and when OTG_EN_DED_TX_FIFO = 1 This value is in terms of 32-bit words. • Minimum value is 16 • Maximum value is 32,768 This field is determined during coreConsultant configuration by Enable Dynamic FIFO Sizing? (OTG_TX_DINEP_DFIFO_DEPTH_0): • OTG_DFIFO_DYNAMIC = 0—These flops are optimized, and reads return the power-on value. • OTG_DFIFO_DYNAMIC = 1—Programmed values must not exceed the power-on value set in coreConsultant. The power-on reset value of this field is specified during coreConsultant configuration as Largest IN Endpoint FIFO 0 Depth (parameter OTG_TX_DINEP_DFIFO_DEPTH_0).
NPTXFSTADDR	[15:0]	RW	16'h100	For Device mode, this field is valid only when OTG_EN_DED_TX_FIFO = 0 This field contains the memory start address for IN Endpoint Transmit FIFO# 0. OTG_RX_DFIFO_DEPTH This field is determined during coreConsultant configuration by Enable Dynamic FIFO Sizing? (OTG_DFIFO_DYNAMIC): • OTG_DFIFO_DYNAMIC = 0 —These flops are optimized, and reads return the power-on value. • OTG_DFIFO_DYNAMIC = 1—The application can write a new value in this field. Programmed values must not exceed the power-on value set in coreConsultant. The power-on reset value of this register is specified during coreConsultant configuration as the Largest Rx Data FIFO Depth (parameter OTG_RX_DFIFO_DEPTH).

6.1.5.2.10 GNPTXSTS

Description：（Global Non-Periodic Transmit FIFO Status）

0x002C			Global NON-Periodic TX Status										GNPTXSTS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved	NPTXQTOP							NPTXQSPCAVAI							
Type		RO							RO							
Reset	0	7'h0							Configurable							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	NPTXFSPCAVAIL															
Type	RO															
Reset	Configurable															

Field Name	Bit	Type	Reset Value	Description
	[31]	RO	1'b0	Reserved
NPTXQTOP	[30:24]	RO	7'h0	Entry in the Non-periodic Tx Request Queue that is currently being processed by the MAC. • Bits [30:27]: Channel/endpoint number • Bits [26:25]: • 2'b00: IN/OUT token - 2'b01: Zero-length transmit packet (device IN/host OUT) - 2'b10: PING/CSPLIT token - 2'b11: Channel halt command • Bit [24]: Terminate (last entry for selected channel/endpoint)
NPTXQSPCAVAIL	[23:16]	RO	0	Indicates the amount of free space available in the Non-periodic Transmit Request Queue. Device mode has only IN requests. • 8'h0: Non-periodic Transmit Request Queue is full • 8'h1: 1 location available • 8'h2: 2 locations available • n: n locations available (0 ≤n ≤8) • Others: Reserved
NPTXFSPCAVAIL	[15:0]	RO	0	Indicates the amount of free space available in the Non-periodic TxFIFO. Values are in terms of 32-bit words. • 16'h0: Non-periodic TxFIFO is full • 16'h1: 1 word available • 16'h2: 2 words available • 16'hn: n words available (where 0 ≤ n ≤ 32,768) • 16'h8000: 32,768 words available • Others: Reserved

6.1.5.2.11 GSNPSID

Description：（Global Synopsys ID）

0x0040	Global Synopsys ID(reset 0x0000_4F54)												GSNPSID			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SYNOPSYSID															
Type	RO															
Reset	32'h4F54															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SYNOPSYSID															
Type	RO															
Reset	32'h4F54															

Field Name	Bit	Type	Reset Value	Description
SYNOPSYSID	[31:0]	RO	32'h4F54	Release number of the DWC_otg core being used, currently OT2.91a.

6.1.5.2.12 GHWCFG1

Description：（Global Hardware Configuration 1）

0x0044	Global Hardware Configuration 1												GHWCFG1			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	epdir															
Type	RO															
Reset	32'b0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	epdir															
Type	RO															
Reset	32'b0															

Field Name	Bit	Type	Reset Value	Description
EPDIR	[31:0]	RO	0	This 32-bit field uses two bits per endpoint to determine the endpoint direction. Endpoint • Bits [31:30]: Endpoint 15 direction

				• Bits [29:28]: Endpoint 14 direction ... • Bits [3:2]: Endpoint 1 direction • Bits[1:0]: Endpoint 0 direction (always BIDIR) Direction • 2'b00: BIDIR (IN and OUT) endpoint • 2'b01: IN endpoint • 2'b10: OUT endpoint • 2'b11: Reserved

6.1.5.2.13 GHWCFG2

Description：（Global Hardware Configuration 2）

0x0048	Global Hardware Configuration 2														GHWCFG2	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved	TKNQDEPTH					Reserved		NPTXQDEPTH		Reserved	MULTIPROCINTRPT	DYNFIFOSIZING	Reserved		
Type		RO							RO			RO	RO			
Reset	0	5'h8					2'b0		2'b10		0	1'b0	1'b1	3'b0		
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		NUMDEVEPS				FSPHYTYPE		HSPHYTYPE		SINGPNT	OTGARCH		OTGMODE		
Type			RO				RO		RO		RO	RO		RO		
Reset	2'b0		4'h7				2'b11		2'b11		1'b1	2'b10		3'b100		

Field Name	Bit	Type	Reset Value	Description
	[31]	RO	0	
TKNQDEPTH	[30:26]	RO	5'h8	Range:0-30
	[25:24]	RO	0	
NPTXQDEPTH	[23:22]	RO	2'b10	• 2'b00: 2 • 2'b01: 4 • 2'b10: 8 • Others: Reserved
	[21]	RO	1'b0	Reserved
MULTIPROCINTRPT	[20]	RO	1'b0	• 1'b0: No • 1'b1: Yes
DYNFIFOSIZING	[19]	RO	1'b1	• 1'b0: No • 1'b1: Yes

	[18:14]	RO	5'b0	Reserved
NUMDEVEPS	[13:10]	4'h7	RO	Indicates the number of device endpoints supported by the core in Device mode in addition to control endpoint 0. The range of this field is 1–15.
FSPHYTYPE	[9:8]	2'b11	RO	• 2'b00: Full-speed interface not supported • 2'b01: Dedicated full-speed interface • 2'b10: FS pins shared with UTMI+ pins • 2'b11: FS pins shared with ULPI pins
HSPHYTYPE	[7:6]	2'b11	RO	• 2'b00: High-Speed interface not supported • 2'b01: UTMI+ • 2'b10: ULPI • 2'b11: UTMI+ and ULPI
SINGPNT	[5]	1'b1	RO	• 1'b0: Multi-point application • 1'b1: Single-point application
OTGARCH	[4:3]	2'b10	RO	• 2'b00: Slave-Only • 2'b01: External DMA • 2'b10: Internal DMA • Others: Reserved
OTGMODE	[2:0]	3'b100	RO	• 3'b000: HNP- and SRP-Capable OTG (Host and Device) • 3'b001: SRP-Capable OTG (Host and Device) • 3'b010: Non-HNP and Non-SRP Capable OTG (Host and Device) • 3'b011: SRP-Capable Device • 3'b100: Non-OTG Device • 3'b101: SRP-Capable Host • 3'b110: Non-OTG Host • Others: Reserved

6.1.5.2.14 GHWCFG3

Description：（Global Hardware Configuration 3）

0x004C			Global Hardware Configuration 3										GHWCFG3			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DfifoDepth															
Type	RO															
Reset	16'h1188															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	OTG_ENABLE_LPM	Reserved	OTG_ENABLE_HSIC	OTG_ENABLE_IC_USB	RSTTYPE	OPTFEATURE	VNDCTLSUPT	I2CINTSEL	OTGEN	PKTSIZEWIDTH			XFERSIZEWIDTH			
Type	RO		RO	RO	RO	RO	RO	RO	RO	RO			RO			
Reset	0	0	0	0	0	1'b1	0	0	0	3'b110			4'b1000			

Field Name	Bit	Type	Reset Value	Description
DFIFODEPTH	[31:16]	RO	16'h1188	This value is in terms of 32-bit words. • Minimum value is 32 • Maximum value is 32,768
OTG_ENABLE_LPM	[15]	RO	1'b0	1'b0:No
	[14]	RO	0	
OTG_ENABLE_HSIC	[13]	RO	1'b0	Non-HSIC-capable
OTG_ENABLE_IC_USB	[12]	RO	1'b0	1'b0:No
RSTTYPE	[11]	RO	1'b0	• 1'b0: Asynchronous reset is used in the core • 1'b1: Synchronous reset is used in the core
OPTFEATURE	[10]	RO	1'b1	Indicates whether the User ID register, GPIO interface ports, and SOF toggle and counter ports were removed for gate count optimization by enabling Remove Optional Features? during coreConsultant configuration. • 1'b0: No • 1'b1: Yes
VNDCTLSUPT	[9]	RO	1'b0	• 1'b0: Vendor Control Interface is not available on the core. • 1'b1: Vendor Control Interface is available.
I2CINTSEL	[8]	RO	1'b0	• 1'b0: I2C Interface is not available on the core. • 1'b1: I2C Interface is available on the core.
OTGEN	[7]	RO	1'b0	The application uses this bit to indicate the DWC_otg core's OTG capabilities. • 1'b0: Not OTG capable

				• 1’b1: OTG Capable
PKTSIZEWIDTH	[6:4]	3’b110	RO	Width of Packet Size Counters (PktSizeWidth) • 3’b000: 4 bits • 3’b001: 5 bits • 3’b010: 6 bits • 3’b011: 7 bits • 3’b100: 8 bits • 3’b101: 9 bits • 3’b110: 10 bits • Others: Reserved)
XFERSIZEWIDTH	[3:0]	4’b1000	RO	• 4’b0000: 11 bits • 4’b0001: 12 bits ... • 4’b1000: 19 bits • Others: Reserved

6.1.5.2.15 GHWCFG4

Description：（Global Hardware Configuration 4）

0x0050			Global Hardware Configuration 4										GHWCFG4			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SCATTER/GATHER DMA	SCATTER/GATHER DMA CONFIGURATION	INEPS				DEDFIFOMODE	SESSENDFLTR	BVALIDFLTR	AVALIDFLTR	VBUSVALIDFLTR	IDDGFLTR	NUMCTLEPS			
Type	RO	RO	RO				RO	RO	RO	RO	RO	RO	RO			
Reset	0	0	4’h7				0	0	0	0	0	0	4’b0			
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PHYDATAWIDTH		Reserved								AHBFREQ	ENABLEPWROPT	NUMDEVPERIOEPS			
Type	RO										RO	RO	RO			
Reset	2’b10		0								1’b0	0	4’h1			

Field Name	Bit	Type	Reset Value	Description
SCATTER/GATHER DMA	[31]	RO	1’b0	• 1'b0: Non Dynamic configuration • 1'b1: Dynamic configuration

SCATTER/GATHER DMA CONFIGURATION	[30]	RO	1’b0	• 1'b0: Non-Scatter/Gather DMA configuration • 1'b1: Scatter/Gather DMA configuration
INEPS	[29:26]	RO	1’b0	• 0:1 IN Endpoint • 1:2 IN Endpoints • .... 15:16 IN Endpoints
DEDFIFOMODE	[25]	RO	1’b0	• 1’b0: Dedicated Transmit FIFO Operation not enabled. • 1’b1: Dedicated Transmit FIFO Operation enabled.
SESSENDFLTR	[24]	RO	1’b0	• 1’b0: No filter • 1’b1: Filter
BVALIDFLTR	[23]	RO	1’b0	• 1’b0: No filter • 1’b1: Filter
AVALIDFLTR	[22]	RO	1’b0	• 1’b0: No filter • 1’b1: Filter
VBUSVALIDFLTR	[21]	RO	1’b0	• 1’b0: No filter • 1’b1: Filter
IDDGFLTR	[20]	RO	1’b0	• 1’b0: No filter • 1’b1: Filter
NUMCTLEPS	[19:16]	RO	4’b0	Range:0-15
PHYDATAWIDTH	[15:14]	RO	2’b10	When a ULPI PHY is used, an internal wrapper converts ULPI to UTMI+ . • 2’b00: 8 bits • 2’b01: 16 bits • 2’b10: 8/16 bits, software selectable • Others: Reserved
	[13:6]			Reserved
AHBFREQ	[5]	RO	1’b0	• 1’b0: No • 1’b1: Yes
ENABLEPWROPT	[4]	RO	1’b0	• 1’b0: No • 1’b1: Yes
NUMDEVPERIOEPS	[3:0]	RO	4’h1	Range:0-15

6.1.5.2.16 DPTXFSIZn

Description：（Device Periodic TX FIFO Size n）

0x0104h+(n-1)*04h	IN Endpoint Tx FIFO Size n												DPTXFSIZn			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INEPnTxFDep															
Type	RW															
Reset	16'h100															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INEPnTxFStAddr															
Type	RW															
Reset	16'h215															

Field Name	Bit	Type	Reset Value	Description
INEPnTxFDep	[31:16]	R/W	16'h100	This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 32,768 The power-on reset value of this register is specified as the Largest IN Endpoint FIFO number Depth (parameter OTG_TX_DINEP_DFIFO_DEPTH_n) during coreConsultant configuration (0 < n <= 15). • If Enable Dynamic FIFO Sizing? was deselected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. • If Enable Dynamic FIFO Sizing? was selected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the power-on value set in coreConsultant.
INEPNTXFSTADDR	[15:0]	R/W	16'h215	This field contains the memory start address for IN endpoint Transmit FIFOn (0 < n <= 15). The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth (parameter OTG_RX_DFIFO_DEPTH) during coreConsultant configuration. OTG_RX_DFIFO_DEPTH + SUM 0 to n – 1 (OTG_DINEP_TXFIFO_DEPTH_n) For example start address of IN endpoint FIFO 1 is OTG_RX_DFIFO_DEPTH + OTG_DINEP_TXFIFO_DEPTH_0 The start address of IN endpoint FIFO 2 is OTG_RX_DFIFO_DEPTH + OTG_DINEP_TXFIFO_DEPTH_0 + OTG_DINEP_TXFIFO_DEPTH_1 • If Enable Dynamic FIFO Sizing? was deselected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 0), these flops

				are optimized, and reads return the power-on value. • If Enable Dynamic FIFO Sizing? was selected in coreConsultant (parameter OTG_DFIFO_DYNAMIC = 1), and you have programmed a new value for RxFIFO depth, you can write that value in this field. Programmed values must not exceed the power-on value set in coreConsultant.

6.1.5.2.17 DCFG

Description：（Device Configure）

0x0800h	Device Configure(reset 0x0000_0000)												DCFG			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type																
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			PERFRINT		DEVADDR							Reserved	NZSTSOUTHSHK	DEVSPD	
Type				RW		RW								RW	RW	
Reset	0			2'h0		7'h0							0	0	0	

Field Name	Bit	Type	Reset Value	Description
	[31:13]	RO	0	Reserved
PERFRINT	[12:11]	R/W	2'h0	Indicates the time within a (micro)frame at which the application must be notified using the End Of Periodic Frame Interrupt. This can be used to determine if all the isochronous traffic for that (micro)frame is complete. • 2'b00: 80% of the (micro)frame interval • 2'b01: 85% • 2'b10: 90% • 2'b11: 95%
DEVADDR	[10:4]	R/W	7'h0	The application must program this field after every SetAddress control command.
	[3]	RO	0	Reserved
NZSTSOUTHSHK	[2]	R/W	1'b0	The application can use this field to select the handshake the core sends on receiving a nonzero-length data packet during the

				OUT transaction of a control transfer's Status stage. • 1'b1: Send a STALL handshake on a nonzero-length status OUT transaction and do not send the received OUT packet to the application. • 1'b0: Send the received OUT packet to the application (zero-length or nonzerolength) and send a handshake based on the NAK and STALL bits for the endpoint in the Device Endpoint Control register.
DEVSPD	[1:0]	R/W	2'b0	Indicates the speed at which the application requires the core to enumerate, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the core is connected. See "Device Initialization" on page 295 for details. • 2'b00: High speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) • 2'b01: Full speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) • 2'b10: Reserved • 2'b11: Full speed (USB 1.1 transceiver clock is 48 MHz)

6.1.5.2.18 DCTL

Description：（Device Control）

0x0804h			Device Control													DCTL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															NAKONBBLE
Type																RW
Reset	0															0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	IGNRFRMNUM	GMC		Reserved	(PWRONPRGDONE	CGOUTNAK	SGOUTNAK	CGNPINNAK	Reserved	TSTCT			GOUTNAKSTS	GNPINNAKSTS	SFTDISCON	RMTWKUPSIG
Type	RW	RO			RW	WO	WO	WO		RW			RO	RO	RW	RW
Reset	0	0		0	0	0	0	1'b0	0	3'b0			0	0	0	0

Field Name	Bit	Type	Reset Value	Description

	[31:17]	RO	0	Reserved
NAKONBBLE	[16]	R/W	1'h0	The core sets NAK automatically for the endpoint on which babble is received.
IGNRFRMNUM	[15]	R/W	1'h0	Ignore frame number for isochronous endpoints in case of Scatter/Gather DMA (IgnrFrmNum) Do NOT program IgnrFrmNum bit to 1'b1 when the core is operating in Threshold mode. Note: • When Scatter/Gather DMA mode is disabled, this field is used by the application to enable periodic transfer interrupt. The application can program periodic endpoint transfers for multiple (micro)frames. - 0: Periodic transfer interrupt feature is disabled; the application must program transfers for periodic endpoints every (micro)frame - 1: Periodic transfer interrupt feature is enabled; the application can program transfers for multiple (micro)frames for periodic endpoints. In non-Scatter/Gather DMA mode, the application receives transfer complete interrupt after transfers for multiple (micro)frames are completed.
GMC	[14:13]	RO	0	GMC must be programmed only once after initialization. Applicable only for Scatter/Gather DMA mode. When Scatter/Gather DMA mode is disabled, this field is reserved. and reads 2'b00.
	[12]	R/W	1'b0	Reserved
PWRONPRGDONE	[11]	R/W	1'b0	The application uses this bit to indicate that register programming is completed after a wake-up from Power Down mode.
CGOUTNAK	[10]	WO	1'b0	A write to this field clears the Global OUT NAK.
SGOUTNAK	[9]	WO	1'b0	A write to this field sets the Global OUT NAK. The application uses this bit to send a NAK handshake on all OUT endpoints. The application must set the this bit only after making sure that the Global OUT NAK Effective bit in the Core Interrupt Register (GINTSTS.GOUTNakEff) is cleared.
CGNPINNAK	[8]	WO	1'b0	A write to this field clears the Global Non-periodic IN NAK.
	[7]	RO	1'b0	Reserved
TSTCTL	[6:4]	R/W	3'b0	• 3'b000: Test mode disabled • 3'b001: Test_J mode

				• 3'b010: Test_K mode • 3'b011: Test_SE0_NAK mode • 3'b100: Test_Packet mode • 3'b101: Test_Force_Enable • Others: Reserved
GOUTNAKSTS	[3]	RO	1'b0	• 1'b0: A handshake is sent based on the FIFO Status and the NAK and STALL bit settings. • 1'b1: No data is written to the RxFIFO, irrespective of space availability. Sends a NAK handshake on all packets, except on SETUP transactions. All isochronous OUT packets are dropped.
GNPINNAKSTS	[2]	RO	1'b0	• 1'b0: A handshake is sent out based on the data availability in the transmit FIFO. • 1'b1: A NAK handshake is sent out on all non-periodic IN endpoints, irrespective of the data availability in the transmit FIFO.
SFTDISCON	[1]	R/W	1'b0	The application uses this bit to signal the DWC_otg core to do a soft disconnect. As long as this bit is set, the host does not see that the device is connected, and the device does not receive signals on the USB. The core stays in the disconnected state until the application clears this bit. The minimum duration for which the core must keep this bit set is specified in Table 5.4. • 1'b0: Normal operation. When this bit is cleared after a soft disconnect, the core drives the phy_opmode_o signal on the UTMI+ to 2'b00, which generates a device connect event to the USB host. When the device is reconnected, the USB host restarts device enumeration. • 1'b1: The core drives the phy_opmode_o signal on the UTMI+ to 2'b01, which generates a device disconnect event to the USB host.
RMTWKUPSIG	[0]	R/W	1'b0	When the application sets this bit, the core initiates remote signaling to wake the USB host. The application must set this bit to instruct the core to exit the Suspend state. As specified in the USB 2.0 specification, the application must clear this bit 1–15 ms after setting it.

6.1.5.2.19 DSTS

Description：（Device Status）

0x0808h			Device Status(reset 0x0000_0002)													DSTS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved										SOFFN					
Type											RO					
Reset	0										0					
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SOFFN								Reserved				ERR TICE RR	ENUMSPD		SUS PST S
Type	RO								3'b0				RO	RO		RO
Reset	0								0				0	2'b01		0

~~Field Name~~	Bit	Type	Reset Value	Description
	[31:22]	RO	0	Reserved
SOFFN	[21:8]	RO	14'h0	When the core is operating at high speed, this field contains a microframe number. When the core is operating at full or low speed, this field contains a frame number.
ERRTICERR	[3]	RO	1'h0	The core sets this bit to report any erratic errors (phy_rxvalid_i/phy_rxvldh_i or phy_rxactive_i is asserted for at least 2 ms, due to PHY error) seen on the UTMI+ . Due to erratic errors, the DWC_otg core goes into Suspended state and an interrupt is generated to the application with Early Suspend bit of the Core Interrupt register (GINTSTS.ErlySusp). If the early suspend is asserted due to an erratic error, the application can only perform a soft disconnect recover.
ENUMSPD	[2:1]	RO	0	Indicates the speed at which the DWC_otg core has come up after speed detection through a chirp sequence. 2'b00: High speed (PHY clock is running at 30 or 60 MHz) • 2'b01: Full speed (PHY clock is running at 30 or 60 MHz) • 2'b10: Low speed (PHY clock is running at 48 MHz, internal phy_clk at 6 MHz) • 2'b11: Full speed (PHY clock is running at 48 MHz) Low speed is not supported for devices using a UTMI+ PHY.
SUSPSTS	[0]	RO	1'b0	In Device mode, this bit is set as long as a Suspend condition is detected on the USB. The core enters the Suspended state when

				there is no activity on the phy_line_state_i signal for an extended period of time. The core comes out of the suspend: • When there is any activity on the phy_line_state_i signal • When the application writes to the Remote Wakeup Signaling bit in the Device Control register (DCTL.RmtWkUpSig).

6.1.5.2.20 DIEPMSK

Description：（Device In Endpoint Mask）

0x0810h			Device In Endpoint Mask(reset 0x0000_0000)										DIEPMSK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		NAKMSK	Reserved			BNAININTRMSK	TXFIFOUNDRNMSK	Reserved	INEPNAKEFFMSK	INTKNEPMISMSK	INTKNTXFEMPMSK	TIMEOUTMSK	AHBERRMSK	EPDISBLDMSK	XFERCOMPLMSK
Type			RW				RW	RW		RW	RW	RW	RW	RW	RW	RW
Reset			0	0			0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:14]	RO	23'h0	Reserved
NAKMSK	[13]	R/W	1'h0	1'b0: Mask interrupt 1'b1: Unmask interrupt
	[12:10]	RO	3'h0	
BNAININTRMSK	[9]	R/W	1'b0	1'b0: Mask interrupt 1'b1: Unmask interrupt
TXFIFOUNDRNMSK	[8]	R/W	1'b0	1'b0: Mask interrupt 1'b1: Unmask interrupt
	[7]	1'b0		Reserved
INEPNAKEFFMSK	[6]	R/W	1'b0	1'b0: Mask interrupt 1'b1: Unmask interrupt
INTKNEPMISMSK	[5]	R/W	1'b0	1'b0: Mask interrupt 1'b1: Unmask interrupt
INTKNTXFEMPMSK	[4]	R/W	1'b0	1'b0: Mask interrupt

				1’b1: Unmask interrupt
TIMEOUTMSK	[3]	R/W	1’b0	1’b0: Mask interrupt 1’b1: Unmask interrupt
AHBERRMSK	[2]	R/W	1’b0	1’b0: Mask interrupt 1’b1: Unmask interrupt
EPDISBLDMSK	[1]	R/W	1’b0	1’b0: Mask interrupt 1’b1: Unmask interrupt
XFERCOMPLMSK	[0]	R/W	1’b0	1’b0: Mask interrupt 1’b1: Unmask interrupt

6.1.5.2.21 DOEPMSK

Description：（Device Out Endpoint Mask）

0x0814h			Device Out Endpoint Mask(reset 0x0000_0000)										DOEPMSK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type																
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	NYETMSK	NAKMSK	BBLEERRMSK	Reserved		BNAOUTINTRMSK	OUTPKTERRMSK	Reserved	BACK2BACKSETUP	Reserved	OUTTKNEPDISMSK	SETUPMSK	AHBERRMSK	EPDISBLDMSK	XFERCOMPLMSK
Type		RW	RW	RW			RW	RW		RW		RW	RW	RW	RW	RW
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:15]	RO	17’h0	Reserved
NYETMSK	[14]	R/W	1’b0	1’b0: Mask interrupt 1’b1: Unmask interrupt
NAKMSK	[13]	R/W	1’h0	1’b0: Mask interrupt 1’b1: Unmask interrupt
BBLEERRMSK	[12]	RO	1’b0	1’b0: Mask interrupt 1’b1: Unmask interrupt
	[11:10]	RO	3’h0	Reserved
BNAOUTINTRMSK	[9]	R/W	1’b0	1’b0: Mask interrupt 1’b1: Unmask interrupt
OUTPKTERRMSK	[8]	R/W	1’b0	1’b0: Mask interrupt

				1’b1: Unmask interrupt
	[7]	1’b0		Reserved
BACK2BACKSETUP	[6]	R/W	1’b0	1’b0: Mask interrupt 1’b1: Unmask interrupt
	[5]	R/W	1’b0	Reserved
OUTTKNEPDISMSK	[4]	R/W	1’b0	Applies to control endpoints only. 1’b0: Mask interrupt 1’b1: Unmask interrupt
SETUPMSK	[3]	R/W	1’b0	Applies to control endpoints only. 1’b0: Mask interrupt 1’b1: Unmask interrupt
AHBERRMSK	[2]	R/W	1’b0	1’b0: Mask interrupt 1’b1: Unmask interrupt
EPDISBLDMSK	[1]	R/W	1’b0	1’b0: Mask interrupt 1’b1: Unmask interrupt
XFERCOMPLMSK	[0]	R/W	1’b0	1’b0: Mask interrupt 1’b1: Unmask interrupt

6.1.5.2.22 DAINT

Description：（Device All Interrupt）

0x0818h			Device All Interrupt(reset 0x0000_0000)										DAINT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	OUTEPINT															
Type	RO															
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INEPINT															
Type	RO															
Reset	0															

Field Name	Bit	Type	Reset Value	Description
OUTEPINT	[31:16]	RO	16’h0	One bit per OUT endpoint: Bit 16 for OUT endpoint 0, bit 31 for OUT endpoint 15
INEPINT	[15:0]	RO	16’b0	One bit per IN Endpoint: Bit 0 for IN endpoint 0, bit 15 for endpoint 15

6.1.5.2.23 DAINTMSK

Description：（Device All Interrupt）

0x081Ch			Device All Interrupt Mask(reset 0x0000_0000)										DAINTMSK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	OUTEPMSK															
Type	RW															
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INEPMSK															
Type	RW															
Reset	0															

Field Name	Bit	Type	Reset Value	Description
OUTEPMSK	[31:16]	R/W	16'h0	One per OUT Endpoint: Bit 16 for OUT EP 0, bit 31 for OUT EP 15 1'b0: Mask interrupt 1'b1: Unmask interrupt
INEPMSK	[15:0]	R/W	16'b0	One bit per IN Endpoint: Bit 0 for IN EP 0, bit 15 for IN EP 15 1'b0: Mask interrupt 1'b1: Unmask interrupt

6.1.5.2.24 DIEPEMPMSK

Description：（Device IN Endpoint Empty Mask）

0x0834h			Device In Endpoint Empty Mask										DIEPEMPMSK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type																
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INEPTXFEMPMSK															
Type	RW															
Reset	0															

Field Name	Bit	Type	Reset Value	Description
	[31:16]	R/W	16'h0	reserved
INEPTXFEMPMSK	[15:0]	R/W	16'b0	These bits acts as mask bits for DIEPINTn. TxFEmp interrupt One bit per IN Endpoint: • Bit 0 for IN endpoint 0 ... • Bit 15 for endpoint 15

6.1.5.2.25 DIEPCTL0

Description：（Device IN Endpoint Control 0）

0x0900h			Device In Endpoint Control 0(reset 0x0000_0000)													DIEPCTL0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	EPENA	EPDIS	Reserved		SNAK	CNAK	TXFNUM				STALL	Reserved	EPTYPE		NAKSTS	Reserved
Type	R_WS_SC	R_WS_SC			WO	WO	RW				R_WS_SC		RO		RO	
Reset	0	0	0		0	0	0				0	0	0		0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	USBACTEP	Reserved													MPS	
Type	RO														RW	
Reset	1	0													0	

Field Name	Bit	Type	Reset Value	Description
EPENA	[31]	R_WS_SC	1'h0	• When Scatter/Gather DMA mode is disabled—such as in buffer-pointer based DMA mode—this bit indicates that data is ready to be transmitted on the endpoint. The core clears this bit before setting the following interrupts on this endpoint: • Endpoint Disabled • Transfer Completed
EPDIS	[30]	R_WS_SC	1'b0	The application sets this bit to stop transmitting data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled

				Interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.
	[29:28]	RO	2'b0	Reserved
SNAK	[27]	WO	1'b0	A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint.
CNAK	[26]	WO	1'b0	A write to this bit clears the NAK bit for the endpoint.
TXFNUM	[25:22]	R/W	4'h0	• For Dedicated FIFO operation, this value is set to the FIFO number that is assigned to IN Endpoint 0.
STALL	[21]	R_WS_SC	1'b0	The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority.
	[20]	RO	1'b0	Reserved
EPTYPE	[19:18]	RO	2'b0	Hardcoded to 00 for control.
NAKSTS	[17]	RO	1'b0	Indicates the following: • 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status • 1'b1: The core is transmitting NAK handshakes on this endpoint. When this bit is set, either by the application or core, the core stops transmitting data, even if there is data available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
	[16]	RO	1'b0	Reserved
USBACTEP	[15]	RO	1'b0	This bit is always set to 1, indicating that control endpoint 0 is always active in all configurations and interfaces.
	[14:2]		13'b0	Reserved
MPS	[1:0]	R/W	2'b0	Applies to IN and OUT endpoints. The application must program this field with the maximum packet size for the current logical endpoint. • 2'b00: 64 bytes • 2'b01: 32 bytes • 2'b10: 16 bytes • 2'b11: 8 bytes

6.1.5.2.26 DOEPCTL0

Description：（Device OUT Endpoint Control 0）

0x0B00h			Device Out Endpoint Control 0(reset 0x0000_1000)												DOEPCTL0	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	EPEna	EPDis	Reserved		SNAK	CNAK	TxFNum				Stall	Snp	EPType		NAK Sts	Reserved
Type	R_WS_SC	R_WS_SC			WO	WO	RW				R_WS_SC	RW	RO		RO	
Reset	0	0	0		0	0	0				0	0	0		0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	USB Act EP	Reserved													MPS	
Type	RO														RW	
Reset	1	0													0	

Field Name	Bit	Type	Reset Value	Description
EPENA	[31]	R_WS_SC	1'h0	• When Scatter/Gather DMA mode is disabled—(such as for buffer-pointer based DMA mode)—this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: • SETUP Phase Done • Endpoint Disabled • Transfer Completed Note: In DMA mode, this bit must be set for the core to transfer SETUP data packets into memory.
EPDIS	[30]	R_WS_SC	1'b0	The application cannot disable control OUT endpoint 0.
	[29:28]	RO	2'b0	Reserved
SNAK	[27]	WO	1'b0	A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set bit on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.
CNAK	[26]	WO	1'b0	A write to this bit clears the NAK bit for the endpoint.
	[25:22]	RO	4'h0	0

STALL	[21]	R_WS_SC	1'b0	The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
SNP	[20]	R/W	1'b0	This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.
EPTYPE	[19:18]	RO	2'b0	Hardcoded to 00 for control.
NAKSTS	[17]	RO	1'b0	Indicates the following: • 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. • 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit, the core stops receiving data, even if there is space in the RxFIFO to accommodate the incoming packet. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
	[16]	RO	1'b0	Reserved
USBACTEP	[15]	RO	1'b0	This bit is always set to 1, indicating that a control endpoint 0 is always active in all configurations and interfaces.
	[14:2]		13'b0	Reserved
MPS	[1:0]	R/W	2'b0	The maximum packet size for control OUT endpoint 0 is the same as what is programmed in control IN Endpoint 0. • 2'b00: 64 bytes • 2'b01: 32 bytes • 2'b10: 16 bytes • 2'b11: 8 bytes

6.1.5.2.27 DIEPCTLn/DOEPCTLn

Description：（Device IN Endpoint Control n/ Device OUT Endpoint Control n）

IN EP:0x900h+(n*20h) OUT EP:0xB00h+(n*20h)	Device In Endpoint Control n Device Out Endpoint Control n															DIEPCTLn DOEPCTLn
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	EPENA	EPDIS	SETD1PID	SETD0PID	SNAK	CNAK	TXFNUM				STALL	SNP	EPTYPE		NAKSTS	DPID
Type	R_WS_SC	R_WS_SC	WO	WO	WO	WO	RW				R_WS_SC	RW	RO		RO	
Reset	0	0	0	0	0	0	0				WS_SC 0	0	0		0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	USBACTEP	Reserved				MPS										
Type	RO					RW										
Reset	1	0				0										

Field Name	Bit	Type	Reset Value	Description
EPENA	[31]	R_WS_SC	1'h0	Applies to IN and OUT endpoints. • When Scatter/Gather DMA mode is enabled—such as for buffer-pointer based DMA mode: - For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. - For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. - The core clears this bit before setting any of the following interrupts on this endpoint: • SETUP Phase Done • Endpoint Disabled • Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory.
EPDIS	[30]	R_WS_SC	1'b0	Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for

				this endpoint.
SETD1PID	[29]	WO	1'b0	Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode.
				Set Odd (micro)frame (SetOddFr) Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/Odd (micro)frame (EO_FrNum) field to odd (micro)frame. This field is not applicable for Scatter/Gather DMA mode.
SETD0PID	[28]	WO	1'b0	Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode.
				In non-Scatter/Gather DMA mode: Set Even (micro)frame (SetEvenFr) Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/Odd (micro)frame (EO_FrNum) field to even (micro) frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure.
SNAK	[27]	WO	1'b0	Applies to IN and OUT endpoints. A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for OUT endpoints on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.
CNAK	[26]	WO	1'b0	Applies to IN and OUT endpoints. A write to this bit clears the NAK bit for the endpoint.
TXFNUM	[25:22]	R/W	4'h0	Dedicated FIFO Operation—these bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO

				number. This field is valid only for IN endpoints.
STALL	[21]	R_WS_SC	1'b0	Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core.
				Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
SNP	[20]	R/W	1'b0	Applies to OUT endpoints only. This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.
EPTYPE	[19:18]	RO	2'b0	Applies to IN and OUT endpoints. This is the transfer type supported by this logical endpoint. • 2'b00: Control • 2'b01: Isochronous • 2'b10: Bulk • 2'b11: Interrupt
NAKSTS	[17]	RO	1'b0	Applies to IN and OUT endpoints. Indicates the following: • 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. • 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: • The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. • For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. • For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets

				with an ACK handshake.
DPID	[16]	RO	1'b0	Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. • 1'b0: DATA0 • 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode.
				Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro) frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. • 1'b0: Even (micro)frame • 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure.
USBACTEP	[15]	R_W_SC	1'b0	Applies to IN and OUT endpoints. Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit.
	[14:11]	R/W	4'b0	Reserved
MPS	[10:0]	R/W	2'b0	Applies to IN and OUT endpoints. The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes.

6.1.5.2.28 DIEPINTn/DOEPINTn

Description：（Device IN Endpoint Interrupt n/ Device OUT Endpoint Interrupt n）

IN EP:0x908h+(n*20h) OUT EP:0xB08h+(n*20h)	Device In Endpoint Int n Device Out Endpoint Int n												DIEPINTn DOEPINTn			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type																
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	NYETINTRPT	NAKINTRPT	BBLEERRINTRPT	PACKETDROPPEDSTATUS	Reserved	BNAINTR	TXFIFOUNDRN OUTPKTERR	TXFEMP	INEPNAKEFF BACK2BACKSETUP	INTKNEPMIS	INTKNTXFEMP OUTTKNEPDIS	TIMEOUT SETUP	AHBERR	EPDISBLD	XFERCOMPL
Type		R_SS_WC	R_SS_WC	R_SS_WC	R_SS_WC		RO	R_SS_WC	RO	R_SS_WC	R_SS_WC	R_SS_WC	R_SS_WC	R_SS_WC	R_SS_WC	R_SS_WC
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
EPENA	[31:15]	RO	16'h0	Reserved
NYETINTRPT	[14]	R_SS_WC	1'b0	The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint.
NAKINTRPT	[13]	R_SS_WC	1'b0	The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo.
BBLEERRINTRPT	[12]	R_SS_WC	1'b0	The core generates this interrupt when babble is received for the endpoint.
PKTDRPSTS	[11]	R_SS_WC	1'b0	This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic

				transfer interrupt feature is selected.
	[10:9]	RO	1'b0	Reserved
TXFIFOUNDRN	[8]	R_SS_WC	1'b0	Applies to IN endpoints Only The core generates this interrupt when it detects a transmit FIFO underrun condition for this endpoint. Dependency: This interrupt is valid only when both of the following conditions are true: • Parameter OTG_EN_DED_TX_FIFO==1 • Thresholding is enabled
OUTPKTERR	[8]	R_SS_WC	1'b0	Applies to OUT endpoints Only This interrupt is asserted when the core detects an overflow or a CRC error for non-Isochronous OUT packet. Dependency: This interrupt is valid only when both of the following conditions are true: • Parameter OTG_EN_DED_TX_FIFO==1 • Thresholding is enabled.
TXFEMP	[7]	RO	1'b1	This bit is valid only for IN Endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)).
INEPNAKEFF	[6]	R_SS_WC	1'b0	Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCTLn.CNAK. This interrupt indicates that the core has sampled the NAK bit set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit.
BACK2BACKSETUP	[6]	R/W	1'b0	Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint. For information about handling this interrupt,
INTKNEPMIS	[5]	R_SS_WC	1'b0	Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received.

	[5]	RO	1'b0	Reserved
INTKNTXFEMP	[4]	R_SS_WC	1'b0	Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/nonperiodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received.
OUTTKNEPDIS	[4]	R_SS_WC	1'b0	Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received.
TIMEOUT	[3]	R_SS_WC	1'b0	• In dedicated FIFO mode, applies only to Control IN endpoints. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint.
SETUP	[3]	R_SS_WC	1'b0	Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet.
AHBERR	[2]	R_SS_WC	1'b0	Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.
EPDISBLD	[1]	R_SS_WC	1'b0	Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.
XFERCOMPL	[0]	R_SS_WC	1'b0	Applies to IN and OUT endpoints. • When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.

6.1.5.2.29 DIEPTSIZ0

Description：（Device IN Endpoint Transfer Size 0）

0x0910h			Device In Endpoint Transfer Size 0(reset 0x0000_0000)													DIEPTSIZ0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved											PKTCNT		Reserved		
Type												RW				
Reset	0											0		0		
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved									XFERSIZE						
Type										RW						
Reset	0									0						

Field Name	Bit	Type	Reset Value	Description
	[31:21]	RO	11'h0	Reserved
PKTCNT	[20:19]	R/W	2'b0	Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO.
	[18:7]	RO	12'b0	Reserved
XFERSIZE	[6:0]	R/W	7'b0	Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet from the external memory is written to the TxFIFO.

6.1.5.2.30 DOEPTSIZ0

Description：（Device OUT Endpoint Transfer Size 0）

0x0B10h			Device Out Endpoint Transfer Size 0(reset 0x0000_0000)													DOEPTSIZ0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved	SUPCNT		Reserved									PKTCNT	Reserved		
Type		RW											RW			
Reset	0	0		0									0	0		
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved									XFERSIZE						
Type										RW						
Reset	0									0						

Field Name	Bit	Type	Reset Value	Description
	[31]	RO	11'h0	Reserved
SUPCNT	[30:29]	R/W	2'h0	This field specifies the number of back-to-back SETUP data packets the endpoint can receive. • 2'b01: 1 packet • 2'b10: 2 packets • 2'b11: 3 packets
	[28:20]		9'h0	Reserved
PKTCNT	[19]	R/W	2'b0	This field is decremented to zero after a packet is written into the RxFIFO.
	[18:7]	RO	12'b0	Reserved
XFERSIZE	[6:0]	R/W	7'b0	Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory.

6.1.5.2.31 DIEPTSIZn/DOEPTSIZn

Description：（Device IN/OUT Endpoint Transfer Size n）

IN EP:0x910h+(n*20h) OUT EP:0xB10h+(n*20h)	Device In Endpoint Transfer Size n Device Out Endpoint Transfer Size n(reset 0x0000_0000)	DIEPTSIZn DOEPTSIZn

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved	MC, RXDPID, SUPCNT		PKTCNT										XFERSIZE		
Type	0	RW		RW										RW		
Reset		0		0										0		

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XFERSIZE															
Type	RW															
Reset	0															

Field Name	Bit	Type	Reset Value	Description
	[31]	RO	11'h0	Reserved
MC	[30:29]	R/W	2'h0	Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per microframe on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints. • 2'b01: 1 packet • 2'b10: 2 packets • 2'b11: 3 packets
			RO	For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetch for an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NextEp).
RXDPID			RO	Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. • 2'b00: DATA0 • 2'b01: DATA2 • 2'b10: DATA1 • 2'b11: MDATA
SUPCNT			R/W	Applies to control OUT Endpoints only. This field specifies the number of

				back-to-back SETUP data packets the endpoint can receive. • 2'b01: 1 packet • 2'b10: 2 packets • 2'b11: 3 packets
PKTCNT	[28:19]	R/W	10'h0	Indicates the total number of USB packets that constitute the Transfer Size amount of data for this endpoint. The power-on value is specified for Width of Packet Counters during coreConsultant configuration (parameter OTG_PACKET_COUNT_WIDTH) • IN Endpoints: This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. • OUT Endpoints: This field is decremented every time a packet (maximum size or short packet) is written to the RxFIFO.
XFERSIZE	[18:0]	R/W	19'b0	This field contains the transfer size in bytes for the current endpoint. The power-on value is specified for Width of Transfer Size Counters during coreConsultant configuration (parameter OTG_TRANS_COUNT_WIDTH). The core only interrupts the application after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet.

6.1.5.2.32 DIEPDMAn/DOEPDMAn

Description：（Device IN/OUT Endpoint DMA n）

IN EP:0x914h+(n*20h) OUT EP:0xB14h+(n*20h)	Device In Endpoint DMA n Device Out Endpoint DMA n(reset 0x0000_0000)														DIEPDMAn DOEPDMAn	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DMAADDR															
Type	RW															
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DMAADDR															
Type	RW															
Reset	0															

Field Name	Bit	Type	Reset Value	Description
DMAADDR	[31:0]	R/W	32'h0	Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. • When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field.

6.1.5.2.33 DTXFSTSn

Description：（Device IN/OUT Endpoint DMA n）

0x918h+(n*20h)	Device TX FIFO Status n												DTXFSTSn			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	0															
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INEPTxFSpcAvai															
Type	RO															
Reset	Configurable															

~~Field Name~~	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
INEPTXFSPCAVAIL	[15:0]	RO	Configurable	Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. • 16'h0: Endpoint TxFIFO is full • 16'h1: 1 word available • 16'h2: 2 words available • 16'hn: n words available (where 0 ≤ n ≤ 32,768) • 16'h8000: 32,768 words available • Others: Reserved

6.1.5.2.34 PCGCCTL

Description：（Power and Clock Gating Control ）

0xE00h			Power and Clock Gating Control(reset 0x0000_0000)													PCGCCTL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type																
Reset	0															
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							RESETAFTERSUSP	L1SUSPENDED	PHYSLEEP	ENBL_L1GATING	PHYSUSPENDED	RSTPDWNMODULE	PWRCLMP	GATEHCLK	STOPPCLK
Type								RW	RO	RO	RW	RO	RW	RW	RW	RW
Reset	0							0	0	0	0	0	0	0	0	0

~~Field Name~~	Bit	Type	Reset Value	Description
	[31:9]	RO	23'h0	Reserved
RESETAFTERSUSP	[8]	R/W	1'b0	In partial power-down mode of operation, this bit needs to be set in host mode before clamp is removed if the host needs to issue reset after suspend. If this bit is not set, then the host issues resume after suspend. This bit is not applicable in device mode and non-partial power-down mode
L1 SUSPENDED	[7]	RO	1'b0	This bit indicates that the PHY is in deep sleep when in L1 state.
PHYSLEEP	[6]	RO	1'b0	This bit indicates that the PHY is in the Sleep state.
ENBL_L1GATING	[5]	R/W	1'b0	When this bit is set, core internal clock gating is enabled in Sleep state if the core cannot assert utmi_l1_suspend_n. When this bit is not set, the PHY clock is not gated in Sleep state.
PHYSUSPENDED	[4]	RO	1'b0	This bit indicates that the PHY has been suspended. After the application sets the Stop Pclk bit (Bit 0), this bit is updated when the PHY becomes suspended. Because the UTMI+ PHY suspend is controlled through a port, the UTMI+ PHY is suspended immediately after the Stop Pclk bit is set. The ULPI PHY takes a few clocks to suspend, however, because the suspend information is conveyed to the ULPI PHY

				through the ULPI protocol.
RSTPDWNMODULE	[3]	R/W	1'b0	This bit is valid only in Partial Power-Down mode. The application sets this bit when the power is turned off. The application clears this bit after the power is turned on and the PHY clock is up.
PWRCLMP	[2]	R/W	1'b0	This bit is valid only in Partial Power-Down mode (OTG_EN_PWROPT = 1). The application sets this bit before the power is turned off to clamp the signals between the power-on modules and the power-off modules. The application clears the bit to disable the clamping before the power is turned on.
GATEHCLK	[1]	R/W	1'b0	The application sets this bit to gate hclk to modules other than the AHB Slave and Master and wakeup logic when the USB is suspended or the session is not valid. The application clears this bit when the USB is resumed or a new session starts.
STOPPCLK	[0]	R/W	1'b0	The application sets this bit to stop the PHY clock (phy_clk) when the USB is suspended, the session is not valid, or the device is disconnected. The application clears this bit when the USB is resumed or a new session starts.

6.1.6 Application Notes

6.1.6.1 Data FIFO RAM Allocation

If Dynamic FIFO Sizing is enabled in the core, external RAM must be allocated among different FIFOs in the core before any transactions can start. The application must follow this procedure every time it changes core FIFO RAM allocation. The application must allocate data RAM per FIFO based on the AHB's operating frequency, the PHY Clock frequency, the available AHB bandwidth, and the performance required on the USB. Based on the above mentioned criteria, the application must provide a table as described below with RAM sizes for each FIFO in each mode.

USB core shares a single SPRAM between transmit FIFO(s) and receive FIFO.

In DMA mode--The SPRAM is also used for storing the some register information .

The Device mode Endpoint DMA address registers (DI/OEPDMAn) is stored in the SPRAM. In addition, the registers DIEPDMAn/DOEPDMAn are maintained in RAM.

6.1.6.2 Memory Calculation

Considerations for allocating data RAM for some of the FIFOs in Device mode are listed here:

1. Receive FIFO RAM allocation:

- RAM for SETUP Packets: 4 * n + 6 locations must be Reserved in the receive FIFO to receive up to n SETUP packets on control endpoints, where n is the number of control endpoints the device core supports. The core does not use these locations, which are Reserved for SETUP packets, to write any other data.
- One location for Global OUT NAK
- Status information is written to the FIFO along with each received packet. Therefore, a minimum space of (Largest Packet Size / 4) + 1 must be allotted to receive packets. If a high-bandwidth

endpoint is enabled, or multiple isochronous endpoints are enabled, then at least two (Largest Packet Size / 4) + 1 spaces must be allotted to receive back-to-back packets. Typically, two (Largest Packet Size / 4) + 1 spaces are recommended so that when the previous packet is being transferred to AHB, the USB can receive the subsequent packet. If AHB latency is high, you must allocate enough space to receive multiple packets. This is critical to prevent dropping any isochronous packets.

- Ø Along with each endpoint's last packet, transfer complete status information is also pushed to the FIFO. Typically, one location for each OUT endpoint is recommended.

2. Transmit FIFO RAM allocation:

- Ø The RAM size for the Periodic Transmit FIFO must equal the maximum amount of data that can be transmitted in a single microframe. The core does not use any data RAM allocated over this requirement, and when data RAM allocated is less than this requirement, the core can malfunction.
- Ø The minimum amount of RAM required for the Non-periodic Transmit FIFO is the largest maximum packet size among all supported non-periodic IN endpoints.
- Ø More space allocated in the Transmit Non-periodic FIFO results in better performance on the USB and can hide AHB latencies. Typically, two Largest Packet Sizes' worth of space is recommended, so that when the current packet is under transfer to the USB, the AHB can get the next packet. If the AHB latency is large, then you must allocate enough space to buffer multiple packets.
- Ø It is assumed that i number of periodic FIFOs is implemented in Device mode.

3. Internal Register Storage Space Allocation:

When operating in Internal DMA mode, the core stores the Endpoint DMA address register (DI/OEPDMA) in the SPRAM. One location must be allocated for each endpoint. For example, if an endpoint is bidirectional, then two locations must be allocated. If an endpoint is IN or OUT, then only one location must be allocated.

6.1.6.3 Calculating the Total FIFO Size for USB core

Total Mem Calculation conditions:

- Ø Minimum FIFO depth allocation
- Ø Support for no more than one Isochronous EndPoint in Device mode
- Ø The FIFO must equal at least one MaxPacketSize (MPS).
- Ø Support for high-bandwidth endpoints.

Total Data FIFO RAM Depth = RxFIFO + Non-periodic TxFIFO + device periodic TxFIFOs

Device RxFIFO = (4 * number of control endpoints + 6) + ((largest USB packet used / 4) + 1) + (2 * number of OUT endpoints) + 1

Non-Periodic TxFIFO =(largest non-periodic USB packet used / 4)

Device Periodic Endpoint-Specific TxFIFOs (a separate FIFO is allocated to each endpoint) = (largest periodic USB packet used for an endpoint / 4) * maximum number of periodic data packets per microframe / frame

Our configuration is as following:

Using Dedicated FIFO mode. The MPS is 1023 bytes for a periodic USB packet and is 512 bytes for a non-periodic USB packet. There are three OUT endpoints, six IN endpoints (non-periodic), one control endpoint, and additional one isochronous (periodic) endpoint. The maximum number of periodic data packets per transfer for Endpoint is 2.With these information, The total data FIFO depth is calculated as follows:

Device RxFIFO = (4 * 1 + 6) + ((1024 / 4) + 1) + 2 * 4 + 1 = 276

Device IN Endpoint TxFIFO:

FIFO # 0 = (64/4) = 16(Assuming this is used for EP0)

FIFO # 1~4 = (512/4) = 128

FIFO # 5 = 2* (1024/4) = 512 (Assuming this is used for Isochonous)

Internal Register = 2 * 8 =16

Total Data FIFO RAM Depth = Max(276 + 128 *3+ 512 + 16 +16 = 1204 , 276 + 128*6 +16 + 16 = 1076) = 1204

Note: Because Dynamic FIFO Sizing is enabled, So FIFO RAM should be dynamically configured for different application:

For Isochronous Endpoint application: only 3 endpoint can be used, so FIFO depth configuration should be 276 + 128 *3+ 512

For Normal application: Up to 6 endpoint can be used, so FIFO depth configuration should be 276 + 128*6

Remember, the default value in register is the largest value, so these registers should be reprogrammed every time the core initiates.

6.2 UART and IrDA interface

6.2.1 Overview

UART is an asynchronous communication interface. SC6820 UART module includes a baud rate generator with software-programmable divider ratios for all common baud rates. Two 128-byte-deep FIFO buffers can minimize processor overhead. The module also includes a flexible interrupt with multiple maskable interrupt sources. Two hardware flow control lines are included (one for input, the other for output). This module also has a built-in IrDA controller and can be configured to connect to an IrDA transceiver. When being used as regular UART port, the IrDA controller is bypassed.

SC6820 provides 3 UART ports, UART0 and UART2 are dedicated for ARM, UART1 is controlled by ARM or DSP depending on global register; when this bit is set to “1”, DSP controls UART1, else ARM controls UART1. UART0 ,UART1 and UART2 have 128-byte FIFO depth.

6.2.2 Features

- Full-duplex operation
- Hardware flow control support
- 128-byte-deep FIFOs minimizes processor overhead at high data rates
- Wide selection of UART word lengths, including 5, 6, 7 and 8 bits
- Stop bit number can be 0, 1, 1.5 or 2 bits
- Support odd/even parity
- Auto detect for parity and framing error
- UART loop-back test mode
- Break character detection and generation
- support DMA operation
- Single interrupt line for multiple maskable interrupt source events
- Programmable interrupt trigger levels for FIFOs
- Baud rate generation based upon programmable divisors, operating from a flexible functional clock
- Includes a built-in IrDA controller

6.2.3 Signal Description

UART0, UART1 and UART2 can be easily connected to the UART port of an external IC. UART0 supports hardware flow control.

Table 6-2 Uart singal description

Signal	I/O	Description	Reset
Uart_tx	O	Serial data output. Since the uart_tx is active high, the pin is set to low on reset	1'h1
Uart_rx	I	Serial data in	1'hx
Uart_ctsn	I	Clear to send Active-low modem status signal. This signal is asserted (logic'0') by the DCE device to inform the UART module that transmission may begin. RTS and CTS are commonly used as handshaking signals to moderate the flow of data into the receiving UART device. The value of this signal is indicated by the UART STS0 bit9 after logical inverse. When the input signal CTSN changes value, either from 0 to 1 or from 1 to 0, an interrupt will be generated to the MCU. If hardware flow control is enabled and the signal CTSN is high, the UART immediately stops data transmission on the TXD output pin after it completes the current data byte transmission. Reading bit 9 of the UART status register checks the condition of uart_cts (inverse).	1'hx
Uart_rtsn	O	Request to send When active (low), the module is ready to receive data. This assertion might mean enabling the transmit circuits of DTE device, or setting up the channel direction in half-duplex applications. When hardware flow control is not set, programming the UART CTL0 bit 6 directly controls the output of RTSN. This pin is the inverse of UART CTL0 bit 6. If receive hardware flow control is set by writing "1" to UART CTL1 bit 7, RTSN will be controlled by the RX FIFO level and Receive_Hardware_Flow_Control threshold. The threshold can be configured by writing UART CTL1[5:0].In this case, RTSN remains high as long as the number of data in the RX FIFO is greater than the configured threshold value.	1

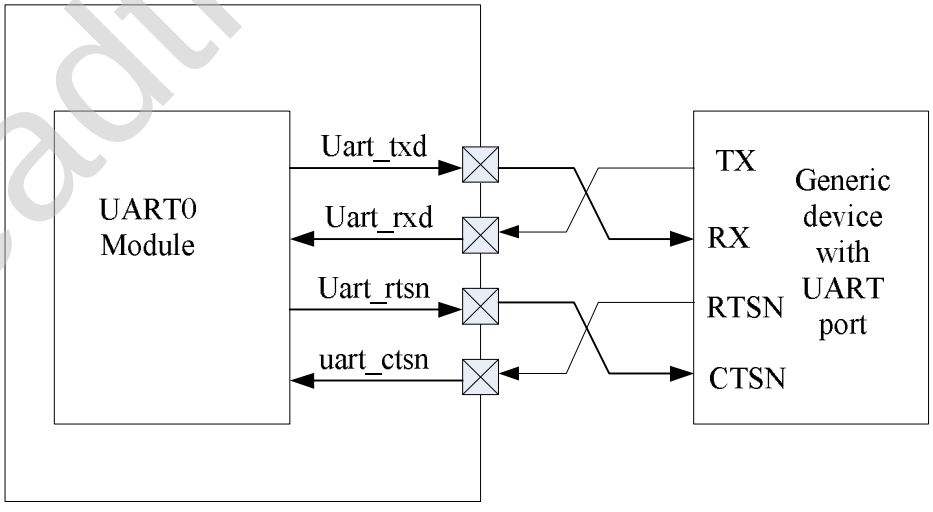


Figure 6-3 UART0 with flow control application

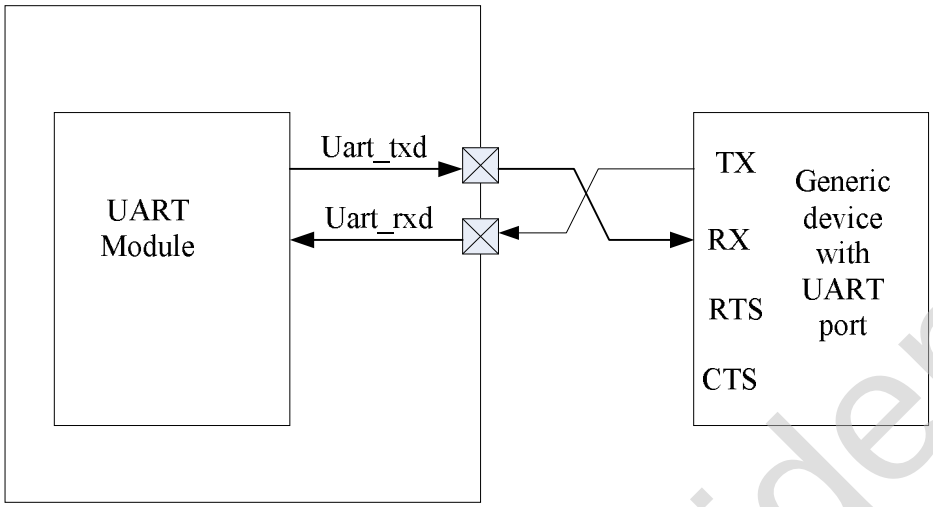


Figure 6-4 UART1/UART2 without flow control application

6.2.4 Function Description

The UART and IRDA baud rate generator is based on the clk_uart, the divisor coefficient is controlled by register UART_CKD0. IRDA part clock period is the 1/16 of the UART part since the required timing of IRDA is 3/16 or 4/16 of bit width. The serial data rate can be changed by modify the clk_uart or the UART divisor coefficient.

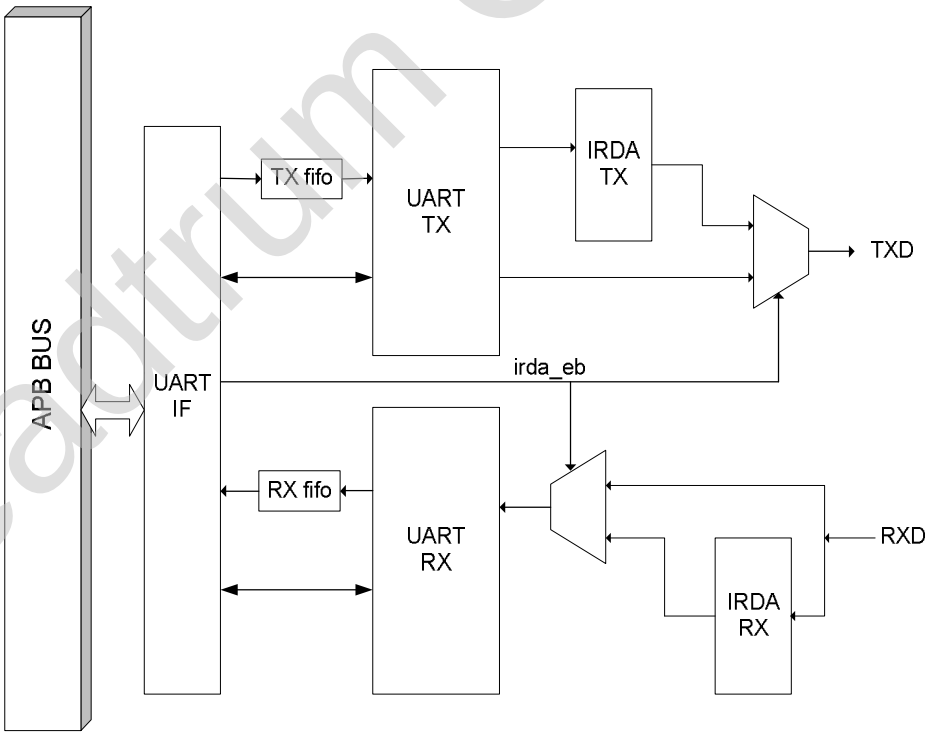


Figure 6-5 Diagram of UART

6.2.4.1 UART Mode Description

UARTs in SC6820 share the same design and each has an independent baud rate generator, which is used as a clock reference for data transmit and recovery. Each of them also has a 128-byte-deep RX FIFO and a 128-byte-deep TX FIFO to decrease processor interrupt load during the data receiving/transmitting.

6.2.4.1.1 FIFO Management

FIFOs are accessed by reading/writing UART_RXD/UART_TXD register. The number of data in TX/RX FIFO can be observed by reading UART_STS1 [6:0]/UART_STS1 [14:8]. Rx_fifo_full and Tx_fifo_empty status can be obtained by reading UART_STS0 [1:0]. UART_CTL2 register controls the FIFO trigger level, which enables the DMA request and interrupt generation.

TX FIFO size is 128 bytes. It uses a FIFO pointer to monitor the number of data in the TX FIFO that has not yet been transmitted. The MCU can read the UART STS1 [14:8] to access the pointer. The UART also provides a TXF empty interrupt threshold that can be configured by writing UART CTL2 [14:8].

RX FIFO size is 128 bytes. It uses a pointer to monitor the number of data in the RX FIFO that have not yet been read by the MCU. The MCU can access the pointer by reading the UART STS1 [6:0]. The UART also provides a RX FIFO full interrupt threshold that can be configured by writing to UART CTL2 [6:0]. In FIFO interrupt mode with flow control, the programmer must also ensure that the Receive_Hardware_Flow_Control_Threshold (UART_CTL1 [6:0]) value is greater than or equal to the Receive_Int_WaterMark (UART_CTL2 [6:0]). Otherwise, FIFO operation stalls.

In FIFO interrupt mode, the processor is informed of the status of the receiver and transmitter by an interrupt signal. The rx_fifo_full interrupt is set when the number of RX FIFO data bytes is larger than the RX interrupt watermark value. It is auto cleared when the condition disappears. The tx_fifo_empty interrupt is set when the number of TX FIFO data bytes is less than the TX interrupt watermark value. It is auto cleared when the condition disappears. The two interrupt sources can be masked by writing “0” to UART_IEN register bit 0 and bit 1.The interrupt signal instructs the local hosts to write data to TX FIFO or read data from RX FIFO.

Note that in the cases of the UART flow control being enabled along with the interrupt capabilities, the user must ensure that the UART flow control FIFO threshold is greater than or equal to the receive FIFO watermark.

The TX and RX FIFO may be accessed by DMA. Writing to control register UART_CTL1 bit 15 will enable DMA mode. In receive mode, a DMA request is generated as soon as the receive FIFO reached its threshold level defined in UART_CTL2 [6:0]. This request is deserted when the number of bytes is less than the threshold level. In transmit mode, a DMA request is automatically asserted when the transmit FIFO is almost empty.

In this mode, when RX FIFO is almost full (the number of RX FIFO data bytes is larger than the RX interrupt watermark value), it will send the receive request to DMA controller, and when TX FIFO is almost empty, it will send the transmit request to DMA controller.

6.2.4.1.2 Hardware Flow Control

SC6820 UART supports both software flow control and hardware flow control. When UART_CTL1 register bit 7 is set to “0”, software will control the signal uart_rtsn by writing UART_CTL0 register bit 6; if ”1”, the signal uart_rtsn will be controlled by hardware itself, called auto-RTS.

Hardware flow control is composed of auto-CTS and auto-RTS. Auto-CTS and auto-RTS can be enabled/disabled independently by programming UART_CTL1 [8:7].

Auto-RTS data flow control originates in the receiver block. The receiver FIFO trigger levels used in auto-RTS are stored in the UART_CTL1 [6:0]. RTS is active if the RX FIFO level is below the HALT trigger level. When the receiver FIFO HALT trigger level is reached, uart_rtsn is deserted. The sending device (external UART device) may send an additional byte after the trigger level is reached because it may not recognize the desertion of RTSn until it has begun sending the additional byte. The assertion requests the sending device to resume transmission. In this case, uart_rtsn is an active-low signal.

With auto-CTS, uart_ctsn must be active before the module can transmit data. The transmitter circuitry checks uart_ctsn before sending the next data byte. When uart_ctsn is active, the transmitter sends the next byte. The auto-CTS function reduces interrupts to the host system. When auto-CTS flow control is enabled, the CTS state changes need not trigger host interrupts because the device automatically controls its own transmitter. Without auto-CTS, the transmitter sends any data present in the transmit FIFO and a receiver overrun error can result. In this case, uart_ctsn is an active-low signal.

6.2.4.1.3 Interrupt sources

The UART also provides a TXF empty interrupt threshold that can be configured by writing UART CTL2 [14:8]. A tx_fifo_empty interrupt will be generated when the number of TX FIFO data bytes is less than the TX interrupt watermark value. It is auto cleared when the condition disappears.

UART also provides a RX FIFO full interrupt threshold that can be configured by writing to UART CTL2 [6:0]. An rx_fifo_full interrupt will be generated when the number of RX FIFO data bytes is larger than the RX interrupt watermark value. The interrupt will be auto cleared when the condition disappears.

An rx_tout interrupt will be generated if the UART has not received data from the input line in a period of time. This period depends on the baudrate and the value of CTL1 [13:9]. If the value of CTL1 [13:9] is ‘0’,the interrupt will never be generated. The interrupt can be cleared by writing “1” to UART_ICLR bit 13.

When having received data, UART generate parity error/framing error if error condition occurs. Also, when having received FIFO overrun, an error interrupt will be generated. Writing to corresponding interrupt clear bit will clear these interrupts.

All interrupt sources in SC6820 UART can be disabled and masked by writing to corresponding registers.

When TX FIFO is empty and TX is idle, setting send break bit forces the TX data output to low.

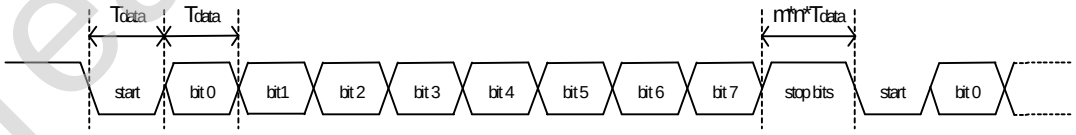


Figure 6-6 UART timing parameter

6.2.4.2 IRDA Mode Description

The IrDA can be used to communicate with other IrDA compatible device. IrDA mode is selected by writing “1” to UART CTL0 [15]. The default value of this bit is “0”.

IrDA mode is achieved by adding IrDA transmit block and IrDA receive block into UART module. The IrDA transmit block changes the UART transmit serial bits to the IrDA timing, and then sends to TXD port. On the other side, the receive module

detects the IrDA timing from the RXD port and changes back to UART bit stream to let the UART receive block to finish the data receiving.

Figure below shows the transmit IrDA timing. The polarity could be changed by UART CTL0 bit 9, and the pulse of a bit may be 3 or 4 high cycle controlled by the UART CTL0 bit 13. In the no polarity invert working mode, when sending “1”, the output remains “0”. And when sending “0”, output follows the IrDA timing as demonstrated in the figure. On the receive data path, the polarity could be change by UART_CTL0 bit 10. The transmission and receive operation could be controlled by the UART CTL0 bit 11 and bit 12.

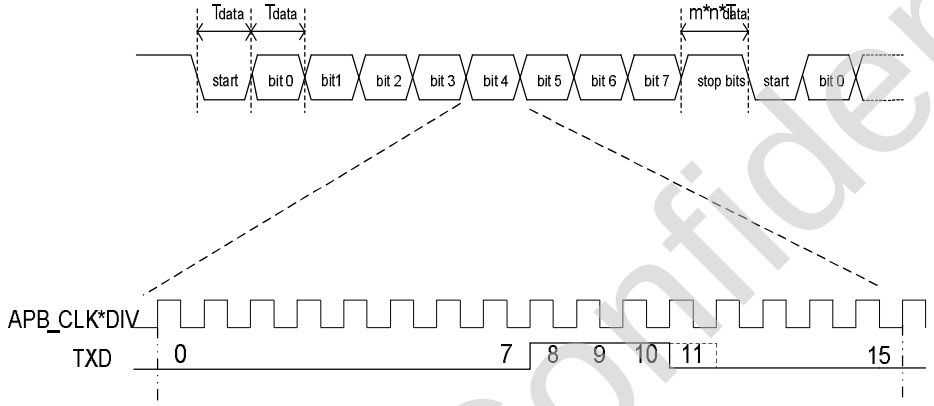


Figure 6-7 IrDA transmit timing

6.2.5 Control Registers

6.2.5.1 Memory map

ARM base address: 0x8300_0000 (UART0)

0x8400_0000 (UART1)

0x8e00_0000 (UART2)

Offset Address / Name	Description
0x0000 UART_TXD	Write data to this address initiates a character transmission through TX FIFO
0x0004 UART_RXD	Read from this address retrieve data from RX FIFO
0x0008 UART_STS0	IIS internal status
0x000C UART_STS1	The data number in TXF and RXF
0x0010 UART_IEN	UART interrupt enable register
0x0014 UART_ICLR	UART interrupt clear register
0x0018 UART_CTRL0	UART control register
0x001C UART_CTRL1	UART control register
0x0020 UART_CTRL2	UART control register
0x0024 UART_CKD0	Divisor is (n+1)*2

Offset Address	Name	Description
0x002C	UART_STS2	UART interrupt mask status
0x0030	UART_DSPWAIT	Control register

6.2.5.2 Register Descriptions

6.2.5.2.1 UART_TXD

Description：Write data to this address initiates a character transmission through TX FIFO.

0x0000			UART TX register(0x0000_0000)													UART_TXD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								UART_TXD							
Type	RO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
UART_TXD	[7:0]	WO	8'h0	Write data to this address initiates a character transmission through TX FIFO

6.2.5.2.2 UART_RXD

Description： Write data to this address initiates a character transmission through TX FIFO.

0x0004			UART RX register(0x0000_0000)													UART_RXD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								UART_RXD							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
UART_TXD	[7:0]	RO	8'h0	FIFO operation register Reading this register retrieves the next data byte from the Rx FIFO.

6.2.5.2.3 UART_STS0

Description： UART status register

0x0008	Register description (0x0000_1802)												UART_STS0			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TRANS_OVER	RXF_REALFULL	TIME_OUT_RAW_STS	TXD	RXD	RTS	CTS	DSR	BRK_DTCT_RAW_STS	CTS_CHG_RAW_STS	DSR_CHG_RAW_STS	RXF_OVERRUN_RAW_STS	FRAME_ERR_RAW_STS	PARITY_ERR_RAW_STS	TXF_EMPTY_RAW_STS	RXF_FULL_RAW_STS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0

Field Name	Bit	R/W	Reset Value	Description
TRANS_OVER	[15]	RO	1'h0	Data transfer is really over
RXF_REALFULL	[14]	RO	1'h0	RX FIFO is real full(not relates to register RXF_FULL_THLD)
TIME_OUT_RAW_STS	[13]	RO	1'h0	RAW timeout interrupt , this bit is set when receive time is out.
TXD	[12]	RO	1'h1	Transmit data
RXD	[11]	RO	1'h1	Receive data
RTS	[10]	RO	1'h0	Request to send
CTS	[9]	RO	1'h0	Clear to send
DSR	[8]	RO	1'h0	Data set ready(no used)
BRK_DTCT_RAW_STS	[7]	RO	1'h0	Raw break detect interrupt
CTS_CHG_RAW_STS	[6]	RO	1'h0	Raw CTS change interrupt
DSR_CHG_RAW_STS	[5]	RO	1'h0	Raw DSR change interrupt
RXF_OVERRUN_RAW_STS	[4]	RO	1'h0	Raw RX FIFO overrun interrupt

FRAME_ERR_RAW_STS	[3]	RO	1'h0	Raw frame error interrupt
PARITY_ERR_RAW_STS	[2]	RO	1'h0	Raw parity error interrupt
TXF_EMPTY_RAW_STS	[1]	RO	1'h1	Raw TX FIFO empty interrupt
RXF_FULL_RAW_STS	[0]	RO	1'h0	Raw RX FIFO full interrupt

6.2.5.2.4 UART_STS1

Description： data number in the TXF and RXF

0x000C			Register description (0x0000_0000)												UART_STS1	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	TXF_CNT							Reserved	RXF_CNT						
Type	RO	RO							RO	RO						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_CNT	[14:8]	RO	7'h0	The number reserved in TX FIFO. The register will increase when writing data to the TX FIFO, while decrease when reading data from TX FIFO
Reserved	[7]	RO	1'h0	
RXF_CNT	[6:0]	RO	7'h0	The number reserved in RX FIFO. The register will increase when writing data to the RX FIFO, while decrease when reading data from RX FIFO

6.2.5.2.5 UART_IEN

Description：UART interrupt enable register

0x0010			Interrupt enable (0x0000_0000)													UART_IEN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		TIME_OUT_INT_EN	Reserved					BRK_DTCT_INT_EN	CTS_CHG_INT_EN	DSR_CHG_INT_EN	RXF_OVERRUN_INT_EN	FRAME_ERR_INT_EN	PARITY_ERR_INT_EN	TXF_EMPTY_INT_EN	RXF_FULL_INT_EN
Type	RO		R/W	RO					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TIME_OUT_INT_EN	[13]	R/W	1'h0	Time out interrupt enable
Reserved	[12:8]	RO	5'h0	
BRK_DTCT_INT_EN	[7]	R/W	1'h0	Break detect interrupt enable
CTS_CHG_INT_EN	[6]	R/W	1'h0	CTS change interrupt enable
DSR_CHG_INT_EN	[5]	R/W	1'h0	DSR change interrupt enable
RXF_OVERRUN_INT_EN	[4]	R/W	1'h0	RX FIFO overrun interrupt enable
FRAME_ERR_INT_EN	[3]	R/W	1'h0	Frame error interrupt enable
PARITY_ERR_INT_EN	[2]	R/W	1'h0	Parity error interrupt enable
TXF_EMPTY_INT_EN	[1]	R/W	1'h0	TX FIFO empty interrupt enable
RXF_FULL_INT_EN	[0]	R/W	1'h0	RX FIFO full interrupt enable

6.2.5.2.6 UART_ICLR

Description：UART interrupt clear register

0x0014			Interrupt clear (0x0000_0000)													UART_ICLR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		TIME_OUT_INT_CLR	Reserved					BRK_DTCT_INT_CLR	CTS_CHG_INT_CLR	DSR_CHG_INT_CLR	RXF_OVERRUN_INT_CLR	FRAME_ERR_INT_CLR	PARITY_ERR_INT_CLR	Reserved	
Type	RO		WO	RO					WO	WO	WO	WO	WO	WO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TIME_OUT_INT_CLR	[13]	WO	1'h0	Write "1" Clear time out interrupt
Reserved	[12:8]	RO	5'h0	
BRK_DTCT_INT_CLR	[7]	WO	1'h0	Write "1" Clear break_detect interrupt
CTS_CHG_INT_CLR	[6]	WO	1'h0	Write "1" Clear cts_change interrupt
DSR_CHG_INT_CLR	[5]	WO	1'h0	Write "1" Clear dsr_change interrupt
RXF_OVERRUN_INT_CLR	[4]	WO	1'h0	Write "1" Clear rxf_overrun interrupt
FRAME_ERR_INT_CLR	[3]	WO	1'h0	Write "1" Clear frame_error interrupt
PARITY_ERR_INT_CLR	[2]	WO	1'h0	Write "1" Clear parity_error interrupt
Reserved	[1:0]	RO	2'h0	

6.2.5.2.7 UART_CTRL0

Description：UART control register

0x0018			Control register (0x0000_0000)													UART_CTRL0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MODE_SEL	Reserved	IR_WCTL	IR_DPLX	IR_TX_EN	IR_RX_IV	IR_TX_IV	DTR_REG	SEND_BRK_EN	RTS_REG	STOP_BIT_NUM		BYTE_LEN		PARITY_EN	ODD_PARITY
Type	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W		R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Field Name	Bit	R/W	Reset Value	Description
MODE_SEL	[15]	R/W	1'h0	"0" : UART "1" : IrDA
Reserved	[14]	RO	1'h0	
IR_WCTL	[13]	R/W	1'h0	set "1", increase pulse width for one clock.
IR_DPLX	[12]	R/W	1'h0	IRDA TX/RX enable
IR_TX_EN	[11]	R/W	1'h0	IRDA TX enable
IR_RX_IV	[10]	R/W	1'h0	IRDA RX polarity inverse
IR_TX_IV	[9]	R/W	1'h0	IRDA TX polarity inverse
DTR_REG	[8]	R/W	1'h0	This bit controls the dtrn output
SEND_BRK_EN	[7]	R/W	1'h0	When TX FIFO is empty and TX is idle, setting this bit forces the TX data output low. Need to be cleared by MCU.
RTS_REG	[6]	R/W	1'h0	When receive hardware flow control is not set, this bit controls the output of RTSN. When RCV_HW_FLOW_EN is set, the output of RTSN is controlled by the register RCV_HW_FLOW_THLD .
STOP_BIT_NUM	[5:4]	R/W	2'h3	0: unused, 1: 1stop bit, 2: 1.5 stop bits, 3: 2 stop bits.
BYTE_LEN	[3:2]	R/W	2'h3	data byte length. 0: 5 bits, 1: 6 bits, 2: 7 bits, 3: 8 bits.
PARITY_EN	[1]	R/W	1'h0	0: parity disabled 1: parity enabled
ODD_PARITY	[0]	R/W	1'h0	0: even parity 1: odd parity

6.2.5.2.8 UART_CTRL1

Description：UART control register

0x001C			Control register (0x0000_0000)													UART_CTRL1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DMA_EN	LOOP_BACK	RX_TOUT_THLD					TX_HW_FLOW_EN	RCV_HW_FLOW_EN	Reserved	RCV_HW_FLOW_THLD					
Type	R/W	R/W	R/W					R/W	R/W	RO	R/W					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
DMA_EN	[15]	R/W	1'h0	"1" enable DMA access UART FIFOs
LOOP_BACK	[14]	R/W	1'h0	Self test mode, TX input to RX
RX_TOUT_THLD	[13:9]	R/W	5'h0	Receive timeout threshold
TX_HW_FLOW_EN	[8]	R/W	1'h0	Transmit_Hardware_Flow_Control_Enable "1" enable transmit hardware flow control "0" disable
RCV_HW_FLOW_EN	[7]	R/W	1'h0	Receive_Hardware_Flow_Control_Enable "1" enable receive hardware flow control "0" disable
Reserved	[6]	RO		
RCV_HW_FLOW_THLD	[5:0]	R/W	6'h0	Receive_Hardware_Flow_Control_Threshold When RCV_HW_FLOW_EN is enabled, if the number of unread bytes in the RX FIFO is greater than the receive hardware flow control threshold value, the RTSN is set to high to stop the remote TX.

6.2.5.2.9 UART_CTRL2

Description：UART TX FIFO empty and RX FIFO full watermark register

0x0020			Control register (0x0000_0008)													UART_CTRL2
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	TXF_EMPTY_THLD							Reserved	RXF_FULL_THLD						
Type	RO	R/W							RO	R/W						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_EMPTY_THLD	[14:8]	R/W	5'h0	TX FIFO data empty threshold
Reserved	[7]	RO	1'h0	
RXF_FULL_THLD	[6:0]	R/W	5'h8	RX FIFO data full threshold

6.2.5.2.10 UART_CKD0

Description：This register is used to configure baud rate

0x0024			Divisor register (0x0000_054A)													SCFG0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	UART_CKD0															
Type	R/W															
Reset	0	0	0	0	0	1	0	1	0	1	0	0	1	0	1	0

Field Name	Bit	R/W	Reset Value	Description
UART_CKD0	[15:0]	R/W	16'h54A	Clock divisor bit 0 to 15

6.2.5.2.11 UART_STS2

Description：UART interrupt mask status

0x002C			INT mask status (0x0000_0000)										UART_STS2			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		TIME_OUT_MASK_STS	Reserved					BRK_DTCT_MASK_STS	CTS_CHG_MASK_STS	DSR_CHG_MASK_STS	RXF_OVERRUN_MASK_STS	FRAME_ERR_MASK_STS	PARITY_ERR_MASK_STS	TXF_EMPTY_MASK_STS	RXF_FULL_MASK_STS
Type	RO		RO	RO					RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TIME_OUT_MASK_STS	[13]	RO	1'h0	Time out interrupt mask status
Reserved	[12:8]	RO	5'h0	
BRK_DTCT_MASK_STS	[7]	RO	1'h0	Break detect interrupt mask status
CTS_CHG_MASK_STS	[6]	RO	1'h0	CTS change interrupt mask status
DSR_CHG_MASK_STS	[5]	RO	1'h0	DSR change interrupt mask status
RXF_OVERRUN_MASK_STS	[4]	RO	1'h0	RX FIFO overrun interrupt mask status
FRAME_ERR_MASK_STS	[3]	RO	1'h0	Frame error interrupt mask status
PARITY_ERR_MASK_STS	[2]	RO	1'h0	Parity error interrupt mask status
TXF_EMPTY_MASK_STS	[1]	RO	1'h0	TX FIFO empty interrupt enable
RXF_FULL_MASK_STS	[0]	RO	1'h0	RX FIFO full interrupt mask status

6.2.5.2.12 UART_DSPWAIT

Description：UART control register

0x0030			Control register (0x0000_0001)													UART_DSPWAIT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										TX_DMA_MOD_SEL	RX_DMA_MOD_SEL	UART_DSPWAIT			
Type	RO										R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Field Name	Bit	R/W	Reset Value	Description
TX_DMA_MOD_SEL	[5]	R/W	1'h0	0: tx_dma_req keep 1 until receiving the rx_dma_ack 1: tx_dma_req is "1" when rx_full is "1",else "0"
RX_DMA_MOD_SEL	[4]	R/W	1'h0	0: rx_dma_req keep 1 until receiving the rx_dma_ack 1: rx_dma_req is "1" when rx_full is "1",else "0"
UART_DSPWAIT	[3:0]	R/W	4'h1	This register is used for DSP control

6.2.6 Application Notes

Including RAM input and output formats, special requirement, software control flow, description, etc.

Working in UART mode with hardware flow control (full duplex)

1. The initiator writes to the setup register (global register)
2. The initiator writes the UART_CTL0 register bit 15 to "0" to enable UART mode.
3. The initiator configures UART_CKD0 registers to generate the suitable baud rate. For example, if clk_uart is 26 MHz, UART_CKD0 is set to 0xe1, then the UART baud rate is 115 k.
4. The initiator configures UART_CTL0 to generate the suitable data format, such as parity enable and parity style, byte length, and stop bit number
5. Set UART_CTL0 register bit 7 to "1" to enable receive hardware flow control
6. The initiator configures UART_CTL1 register bit [5:0] to suitable value
7. Set UART_CTL0 register bit 8 to "1" to enable transmit hardware flow control
8. The initiator configures UART_CTL2 to generate receive watermark and transmit watermark
9. The initiator writes UART_CTL1 register to configure receive timeout value
10. Enable related interrupts by writing UART_STS2 register

11. Writing data to UART_TXD

Once the TX FIFO is not empty:

12. data in TX FIFO will appear on TX line in sequence
13. If data number in the TX FIFO is less than the data empty threshold value, a txf_empty interrupt will be generated. After receiving this interrupt, MCU should clear the interrupt and write more data into the TX FIFO
14. If data number in the RX FIFO is more than the data full threshold value. An rxf_full interrupt will be generated. After receiving this interrupt, MCU should clear the interrupt and read data from RX FIFO
15. If receiving RX_TOUT interrupt, read all data in the RX FIFO

When the transmission is completed:

16. If RX FIFO is not empty, read all data in the RX FIFO when receiving RX_TOUT interrupt
17. Disable all interrupts, disable uart_en in global register

6.3 SPI Interface

6.3.1 Overview

SPI is a serial synchronous communication interface. SPI block enables the device to interface with SPI peripherals (i.e. A/D converters, display drivers, EEPROMs etcs.) It consists of a serial shift register with serial data input, serial data output and serial shift clock. The shift clock can be selected from either an interval source or an external source. Operating the SPI with the internal clock source is called the Master mode of operation. Similarly, operating the SPI with an external shift clock is called the Slave mode of operation. SPI module support MICROWIRE/PLUS mode, sync mode , s8 mode and 3-wire mode. Only in MICROWIRE/PLUS mode, master and slave both be supported. This document defines function and configuration of SPI block.

SC6820 has 2 SPI controllers, SPI0 & SPI1.

6.3.2 Features

- Compliant with the SPI standard
- Support MICRO/PLUS mode, SYNC mode, S8 mode and 3-wire mode
- Serial clock with programmable frequency , polarity
- Wide selection of SPI word lengths ranging from 1 to 32 bits
- Two 32-word-deep FIFOs minimizes processor overhead at high data rates
- Master / slave
- MSB / LSB
- Transmit only/ receive only / transmit and receive mode
- Only receive mode , the length of words ready to receive form the slave can be programmed
- The intervals of two SPI frames can be programmed
- 2 DMA requests
- Single interrupt line for multiple interrupt source events
- The polarity and position of the sync can be configured
- As slave transmit phase adjustable

- TX/RX FIFO address can be reset

6.3.3 Signal Description

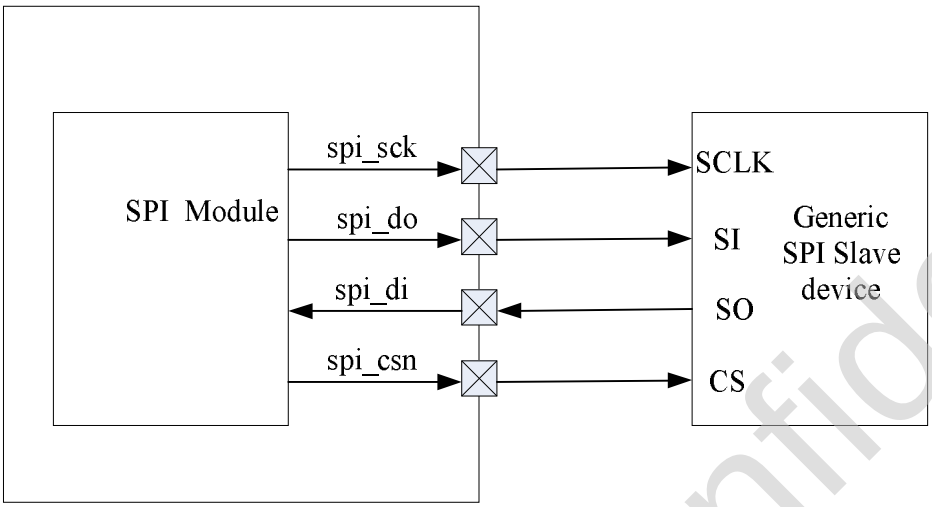


Figure 6-8 SPI in Master Mode(FULL-Duplex)

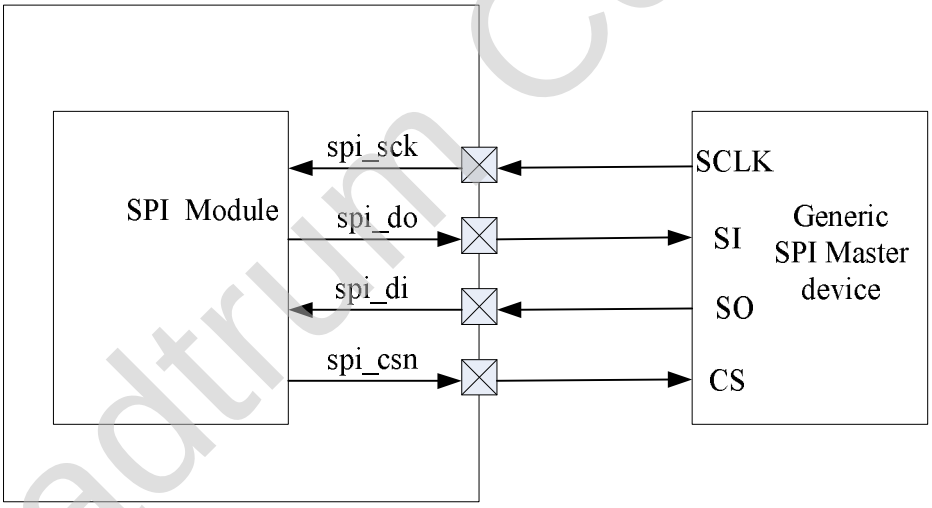


Figure 6-9 SPI in Slave Mode(FULL-Duplex

6.3.4 Function Description

The SPI master mode supports communication with up to two independent SPI devices. SPI initiates a data transfer on the data lines (spi_do and spi_di) and generate clock (sck) and control signals(spi_ncsi).

Write data to this Spi_txd register initiates a character transmission through TX FIFO, the pointer txf_wr_address will increase. All data ready to send must be written into the TX FIFO first, thenoccurs in transmit line.

Data sampled from receive line is placed in RX FIFO first. When the data number in the RX FIFO is more than the receive data full threshold value, an rxf_full interrupt is generated. MCU will read data from RX FIFO as soon as receiving the interrupt.

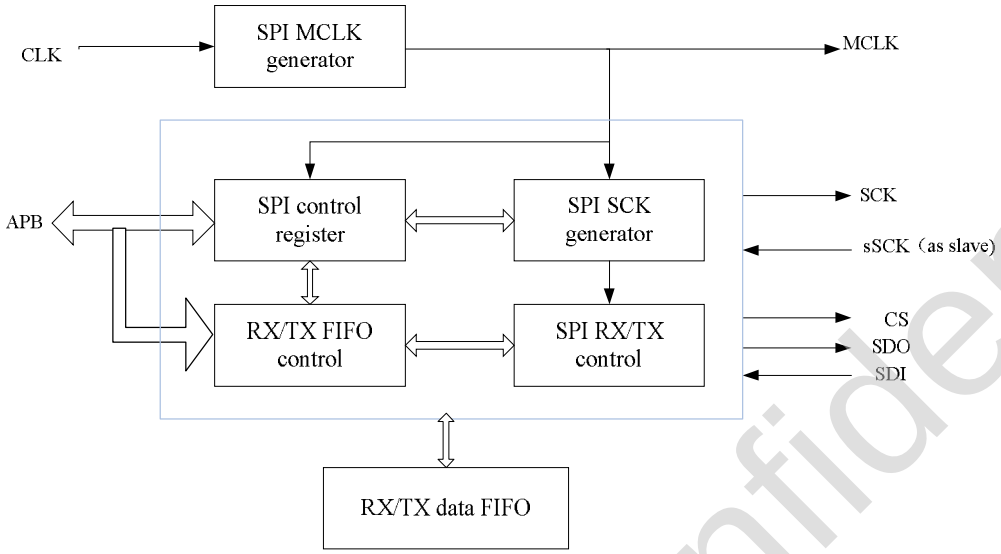


Figure 6-10 diagram of SPI

6.3.4.1 MICROWIRE/PLUS work mode

MICROWIRE/PLUS is an enhancement of the MICROWIRE™ synchronous serial communications scheme, originally implemented by National Semiconductor's COP400 family microcontrollers. It has three wires, SI (serial input), SO (serial output), and SK (serial clock). The input data one the SI is shifted high order first into the chip; the output data is shifted out high order first from the Most Significant Bit (MSB) on SO. The SK clock is generated internally for the master mode. One burst has 8 data bits. The input data is captured on the rising edge of SK. Following is the timing diagram.

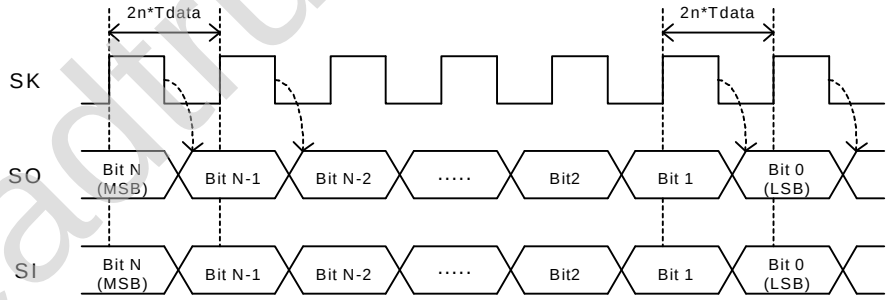


Figure 6-11 MICROWIRE/PLUS Timing (CPOL=0, CPHA=0)

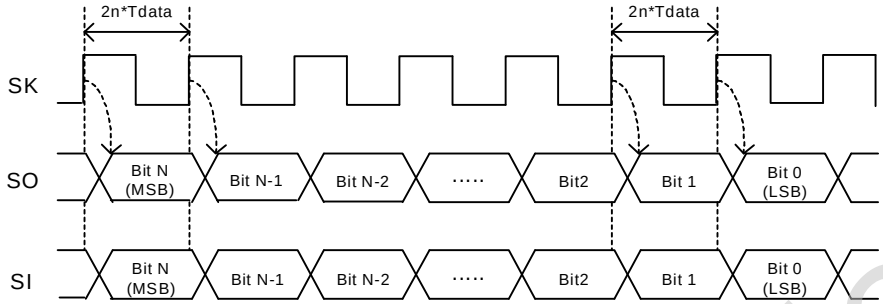


Figure 6-12 Alternated Phase SK Clock Timing (CPOL=0, CPHA=1)

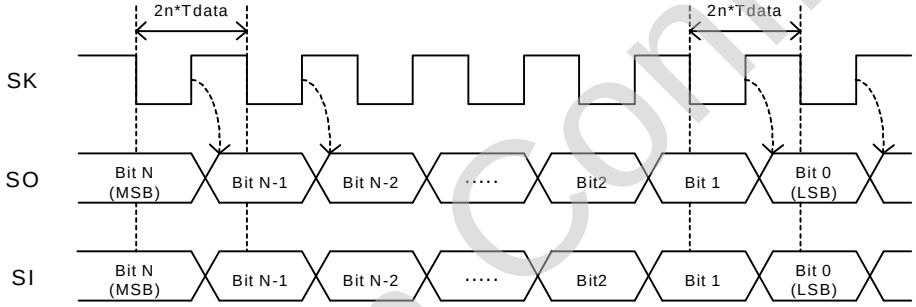


Figure 6-13 MICROWIRE/PLUS Timing (CPOL=1, CPHA=0)

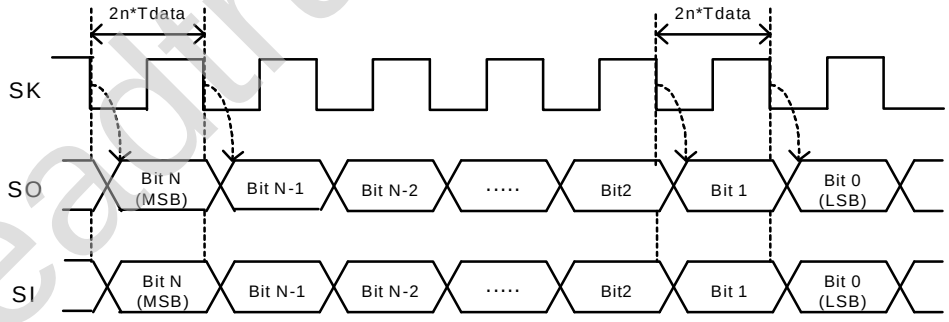


Figure 6-14 MICROWIRE/PLUS Timing (CPOL=1, CPHA=1)

In the normal mode data is shifted in on the rising edge of the SCK clock and data is shifted out on the falling edge of the SCK clock. It is also allow an additional Alternate SCK Phase Operation. In the alternate SCK phase operation, data is shifted in on the falling edge of the SCK clock and data is shifted out on the rising edge of the SCK clock.

To configure SPI for this mode, just enable SPI clock in global control register, program spi_ctl0 control register, enable RX data shift in at SCK rising edge(spi_ctl0[0] = 1), and

enable TX data shift out at SCK falling edge(spi_ctl0[1] = 0), set transmit data bit number to 8 . Also program spi_clkd according to MCLK and SCK clock rate. Leaving other control register with default value. When put data into TX FIFO, the SPI will send and receive an N bit data at the same time.

The clock phase and TX/RX data timing is programmable to meet other requirements. For example, for:

N = 8, CS0, CPOL=0, CPHA =0 timing as Figure6-11, set spi_ctl0 = 0x0e22

N = 8, CS0, CPOL=0, CPHA =1 timing as Figure6-12, set spi_ctl0 = 0x0e21

N = 8, CS0, CPOL=1, CPHA =0 timing as Figure6-13, set spi_ctl0 = 0x2e22

N = 8, CS0, CPOL=1, CPHA =1 timing as Figure6-14, set spi_ctl0 = 0x2e21

CPOL=0 means SCK idle phase is low, maps to spi_ctl0[13] = 0;

CPOL=1 means SCK idle phase is high, maps to spi_ctl0[13]=1;

CPHA decides SPI working in normal mode or in the alternate SK phase operation.

CPHA maps to ctl0_reg[1:0],

“10” (CPHA=0) means output data at negedge of clk while receiving data at posedge of clk

“01”(CPHA=1)means output data at posedge of clk while receiving data at negedge of clk

“00” and “11” are not available in this mode

6.3.4.2 Synchronous SPI

Besides SCK, SDI, SDO, Synchronous SPI provides the fourth pin as a synchronous signal. It generates single bit width pulse on one of the TX/RX bit position. On slave side, it tells when to latch the received byte and prepare the next data for transmit.

If enable sync mode by setting spi_ctl0 register bit14, the sync pulse will appear on the last bit. If program spi_ctl1 register bit 4~0 to N, the sync pulse will locates on top of bit N. The SYNC bit can be program output to one of the 4 chip select pins by setting spi_ctl1[11:8].

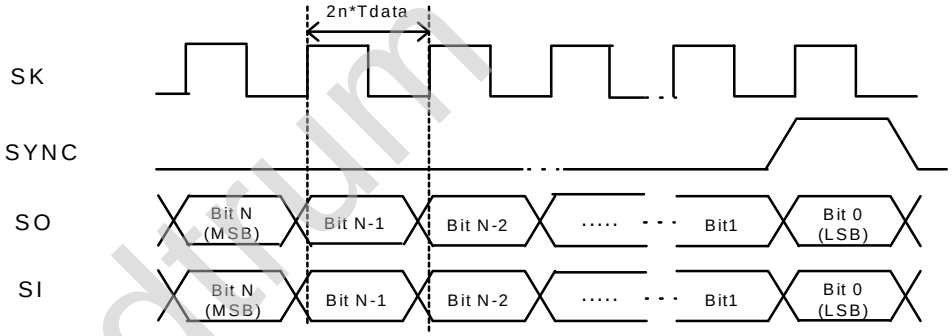


Figure 6-15 Alternated Phase SK Clock Timing (CPOL=0, CPHA=1)

6.3.4.3 4-wire Serial Interface(s8)

SC6820 SPI supports 4-wire serial interface, which required by LCD driver like ULTRACHIP UC1607. Only write operations are supported in this mode. Pin CS is used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. On each write cycle, 8 bits of data, MSB first, are transmitted on falling SCK edges. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data. Pin CD is examined when SCK is pulled low for the LSB(D0) of each burst. The maximum SCK frequency required is 5MHZ.

To enable SPI working in this mode, all settings are same as program MICROWIRE except to enable TX data shifting out at SCK rising edge. Also need to set spi_ctl1 control register bit7, enable s8 mode, and assign the CD signal output from one of the four CS pins by programming bit11~8. Please pay attention to not mapping CD to the same CS pin used for LCD chip select. For example using CS0 as chip select, using cs1 as CD, we

should program spi_ctl0 register bit11~8 “1100” and programming spi_ctl1 register bit11~8 “0010”.

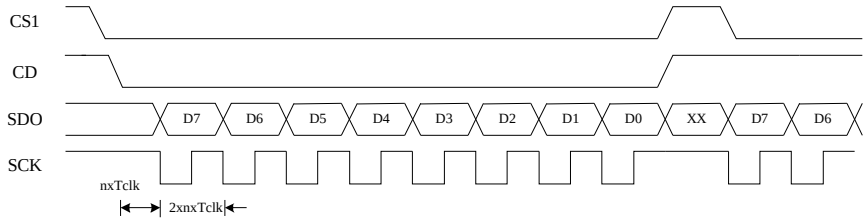


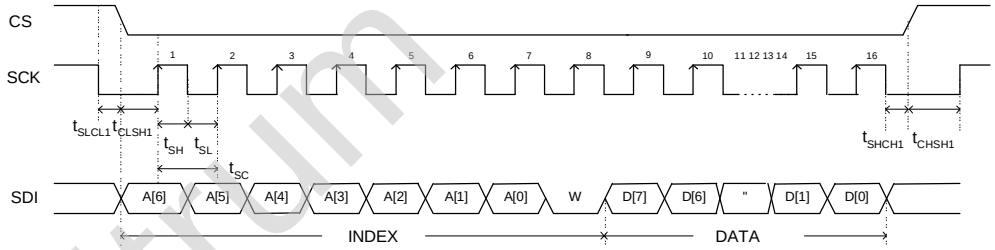
Figure 6-16 4-wire Serial Interface (s8) Timing

SW should write 9 bits data to TX FIFO while ctl0_reg[6:2]] program to 8. Bit 8 is used to control CD signal, and bit[7:0] will be used to transmit to slave.

6.3.4.4 3-wire Serial interface

The 3-wire serial interface is required by Sound Generator Chips like OKIML2860. SDO works as an in/out pin because data has to be read/write through the same pin. SCK is the serial clock, output data from SDO change at clock falling edge, input data is sampled at falling edge. See Figure 8. There is also an alternate SCK phase operation, data output at clock rising edge and input data is sampled at rising edge. See Figure 12. One burst has 16 bits. 7 address bits sent first. Bit8 is command bit. “1” means writing 8 bits data to the slave. “0” means reading 8 bits data from the slave, the read data address in slave is the 7 bits address sent in the same burst.

Data Write Timing 1



Data Read Timing 1

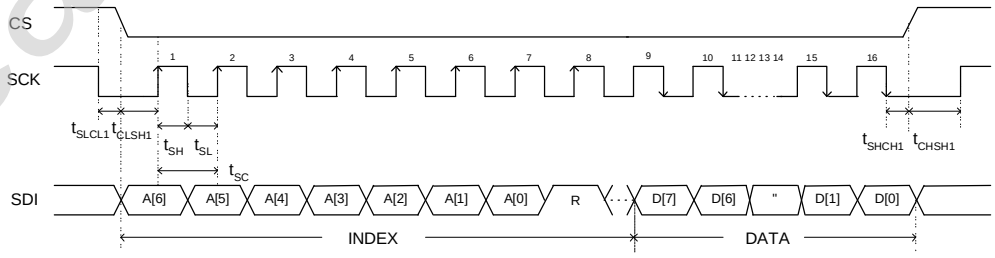
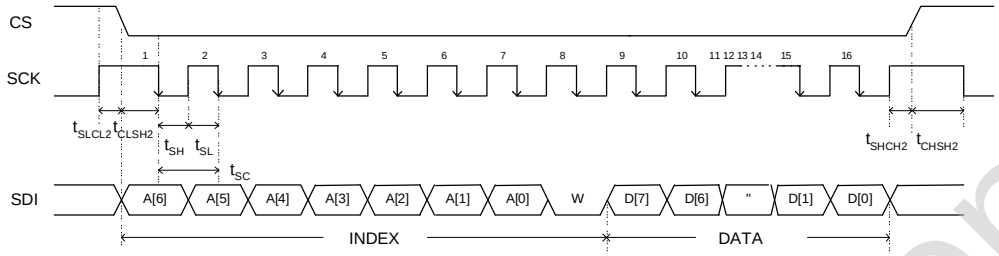


Figure 6-17 3-wire Serial InterfaceTiming 1

Data Write Timing 2



Data Read Timing 2

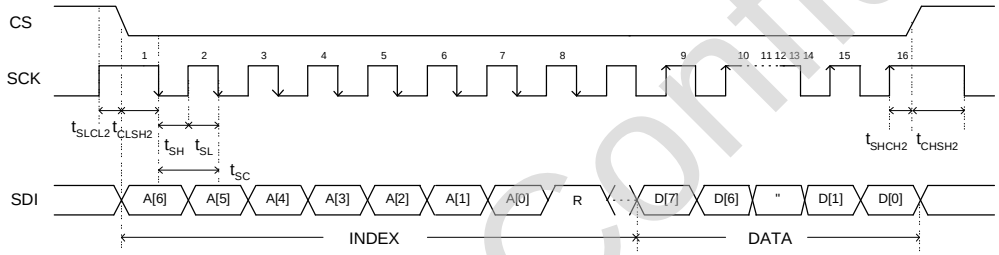


Figure 6-18 3-wire Serial InterfaceTiming 2

To program SPI in this mode, set spi_ctl0 control register to 0x0e43 ,means 16bits sent in one burst, TX at clock falling edge, RX sample at clock falling edge, CS maps to cs0. Set spi_ctl1 to 0x3028 , means to enable 3-wire mode, command bit is bit8. Set spi_ctl2 to 0x07 , the read data starts from bit7. Then put 16 bits data into TX FIFO, and receive 8 bit data from RX FIFO.

If set spi_ctl1 bit6 to “1”, signal CS will change to low before half cycle of the first edge of SCK, and go high after half cycle of the last edge of SCK .

To program alternate SCK phase timing as Figure 9, set spi_ctl0 bit13 to “1”, other setting are same as timing 1.

6.3.5 Control Registers

6.3.5.1 Memory map

ARM base address: 0x8e00_2000 SPI0

0x8e00_3000 SPI1

Offset Address	Name	Description
0x0000	SPI_TXD	Write data to this address initiates a character transmission through tx FIFO Read this address retrieve data from rx fifo
0x0004	SPI_CLKD	Clock divider bit 0 to 15. Divider is (n+1)*2

Offset Address	Name	Description
		Only used for slave mode
0x0008	SPI_CTL0	SPI control register
0x000C	SPI_CTL1	SPI control register
0x0010	SPI_CTL2	SPI control register
0x0014	SPI_CTL3	SPI control register
0x0018	SPI_CTL4	SPI control register
0x001C	SPI_CTL5	SPI control register
0x0020	SPI_INT_EN	SPI interrupt enable register
0x0024	SPI_INT_CLR	SPI interrupt clear register
0x0028	SPI_INT_RAW_STS	SPI interrupt raw status
0x002C	SPI_INT_MASK_STS	SPI interrupt mask status
0x0030	SPI_STS1	SPI status register
0x0034	SPI_STS2	SPI status register
0x0038	DSP_WAIT	Used for DSP control
0x003C	SPI_STS3	SPI status register
0x0040	SPI_CTL6	SPI control register
0x0044	SPI_STS4	SPI status reigster
0x0048	SPI_FIFO_RST	SPI RX/TX FIFO reset bit

6.3.5.2 Register Descriptions

6.3.5.2.1 SPI_TXD

Description：Transmit word or Receive word

0x0000	RTX register (Reset 0x0000_0000)												SPI_TXD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SPI_TXD															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SPI_TXD															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
SPI_TXD	[31:0]	R/W	32'h0	Write data to this address initiates a character

				transmission through TX FIFO Read from this address retrieve data from RX FIFO

6.3.5.2.2 SPI_CLKD

Description：Clock divisor bit 0 to 15

0x0004	Clock divisor (Reset 0x0000_0003)												SPI_CLKD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SPI_CLKD															
Type	SPI_CLKD															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Field Name	Bit	Type	Reset Value	Description
SPI_CLKD	[15:0]	R/W	16'h3	Specify the clock ratio between spi_sck and clk_spi. If clk_spi runs at 48 MHz, and iis_sck runs at 12MHz, SPI_CLKD should be 1, spi_sck = clk_spi/2(n+1).

Note:

When work in the slave mode, the frequency of spi_sck depends on the IIS master, so the register SPI_CLKD is not used .

6.3.5.2.3 SPI_CTL0

Description：This register is used to configuration of the SPI interface

0x0008	Configure register (Reset 0x0000_0F02)												SPI_CTL0			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SYNC_POL	SYNC_MD	SCK_REV	Reserved	SPI_CSN_PRE				LSB	CHNL_LEN					NG_TX	NG_RX
Type	R/W	R/W	R/W	RO	R/W				R/W	R/W					R/W	R/W
Reset	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	0

Field Name	Bit	R/W	Reset Value	Description

SYNC_POL	[15]	R/W	1'h0	Sync_polarity, positive or negative pulse for SPI or 3-wire mode ,read command polarity
SYNC_MD	[14]	R/W	1'h0	"1" : sync mode
SCK_REV	[13]	R/W	1'h0	"1" : spi_sck reverse
Reserved	[12]	RO	1'h0	
SPI_CSN_PRE	[11:8]	R/W	4'hf	4 bit chip select. There are totally 4 chip selects for SPI "1110": cs0 is valid "1101": cs1 is valid ……
LSB	[7]	R/W	1'h0	In default, The input data is shifted high order first into the chip; the output data is shifted out high order first from the Most Significant Bit (MSB) on SO. When this bit is set, the data will be shift out or in from the LSB
CHNL_LEN	[6:2]	R/W	1'h0	Transmit data bit number. "0" : 32 bits per word "1" : 1 bits per word … "31": 31 bits per word
NG_TX	[1]	R/W	1'h1	"1" enable TX data shift out at clock neg-edge
NG_RX	[0]	R/W	1'h0	"1" enable RX data shift in at clock neg-edge

6.3.5.2.4 SPI_CTL1

Description：This register is used to configuration of the SPI interface

0x000C			Configure register (Reset 0x0000_3000)													SPI_CTL1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		RTX_MD		SYN_CSN_SEL				S8_MD	CS_H_MD	S3W_MD	S3W_POS				
Type	RO		R/W		R/W				R/W	R/W	R/W	R/W				
Reset	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:14]	RO	2'h0	

RTX_MD	[13:12]	R/W	2'h3	"00" : idle mode "01" : receive mode "10" : transmit mode "11" : transmit and receive
SYN_CSN_SEL	[11:8]	R/W	4'h0	S8 CD or SYNC signal maps to csn number "0x0001" selects csn0 as cd signal "0x0010" selects csn1 as cd signal …
S8_MD	[7]	R/W	1'h0	"1" : enable S8 mode
CS_H_MD	[6]	R/W	1'h0	3-wire Melody timing 1, csn high mode enable
S3W_MD	[5]	R/W	1'h0	"1" : enable 3-wire mode
S3W_POS	[4:0]	R/W	5'h0	3-wire mode, w/r control position or the sync pulse position(the pulse will locates on top of bit N)

6.3.5.2.5 SPI_CTL2

Description：This register is used to configuration of the SPI interface

0x0010	Configure register (Reset 0x0000_0000)														SPI_CTL2	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						TX_DMA_SEL	RX_DMA_SEL	RX_ONLY_HLD	DMA_EN	IS_SLVD	S3W_RD_STRT				
Type	RO						R/W	R/W	R/W	R/W	R/W	R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

~~Field Name~~	Bit	R/W	Reset Value	Description
Reserved	[15:10]	RO	6'h0	
TX_DMA_SEL	[9]	R/W	1'h0	0: tx_dma_req keep 1 until receiving the tx_dma_ack 1: rx_dma_req is "1" when tx_empty is "1",else "0"
RX_DMA_SEL	[8]	R/W	1'h0	0: rx_dma_req keep 1 until receiving the rx_dma_ack 1: rx_dma_req is "1" when rx_full is "1",else "0"

RX_ONLY_HLD	[7]	R/W	1'h0	"0" : working on only receive mode, when rxf_realfull is high, SPI will be held until rxf_realfull is low "1" : no holding
DMA_EN	[6]	R/W	1'h0	"1" enable DMA mode
IS_SLVD	[5]	R/W	1'h0	"0" : master "1" : slave, only support microplus mode
S3W_RD_STRT	[4:0]	R/W	5'h0	Read data start bit ,used for 3-wire mode

6.3.5.2.6 SPI_CTL3

Description：SPI RX FIFO FULL/EMPTY watermark

0x0014	RXF watermark (Reset 0x0000_1010)															SPI_CTL3
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			RXF_EMPTY_THLD					Reserved			RXF_FULL_THLD				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

~~Field Name~~	Bit	R/W	Reset Value	Description
RXF_EMPTY_THLD	[12:8]	R/W	5'h10	Receive FIFO data empty threshold. Relative with rx_fifo_empty interrupt
Reserved	[7:5]	RO	3'h0	
RXF_FULL_THLD	[4:0]	R/W	5'h10	Receive FIFO data full threshold. Relative with rx_fifo_full interrupt

6.3.5.2.7 SPI_CTL4

Description：This register is used to configuration of the SPI interface

0x0018	Configure register (Reset 0x0000_0000)															SPI_CTL4
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RX_ONLY_DO	IS_FST	PHS_DLY		SYNC_CLKMASK	SYNC_HALF	IS_RX_ONLY	BLOCK_NUM								
Type	R/W	R/W	R/W		R/W	R/W	R/W	R/W								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
RX_ONLY_DO	[15]	R/W	1'h0	working in only receive mode, "0" : SPI send all 0 to slave "1" : SPI send all 1 to slave
IS_FST	[14]	R/W	1'h0	"0" : normal mode "1" : fast mode Only used for slave mode
PHS_DLY	[13:12]	R/W	2'h0	Phase delay. Relate to fast mode. When in normal mode, this bit is not used . Only used for slave mode
SYNC_CLKMASK	[11]	R/W	1'h0	"1" Mask out the first clock pulse in SPI mode
SYNC_HALF	[10]	R/W	1'h0	Sync_half, sync width is half spi_sck cycle
IS_RX_ONLY	[9]	R/W	1'h0	"1":receive data only. The bit should be written at last. Only used for master mode
BLOCK_NUM	[8:0]	R/W	9'h0	Number of data words ready to receive in "receive only" mode. Only used for master mode.

6.3.5.2.8 SPI_CTL5

Description：This register is used to configuration of the SPI interface

0x001C		Configure register(Reset 0x0000_0000)													SPI_CTL5
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ITVL_NUM															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
ITVL_NUM	[15:0]	R/W	16'h0	For master, transmit data interval, programmable n from 0 to 65535, delay is (n*4+3) clock cycle(clk_spi). For slave, max receive data interval. If the slave has not sampled the edge of spi_clk in the interval(n*4+3)(clk_spi), slave will stop the receive process and send timout interrupt

6.3.5.2.9 SPI_INT_EN

Description：SPI interrupt enable register

0x0020		Interrupt enable (Reset 0x0000_0000)													SPI_INT_EN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								TXF_EMPTY_INT_EN	RXF_FULL_INT_EN	TIME_OUT_INT_EN	RX_OVF_INT_EN	Reserved	TXF_FULL_INT_EN	RXF_EMPTY_INT_EN	Reserved
Type	RO								R/W	R/W	R/W	R/W	RO	R/W	R/W	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description

TXF_EMPTY_INT_EN	[7]	R/W	1'h0	txf_empty interrupt enable
RXF_FULL_INT_EN	[6]	R/W	1'h0	Rxf_full interrupt enable
TIME_OUT_INT_EN	[5]	R/W	1'h0	Slave mode timeout interrupt enable
RX_OVF_INT_EN	[4]	R/W	1'h0	Rx_overrun_reg interrupt enable
Reserved	[3]	RO	1'h0	
TXF_FULL_INT_EN	[2]	R/W	1'h0	Tx_fifo_full interrupt enable
RXF_EMPTY_INT_EN	[1]	R/W	1'h0	Rx_fifo_empty interrupt enable
Reserved	[0]	RO	1'h0	

6.3.5.2.10 SPI_INT_CLR

Description：SPI interrupt clear register

0x0024	Interrupt clear (Reset 0x0000_0000)														SPI_INT_CLR	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										TIME_OUT_INT_CLR	RX_OVF_INT_CLR	Reserved	TXF_FULL_INT_CLR	RXF_EMPTY_INT_CLR	Reserved
Type	RO										WO	WO	RO	WO	WO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TIME_OUT_INT_CLR	[5]	WO	1'h0	Write "1" clear slave mode timeout interrupt
RX_OVF_INT_CLR	[4]	WO	1'h0	Write "1" clear Rx_overrun_reg interrupt
Reserved	[3]	RO	1'h0	
TXF_FULL_INT_CLR	[2]	WO	1'h0	Write "1" clear Tx_fifo_full interrupt
RXF_EMPTY_INT_CLR	[1]	WO	1'h0	Write "1" clear Rx_fifo_empty interrupt
Reserved	[3]	RO	1'h0	

6.3.5.2.11 SPI_INT_RAW

Description：SPI interrupt raw status

0x0028			Raw status (Reset 0x0000_008A)												SPI_INT_RAW_STS	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								TXF_EMPTY_RAW_STS	RXF_FULL_RAW_STS	TIME_OUT_RAW_STS	RX_OVF_RAW_STS	TX_FIFO_EMPTY_W	TXF_FULL_RAW_STS	RXF_EMPTY_RAW_STS	RX_FIFO_FULL_R
Type	RO								RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0

Field Name	Bit	R/W	Reset Value	Description
TXF_EMPTY_RAW_STS	[7]	RO	1'h1	Raw txf_empty interrupt, This bit is set when the number of tx fifo data byte is less than the tx empty watermark value. Auto cleared when the condition disappears.
RXF_FULL_RAW_STS	[6]	RO	1'h0	Raw rxf_full interrupt.This bit is set when the number of rx fifo data byte is larger than the rx full watermark value. Auto cleared when the condition disappears.
TIME_OUT_RAW_STS	[5]	RO	1'h0	Raw slave mode time out interrupt
RX_OVF_RAW_STS	[4]	RO	1'h0	Raw Rx_overrun_reg interrupt
TX_FIFO_EMPTY_W	[3]	RO	1'h1	Txf_empty_w(for debug)
TXF_FULL_RAW_STS	[2]	RO	1'h0	Raw Tx_fifo_full interrupt
RXF_EMPTY_RAW_STS	[1]	RO	1'h1	Raw rx_fifo_empty interrupt
RX_FIFO_FULL_R	[0]	RO	1'h0	Rxf_full_r(for debug)

6.3.5.2.12 SPI_INT_MASK_STS

Description：IIS interrupt raw status

0x002C			Mask status (Reset 0x0000_0000)										SPI_INT_MASK_STS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								TXF_EMPTY_MASK_STS	RXF_FULL_MASK_STS	TIME_OUT_MASK_STS	RX_OVF_MASK_STS	Reserved	TXF_FULL_MASK_STS	RXF_EMPTY_MASK_STS	Reserved
Type	RO								RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_EMPTY_MASK_STS	[7]	RO	1'h1	Txf_empty interrupt mask status.
RXF_FULL_MASK_STS	[6]	RO	1'h0	Rxf_full interrupt mask status.
TIME_OUT_MASK_STS	[5]	RO	1'h0	Slave mode time out interrupt mask status
RX_OVF_MASK_STS	[4]	RO	1'h0	Rx_overrun_reg interrupt mask status
Reserved	[3]	RO	1'h0	
TXF_FULL_MASK_STS	[2]	RO	1'h0	Tx_fifo_full interrupt mask status
RXF_EMPTY_MASK_STS	[1]	RO	1'h1	Rx_fifo_empty interrupt mask status
Reserved	[0]	RO	1'h0	

6.3.5.2.13 SPI_STS1

Description：SPI RX FIFO write address and read address

0x0030			RXF address (Reset 0x0000_0000)												SPI_STS1	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		RXF_WADDR						Reserved			RXF_RADDR				
Type	RO		RO						RO			RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
RXF_WADDR	[12:8]	RO	5'h0	RX FIFO write address
Reserved	[7:5]	RO	3'h0	
RXF_RADDR	[4:0]	RO	5'h0	RX FIFO read address

6.3.5.2.14 SPI_STS2

Description：SPI status register

0x0034	Register description (Reset 0x0000_12AA)													SPI_STS2		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
SPI_CS	[12]	RO	1'h1	Spi_cs(for debug)
SPI_SCK	[11]	RO	1'h0	Spi_sck(for debug)
SPI_TXD	[10]	RO	1'h0	Spi_txd(for debug)
SPI_RXD	[9]	RO	1'h1	Spi_rxd(for debug)
BUSY	[8]	RO	1'h0	"1" transmit process "0" idle state
TXF_REAL_EMPTY	[7]	RO	1'h1	TX FIFO has no data
TXF_REAL_FULL	[6]	RO	1'h0	TX FIFO is real full. (not relates to TX full threshold)
RXF_REAL_EMPTY	[5]	RO	1'h1	RX FIFO has no data
RXF_REAL_FULL	[4]	RO	1'h0	RX FIFO is real full. (not relates to TX full threshold)
TXF_EMPTY	[3]	RO	1'h1	This bit is set when the number of TX FIFO data byte is less than the TX empty interrupt watermark value. Auto cleared when the condition disappears.
TXF_FULL	[2]	RO	1'h0	This bit is set when the number of TX FIFO data byte is larger than the TX full interrupt watermark value. Auto cleared when the condition disappears.
RXF_EMPTY	[1]	RO	1'h1	This bit is set when the number of RX FIFO data byte is less

				than the RX empty interrupt watermark value. Auto cleared when the condition disappears.
RXF_FULL	[0]	RO	1'h0	This bit is set when the number of RX FIFO data byte is larger than the RX full interrupt watermark value. Auto cleared when the condition disappears.

6.3.5.2.15 SPI_DSPWAIT

Description：This register is used for DSP control

0x0038			Register description (Reset 0x0000_0001)												SPI_DSPWAIT	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												IIS_DSPWAIT			
Type	RO												R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Field Name	Bit	R/W	Reset Value	Description
SPI_DSPWAIT	[3:0]	R/W	4'h1	This register is used for DSP control

6.3.5.2.16 SPI_STS3

Description：This register is used to observe the status

0x003C			Register description (Reset 0x0000_0000)												SPI_STS3	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							RX_CNT								
Type	RO							RO								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
RX_CNT	[8:0]	RO	9'h0	working in only receive mode as master

6.3.5.2.17 SPI_CTL6

Description：This register is used to configuration of the SPI interface

0x0040	Register description (Reset 0x0000_1010)															SPI_CTL6
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			TXF_EMPTY_THLD					Reserved			TXF_FULL_THLD				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_EMPTY_THLD	[12:8]	R/W	5'h10	TX FIFO data empty threshold. Relative with rx_fifo_empty interrupt
Reserved	[7:5]	RO	3'h0	
TXF_FULL_THLD	[4:0]	R/W	5'h10	TX FIFO data full threshold. Relative with rx_fifo_full interrupt

6.3.5.2.18 SPI_STS4

Description：SPI status register

0x0044	Register description (Reset 0x0000_0000)															SPI_STS4
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			TXF_WADDR					Reserved			TXF_RADDR				
Type	RO			RO					RO			RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_WADDR	[12:8]	RO	5'h0	TX FIFO write address
Reserved	[7:5]	RO	3'h0	
TXF_RADDR	[4:0]	RO	5'h0	TX FIFO read address

6.3.5.2.19 SPI_FIFO_RST

Description：Used to reset TX/RX FIFO

0x0048			Register description (Reset 0x0000_0000)													SPI_FIFO_RST
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															SPI_FIFO_RST
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
SPI_FIFO_RST	[0]	R/W	1'h0	"1" : reset all FIFOs. FIFO address will changed to 0

6.3.6 Application Notes

6.3.6.1 Programming Model

6.3.6.1.1 MICRO/PLUS mode program examples

1. MICRO/PLUS mode, master, 32 bits per-channel, MCLK 80M, SCK 20M, CS0 is valid, RX at rising edge, TX at negedge, SCK idle phase being low, Program control register:

   Spi_clkd = 0x0001;
   Spi_ctl0 = 0x0e02;
   Spi_ctl1 = 0x3000;
   Spi_ctl2 = 0x0;
   Spi_ctl3 = 0x1010;
   Spi_ctl4 = 0x0;
   Spi_ctl5 = 0x0;
   Spi_ctl6 = 0x1010

2. 16 bits per-channel, master, MCLK 80M, SCK 10M, only receive mode, ready to receive 0x1f words from slave, CS1 is valid, RX at falling edge, TX at rising edge, SCK idle phase being low,Program control register:

   Spi_clkd = 0x0003;
   Spi_ctl0 = 0x0d41;
   Spi_ctl1 = 0x1000;
   Spi_ctl2 = 0x0;
   Spi_ctl3 = 0x1010;
   Spi_ctl4 = 0x021f;
   Spi_ctl5 = 0x0;
   Spi_ctl6 = 0x1010

3. 8 bits per-channel, master, MCLK 48M, SCK 24M, CS2 is valid, RX at falling edge, TX at rising edge, SCK idle phase being high, LSB, dma_en, Program control register:

```
Spi_clkd = 0x0000;
Spi_ctl0   = 0x26b2;
Spi_ctl1   = 0x3000;
Spi_ctl2   = 0x40;          //bit[6], enable dma
Spi_ctl3   = 0x1010;
Spi_ctl4   = 0x0000;
Spi_ctl5   = 0x0;
Spi_ctl6   = 0x1010
```

4. MICRO/PLUS mode, master, 32 bits per-channel, MCLK 80M, SCK 20M, CS0 is valid, RX at rising edge, TX at negedge, SCK idle phase being low, transmit only, Program control register:

```
          Spi_clkd = 0x0001;
Spi_ctl0   = 0x0e02;
Spi_ctl1   = 0x2000;   // transmit only
Spi_ctl2   = 0x0;
Spi_ctl3   = 0x1010;
Spi_ctl4   = 0x0;
Spi_ctl5   = 0x0;
Spi_ctl6   = 0x1010
```

5. MICRO/PLUS mode, slave, 32 bits per-channel, RX at rising edge, TX at negedge, SCK idle phase being low, Program control register :

```
Spi_clkd   //no use when SPI working as slave , half SCK must have at least 4
           system(MCLK) clock cycle.
Spi_ctl0   = 0x0f02;
Spi_ctl1   = 0x3000;
Spi_ctl2   = 0x20;
Spi_ctl3   = 0x1010;
Spi_ctl4   = 0x0;
Spi_ctl5   = 0x80;
Spi_ctl6   = 0x1010
```

6. MICRO/PLUS mode, slave, 8 bits per-channel, RX at falling edge, TX at rising edge, SCK idle phase being low, TX only/ RX only, Program control register:

```
Spi_ctl0   = 0x0e21;
Spi_ctl1   = 0x2000(TX only);   / spi_ctl1 = 0x1000(RX only)
Spi_ctl2   = 0x20;
Spi_ctl3   = 0x1010;
Spi_ctl4   = 0x0;
Spi_ctl5   = 0x90;
Spi_ctl6   = 0x1010
```

6.3.6.1.2 SYNC mode program examples

Only work in master mode.

Relative register: spi_ctl0[15:14], spi_ctl1[4:0], spi_ctl1[11:8],

1. SYNC mode, master, 32 bits per-channel, MCLK 48M, SCK 12M, RX at rising edge, TX at falling edge, CS0 is valid , and signal sync maps to cs2, Program control register:

   Spi_clkd = 0x0001;

   Spi_ctl0 = 0x4a02;//biy[14] enable sync mode, bit[15] = 0 means positive pulse

   Spi_ctl1 = 0x3400;// sync pulse position will locate on top of bit0, sync maps to cs2

   Spi_ctl2 = 0x0;

   Spi_ctl3 = 0x1010;

   Spi_ctl4 = 0x0;

   Spi_ctl5 = 0x0;

   Spi_ctl6 = 0x1010

6.3.6.1.3 4-WIRE(S8) mode program examples

only work in master mode and only operation write being supported, TX at falling edgerelative register: spi_ctl1[7], spi_ctl1[11:8].

1. S8 mode, 8 bits per-channel, TX at falling edge, CS0 is valid and signal CD maps to cs1, program control register:

   Spi_ctl0 = 0x2c21;

   Spi_ctl1: 0x3280;

6.3.6.1.4 3-WIRE mode program examples

Only work in master mode.

Relative register: spi_ctl0[15], spi_ctl1[4:0], spi_ctl1[5], spi_ctl1[6], spi_ctl2[4:0]

1. timing1(TX RX at falling edge), 16 bits per-channel, CS0 is valid, read command polarity is high, w/r control position is 8, read data start bit is 7, program control register:

   spi_ctl0 = 0x0e43;

   spi_ctl1 = 0x3068;

   spi_ctl2 = 0x07;

2. timing2(TX RX at rising edge), 16 bits per-channel, CS0 is valid, read command polarity is low, w/r control position is 8, read data start bit is 7, program control register:

   spi_ctl0 = 0xae43;

   spi_ctl1 = 0x3068;

   spi_ctl2 = 0x07;

6.3.6.2 Programming Notes

1. only receive mode

   as master: set spi_ctl4[9] = 1 and set spi_ctl1[13:12] = “01” and program spi_ctl4[8:0] to N, means enable rx only mode , and ready to receive N words from slave.

   as slave: set spi_ctl1[13:12] = “01” , the received number depending on master the posedge of is_rx_only(spi_ctl4[9] = 1) will trigger the process, so SW should write to “0” first, then write to “1” to this bit.

2. fast mode

   used for slave mode. In slave mode, half SCK must have at least 4 system clock cycle.

   When SCK < 14X MCLK, recommend to use fast mode.

8X : is_fst(spi_ctl4[14]) =1, phs_dly([spi_ctl4[13:12]] = 1

10X : is_fst=1, phs_dly = 2

12X : IS_fst=1, phs_dly = 3

3. In salve mode, spi_ctl5[15:0]* Tclk_spi should not be such smaller than Tspi_sck, so as not to make SPI stop transfer.

4. DMA enable
   a) DMA should be configured first
   b) Program SPI control register except spi_ctl2[6]
   c) Write spi_ctl2[6] at last

5. When change SPI control register configuration , SW should ensure:
   a) tx_fifo is real empty at first
   b) then, rx_fifo is real empty
   c) change SPI control register

6.4 IIS and PCM Interface

6.4.1 Overview

IIS is a common digital audio interface specification. SC6820 IIS Interface can be used to implement a CODEC interface with external digital audio system working as host or slave. The IIS interface supports both IIS and PCM data format. The interface can transmit and receive data simultaneously as well as transmit or receive data alternatively at a time. This document defines function and configuration of IIS block.

SC6820 IIS module is controlled by ARM or DSP depending on global register IIS0_CTRL_SEL/IIS1_CTRL_SEL, when this bit is set to “1”, DSP controls IIS, else ARM controls IIS.

SC6820 has 2 IIS controllers, IIS0 & IIS1.

6.4.2 Features

- Compliant with the IIS/PCM standard
- Support IIS , MSB-Justified and DSP data bus interface working on IIS mode
- Support Long Frame, Short Frame and Multi-cycle Frame working on PCM mode
- Serial clock with programmable frequency
- Two 32-word-deep FIFOs minimizes processor overhead at high data rates
- LRCK polarity can be configured
- Wide selection of IIS data lengths 8,16,32bits
- Master / slave
- MSB / LSB
- Transmit only/ receive only / transmit and receive mode
- 2 DMA requests
- Single interrupt line for multiple interrupt source events

6.4.3 Signal Description

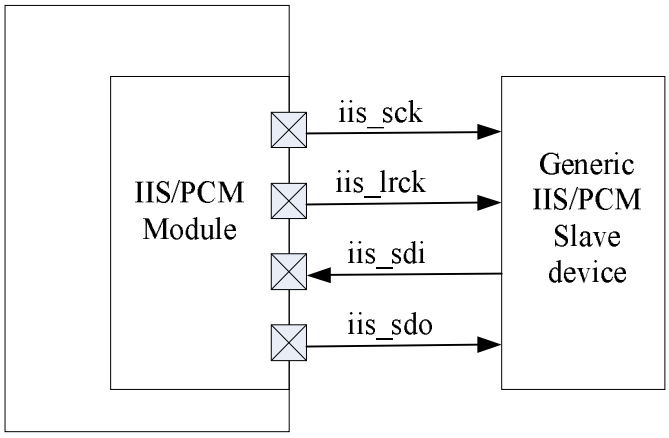


Figure 6-19 IIS connection as master

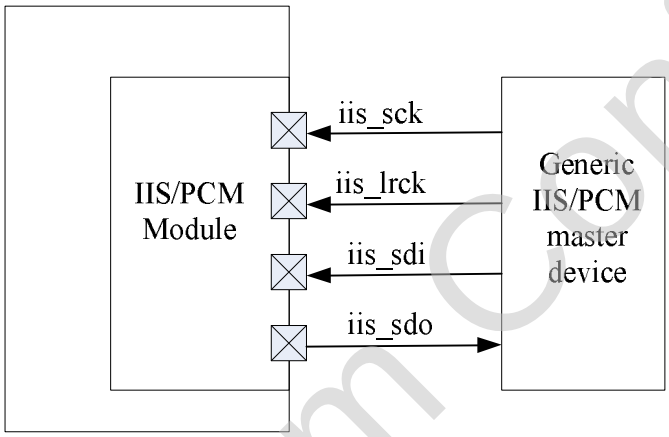


Figure 6-20 IIS connection as slave

6.4.4 Function Description

6.4.4.1 IIS interface and Timing modes

IIS module consists of RX/TX controller, ARM APB interface control register, clock generator and FIFO control. ARM programs IIS register, enable IIS mode, starts RX/TX data transfer. Output data is written to TX FIFO and received data is stored in RX FIFO. Each FIFO is 32-bit width plus 32-address length.

MCLK generator generates main clock for IIS block. This clock also output as master clock during hand shaking. In slave mode, external clock source can be input, working as the IIS main clock. Clock divider value and control signal for MCLK come from global control register.

The IIS SCLK generator divides main clock according to a 16-bit clock divider register, which defines half SCLK clock width. It can be programmed from 0 to 32767.

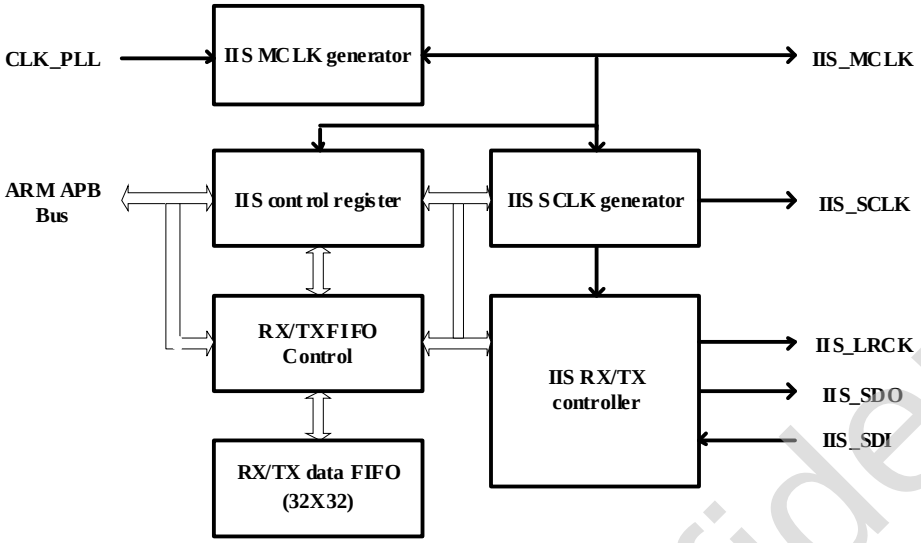


Figure 6-21 diagram of IIS

IIS interface has 4 pins, IIS_SCK is serial clock output, IIS_SDI is serial data input, IIS_SDO is serial data output. IIS_LRCK is left/right channel select. The device generating IIS_LRCK and IIS_SCK is the master. IIS_LRCK and IIS_SCK are output pins if working as master. They are input pins if working as slave.

Serial data is transmitted in two's complement format with the MSB first. Serial data can be sent at rising or falling edge of SCK, at receiver, it must be latched at rising edge. When system word length is greater than the transmitter word length, the word is truncated (least significant data bits are set to '0') for data transmission. If the receiver is sent more bits than its word length, the bits after the LSB are ignored. On the other hand, if the receiver is sent fewer bits than its word length, the missing bits are set to zero internally.

Three bus formats are available in this module. Following Figures illustrate the relationship between the SCK, LRCK and serial data I/O for different interface protocols. The polarity of LRCK is programmable. The bits per-channel is programmable up to 32bit.

IIS mode is where the MSB is available on the 2nd rising edge of SCLK following a LRCK transition.

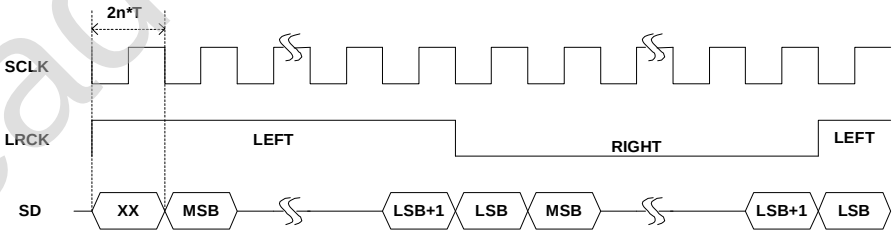


Figure 6-22 IIS-compatible Serial Format

MSB-justified mode is where the MSB is available on the first rising edge of SCK following a LRCK transition.

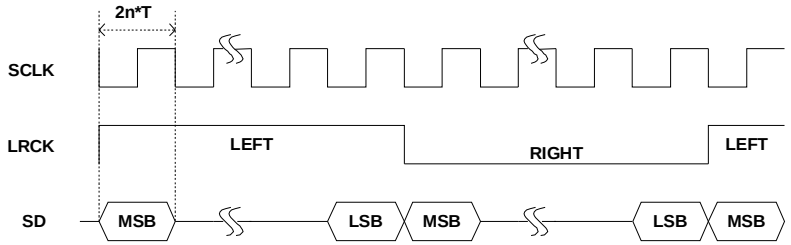


Figure 6-23 MSB-justified Format

Sync mode is where the left channel MSB is available on either the 1st or 2nd rising edge of BCLK following a LRCK transition high. Right channel data immediately follows left channel data.

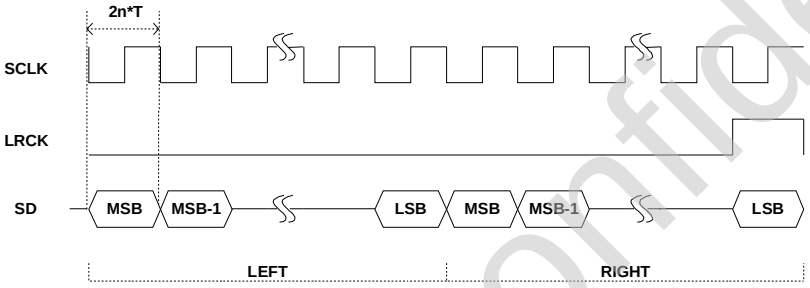


Figure 6-24 Synchronized Format

Symbol	Parameter	Min	Max	Unit
T	System clock cycle	T	–	ns

Note:

T: 1/(system clock frequency)

n: register programmable integer, n-1 = 1, …., 32767

6.4.4.2 PCM interface

PCM interface is a direct voice interface connects to standard CODEC. The implementation is compliant with the MP-PCM requirements for voice transfer (8 kHz PCM_SYNC and 8 or 16 bits data). The four signals of the PCM interface are:

– PCM_CLK: PCM clock

– PCM_SYNC: PCM 8KHz synchronization signal

– PCM_OUT: PCM output data

– PCM_IN: PCM input data

These four pins is able to share IIS interface follow this mapping:

PCM_CLK share with IIS_SCK,

PCM_IN share with IIS_SDI,

PCM_OUT share with IIS_SDO,

PCM_SYNC share with IIS_LRCK.

The data can be linear PCM (13-16 bit), μ-Law (8 bit) or A-Law (8bit). The interface can work as either Master or Slave.

Programming IIS_CTL 0 register bit 15 to 1 configures the PCM mode.

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC

indicates the start of the PCM word. When SC6820 is configured as PCM Master, generating PCM_SYNC and PCM_CLK, 8 bits in one frame, then PCM_SYNC is 7-bit long. When SC6820 is configured as PCM Slave, PCM_SYNC may be from one consecutive falling edges of PCM_CLK to not big or equal than PCM data length (as figure shows, PCM_SYNC is 2~7.5 bits) long.

Programming IIS_CTL0 register bit8 to zero configures the Long Frame Sync mode.

PCM_IN is captured on the falling edge of PCM_CLK and PCM_OUT transmits on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge. The control bit is IIS_CTL2 bit10, if high, OE changes to low at falling edge of the last bit.

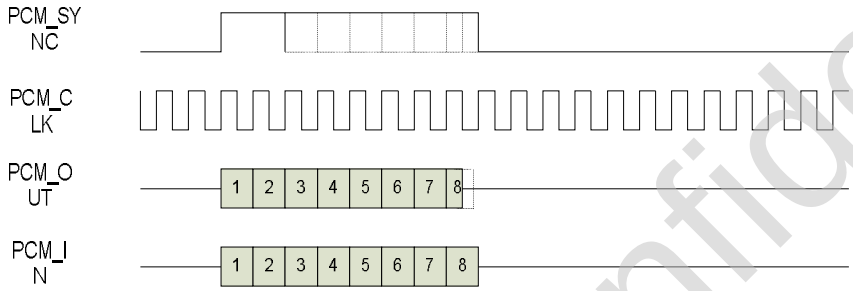


Figure 6-25 Long Frame Sync (Shown with 8-bit Sample)

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

As with Long Frame Sync, SC6820 samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

Programming IIS_CTL0 register bit8 to high configures the Short Frame Sync mode.

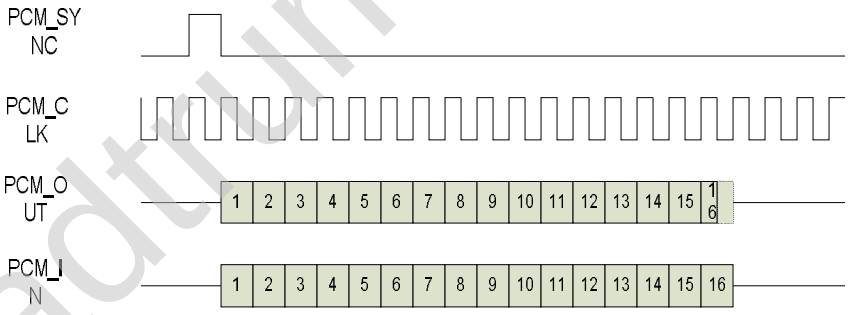


Figure 6-26 Short Frame Sync (Shown with 16-bit Sample)

More than one channel connection over the PCM interface is supported using multiple slots. Up to three channel connections can be carried over any of the first three slots.

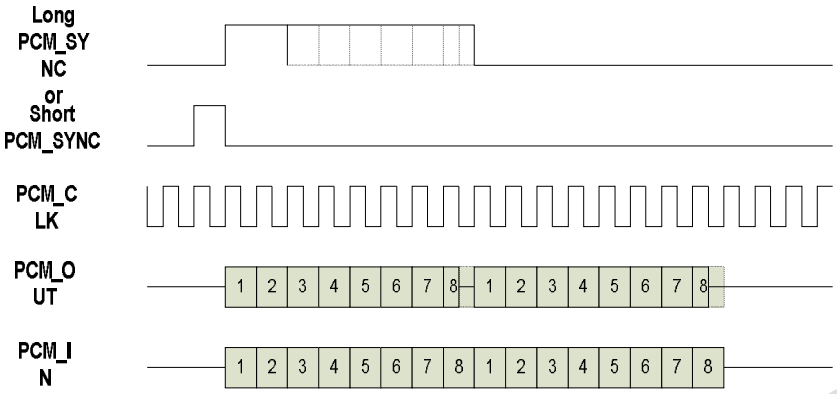


Figure 6-27 Multi-slot Operation with Two Slots and 8-bit Compounded Samples

Three slots can be configured in one PCM frame; IIS_CTL2 register bit 2~0 define which channel is occupied. Each bit configures one of the three channels. If bit0 is high, then slot0 is carrying data. If channel 0 and 2 is active, this register is 0x5.

PCM data format in TX/RX buffer is different between master and slave mode. If burst size is 16 or 8bit, in slave mode, data for slot 0 and slot 1 are packed into one word, which locates in lower address; data for slot2 locates in higher address; slot0 and slot2 fill higher bits (bit31~24). In master mode, only slot0 takes lower address and locates on lower bits (bit15~8); slot1, slot2 packed in higher address, and slot2 takes lower bits while slot1 in higher bits. Following table shows PCM data format for master and slave mode.

Table 6-3 PCM data format for master mode

IIS_CTL bit1~0	Bits/channel	Data arrangement
00	8bit	Data for channel 0 on bit 15~8, in lower address. Data for channel 1 on bit 31~24, Data for channel 2 on bit 15~8, on higher address.
01	16bit	Data for channel 0 on bit 15~0, in lower address. Data for channel 1 on bit 31~16, Data for channel 2 on bit 15~0, on higher address
1x	32bit	Data for channel 0 store in low address, data for channel 1, 2 store in high address.

Table 6-4 PCM data format for slave mode

IIS_CTL bit1~0	Bits/channel	Data arrangement
00	8bit	Data for channel 0 on bit 31~24, Data for channel 1 on bit 15~8, in lower address. Data for channel 2 on bit 31~24, on higher address.
01	16bit	Data for channel 0 on bit 31~16, Data for channel 1 on bit 15~0,

		in lower address. Data for channel 2 on bit 31~16, on higher address
1x	32bit	Data for channel 0 store in low address, data for channel 1, 2 store in high address.

6.4.5 Control Registers

6.4.5.1 Memory map

ARM base address: 0x8E00_1000 IIS0

0x8E00_4000 IIS1

Offset Address	Name	Description
0x0000	IIS_TXD	Write data to this address initiates a character transmission through TX FIFO Read from this address retrieve data from RX FIFO
0x0004	IIS_CLKD	Divisor is (n+1)*2
0x0008	IIS_CTRL0	Control register
0x000C	IIS_CTRL1	Control register
0x0010	IIS_CTRL2	Control register
0x0014	IIS_CTRL3	RX FIFO watermark
0x0018	IIS_INT_IEN	IIS interrupt enable register
0x001C	IIS_INT_CLR	IIS interrupt clear register
0x0020	IIS_INT_RAW	IIS interrupt raw status
0x0024	IIS_INT_STS	IIS interrupt mask status
0x0028	IIS_STS1	RX FIFO address
0x002C	IIS_STS2	IIS internal status
0x0030	IIS_STS3	IIS internal status
0x0034	IIS_DSPWAIT	Control register
0x0038	IIS_CTRL4	TX FIFO watermark
0x003C	IIS_STS4	TX FIFO address

6.4.5.2 Register Descriptions

6.4.5.2.1 IIS_TXD

Description： Write data to this address initiates a character transmission through TX FIFO; Read from this address retrieve data from RX FIFO.

0x0000			IIS RTX register(0x0000_0000)													IIS_TXD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	IIS_TXD															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	IIS_TXD															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
IIS_TXD	[31:0]	R/W	32'h0	Write data to this address initiates a character transmission through TX FIFO Read from this address retrieve data from RX FIFO

6.4.5.2.2 IIS_CLKD

Description：Clock divisor bit 0 to 15

0x0004			Clock divisor (Reset 0x0000_0003)													IIS_CLKD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	IIS_CLKD															
Type	IIS_CLKD															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Field Name	Bit	Type	Reset Value	Description
IIS_CLKD	[15:0]	R/W	16'h3	Specify the clock ratio between iis_sck and clk_iis. If clk_iis runs at 5.12 MHz, and iis_sck runs at 256KHz, IIS_CLKD should be 9, Iis_sck = clk_iis/2(+1).

Note:

When work in the slave mode, the frequency of iis_sck depends on the IIS master, so the register IIS_CLKD is not used.

6.4.5.2.3 IIS_CTL0

Description：IIS control register

0x0008	Control register (Reset 0x0000_00C1)														IIS_CTL0	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PCM_EB	DMA_EN	Reserved		SCK_REV	IS_LRCK_PH	IS_SYNC_MD	IS_IISC_SHRTF	RTX_MD		BPCHN		IS_SLVD	LSB	NG_TX	NG_RX
Type	R/W	R/W	RO		R/W	R/W	R/W	R/W	R/W		R/W		R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1

Field Name	Bit	R/W	Reset Value	Description
PCM_EB	[15]	R/W	1'h0	"1" : PCM mode "0" : IIS mode
DMA_EN	[14]	R/W	1'h0	"1" : enable DMA
Reserved	[13:12]	R/W	2'h0	
SCK_REV	[11]	R/W	1'h0	SCK inverse enable (IIS mode: set to 1 Pcm mode : set to 0)
IS_LRCK_PH	[10]	R/W	1'h0	Active level of left / right channel(0 for PCM mode) "0" : low for left "1" : high for left
IS_SYNC_MD	[9]	R/W	1'h0	Output LRCK or SYNC for IIS mode "0" : LRCK "1" : SYNC(DSP mode)
IS_IISC_SHRTF	[8]	R/W	1'h0	"0" : MSB justified in IIS mode Long frame in PCM mode "1" : iis-compatible format in IIS mode Short frame in PCM mode When DSP mode, this bit should set to 0
RTX_MD	[7:6]	R/W	2'h3	"00" : idle mode "01" : receive mode "10" : transmit mode "11" : transmit and receive
BPCHN	[5:4]	R/W	2'h0	Serial bit per channel "00" : 8 bits "01": 16 bits "1x": 32 bits
IS_SLVD	[3]	R/W	1'h0	"0": IIS/PCM work as master

				“1”: IIS/PCM work as slave
LSB	[2]	R/W	1’h0	“1”: enable transmit data from LSB (PCM can’t support this bit)
NG_TX	[1]	R/W	1’h0	“1” enable TX data shift out at clock neg-edge(use default value, can’ set to 1)
NG_RX	[0]	R/W	1’h1	“1” enable RX data shift in at clock neg-edge (use default value, can’ set to 0)

Note:

[1] NG_RX, NG_TX should be default config

[2] When PCM slave mode, Long Frame sync, Low for left config(PCM_EB=1, IS_SLVD=1, IS_IISC_SHRTF=1), can’t support LSB mode(LSB = 1).

[3] PCM RX and TX mode should be set both, when use PCM RX mode, and write data to tx fifo. Because, PCM sck is controlled by TX mode.

[4] PCM multi slot config, when slot 0 set only, pcm cyc < 3

[5] PCM mode , slave mode can’t support High_for_left(IS_LRCK_PH=1)

[6] DSP mode, slave can’t support High_for_left(IS_LRCK_PH=1)

[7] DSP mode, can’t support iis-compatible format

6.4.5.2.4 IIS_CTL1

Description：IIS configure register

0x000C			Control reigster (Reset 0x0000_0000)													IIS_CTL1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	IS_RXIOSTP	IS_TXIOSTP	IS_FSCNT_EB	IS_NUM_CNT	ITVL_NUM											
Type	R/W	R/W	R/W	R/W	R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
IS_RXIOSTP	[15]	R/W	1’h0	Receive IO stop enable “1” : enalbe
IS_TXIOSTP	[14]	R/W	1’h0	Transmit IO stop enable “1” : enable
IS_FSCNT_EB	[13]	R/W	1’h0	Clock counter enable, for debug “1”: enable

IS_NUM_CNT	[12]	R/W	1'h0	Count clock for one "0" : lrck cycle "1" : sclk cycle
ITVL_NUM	[11:0]	R/W	12'h0	Used for timeout decision for slave mode If the slave has not sampled the edge of iis_sck in the interval (n*4+3)*Tclk_iis, slave will stop the receive process and send timeout interrupt

6.4.5.2.5 IIS_CTL2

Description：IIS control register

0x0010	Control register (Reset 0x0000_0021)															IIS_CTL2
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SYNC_POS					PCM_OE_EN	PCM_CYC							PCM_SLOT		
Type	R/W					R/W	R/W							R/W		
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

~~Field Name~~	Bit	R/W	Reset Value	Description
SYNC_POS	[15:11]	R/W	5'h0	SYNC position when working in DSP format: 0: MSB is available on the 2nd rising edge of SCK Channel length-1: MSB is available on the 1ST rising edge of SCK
PCM_OE_EN	[10]	R/W	1'h0	"1" : Enable data oe change to low at falling edge of last bit (0: enable data oe only for valid data 1: enable data oe for all transimission)
PCM_CYC	[9:3]	R/W	7'h4	Pcm_cycle, used for multi_slot PCM (if not multi slot, set to 0 Mult slot: 1: indicates 1 slot interval between 2 pcm sync(if long frame sync)

				2:indicates 2 slot interval between 2 pcm sync …)
PCM_SLOT	[2:0]	R/W	3'h1	Pcm_slot, used for multi_slot PCM "001": slot 0 is used "010": slot 1 is used "100": slot 2 is used "011": slot 0 and slot 1 are in use …

6.4.5.2.6 IIS_CTL3

Description：IIS RX FIFO FULL/EMPTY watermark value

0x0014			RXF watermark (Reset 0x0000_0808)													IIS_CTL3
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			RXF_EMPTY_THLD					Reserved			RXF_FULL_THLD				
Type	RO								RO							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

~~Field Name~~	Bit	R/W	Reset Value	Description
RXF_EMPTY_THLD	[12:8]	R/W	5'h8	Receive data full threshold
Reserved	[7:5]	R/W	3'h0	
RXF_FULL_THLD	[4:0]	R/W	5'h0	Receive data empty threshold

6.4.5.2.7 IIS_INT_EN

Description：IIS interrupt enable register

0x0018			Interrupt enable (Reset 0x0000_0000)													IIS_INT_EN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								TXF_EMPTY_INT_EN	RXF_FULL_INT_EN	TIME_OUT_INT_EN	RX_OVF_INT_EN	Reserved	TXF_FULL_INT_EN	RXF_EMPTY_INT_EN	Reserved
Type	RO								R/W	R/W	R/W	R/W	RO	R/W	R/W	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_EMPTY_INT_EN	[7]	R/W	1'h0	Rx_fifo_full interrupt enable
RXF_FULL_INT_EN	[6]	R/W	1'h0	Rx_fifo_empty interrupt enable
TIME_OUT_INT_EN	[5]	R/W	1'h0	Slave mode timeout interrupt enable
RX_OVF_INT_EN	[4]	R/W	1'h0	Rx_overrun_reg interrupt enable
Reserved	[3]	R/W	1'h0	
TXF_FUL_INT_EN	[2]	R/W	1'h0	Tx_fifo_full interrupt enable
RXF_EMPTY_INT_EN	[1]	R/W	1'h0	Rx_fifo_empty interrupt enable
Reserved	[0]	R/W	1'h0	

6.4.5.2.8 IIS_INT_CLR

Description：IIS interrupt clear register

0x001C		Interrupt clear (Reset 0x0000_0000)													IIS_INT_CLR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										TIME_OUT_INT_CLR	RX_OVF_INT_CLR	Reserved	TXF_FULL_INT_CLR	RXF_EMPTY_INT_CLR	Reserved
Type	RO										WO	WO	RO	WO	WO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TIME_OUT_INT_CLR	[5]	WO	1'h0	Write "1" clear slave mode timeout interrupt
RX_OVF_INT_CLR	[4]	WO	1'h0	Write "1" clear Rx_overrun_reg interrupt
Reserved	[3]	RO	1'h0	
TXF_FULL_INT_CLR	[2]	WO	1'h0	Write "1" clear Tx_fifo_full interrupt
RXF_EMPTY_INT_CLR	[1]	WO	1'h0	Write "1" clear Rx_fifo_empty interrupt
Reserved	[0]	RO	1'h0	

6.4.5.2.9 IIS_INT_RAW_STS

Description: IIS interrupt raw status

0x0020		Raw status (Reset 0x0000_008A)													IIS_INT_RAW_STS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								TXF_EMPTY_RAW_STS	RXF_FULL_RAW_STS	TIME_OUT_RAW_STS	RX_OVF_RAW_STS	TX_FIFO_EMPTY_W	TXF_FULL_RAW_STS	RXF_EMPTY_RAW_STS	RX_FIFO_FULL_R
Type	RO								RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0

Field Name	Bit	R/W	Reset	Description

			Value	
TXF_EMPTY_RAW_STS	[7]	RO	1'h1	Raw txf_empty interrupt, This bit is set when the number of tx fifo data byte is less than the tx empty watermark value. Auto cleared when the condition disappears.
RXF_FULL_RAW_STS	[6]	RO	1'h0	Raw rxf_full interrupt.This bit is set when the number of rx fifo data byte is larger than the rx full watermark value. Auto cleared when the condition disappears.
TIME_OUT_RAW_STS	[5]	RO	1'h0	Raw slave mode time out interrupt
RX_OVF_RAW_STS	[4]	RO	1'h0	Raw Rx_overrun_reg interrupt
TX_FIFO_EMPTY_W	[3]	RO	1'h1	Txf_empty_w(for debug)
TXF_FULL_RAW_STS	[2]	RO	1'h0	Raw Tx_fifo_full interrupt
RXF_EMPTY_RAW_STS	[1]	RO	1'h1	Raw rx_fifo_empty interrupt
RX_FIFO_FULL_R	[0]	RO	1'h0	Rxf_full_r(for debug)

6.4.5.2.10 IIS_INT_MASK_STS

Description：IIS interrupt mask status

0x0024	Mask status (Reset 0x0000_0000)													IIS_INT_MASK_STS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								TXF_EMPTY_MASK_STS	RXF_FULL_MASK_STS	TIME_OUT_MASK_STS	RX_OVF_MASK_STS	Reserved	TXF_FULL_MASK_STS	RXF_EMPTY_MASK_STS	Reserved
Type	RO								RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_EMPTY_MASK_STS	[7]	RO	1'h1	Txf_empty interrupt mask status.
RXF_FULL_MASK_STS	[6]	RO	1'h0	Rxf_full interrupt mask status.

TIME_OUT_MASK_STS	[5]	RO	1'h0	Slave mode time out interrupt mask status
RX_OVF_MASK_STS	[4]	RO	1'h0	Rx_overrun_reg interrupt mask status
Reserved	[3]	RO	1'h1	
TX_FIFO_FULL_MASK_STS	[2]	RO	1'h0	Tx_fifo_full interrupt mask status
RX_FIFO_EMPTY_MASK_STS	[1]	RO	1'h1	Rx_fifo_empty interrupt mask status
Reserved	[0]	RO	1'h0	

6.4.5.2.11 IIS_STS1

Description：IIS RX FIFO write address and read address

0x0028	RXF address (Reset 0x0000_0000)												IIS_STS1			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			RXF_WR_ADDR					Reserved			RXF_RD_ADDR				
Type	RO			RO					RO			RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
RXF_WR_ADDR	[12:8]	RO	5'h0	RX FIFO write address
Reserved	[7:5]	RO	3'h0	
RXF_RD_ADDR	[4:0]	RO	5'h0	RX FIFO read address

6.4.5.2.12 IIS_STS2

Description：IIS status register

0x002C			Status register (Reset 0x0000_00AA)													IIS_STS2
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			IIS_LRCK	IIS_CLK	IIS_DO	IIS_DI	BUSY	TXF_REALEMPTY	TXF_REALFULL	RXF_REALEMPTY	RXF_REALFULL	TXF_EMPTY	TXF_FULL	RXF_EMPTY	RXF_FULL
Type	RO			RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0

~~Field Name~~	Bit	R/W	Reset Value	Description
IIS_LRCK	[12]	RO	1'h0	IIS_LRCK, for debug
IIS_SCK	[11]	RO	1'h0	IIS_SCK, for debug
IIS_DO	[10]	RO	1'h0	IIS_DO, for debug
IIS_DI	[9]	RO	1'hX	IIS_DI, for debug
BUSY	[8]	RO	1'h0	BUSY, for debug
TXF_REALEMPTY	[7]	RO	1'h1	TX FIFO is real empty. TX FIFO has no data
TXF_REALFULL	[6]	RO	1'h0	TX FIFO is real full.(not relates to register TXF_FULL_THLD)
RXF_REALEMPTY	[5]	RO	1'h1	RX FIFO is real empty. RX FIFO has no data
RXF_REALFULL	[4]	RO	1'h0	RX FIFO is real full.(not relates to register RXF_FULL_THLD)
TXF_EMPTY	[3]	RO	1'h1	This bit is set when the number of TX FIFO data byte is less than the TX empty watermark value. Auto cleared when the condition disappears.
TXF_FULL	[2]	RO	1'h0	This bit is set when the number of TX FIFO data byte is larger than the TX full watermark value. Auto cleared when the condition disappears.
RXF_EMPTY	[1]	RO	1'h1	This bit is set when the number of RX FIFO data byte is less than the RX empty interrupt watermark value. Auto cleared when the condition disappears.
RXF_FULL	[0]	RO	1'h0	This bit is set when the number of RX FIFO data byte is larger than the RX full watermark value. Auto cleared when the

				condition disappears.

6.4.5.2.13 IIS_STS3

Description：IIS status register

0x0030			Status register(Reset 0x0000_0000)										IIS_STS3			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LRCKCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
LRCKCNT	[15:0]	RO	16'h0	Number of clk_iis cycle per SCK cycle or LRCK cycle , depends on ctl1[12].

6.4.5.2.14 IIS_DSPWAIT

Description：This register is used for DSP control

0x0034			Control register(Reset 0x0000_0001)										IIS_DSPWAIT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												IIS_DSPWAIT			
Type	RO												R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Field Name	Bit	R/W	Reset Value	Description
IIS_DSPWAIT	[3:0]	R/W	4'h1	This register is used for DSP control

6.4.5.2.15 IIS_CTL4

Description：IIS TX FIFO full/empty watermark register

0x0038	TXF watermark (Reset 0x0000_0808)												IIS_CTL4			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			TXF_EMPTY_THLD					Reserved			TXF_FULL_THLD				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_EMPTY_THLD	[12:8]	R/W	5'h8	TX FIFO data empty threshold
Reserved	[7:5]	R/W	3'h0	
TXF_FULL_THLD	[4:0]	R/W	5'h8	TX FIFO data full threshold

6.4.5.2.16 IIS_STS4

Description：IIS TXF FIFO write address and read address

0x003C	TXF address (Reset 0x0000_0000)												IIS_STS4			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			TXF_WR_ADDR					Reserved			TXF_RD_ADDR				
Type	RO			RO					RO			RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_WR_ADDR	[12:8]	RO	5'h0	TX FIFO write address
Reserved	[7:5]	RO	3'h0	
TXF_RD_ADDR	[4:0]	RO	5'h0	TX FIFO read address

Note:

[1] in slave mode , when write data to tx fifo , the first data will read to shifter register, prepare for TX, and TXF_RD_ADDR will inc 1. When master request data, slave tx fifo will tx data to master.

6.4.6 Application Notes

6.4.6.1 IIS Program examples

1. Justified format, master, 16 bits per-channel, LRCK low for left, Program control register:
   iis_clkd = 32'0000_000a
   iis_ctl0 = 32'h0000_08d1
   iis_ctl1 = 32'h0000_0f11
   iis_ctl2 = 32'h0000_0000

2. IIS format, master , 8 bits per-channel, LRCK high for left,Program control register:
   iis_clkd = 32'0000_000a
   iis_ctl0 = 32'h0000_0dc1
   iis_ctl1 = 32'h0000_0f11
   iis_ctl2 = 32'h0000_0000

3. DSP (sync) format, master, 16 bits per-channel, MSB is available on the 1st rising edge, Program control register
   iis_clkd = 32'0000_000a
   iis_ctl0 = 32'h0000_0ad1
   iis_ctl1 = 32'h0000_0f11
   iis_ctl2 = 32'h0000_0000

4. DSP format, master, 16 bits per-channel, MSB is available on the 1st rising edge , Program control register:
   iis_clkd = 32'0000_000a
   iis_ctl0 = 32'h0000_0ed1
   iis_ctl1 = 32'h0000_3f11
   iis_ctl2 = 32'h0000_7800

5. Justified mode, slave, 8 bits per-channel, enable clock counter,Program control register:
   iis_ctl0 = 32'h0000_08c9
   iis_ctl1 = 32'h0000_3f22
   iis_ctl2 = 32'h0000_0000

6.4.6.2 PCM program examples

Programming IIS_CTL0 register bit[15] "1" enable SC6820 working in PCM mode

1. Long Frame format, master, 8 bits per-channel, RX at falling edge, TX at rising edge, Program control register:
   iis_clkd = 32'0000_000a
   iis_ctl0 = 32'h0000_80c1
   iis_ctl1 = 32'h0000_0f11
   iis_ctl2 = 32'h0000_0001

2. Short Frame format, master, 8 bits per-channel,
   iis_clkd = 32'0000_000a
   iis_ctl0 = 32'h0000_81c1
   iis_ctl1 = 32'h0000_0f11

iis_ctl2 = 32'h0000_0001

3. Multi-cycle format, master, 8 bits per-channel, pcm_oe=1,pcm_cyc=1, slot0 is occupied
   iis_clkd = 32'0000_000a
   iis_ctl0 = 32'h0000_80c1
   iis_ctl1 = 32'h0000_0f11
   iis_ctl2 = 32'h0000_0409

4. Muti-cycle format, master, 8 bits per-channel, pcm_cyc=2, slot0 and slot1 are occupied
   iis_clkd = 32'0000_000a
   iis_ctl0 = 32'h0000_80c1
   iis_ctl1 = 32'h0000_0f11
   iis_ctl2 = 32'h0000_0013

5. Long frame format, slave, 16 bits per-channel, enable clock count,
   iis_ctl0 = 32'h0000_80c9
   iis_ctl1 = 32'h0000_3f11
   iis_ctl2 = 32'h0000_0001

6. Short frame format , slave, 16 bits per-channel, enable clock count,
   iis_ctl0 = 32'h0000_81cd
   iis_ctl1 = 32'h0000_3a1
   iis_ctl2 = 32'h0000_0001

6.5 I2C Interface

6.5.1 Overview

I2C: Inter-Integrated Circuit

2 wire serial system is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices.

The interface defines 3 transmission speeds:

- normal: 100kbps
- fast: 400kbps
- high speed:3.5Mbps

SC6820 has 4 IIC controllers, IIC0&IIC1&IIC2&IIC3.

6.5.2 Features

I2C features list

- Software programmable clock frequency
- Software programmable acknowledge bit
- Interrupt driven data-transfers
- Start/Stop/Repeated Start/Acknowledge generation
- Supports Clock Stretching/Wait state generation
- Single Master Operation
- 8 word buffer mode support
- Only normal and fast modes are supported in this design

6.5.3 Signal Description

The 2 wire serial interface uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. Both lines must be pulled-up to VCC by external resistors. The tri-state buffers for the SCL and SDA lines have to be added at a higher hierarchical level.

Connections should be made according to the following figure:

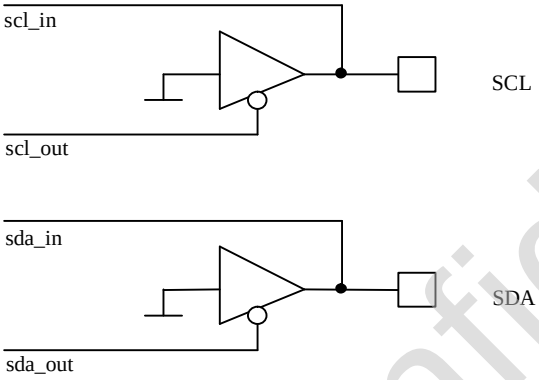


Figure 6-28 I2C PAD connection

6.5.4 Function Description

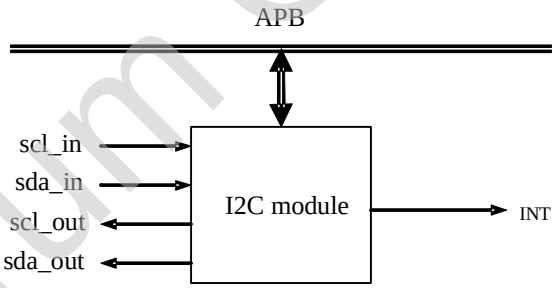


Figure 6-29 I2C system diagram

6.5.4.1 System Configuration

The 2 wire serial system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. The logic AND function is exercised on both lines with external pull-up resistors.

The 2 wire serial controller implemented here is a single master device; therefore it starts generating a clock as soon as it is enabled. The user should program this register to the desired value before starting any transfers.

Data is transmitted synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. There is an acknowledge bit following each transferred byte. Each bit is sampled during the high period of SCL; therefore the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP command).

6.5.4.2 Wire Serial Protocol

Normally, a standard communication consists of four parts:

- START signal generation
- Slave address transfer
- Data transfer
- STOP signal generation

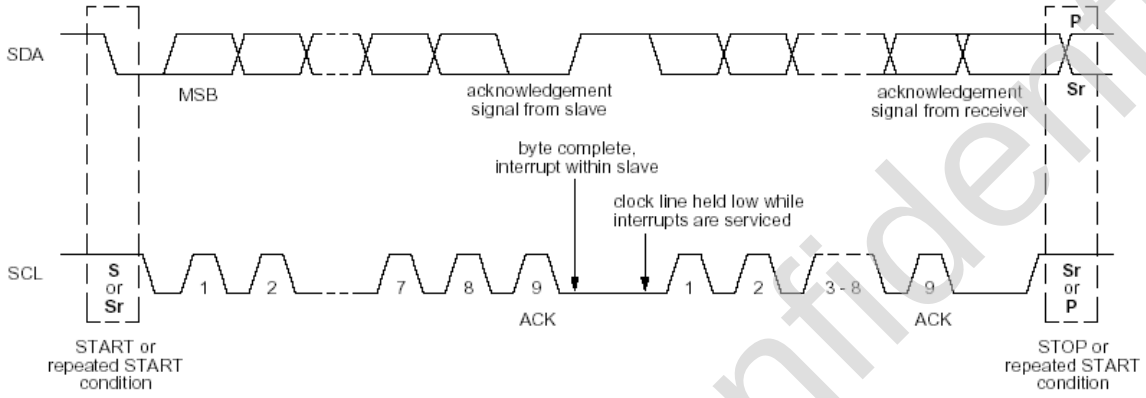


Figure 6-30 I2C system diagram

1. START signal

When the bus is free/idle, that is no master device is engaging the bus (both SCL and SDA lines are high), a master can initiate a transfer by sending a START signal. A START signal is defined as a high-to-low transition of SDA while SCL is high. The START signal denotes the beginning of a new data transfer.

A repeated START is a START signal without first generating a STOP signal. The master uses this method to communicate with another slave or the same slave in a different transfer direction (e.g. writing to device to reading from device) without releasing the bus.

The controller generates a START signal when the start bit in the 2ws_command Register is set and the read or write bits are set. Depending on the current status of the SCL line a START or Repeated START is generated.

2. Slave Address Transfer

The first byte of data transferred by the master immediately after the START signal is the slave address. This is a seven-bit calling address followed by a RW bit. The RW bit signals the slave data transfer direction. No two slaves in the system can have the same address. Only the slave with an address that matches the one transmitted by the master will respond by returning an acknowledge bit by pulling the SDA low at the 9th SCL clock cycle.

The controller treats a Slave Address Transfer as any other write action. Store the slave device's address in the 2ws_command register and set the write bit. The controller will then transfer the slave address on the bus.

3. Data Transfer

Once successful slave addressing is achieved, the data transfer can proceed on a byte-by-byte basis in the direction specified by the RW bit sent by the master. Each transferred byte is followed by an acknowledge bit on the 9th SCL clock cycle. If the slave signals a No Acknowledge (NACK), the master can generate a STOP signal to

abort the data transfer or generate a repeated START signal and start a new transfer cycle.

If the master, as the receiving device, does not acknowledge the slave, the slave releases the SDA line for the master to generate a STOP or repeated START signal.

For writing data to a slave, store the data to transmit in the 2ws_command register and set the write bit. For reading data from a slave, set the read bit. When the transfer is done, an interrupt is generated to MCU. The 2ws_command bit 8 to bit 15 contains valid data. The user may issue a new write or read command at this time.

3. STOP signal

The master can terminate the communication by generating a STOP signal. A STOP signal is defined as a low-to-high transition of SDA while SCL is at logical '1'.

6.5.4.3 Arbitration Procedure

Since the 2 wire serial controller supports single master configurations only, no Arbitration logic is added to the controller. Only clock synchronization is supported since slave devices can use this mechanism for clock stretching.

1. Clock Synchronization

Since the logical AND function is performed on the signals, a high to low transition on SCL or SDA affect all devices connected to the bus. The SCL clock signal can be synchronized between multiple masters using this feature. Each device starts counting its SCL low period when the current master drives SCL low. Once a device's clock has gone low, it holds the SCL line low until the clock high state is reached.

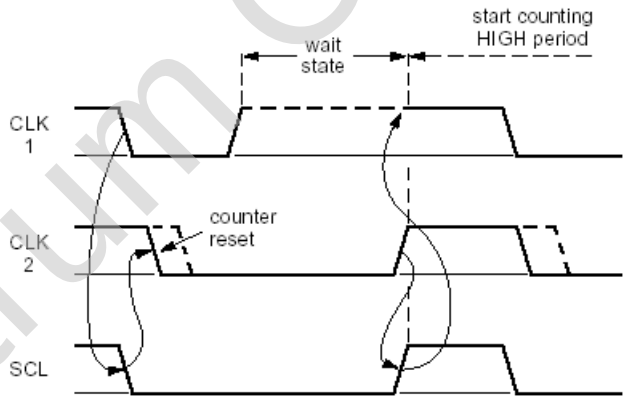


Figure 6-31 Clock synchronization during the arbitration procedure

2. Clock Stretching

Slave devices can use the clock synchronization mechanism to slow down the transfer bit rate. After the master has driven SCL low the slave can drive SCL low for the required period and then release it. If the slave's SCL low period is greater than the master's SCL low period, the resulting SCL bus signal low period is stretched, thus inserting wait-states.

6.5.5 Control Registers

6.5.5.1 Memory map

ARM base address: 0x8600_0000 IIC0

0x8600_1000 IIC1
0x8600_2000 IIC2
0x8600_2000 IIC3

Offset Address	Name	Description
0x0000	2WS_CONTROL	2 wire serial system control register
0x0004	2WS_COMMAND	2 wire serial system command register
0x0008	2WS_DIVIDOR0	2 wire serial system divider register0
0x000C	2WS_DIVIDOR1	2 wire serial system divider register1
0x0010	2WS_RST	2 wire serial system reset register
0x0014	2WS_CMD_BUF	2 wire serial system command buffer register

6.5.5.2 Register Descriptions

6.5.5.2.1 2WS_CONTROL

Description： 2 wire serial system control register

0x0000	2ws system control register (Reset 0x0000_0000)													2WS_CONTROL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			2ws_ cmdbuf_wptr			2ws_st_cmdbuf			2ws_cmd_exec	2ws_cmdbuf_en	2ws_en	2ws_ie	2ws_busy	2ws_ack	2ws_int
Type	RO			R/W			R/W			R/W	R/W	R/W	R/W	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:13]	RO	19'h0	Reserved
2ws_ cmdbuf_wptr	[12:10]	R/W	3'h0	2ws command buffer write pointer
2ws_st_cmdbuf	[9:7]	R/W	3'h0	The state of 2ws command buffer state machine.
2ws_cmd_exec	[6]	R/W	1'h0	Start to exec the command in the command buffer
2ws_cmdbuf_en	[5]	R/W	1'h0	Enable the command buffer mode
2ws_en	[4]	R/W	1'h0	2ws module enable
2ws_ie	[3]	R/W	1'h0	2ws interrupt enable
2ws_busy	[2]	RO	1'h0	2ws data line value
2ws_ack	[1]	RO	1'h0	2ws received ack value

2ws_int	[0]	RO	1'h0	2ws interrupt

6.5.5.2.2 2WS_COMMAND

Description： 2 wire serial system command register

0x0004	2ws system command register (Reset 0x0000_0000)												2WS_ COMMAND			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	2ws_data								2ws_busy	2ws_ack	cmd_start	cmd_stop	cmd_read	cmd_write	tx_ack	int_ack
Type	R/W								RO	RO	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
2ws_data	[15:8]	R/W	8'h0	2ws data received or data need to be transmitted
2ws_busy	[7]	RO	1'h1	2ws busy in exec commands
2ws_ack	[6]	RO	1'h0	2ws received ack value
cmd_start	[5]	R/W	1'h0	2ws start command
cmd_stop	[4]	R/W	1'h0	2ws stop command
cmd_read	[3]	R/W	1'h0	2ws read command
cmd_write	[2]	R/W	1'h0	2ws write command
tx_ack	[1]	R/W	1'h0	2ws transmit ack that need to be send
int_ack	[0]	R/W	1'h0	2ws interrupt clear bit

6.5.5.2.3 2WS_DIVIDOR0

Description： 2 wire serial system dividor register0

0x0008			2 wire serial system dividor register0 (Reset 0x0000_0040)													2WS_DIVIDOR0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	2ws_dividor0															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
2ws_dividor0	[15:0]	R/W	16'h0	2ws clock dividor [15:0], default is 0x40

6.5.5.2.4 2WS_DIVIDOR1

Description： 2 wire serial system dividor register1

0x000C			2 wire serial system dividor register1 (Reset 0x0000_0000)													2WS_DIVIDOR1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	2ws_dividor1															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
2ws_dividor1	[15:0]	R/W	16'h0	2ws clock dividor [31:16], default is 0x0

Note:

Change the value of prescale register only when the w2s_control[4] bit is cleared.

Due to the structure of the I2C interface, the controller uses "4*SCL" clock internally.

Example: PCLK = 26MHz, desired SCL = 100khz,

prescale = 26MHz/(4*100khz) – 1 = 64 (dec) = 40 (hex)

Reset value : 0x40

6.5.5.2.5 2WS_RST

Description： 2 wire serial system reset register

0x0010			2ws system reset register (Reset 0x0000_0000)													2WS_RST
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															2ws_rst
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:1]	RO	31'h0	Reserved
2ws_rst	[0]	R/W	1'h0	Write with bit 0 set to 1 will reset the 2ws module.

6.5.5.2.6 2WS_CMD_BUF

Description： 2ws system command buffer register

0x0014			2ws system command buffer register (Reset 0x0000_0000)													2WS_CMD_BUF
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	2ws_cmd_buf															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	31'h0	Reserved
2ws_cmd_buf	[15:0]	R/W	16'h0	Write command to this register will save the command to the command buffer. Read from this register after the commands are all finished will return the results of the corresponding commands. The format of the command and the return result is the same as i2c_command register.

6.5.6 Application Notes

List all data formats. Detail the programming flow for the module.

- Standard mode; a single master operation; a master-transmitter addressing a slave receiver with a 7-bit address; single common mode

```
w2s_rst          = 0x0000;          //
w2s_dividor0     = 0x0040;          //
w2s_dividor1     = 0x0000;          //
w2s_control          = 0x0018;          // 2ws_en = 1; 2ws_ie = 1
w2s_command = 0x9C25;          // 1001110        0      0010 0101
                                // ADDRESS    W         S         W Iack
w2s_command = 0xFE05;          // 11111110      0000 0101
                                //    DATA
w2s_command = 0xFE15;          // 11111110      0001 0101
                                // DATA                      P
```

- Fast mode; a single master operation; combined format; 7-bit address; common buffer mode: a burst of 8 commands is written to the buffer

```
w2s_rst          = 0x0000;          //
w2s_dividor0     = 0x0040;          //
w2s_dividor1     = 0x0000;          //
w2s_control          = 0x0038;          // 2ws_cmdbuf_en=1; 2ws_en=1; 2ws_ie=1
w2s_command = 0x9C25;          // 1001110        0      0010 0101
                                // ADDRESS    W         S         W Iack
w2s_command = 0x2005;          //
w2s_command = 0x9D15;          //
w2s_command = 0x001B;          //
w2s_command = 0x9C25;          //
w2s_command = 0x2005;          //
w2s_command = 0x9D15;          //
w2s_command = 0x001B;          //
w2s_command = 0x9C25;          //
w2s_command = 0x2005;          //
w2s_command = 0x9D15;          //
w2s_command = 0x001B;          //
w2s_command = 0x9C25;          //
w2s_command = 0x2005;          //
w2s_command = 0x9D15;          //
w2s_command = 0x001B;          //
```

6.6 Keypad Interface

6.6.1 Overview

Here Keypad means “keypad controller” which is one APB device in ARM system. The keypad controller scans the external “key matrix” whose maximum size is 8 rows x 8 columns. It scans the “key matrix” row by row and checks the keys of the row one by one. There are at most four keys “pressed”. “released” status can be detected in the same time, which is the so called “multi-key detection”. On the other hand, one pressed key can generate multi interrupts periodically to software and this mode is named the “long key” mode.

For the reason that the external “key matrix” is pure mechanical, if the geometric shape constituted by any three “pressed keys” is a “right-angled triangle “, the keypad controller will detect another “inductive pressed” key. For example, if key 1 (x1, y1),

key 2 (x2, y2), key 3 (x1, y2) are pressed then the key 4 (x2, y1) will also be detected as the “pressed” key. The keypad controller will check the geometric shape constituted by the three “pressed keys” and if above condition is detected one “error” status will be reported to software, which should discard current error multi-keys combination.

Finally, low power of the keypad controller is very important. If the controller finds that none key is pressed in the specific time, the clock of most logic inside the controller will be disabled to save power and controller goes into the sleep mode. In the sleep mode controller will be sensitive to any change of the “key matrix”. In other words, any key’s press or release will wakes up the controller to scan the “key matrix”.

6.6.2 Features

- Support maximum 8 row x 8 column key matrix and size is programmable
- Support at most four keys detection under “multi-key” mode
- Support “long key” or “single key” mode for any pressed key
- Support “right-angled triangle” geometric shape detection for the pressed keys
- Support sleep mode to save power
- Support programmable “de-bounce” time for key’s press and release
- Support programmable I/O polarity
- Support programmable scan speed

6.6.3 Signal Description

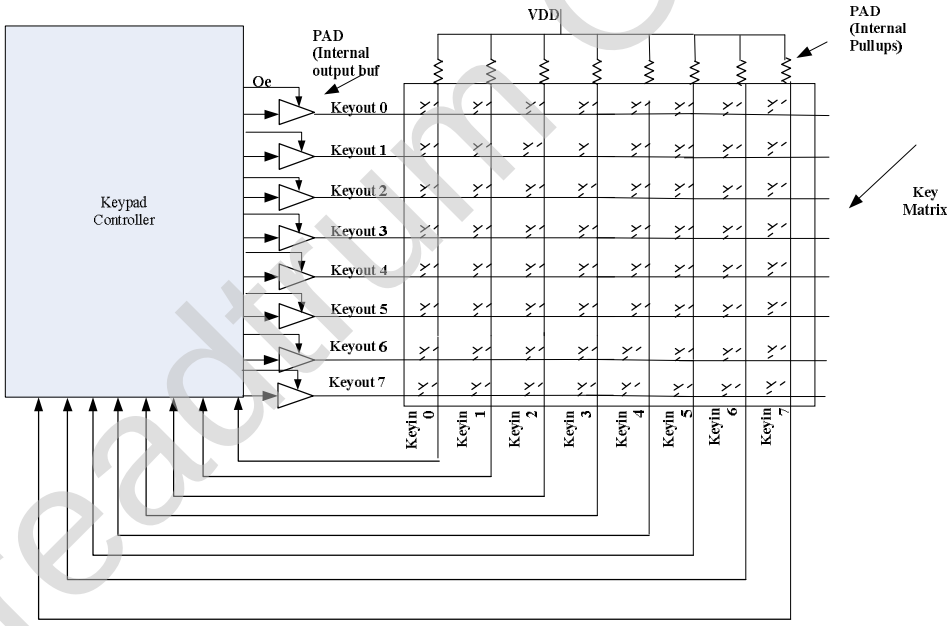


Figure 6-32 Keypad connection with external key matrix

The above diagram shows how to interface the keypad controller and the key matrix with pad internal pull-up resistance when the key matrix is 8 rows x 8 columns. For key matrix, the input is keyout 0 ~ keyout 7 and the output is the keyin 0 ~ keyin 7. Every keyout signal can be enabled or disabled. The keyout signal will be forced to be “low level” when it is enabled and only one keyout should be enabled at any time during scanning.

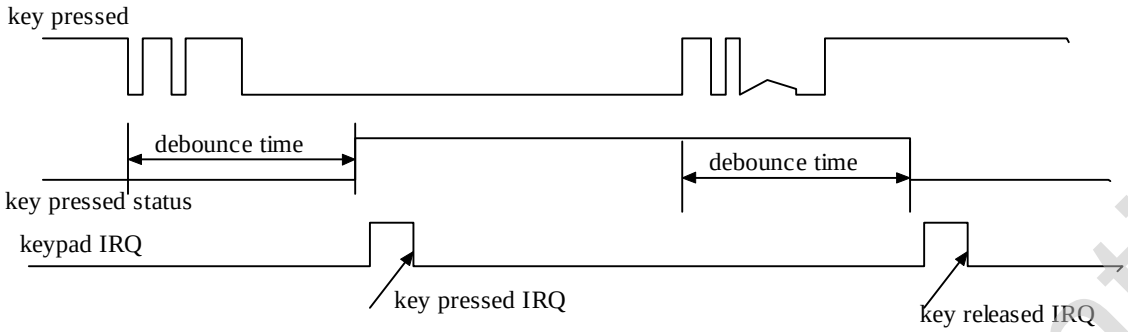


Figure 6-33 Single-key mode

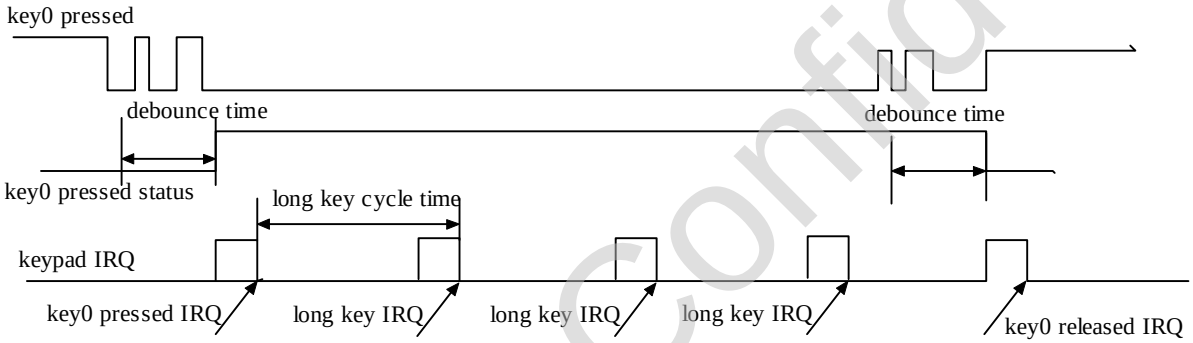


Figure 6-34 Long-key mode

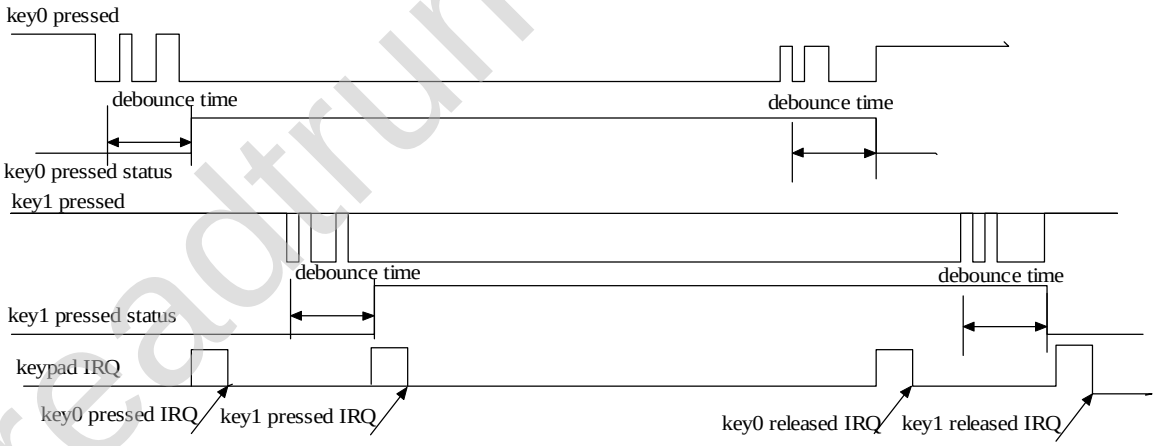


Figure 6-35 Multi-key mode

6.6.4 Function Description

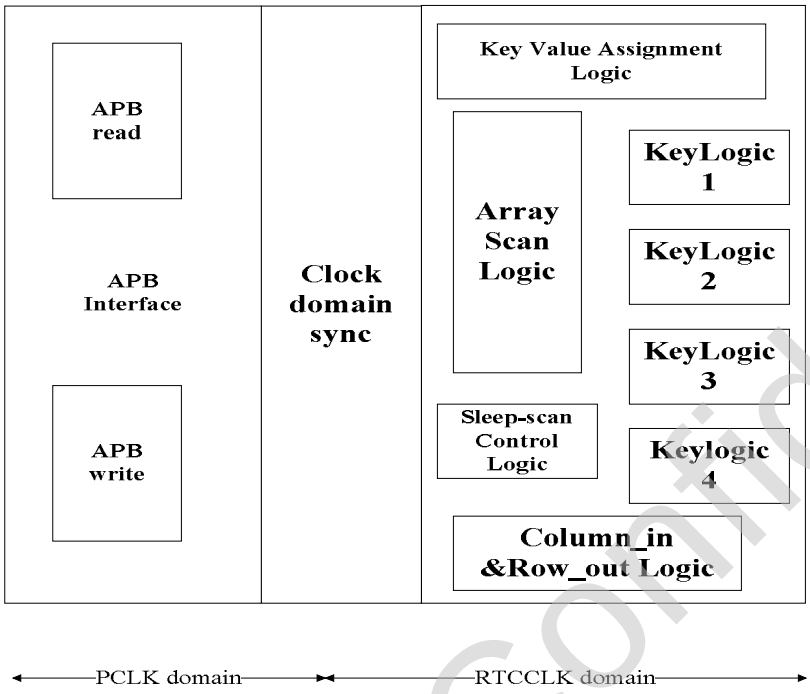


Figure 6-36 Keypad controller diagram

6.6.5 Control Registers

6.6.5.1 Memory map

Physical base address: 0x8700_0000

Offset Address / Name	Description
0x0000 KPD_CTRL	Keypad global control register
0x0004 KPD_INT_EN	Keypad INT enable register
0x0008 KPD_INT_RAW_STATUS	Keypad INT raw status register
0x000C KPD_INT_MASK_STATUS	Keypad INT status register
0x0010 KPD_INT_CLR	Keypad INT clear register
0x0014	Reserved
0x0018 KPD_POLARITY	Keypad I/O polarity control register
0x001C KPD_DEBOUNCE_CNT	Keypad de-bouncing time configuration register
0x0020 KPD_LONG_KEY_CNT	Keypad long-key time configuration register

Offset Address	Name	Description
0x0024	KPD_SLEEP_CNT	Keypad sleep wait time configuration register
0x0028	KPD_CLK_DIVIDE_CNT	Keypad scan clock division coefficient register
0x002C	KPD_ KEY_STATUS	Keypad key status register
0x0030	KPD_SLEEP_STATUS	Keypad sleep status register
0x0034	KPD_DEBUG_STATUS1	Keypad debug status register1
0x0038	KPD_DEBUG_STATUS2	Keypad debug status register2

6.6.5.2 Register Descriptions

6.6.5.2.1 KPD_CTRL

0x0000			Keypad control register													KPD_CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reerved							KPD_COL7_EN	KPD_COL6_EN	KPD_COL5_EN	KPD_COL4_EN	KPD_COL3_EN	KPD_ROW7_EN	KPD_ROW6_EN	KPD_ROW5_EN	KPD_ROW4_EN
Type	RO							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved													KPD_LONG_KEY_EN	KPD_SLEEP_EN	KPD_EN
Type	RO													R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:25]	R	0	Reserved
KPD_COL7_EN	[24]	R/W	0	Enable bit for column 7
KPD_COL6_EN	[23]	R/W	0	Enable bit for column 6
KPD_COL5_EN	[22]	R/W	0	Enable bit for column 5
KPD_COL4_EN	[21]	R/W	0	Enable bit for column 4

KPD_COL3_EN	[20]	R/W	0	Enable bit for column 3
KPD_ROW7_EN	[19]	R/W	0	Enable bit for row 7
KPD_ROW6_EN	[18]	R/W	0	Enable bit for row 6
KPD_ROW5_EN	[17]	R/W	0	Enable bit for row 5
KPD_ROW4_EN	[16]	R/W	0	Enable bit for row 4
	[15:3]	R	0	Reserved
KPD_LONG_KEY_EN	[2]	R/W	0	When set to 1, keypad can enter long key mode if a key is pressed for a long time
KPD_SLEEP_EN	[1]	R/W	0	When set to 1, the keypad can enter sleep mode if there is no key press for a certain time. The scan will stop until there has a press pulse.
KPD_EN	[0]	R/W	0	Keypad global enable signal. Set to1 will make whole keypad work by generate the clk_en signal to do scan and other process. Notice: port signal kpd_eb directly generates RTCLK clock gating.

6.6.5.2.2 KPD_INT_EN

0x0004			Keypad interrupt enable												KPD_INT_EN	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					KPD4_LONG_KEY_INT_EN	KPD3_LONG_KEY_INT_EN	KPD2_LONG_KEY_INT_EN	KPD1_LONG_KEY_INT_EN	KPD4_RELEA_INT_EN	KPD3_RELEA_INT_EN	KPD2_RELEA_INT_EN	KPD1_RELEA_INT_EN	KPD4_PRESS_INT_EN	KPD3_PRESS_INT_EN	KPD2_PRESS_INT_EN	KPD1_PRESS_INT_EN
Type	RO				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:12]	R	0	Reserved
KPD4_LONG_KEY_INT_EN	[11]	R/W	0	Keypad long-key interrupt enable for No.4
KPD3_LONG_KEY_INT_EN	[10]	R/W	0	Keypad long-key interrupt enable for No.3
KPD2_LONG_KEY_INT_EN	[9]	R/W	0	Keypad long-key interrupt enable for No.2
KPD1_LONG_KEY_INT_EN	[8]	R/W	0	Keypad long-key interrupt enable for No.1
KPD4_RELEA_INT_EN	[7]	R/W	0	Keypad release interrupt enable for No.4
KPD3_RELEA_INT_EN	[6]	R/W	0	Keypad release interrupt enable for No.3
KPD2_RELEA_INT_EN	[5]	R/W	0	Keypad release interrupt enable for No.2
KPD1_RELEA_INT_EN	[4]	R/W	0	Keypad release interrupt enable for No.1
KPD4_PRESS_INT_EN	[3]	R/W	0	Keypad press interrupt enable for No.4
KPD3_PRESS_INT_EN	[2]	R/W	0	Keypad press interrupt enable for No.3
KPD2_PRESS_INT_EN	[1]	R/W	0	Keypad press interrupt enable for No.2
KPD1_PRESS_INT_EN	[0]	R/W	0	Keypad press interrupt enable for No.1

6.6.5.2.3 KPD_INT_RAW_STATUS

0x0008			Keypad interrupt raw status											KPD_INT_RAW_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					KPD4_LONG_KEY_INT	KPD3_LONG_KEY_INT	KPD2_LONG_KEY_INT	KPD1_LONG_KEY_INT	KPD4_RELEA_INT	KPD3_RELEA_INT	KPD2_RELEA_INT	KPD1_RELEA_INT	KPD4_PRESS_IN	KPD3_PRESS_INT	KPD2_PRESS_INT	KPD1_PRESS_INT
Type	RO				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:12]	R	0	Reserved
KPD4_LONG_KEY_INT	[11]	R/W	0	Keypad long-key interrupt for No.4
KPD3_LONG_KEY_INT	[10]	R/W	0	Keypad long-key interrupt for No.3
KPD2_LONG_KEY_INT	[9]	R/W	0	Keypad long-key interrupt for No.2
KPD1_LONG_KEY_INT	[8]	R/W	0	Keypad long-key interrupt for No.1
KPD4_RELEA_INT	[7]	R/W	0	Keypad release interrupt for No.4
KPD3_RELEA_INT	[6]	R/W	0	Keypad release interrupt for No.3
KPD2_RELEA_INT	[5]	R/W	0	Keypad release interrupt for No.2
KPD1_RELEA_INT_EN	[4]	R/W	0	Keypad release interrupt for No.1
KPD4_PRESS_INT	[3]	R/W	0	Keypad press interrupt for No.4

KPD3_PRESS_INT	[2]	R/W	0	Keypad press interrupt for No.3
KPD2_PRESS_INT	[1]	R/W	0	Keypad press interrupt for No.2
KPD1_PRESS_INT	[0]	R/W	0	Keypad press interrupt for No.1

6.6.5.2.4 KPD_INT_MASK_STATUS

0x000C			Keypad interrupt mask										KPD_INT_MASK_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					KPD4_MASK_LONG_KEY_INT	KPD3_MASK_LONG_KEY_INT	KPD2_MASK_LONG_KEY_INT	KPD1_MASK_LONG_KEY_INT	KPD4_MASK_RELEA_INT	KPD3_MASK_RELEA_INT	KPD2_MASK_RELEA_INT	KPD1_MASK_RELEA_INT	KPD4_MASK_PRESS_IN	KPD3_MASK_PRESS_INT	KPD2_MASK_PRESS_INT	KPD1_MASK_PRESS_INT
Type	RO				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:12]	R	0	Reserved
KPD4_MASK_LONG_KEY_INT	[11]	R/W	0	No.4 keypad long-key interrupt masked by long-key interrupt enable.
KPD3_MASK_LONG_KEY_INT	[10]	R/W	0	No.3 keypad long-key interrupt masked by long-key interrupt enable.
KPD2_MASK_LONG_KEY_INT	[9]	R/W	0	No.2 keypad long-key interrupt masked by long-key interrupt enable.
KPD1_MASK_LONG_	[8]	R/W	0	No.1 keypad long-key

KEY_INT				interrupt masked by long-key interrupt enable.
KPD4_MASK_RELEA_INT	[7]	R/W	0	No.4 keypad release interrupt masked by release interrupt enable.
KPD3_MASK_RELEA_INT	[6]	R/W	0	No.3 keypad release interrupt masked by release interrupt enable.
KPD2_MASK_RELEA_INT	[5]	R/W	0	No.2 keypad release interrupt masked by release interrupt enable.
KPD1_MASK_RELEA_INT_EN	[4]	R/W	0	No.1 keypad release interrupt masked by release interrupt enable.
KPD4_MASK_PRESS_INT	[3]	R/W	0	No.4 keypad press interrupt masked by press interrupt enable.
KPD3_MASK_PRESS_INT	[2]	R/W	0	No.3 keypad press interrupt masked by press interrupt enable.
KPD2_MASK_PRESS_INT	[1]	R/W	0	No.2 keypad press interrupt masked by press interrupt enable.
KPD1_MASK_PRESS_INT	[0]	R/W	0	No.1 keypad press interrupt masked by press interrupt enable.

6.6.5.2.5 KPD_INT_CLR

0x0010			Keypad interrupt clear													KPD_INT_CLR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					KPD4_LONG_KEY_INT_CLR	KPD3_LONG_KEY_INT_CLR	KPD2_LONG_KEY_INT_CLR	KPD1_LONG_KEY_INT_CLR	KPD4_RELEA_INT_CLR	KPD3_RELEA_INT_CLR	KPD2_RELEA_INT_CLR	KPD1_RELEA_INT_CLR	KPD4_PRESS_INT_CLR	KPD3_PRESS_INT_CLR	KPD2_PRESS_INT_CLR	KPD1_PRESS_INT_CLR
Type	RO				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:12]	R	0	Reserved
KPD4_LONG_KEY_INT_CLR	[11]	R/W	0	Write 1 to this bit will clear the No.4 key long-key interrupt raw status.
KPD3_LONG_KEY_INT_CLR	[10]	R/W	0	Write 1 to this bit will clear the No.3 key long-key interrupt raw status.
KPD2_LONG_KEY_INT_CLR	[9]	R/W	0	Write 1 to this bit will clear the No.2 key long-key interrupt raw status.
KPD1_LONG_KEY_INT_CLR	[8]	R/W	0	Write 1 to this bit will clear the No.1 key long-key interrupt raw status.
KPD4_RELEA_INT_CLR	[7]	R/W	0	Write 1 to this bit will clear the No.4 key release interrupt raw status.
KPD3_RELEA_INT_CLR	[6]	R/W	0	Write 1 to this bit will clear the No.3 key release interrupt raw status.
KPD2_RELEA_INT_CLR	[5]	R/W	0	Write 1 to this bit will clear the No.2 key release interrupt raw status.
KPD1_RELEA_	[4]	R/W	0	Write 1 to this bit will clear the No.1 key release interrupt raw

INT_CLR				status.
KPD4_PRESS_ INT_CLR	[3]	R/W	0	Write 1 to this bit will clear the No.4 key press interrupt raw status.
KPD3_PRESS_ INT_CLR	[2]	R/W	0	Write 1 to this bit will clear the No.3 key press interrupt raw status.
KPD2_PRESS_ INT_CLR	[1]	R/W	0	Write 1 to this bit will clear the No.2 key press interrupt raw status.
KPD1_PRESS_ INT_CLR	[0]	R/W	0	Write 1 to this bit will clear the No.1 key press interrupt raw status.

6.6.5.2.6 KPD_POLARITY

0x0018			Register description (Reset value)												KPD_POLARITY	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KPD_COLUMN_POLARITY								KPD_ROW_POLARITY							
Type																
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

~~Field Name~~	Bit	R/W	Reset Value	Description
	[31:16]	R	0	Reserved
KPD_COLUMN_ POLARITY	[15:8]	R/W	8'hFF	Column input xor with this value to generate the internal column input. This register is used to control the column input polarity.
KPD_ROW_ POLARITY	[7:0]	R/W	8'hFF	Internal row output xor with this value to generate row output. This register is used to control the row output polarity.

6.6.5.2.7 KPD_DEBOUNCE_CNT

0x001C			Key press and release de-bounce time control register										KPD_DEBOUNCE_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KPD_DEBOUNCE_CNT															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	0	Reserved
KPD_DEBOUNCE_CNT	[15:0]	R/W	16'h0080	Counter for de-bounce time It is the function of scan array size and clock divider number. Default value: 165ms when clk_divider is 0 and 42 keys are enable(7*6 array) The calculation method is: y(ms)= (x +1) * array_size /(32.768/(clk_div_num+1))

6.6.5.2.8 KPD_LONG_KEY_CNT

0x0020			Long key time control register										KPD_LONG_KEY_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KPD_LONG_KEY_CNT															
Type	R/W															
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	0	Reserved

KPD_LONG_KEY_CNT	[15:0]	R/W	16'h0400	Counter for long key time It is the function of scan array size and clock divider number. Default value: 1.34s when clk_divider is 0 and 42 keys are enable(7*6 array) The calculation method is: y(ms)= (x +1) * array_size /(32.768/(clk_div_num+1))

6.6.5.2.9 KPD_SLEEP_CNT

0x0024			Counter for enter sleep mode enable(from no key press)										KPD_SLEEP_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved									KPD_SLEEP_CNT						
Type	RO									R/W						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KPD_SLEEP_CNT															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:23]	R	0	Reserved
KPD_SLEEP_CNT	[22:0]	R/W	23'h080000	Counter for enter sleep mode enable(from no key press) It is not the function of scan number and clock divider number. Default value:16.384s Y(ms)=(x+1)/32.768

6.6.5.2.10 KPD_CLK_DIVIDE_CNT

0x0028			Keypad scan clock divider coefficients configuration register.										KPD_CLK_DIVIDE_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								KPD_CLK_DIVIDE_CNT							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:8]	R	0	Reserved
KPD_CLK_DIVIDE_CNT	[7:0]	R/W	0	Clk_divider[7:0], divide RTCLK (32.768 kHz) used for keypad. Can slow down keypad's work speed. The RTCLK will be divided (cnt + 1) times

6.6.5.2.11 KPD_KEY_STATUS

0x002C			Keypad keys status register.										KPD_KEY_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	KPD4_KEY_STS	KPD4_ROW_CNT			Reserved	KPD4_COL_CNT			KPD3_KEY_STS	KPD3_ROW_CNT			Reserved	KPD3_COL_CNT		
Type	RO	RO			RO	RO			RO	RO			RO	RO		
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KPD2_KEY_STS	KPD2_ROW_CNT			Reserved	KPD2_COL_CNT			KPD1_KEY_STS	KPD1_ROW_CNT			KPD_FOUR_KEY_CROSS	KPD1_COL_CNT		
Type	RO	RO			RO	RO			RO	RO			RO	RO		
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1

Field Name	Bit	R/W	Reset Value	Description
KPD4_KEY_STS	[31]	R	0	No.4 key is pressed status
KPD4_ROW_CNT	[30:28]	R	3'b111	No.4 key row coordinate
	[27]	R		Reserved
KPD4_COL_CNT	[26:24]	R	3'b111	No.4 key column coordinate
KPD3_KEY_STS	[23]	R	0	No.3 key is pressed status.
KPD3_ROW_CNT	[22:20]	R	3'b111	No.3 key row coordinate
	[19]	R	0	Reserved
KPD3_COL_CNT	[18:16]	R	3'b111	No.3 key column coordinate
KPD2_KEY_STS	[15]	R	0	No.2 key is pressed status.
KPD2_ROW_CNT	[14:12]	R	3'b111	No.2 key row coordinate
	[11]	R	0	Reserved
KPD2_COL_CNT	[10:8]	R	3'b111	No.2 key column coordinate
KPD1_KEY_STS	[7]	R	0	No.1 key is pressed status.
KPD1_ROW_CNT	[6:4]	R	3'b111	No.1 key row coordinate
KPD_FOUR_KEY_CROSS	[3]	R	0	Set to 1 indicates that when 4 keys are all pressed, these keys can be constructed into right-angled coordinate
KPD1_COL_CNT	[2:0]	R	3'b111	No.1 key column coordinate

6.6.5.2.12 KPD_SLEEP_STATUS

0x0030			Keypad sleep status register										KPD_SLEEP_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															KPD_SLEEP_STS
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:1]	R	0	Reserved
KPD_SLEEP_STS	[0]	R	0	Set to 1 shows keypad is in sleep state, 0 shows in common scan state

6.6.5.2.13 KPD_DEBUG_STATUS1

0x0034			Keypad debug status1 register										KPD_DEBUG_STATUS1			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved					KPD_ROW_CNT			Reserved	KPD_COL_CNT			Reserved			KPD_KEY_VALUE
Type	RO					RO			RO	RO			RO			RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description

	[31:11]	R	0	Reserved
KPD_ROW_CNT	[10:8]	R	3'd0	Current scanning key's column coordinate
	[7]	R	0	Reserved
KPD_COL_CNT	[6:4]	R	3'd0	Current scanning key's row coordinate
	[3:1]	R	0	Reserved
KPD_KEY_VALUE	[0]	R	0	Keypad scanning flag, active high.

6.6.5.2.14 KPD_DEBUG_STATUS2

0x0038			Keypad debug status2 register											KPD_DEBUG_STATUS2			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name				KPD_KEY4_STATE								KPD_KEY3_STATE				
Type				RO								RO				
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				KPD_KEY2_STATE								KPD_KEY1_STATE				
Type				RO								RO				
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Field Name	Bit	R/W	Reset Value	Description
	[31:29]	R	0	Reserved
Kpd_key4_ state	[28:24]	R	5'b00001	Key_state_4 FSM's state The same as above
	[23:21]	R	0	Reserved
Kpd_key3_ state	[20:16]	R	5'b00001	Key_state_3 FSM's state The same as above
	[15:13]	R	0	Reserved
Kpd_key2_ state	[12:8]	R	5'b00001	Key_state_2 FSM's state The same as above
	[7:5]	R	0	Reserved
Kpd_key1_	[4:0]	R	5'b00001	Key_state_1 FSM's state

state				00001: release state 00010: press de-bounce state 00100: press state 01000: release de-bounce state 10000: release busy state

6.6.6 Application Notes

6.6.7 Clock enable

There are two clock inputs for keypad controller: clk_rtc and APB PCLK. Before enable keypad controller to work these two clocks should be enabled. Please refer to the 0x8B00_0008 register (GEN0 in APB global register)

[26]	RTC_KPD_EB	Clock rtc enable for keypad 0: Clock rtc will be off for keypad use. 1: Clock rtc will be on for keypad use.
[8]	KPD_EB	Keypad access enable 0: The peripheral clock (PCLK) of keypad controller will be off so its control registers cannot be accessed by MCU. 1: MCU can read or write keypad control registers.

6.6.8 KPD configuration

Please assure the right “keypad matrix size”, “row in/out polarity”, “key de-bounce time”, and “int enables”.

Also set the keypad controller works under the “sleep mode” by enable the “KPD_CTRL” register bit[0] can save power.

6.7 Pulse Width Modulation(PWM)

6.7.1 Overview

SC6820 provides up to 4 PWM outputs that can be used to control a ringer or buzzer or LCD lights. Each PWM can output 0%~100% duration waves for kinds of applications.

6.7.2 Features

- Support up to 4 PWM outputs;
- Support clock pre-scaling, from 1 to 256;
- Support configurable duty ratio, it can cover 0%~100%;

6.7.3 Signal Description

SC6820 has 4 PWM outputs, they are listed in Table xx.

Table xx PWM signal list

Signal Name	Direction	Width	Description
RFCTL[3]	O	1	PWM_A, when pin function is 1.
RFCTL[4]	O	1	PWM_B, when pin function is 1.
RFCTL[6]	O	1	PWM_C, when pin function is 1.
RFCTL[9]	O	1	PWM_D, when pin function is 1.

6.7.4 Function Description

A PWM functional block diagram is shown in the following diagram.

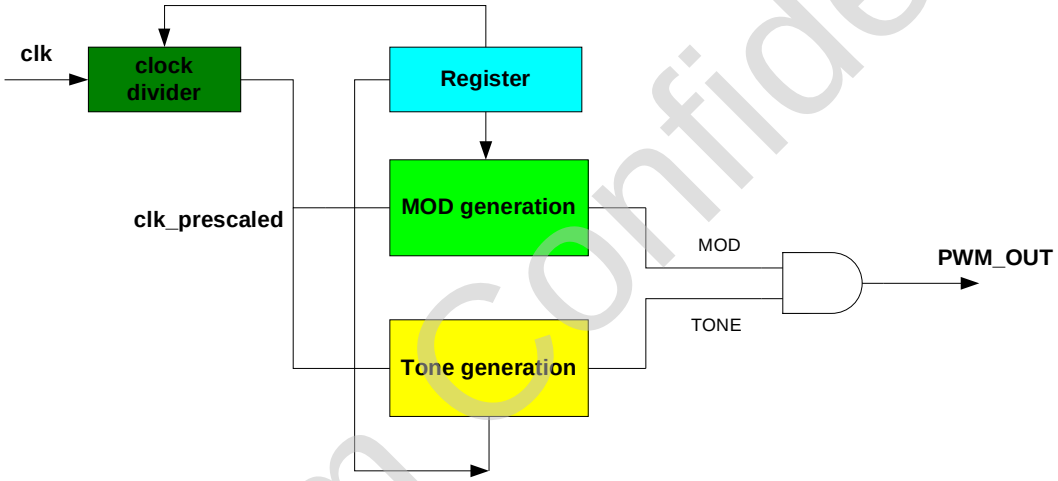


Figure 6-37 PWM Block Diagram

A PWM timing diagram is shown below.

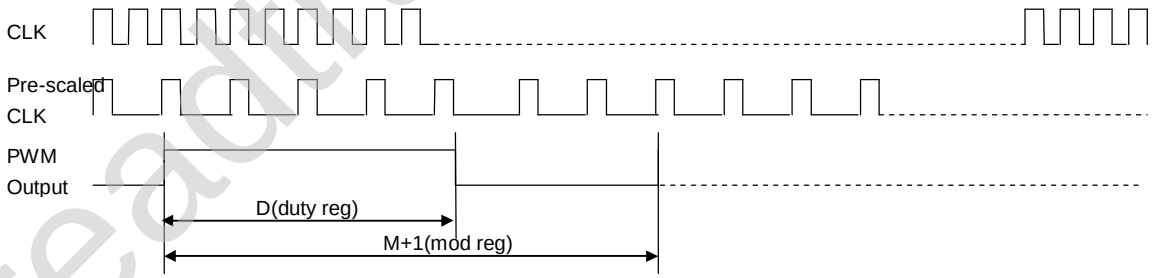


Figure 6-38 PWM Timing Diagram

If pre-scale register is P, and mod counter register is M, and duty cycle register is D, then output period T_O is T_{CLK} * (P+1) * (M+1), and active output period T_{ACT} is T_{CLK} * (P+1) * D, and duty ratio is D/(M+1).

6.7.5 Control Registers

6.7.5.1 Memory map

ARM base address: 0x8800_0000

Offset Address	Name	Description
0x0000	PWM0_PRESCALE	PWM0 prescale
0x0004	PWM0_CNT	PWM0 counter
0x0008	PWM0_DIV	PWM0 tone divider
0x000C	PWM0_PAT_LOW	PWM0 pattern low bits
0x0010	PWM0_PAT_HIGH	PWM0 pattern high bits
0x0020	PWM1_PRESCALE	PWM1 prescale
0x0024	PWM1_CNT	PWM1 counter
0x0028	PWM1_DIV	PWM1 tone divider
0x002C	PWM1_PAT_LOW	PWM1 pattern low bits
0x0030	PWM1_PAT_HIGH	PWM1 pattern high bits
0x0040	PWM2_PRESCALE	PWM2 prescale
0x0044	PWM2_CNT	PWM2 counter
0x0048	PWM2_DIV	PWM2 tone divider
0x004C	PWM2_PAT_LOW	PWM2 pattern low bits
0x0050	PWM2_PAT_HIGH	PWM2 pattern high bits
0x0060	PWM3_PRESCALE	PWM3 prescale
0x0064	PWM3_CNT	PWM3 counter
0x0068	PWM3_DIV	PWM3 tone divider
0x006C	PWM3_PAT_LOW	PWM3 pattern low bits
0x0070	PWM3_PAT_HIGH	PWM3 pattern high bits

6.7.5.2 Register Descriptions

6.7.5.2.1 PWMx_PRESCALE

Description: PWM prescale coefficient for work clock.

0x0000	PWM0 prescale coefficient (reset 0x0)	PWM0_PRESCALE
0x0020	PWM1 prescale coefficient (reset 0x0)	PWM1_PRESCALE
0x0040	PWM2 prescale coefficient (reset 0x0)	PWM2_PRESCALE
0x0060	PWM3 prescale coefficient (reset 0x0)	PWM3_PRESCALE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved							PWMx_EN	PWMx_PRESCALE							
Type	RO							R/W	R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:9]	RO	23'h0	Reserved
PWMx_EN	[8]	R/W	1'h0	PWMx enable 0: disable; 1: enable.
PWMx_PRESCALE	[7:0]	R/W	8'h0	PWMx prescale coefficient.

6.7.5.2.2 PWMx_CNT

Description: PWM counter.

0x0004	PWM0 counter (reset 0x0)	PWM0_CNT
0x0024	PWM1 counter (reset 0x0)	PWM1_CNT
0x0044	PWM2 counter (reset 0x0)	PWM2_CNT
0x0064	PWM3 counter (reset 0x0)	PWM3_CNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PWMx_DUTY								PWMx_MOD							
Type	R/W								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved

PWMx_DUTY	[15:8]	R/W	8'h0	PWMx duty counter.
PWMx_MOD	[7:0]	R/W	8'h0	PWMx mod counter.

6.7.5.2.3 PWMx_DIV

Description: PWM tone divider.

0x0008			**PWM0 tone divider (reset 0x0)**													**PWM0_DIV**
0x0028			**PWM1 tone divider (reset 0x0)**													**PWM1_DIV**
0x0048			**PWM2 tone divider (reset 0x0)**													**PWM2_DIV**
0x0068			**PWM3 tone divider (reset 0x0)**													**PWM3_DIV**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PWMx_DIV															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
PWMx_DIV	[15:0]	R/W	16'h0	PWMx tone divider.

6.7.5.2.4 PWMx_PAT_LOW

Description: PWM pattern low part.

0x000c			**PWM0 pattern low part (reset 0x0)**													**PWM0_PAT_LOW**
0x002c			**PWM1 pattern low part (reset 0x0)**													**PWM1_PAT_LOW**
0x004c			**PWM2 pattern low part (reset 0x0)**													**PWM2_PAT_LOW**
0x006c			**PWM3 pattern low part (reset 0x0)**													**PWM3_PAT_LOW**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PWMx_PAT_LOW															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

			Value	
	[31:16]	RO	16'h0	Reserved
PWMx_PAT_LOW	[15:0]	R/W	16'h0	PWMx pattern low part.

6.7.5.2.5 PWMx_PAT_HIGH

Description: PWM pattern high part.

0x0010	PWM0 pattern high part (reset 0x0)	PWM0_PAT_LOW
0x0030	PWM1 pattern high part (reset 0x0)	PWM1_PAT_HIGH
0x0050	PWM2 pattern high part (reset 0x0)	PWM2_PAT_HIGH
0x0070	PWM3 pattern high part (reset 0x0)	PWM3_PAT_HIGH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PWMx_PAT_HIGH															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
PWMx_PAT_HIGH	[15:0]	R/W	16'h0	PWMx pattern high part.

6.7.6 Application Notes

- When software uses PWM, it should set PWM global enable control register first, which is bit[24:21] of 0x8B000074; select their clock source through bit[28:25] of 0x8B000074; and set RFCTL[9]/[6]/[4]/[3] PAD function to 1;
- Before turning on PWMx_EN of PWMx_PRESCALE, software should configure all others control registers, then set PWMx_EN to 1 to start the PWM output;
- When software completes PWM output, it should disable PWMx_EN first, and then disable pwm_eb in global control registers;
- When prescale is P, mod reg is M and duty reg is D, the output pulse width is $T_O = (P+1) * (M+1) * T_{CLK}$, the duty ratio is R = D/(M+1);

6.8 GPIO

6.8.1 Overview

The GPIO module provides up to 176 GPIO pins of MCU. However, many of the pins are multiplexed with other functions and system design trade-off must be exercised on selecting them. All the GPIO pins can be programmed to be either input or output. When in input mode, they can be programmed to trigger interrupt to the MCU.

6.8.2 Features

6.8.2.1 GPIO

- positive edge detect and interrupt generate
- negative edge detect and interrupt generate
- both edges detect and interrupt generate
- high level detect and interrupt generate
- low level detect and interrupt generate
- interrupt mask
- interrupt clear
- input data sample or mask
- output data or mask
- level interrupt generate at system powerdown
- change level detect conditions at arbitary time
- different interrupts happen
- change edge detect conditions

6.8.3 Function Description

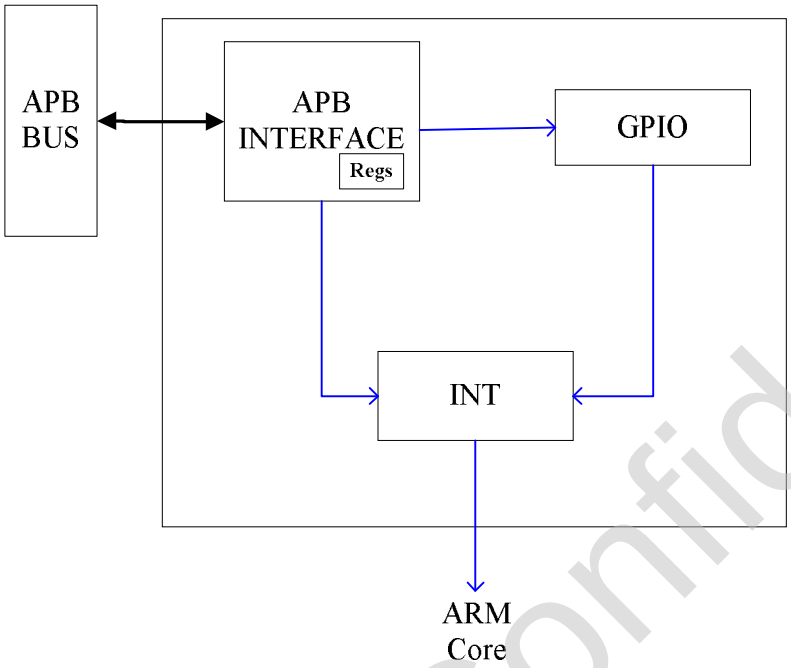


Fig 1 GPIO block diagram

As the above diagram shows, SW communicates with GPIO module by APB BUS. When the module has received active input signals, interrupts will be created to notify ARM core.

6.8.4 Control Registers

6.8.4.1 Memory map

Table 1 GPIO Control Register Address Map

ARM base address:

For GPIO16~GPIO159 (16 gpios for one address):
0x8A00_0000, 0x8A00_0080, 0x8A00_0100, 0x8A00_0180,
0x8A00_0200, 0x8A00_0280, 0x8A00_0300, 0x8A00_0380,
0x8A00_0400

GPIO16-144: come from external pad, refer to SC6820 pin list;
GPIO145: usbd_vm;
GPIO146: usbd_vp;
GPIO147: usbd_se0_wakeup;
GPIO148-159: reserved;

For GPIO176~GPIO207 (16 gpios for one address):
0x8200_0480, 0x8200_04C0

GPIO176-205: come from external pad, refer to chapter 3 Pin Information;
GPIO206-207: reserved;

Offset Address	Name	Description
0x0000	GPIODATA	GPIO bits data
0x0004	GPIODMSK	GPIO bits data mask
0x0008	GPIODIR	GPIO bits data direction
0x000C	GPIOIS	GPIO bits interrupt sense
0x0010	GPIOIBE	GPIO bits both edges interrupt
0x0014	GPIOIEV	GPIO bits interrupt event
0x0018	GPIOIE	GPIO bits interrupt enable
0x001C	GPIORIS	GPIO bits raw interrupt status
0x0020	GPIOMIS	GPIO bits masked interrupt status
0x0024	GPIOIC	GPIO bits interrupt clear
0x0028	GPIOINEN	GPIO input enable

6.8.4.2 Register Descriptions

6.8.4.2.1 GPIODATA

Description：GPIO bits data register

0x0000			(reset 0x0000_0000)													GPIOATA
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIODATA															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	R/W	16'h0	Reserved
GPIODATA	[15:0]	R/W	16'h0	GPIO bits data input

6.8.4.2.2 GPIODMSK

Description：GPIO bits mask register

0x0004			(reset 0x0000_0000)													GPIODMSK
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIODMSK															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIODMSK	[15:0]	R/W	16'h0	GPIODATA register can be read/write if GPIO DMSK set "1"

6.8.4.2.3 GPIODIR

Description：GPIO bits direction register

0x0008			(reset 0x0000_0000)													GPIODIR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIODIR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIODIR	[15:0]	R/W	16'h0	"1" configure gpio bits to be output "0" configure gpio bits to be input

6.8.4.2.4 GPIOIS

Description：GPIO bits interrupt sense register

0x000C			(reset 0x0000_FFFF)													GPIOIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIS															
Type	R/W															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOIS	[15:0]	R/W	16'hFFFF	"1" detect signals level "0" detect signals edge

6.8.4.2.5 GPIOIBE

Description：GPIO bits both edges interrupt register

0x0010			(reset 0x0000_0000)													GPIOIBE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIBE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOIBE	[15:0]	R/W	16'h0	"1" both edges trigger an interrupt, "0" interrupt generation event is controlled by GPIOIEV

6.8.4.2.6 GPIOIEV

Description： GPIO bits interrupt status register

0x0014			(reset 0x0000_FFFF)													GPIOIEV
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIEV															
Type	R/W															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOIEV	[15:0]	R/W	16'hFFFF	GPIO bits interrupt event register: "1" high levels trigger interrupts, "0" low levels trigger interrupts.

6.8.4.2.7 GPIOIE

Description： GPIO bits interrupt enable register

0x0018			(reset 0x0000_0000)													GPIOIE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOIE	[15:0]	R/W	16'h0	GPIO bits interrupt enable register: "1" corresponding bit interrupt is enabled. "0" corresponding bit interrupt isn't enabled

6.8.4.2.8 GPIORIS

Description： GPIO bits raw interrupt status register, and it reflects the status of interrupts trigger conditions detection on pins (prior to GPIOMIS)

0x001C			(reset 0x0000_0000)													GPIORIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIORIS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIORIS	[15:0]	RO	16'h0	GPIO bits raw interrupt status register: "1" interrupt condition met "0" condition not met

6.8.4.2.9 GPIOMIS

Description： GPIO bits masked interrupt status register

0x0020			(reset 0x0000_0000)													GPIOMIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOMIS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOMIS	[15:0]	RO	16'h0	GPIO bits masked interrupt status register: "1" Interrupt active "0" interrupt not active

6.8.4.2.10 GPIOIC

Description： GPIO bits interrupt clear register

0x0024			(reset 0x0000_0000)													GPIOIC
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIC															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOIC	[15:0]	WO	16'h0	GPIO bits interrupt clear register: "1" clears detected interrupt. "0" has no effect.

6.8.4.2.11 GPIOINEN

Description： GPIO input enable register

0x0028			(reset 0x0000_FFFF)													GPIOINEN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOINEN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOINEN	[15:0]	RW	16'h0	GPIO input enable register: "1" input enable. "0" input disable.

6.8.4.2.12 Related Clock & Interrupt control registers

Table 2 Related Clock & Interrupt control registers

Address	Register Name	Bit Pos	Default	Description
0x2090_0214	CTRL0	[3]	1	APB clock Enable of total system
0x2090_0218	CTRL5	[0]	1	Remap control
0x8000_3000	ARM_INT_STATUS	[8]	0	GPIO interrupt status, using No.8 interrupt for GPIO and No.24 interrupt for GPIOA
0x8000_3008	ARM_INT_EN	[8]	0	GPIO interrupt enable
0x8000_300c	ARM_INT_DIS	[8]	0	GPIO interrupt disable/clear
0x8000_3000	ARM_INT_STATUS	[24]	0	ADI interrupt status
0x8000_3008	ARM_INT_EN	[24]	0	ADI interrupt enable
0x8000_300c	ARM_INT_DIS	[24]	0	ADI interrupt disable/clear
0x8B00_0008	GEN0	[6]	1	Enable ADI's PCLK
0x8B00_005C	GLB_DLY	[29]	1	Enable clk_adi
0x8200_0600	ADI_AGEN	[6]	0	APB clock Enable of GPIOA module
0x8200_0024	ADI_READ_CMD	[25:0]	0	ADI read command register
0x8200_0028	ADI_READ_DATA	[31:0]	0	To obtain register value on analog control module
0x8B00_0008	GEN0	[5]	0	APB clock Enable of GPIO module
0x8B00_0008	GEN0	[13]	0	Pin control register bit

6.8.5 Application Notes

6.8.5.1 Programming Notes

1) GPIOMIS is equal to GPIOIE & GPIORIS.

6.9 EIC

6.9.1 Overview

The EIC module includes two sub-modules: EIC and SIC.

The EIC sub-module provides up to 8 EIC source input signal connection. A de-bounce mechanism is used to capture EIC's stable status and a single-trig mechanism is introduced into this sub-module to enhance the input event detect reliability. In addition, this sub-module's clock can be shut off automatically to reduce power dissipation. The de-bounce range is from 1 ms to 4 s with the step of 1 ms. Those input signals shorter than 1 ms will be omitted at this sub-module.

THE SIC sub-module is used to latch some special input signal and send interrupts to MCU core, and it can provides up to 8 SIC source input signal connection.

6.9.2 Features

6.9.2.1 EIC

- high level detect and interrupt generate(not bypass mode)
- low level detect and interrupt generate(not bypass mode)
- interrupt mask(not bypass mode)
- interrupt clear(not bypass mode)
- level interrupt generate at system powerdown with once active trig(not bypass mode)
- keep interrupt stable when no interrupt clear(not bypass mode)
- input data sample or mask(not bypass mode)
- debounce number configurable(not bypass mode)
- only once trig active(not bypass mode)
- trig level condition configurable(not bypass mode)
- high level detect and interrupt generate(bypass mode)
- low level detect and interrupt generate(bypass mode)
- interrupt mask(bypass mode)
- interrupt clear(bypass mode)
- input data sample or mask(bypass mode)
- level interrupt generate at system power down(bypass mode)
- force to open the clock of debounce

6.9.2.2 SIC

- Special IRQ or FIQ interrupt on channel 0 is used to latch some input signal status and trigger IRQ or FIQ interrupt by level detecting (no edge detecting)
- Special IRQ or FIQ interrupt on channel 0 is multiplexed from 8 independent input sources
- Using Latch circuit to realize interrupt generation, SICINTMSK connected to the set port of Latch, and SICINTCLR connected to the clear port of Latch.
- Provide raw status for each of 8 input sources on special channel
- Provide polarity control bit for each of 8 input sources on special channel
- Provide only one clear bit to clear all latches on special channel
- Each input source can be enabled or disabled independently on special channel

6.9.3 Function Description

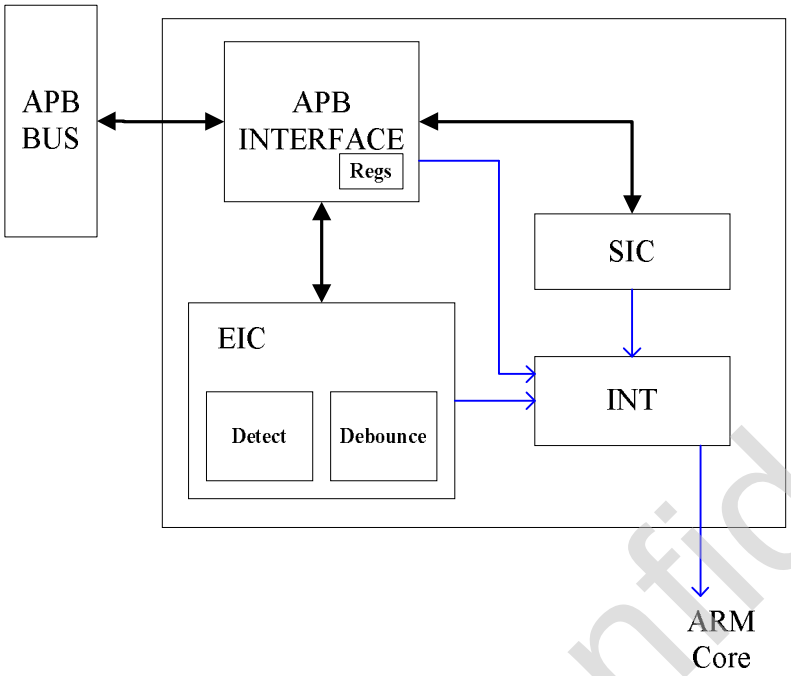


Fig 2 EIC block diagram

As the above diagram shows, SW communicates with EIC module by APB BUS. When the module has received active input signals, interrupts will be created to notify ARM core.

6.9.4 Control Registers

6.9.4.1 Memory map

Table 3 EIC Control Register Address Map

ARM base address: 0x8A00_1000 (EIC) (EIC0-EIC15)
0x8200_0700 (EICA) (EIC160-175)

EIC0-2: come from external pad, refer to SC6820 pin list
EIC3-15: reserved;
EIC160: from TP_XL pad;
EIC161: reserved;
EIC162: CHAR_INT;
EIC163: PBINT
EIC164: HEAD_BUTTON;
EIC165: HEADMIC_DETECTION;
EIC166: CHGR_OVI;
EIC167-175:

Offset Address	Name	Description
0x0000	EICDATA	EIC bits data input
0x0004	EICDMSK	EIC bits data mask

Offset Address	Name	Description
0x0014	EICIEV	EIC bits interrupt event
0x0018	EICIE	EIC bits interrupt enable
0x001C	EICRIS	EIC bits raw interrupt status
0x0020	EICMIS	EIC bits masked interrupt status
0x0024	EICIC	EIC bits interrupt clear
0x0028	EICTRIG	EIC bits trig control
0x0040	EIC0CTRL	EIC0 control register
0x0044	EIC1CTRL	EIC1 control register
0x0048	EIC2CTRL	EIC2 control register
0x004C	EIC3CTRL	EIC3 control register
0x0050	EIC4CTRL	EIC4 control register
0x0054	EIC5CTRL	EIC5 control register
0x0058	EIC6CTRL	EIC6 control register
0x005C	EIC7CTRL	EIC7 control register

Table 4 SIC Control Register Address Map

ARM base address: 0x8A00_1080

SIC0: uart0_rxd, internal source.
SIC1: uart0_ctsn, internal source;
SIC2: uart1_rxd, internal source;
SIC3: uart2_rxd, internal source;
SIC4: usbd_se0_wakeup, internal source;
SIC5: uart2_ctsn, internal source;
SIC6: ARM core power-up require, internal source;
SIC7: reserved;

Offset Address	Name	Description
0x0000	SICINTEN	SIC interrupt enable
0x0004	SICINTRAW	SIC raw interrupt
0x0008	SICINTMSK	SIC interrupt mask
0x000C	SICINTCLR	SIC interrupt clear
0x0010	SICINTPOL	SIC interrupt polarity

Offset Address	Name	Description
0x0014	SICINTMODE	SIC interrupt mode

6.9.4.2 Register Descriptions

6.9.4.2.1 EICDATA

Description： EIC bits data register, read only

0x0000		(reset 0x0000_0000)										EICDATA			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EICDATA							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EICDATA	[7:0]	RO	8'h0	EIC bits data input

Note: EICDATA synchronizes the original data inputs with 2 cycles of Rtcdiv5_clk, so SW need delay 2ms to get the exact value of original data inputs when Rtcdiv5_clk is enabled.

6.9.4.2.2 EICDMSK

Description： EIC bits data mask register

0x0004			(reset 0x0000_0000)													EICDMSK
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EICDMSK							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EICDMSK	[7:0]	R/W	8'h0	EICDATA register can be read if EICDMSK set "1"

6.9.4.2.3 EICIEV

Description： EIC bits interrupt status register

0x0014			(reset 0x0000_00FF)													EICIEV
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EICIEV							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EICIEV	[7:0]	R/W	8'hFF	EIC bits interrupt status register: "1" high levels trigger interrupts, "0" low levels trigger interrupts.

6.9.4.2.4 EICIE

Description： EIC bits interrupt enable register

0x0018			(reset 0x0000_0000)													EICIE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EICIE							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EICIE	[7:0]	R/W	8'h0	EIC bits interrupt enable register: "1" corresponding bit interrupt is enabled. "0" corresponding bit interrupt isn't enabled

6.9.4.2.5 EICRIS

Description： EIC bits raw interrupt status register, and it reflects the status of interrupts trigger conditions detection on pins (prior to EICMIS)

0x001C			(reset 0x0000_0000)													EICRIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EICRIS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EICRIS	[7:0]	RO	8'h0	EIC bits raw interrupt status register: "1" interrupt condition met "0" condition not met

6.9.4.2.6 EICMIS

Description： EIC bits masked interrupt status register

0x0020			(reset 0x0000_0000)													EICMIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EICMIS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: EICMIS = EICIE & EICRIS

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EICMIS	[7:0]	RO	8'h0	EIC bits masked interrupt status register: "1" interrupt active "0" interrupt not active

6.9.4.2.7 EICIC

Description： EIC bits interrupt clear register

0x0024			(reset 0x0000_0000)													EICIC
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EICIC							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	WO	24'h0	Reserved
EICIC	[7:0]	WO	8'h0	EIC bits interrupt clear register: "1" clears detected interrupt.

				“0” has no effect.

6.9.4.2.8 EICTRIG

Description： EIC bits trig control register

0x0028			(reset 0x0000_0000)													EICTRIG
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EICTRIG							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	WO	24’h0	Reserved
EICTRIG	[7:0]	WO	8’h0	EIC bits trig control register: “1”: generate the trig_start pulse “0”: no effect It must set EICTRIG for using de-bounce function and getting active interrupt.

6.9.4.2.9 EIC0CTRL

Description： EIC0 control register

0x0040			(reset 0x0000_4032)													EIC0CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset	Description

			Value	
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.10 EIC1CTRL

Description： EIC1 control register

0x0042			(reset 0x0000_4032)													EIC1CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.11 EIC2CTRL

Description： EIC2 control register

0x0048			(reset 0x0000_4032)												EIC2CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.12 EIC3CTRL

Description： EIC3 control register

0x004C			(reset 0x0000_4032)													EIC3CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.13 EIC4CTRL

Description： EIC4 control register

0x0050			(reset 0x0000_4032)												EIC4CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.14 EIC5CTRL

Description： EIC5 control register

0x0054			(reset 0x0000_4032)													EIC5CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.15 EIC6CTRL

Description： EIC6 control register

0x0058			(reset 0x0000_4032)												EIC6CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.16 EIC7CTRL

Description： EIC7 control register

0x005C			(reset 0x0000_4032)													EIC7CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.17 SICINTEN

Description：SIC interrupt enable register

0x0000			(reset 0x0000_0000)													SICINTEN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								SICINTEN							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

	[31:8]	RO	24'h0	Reserved
SICINTEN	[7:0]	RW	8'h0	SIC interrupt enable register: "1": enable bit interrupt "0": disable bit interrupt

6.9.4.2.18 SICINTRAW

Description：SIC raw interrupt register

0x0004			(reset 0x0000_0000)													SICINTRAW
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								SICINTRAW							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
SICINTRAW	[7:0]	RW	8'h0	SIC raw interrupt status register: "1" interrupt condition met "0" condition not met

6.9.4.2.19 SICINTMSK

Description：SIC interrupt mask register

0x0008			(reset 0x0000_0000)													SICINTMSK
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								SICINTMSK							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
SICINTMSK	[7:0]	RO	8'h0	SIC interrupt mask register "1" Interrupt active "0" interrupt not active

Note: SICINTMSK = SICINTEN & SICINTRAW, and SICINTMSK are connected to the set port of Latch

6.9.4.2.20 SICINTCLR

Description：SIC interrupt clear register

0x000C			(reset 0x0000_0000)										SICINTCLR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								SICINTCLR							
Type	RO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
SICINTCLR	[7:0]	WO	8'h0	SIC interrupt clear register: "1" clears detected interrupt. "0" has no effect.

Note: SICINTCLR are connected to the "clear" port of Latch, and it need disable the "set" port of Latch by changing SICINTPOL to clear SIC interrupt.

6.9.4.2.21 SICINTPOL

Description：SIC interrupt polarity register

0x0010			(reset 0x0000_0000)													SICINTPOL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								SICINTPOL							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
SICINTPOL	[7:0]	RW	8'h0	SIC polarity register: "0": high levels trigger interrupts, "1": low levels trigger interrupts.

6.9.4.2.22 SICINTMODE

Description： SIC interrupt mode register

0x0014			(reset 0x0000_0000)													SICINTMODE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								SICINTMODE							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
SICINTMODE	[7:0]	RW	8'h0	SIC interrupt mode register: "1": interrupt active without chip sleep "0": interrupt active with chip sleep

6.9.4.2.23 Related Clock & Interrupt control registers

Table 5 Related Clock & Interrupt control registers

Address	Register Name	Bit Pos	Default	Description
0x2090_0214	CTRL0	[3]	1	APB clock Enable of total system
0x2090_0218	CTRL5	[0]	1	Remap control
0x8000_3000	ARM_INT_STATUS	[24]	0	ARM interrupt status, using No.8 interrupt for EIC and No.24 interrupt for EICA
0x8000_3008	ARM_INT_EN	[24]	0	ARM interrupt enable
0x8000_300c	ARM_INT_DIS	[24]	0	ARM interrupt disable/clear
0x8B00_0008	GEN0	[6]	1	Enable ADI's PCLK
0x8B00_005C	GLB_DLY	[29]	1	Enable clk_adi
0x8200_0024	ADI_READ_CMD	[25:0]	0	ADI read command register
0x8200_0028	ADI_READ_DATA	[31:0]	0	To obtain register value
0x8B00_0008	GEN0	[9]	0	APB clock Enable of EIC module
0x8B00_0008	GEN0	[24]	0	Rtcdiv5_clk Enable of EIC module
0x8200_0600	ADI_AGEN	[3]	0	APB clock Enable of EICA
0x8200_0600	ADI_AGEN	[11]	0	Rtcdiv5_clk clock Enable of EICA
0x8B00_0008	GEN0	[13]	0	Pin control register bit
0x8B00_004C	GEN3	[29]	0	Software reset EIC module

6.9.5 Application Notes

6.9.5.1 Programming Model

For EIC sub-module, software needs to adopt corresponding steps as follows:

1) When system resets, EIC module is also under the reset status and cannot capture the EIC input signals. At the process of system initialization, ARM needs to configure the EIC input signal detecting conditions, such as '1'/'0' detection, read INT status registers and write EICIC to clear the EIC INTs. Then, if necessary, ARM sends a trig_start pulse to commence one EIC signal detection process. Before system enters deep-sleep mode or closes PCLK, it ought to assure that EIC INT has been enabled and cleared and system has sent out active trig_start pulse.
2) After receiving the trig_start pulse, EIC module starts the process of EIC signal detection. If EIC captures one stable input signal, it will send an INT to ARM, shut off the clock of debounce circuit automatically and wait for next trig_start pulse.
3) When ARM receives the EIC INT again, it enters INT process flow. And if EIC input condition changes, ARM needs to configure those detecting condition registers again. Then, if necessary, ARM sends a trig_start pulse again to commence a new EIC signal detection process.
4) Step 1 to step 3 cycles.
5) For the debounce bypass mode, ARM can receive INT without the need of sending trig_start pulse.

6.9.5.2 Programming Notes

1) The register, EICIEV, is used to set the input signal constraints for INT trigger.
2) EICINT comes from EICMIS, which EICMIS is equal to EICIE & EICRIS. So, if it needs to get some EIC' INT, the EICIE should be unmasked. And if ARM has received one EIC INT, it maybe need to mask the corresponding bit of EICIE to avoid to received the same INT, and set corresponding bits 1 to of EICIC.
3) The interval of two EIC trigger instructions needs be longer than 2 ms.
4) To quit EIC FSM correctly, it needs 2 or 3 additional milliseconds. So it needs consider the additional time for exact debounce period.

6.10 Auxiliary ADC

6.10.1 Overview

The AuxADC is a 16-channel ADC, it samples VBAT voltage, touch panel signals, etc. The channel assignment is shown in the following table:

Table 6-5 ADC Channel Assignment

Channel ID	Application
Ch0	General signal input channel, the signal is from external input.
Ch1	General signal input channel, the signal is from external input.
Ch2	TPC X signal input channel, the signal is from external input.
Ch3	TPC Y signal input channel, the signal is from external input.
Ch4	PROG2ADC (in Charger) signal input channel, the signal is on chip.
Ch5	VBAT signal input channel, the signal is on chip.

Ch6	VCHGSEN signal input channel, the signal is on chip.
Ch7	General signal input channel, the signal is from external input.
Ch8	General signal input channel, the signal is from external input.
Ch9	VCHGBandGap signal input channel, the signal is on chip.
Ch10	VDCDC to ARM signal input channel, the signal is on chip.
Ch11	VDCDC to others signal input channel, the signal is on chip.
Ch12~Ch15	Reserved

The ADC mainly arbitrates multi-channel ADC request and controls the sampling process of analog part. Among these 16 channels, all channels can be controlled by SW, and therefore, they are called SW channels. When some channel is used to measure touch panel signals, the touch panel controller (TPC) can control its sampling, they are also called HW channels.

6.10.2 Features

- Sample frequency >= 85 kHz;
- Support arbitration between SW and HW channels;
- Support up to 16 channels;
- Support interrupt functions;
- Configurable channel ID for TPC channel;
- Configurable sampling delay for TPC channel;

6.10.3 Signal Description

There are 16 signal sources to ADC, 6 are from external, 4 are connected on chip and others are reserved. The external input signals are for ADC channels 0, 1, 2, 3, 7 and 8, as listed in the following table:

Table 6-6 ADC signal list

Signal Name	Direction	Width	Description
ADCI0 (Ch0)	I	1	General signal input, it is for ADC channel 0.
ADCI1 (Ch1)	I	1	General signal input, it is for ADC channel 1.
TP_XL (Ch2)	I/O	1	TPC signal in Y direction, it is for ADC channel 3.
TP_YD (Ch3)	I/O	1	TPC signal in X direction, it is for ADC channel 2.
ADCI2 (Ch7)	I	1	General signal input, it is for ADC channel 7.
ADCI3 (Ch8)	I	1	General signal input, it is for ADC channel 8.

6.10.4 Function Description

The ADC application circuit is as follows.

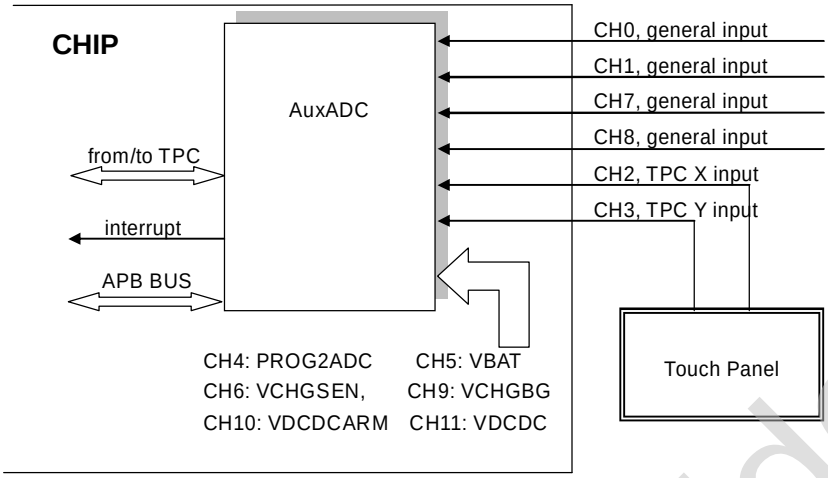


Figure 6-39 ADC Application Diagram

The ADC is controlled by system through APB bus, and it is used to check 16 signals from different sources. ADC does the channel arbitration and ADC conversion control. Because channels 2 and 3 are for TPC, there are some signals between ADC and TPC for their interaction. The ADC's block diagram is shown in the following figure.

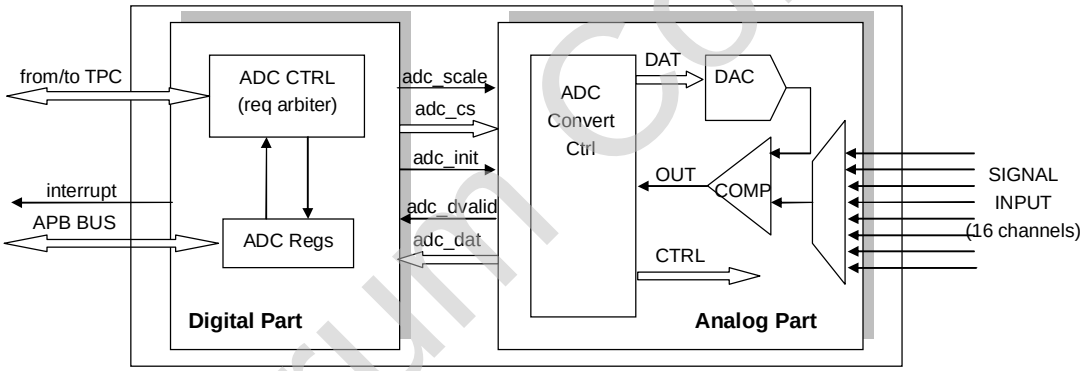


Figure 6-40 ADC controller block diagram

The ADC includes a digital control part and an analog conversion part. The digital control part arbitrates and responds to the sampling request, sends the control to the analog part. The analog part consist of a DAC (digital to analog convertor), and a comparator. The DAC converses the input data to a reference voltage, while the comparator compares the reference voltage and input voltage and sends out a compare result.

First, the digital part powers up the analog part, and gives an initial data (0x200) to the analog part. After the initial process, the ADC starts the MSB conversion. The initial data is for half reference voltage. If the input voltage is greater than it, the data will be changed to 0x300, else the data will be changed to 0x100. After such 10 iterations, all 10 bits are complete, and the active ADC data occurs and can be outputted. The ADC conversion process is as in the figure below.

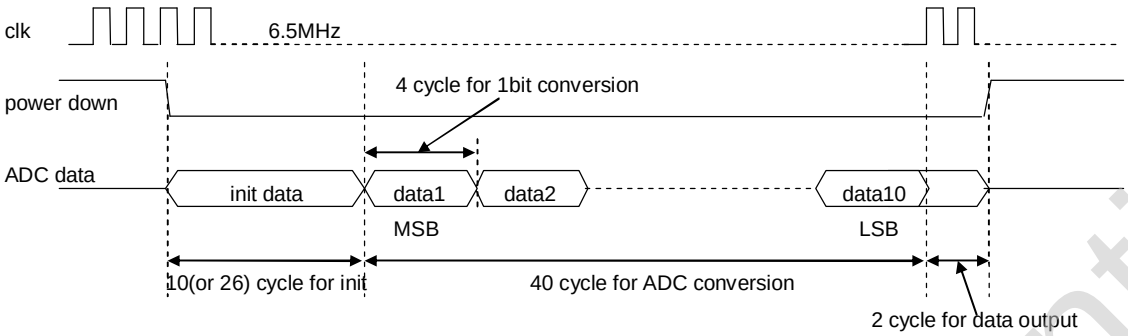


Figure 6-41 ADC Conversion

The TPC channels have larger internal resistance than others channels, so they need longer initial time, it includes 26 6.5MHz clocks, others are 10 6.5MHz clocks.

When ADC is controlled by SW entirely, every channel can use the ADC one by one without request confliction. But the TPC can always run, the ADC can arbitrate the requests from SW channel or TPC channel automatically, so software can insert SW request randomly, the switch of ADC between SW channels and TPC channels is as below.

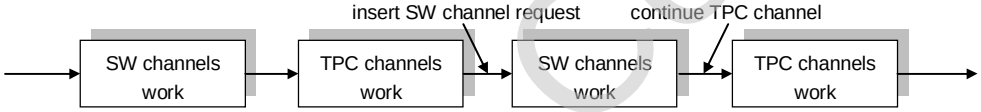


Figure 6-42 ADC Switch Diagram

Normally, the TPC holds the ADC for a long time and it is HW request, so we assign a lower priority for HW channels, a higher priority for SW channels. When there is only one channel active, ADC responds to it. When there are two requests, ADC will respond to the SW channel first, then the HW one. ADC's response is at the end of sampling, thus it can guarantee every sampling is an atom operation.

An example for ADC usage is shown in the following figure.

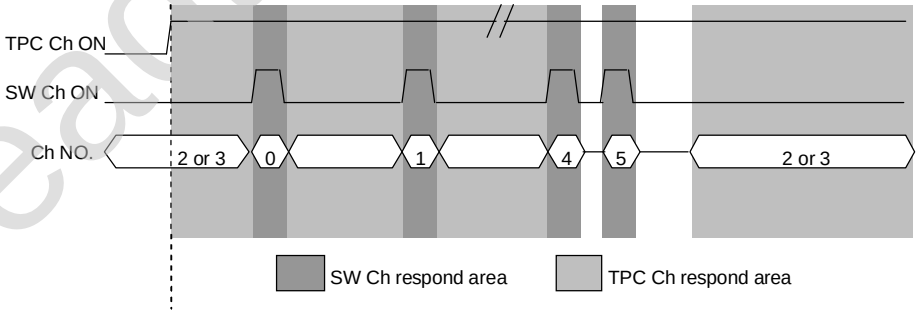


Figure 6-43 ADC Usage Example

6.10.5 Control Registers

6.10.5.1 Memory map

ARM base address: 0x8200_0300

Offset Address	Name	Description
0x0000	ADC_CTRL	ADC control
0x0004	ADC_CS	ADC channel configuration
0x0008	ADC_TPC_CH_CTRL	TPC channel control
0x000C	ADC_DAT	ADC data
0x0010	ADC_IRQ_EN	ADC interrupt enable
0x0014	ADC_IRQ_CLR	ADC interrupt clear
0x0018	ADC_IRQ_STATUS	ADC interrupt status
0x001C	ADC_IRQ_SRC	ADC interrupt source

6.10.5.2 Register Descriptions

6.10.5.2.1 ADC_CTRL

Description: ADC module control.

0x0000		ADC control register (reset 0x0)											ADC_CTRL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											ADC_STATUS	HW_INT_EN	TPC_CH_ON	SW_CH_ON	ADC_EN
Type	RO											RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:5]	RO	27'h0	Reserved
ADC_STATUS	[4]	RO	1'h0	ADC sampling status, 1: for completing an active sampling
HW_INT_EN	[3]	R/W	1'h0	TPC channel IRQ enable, It is only for test purpose.
TPC_CH_ON	[2]	R/W	1'h0	TPC channel on/off, 0: turn off TPC channel; 1: turn on TPC channel. It is only for TPC channel, here, is for channel 2/3.
SW_CH_ON	[1]	R/W	1'h0	SW channel on/off, 0: turn off some a SW channel; 1: turn on some a SW channel.
ADC_EN	[0]	R/W	1'h0	ADC global enable,

				0: ADC module disable; 1: ADC module enable.

6.10.5.2.2 ADC_CS

Description: ADC channel configuration.

0x0004	ADC channel configuration (reset 0x0f)															ADC_CS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										ADC_SLOW	ADC_SCALE	ADC_CS			
Type	RO										R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:6]	RO	26'h0	Reserved
ADC_SLOW	[5]	R/W	1'h0	ADC coversion speed control, 0: quick mode, coversion initial includes 10 ADC clocks; 1: slow mode, conversion initial includes 26 ADC clocks.
ADC_SCALE	[4]	R/W	1'h0	ADC scale setting for current ADC channel, 0: little scale, 0 ~ 1.2 V; 1: big scale, 0 ~ 3.0 V.
ADC_CS	[3:0]	R/W	4'h0	ADC channel ID, It is in 0 ~ 15.

6.10.5.2.3 ADC_TPC_CH_CTRL

Description: TPC channel control.

0x0008	TPC channel control (reset 0x32)															ADC_TPC_CH_CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TPC_CH_DELAY								TPC_Y_CH				TPC_X_CH			
Type	R/W								R/W				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
TPC_CH_DELAY	[15:8]	R/W	8'h0	TPC channel sampling delay, it is 6.5MHz clock number.
TPC_Y_CH	[7:4]	R/W	4'h3	TPC Y channel ID. it can be 0 ~ 15, here, it should be 3.
TPC_X_CH	[3:0]	R/W	4'h2	TPC X channel ID. it can be 0 ~ 15, here, it should be 2.

6.10.5.2.4 ADC_DAT

Description: ADC conversion result.

0x000C			ADC data (reset 0x0)													ADC_DAT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						ADC_DAT									
Type	RO						RO									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:10]	RO	22'h0	Reserved
ADC_DAT	[9:0]	RO	10'h0	ADC conversion result.

6.10.5.2.5 ADC_IRQ_EN

Description: ADC interrupt enable.

0x0010			ADC interrupt enable (reset 0x0)													ADC_IRQ_EN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															ADC_IRQ_EN
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:1]	RO	31'h0	Reserved
ADC_IRQ_EN	[0]	R/W	1'h0	ADC interrupt enable, 0: interrupt disable; 1: interrupt enable.

6.10.5.2.6 ADC_IRQ_CLR

Description: ADC interrupt clear.

0x0014	ADC interrupt clear (reset 0x0)															ADC_IRQ_CLR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															ADC_IRQ_CLR
Type	RO															WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:1]	RO	31'h0	Reserved
ADC_IRQ_CLR	[0]	WO	1'h0	ADC interrupt clear. Write "1" to clear.

6.10.5.2.7 ADC_IRQ_STSTUS

Description: ADC masked interrupt.

0x0018	ADC interrupt status (reset 0x0)															ADC_IRQ_STATUS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															ADC_IRQ_STATUS
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:1]	RO	31'h0	Reserved
ADC_IRQ_STATUS	[0]	RO	1'h0	ADC masked interrupt.

6.10.5.2.8 ADC_IRQ_RAW

Description: ADC raw interrupt.

0x001C			ADC raw interrupt													ADC_IRQ_RAW
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															ADC_IRQ_RAW
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:1]	RO	31'h0	Reserved
ADC_IRQ_RAW	[0]	RO	1'h0	ADC raw interrupt.

6.10.6 Application Notes

6.10.6.1 Program Flow

Before configure module, set some global parameters,

Set bit[13] of 0x8200_0600 to enable CLK_ADC;

Set bit[14] of 0x8200_0600 to enable CLK_AUXAD;

Set bit[5] of 0x8200_0600 to enable AuxADC module;

Set or reset bit[4] of 0x8200_0604 to reset AuxADC module;

Set bit[24] of 0x8000_3008 to enable ADI interrupt, later, we need scan ADI interrupt status, check bit[0] of 0x8200_0380 for ADC module interrupt and bit[4] of 0x8200_0380 for TPC module interrupt;

Some registers are configured through ADI module, so ADI must be ready before do these.

Flow for SW request channels

- Clear ARM's ADI interrupt and ADC interrupt, and enable them;
- Configure ADC module registers;
- Enable ADC module, set "ADC_EN" bit of ADC_CTRL, and the ADC is ready to work;

- When program needs to use ADC, set its channel ID, and switch on the ADC SW channel;
- When ARM's ADI interrupt asserts, and "adc_irq" occurs or "adc_status" flag become '1', read out the sample data;
- Switch off the ADC SW channel and set channel ID to last one.

Flow for HW request channels (only for TPC application)

- Clear ARM's ADI interrpt, ADC interrupt and TPC interrupt, and enable them;
- Configure ADC and TPC registers;
- Enable ADC and TPC module, set "ADC_EN" bit of ADC_CTRL, and the ADC is ready to work;
- When TPC receives "down_irq", switch on TPC channel, and run the TPC, then ADC will work;
- ADC responses the TPC's continue request, TPC responses to "done_irq";
- If need insert SW ADC request, program insert SW request arbitrarily;
- When TPC receives "up_irq", stop the TPC, switch off the TPC channel and cancel TPC selection.

6.10.6.2 Program Notes

- If channel 2 or 3 are used for TPC channel, then ADC_CS[3:0] = 2 or ADC_CS[3:0] = 3 are same function, it means that ADC_CS[3:0] can be Y channel also can be X channel when for TPC application;
- SW should guarantee two SW channels cannot be accessed at same time;
- In SW channel control, switch on and switch off SW channel must be occurred in pair;
- When ADC is in sampling, do not change control registers randomly;
- When insert SW request, firstly, update channel selection etc. registers, lastly, switch on SW channel;

6.11 Touch Pannel Controller (TPC)

6.11.1 Overview

SC6820 has one on-chip touch panel controller module, which shares both the channel 3 and channel 2 of auxiliary ADC. The TPC measures the position of pressure point, records these position information, and generates interrupts for system responding pen down/up and getting data.

6.11.2 Features

- Support de-bouncing;
- Support noise filter;
- Support position calculation;
- Configurable sampling time interval;
- Configurable sample number;
- Support 3-D measure with X/Y/Z;
- Raw X/Y ADC output or X/Y position output;
- Raw Z ADC output;
- Support switch between X and Y analog input;
- Support wake up;

6.11.3 Signal Description

There are 4 signals for sampling control. TP_XL and TP_XR are for X direction, and TP_YU and TP_YD are for Y direction; they are listed in the Table xx.

Table 6-7 TPC signal list

Signal Name	Direction	Width	Description
TP_XL	I/O	1	High level output in X direction when it is output; TPC signal in Y direction when it is input, it is connected to AuxADC channel 3.
TP_XR	O	1	Low level output in X direction.
TP_YU	O	1	High level output in Y direction.
TP_YD	I/O	1	Low level output in Y direction when it is output; TPC signal in X direction when it is input, it is connected to AuxADC channel 2.

6.11.4 Function Description

The touch panel application circuit is as follows.

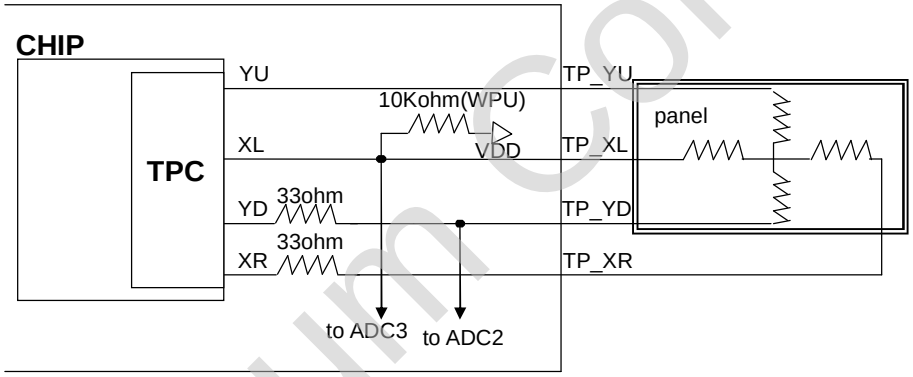


Figure 6-44 Touch panel application diagram

The TPC's block diagram is shown in the following figure.

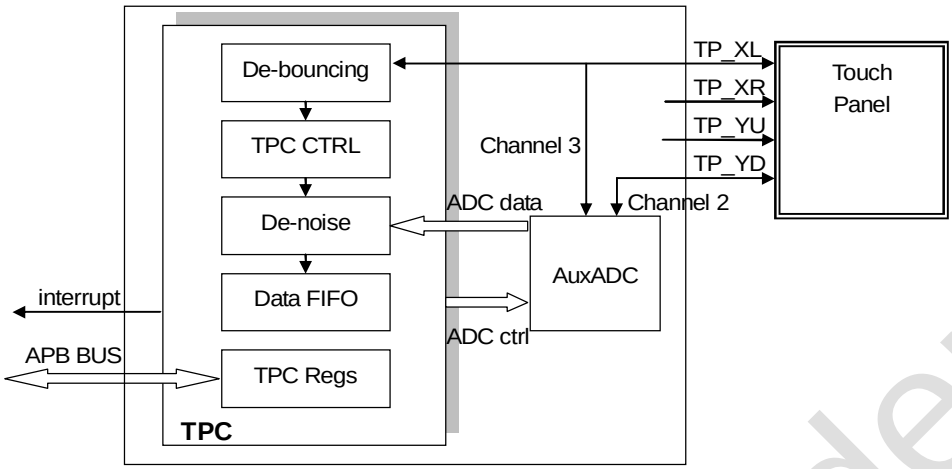


Figure 6-45 TPC block diagram

The TPC includes de-bouncing, de-noise, data FIFO, sampling control logic, etc.

The TPC supports 3D measure, it means it can measure different input from X/Y/Z, the X/Y is used for location, and the Z is used for pressure.

The sampling of X/Y is shown below.

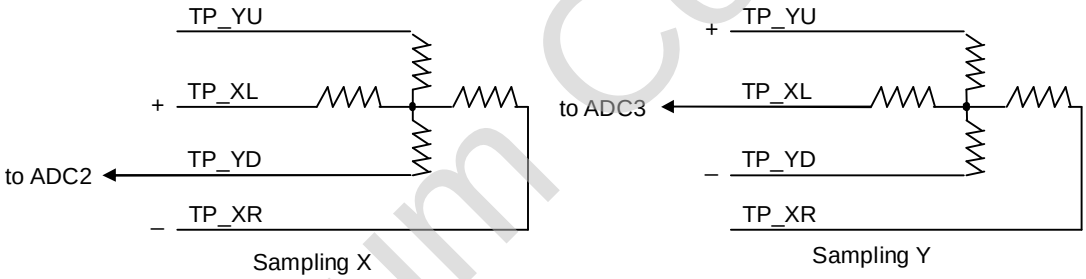


Figure 6-46 Sampling of X/Y

The sampling of Z is different from X/Y, and it is shown below.

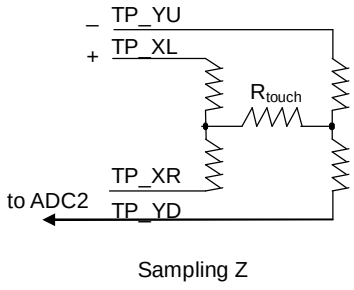


Figure 6-47 Sampling of Z

The method is based X, Y, Z data,

R_{touch}= (1024/Z-1) * R_x * X/1024 + R_y * (1 – Y/1024)

Here, X is raw ADC value of X, Y is raw ADC value of Y, Z is raw ADC value of Z, R_x is total resistance of X, R_y is total resistance of Y. Because above formulas include division, TPC only reports raw Z data, the R_{touch} or pressure is calculated by SW.

The control of 4 TPC PAD is shown in the following table.

Table 6-8 TPC pad control

PAD	Sampling Y	Sampling X	Sampling Z1	Idle
TP_YU	output '1'	input	output '1'	output '0'
TP_YD	output '0'	input to adc2	input	input
TP_XL	input to adc3	output '1'	input to adc3	input, pad wpu on
TP_XR	input	output '0'	output '0'	input

The detail TPC sampling control flow is as in the following figure.

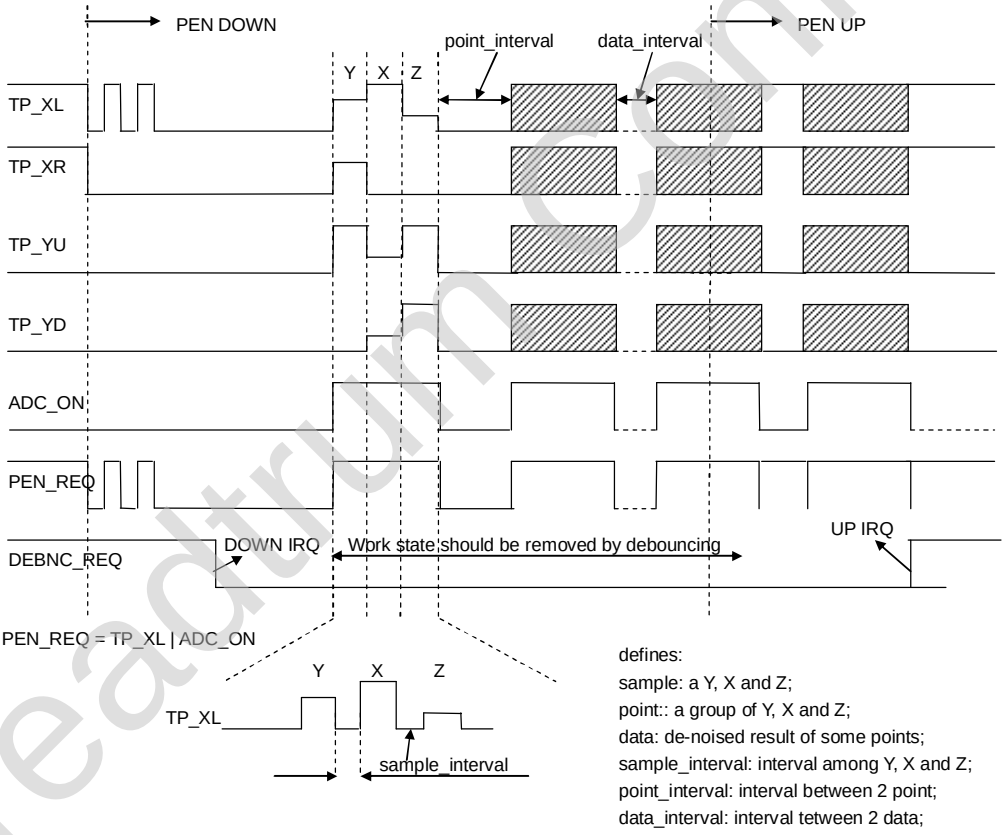


Figure 6-48 TPC sampling control flow

The de-bouncing logic checks the pen-down signal and cleans it. During pressing the panel, bounce always exists, and it may be short, or it may be long. In order to cancel some inactive pressing, de-bouncing is needed. A configurable check interval is used to control the input sample. If every result is the same in specified check times, it is considered an active pressing; otherwise, it is considered an inactive pressing. The de-bouncing process is show in the following figure.

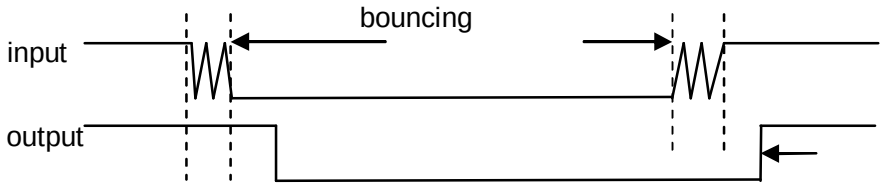


Figure 6-49 De-bouncing diagram

The de-noise logic tries to remove the exceptional samples. After measuring, there are several sample values for one point. To get the most reasonable result, some processing is needed for these data, such as noise filtering.

The normal noise filter is an average filter or median filter. The average filter can get smoother signal wave, while the median filter is good to cancel discrete noise.

The average filter is as follows.

$X = X_0C_0 + X_1C_1 + X_2C_2 + \ldots + X_nC_n$

where X_i (I = 0, 1, …, n) are sample values, C_i (I = 0, 1, …, n) are filter coefficients, and X is filter output.

The median filter is as follows.

$X = \text{median}(X_0, X_1, X_2, \ldots, X_n)$

where X_i (I = 0, 1, …, n) are sample values, X is filter output, and median() gets the median value from X_i (I = 0, 1, …, n) sequence. For example, if $X_0 < X_1 < X_2$, $\text{median}(X_0, X_1, X_2) = X_1$.

Expect for calibration, we need the active coordinate data. We assume the panel is a linear device, so the X and Y positions are a linear function of their measured value. Therefore, their formulas are as follows.

$X = a_X*A_X + b_X$

$Y = a_Y*A_Y + b_Y$

X is sample result in horizontal, a_X and b_X are line parameters for X; Y is sample result in vertical, a_Y and b_Y are line parameters for Y. A_X and A_Y are ADC outputs.

If weconfigure the a_X, b_X, a_Y and b_Y, we can calculate the position result for every pressure based on the above formulas.

6.11.5 Control Registers

6.11.5.1 Memory map

ARM base address: 0x8200_0280

Offset Address	Name	Description
0x0000	TPC_CTRL	Touch panel controller control
0x0004	TPC_SAMPLE_CTRL0	TPC sample control0

Offset Address	Name	Description
0x0008	TPC_SAMPLE_CTRL1	TPC sample control1
0x000C	TPC_BOUNCE_CTRL	TPC bounce control
0x0010	TPC_FILTER_CTRL	TPC filter control
0x0014	TPC_CALC_CTRL	TPC calculation control
0x0018	TPC_CALC_X_COEF_A	TPC calculation x coefficient a
0x001C	TPC_CALC_X_COEF_B	TPC calculation x coefficient b
0x0020	TPC_CALC_Y_COEF_A	TPC calculation y coefficient a
0x0024	TPC_CALC_Y_COEF_B	TPC calculation y coefficient b
0x0028	TPC_IRQ_EN	TPC interrupt enable
0x002C	TPC_IRQ_STATUS	TPC interrupt status
0x0030	TPC_IRQ_RAW	TPC raw interrupt status
0x0034	TPC_IRQ_CLR	TPC interrupt clear
0x0038	TPC_BUF_CTRL	TPC buffer control
0x003C	TPC_X_DATA	TPC X data
0x0040	TPC_Y_DATA	TPC Y data
0x0044	TPC_Z_DATA	TPC Z data

6.11.5.2 Register Descriptions

6.11.5.2.1 TPC_CTRL

Description: Touch panel control.

0x0000			Touch panel control (reset 0x0d08)												TPC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PRESCALE								Reserved		TPC_STOP	TPC_RUN	TPC_MODE	XY_INPUT_SWITCH	PEN_REQ_POL	TPC_EN
Type	R/W								RO		WO	WO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	0	1	0	0	0	0	1	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
PRESCALE	[15:8]	R/W	8'h0d	The pre-scale coefficient for ADC 6.5MHz clock.

				The divided clock is interval count clock. 0 and 1 as bypass.
	[7:6]	RO	2'h0	Reserved
TPC_STOP	[5]	WO	1'h0	TPC stop control, write '1' to stop TPC work, and it is cleared by HW.
TPC_RUN	[4]	WO	1'h0	TPC run control, write '1' to start TPC work, and it is cleared by HW.
TPC_MODE	[3]	R/W	1'h1	TPC work mode, 0: 2D mode, includes X and Y; 1: 3D mode, includes X, Y and Z1.
XY_INPUT_SWITCH	[2]	R/W	1'h0	X/Y analog input switch, 0: x for x, y for y; 1: x for y, y for x.
PEN_REQ_POL	[1]	R/W	1'h0	External pen request polarity, 0: '0' for down, '1' for up; 1: '0' for up, '1' for down.
TPC_EN	[0]	R/W	1'h0	Touch panel controller enable, 0: TPC disabled; 1: TPC enabled.

6.11.5.2.2 TPC_SAMPLE_CTRL0

Description: TPC sample control.

0x0004	TPC sample control0 (reset 0x4200)												TPC_SAMPLE_CTRL0			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	POINT_INTERVAL								SAMPLE_INTERVAL							
Type	R/W								R/W							
Reset	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
POINT_INTERVAL	[15:8]	R/W	8'h42	The interval between 2 output points, (A point includes Y, X, Z1), it should be > 1.
SAMPLE_INTERVAL	[7:0]	R/W	8'h0	The interval between 2 samplings. (Y and X, X and Z1)

6.11.5.2.3 TPC_SAMPLE_CTRL1

Description: TPC sample control.

0x0008	TPC sample control1 (reset 0x8271)															TPC_SAMPLE_CTRL1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SAMPLE_NUM				DATA_INTERVAL											
Type	R/W				R/W											
Reset	1	0	0	0	0	0	1	0	0	1	1	1	0	0	0	1

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
SAMPLE_NUM	[15:12]	R/W	4'h8	The number of samples, active range is <= 8 for filter limiting. It should be >= 1.
DATA_INTERVAL	[11:0]	R/W	12'h271	The interval between 2 active data, (A data filter from some points), it should be > 1.

6.11.5.2.4 TPC_BOUNCE_CTRL

Description: TPC de-bounce control.

0x000C	TPC bounce control (reset 0x29)															TPC_BOUNCE_CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							DEBOUNCE_NUM								DEBOUNCE_EN
Type	RO							R/W								R/W
Reset	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1

Field Name	Bit	Type	Reset Value	Description
	[31:9]	RO	23'h0	Reserved
DEBOUNCE_NUM	[8:1]	R/W	8'h14	De-bouncing check number.
DEBOUNCE_EN	[0]	R/W	1'h1	De-bouncing enable, 0: debounce disabled; 1: debounce enabled.

6.11.5.2.5 TPC_FILTER_CTRL

Description: TPC filter control.

0x0010	TPC filter control (reset 0x23)													TPC_FILTER_CTRL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										FILTER_TAP				FILTER_MODE	FILTER_EN
Type	RO										R/W				R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:6]	RO	26'h0	Reserved
FITLER_TAP	[5:2]	R/W	4'h8	Filter taps. When in average mode, tap should be 1/2/4/8; when in median mode, tap should be >= 1 and <= 8.
FILTER_MODE	[1]	R/W	1'h1	Filter mode, 0: average filter; 1: median filter.
FILTER_EN	[0]	R/W	1'h1	Noise filter enable, 0: disabled; 1: enabled.

6.11.5.2.6 TPC_CALC_CTRL

Description: TPC calculation control.

0x0014	TPC calculation control (reset 0x0)													TPC_CALC_CTRL		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved													DUMMY		CALC_EN
Type	RO													R/W		R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

	[31:3]	RO	29'h0	Reserved
DUMMY	[2:1]	R/W	2'h0	Reserved
CALC_EN	[0]	R/W	1'h1	Calculation enable, 0: disabled; 1: enabled. It should be disabled during calibration, and enabled in normal mode.

6.11.5.2.7 TPC_CALC_X_COEF_A

Description: TPC calculation coefficient a for X.

0x0018	TPC calculation coefficient a for X (reset 0x0)	TPC_CALC_X_COEF_A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						X_COEF_A									
Type	RO						R/W									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:10]	RO	22'h0	Reserved
X_COEF_A	[9:0]	R/W	10'h0	a_x. It is S2.8, in [-2, 1.996].

6.11.5.2.8 TPC_CALC_X_COEF_B

Description: TPC calculation coefficient b for X.

0x001C	TPC calculation coefficient b for X (reset 0x0)	TPC_CALC_X_COEF_B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved					X_COEF_B										
Type	RO					R/W										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

			Value	
	[31:11]	RO	21'h0	Reserved
X_COEF_B	[10:0]	R/W	11'h0	b_x. It is S11, in [-1024, 1023]

Note: $X = a_x * ADC_x + b_x$

6.11.5.2.9 TPC_CALC_Y_COEF_A

Description: TPC calculation coefficient a for Y.

0x0020	TPC calculation coefficient a for Y (reset 0x0)	TPC_CALC_Y_COEF_A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved						Y_COEF_A									
Type	RO						R/W									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:10]	RO	22'h0	Reserved
Y_COEF_A	[9:0]	R/W	10'h0	a_y. It is S2.8, in [-2, 1.996]

6.11.5.2.10 TPC_CALC_Y_COEF_B

Description: TPC calculation coefficient b for Y.

0x0024	TPC calculation coefficient b for Y (reset 0x0)	TPC_CALC_Y_COEF_B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved					Y_COEF_B										
Type	RO					R/W										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:11]	RO	21'h0	Reserved
Y_COEF_B	[10:0]	R/W	11'h0	b_y. It is S11, in [-1024, 1023]

Note: $Y = a_y * ADC_y + b_y$

6.11.5.2.11 TPC_IRQ_EN

Description: TPC interrupt enable.

0x0028			TPC interrupt enable (reset 0x0)												TPC_IRQ_EN	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved													DONE_IRQ_EN	UP_IRQ_EN	DOWN_IRQ_EN
Type	RO													R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:3]	RO	29'h0	Reserved
DONE_IRQ_EN	[2]	R/W	1'h0	Specified sample done interrupt enable, 0: disabled; 1: enabled.
UP_IRQ_EN	[1]	R/W	1'h0	Press up interrupt enable, 0: disabled; 1: enabled.
DOWN_IRQ_EN	[0]	R/W	1'h0	Press down interrupt enable, 0: disabled; 1: enabled.

6.11.5.2.12 TPC_IRQ_STATUS

Description: TPC masked interrupt.

0x002C			TPC interrupt status (reset 0x0)												TPC_IRQ_STATUS	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved													DONE_IRQ_STS	UP_IRQ_STS	DOWN_IRQ_STS
Type	RO													RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:3]	RO	29'h0	Reserved
DONE_IRQ_STS	[2]	RO	1'h0	Masked DONE_IRQ.
UP_IRQ_STS	[1]	RO	1'h0	Masked UP_IRQ.
DOWN_IRQ_STS	[0]	RO	1'h0	Masked DOWN_IRQ.

6.11.5.2.13 TPC_IRQ_RAW

Description: TPC raw interrupt.

0x0030			TPC raw interrupt status (reset 0x0)												TPC_IRQ_RAW	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved													DDONE_IRQ_RAW	UP_IRQ_RAW	DOWN_IRQ_RAW
Type	RO													RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:3]	RO	29'h0	Reserved
DONE_IRQ_RAW	[2]	RO	1'h0	Raw DONE_IRQ.
UP_IRQ_RAW	[1]	RO	1'h0	Raw UP_IRQ.
DOWN_IRQ_RAW	[0]	RO	1'h0	Raw DOWN_IRQ.

6.11.5.2.14 TPC_IRQ_CLR

Description: TPC interrupt clear.

0x0034			TPC interrupt clear (reset 0x0)												TPC_IRQ_CLR	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved													DONE_IRQ_CLR	UP_IRQ_CLR	DOWN_IRQ_CLR
Type	RO													WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:3]	RO	29'h0	Reserved
DONE_IRQ_CLR	[2]	WO	1'h0	Write '1' to clear DONE_IRQ.
UP_IRQ_CLR	[1]	WO	1'h0	Write '1' to clear Raw UP_IRQ.
DOWN_IRQ_CLR	[0]	WO	1'h0	Write '1' to clear Raw DOWN_IRQ.

6.11.5.2.15 TPC_BUF_CTRL

Description: TPC buffer control.

0x0038			TPC buffer control (reset 0x25)												TPC_BUF_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										BUF_EMP	BUF_FULL	BUF_LENGTH			
Type	RO										RO	RO	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1

Field Name	Bit	Type	Reset Value	Description
	[31:6]	RO	26'h0	Reserved
BUF_EMP	[5]	RO	1'h1	Internal buffer empty status, '1' for empty.
BUF_FULL	[4]	RO	1'h0	Internal buffer full status, '1' for full.
BUF_LENGTH	[3:0]	R/W	4'h5	Specify sample done length. When writing length is

				equal to it, done_irq occurs. It should be >= 1.

6.11.5.2.16 TPC_X/Y/Z_DATA

Description: TPC X/Y/Z data.

0x003C	TPC X data (reset 0x0)	TPC_X_DATA
0x0040	TPC Y data (reset 0x0)	TPC_Y_DATA
0x0044	TPC Z data (reset 0x0)	TPC_Z_DATA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						DATA									
Type	RO						RO									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:10]	RO	22'h0	Reserved
DATA	[9:0]	RO	10'h0	X/Y ADC or position value or Z ADC value.

6.11.6 Application Notes

6.11.6.1 Program Flow

Before configure module, set some global parameters,

Set bit[13] of 0x8200_0600 to enable CLK_ADC;

Set bit[14] of 0x8200_0600 to enable CLK_AUXAD;

Set bit[5]/[4]/[12]/[8] of 0x8200_0600 to enable AuxADC/TPC/RTC_TPC/RTC_ARCH;

Set or reset bit[4]/[5] of 0x8200_0604 to reset AuxADC/TPC module;

Set bit[24] of 0x8000_3008 to enable ADI interrupt, later, we need scan ADI interrupt status, check bit[0] of 0x8200_0380 for ADC module interrupt and bit[4] of 0x8200_0380 for TPC module interrupt;

Some registers are configured through ADI module, so ADI must be ready before do these.

Its work flow is as follows:

- Clear ARM's ADI, ADC, and TPC interrupt, and enable DOWN and UP interrupt;
- Configure ADC and TPC module registers;
- Enable ADC and TPC module;
- When ARM's ADI interrupt asserts, if "down_irq" occurs, run the TPC, and clear the DONE interrupt, then enable the DONE interrupt;
- If "done_irq" occurs, read out sample data;

- If the ADC is needed for other purposes, SW can use it directly, without caring about TPC;

- If “up_irq” occurs, stop the TPC, and disable the DONE interrupt; if necessary, SW can stop TPC at anytime;

- If “down_irq” occurs, adjust control registers, and start a new process with the same flow.

6.11.6.2 Program Notes

- When in 2D mode, the read order is X/Y, When in 3D mode, reading order is Z/X/Y, since the read address will increases 1 after reads Y data, so the Y data is always read out lastly;

- When in work, the de-bouncing should be always turned on, the TP_XL includes pen input signal and sampling control, so we need filter the sampling control;

- When enable de-bouncing, because the bouncing during release pen and de-bouncing, the de-bounced signal includes some invalid part, it is shown in Figure xx. Thus, we should discard those data sampled in invalid range.

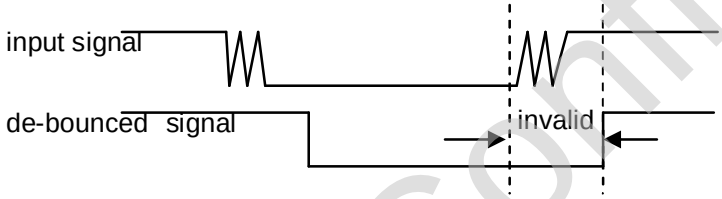


Figure xx Invalid Part in De-bounced Signal

- When in 3D mode, the status from sampling Z to idle will include an obvious charge process in TP_XL pad if panel has a big capacitance, it maybe affect the UP interrupt, we need control the sampling speed, the reference speed is writing a FIFO data more than 1ms.

6.12 SIM Card Interface

6.12.1 Overview

SIM: Subscriber Identity Module

The SIM card interface is implemented according to GSM SIM card standard and conformed to ISO7816. It only supports protocol type T = 0 asynchronous half duplex character transmission mode. The SIM card interface is used to transfer data to/from a SIM card in an asynchronous fashion in half duplex mode through a bi-directional I/O pin.

6.12.2 Features

- Programmable generation of clock to SIM card
- Programmable transmission baud rate
- Support for T = 0 asynchronous protocol type
- Character transmitting and receiving with one 16 byte Tx FIFO and one 16 byte Rx FIFO
- Parity checking and error handling
- Transmission and receiving in DMA mode
- Retransmission after detecting parity error
- Support different interrupt modes
- 2 hardware controllers support 4 software controllers

6.12.3 Signal Description

Table 6-9 Signal Description

PAD Name	Direction	Attribute	Description
SIM_PE	Output	Internal	Used to power up / down SIM card
SIM_RST	Output	PAD	Used to reset SIM card
SIM_CLK	Output	PAD	Used to supply clock for SIM card
SIM_DAT_I	Input	PAD	Serial data in
SIM_DAT_O	Output	PAD	Serial data out

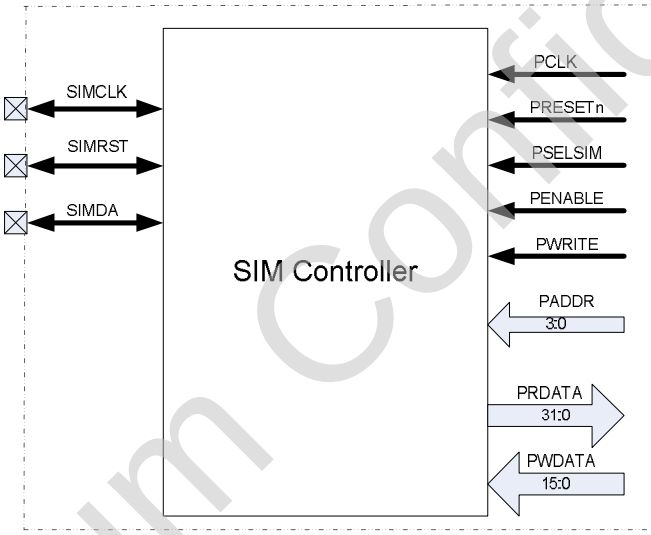


Figure 6-50 SIM Interface Signals

SIM card interface signals are compliant with ISO7816-2 standard where each signal connects to the corresponding SIM card pins listed as the table.

Table 6-10 SIM Card Pin List

C1 : Vcc = 5V	C5 : Gnd
C2 : Reset	C6 : Vpp
C3 : Clock	C7 : I/O
C4 : RFU	C8 : RFU

APB bus is used to configure and control the SIM card controller.

6.12.4 Function Description

6.12.4.1 SIM Controller Interface Block Diagram

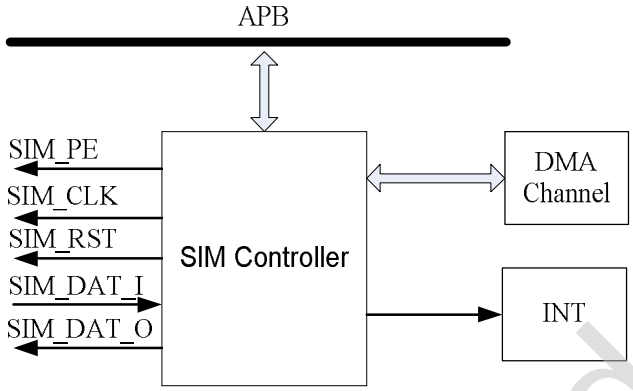


Figure 6-51 SIM Interface Block Diagram

6.12.4.2 SIM Clock and Baud Rate Control

The SIM card clock is generated and sent from the SIM card controller to the SIM card. The SIM_CTL1 register bits [10:8] decide the generated SIM clock frequency.

Table 6-11 SIM Clock and Baud Rate

Clock mode, 0x8500_001C [10:8]	SIM clock frequency
0	MCU clock / 2
1	MCU clock / 4
2	MCU clock / 8
3	MCU clock / 16
4	MCU clock / 32
5	MCU clock / 64
6	MCU clock / 128
7	MCU clock / 256

The baud rate that the SIM card controller uses in Tx and Rx is controlled through programming SIM_CLK_DVD register.

The clock output to the SIM card needs to match the baud rate that the SIM card controller uses so that the Rx and Tx can be done correctly.

6.12.4.3 Resource

Memory:

TX FIFO: 16X8

RX FIFO: 16X8

6.12.4.4 SIM Controller Operations Procedure

The SIM interface device and the SIM card shall be conducted through the following consecutive operations:

- Connection and activation of the contacts by the interface device
- Deactivation of the contacts by the interface device
- Reset of the card
- Subsequent information exchange between the card and the interface device

6.12.4.4.1 Activation and Deactivation of the contacts

The SIM card shall not be activated until the contacts are connected to the interface device to avoid possible damage to any SIM card meeting these standards.

The activation of the contacts by the SIM interface device shall consist of the following consecutive operations:

- RST is in state L.
- VCC shall be powered.
- I/O in the interface device shall be put in reception mode.
- CLK shall be provided with a suitable and stable clock.

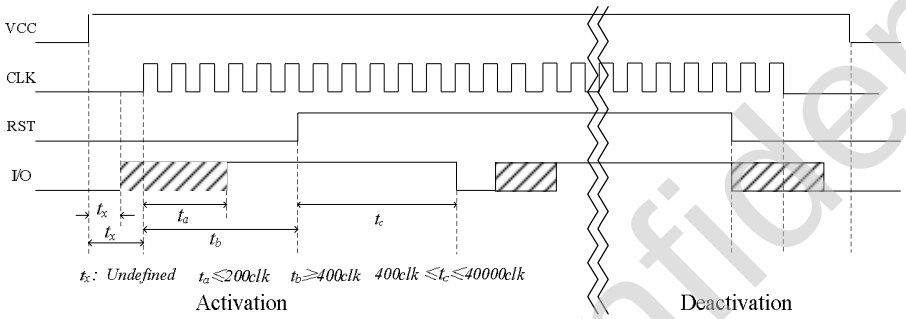


Figure 6-52 Activation and Deactivation Timing Sequence

The SIM card controller is implemented with the some modules; the activation/deactivation control module controls the activation/deactivation sequence of the SIM interface.

After sending an activate command (writing 1 to SIM_CTL0 register bit 11), the activation sequence will be sent to the SIM card.

The following are brief list of commands for the activation functions.

- Program active_deactiva_en bit to 1 to enable activation function.
- Program do_act bit to 1 to start activation sequence.

When information-exchanging is terminated or aborted (unresponsive card or detection of card removal), the electrical contacts should be deactivated.

The deactivation by the interface device shall consist of the following consecutive operations:

- State L on RST
- State L on CLK
- State A on I/O
- VDD inactive

Software program do-deact bit to 1 to begin deactivation sequence.

6.12.4.4.2 Reset of the Card

A card reset is initiated by the interface device, whereupon the card shall respond with an Answer to Reset.

By the end of the activation of the contacts (RST is in L, VDD powered and stable, I/O in reception mode in the interface device, CLK provided suitable and stable clock), the card answering asynchronously is ready for reset.

The clock signal is applied to CLK at time T0. The I/O line shall be to state Z within 200 clock cycles of the clock signal (t2) being applied to CLK (time t2 T0).

The internal reset takes effect a few clock cycles after reset. Answer to Reset on I/O shall begin between 400 and 40,000 clock cycles (t1) after the clock signal applied to CLK (time t1 after T0).

A card with an active low reset is reset by RST in L for at least 40,000 clock cycles (t3) after the clock signal is applied on CLK (time t3 after T0). Thus if no Answer to Reset began within 40,000 clock cycles (t3) with RST in state L, RST is put to state H (at time T1). The Answer to Reset on I/O shall begin between 400 and 40,000 clock cycles (t1) after the rising edge of the signal on RST (time t1 after T1).

If the answer to Reset does not begin within 40,000 clock cycles (t3) with RST in state H (t3 after T1), the signal on RST shall be returned to state L (at time T2) and the contacts shall be deactivated by the interface device.

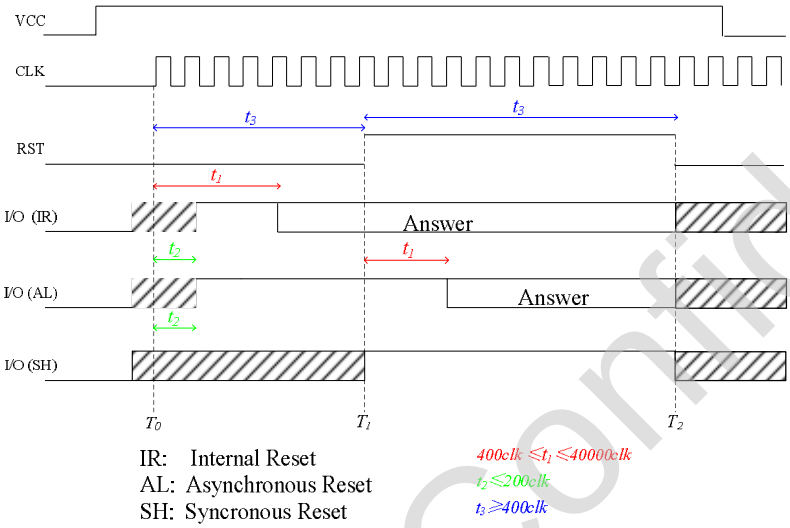


Figure 6-53 Answer to Reset Sequence

NOTES:

The internal state of the card is assumed undefined before reset. Therefore, the design of the card has to avoid improper operations.

In order to continue the dialogue with the card, RST shall be maintained in the state where an answer occurs on I/O.

Reset of a card can be initiated by the interface device at its discretion at any time.

Interface devices may support one or more of these types of reset behavior. The priority of testing for asynchronous or synchronous cards is not defined in the standard.

6.12.4.4.3 Subsequent information exchange between the card and the interface device

6.12.4.4.3.1 Character frame

For asynchronous transmission type, the character of frame during answer to reset is like in the following diagram.

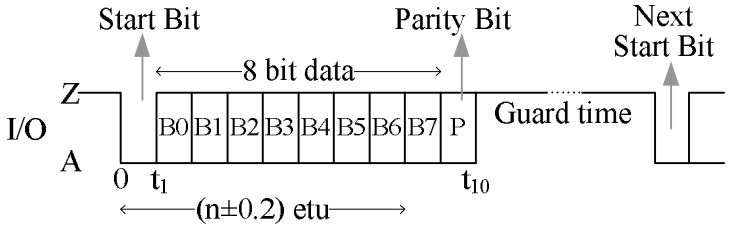


Figure 6-54 The Character of Frame

A character consists of ten consecutive bits:

- A start bit in state A;
- Eight bits of information, designated B0 to B7 and conveying a data byte;
- A tenth bit bi used for even parity checking.

At the SIM interface, a data byte consists of 8 bits B_0 ~ B_7, from the least significant bit (LSB, B_0) to the most significant bit (MSB, B_7)

6.12.4.4.3.2 T = 0, Asynchronous Half Duplex Character Transmission Protocol

The following diagram shows the byte transmission frame structure.

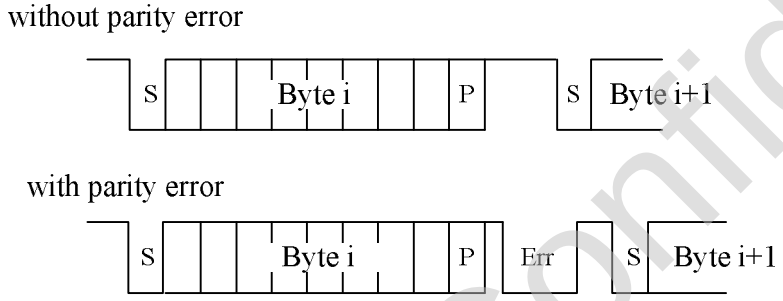


Figure 6-55 T=0 Byte Transmission Diagram

The interface device transmits a header over five successive bytes designated CLA, INS, A1, A2; L. CLA is an instruction class. The value FF is reserved for PTS.

INS is an instruction code in the instruction class. The instruction code is valid only if the least significant bit is 0, and the most significant half byte is neither 6 nor 9. P1, P2 are a reference (e.g., an address) completing the instruction cod.P3 codes the number n of data bytes (D1... Dn) which are to be transmitted during the command. The direction of movement of these data is a function of the instruction. In an outgoing data transfer command, P3 = 0 introduces a 256 byte data transfer from the card. In an incoming data transfer command, P3 = 0 introduces no transfer of data. All remaining encoding possibilities for the header are specified in ISO7816.

6.12.4.4.3.3 SIM Data Tx and Rx

The Tx will start when the tx_enable is 1, there is data in the FIFO and the last Rx is completed. The tx_int_mark sets the condition under which the tx_int will happen. When the empty entry in the tx_fifo is less than tx_int mark, tx_empty int will be set.

The Rx will start when the rx_enable is 1, when the last Tx is done and there is data coming in from the data input. The rx_int_mark sets the condition under which the rx_int will happen. When the data entry in the rx_fifo is greater than rx_int mark, rx_full int will be set.

The bit_convention register decides MSB and LSB in the Tx/Rx serial data, logic_level register decides if high electrical level represents logic 1 in Tx/Rx serial data, and odd_parity register bit decides if using odd or even parity in Tx/Rx data.

In the SIM interface module, a timer is also designed to check if the receive portion is idle for a certain period of time and generate an interrupt when it happens. The watch_dog_count_limit register defines the idle period in data bit streaming. Watch_dog_repeat_en register decides if the timer starts right after the interrupt is acknowledged (the interrupt is cleared). Writing 1 to watch_dog_trigger starts the timer counting. Any activity in the Rx portion will reset the timer counting.

6.12.4.4.3.4 Rx/Tx Control

The Rx/Tx control module controls the transmitting and receiving data to/from the SIM card. The SIM card controller receives/transmits data according to the data-level and bit ordering that are specified in the Logic_level (bit 1) and Bit_convention (bit 0) bits in the SIM_CTL0 register. The data format is: 10 bits per character, 1 start bit + 8 data bits + 1 parity bit.

The SIM card controller includes a 16 byte Tx FIFO for data transmission. It uses a pointer to monitor the number of data in the Tx FIFO that have not yet been transmitted. The MCU can access the pointer by reading the SIM_STS1 register bits 4 to bit 0.

The SIM card controller also uses a configurable Tx interrupt threshold that can be configured by writing to the SIM_CTL1 register bits 4 to 7. This field specifies the number of empty characters that should be available in the Tx FIFO before issuing an interrupt. Whenever the number of empty characters exceeds this value, an interrupt is generated to the MCU. This interrupt is automatically cleared when the number of empty bytes in the Tx FIFO equals to or falls below the specified Tx interrupt threshold value.

The SIM card controller also includes a 16 byte Rx FIFO for data receiving. It uses a pointer to monitor the number of bytes in the Rx FIFO that have not yet been read by the MCU. The MCU reads the SIM_STS1 register bits 0 to 4 to access the pointer.

The SIM card controller also uses a configurable Rx interrupt threshold that can be configured by writing to the SIM_CTL1 register bits 0 to 3. This field specifies the number of unread data that should be available in the Rx FIFO before issuing an interrupt. Whenever the number of unread data exceeds this value, an interrupt is generated to the MCU. This interrupt is automatically cleared when the number of unread data in the Rx FIFO equals to or falls below the specified Rx interrupt threshold value.

6.12.4.4.3.5 Retransmission

The SIM card controller supports retransmission upon detecting an error condition. The SIM card controller checks the I/O line from the SIM card 11 bits after the start bit leading edge. If the detected I/O is a zero (error ACK), it assumes an error occurred and retransmits the byte. If the error ACK signal is repeated for the programmable number of times specified in the SIM_SHE register, The SIM card interface sets the bad Tx parity error bit in the status register (SIM_STS0 bit 3) and issues an interrupt.

For the transmission from the SIM card controller to the SIM card, when the SIM card controller detects a parity error following the transmission of a data byte, it performs the following sequence:

- The SIM card interface retransmits the data.
- If the retransmission succeeds, it ignores the initial failure.
- If the retransmission fails for the number of times specified in the programmable SIM_SHE register, the SIM card interface sets the bad parity bit interrupt the SIM_STS0 register, issues an interrupt to the MCU, and stops retransmission of the byte.

6.12.4.5 SIM Power Supply

VSIM is the power supply to the SIM card. During the activation/deactivation process, VSIM output is automatically controlled. The on/off of VSIM can also be controlled by directly programming the SIM_CTL0 register bit 7.

6.12.4.6 Unresponsive Card Detection

The SIM interface can detect an unresponsive card by means of a watchdog timer function, which determines the maximum allowable time that a data byte should take to arrive from the SIM card. The MCU can configure the watchdog timer by programming the SIM_WDT register. The watchdog timer can function in two modes: auto mode and single mode. In the auto mode, the watchdog timer is continuously enabled. In the single mode, the watchdog timer disables itself when a data byte is received from the card, or after it has timed out.

6.12.4.7 SIM Interface Watchdog

There are two separate watchdogs in SIM card module.

- One watchdog is used to report Rx idle for a preprogrammed time.
- The other watchdog is for time out when RX retransmission is on error.

6.12.4.8 SIM Interconnection

It is recommended to connect the SIM card as follows.

- Connect a 2.2 uF capacitor at VSIM.
- Connect a 10 kΩ resistor from SIMDA pin to VSIM.
- The driving strength setting on SIMRST, SIMCLK and SIMDA should be 00 (the default).

6.12.5 Control Registers

6.12.5.1 Memory map

ARM base address: 0x8500_0000 (SIM0) 0x8500_3000 (SIM1)

DSP base address 0x0000_0000

Offset Address	Name	Description
0x0000	SIM_TX	SIM card transmit register
0x0004	SIM_RX	SIM card receiver register
0x0008	SIM_STS0	SIM card status register 0
0x000c	SIM_STS1	SIM card status register 1
0x0010	SIM_IE	SIM card interrupt enable
0x0014	SIM_ICLR	SIM card interrupt clear
0x0018	SIM_CTL0	SIM card control register 0
0x001c	SIM_CTL1	SIM card control register 1
0x0020	SIM_RX_CK_DVD	SIM card RX clock divider control
0x0024	SIM_SEH	SIM card retransmit control
0x0028	SIM_TGC	SIM card turnaround guard control
0x002c	SIM_WDT	SIM card watchdog control
0x0030	SIM_INT_M	SIM card interrupt mask

Offset Address	Name	Description
0x0034	SIM_TX_CK_DVD	SIM card TX clock divider control
0x0038	SIM_WDT1	SIM card watchdog control 1

6.12.5.2 Register Descriptions

6.12.5.2.1 SIM_TX Registers

Description： SIM card transmit register

0x0000	Transmit Buffer register(Reset 0x0000)														SIM_TX	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								SIM_TX							
Type	RO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
SIM_TX	[7:0]	WO		Writing to this reg will send data to Tx FIFO and then the data get transmitted

6.12.5.2.2 SIM_RX Registers

Description： SIM card receiver register

0x0004	Receive Buffer register (Reset 0x0000)														SIM_RX	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								SIM_RX							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:8]	RO	24'h0	Reserved

SIM_RX	[7:0]	RO		Read from this address retrieve data from Rx FIFO

6.12.5.2.3 SIM_STS0 Registers

Description： SIM card status registers 0

0x0008	SIM Card Status Registers (Reset 0x0002)														SIM_STS0	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						RX_TOUT	ACTIVE_DONE	EARLY_ANS_TO_RST	CARD_OUT	CARD_IN	RX_TOUT_UNRESP	TX_PAR_ERR	RX_PAR_ERR	TX_FIFO_EMP	RX_FIFO_FULL
Type	RO						RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Field Name	Bit	R/W	Reset Value	Description
	[31:10]	RO	22'h0	Reserved
RX_TOUT	[9]	RO	1'h0	Int status bit to show Rx time out under idle state
ACT_DONE	[8]	RO	1'h0	Int status bit to show activation is done
EARLY_ANS_TO_RST	[7]	RO	1'h0	Int status bit for early answer to reset
CARD_OUT	[6]	RO	1'h0	Int status bit for card removed (not support in SC6820)
CARD_IN	[5]	RO	1'h0	Int status bit for card inserted (not support in SC6820)
RX_TOUT_UNRSP	[4]	RO	1'h0	Int status bit for Rx time out or card unresponsive
TX_PAR_ERR	[3]	RO	1'h0	Int status bit for Tx parity error
RX_PAR_ERR	[2]	RO	1'h0	Int status bit for Rx parity error
TX_FIFO_EPT	[1]	RO	1'h1	Tx FIFO data number bigger than tx_int_mark
RX_FIFO_FULL	[0]	RO	1'h0	Rx FIFO data number bigger than rx_int_mark

6.12.5.2.4 SIM_STS1 Registers

Description： SIM card status registers 1

0x000C	SIM Card Status Registers (Reset 0x0000)															SIM_STS1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		DEACTIVE_ON	ACTIVE_ON	SIM_ACTIVE_ST	SIM_DATA	CARD_INSERT	TX_FIFO_CNT					RX_FIFO_CNT				
Type		RO	RO	RO	RO	RO	RO					RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:15]	RO	17'h0	Reserved
DEACTIVE_ON	[14]	RO	1'h0	Busy in deactivation process
ACTIVE_ON	[13]	RO	1'h0	Busy in activation process
SIM_ATC_ST	[12]	RO	1'h0	Activation status, 1: activated; 0: not activated.
SIM_DATA	[11]	RO	1'h0	Reflect of sim data io pin
CARD_INSERT	[10]	RO	1'h0	Reflect of card in input pin (not support)
TX_FIFO_CNT	[9:5]	RO	5'h0	Tx FIFO data count, bit 9 used for debug only.
RX_FIFO_CNT	[4:0]	RO	5'h0	Rx FIFO data count, bit 4 used for debug only.

6.12.5.2.5 SIM_IE Registers

Description： SIM card interrupt enable

0x0010			SIM Card Interrupt Enable (Reset 0x0000)													SIM_IE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						RX_TOUT_IE	ACTIVE_DONE_IE	EARLY_ATR_IE	CARD_OUT_IE	CARD_IN_IE	UNRESP_IE	TX_PAR_ERR_IE	RX_PAR_ERR_IE	TX_EMP_IE	RX_FULL_IE
Type	RO						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

~~Field Name~~	Bit	R/W	Reset Value	Description
	[31:10]	RO	22'h0	Reserved
RX_TOUT_IE	[9]	R/W	1'h0	Enable bit for Rx time out
ACT_DONE_IE	[8]	R/W	1'h0	Enable bit for active done
EARLY_ATR_IE	[7]	R/W	1'h0	Enable bit for early answer to reset
CARD_OUT_IE	[6]	R/W	1'h0	Enable bit for card_out (not support in SC6820)
CARD_IN_IE	[5]	R/W	1'h0	Enable bit for card_in (not support in SC6820)
URSP_CARD_IE	[4]	R/W	1'h0	Enable bit for unresp_card
TX_PRT_ERR_IE	[3]	R/W	1'h0	Enable bit for tx_parity_error
RX_PRT_ERR_IE	[2]	R/W	1'h0	Enable bit for rx_parity_error
TX_EPT_IE	[1]	R/W	1'h0	Enable bit for Tx empty int
RX_FULL_IE	[0]	R/W	1'h0	Enable bit for Rx full int

6.12.5.2.6 SIM_ICLR Registers

Description: SIM card interrupt clear

0x0014			SIM Card Interrupt Clear (Reset 0x0000)													SIM_ICLR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						RX_TOUT_CLR	ACTIVE_DONE_CLR	EARLY_ATR_CLR	CARD_OUT_CLR	CARD_IN_CLR	UNRESP_CLR	TX_PAR_ERR_CLR	RX_PAR_ERR_CLR	TX_EMP_CLR	RX_FULL_CLR
Type	RO						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:10]	RO	22'h0	Reserved
RX_TOUT_CLR	[9]	WO	1'h0	Int clear bit for Rx time out
ACT_DONE_CLR	[8]	WO	1'h0	Int clear bit for active done
EARLY_ATR_CLR	[7]	WO	1'h0	Int clear bit for early answer to reset
CARD_OUT_CLR	[6]	WO	1'h0	Int clear bit for card_out (not support in SC6820)
CARD_IN_CLR	[5]	WO	1'h0	Int clear bit for card_in (not support in SC6820)
URSP_CARD_CLR	[4]	WO	1'h0	Int clear bit for unresp_card
TX_PRT_ERR_CLR	[3]	WO	1'h0	Int clear bit for tx_parity_error
RX_PRT_ERR_CLR	[2]	WO	1'h0	Int clear bit for rx_parity_error
TX_EPT_CLR	[1]	WO	1'h0	Int clear bit for Tx empty int
RX_FULL_CLR	[0]	WO	1'h0	Int clear bit for Rx full int

6.12.5.2.7 SIM_CTL0 Registers

Description: SIM card control registers 0

0x0018			SIM Card Control Registers 0 (Reset 0x0000)													SIM_CTL0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TX_DOUT_LOW	AUTO_ACT_DEACT	ACT_DEACT_EN	DO_DEACT	DO_ACT	TX_EN	RX_EN	CARD_OUT_LTCH	PWR_EN	SIM_RST	TX_FIFO_RST	RX_FIFO_RST	LOOPBACK_MODE	ODD_PAR	LOGIC_LEVEL	BIT_CONV
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
TX_DOUT_LOW	[15]	R/W	1'h0	Force the Tx data to low logic level.
AUTO_ACT_DEACT	[14]	R/W	1'h0	Enable the auto start of active/deactive when card_in or card_out happen
ACT_DEACT_EN	[13]	R/W	1'h0	Enable the active/deactive procedure
DO_DEACT	[12]	R/W	1'h0	Do deactivate operation
DO_ACT	[11]	R/W	1'h0	Do activate operation
TX_EN	[10]	R/W	1'h0	Enable the sim Tx
RX_EN	[9]	R/W	1'h0	Enable the sim Rx
CARD_OUT_LATCH	[8]	R/W	1'h0	This bit will be 1 if card_out happened (not support in SC6820)
POWER_EN	[7]	R/W	1'h0	Enable the Power supply to sim card
SIM_RST	[6]	R/W	1'h0	Reset the sim card module
TX_FIFO_RST	[5]	R/W	1'h0	Reset the Tx FIFO
RX_FIFO_RST	[4]	R/W	1'h0	Reset the Rx FIFO
LOOPBACK_MODE	[3]	R/W	1'h0	Transmit data looped back to receive.
ODD_PRT	[2]	R/W	1'h0	0: Even Parity 1: Odd Parity
LOGIC_LEVEL	[1]	R/W	1'h0	0: high logic level represent "0" 1: high logic level represent "1"
BIT_COVT	[0]	R/W	1'h0	Bit convention: 0: MSB (bit 7) transmitted first

				1: LSB (bit 0) transmitted first

6.12.5.2.8 SIM_CTL1 Registers

Description： SIM card control registers 1

0x001C			SIM Card Control Register 1 (Reset 0x0000)										SIM_CTL1			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	AD_SPD_CTRL			CLK_POL	CLK_EN	CLK_MODE			TX_INT_MARK				RX_INT_MARK			
Type	R/W			R/W	R/W	R/W			R/W				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16’h0	Reserved
AD_SPEED_CTL	[15:13]	R/W	3’h0	Control the speed of the active/deactive sequence. 0: slowest, 7: fastest.
CLK_POL	[12]	R/W	1’h0	Set the polarity of the sim_clk signal When the sim clk is stopped
CLK_EN	[11]	R/W	1’h0	Enable for the sim clk output
CLK_MODE	[10:8]	R/W	3’h0	Select the sim clk speed. The sim CLK is divided From the ARM bus clock: 0: ARM CLK/2 1: ARM CLK/4 2: ARM CLK/8 3: ARM CLK/16 4: ARM CLK/32 5: ARM CLK/64 6: ARM CLK/128 7: ARM CLK/256
TX_INT_MARK	[7:4]	R/W	4’h0	Tranmit_Int_WaterMark
RX_INT_MARK	[3:0]	R/W	4’h0	Receive_Int_WaterMark

6.12.5.2.9 SIM_RX_CK_DVD Registers

Description： SIM card RX clock divider control

0x0020	SIM Card RX Clock Divider Control (Reset 0x5952)													SIM_RX_CK_DVD		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SIM_RX_CLK_DIV															
Type	R/W															
Reset	0	1	0	1	1	0	0	1	0	1	0	1	0	0	1	0

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
SIM_RX_CK_DIV	[15:0]	R/W	16'h5952	Clock divider bit 0 to 15 for receiving data

6.12.5.2.10 SIM_SEH Registers

Description： SIM card retransmit control

0x0024	SIM Card Retransmit Control (Reset 0x0000)													SIM_SEH		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TX_ETU_SEL			Reserved	TX_DMA_SEL	RX_DMA_SEL	DMA_TX_EN	DMA_RX_EN	TX_RETRX_LMT				RX_RETRX_LMT			
Type	R/W			RO	R/W	R/W	R/W	R/W	R/W				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
TX_ETU_SEL	[15:13]	R/W	3'h0	Select the Tx etu divider: 0x111: the Tx etu is decided by sim_tx_clock_divider at address 0x0034 Others: the Tx etu is the same as Rx etu.
	[12]	RO	1'h0	Reserved
TX_DMA_SEL	[11]	R/W	1'h0	In TX mode, once TX FIFO empty, whether DMA request keep its value until DMA

				acknowledge is arrived or not 0: keep 1: not keep
RX_DMA_SEL	[10]	R/W	1'h0	In RX mode, once RX FIFO full, whether DMA request keep its value until DMA acknowledge is arrived or not 0: keep 1: not keep
DMA_TX_EN	[9]	R/W	1'h0	TX DMA mode enable
DMA_RX_EN	[8]	R/W	1'h0	RX DMA mode enable
TX_RETRX_LMT	[7:4]	R/W	4'h0	Tx retransmit limit
RX_RETRX_LMT	[3:0]	R/W	4'h0	Rx retransmit limit

6.12.5.2.11 SIM_TGC Registers

Description： SIM card turnaround guard control

0x0028	SIM Card Turnaround Guard Control (Reset 0x3030)														SIM_TGC	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TGC_TIME								GUARD_TIME							
Type	R/W								R/W							
Reset	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
TGC_TIME	[15:8]	R/W	8'h30	Times in bit unit between the Rx and Tx.
GUARD_TIME	[7:0]	R/W	8'h30	Times in bit unit between the consecutive byte during data transmission to the SIM card.

6.12.5.2.12 SIM_WDT Registers

Description： SIM card watchdog control

0x002C			SIM Card Watchdog Control (Reset 0x0802)												SIM_WDT	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	WDOG_CNT_LMT														WDOG_RTX_TOUT_EN	WDOG_RX_TOUT_EN
Type	R/W														R/W	R/W
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
WDOG_CNT_LMT	[15:2]	R/W	14'h200	Watch dog timer limit for Rx retransmit watch dog
WDOG_RTX_TOUT_EN	[1]	R/W	1'h1	Enable the Rx retransmit watch dog timer. This timer watches when Rx re-transition is happening and it will flag the unresponsive card int when the data from the sim card is time out (no data comes back)
WDOG_RX_TOUT_EN	[0]	RW	1'h0	Enable the Rx time out watch dog

6.12.5.2.13 SIM_INT_M Registers

Description： SIM card interrupt mask

0x0030			SIM Card Interrupt Mask (Reset 0x0000)													SIM_INT_M
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						RX_TOUT_MSK	ACTIVE_DONE_MSK	EARLY_ATR_MSK	CARD_OUT_MSK	CARD_IN_MSK	UNRESP_MSK	TX_PAR_ERR_MSK	RX_PAR_ERR_MSK	TX_EMP_MSK	RX_FULL_MSK
Type	RO						RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:10]	RO	22'h0	Reserved
RX_TOUT_MSK	[9]	RO	1'h0	Masked Int status bit to show Rx time out under idle state
ACT_DONE_MSK	[8]	RO	1'h0	Masked int bit for active done
EATR_MSK	[7]	RO	1'h0	Masked int bit for early answer to reset
CARD_OUT_MSK	[6]	RO	1'h0	Masked int bit for card_out
CARD_IN_MSK	[5]	RO	1'h0	Masked int bit for card_in
URSP_CARD_MSK	[4]	RO	1'h0	Masked int bit for unresp_card
TX_PRT_ERR_MSK	[3]	RO	1'h0	Masked int bit for Tx_parity_error
RX_PRT_ERR_MSK	[2]	RO	1'h0	Masked int bit for Rx_parity_error
TX_EMP_MSK	[1]	RO	1'h0	Masked int bit for Tx empty int
RX_FULL_MSK	[0]	RO	1'h0	Masked int bit for Rx full int

6.12.5.2.14 SIM_TX_CK_DVD Registers

Description: SIM card TX clock divider control

0x0034			SIM Card TX Clock Divider Control (Reset 0x5952)													SIM_TX_CK_DVD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SIM_TX_CLK_DIV															
Type	R/W															
Reset	0	1	0	1	1	0	0	1	0	1	0	1	0	0	1	0

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
SIM_TX_CK_DIV	[15:0]	R/W	16'h5952	Clock divider bit 0 to 15 for Tx data

6.12.5.2.15 SIM_WDT1 Registers

Description： SIM card watchdog control 1

0x0038			SIM Card Watchdog Control 1(Reset 0x0200)													SIM_WDT1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		SIM_WDT1													
Type	RO		R/W													
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:14]	RO	18'h0	Reserved
SIM_WDT1	[13:0]	R/W	14'h200	Watch dog count limit for Rx time out.

6.12.6 Application Notes

1. SC6820 have 2 hardware sim controllers, and it can be act as 4 software controllers.
2. Hardware SIM0 act as software sim0 & sim2; Hardware SIM1 act as software sim1 & sim3
3. To reset simcard, software should write 32'h8B00_004C bit 5 for SIM0, bit 6 for SIM1
4. To enable SIM0/SIM1 interrupt, software should write 32'h20A0_0010 bit 12 for SIM0 and SIM1

5. To configure the clock plority when sim clock is stop, software should write 32'h8C00_0000 bit[19] for sim0,

bit[20] for sim1, bit[30] for sim2, bit[31] for sim3

6. To enable simcard, software should write 32'h8B00_0008 bit[3] for SIM0, bit[16] for SIM1.

7. To switch the sim0/sim2 of SIM0, or sim1/sim3 of SIM1, software should first open the pin reg write property by

wirte 32'h8B00_0008 bit[13], then write bit[4] 0 for SIM0's sim0, 1 for SIM0's sim2;

write bit[5] 0 for SIM1's sim1, 1 for SIM1's sim3.

8. after all of this register are configured, the software can configure the sim internal registers.

6.13 SDIO Host Controller

6.13.1Overview

The SD/SDIO Host Controller is a Host Controller with an ARM processor interface. The SDIO Host Controller handles SD/SDIO Protocol at transmission level, packing data, adding cyclic redundancy check (CRC), start/end bit, and checking for transaction format correctness.

6.13.2Features

- Meets SD Host Controller Standard Specification Draft Version 1.0
- Meets SDIO card specification version 1.0.
- Meets SD Memory Card Security Specification version 1.01.
- Supports both DMA and Non-DMA mode of operation
- Host clock rate variable between 0 and 48 MHz
- Supports 1 bit, 4 bit SD modes.
- Allows card to interrupt host in 1bit, 4 bit SD modes.
- Upto 10Mbytes per second read and write rates using 4 parallel data lines (sd4 bit mode)
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity
- Designed to work with I/O cards, Read-only cards and Read/Write cards.
- Supports Read wait Control, Suspend/Resume operation.
- Supports FIFO Overrun and Underrun condition by stopping SD clock
- Conforms to AMBA specification AHB (2.0)

6.13.3Signal Description

The connection of SDIO host PADs is shown in the following figure.

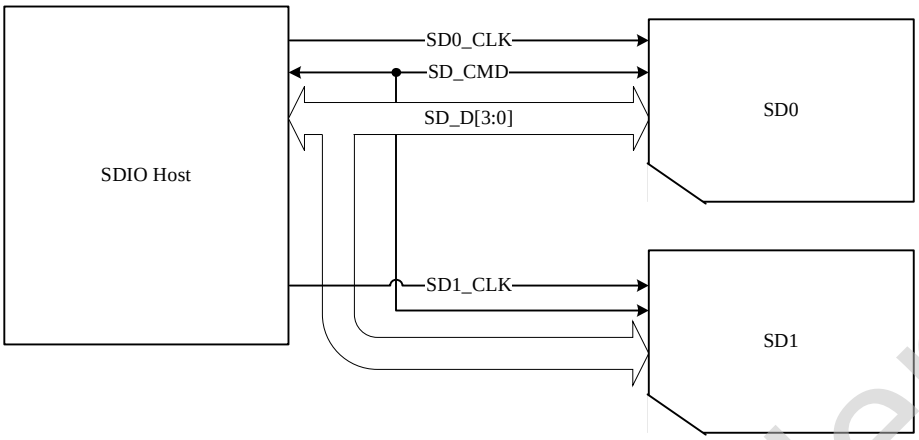


Figure 6-56 SDIO Host connection

6.13.4Function Description

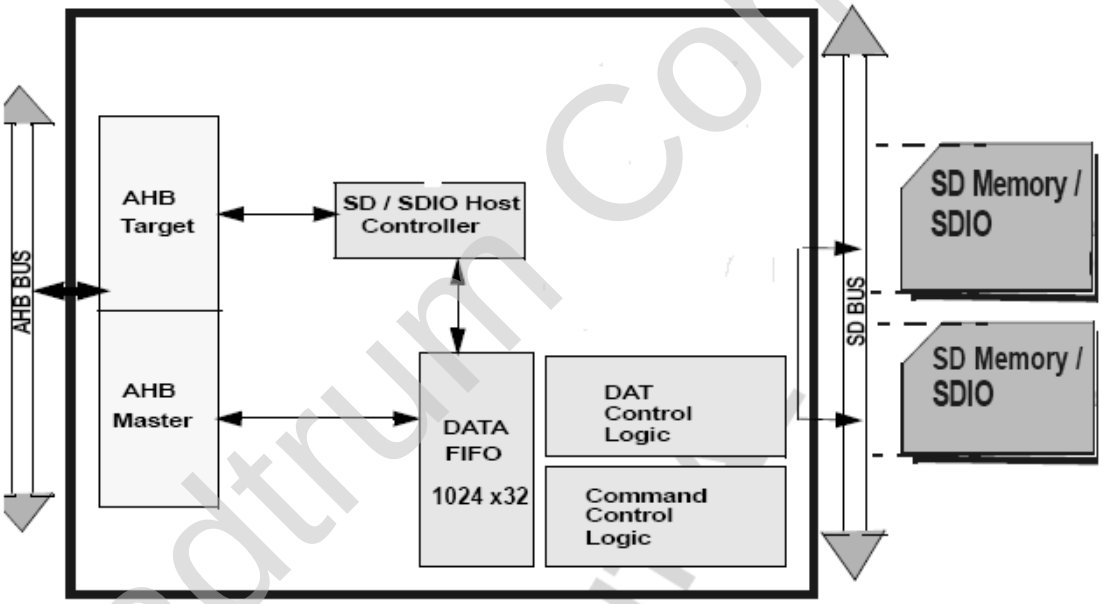


Figure 6-57 Function Block Diagram

6.13.4.1 AHB Master

The AHB master initiates a read or write transaction with the memory if the Data transaction is done using DMA data transfer method.

6.13.4.2 AHB Target

The AHB target is having the SD/SDIO control registers and these registers are programmed by the ARM processor through the AHB target interface. The data transaction is performed through the AHB target interface in case of Programmed IO method of data transfer.

6.13.4.3 SD/SDIO Host Controller

The SD/SDIO Host Controller comprises of Host_AHB interface, SD/SDIO controller registers, Bus monitor, Clk_gen, CRC generator and checker (CRC7 and CRC16),. The Host_AHB interface acts as the bridge between the ARM processor and Host Controller. The SD/SDIO controller registers are programmed by the ARM processor through AHB target interface. Interrupts are generated to the ARM processor based on the values set in the Interrupt status register and Interrupt enable registers. Bus monitor will check for any violations occurring in the SD bus and time-out conditions.

The Clock generation block will generate the SD clock depending on the value programmed by the ARM processor in the Clock Control Register. The CRC7 and CRC16 generator calculate the CRC for command and Data respectively to send the CRC to the SD/SDIO card. The CRC7 and CRC16 checker checks for any CRC error in the Response and Data send by the SD/SDIO card.

6.13.5Control Registers

6.13.5.1 Memory map

ARM base address: 0x2090_0000

Offset Address	Name	Description
0x0000	SYS_ADDR	System address
0x0004	BLK_SIZE	Block size and count
0x0008	ARG	Argument
0x000C	TR_MODE	Transfer mode and command
0x0010	RESP0	Response 0, 1
0x0014	RESP2	Response 2, 3
0x0018	RESP4	Response 4, 5
0x001C	RESP6	Response 6, 7
0x0020	BUF_PRT	Buffer data port
0x0024	PRES_STATE	Present state
0x0028	SD_CTRL1	SD Control Register1
0x002C	SD_CTRL2	SD Control Register2
0x0030	INT_ST	Normal and error interrupt status
0x0034	INT_ST_EN	Interrupt status enable
0x0038	INT_SIG_EN	Interrupt signal enable
0x003C	CMD12_ST	Auto CMD12 error status
0x0040	CAP1	Capabilities 1
0x0044	CAP2	Capabilities 2 (reserved)
0x0048	MAX_CUR_CAP1	Maximum current capabilities 1
0x004C	MAX_CUR_CAP2	Maximum current capabilities 2 (reserved)
…	…	…
0x002C	SLT_INT_ST	Slot interrupt status and version number

Note:

The SD host controller registers given above are for Slot 1. The same set of registers is used for Slot 2.

Address range for Slot 1: 0x0000 ~ 0x00FF

Address range for Slot 2: 0x0100 ~ 0x01FF

6.13.5.2 Register Descriptions

6.13.5.2.1 SYS_ADDR

Description：DMA system address

0x0000	System Address (reset 0x0000_0000)												SYS_ADDR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DMA_SYS_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DMA_SYS_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
DMA_SYS_ADDR	[31:0]	R/W	32'h0	This register contains the system memory address for a DMA transfer. When the Host Controller (HC) stops a DMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during a transfer return an invalid value. The Host Driver (HD) shall initialize this register before starting a DMA transaction. After DMA has stopped, the next system address of the next contiguous data position can be read from this register. The DMA transfer waits at every boundary specified by the **Host DMA Buffer Size** in the Block Size register. The Host Controller generates DMA **Interrupt** to request to update this register. The HD set the next system address of the next data position to this register. When most upper byte of this register (0x0003) is written, the HC restarts the DMA transfer. When restarting DMA by the resume command or by setting **Continue Request** in the Block Gap Control register, the HC shall start at the next contiguous address stored here in the System Address register

6.13.5.2.2 BLK_SIZE

Description：Block Size and Count

0x0004			Block Size and Count (reset 0x0000_0000)										BLK_SIZE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	BLK_CNT															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TR_BLK_SIZE	HST_DMA_BUF_SIZE			TR_BLK_SIZE											
Type	R/W	R/W			R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
BLK_CNT	[31:16]	R/W	16'h0	Block count. This register is enabled when **Block Count Enable** in the Transfer Mode register is set to 1 and is valid only for multiple block transfers. The HC decrements the block count after each block transfer and stops when the count reaches zero. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored. When saving transfer context as a result of Suspend command, the number of blocks yet to be transferred can be determined by reading this register. When restoring transfer context prior to issuing a Resume command, the HD shall restore the previously saved block count.0x0000: stop count0x0001: 1 block0x0002: 2 blocks…0xFFFF: 65535 blocks
TR_BLK_SIZE	[15]	R/W	1'h0	Transfer block size bit [12]. This bit is added to support 4 kb data block transfer.
HST_DMA_BUF_SIZE	[14:12]	R/W	3'h0	Host DMA buffer size. To perform long DMA transfer, System Address register shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at every boundary specified by these fields and the HC generates the **DMA Interrupt** to request the HD to update the System Address register. These bits shall be used when the **DMA Support** in the Capabilities register is set to 1 and this function is active when the **DMA Enable** in the Transfer Mode register is set to 1. 000: 4 KB (detect A11 carry out) 001: 8 KB (detect A11 carry out) 010: 16 KB (detect A11 carry out)

				011: 32 KB (detect A11 carry out) 100: 64 KB (detect A11 carry out) 101: 128 KB (detect A11 carry out) 110: 256 KB (detect A11 carry out) 111: no limit, HC will not generate the DMA interrupt
TR_BLK_SIZE	[11:0]	R/W	12'h0	Transfer block size. This register specifies the block size for block data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored. 0x0000: no data transfer 0x0001: 1 byte 0x0002: 2 bytes … 0x0200: 512 bytes

6.13.5.2.3 TR_MODE

Description：Transfer mode and command

0x000C			Transfer mode and command (reset 0x0000_0000)										TR_MODE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved		CMD_INDEX						CMD_TYPE		DATA_PRE_SEL	CMD_IND_CHK_EN	CMD_CRC_CHK_EN	Reserved	RESP_TYPE_SEL	
Type	RO		R/W						R/W		R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved									CMD_COMP_ATA	MULT_BLK_SEL	DATA_DIR_SEL	Reserved	AUTO_CMD12_EN	BLK_CNT_EN	DMA_EN
Type	RO									R/W	R/W	R/W	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:30]	RO	2'h0	Reserved
CMD_INDEX	[29:24]	R/W	6'h0	Command index, set to the command number (CMD0-63, ACMD0-63)
CMD_TYPE	[23:22]	R/W	2'h0	Commend type. There are three types of special commands, Suspend, Resume and Abort. These bits shall bet set to 00b for all other commands. 00: Normal 01: Suspend

				10: Resume 11: Abort
DATA_PRE_SEL	[21]	R/W	1'h0	Data present select 0: no data present 1: data present This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: 1. Commands using only CMD line (e.g., CMD52) 2. Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b, e.g., CMD38) 3. Resume Command
CMD_IND_CHK_EN	[20]	R/W	1'h0	Command index check enable 0: disable 1: enable If this bit is set to 1, the HC shall check the index field in the Response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked.
CMD_CRC_CHK_EN	[19]	R/W	1'h0	Command CRC check enable 0: disable 1: enable If this bit is set to 1, the HC shall check the CRC field in the Response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked.
	[18]	R/W	1'h0	Reserved
RESP_TYPE_SEL	[17:16]	R/W	2'h0	Response type select 00: no response 01: response length 136 10: response length 48 11: response length 48, check Busy after response
	[15:7]	R/W	9'h0	Reserved
CMD_COMP_ATA	[6]	R/W	1'h0	Command completion signal enable for CE-ATA device 0: device will not send command completion signal 1: device will send command completion signal
MULT_BLK_SEL	[5]	R/W	1'h0	Multiple/single block select 0: single block 1: multiple blocks
DATA_DIR_SEL	[4]	R/W	1'h0	Data transfer direction select 0: write (Host to Card) 1: read (Card to Host)

	[3]	R/W	1'h0	Reserved
AUTO_CMD12_EN	[2]	R/W	1'h0	Auto CMD12 enable 0: disable 1: enable Multiple block transfers for memory require CMD12 to stop the transaction. When this bit is set to 1, the HC shall issue CMD12 automatically when last block transfer is completed. The HD shall not set this bit to issue commands that do not require CMD12 to stop data transfer.
BLK_CNT_EN	[1]	R/W	1'h0	Block count enable 0: disable 1: enable This bit is used to enable the Block count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer.
DMA_EN	[0]	R/W	1'h0	DMA enable 0: disable 1: enable DMA can be enabled only if **DMA Support** bit in the Capabilities register is set. If this bit is set to 1, a DMA operation shall begin when the HD writes to the upper byte of Command register (0x000F).

6.13.5.2.4 RESPONSE

Description：Response 0, 1, 2, 3, 4, 5, 6, and 7

0x0010			Response 0 and 1 (reset 0x0000_0000)													RESP0&1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	RESPONSE [31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RESPONSE [15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x0014	Response 2 and 3 (reset 0x0000_0000)															RESP2&3
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	RESPONSE [63:48]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RESPONSE [47:32]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x0018	Response 4 and 5 (reset 0x0000_0000)															RESP4&5
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	RESPONSE [95:80]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RESPONSE [79:64]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x001C	Response 6 and 7 (reset 0x0000_0000)															RESP6&7
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	RESPONSE [127:112]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RESPONSE [111:96]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
RESPONSE	[127:0]	RO	128'h0	The following table describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[ ] refers to a bit range within the response data as transmitted on the SD Bus, and REP[ ] refers to a bit range within the Response register.

6.13.5.2.5 BUF_PRT

Description：Buffer Data Port

0x0020	Buffer Data Port (reset 0x0000_0000)												BUF_PRT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	BUF_DATA															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BUF_DATA															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
BUF_DATA	[31:0]	R/W	32'h0	The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

6.13.5.2.6 PRES_STATE

Description：Present State

0x0024	Present State (reset 0x01f0_0000)												PRES_STATE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved							CMD_SIG_LVL	DAT3_0_SIG_LVL				Reserved			
Type	RO							RO	RO				RO			
Reset	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				BUF_READ_EN	BUF_WR_EN	READ_ACTIVE	WRITE_ACTIVE	Reserved					DAT_LINE_ACTRIVE	CMD_INH_DAT	CMD_INH_CMD
Type	RO				RO	RO	RO	RO	RO					RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:25]	RO	7'h0	Reserved
CMD_SIG_LVL	[24]	RO	1'h0	CMD line signal level. This status is used to check **CMD** line level to recover from errors, and for debugging.
DAT3_0_SIG_LVL	[23:20]	RO	4'h0	DAT [3:0] line signal level. This status is used to check **DAT** line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT [0].

				[23]: for DAT[3] [22]: for DAT[2] [21]: for DAT[1] [20]: for DAT[0]
	[19:12]	RO	8'h0	Reserved
BUF_READ_EN	[11]	RO	1'h0	Buffer read enable. This status is used for non-DMA read transfers. This read only flag indicates that valid data exists in the Host side buffer. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when all the block data is ready in the buffer and the **Buffer Read Ready** Interrupt is generated. 0: read disable 1: read enable
BUF_WR_EN	[10]	RO	1'h0	Buffer write enable. This status is used for non-DMA write transfers. This write only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer. A change of this bit from 0 to 1 occurs when top of block data can be written to the buffer and the **Buffer Write Ready** Interrupt is generated. 0: write disable 1: write enable
READ_ACTIVE	[9]	RO	1'h0	Read transfer active. This status is used for detecting completion of a read transfer. This bit is set to 1 for either of the following conditions: 1. After the end bit of the read command 2. When writing a 1 to continue Request in the Block Gap Control register to restart a read transfer This bit is cleared to 0 for either of the following conditions: 1. When the last data block as specified by block length is transferred to the system. 2. When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop at Block Gap Request set to 1. A transfer complete interrupt is generated when this bit changes to 0. 0: no valid data 1: transferring data
WRITE_ACITVE	[8]	RO	1'h0	Write transfer active. This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the HC. This bit is set in either of the following cases: 1. After the end bit of the write com mand 2. When writing a 1 to Continue Request in the Block Gap Control register to restart a write

				transfer This bit is cleared in either of the following cases: 1. After getting the CRC status of the last data block as specified by the t ransfer count (Single or Multiple) 2. After getting a CRC status of any block where data transmission is about to be stopped by a Stop at Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as a result of the Stop at Block Gap Request being set. This status is useful for the HD in determining when to issue commands during write busy. 0: no valid data 1: transferring data
	[7:3]	RO	5'h0	Reserved
DAT_LINE_ACTIVE	[2]	RO	1'h0	DAT line active. This bit indicates whether one of the **DAT** line on SD bus is in use. 0: DAT line inactive 1: DAT line active
CMD_INH_DAT	[1]	RO	1'h0	Command inhibit (DAT) This status bit is generated if either the **DAT Line Active** or the **Read Transfer Active** is 1. If this bit is 0, it indicates the HC can issue the next SD command. Commands with busy signal belong to **Command Inhibit (DAT)** (e.g., R1b, R5b type). Changing from 1 to 0 generates a **Transfer Complete** interrupt in the Normal Interrupt status register.Note: The SD Host Driver can save registers in the range of 0x0000 ~ 0x000D for a suspend transaction after this bit has changed from 1 to 0. 0: can issue command that uses the DAT line 1: cannot issue command that uses the DAT line
CMD_INH_CMD	[0]	RO	1'h0	Command inhibit (CMD) If this bit is 0, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after the Command register (0x000F) is written. This bit is cleared when the command response is received. Even if the Command Inhibit (DAT) is set to 1, Commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a Command complete interrupt in the Normal Interrupt Status register. If the HC cannot issue the command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1 and the Command Complete is not set. Status issuing Auto CMD12 is not read from this bit.

6.13.5.2.7 SD_CTRL1

Description：SD Control Register1

0x0028	SD Control Register1 (reset 0x0000_0000)															SD_CTRL1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved					WK_EN_CRD_REM	WK_EN_CRD_INS	CMD_SIG_LVL	Reserved				INT_AT_BLK_GAP	RD_WAIT_CTRL	CONT_REQUEST	STP_AT_BLK_GAP_REQ
Type	RO					R/W	R/W	R/W	RO				R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							SD_BUS_PWR	Reserved					HI_SPD_EN	SD4B_MODE	Reserved
Type	RO							R/W	RO					R/W	R/W	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:27]	RO	5'h0	Reserved
WK_EN_CRD_REM	[26]	R/W	1'h0	Wakeup event enable on SD card removal. This bit enables wakeup event via **Card Removal** assertion in the Normal Interrupt Status register. **FN_WUS** (Wakeup Support) in CIS does not affect this bit. 0: disable 1: enable
WK_EN_CRD_INS	[25]	R/W	1'h0	Wakeup event enable on SD card insertion. This bit enables wakeup event via **Card Insertion** assertion in the Normal Interrupt Status register. **FN_WUS** (Wakeup Support) in CIS does not affect this bit. 0: disable 1: enable
WK_EN_CRD_INT	[24]	R/W	1'h0	Wakeup event enable on SD card interrupt. This bit enables wakeup event via **Card Interrupt** assertion in the Normal Interrupt Status register. This bit can be set to 1 if FN_WUS (Wakeup Support) in CIS is set to 1. 0: disable 1: enable
	[23:20]	RO	4'h0	Reserved
INT_AT_BLK_GAP	[19]	R/W	1'h0	Interrupt at block gap. This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. If the SD card cannot signal an interrupt during a multiple

				block transfer, this bit should be set to 0. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card.
RD_WAIT_CTRL	[18]	R/W	1'h0	Read wait control. The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise, the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1 or DAT line conflict may occur. If this bit is set to 0, Suspend/Resume cannot be supported. 0: disable read wait control 1: enable read wait control
CONT_REQUEST	[17]	R/W	1'h0	Continue request. This bit is used to restart a transaction that was stopped using the Stop at Block Gap Request. To cancel stop at the block gap, set Stop at Block Gap Request to 0 and set this bit to restart the transfer. The HC automatically clears this bit in either of the following cases: 1. In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts 2. In the case of a write transaction, the Write transfer active changes from 0 to 1 as the write transaction restarts Therefore it is not necessary for Host driver to set this bit to 0. If Stop at Block Gap Request is set to 1, any write to this bit is ignored. 0: ignored 1: restart
STP_AT_BLK_GAP_REQ	[16]	R/W	1'h0	Stop at block gap request. This bit is used to stop executing a transaction at the next block gap for both DMA and non-DMA transfers. Until the transfer complete is set to 1, indicating a transfer completion, the HD shall leave this bit set to 1. Clearing both the Stop at Block Gap Request and Continue Request shall not cause the transaction to restart. Read Wait is used to stop the read transaction at the block gap. The HC shall honor Stop at Block Gap Request for write transfers, but for read transfers it requires that the SD card support Read Wait. Therefore the HD shall not set this bit during read transfers unless the SD card supports Read Wait and has set Read Wait Control to 1. In case of write transfers in which the HD writes data to the Buffer Data Port register,

				the HD shall set this bit after all block data is written. If this bit is set to 1, the HD shall not write data to Buffer data port register. This bit affects Read Transfer Active, Write Transfer Active, DAT line active and Command Inhibit (DAT) in the Present State register. 0: transfer 1: stop
	[15:9]	RO	7'h0	Reserved
SD_BUS_PWR	[8]	R/W	1'h0	SD bus power. Before setting this bit, the SD host driver shall set SD Bus Voltage Select. If the HC detects the No Card State, this bit shall be cleared. 0: power off 1: power on
	[7:3]	RO	5'h0	Reserved
HI_SPD_EN	[2]	R/W	1'h0	High speed enable. This bit is optional. Before setting this bit, the HD shall check the **High Speed Support** in the Capabilities register. If this bit is set to 0 (default), the HC outputs **CMD** line and **DAT** line at the falling edge of the SD clock (up to 25 MHz). If this bit is set to 1, the HC outputs **CMD** line and **DAT** line at the rising edge of the SD clock (up to 50 MHz). 0: normal speed mode 1: high speed mode
SD4B_MODE	[1]	R/W	1'h0	Data transfer width, SD1 or SD4. This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. 0: 1-bit mode 1: 4-bit mode
	[0]	RO	1'h0	Reserved

6.13.5.2.8 SD_CTRL2

Description：SD Control Register2

0x002C			SD Control Register2 (reset 0x0000_0000)													SD_CTRL2
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved					SW_RST_DAT	SW_RST_CMD	SW_RST_ALL	Reserved				DATA_TIMEOUT_CNT			
Type	RO					R/W	R/W	R/W	RO				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SDCLK_FRQ_SEL								Reserved					SDCLK_EN	INT_CLK_STABLE	INT_CLK_EN
Type	R/W								RO					R/W	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:27]	RO	5'h0	Reserved
SW_RST_DAT	[26]	R/W	1'h0	Software reset for DAT line. Only part of data circuit is reset. DMA circuit is also reset. The following registers and bits are cleared by this bit: • Buffer Data Port Register: ¡ Buffer is cleared and initialized. • Present State register: ¡ Buffer Read Enable ¡ Buffer Write Enable ¡ Read Transfer Active ¡ Write Transfer Active ¡ DAT Line Active ¡ Command Inhibit (DAT) • Block Gap Control register: ¡ Continue Request ¡ Stop At Block Gap Request • Normal Interrupt Status register ¡ Buffer Read Ready ¡ Buffer Write Ready ¡ Block Gap Event Transfer Complete 0: work 1: reset
SW_RST_CMD	[25]	R/W	1'h0	Software reset for CMD line. Only part of command circuit is reset. The following registers and bits are cleared by this bit: • Present State register ¡ Command Inhibit (CMD) • Normal Interrupt Status register ¡ Command Complete

				0: work 1: reset
SW_RST_ALL	[24]	R/W	1'h0	Software reset for all. This reset affects the entire HC except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0. During its initialization, the HD shall set this bit to 1 to reset the HC. The HC shall reset this bit to 0 when Capabilities registers are valid and the HD can read them. Additional use of **Software Reset for All** may not affect the value of the Capabilities registers. If this bit is set to 1, the SD card shall reset itself and must be reinitialized by the HD. 0: work 1: reset
	[23:20]	RO	4'h0	Reserved
DATA_TIMEOUT_CNT	[19:16]	R/W	4'h0	Data timeout counter value. This value determines the interval by which DAT line timeouts are detected. Refer to the **Data Timeout Error** in the Error Interrupt Status register for information on factors that dictate timeout generation. Timeout clock frequency will be generated by dividing the base clock TMCLK by this value. When setting this register, prevent inadvertent timeout events by clearing the **Data Timeout Error Status Enable** (in the Error Interrupt Status Enable register). 0000: TMCLK * 2^(13) 0001: TMCLK * 2^(14) … 1110: TMCLK * 2^(27) 1111: reserved
SDCLK_FRQ_SEL	[15:8]	R/W	8'h0	SD clock frequency select. This register is used to select the frequency of the **SDCLK** pin. The frequency is not programmed directly; rather this register holds the divisor of the **Base Clock Frequency for SD clock** in the Capabilities register. Only the following settings are allowed. 0x00: base clock (10~63 MHz) 0x01: base clock divided by 2 0x02: base clock divided by 4 0x04: base clock divided by 8 0x08: base clock divided by 16 0x10: base clock divided by 32 0x20: base clock divided by 64 0x40: base clock divided by 128 0x80: base clock divided by 256 Setting 0x00 specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor,

				but multiple bits should not be set. The two default divider values can be calculated by the frequency that is defined by the **Base Clock Frequency for SD Clock** in the Capabilities register. 1. 25 MHz divider value 2. 400 kHz divider value The frequency of the SDCLK is set by the following formula: Clock Frequency = (Base clock) / divisor Thus choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency.
	[7:3]	RO	5'h0	Reserved
SDCLK_EN	[2]	R/W	1'h0	SD clock enable. The HC shall stop **SDCLK** when writing this bit to 0. **SDCLK Frequency Select** can be changed when this bit is 0. Then, the HC shall maintain the same clock frequency until **SDCLK** is stopped (stop at **SDCLK** = 0). If the HC detects the No Card state, this bit shall be cleared. 0: disable 1: enable
INT_CLK_STABLE	[1]	RO	1'h0	Internal clock stable. This bit is set to 1 when SD clock is stable after writing to **Internal Clock Enable** in this register to 1. The SD Host Driver shall wait to set **SD Clock Enable** until this bit is 1.Note: This is useful when using PLL for a clock oscillator that requires setup time. 0: not ready 1: ready
INT_CLK_EN	[0]	R/W	1'h0	Internal clock enable. This bit is set to 0 when the HD is not using the HC or the HC awaits a wakeup event. The HC should stop its internal clock to go to the very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1. When clock oscillation is stable, the HC shall set **Internal Clock Stable** in this register to 1. This bit shall not affect card detection. 0: stop 1: oscillate

6.13.5.2.9 INT_ST

Description：Normal and error interrupt status

0x0030	Normal and error interrupt status (reset 0x0000_0000)												INT_ST			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	VNDR_ERR_ST			TRGT_RESP_ERR	Reserved			SW_RST_ALL	AUTO_CMD12_ERR	CUR_LMT_ERR	DATA_END_BIT_ERR	DATA_CRC_ERR	DATA_TIMEOUT_ERR	CMD_IND_ERR	CMD_END_BIT_ERR	CMD_CRC_ERR
Type	R/W			R/W	RO			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ERR_INT	Reserved						CARD_INT	Reserved		BUF_READ_RDY	BUF_WRITE_RDY	DMA_INT	BLK_GAP_EVNT	TR_COMPLETE	CMD_COMPLETE
Type	RO	RO						R/W	RO		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:

Read-only status, write 1 to clear status: register bits indicate status when read, a set bit indicating a event may be cleared by writing 1, Writing 0 has no effect

Field Name	Bit	Type	Reset Value	Description
VNDR_ERR_ST	[31:29]	R/W	3'h0	Vender specified error status. Additional status bits can be defined in this register by the vendor.
TRGT_RESP_ERR	[28]	R/W	1'h0	Target response error status. This occurs when detecting error in m_hresp. 0: no error 1: error
	[27:25]	RO	3'h0	Reserved
AUTO_CMD12_ERR	[24]	R/W	1'h0	Auto CMD12 error. This occurs when detecting that one of the bits in Auto CMD12 Error Status register has changed from 0 to 1. This bit is set to 1 also when Auto CMD12 is not executed due to the previous command error. 0: no error 1: error
CUR_LMT_ERR	[23]	R/W	1'h0	Current limit error. By setting the **SD Bus Power** bit in the Power Control Register, the HC is requested to supply power for the SD Bus. If the HC supports the Current Limit Function, it can be protected from an illegal card by stopping power supply to the card in which case this bit indicates a failure status. Reading 1 means the HC is not supplying power to SD card due to some failure. Reading 0 means that the HC is supplying power and no error has occurred. This bit shall always set to be 0, if the HC does not support this function.

				0: no error 1: power failure
DATA_END_BIT_ERR	[22]	R/W	1'h0	Data end bit error. This occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status. 0: no error 1: error
DATA_CRC_ERR	[21]	R/W	1'h0	Data CRC error. This occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than "010". 0: no error 1: error
DATA_TIMEOUT_ERR	[20]	R/W	1'h0	Data timeout error. This occurs when detecting one of the following timeout conditions. 1. Busy Timeout for R1b, R5b type 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout 0: no error 1: timeout
CMD_IND_ERR	[19]	R/W	1'h0	Command index error. This occurs if a Command Index error occurs in the Command Response. 0: no error 1: error
CMD_END_BIT_ERR	[18]	R/W	1'h0	Command end bit error. This occurs when detecting that the end bit of a command response is 0. 0: no error 1: end bit error generated
CMD_CRC_ERROR	[17]	R/W	1'h0	Command CRC error. Command CRC Error is generated in two cases. 1. If a response is returned and the Command Timeout Error is set to 0, this bit is set to 1 when detecting a CRC error in the command response 2. The HC detects a CMD line conflict by monitoring the CMD line when a command is issued. If the HC drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SDCLK edge, then the HC shall abort the command (stop driving CMD line) and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict. 0: no error 1: CRC error generated
CMD_TIMEOUT_ERR	[16]	R/W	1'h0	Command timeout error. This occurs only if the

				no response is returned within 64 **SDCLK** cycles from the end bit of the command. If the HC detects a **CMD** line conflict, in which case **Command CRC Error** shall also be set. This bit shall be set without waiting for 64 **SDCLK** cycles because the command will be aborted by the HC. 0: no error 1: timeout
ERR_INT	[15]	RO	1'h0	Vender specified error status. Additional status bits can be defined in this register by the vendor.
	[14:9]	RO	6'h0	Reserved
CARD_INT	[8]	R/W	1'h0	Card interrupt. Writing this bit to 1 does not clear this bit. It is cleared by resetting the SD card interrupt factor. In 1-bit mode, the HC shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the card and the interrupt to the Host system. When this status has been set and the HD needs to start this interrupt service, Card Interrupt Status Enable in the Normal Interrupt Status register shall be set to 0 in order to clear the card interrupt statuses latched in the HC and stop driving the Host System. After completion of the card interrupt service (the reset factor in the SD card and the interrupt signal may not be asserted), set Card Interrupt Status Enable to 1 and start sampling the interrupt signal again. 0: no card interrupt 1: card interrupt generated
	[7:6]	RO	2'h0	Reserved
BUF_READ_RDY	[5]	R/W	1'h0	Buffer read ready. This status is set if the Buffer Read Enable changes from 0 to 1. 0: not ready to read buffer 1: ready to read buffer
BUF_WRITE_RDY	[4]	R/W	1'h0	Buffer write ready. This status is set if the Buffer Write Enable changes from 0 to 1. 0: not ready to write buffer 1: ready to write buffer
DMA_INT	[3]	R/W	1'h0	DMA interrupt. This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size register. 0: no DMA interrupt 1: DMA interrupt generated
BLK_GAP_EVENT	[2]	R/W	1'h0	Block gap event. If the Stop at Block Gap Request in the Block Gap Control Register is set, this bit is set.

				Read Transaction: This bit is set at the falling edge of the DAT Line Active Status (when the transaction is stopped at SD Bus timing. The Read Wait must be supported in order to use this function). Write Transaction: This bit is set at the falling edge of Write Transfer Active Status (after getting CRC status at SD Bus timing). 0: no block gap event 1: transaction stopped at block gap
TR_COMPLETE	[1]	R/W	1'h0	Transfer complete. This bit is set when a read/write transaction is completed. Read Transaction: This bit is set at the falling edge of Read Transfer Active Status. There are two cases in which the Interrupt is generated. The first is when a data transfer is completed as specified by data length (after the last data has been read to the Host System). The second is when data has stopped at the block gap and completed the data transfer by setting the Stop at Block Gap Request in the Block Gap Control register (after valid data has been read to the Host System). Write Transaction: This bit is set at the falling edge of the DAT Line Active Status. There are two cases in which the Interrupt is generated. The first is when the last data is written to the card as specified by data length and Busy signal is released. The second is when data transfers are stopped at the block gap by setting Stop at Block Gap Request in the Block Gap Control register and data transfers completed (after valid data is written to the SD card and the busy signal is released). Note: Transfer Complete has higher priority than Data Timeout Error. If both bits are set to 1, the data transfer can be considered complete. 0: no data transfer complete 1: data transfer complete
CMD_COMPLETE	[0]	R/W	1'h0	Command complete. This bit is set when getting the end bit of the command response (except auto CMD12). Note: Command Timeout Error has higher priority than Command Complete. If both are set to 1, it can be considered that the response was not received correctly. 0: no command complete 1: command complete

6.13.5.2.10 INT_ST_EN

Description：Normal and error interrupt status enable

0x0034			Normal and error interrupt status enable (reset 0x0000_0000)											INT_ST_EN		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	VNDR_ERR_ST_EN			TRGT_RESP_ERR_EN	Reserved			AUTO_CMD12_ERR_EN	CUR_LMT_ERR_EN	DATA_END_BIT_ERR_EN	DATA_CRC_ERR_EN	DATA_TIMEOUT_ERR_EN	CMD_IND_ERR_EN	CMD_END_BIT_ERR_EN	CMD_CRC_ERR_EN	CMD_TIMEOUT_ERR_EN
Type	R/W			R/W	RO			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							CARD_INT_EN	Reserved		BUF_READ_RDY_EN	BUF_WRITE_RDY_EN	DMA_INT_EN	BLK_GAP_EVNT_EN	TR_COMPLETE_EN	CMD_COMPLETE_EN
Type	RO							R/W	RO		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VNDR_ERR_ST_EN	[31:29]	R/W	3'h0	Vender specified error signal enable 0: masked 1: enabled
TRGT_RESP_ERR_EN	[28]	R/W	1'h0	Target response error signal enable 0: masked 1: enabled
	[27:25]	RO	3'h0	Reserved
AUTO_CMD12_ERR_EN	[24]	R/W	1'h0	Auto CMD12 error signal enable 0: masked 1: enabled
CUR_LMT_ERR_EN	[23]	R/W	1'h0	Current limit error signal enable 0: masked 1: enabled
DATA_END_BIT_ERR_EN	[22]	R/W	1'h0	Data end bit error signal enable 0: masked 1: enabled
DATA_CRC_ERR_EN	[21]	R/W	1'h0	Data CRC error signal enable 0: masked 1: enabled
DATA_TIMEOUT_ERR_EN	[20]	R/W	1'h0	Data timeout error signal enable 0: masked 1: enabled
CMD_IND_ERR_EN	[19]	R/W	1'h0	Command index error signal enable 0: masked

				1: enabled
CMD_END_BIT_ERR_EN	[18]	R/W	1'h0	Command end bit error signal enable 0: masked 1: enabled
CMD_CRC_ERROR_EN	[17]	R/W	1'h0	Command CRC error signal enable 0: masked 1: enabled
CMD_TIMEOUT_ERR_EN	[16]	R/W	1'h0	Command timeout error signal enable 0: masked 1: enabled
	[15:9]	RO	7'h0	Reserved
CARD_INT_EN	[8]	R/W	1'h0	Card interrupt signal enable 0: masked 1: enabled
	[7:6]	RO	2'h0	Reserved
BUF_READ_RDY_EN	[5]	R/W	1'h0	Buffer read ready signal enable 0: masked 1: enabled
BUF_WRITE_RDY_EN	[4]	R/W	1'h0	Buffer write ready signal enable 0: masked 1: enabled
DMA_INT_EN	[3]	R/W	1'h0	DMA interrupt signal enable 0: masked 1: enabled
BLK_GAP_EVENT_EN	[2]	R/W	1'h0	Block gap event signal enable 0: masked 1: enabled
TR_COMPLETE_EN	[1]	R/W	1'h0	Transfer complete signal enable 0: masked 1: enabled
CMD_COMPLETE_EN	[0]	R/W	1'h0	Command complete signal enable 0: masked 1: enabled

6.13.5.2.11 INT_SIG_EN

Description：Normal and error interrupt signal enable

0x0038	Normal and error interrupt signal enable (reset 0x0000_0000)													INT_SIG_EN		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	VNDR_ERR_ST_EN			TRGT_RESP_ERR_EN	Reserved			AUTO_CMD12_ERR_EN	CUR_LMT_ERR_EN	DATA_END_BIT_ERR_EN	DATA_CRC_ERR_EN	DATA_TIMEOUT_ERR_EN	CMD_IND_ERR_EN	CMD_END_BIT_ERR_EN	CMD_CRC_ERR_EN	CMD_TIMEOUT_ERR_EN
Type	R/W			R/W	RO			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							CARD_INT_EN	Reserved		BUF_READ_RDY_EN	BUF_WRITE_RDY_EN	DMA_INT_EN	BLK_GAP_EVNT_EN	TR_COMPLETE_EN	CMD_COMPLETE_EN
Type	RO							R/W	RO		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VNDR_ERR_ST_EN	[31:29]	R/W	3'h0	Vender specified error signal enable 0: masked 1: enabled
TRGT_RESP_ERR_EN	[28]	R/W	1'h0	Target response error signal enable 0: masked 1: enabled
	[27:25]	RO	3'h0	Reserved
AUTO_CMD12_ERR_EN	[24]	R/W	1'h0	Auto CMD12 error signal enable 0: masked 1: enabled
CUR_LMT_ERR_EN	[23]	R/W	1'h0	Current limit error signal enable 0: masked 1: enabled
DATA_END_BIT_ERR_EN	[22]	R/W	1'h0	Data end bit error signal enable 0: masked 1: enabled
DATA_CRC_ERR_EN	[21]	R/W	1'h0	Data CRC error signal enable 0: masked 1: enabled
DATA_TIMEOUT_ERR_EN	[20]	R/W	1'h0	Data timeout error signal enable 0: masked 1: enabled
CMD_IND_ERR_EN	[19]	R/W	1'h0	Command index error signal enable 0: masked

				1: enabled
CMD_END_BIT_ERR_EN	[18]	R/W	1'h0	Command end bit error signal enable 0: masked 1: enabled
CMD_CRC_ERROR_EN	[17]	R/W	1'h0	Command CRC error signal enable 0: masked 1: enabled
CMD_TIMEOUT_ERR_EN	[16]	R/W	1'h0	Command timeout error signal enable 0: masked 1: enabled
	[15:9]	RO	7'h0	Reserved
CARD_INT_EN	[8]	R/W	1'h0	Card interrupt signal enable 0: masked 1: enabled
	[7:6]	RO	2'h0	Reserved
BUF_READ_RDY_EN	[5]	R/W	1'h0	Buffer read ready signal enable 0: masked 1: enabled
BUF_WRITE_RDY_EN	[4]	R/W	1'h0	Buffer write ready signal enable 0: masked 1: enabled
DMA_INT_EN	[3]	R/W	1'h0	DMA interrupt signal enable 0: masked 1: enabled
BLK_GAP_EVENT_EN	[2]	R/W	1'h0	Block gap event signal enable 0: masked 1: enabled
TR_COMPLETE_EN	[1]	R/W	1'h0	Transfer complete signal enable 0: masked 1: enabled
CMD_COMPLETE_EN	[0]	R/W	1'h0	Command complete signal enable 0: masked 1: enabled

6.13.5.2.12 CMD12_ST

Description：Auto CMD12 error status

0x003C			Auto CMD12 error status (reset 0x0000_0000)													CMD12_ST
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								CMD_NOT_ERR	Reserved		IND_ERR	END_BIT_ERR	CRC_ERR	TIMEOUT_ERR	Reserved
Type	RO								RO	RO		RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

~~Field Name~~	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
CMD_NOT_ERR	[7]	RO	1'h0	Command not issued error. Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 error ([4:1]) in this register. 0: no error 1: not issued
	[6:5]	RO	2'h0	Reserved
IND_ERR	[4]	RO	1'h0	Auto CMD12 index error. This occurs if the Command Index error occurs in response to a command. 0: no error 1: error
END_BIT_ERR	[3]	RO	1'h0	Auto CMD12 end bit error. This occurs when detecting that the end bit of command response is 0. 0: no error 1: end bit error generated
CRC_ERR	[2]	RO	1'h0	Auto CMD12 CRC error. This occurs when detecting a CRC error in the command response. 0: no error 1: CRC error generated
TIMEOUT_ERR	[1]	RO	1'h0	Auto CMD12 timeout error. This occurs if the no response is returned within 64 **SDCLK** cycles from the end bit of the command. If this bit is set to 1, the other error status bits ([4:2]) are meaningless. 0: no error 1: timeout
	[0]	RO	1'h0	Reserved

6.13.5.2.13 CAP

Description：Capabilities

0x0040	Capabilities (reset 0x02e1_0080)															CAP
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved					V18	V30	V33	SUSP_RES	DMA	HIGH_SPEED	Reserved			MAX_BLK_SIZE	
Type	RO					RO	RO	RO	RO	RO	RO	RO			RO	
Reset	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		BASE_CLK_FRQ						TIMEOUT_CLK_UNIT	Reserved	TIMEOUT_CLK_FRQ					
Type	RO		RO						RO	RO	RO					
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:27]	RO	5'h0	Reserved
V18	[26]	RO	1'h0	Voltage support 1.8 V. 0: 1.8 V not supported 1: 1.8 V supported
V30	[25]	RO	1'h1	Voltage support 3.0 V. 0: 3.0 V not supported 1: 3.0 V supported
V33	[24]	RO	1'h0	Voltage support 3.3 V. 0: 3.3 V not supported 1: 3.3 V supported
SUSP_RES	[23]	RO	1'h1	Suspend/resume support. This bit indicates whether the HC supports Suspend/Resume function. If this bit is 0, the Suspend and Resume mechanism is not supported and the HD shall not issue either Suspend/Resume command. 0: not supported 1: supported
DMA	[22]	RO	1'h1	DMA support. This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly. 0: DMA not supported 1: DMA supported
HIGH_SPEED	[21]	RO	1'h1	High speed support. This bit indicates whether the HC and the Host System support High Speed mode and they can supply SD Clock frequency from 25 MHz to 50 MHz.

				0: high speed not supported 1: high speed supported
	[20:18]	RO	3'h0	Reserved
MAX_BLK_SIZE	[17:16]	RO	2'h01	This value indicates the maximum block size that the HD can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. 00: 512 bytes 01: 1024 bytes 10: 2048 bytes 11: 4096 bytes
	[15:14]	RO	2'h0	Reserved
BASE_CLK_FRQ	[13:8]	RO	6'h0	This value indicates the base (maximum) clock frequency for the SD clock. The unit is MHz. If the real frequency is 16.5 MHz, a larger value shall be set, i.e., 010001b (17 MHz) because the HD uses this value to calculate the clock divider value and it shall not exceed the upper limit of the SD clock frequency. The supported range is 10 to 63 MHz. If these bits are all 0, the Host System has to get information via another method. 0: get information via another method (Registry Entry) 1: 1 MHz 2: 2 MHz … 63: 63 MHz
TIMEOUT_CLK_UNIT	[7]	RO	1'h1	This bit shows the unit of base clock frequency used to detect Data Timeout Error. 0: kHz 1: MHz
	[6]	RO	1'h0	Reserved
TIMEOUT_CLK_FRQ	[5:0]	RO	6'h0	This bit shows the base clock frequency used to detect Data Timeout Error. 0: get information via another method 1: 1 MHz 2: 2 MHz … 63: 63 MHz

6.13.5.2.14 MAX_CUR_CAP

Description：Maximum current capabilities

0x0048			Maximum current capabilities (reset 0x0000_0000)													MAX_CUR_CAP
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved								MAX_CUR_V18							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MAX_CUR_V30								MAX_CUR_V33							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:24]	RO	8'h0	Reserved
MAX_CUR_V18	[23:16]	RO	8'h0	Maximum current for 1.8 V. 0: get information via another method
MAX_CUR_V30	[15:8]	RO	8'h0	Maximum current for 3.0 V. 0: get information via another method
MAX_CUR_V33	[7:0]	RO	8'h0	Maximum current for 3.3 V. 0: get information via another method

6.13.5.2.15 SLT_INT_ST

Description：Slot interrupt status and version number

0x00FC			Slot interrupt status and version number (reset 0x0000_0000)													SLT_INT_ST
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	VNDR_VER_NO								SPEC_VER_NO							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								SLT_INT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VNDR_VER_NO	[31:24]	RO	8'h0	This status is reserved for the vendor version number. The HD should not use this status.
SPEC_VER_NO	[23:16]	RO	8'h0	This status indicates the Host Controller Spec Version. The upper and lower 4 bits indicate the version. 0: SD Host Specification version 1.0

				Others: reserved
	[15:8]	RO	8'h0	Reserved
SLT_INT	[7:0]	RO	8'h0	These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot. A maximum of 8 slots can be defined. If one interrupt signal is associated with multiple slots, the HD can know which interrupt is generated by reading these status bits. By a power-on reset or by Software Reset for All, the Interrupt signal shall be deasserted and this status shall read 0. [0]: slot 1 [1]: slot 2

6.14 SDIO slave Controller

6.14.1 Overview

SDIO: SD Input/Output

The SDIO (SD Input/Output) slave model is based on and compatible with the SD memory card. The intent of SDIO module used in SPRD design is to transfer data from/to data card. It has the AHB master and slave interface to commute with the main AHB bus.

6.14.2 Features

- Targeted for high speed data transfer applications (as slave).
- Compatible with SD physical layer specification ver2.0
- Compatible with SDIO specification ver2.0
- Allows card to interrupt host
- SDIO card only
- Support only function 1 (function 0 default support)
- Support SD 4/1 bit mode
- Support read wait
- Support suspend/resume
- Support direct commands during data transfer
- Support multi-block
- Support infinite transfer
- Support interrupt between blocks of data in 4-bit SD mode
- Support f0 max block size 1 bytes
- Support f1 max block size 1024bytes
- Support full speed card 25MHz
- Support high speed card 50MHz
- No support master power control
- No support code storage area
- No support SPI mode of this module (it reused with the outside independent SPI module)
- Initialization IO voltage: 3.3V
- Operational IO voltage range: (4 level adjustable outside this module)

6.14.3 Signal Description

There are 6 signals to interface with external chip of SDIO host. CLK pad is used to provide the working clock for internal register, CMD pad is to receive SDIO host command or send response, and the DAT3~ 0 lines is used to transfer data.

Table 6-12 SDIO interface

PIN Name	Description
CLK	Clock
CMD	Command line
DAT0	Data 0 line
DAT1	Data 1 line
DAT2	Data 2 line
DAT3	Data 3 line

The external connection of SDIO host and SDIO slave can be refer to the following figure.

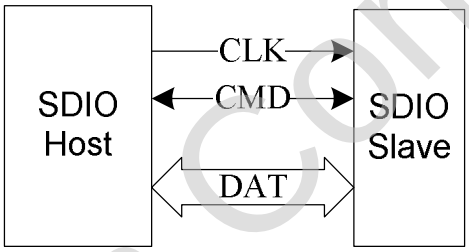


Figure 6-58 SDIO Connection

6.14.4 Function Description

The preliminary idea of this module is to interconnect AP to our BB module and interchange data using the popular interface of SDIO port.

The SDIO slave module is used to transfer data using the SDIO protocol which compatible with the "*SD Specifications Part E1 SDIO Specification Version 2.00 January 30, 2007*" and "*SD Specifications Part 1 Physical Layer Specification Version 2.00*" except for the omitted SPI protocol which divided to an individual module.

6.14.4.1 Block Diagram

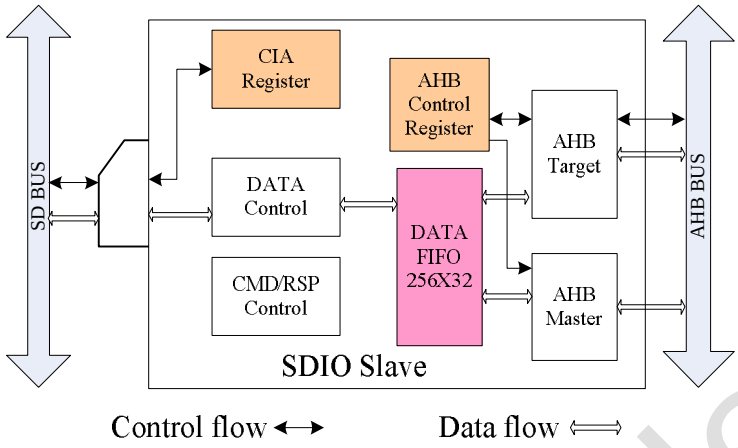


Figure 6-59 System Block Diagram

This SDIO slave have there main interfaces. The first is the SD bus which act as the SDIO slave interface to receive the host command and transfer data to/from internal data FIFO. The other two interfaces are AHB master and target interface which act as the porter that transit data between AHB bus and internal data FIFO.

As the figure shows, the control flow and data flow are draw with different type of arrows.

The CIA register is configured through the SD bus interface, AHB control register is configured through AHB target interface.

The internal FIFO is operated in Ping-Pang mode, and the data can be take away by CPU read/write through AHB target interface of directly read/write through AHB master by DMA.

6.14.4.2 SDIO Slave Initial Sequence

After reset or power-up, I/O function 1 on the card is disabled and shall not execute any operation except CMD5. At first the host sends CMD5 with no argument to ask the card for the OCR, and the card responses with its supported OCR and supported functions (in this card, only function 1 is support). After this, host set an appropriate voltage according to the card's replied OCR and wait for the card is ready to operate. After the card is ready, host send CMD3 to ask card for the RCA which used to distinguish the different slave card if there are more than one card existed. All the initialized of the I/O card is completed after card replayed with right RCA.

This I/O only card will not respond to the CMD0, CMD1 and CMD55/ACMD41 command, so any of the following except cases are no response and the card will be set to inactive state which has no affect to the card.

- if the host is non-I/O aware host
- if the host wants to initialize the card to SD or MMC memory card
- if the host wants to initialize the card to SPI mode

To select this card, the host shall send CMD7 with the given RCA before all the following operations. After the host has initialized the I/O portion of the card, it then reads the Common Information Area (CIA) of the card. This is done by issuing a read command, starting with the byte at address 0x00, of I/O function 0. The CIA contains the Card Common Control Registers (CCCR) and the Function Basic Registers (FBR). Also included in the CIA are pointers to the card's common Card Information Structure (CIS) and each individual function's CIS. The CIS includes information on power, function, manufacturer and other things the host needs to determine if the I/O function(s) is appropriate to power-up. If the host determines that the card should be activated, a register in the CCCR area enables the card and each individual function.

At this time, all functions of the I/O card are fully available. In addition, the host can enable/disable interrupts on a function-by-function basis.

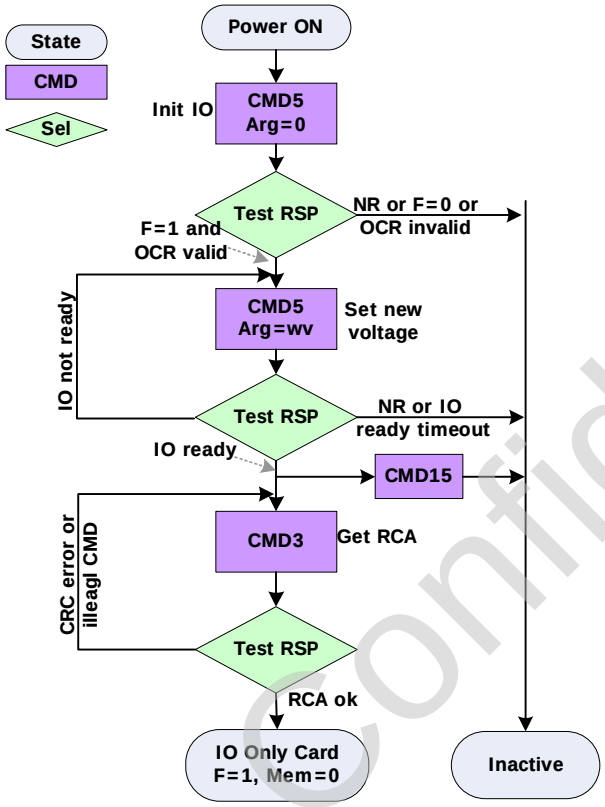


Figure 6-60 SDIO Initial Sequence

6.14.4.3 Supported Command and Response

In our design, there are just 6 command supported. CMD5 is used to get card's support voltage and set new appreciate voltage; CMD3 is used to get card's relative card address. CMD5 and CMD3 command are acted as initial command. CMD7 is used to select the right card base on previously get RCA or to unselect the card. CMD52 is an IO direct read/write command, it is the fastest means to read or write single I/O register, also act to read or write the control registers. CMD53 is an IO extended read/write command; it is used to transfer a large number of data in one time. CMD15 is not a common used command; it is used to send card into an inactive state which just can be active by power reset.

Table 6-13 Support CMD and RSP

Command	Command Name	Response	Description
CMD3	SEND_RELATIVE_ADDR	R6	Ask the card to publish a new relative address (RCA)
CMD5	IO_SEND_OP_COND	R4	It is used to inquire about the voltage range needed by the I/O card.
CMD7	SELECT/ DESELECT_CARD	R1b	Command toggles a card between the stand-by and transfer states or between the programming and disconnects states.
CMD15	GO_INACTIVE_S	N/A	Sends an addressed card into the Inactive State.

	TATE		
CMD52	IO_RW_DIRECT	R5	This command is the fastest means to read or write single I/O registers, as it requires only a single command / response pair.
CMD53	IO_RW_EXTENDED	R5	This command allows the reading or writing of a large number of I/O registers with a single command.

6.14.4.3.1 CMD3

Bit	47	46	45:40	39:8	7:1	0
Width	1	1	6	32	7	1
Value	0	1	6'b000011	32'h0000_0000	x	1
Description	S	D	CMD Index	Stuff bits	CRC7	E

Note:

The gray color background table are don't care registers and reserved to fix value.

6.14.4.3.2 CMD5

Bit	47	46	45:40	39:8		7:1	0
Width	1	1	6	8	24	7	1
Value	0	1	6'b000101	8'h0	x	x	1
Description	S	D	CMD Index	Stuff	I/O OCR (*1)	CRC7	E

6.14.4.3.3 CMD7

Bit	47	46	45:40	39:8		7:1	0
Width	1	1	6	16	16	7	1
Value	0	1	6'b000111	x	16'h0	x	1
Description	S	D	CMD Index	RCA	Stuff bits	CRC7	E

6.14.4.3.4 CMD15

Bit	47	46	45:40	39:8		7:1	0
Width	1	1	6	16	16	7	1
Value	0	1	6'b001111	x	16'h0	x	1
Description	S	D	CMD Index	RCA	Stuff bits	CRC7	E

6.14.4.3.5 CMD52

Bit	47	46	45:40	39:8							7:1	0
Width	1	1	6	1	3	1	1	17	1	8	7	1
Value	0	1	6'b110100	x	x	x	0	X	0	X	7'h0	1
Des.	S	D	CMD Index	RW Flag	Func. Num	RAW Flag	Stuff	Reg. Addr	Stuff	Write Data	CRC7	E

6.14.4.3.6 CMD53

Bit	47	46	45:40	39:8						7:1	0
Width	1	1	6	1	3	1	1	17	9	7	1
Value	0	1	6'b110101	x	x	x	x	X	x	7'h0	1
Des.	S	D	CMD Index	RW Flag	Func. Num	Block Mode	OP Code	Reg. Addr	Byte/Block Count	CRC7	E

6.14.4.3.7 R6

Bit	47	46	45:40	39:8		7:1	0
Width	1	1	6	16	16	7	1
Value	0	0	6'b000011	x	x	x	1
Description	S	D	CMD Index	New published RCA	Card Status(*2)	CRC7	E

6.14.4.3.8 R4

Bit	47	46	45:40	39:8					7:1	0
Width	1	1	6	1	3	1	3	24	7	1
Value	0	0	6'b111111		1	0	3'b0	x	7'h0	1
Description	S	D	Rsv	C	Num of I/O	Mem Pres	Stuff Bits	I/O OCR	Rsv	E

6.14.4.3.9 R1b

Bit	47	46	45:40	39:8	7:1	0
Width	1	1	6	32	7	1
Value	0	0	6'b000111	x	x	1
Description	S	D	CMD Index	Card status(*3)	CRC7	E

6.14.4.3.10 R5

Bit	47	46	45:40	39:8			7:1	0
Width	1	1	6	16	8	8	7	1
Value	0	0	6'b110101	x	x	x	x	1
Description	S	D	CMD Index	Stuff	Response Flags (*4)	Read / Write Data	CRC7	E

6.14.4.3.11 Note

*1, OCR

Table 6-14 OCR map

I/O OCR bit position	VDD voltage window (in volts)
0 ~ 7	Reserved
8	2.0 ~ 2.1

9	2.1 ~ 2.2
10	2.2 ~ 2.3
11	2.3 ~ 2.4
12	2.4 ~ 2.5
13	2.5 ~ 2.6
14	2.6 ~ 2.7
15	2.7 ~ 2.8
16	2.8 ~ 2.9
17	2.9 ~ 3.0
18	3.0 ~ 3.1
19	3.1 ~ 3.2
20	3.2 ~ 3.3
21	3.3 ~ 3.4
22	3.4 ~ 3.5
23	3.5 ~ 3.6

*2, Card Status 1 (16 bits)

Bits	Identifier	Type	Value	Description	Clear Condition
15	COM_CRC_ERROR	E R	0, no error 1, error	The CRC check of the previous command failed.	B
14	ILLEGAL_COMMAND	E R	0, no error 1, error	Command not legal for the card state	B
13	ERROR	E R X	0, no error 1, error	A general or an unknown error occurred during the operation.	C
12:0	Reserved		0		

*3, Card Status 2 (32 bits)

Bits	Identifier	Type	Value	Description	Clear Condition
23	COM_CRC_ERROR	E R	0, no error 1, error	The CRC check of the previous command failed.	B
22	ILLEGAL_COMMAND	E R	0, no error 1, error	Command not legal for the card state	B
21:20	Reserved		0		
19	ERROR	E R X	0, no error 1, error	A general or an unknown error occurred during the operation.	C
18:0	Reserved		0		

*4, Response Flags

Bits	Identifier	Type	Value	Description	Clear Condition
7	COM_CRC_ERROR	E R	0, no error 1, error	The CRC check of the previous command failed.	B
6	ILLEGAL_COMMAND	E R	0, no error 1, error	Command not legal for the card state	B
5:4	IO_CURRENT_STATE	S	00, DIS 01, CMD 02, TRN 03, RFU	DIS: Disabled: CMD: Data line free. TRN: Data transferring	B
3	ERROR	E R (CMD52) E R X (CMD53)	0, no error 1, error	A general or an unknown error occurred during the operation.	C
2	Reserved		0		
1	FUNCTION_NUMBER	E R	0, no error 1, error	An invalid function number was requested	C
0	OUT_OF_RANGE	E R	0, no error 1, error	The command's argument was out of the allowed range for this card.	C

Type:	
E:	Error bit.
R:	Detected and set for the actual command response.
S:	Status bit.
X:	Detected and set during command execution. The host can get the status by issuing a command with R1 response
Clear Condition:	
C:	Clear by read.
B:	Always related to the previous command. Reception of a valid command will clear it (with a delay of one command).

6.14.4.4 Bus State Diagram for SDIO card

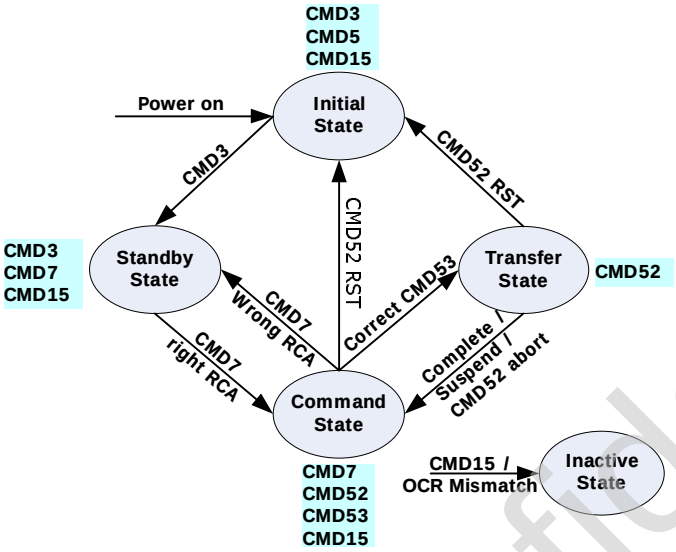


Figure 6-61 Bus State Diagram

6.14.5 Control Registers

The SDIO register has divided into two parts, the SD domain and AHB domain.

6.14.5.1 AHB Domain Memory map

ARM base address: 0x2050_0200 (*SC6820*)

Table 6-15 AHB Domain Registers

Offset Address	Name	Description
0x0000	SYS_ADDR	DMA system address
0x0004	RST_DMASET	DMA setting and software reset
0x0008		Reserved
0x000C	BLK_CNT_SIZE	Block size and block count information
0x0010	TRANS_MODE	Transfer mode information
0x0014	CURT_STATUS	Current operation status
0x0018	CMD_ARG	Current command argument
0x001C	RSP_ARG	Current response argument
0x0020	DAT_PORT	Read or write buffer data port
0x0024		Reserved
0x0028		Reserved
0x002C		Reserved
0x0030	INT_EN	Interrupt enable signal
0x0034	INT_CLR	Interrupt clear signal
0x0038	INT_RAW	Interrupt raw status
0x003C	INT_STA	Interrupt masked status

Offset Address	Name	Description
0x0040	SUPT_OCR	Supported OCR
0x0044	CURT_OCR	Set current OCR

6.14.5.2 AHB Domain Register Descriptions

6.14.5.2.1 SYS_ADDR Registers

Description：System memory address for DMA transfer

This register indicates the DMA where to read or write data. To use DMA transfer, this register should be set first.

0x0000			DMA system address (Reset 0x0000_0000)										SYS_ADDR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SYS_ADDR (H)															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SYS_ADDR (L)															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:

You can write the system address registers bytes by bytes, half-word by half-word or word by word.

(H) Indicate the high end of this register, (L) indicate the low end of this register.

Field Name	Bit	Type	Reset Value	Description
SYS_ADDR	[31:0]	R/W	32'h0	This register indicates the DMA where to read or write data. To use DMA transfer, this register should be set first. Note, once the DMA transfer is processing, modifying is forbidden

6.14.5.2.2 RST_DMASET Registers

Description：Write 1 to the relative register can reset the AHB or SDIO domain registers;

Before using DMA, the DMA buffer size and DMA enable register should be set first;

0x0004			DMA setting and soft reset register (Reset 0x0000_0000)										RST_DMASET			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved												DMA_BUF_SIZE			DMA_EN
Type	RO												R/W			R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												FUNC1_INT	SOFT_RST_SDIO	SOFT_RST_AHB	SOFT_RST_ALL
Type	RO												WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:20]	RO	12'h0	Reserved
DMA_BUF_SIZE	[19:17]	R/W	3'h0	Specify the DMA buffer size when use DMA methods to transfer data. Once the DMA has transfer the size amount data, it then sent a DMA interrupt to notice software to fetch data.
DMA_EN	[16]	R/W	1'h0	DMA enable signal. 0: Disable 1: Enable
	[15:4]	RO	12'h0	Reserved
FUNC1_INT	[3]	WO	1'h0	Set this bit to 1 to manual generate a function 1 interrupt. Auto clear to 0 after write 1
SOFT_RST_SDIO	[2]	WO	1'h0	Set this bit to 1 to soft reset SDIO domain registers. Auto clear to 0 after write 1
SOFT_RST_AHB	[1]	WO	1'h0	Set this bit to 1 to soft reset AHB domain registers. Auto clear to 0 after write 1
SOFT_RST_ALL	[0]	WO	1'h0	Set this bit to 1 to soft reset SDIO and AHB domain registers. Auto clear to 0 after write 1.

6.14.5.2.3 BLK_CNT_SIZE Registers

Description：This register give the SDIO host set block size and block counter.

0x000C			Block Size and Counter (Reset 0x0000_0000)													BLK_CNT_SIZE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved							BLK_CNT								
Type	RO							RO								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				BLK_SIZE											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:25]	RO	7'h0	Reserved
BLK_CNT	[24:16]	RO	9'h0	Transfer Block Count. Set by SDIO host through SD bus.
	[15:12]	RO	4'h0	Reserved
BLK_SIZE	[11:0]	RO	5'h0	Transfer Block Size. Set by SDIO host through SD bus.

6.14.5.2.4 TRANS_MODE Registers

Description： Specify some read only register that SDIO host set transferring mode.

0x0010			Transfer mode register (Reset 0x0000_0000)													TRANS_MODE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								INFIN_MODE	SIG_MULT	HIGH_SPEED	BUS_WIDTH		TRANS_DIR	OPER_MODE	BLK_MODE
Type	RO								RO	RO	RO	RO		RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
INFIN_MODE	[7]	RO	1'h0	Indicate whether the transfer is infinite or not 0: Infinite transfer 1: Finite transfer
SIG_MULT	[6]	RO	1'h0	Indicate whether the transfer is signal or multiply transfer. 0: Signal block 1: Multiply block

HIGH_SPEED	[5]	RO	1'h0	Indicate whether the transfer is high speed or not. 0: Normal transfer (<=25MHz) 1: High Speed transfer (50MHz)
BUS_WIDTH	[4:3]	RO	2'h0	Indicate whether the transfer bus width is 1 bit or 4 bits. 2'b00: 1 bit width 2'b10: 4 bit width
TRANS_DIR	[2]	RO	1'h0	Indicate whether the transfer is read or write. 0: Read 1: Write
OPER_MODE	[1]	RO	1'h0	Indicate whether the transfer mode is increasing or fixing address. 0: Fixing address 1: Increasing address
BLK_MODE	[0]	RO	1'h0	Indicate whether the transfer is block mode or byte mode. 0: Byte mode transfer. 1: Block mode transfer.

6.14.5.2.5 CURT_STATUS Registers

Description： Specify some read only register that SDIO host transferring status.

0x0014	Current Status Register(Reset 0x0000_0000)												CURT_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved											DAT3	DAT2	DAT1	DAT0	CMD
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved					SUSP_STA	RD_WAIT_ST	BUS_STA			CMD_IDX					
Type	RO					RO	RO	RO			RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:

These registers are just used for debug only.

Field Name	Bit	Type	Reset Value	Description
	[31:21]	RO	11'h0	Reserved
DAT3	[20]	RO	1'h0	Data 3 line latched
DAT2	[19]	RO	1'h0	Data 2 line latched
DAT1	[18]	RO	1'h0	Data 1 line latched

DAT0	[17]	RO	1'h0	Data 0 line latched
CMD	[16]	RO	1'h0	Command line latched
	[15:11]	RO	5'h0	Reserved
SUSP_STA	[10]	RO	1'h0	Indicate whether the transfer is suspending or not. 0: Normal 1: Suspending.
RD_WAIT_STA	[9]	RO	1'h0	Indicate whether the transfer is in read wait state or not. 0: Normal 1: Read wait state
BUS_STA	[8:6]	RO	3'h0	Specify the current bus state. 3'b000: Bus idle 3'b001: Bus standby 3'b010: Bus command 3'b011: Bus transfer 3'b100: Bus inactive
CMD_IDX	[5:0]	RO	6'h0	Specify the current command index

6.14.5.2.6 CMD_ARG Registers

Description： Specify read only register that SDIO host transferring command argument.

0x0018	Command Argument(Reset 0x0000_0000)													CMD_ARG			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	CMD_ARG (H)															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CMD_ARG (L)															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:

This register is just used for debug only.

Field Name	Bit	Type	Reset Value	Description
CMD_ARG	[31:0]	RO	32'h0	This register indicates the current transmitted command argument.

6.14.5.2.7 RSP_ARG Registers

Description： Specify read only register that SDIO host received response argument.

0x001C			Response Argument(Reset 0x0000_0000)													RSP_ARG
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	RSP_ARG (H)															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RSP_ARG (L)															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:

This register is just used for debug only.

Field Name	Bit	Type	Reset Value	Description
RSP_ARG	[31:0]	RO	32'h0	This register indicates the current transmitted response argument.

6.14.5.2.8 DAT_PORT Registers

Description： This register is used to read or write data when using NON-DMA transferring mode.

0x0020			Buffer Data Port Register (Reset 0x0000_0000)													DAT_PORT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DAT_PORT (H)															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DAT_PORT (L)															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:

This registers should be accessed word by word.

Field Name	Bit	Type	Reset Value	Description
DAT_PORT	[31:0]	R/W	32'h0	This register is used to read or write data when using non-DMA transferring mode.

6.14.5.2.9 INT_EN Registers

Description： Interrupt enable signals

0x0030			Interrupt enable signals (Reset 0x0000_0000)											INT_EN		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved												AHB_TRN_ERR_EN	WD_CRC_ERR_EN	CMD_ILL_EN	CMD_CRC_ERR_EN
Type	RO												R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								OCR_INT_EN	SLV_RD_EN	SLV_WR_EN	AHB_WRDY_EN	AHB_RRDY_EN	DMA_INT_EN	RD_CMP_EN	WR_CMP_EN
Type	RO								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:20]	RO	12'h0	Reserved
AHB_TRN_ERR_EN	[19]	R/W	1'h0	AHB transfer error enable
WD_CRC_ERR_EN	[18]	R/W	1'h0	Write data crc err interrupt enable
CMD_ILL_EN	[17]	R/W	1'h0	Command illegal interrupt enable
CMD_CRC_ERR_EN	[16]	R/W	1'h0	Command crc error interrupt enable
	[15:8]	RO	8'h0	Reserved
OCR_INT_EN	[7]	R/W	1'h0	SDIO host CMD5 set OCR interrupt enable
SLV_RD_EN	[6]	R/W	1'h0	Slave read begin enable
SLV_WR_EN	[5]	R/W	1'h0	Slave write begin enable
AHB_WRDY_EN	[4]	R/W	1'h0	No-dma mode write buffer ready enable
AHB_RRDY_EN	[3]	R/W	1'h0	No-dma mode read buffer ready enable
DMA_INT_EN	[2]	R/W	1'h0	DMA transfer data complete enable
RD_CMP_EN	[1]	R/W	1'h0	Read transfer data complete enable
WR_CMP_EN	[0]	R/W	1'h0	Write transfer data complete enable

6.14.5.2.10 INT_CLR Registers

Description： Interrupt status clear signals

0x0034			Interrupt status clear signals (Reset 0x0000_0000)													INT_CLR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved												AHB_TRN_ERR_CLR	WD_CRC_ERR_CLR	CMD_ILL_CLR	CMD_CRC_ERR_CLR
Type	RO												R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								OCR_INT_CLR	SLV_RD_CLR	SLV_WR_CLR	AHB_WRDY_CLR	AHB_RRDY_CLR	DMA_INT_CLR	RD_CMP_CLR	WR_CMP_CLR
Type	RO								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:20]	RO	12'h0	Reserved
AHB_TRN_ERR_CLR	[19]	R/W	1'h0	AHB transfer error clear
WD_CRC_ERR_CLR	[18]	R/W	1'h0	Write data crc err interrupt clear
CMD_ILL_CLR	[17]	R/W	1'h0	Command illegal interrupt clear
CMD_CRC_ERR_CLR	[16]	R/W	1'h0	Command crc error interrupt clear
	[15:8]	RO	8'h0	Reserved
OCR_INT_CLR	[7]	R/W	1'h0	SDIO host CMD5 set OCR interrupt clear
SLV_RD_CLR	[6]	R/W	1'h0	Slave read begin clear
SLV_WR_CLR	[5]	R/W	1'h0	Slave write begin clear
AHB_WRDY_CLR	[4]	R/W	1'h0	No-dma mode write buffer ready clear
AHB_RRDY_CLR	[3]	R/W	1'h0	No-dma mode read buffer ready clear
DMA_INT_CLR	[2]	R/W	1'h0	DMA transfer data complete clear
RD_CMP_CLR	[1]	R/W	1'h0	Read transfer data complete clear
WR_CMP_CLR	[0]	R/W	1'h0	Write transfer data complete clear

6.14.5.2.11 INT_RAW Registers

Description： Interrupt raw status signals

0x0038	Interrupt raw status signals (Reset 0x0000_0000)												INT_RAW			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved												AHB_TRN_ERR_RAW	WD_CRC_ERR_RAW	CMD_ILL_RAW	CMD_CRC_ERR_RAW
Type	RO												RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								OCR_INT_RAW	SLV_RD_RAW	SLV_WR_RAW	AHB_WRDY_RAW	AHB_RRDY_RAW	DMA_INT_RAW	RD_CMP_RAW	WR_CMP_RAW
Type	RO								RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:20]	RO	12'h0	Reserved
AHB_TRN_ERR_RAW	[19]	RO	1'h0	AHB transfer error raw status
WD_CRC_ERR_RAW	[18]	RO	1'h0	Write data crc err interrupt raw status
CMD_ILL_RAW	[17]	RO	1'h0	Command illegal interrupt raw status
CMD_CRC_ERR_RAW	[16]	RO	1'h0	Command crc error interrupt raw status
	[15:8]	RO	8'h0	Reserved
OCR_INT_RAW	[7]	RO	1'h0	SDIO host CMD5 set OCR interrupt raw status
SLV_RD_RAW	[6]	RO	1'h0	Slave read begin raw status
SLV_WR_RAW	[5]	RO	1'h0	Slave write begin raw status
AHB_WRDY_RAW	[4]	RO	1'h0	No-dma mode write buffer ready raw status
AHB_RRDY_RAW	[3]	RO	1'h0	No-dma mode read buffer ready raw status
DMA_INT_RAW	[2]	RO	1'h0	DMA transfer data complete raw status
RD_CMP_RAW	[1]	RO	1'h0	Read transfer data complete raw status
WR_CMP_RAW	[0]	RO	1'h0	Write transfer data complete raw status

6.14.5.2.12 INT_STA Registers

Description： Interrupt masked status signals

0x003C			Interrupt masked status signals (Reset 0x0000_0000)													INT_STA
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved												AHB_TRN_ERR_STA	WD_CRC_ERR_STA	CMD_ILL_STA	CMD_CRC_ERR_STA
Type	RO												RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								OCR_INT_STA	SLV_RD_STA	SLV_WR_STA	AHB_WRDY_STA	AHB_RRDY_STA	DMA_INT_STA	RD_CMP_STA	WR_CMP_STA
Type	RO								RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:20]	RO	12'h0	Reserved
AHB_TRN_ERR_STA	[19]	RO	1'h0	AHB transfer error masked status
WD_CRC_ERR_STA	[18]	RO	1'h0	Write data crc err interrupt masked status
CMD_ILL_STA	[17]	RO	1'h0	Command illegal interrupt masked status
CMD_CRC_ERR_STA	[16]	RO	1'h0	Command crc error interrupt masked status
	[15:8]	RO	8'h0	Reserved
OCR_INT_STA	[7]	RO	1'h0	SDIO host CMD5 set OCR interrupt masked status
SLV_RD_STA	[6]	RO	1'h0	Slave read begin masked status
SLV_WR_STA	[5]	RO	1'h0	Slave write begin masked status
AHB_WRDY_STA	[4]	RO	1'h0	No-dma mode write buffer ready masked status
AHB_RRDY_STA	[3]	RO	1'h0	No-dma mode read buffer ready masked status
DMA_INT_STA	[2]	RO	1'h0	DMA transfer data complete masked status
RD_CMP_STA	[1]	RO	1'h0	Read transfer data complete masked status
WR_CMP_STA	[0]	RO	1'h0	Write transfer data complete masked status

6.14.5.2.13 SUPT_OCR Registers

Description： Support OCR register.

0x0040	Support OCR register (Reset 0x0000_0000)															SUPT_OCR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved							LDO_RDY	SUPT_OCR (H)							
Type	RO							R/W	R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SUPT_OCR (L)															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:25]	RO	7'h0	Reserved
LDO_RDY	[24]	R/W	1'h0	When set new OCR, the AHB should adjust the LDO to adapt the new voltage, after the LDO is stable, AHB set this bit to notice the SDIO host that the IO is ready, and then the initialization can be in progress.
SUPT_OCR	[23:0]	R/W	24'h0	This register is set by AHB to tell the host the voltage round of this slave supported.

Note:

Before the initial state, software should set SUPT_OCR register with the supported OCR value first, then the SDIO initial process can be proceed.

In the initial process, the R4 will response to host with the SUPT_OCR value, if it matched host's OCR, then the host will send a new OCR value to slave (reflect to the following register of CURT_OCR). At the same time, an interrupt of OCR_INT_STA will occurred to ask slave to set the LDO using the new set OCR.

After the LDO is stable, the software set LDO_RDY bit to indicate it is ready to process the following initial process.

6.14.5.2.14 CURT_OCR Registers

Description: Current OCR register.

0x0044			Current OCR register (Reset 0x0000_0000)													CURT_OCR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved								CURT_OCR (H)							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CURT_OCR (L)															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:24]	RO	8'h0	Reserved
CURT_OCR	[23:0]	RO	24'h0	This register is set by SDIO host to tell the AHB what the new set voltage is, and then the AHB should adjust the LDO.

Note:

Refer to the before interpretation of SUPT_OCR for the detail information.

For the SD domain, only the SDIO host can access it and it is not visible for ARM or DSP. The SD domain register are call Common I/O Area register (CIA). The CIA shall be implemented on all SDIO cards. The CIA is accessed by the host via I/O reads and writes to function 0. The registers within the CIA are provided to enable/disable the operation of the I/O function(s), control the generation of interrupts and optionally load software to support the I/O functions. The registers in the CIA also provide information about the function(s) abilities and requirements. There are three distinct register structures supported within the CIA. They are:

- Card Common Control Registers (CCCR)
- Function Basic Registers (FBR)
- Card Information Structure (CIS)

6.14.5.3 SD Domain Memory map (CCCR)

The Card Common Control Registers allow for quick host checking and control of an I/O card's enable and interrupts on function basis. The bits in the CCCR are mixed Read/Write and read only. If the functions are not provided on an SDIO card, the bits corresponding to unused functions shall all be read-only and read as 0. All reserved for future use bits (RFU) shall be read-only and return a value of 0. All writeable bits are set to 0 after power-up or reset. Access to the CCCR is possible even after initialization when the I/O functions are disabled. Access is performed using the I/O read and write commands. This allows the host to enable functions after initialization. This abstract SDIO slave CCCR is as follows:

Table 6-16 Card Common Control Registers (CCCR)

Card Common Control Registers (CCCR)										
Offset	**Reset**	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	8'h32	CCCR / SDIO Rev	SDIO Specification Rev				CCCR Format Version			
0x01	8'h02	SD Rev	RFU				SD Format Version			
0x02	8'h00	I/O Enable	IOE7	IOE6	IOE5	IOE4	IOE3	IOE2	IOE1	RFU
0x03	8'h00	I/O Ready	IOR7	IOR6	IOR5	IOR4	IOR3	IOR2	IOR1	RFU
0x04	8'h00	Int Enable	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IENM
0x05	8'h00	Int Pending	INT7	INT6	INT5	INT4	INT3	INT2	INT1	RFU
0x06	8'h00	I/O Abort	RFU				RES	AS[2:0]		
0x07	8'h00	Bus Intf Control	CD dis	SCSI	ECSI	RFU			Bus Width	
0x08	8'h1F	Card Capability	4BLS	LSC	E4MI	S4MI	SBS	SRW	SMB	SDC
0x09-0x0B	24'h 1000	Common CIS Pointer	Pointer to card's common Card Information Structure (CIS)							
0x0C	8'h00	Bus Suspend	RFU						BR	BS
0x0D	8'h00	Function Select	DF	RFU			FS[3:0]			
0x0E	8'h00	Exec Flags	EX7	EX6	EX5	EX4	EX3	EX2	EX1	EXM
0x0F	8'h02	Ready Flags	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RFM
0x10-0x11	16'h0	FN0 Block Size	I/O Block Size for Function 0							
0x12	8'h00	RFU	RFU						EMPC	SMPC
0x13	8'h01	High-Speed	RFU						EHS	SHS
0x14-0xEF		RFU	RFU							
0xF0-0xF3	32'h0	Free Read/Write	Free Read or Write Area							
0xF4 0xFF		Vendors Area	RFU							

Note:

The gray back color table are don't care registers and reserved to 0.

6.14.5.4 SD Domain Register Descriptions (CCCR)

6.14.5.4.1 CCCR/SDIO Rev Registers

Description：The version of CCCR and SDIO

0x0000	CCCR/SDIO version (Reset 0x32)						CCCR/SDIO Rev	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SDIO_SPC_VER				CCCR_FMT_VER			
Type	RO				RO			
Reset	0	0	1	1	0	0	1	0

Field Name	Bit	R/W	Reset Value	Description
SDIO_SPC_VER	[7:4]	RO	4'h3	SDIO Specification Version ---------- Value SDIO Specification 0x00 Version 1.00 0x01 Version 1.10 0x02 Version 1.20 0x03 Version 2.00 0x04-0x0F Reserved
CCCR_FMT_VER	[3:0]	RO	4'h2	CCCR Format Version. ---------- Value CCCR/FBR 0x00 Version 1.00 0x01 Version 1.10 0x02 Version 1.20 0x03-0x0F Reserved

6.14.5.4.2 SD Version Registers

Description：SD Version, Read Only.

0x0001	SD version (Reset 0x02)						SD Rev	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				SD_VER			
Type	RO				RO			
Reset	0	0	0	0	0	0	1	0

Field Name	Bit	R/W	Reset Value	Description
	[7:4]	RO	4'h0	Reserved
SD_VER	[3:0]	RO	4'h2	SD Format Version number. ---------- Value SD Physical Spec. 0x00 Version 1.01 0x01 Version 1.10 0x02 Version 2.00 0x03-0x0F Reserved

6.14.5.4.3 I/O Enable Registers

Description：I/O Enable registers. It is used to enable, initial or reset functions.

0x0002	I/O Enable Registers (Reset 0x00)						I/O Enable	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						IOE1	Reserved
Type	RO						R/W	RO
Reset	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[7:2]	RO	6'h0	Reserved
IOE1	[1]	R/W	1'h0	Enable Function 0: Function 1 is disabled; 1: Function 1 is enabled to start initialization.
	[0]	RO	1'h0	Reserved

Note:

The host can use IOE1 as function 1 reset for error recovery. The host sequence to reset IOE1 to 0, wait until IOR1 becomes 0 and then set IOE1 to 1 again.

6.14.5.4.4 I/O Ready Registers

Description：I/O Ready registers. It is used to enable, initial or reset functions.

0x0003	I/O Ready Registers (Reset 0x00)						I/O Ready	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						IOR1	Reserved
Type	RO						RO	RO
Reset	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[7:2]	RO	6'h0	Reserved
IOR1	[1]	RO	1'h0	I/O Function Ready 0: Func1 is not ready to operate 1: Func1 is ready to operate.
	[0]	RO	1'h0	Reserved

Note:

When software set the LDO_RDY register in AHB domain, this register will set to 1 automatically, and then the R4 will response to SDIO host that the SDIO slave is ready to operate, and initial sequence will be processed.

6.14.5.4.5 Int Enable Registers

Description：Int Enable registers. It is used to enable function's interrupt.

0x0004	Int Enable Registers (Reset 0x00)						Int Enable	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						IEN1	IENM
Type	RO						R/W	R/W
Reset	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[7:2]	RO	6'h0	Reserved
IEN1	[1]	R/W	1'h0	Interrupt Enable for function 1. 0: Disable function 1 interrupt; 1: Enable function 1 interrupt. At the precondition of IENM set to 1.
IENM	[0]	R/W	1'h0	Interrupt Enable Master. 0: Disable all interrupt of functions. 1: Enable all interrupt of functions.

6.14.5.4.6 Int Pending Registers

Description：Int Pending registers. It is used to display which function is pending interrupt.

0x0005	Int Pending Registers (Reset 0x00)						Int Pending	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						INT1	Reserved
Type	RO						RO	RO
Reset	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[7:2]	RO	6'h0	Reserved
INT1	[1]	RO	1'h0	Interrupt pending for function 1. 0:Func1 interrupt is not pending 1: Func1 interrupt is pending. At the precondition of IENM and IEN1 are set to 1.
	[0]	RO	1'h0	Reserved

6.14.5.4.7 I/O Abort Registers

Description：I/O Abort registers. It is used to abort the data transfer of reset all the registers.

0x0006	I/O Abort Registers (Reset 0x00)						I/O Abort	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				RES	ASx		
Type	RO				WO	WO		
Reset	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[7:4]	RO	4'h0	Reserved
RES	[3]	WO	1'h0	I/O CARD RESET.
ASx	[2:0]	WO	3'h0	Abort Select. To abort an I/O read or write and free the SD bus. For this design just has function 1 inside, to abort the function 1 transferring, the 0x01 should be set to stop it. 0x01: Abort function 1 data transferring; 0x00, 0x02~0x07: Not support and no action.

Note:

Setting the RES to 1 shall cause all I/O functions in an SDIO to perform a soft reset.
Setting the RES to 1 does not affect the CD Disable.
Setting of the RES bit shall only be performed using CMD52.
When RES=1, the values of AS2-0 are don't-cares.
The RES bit is auto cleared, so there is no need to rewrite a value of 0.

6.14.5.4.8 Bus Intf Control Registers

Description：Bus interface control registers.

0x0007	Bus intf control (Reset 0x00)						BUS_CTRL	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CD_DIS	Reserved					BUS_WIDTH	
Type	R/W	RO					R/W	
Reset	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
CD Disable	[7]	R/W	1'h0	Connect/Disconnect the 10K-90K ohm pull-up resistor on CD / DAT3 of the card which is used for card detection. 0x00: Connect (default). 0x01: Disconnect.

				On power-on, this bit is cleared to 0. On soft-reset, this bit is not affected.
	[6:2]	RO	5'h0	Reserved
Bus Width	[1:0]	R/W	2'h0	Data bus width. 0x00: 1-bit data width 0x02: 4-bit data width On reset or power-on, these bits are cleared to 0.

6.14.5.4.9 Card Capability Registers

Description：Card Capability registers.

0x0008	Card Capability Registers (Reset 0x1F)						CARD_CAP	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		E4MI	S4MI	SBS	SRW	SMB	SDC
Type	RO		R/W	RO	RO	RO	RO	RO
Reset	0	0	0	1	1	1	1	1

~~Field Name~~	Bit	R/W	Reset Value	Description
	[7:6]	RO	2'h0	Reserved
E4MI	[5]	R/W	1'h0	Enable interrupt between blocks of data in 4-bit SD mode. 0x00: Disable 0x01: Enable
S4MI	[4]	RO	1'h1	Supports interrupt between blocks of data in 4-bit SD mode. 0x00: Not Support 0x01: Support
SBS	[3]	RO	1'h1	Card supports Suspend / Resume. 0x00: Not Support 0x01: Support
SRW	[2]	RO	1'h1	Card Supports Read Wait. 0x00: Not Support 0x01: Support
SMB	[1]	RO	1'h1	Card Supports Multi-Block. 0x00: Not Support 0x01: Support
SDC	[0]	RO	1'h1	Card Supports Direct Commands during data transfer. 0x00: Not Support 0x01: Support

6.14.5.4.10 Common CIS Pointer Registers

Description：Common CIS Pointer registers.

0x0009~0x000B	Card Capability Registers (Reset 0x1000)						COM_CIS_PT	
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	COM_CIS_PT							
Type	RO							
Reset	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name	COM_CIS_PT							
Type	RO							
Reset	0	0	0	1	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	COM_CIS_PT							
Type	RO							
Reset	0	0	0	0	0	0	0	0

Note:

There are 24 bits, not 8 bits.

Field Name	Bit	R/W	Reset Value	Description
COM_CIS_PT	[23:0]	RO	24‘h1000	This 3-byte pointer points to the start of the card’s common CIS. The common CIS contains information relation to the entire card. This card’s common CIS located within the CIS space of function 0 (0x001000).

6.14.5.4.11 Bus Suspend Registers

Description：Bus Suspend registers.

0x000C	Bus Suspend Registers (Reset 0x00)						BUS_SUSP	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						BR	BS
Type	RO						R/W	RO
Reset	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[7:2]	RO	6’h0	Reserved
BR	[1]	R/W	1’h0	Bus Release Request/Status: This bit is used to request that the addressed function release the data lines and suspend operation. 0x00: No bus release request is

				processing. 0x01: Host sends a bus release request. Once the host sets this bit to 1, the addressed function shall temporarily halt data transfer on the DAT[x] lines and suspend the command that is in process. The BR bit shall remain set to 1 until the release is complete. This bit can be cleared either by card when after the bus release is complete or by host writes it to 0 initiatives.
BS	[0]	RO	1'h0	Bus status. This bit indicates if the currently addressed function is currently executing a command which transfers data on the DAT lines. For this design, there is just function 1 inside; the only support function number is 1. 0x00: No data is transferring. 0x01: Data is transferring.

6.14.5.4.12 Function Select Registers

Description：Function Select registers.

0x000D	Function Select Registers (Reset 0x00)						FUNC_SEL
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DF	Reserved			FS			
Type	RO	RO			R/W			
Reset	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
DF	[7]	RO	1'h0	Resume Data Flag. Once the transaction is resumed, the DF indicates if more data will be transferred. 0x00: No additional data will be transferred after the function is resumed. 0x01: There is more data to transfer that will begin after the function in resumed.
	[6:4]	RO	3'h0	Reserved
FS	[3:0]	R/W	4'h0	Select Function bits. If a function is currently suspended, the writing of it's number to FSx shall re-start (resume) the data transfer

				operation When reading FSx, the value returned shall be the number of the currently addressed function. FSx Current Transaction 0000 Transaction of function 0 0001 Transaction to functions 1 0002-1111 Not defined.

6.14.5.4.13 Exec Flag Registers

Description：Execute flag registers.

0x000E	Execute Flag Registers (Reset 0x00)						EXEC_FLG	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						EX1	Reserved
Type	RO						RO	RO
Reset	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[7:2]	RO	6'h0	Reserved
EX1	[1]	RO	1'h0	Execution Flag bits These bits are used by the host to determine the current execution status of function 1 either currently executing or suspended. 0x00: Function 1 is not currently execution. 0x01: Function 1 is currently execution.
	[0]	RO	1'h0	Reserved

6.14.5.4.14 Ready Flag Registers

Description：Functions Ready flag registers.

0x000F	Functions Ready Flag Registers (Reset 0x02)						RDY_FLG	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						RF1	Reserved
Type	RO						RO	RO
Reset	0	0	0	0	0	0	1	0

Field Name	Bit	R/W	Reset Value	Description
	[7:2]	RO	6'h0	Reserved
RF1	[1]	RO	1'h1	Ready Flag bits. This bit tells the host the reads or writes busy status for function

				1. 0x00: Function 1 is busy reading or writing. 0x01: Function 1 is ready to be transferred.
	[0]	RO	1'h0	Reserved

6.14.5.4.15 FN0 Block Size Registers

Description：Function 0 Block size registers

0x0010~0x0011	Function 0 Block Size Registers (Reset 0x0000)						FN0_SIZE	
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name	FN0 Block Size (H)							
Type	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FN0 Block Size (L)							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Note:

There are 16 bits, not 8 bits.

Field Name	Bit	R/W	Reset Value	Description
FN0 Block Size	[15:0]	R/W	16'h0	This 16-bit register sets the block size for I/O block operations for function 0. Just support 0x0001 (1byte). The host is responsible for setting the appropriate value for the block size supported by function 0. This pointer is stored in little-endian format.

6.14.5.4.16 High Speed Control Registers

Description：High Speed Control registers.

0x0013	High Speed Control Registers (Reset 0x01)						HIGH_SPEED	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						EHS	SHS
Type	RO						R/W	RO
Reset	0	0	0	0	0	0	0	1

Field Name	Bit	R/W	Reset Value	Description
	[7:2]	RO	6'h0	Reserved
EHS	[1]	R/W	1'h0	Enable High-Speed. 0x00: The card operates in

				default timing mode with a clock rate up to 25MHz 0x01: The card work in high speed mode of 50MHz
SHS	[0]	RO	1'h1	Support High-Speed. This bit reports the card's ability to operate in High-Speed mode. 0x00: The card does not support high speed mode 0x01: The card support high speed mode.

6.14.5.4.17 Free Read/Write Registers

Description：Free Read and write registers.

0x00F0~0x00F3		Free Read and Write Registers (Reset 0x0000)						FRER_RW
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
Name	FRW	FRW	FRW	FRW	FRW	FRW	FRW	FRW
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	FRW	FRW	FRW	FRW	FRW	FRW	FRW	FRW
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name	FRW	FRW	FRW	FRW	FRW	FRW	FRW	FRW
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FRW	FRW	FRW	FRW	FRW	FRW	FRW	FRW
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note:

There are 32 bits, not 8 bits.

Field Name	Bit	R/W	Reset Value	Description
Free Read/ Write	[31:0]	R/W	32'h0	This 32-bit register can be freely read or write

6.14.5.5 SD Domain Memory map (FBR)

In addition to the CCCR, function 1 I/O has a 256-byte area used to allow the host to quickly determine the abilities and requirements or enable power selection and to enable software loading. The address of this area is from 0x00100 to 0x001FF. This function 1 area is structured as follows:

Table 6-17 Function Basic Register (FBR)

Function Basic Register (FBR)									
Offset	**Register Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x100-0x108	RFU								
0x109-0x10B	Pointer to Function 1 Card Information Structure (CIS)								
0x10C-0x10F	RFU								
0x110-0x111	I/O block size for Function 1								
0x112-0xFFF	RFU								

6.14.5.6 SD Domain Register Descriptions (FBR)

6.14.5.6.1 Pointer to Card Information Structure Registers

Description：Pointer to function 1 Card Information Structure.

0x0109~0x010B	**Pointer to Func1 CIS Registers (Reset 0x2000)**						**F1_CIS_PT**	
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	F1_CIS_PT							
Type	RO							
Reset	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name	F1_CIS_PT							
Type	RO							
Reset	0	0	1	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	F1_CIS_PT							
Type	RO							
Reset	0	0	0	0	0	0	0	0

Note:

There are 24 bits, not 8 bits.

Field Name	**Bit**	**R/W**	**Reset Value**	**Description**
Address pointer to Function 1 CIS	[23:0]	RO	24'h2000	These three bytes make up a 24-bit pointer to the start of the Card Information Structure (CIS) that is associated with function 1. This pointer is stored in little-endian format (LSB first). Note: The function 0 CIS pointer address is 0x01000

				The function 1 CIS pointer address is 0x02000

6.14.5.6.2 Pointer to Card Information Structure Registers

Description：Function 1 blocks size registers.

0x0110~0x0111	Function 1 Block Size Registers (Reset 0x0000)						FUNC1_SIZE	
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name	FUNC1_SIZE (H)							
Type	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FUNC1_SIZE (L)							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Note:

There are 16 bits, not 8 bits.

Field Name	Bit	R/W	Reset Value	Description
Function 1 Block Size	[15:0]	R/W	16'h0	This 16-bit register sets the block size for I/O block operations for function 1. Support range: 0x0001 (1byte) ~ 0x0200 (512bytes). The host is responsible for setting the appropriate value for the block size supported by function 1. This pointer is stored in little-endian format.

6.14.5.7 SD Domain Memory map (CIS)

The Card Information Structure provides more complete information about the card and the individual functions. The CIS is the common area to read information about all I/O functions that exist in a card. The design is based on the PC Card16 design standardized by PCMCIA. The CIS is accessed by reads to a fixed area as shown in Table 17 This one area serves the card as a Common CIS and also as the storage area for function 1. The common area and function 1 have a pointer to the start of its CIS within this memory space.

Table 6-18 Function 0 CIS

Function 0 CIS Structure									
Offset	**Value**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x1000	0x20	TPL_CODE: CISTPL_MANFID							
0x1001	0x04	TPL_LINK							
0x1002	0x00	TPLMID_MANF (L) 0000							

0x1003	0x00	TPLMID_MANF(H) 0000
0x1004	0x60	TPLMID_CARD (L) 8800
0x1005	0x22	TPLMID_CARD (H) 8800
0x1006	0x21	TPL_CODE: CISTPL_FUNCID
0x1007	0x02	TPL_LINK
0x1008	0x0C	TPLFID_FUNCTION
0x1009	0x00	TPLFID_SYSINIT
0x100A	0x22	TPL_CODE: TPL_CODE CISTPL_FUNCE
0x100B	0x04	TPL_LINK
0x100C	0x00	TPLFE_TYPE (00)
0x100D	0x01	TPLFE_FN0_BLK_SIZE (L)
0x100E	0x00	TPLFE_FN0_BLK_SIZE (H)
0x100F	0x5A	TPLFE_MAX_TRAN_SPEED (50MHz)
0x1010	0xFF	CISTPL_END

Note:

For function 0, the tuple code of CISTPL_MANFID, CISTPL_FUNCID, CISTPL_FUNCE and CISTPL_END are listed.

TPLMID_MANF: The manufacture id of SPRD is not defined and reserved to 0x0000;

TPLMID_CARD: The chip is defined to 8800(decimal) to adapt the SPRD “G” chip;

TPLFID_FUNCTION: is default 0x0c;

TPLFID_SYSINIT: is not used and reserved to 0x00;

TPLFE_FN0_BLK_SIZE: function 0 max block size is 0x01

TPLFE_MAX_TRAN_SPEED: support high speed of 50MHz.

Table 6-19 Function 1 CIS

Function 1 CIS Structure									
Offset	**Value**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x2000	0x21	TPL_CODE: CISTPL_FUNCID							
0x2001	0x02	TPL_LINK							
0x2002	0x0C	TPLFID_FUNCTION							
0x2003	0x00	TPLFID_SYSINIT							
0x2004	0x22	TPL_CODE: TPL_CODE CISTPL_FUNCE							
0x2005	0x2A	TPL_LINK							
0x2006	0x01	TPLFE_TYPE (01)							
0x2007	0x00	TPLFE_FUNCTION_INFO							
0x2008	0x00	TPLFE_STD_IO_REV							
0x2009	0x00	TPLFE_CARD_PSN							
0x200A	0x00								
0x200B	0x00								
0x200C	0x00								

0x200D 0x200E 0x200F 0x2010	0x00 0x00 0x00 0x00	TPLFE_CSA_SIZE
0x2011	0x00	TPLFE_CSA_PROPERTY
0x2012 0x2013	0x00 0x40	TPLFE_MAX_BLK_SIZE (1024 bytes)
0x2014 0x2015 0x2016 0x2017	0x00 0xFF 0xFF 0x00	TPLFE_OCR (2.0 ~ 3.6)
0x2018	0x00	TPLFE_OP_MIN_PWR
0x2019	0x00	TPLFE_OP_AVG_PWR
0x201A	0x00	TPLFE_OP_MAX_PWR
0x201B	0x00	TPLFE_SB_MIN_PWR
0x201C	0x00	TPLFE_SB_AVG_PWR
0x201D	0x00	TPLFE_SB_MAX_PWR
0x201E 0x201F	0x00 0x00	TPLFE_MIN_BW
0x2020 0x2021	0x00 0x00	TPLFE_OPT_BW
0x2022 0x2023	0x64 0x00	TPLFE_ENABLE_TIMEOUT_VAL (1s = 100*10ms)
0x2024 0x2025	0x00 0x00	TPLFE_SP_AVG_PWR_3.3V
0x2026 0x2027	0x00 0x00	TPLFE_SP_MAX_PWR_3.3V
0x2028 0x2029	0x00 0x00	TPLFE_HP_AVG_PWR_3.3V
0x202A 0x202B	0x00 0x00	TPLFE_HP_MAX_PWR_3.3V
0x202C 0x202D	0x00 0x00	TPLFE_LP_AVG_PWR_3.3V
0x202E 0x202F	0x00 0x00	TPLFE_LP_MAX_PWR_3.3V
0x2030	0xFF	CISTPL_END

Note:

TPLFE_MAX_BLK_SIZE: Function 1 max block size is 1024 bytes.

TPLFE_OCR: Support voltage range is 2.0v ~ 3.6v.

TPLFE_ENABLE_TIMEOUT_VAL: Timeout value is 1s = 100 * 10ms (unit is 10ms)

6.14.6 Application Notes

6.14.6.1 Initial sequence programming guide

To adapt our usage, there are some adjustments of the normal initial sequence which need MCU to configure some registers inside the flow. The light blue in the following figure are the added operation. The following are three methods to descript the programming flow.

DESCRIPTION:

1. **MCU** set AHB domain register SUPT_OCR with the supported OCR value. (e.g. 24'hFF00)
2. **SDIO host** sends **CMD5** with OCR value 24'h0000
3. **SDIO host** sends **CMD5** with support OCR value. (e.g. 24'h0100)
4. **MCU** adjust the LDO to a appropriate value, and wait LDO is stable, then set AHB domain register **LDO_RDY** to 1 to indicate it is ready.
5. **SDIO host** wait card_rdy (or IO_RDY, it is other description of LDO_RDY) by repeat send **CMD5** and check the response flag.
6. **SDIO host** send **CMD3** to get RCA.
7. **SDIO host** send **CMD7** to select the card (not show in the figure).
8. **SDIO host** send some **CMD52** commands to configure the CCCR/FBR registers.(not show in the figure)

PSEUDOCODE:

1. ahb_write (slave_base_addr+8'h40, { ldo_rdy=0, support_ocr})
2. sendcmd5 (0)
3. sendcmd5 (24'h100)
4. ahb_write (slave_ldo_addr, new_ldo_valud)
5. ahb_write (slave_base_addr+8'h40, {ldo_rdy=1, support_ocr})
6. while(!card_rdy) sendcmd5 (24'h100)
7. sendcmd3
8. sendcmd7(new_rca)
9. sendcmd52(write,func0,raw_yes,17'h2,8'h2,"enable func1 IO")
10. sendcmd52(write,func0,raw_yes,17'h4,8'h3,"enable func1 int")
11. sendcmd52(write,func0,raw_yes,17'h8,8'h3f,"enable int between blocks")

FIGURE:

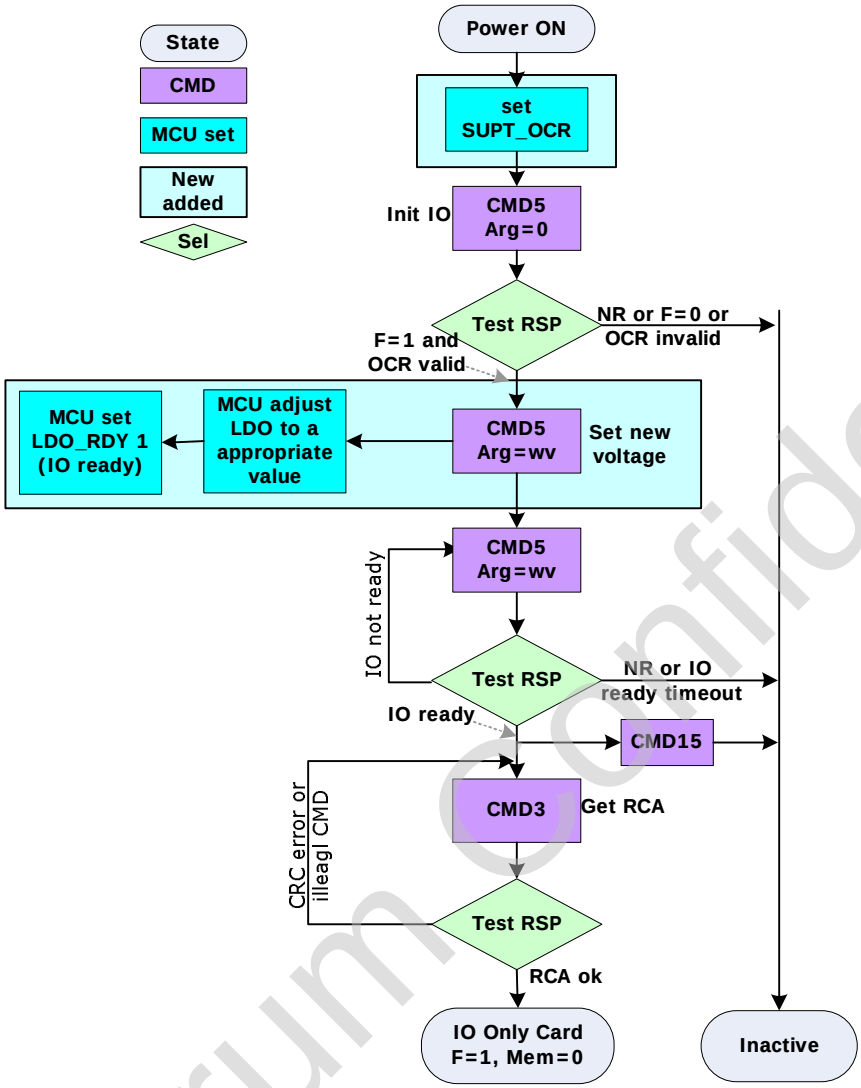


Figure 6-62 Software Initial Control Flow

6.14.6.2 Non-DMA read programming guide

1. Initial SDIO slave card
2. Enable AHB domain interrupt register SLV_RD_EN, AHB_WRDY_EN, RD_CMP_EN.
3. SDIO host send CMD53 to read function 1
4. Once the SLV_RD_STA interrupt occurred, then software read BLK_CNT and BLK_SIZE to prepare for reading data.
5. Once the AHB_WRDY_STA interrupt occurred, then software should send BLK_SIZE data to buffer data port DAT_PORT
6. Once he RD_CMP_STA interrupt occurred, then all the data is transferred over.

6.14.6.3 DMA read programming guide

1. Initial SDIO slave card
2. Enable AHB domain interrupt register DMA_INT_EN, RD_CMP_EN
3. Set SYS_ADDR, DMA_BUF_SIZE, and enable DMA_EN.
4. SDIO host send CMD53 to read function 1

5. Once the DMA_INT_EN, it means that the DMA have transfer DMA_BUF_SIZE data, then software should change a new SYS_ADDR to receive more data.
6. Once the RD_CMP_STA interrupt occurred, then all the data is transferred over

6.14.6.4 Non-DMA write programming guide

1. Initial SDIO slave card
2. Enable AHB domain interrupt register SLV_WR_EN, AHB_RRDY_EN, WR_CMP_EN.
3. SDIO host send CMD53 to write function 1
4. Once the SLV_WR_STA interrupt occurred, then software read BLK_CNT and BLK_SIZE to prepare for writing data.
5. Once the AHB_RRDY_STA interrupt occurred, then software should get BLK_SIZE data from buffer data port DAT_PORT
6. Once he WR_CMP_STA interrupt occurred, then all the data is transferred over.

6.14.6.5 DMA write programming guide

1. Initial SDIO slave card
2. Enable AHB domain interrupt register DMA_INT_EN, WR_CMP_EN
3. Set SYS_ADDR, DMA_BUF_SIZE, and enable DMA_EN.
4. SDIO host send CMD53 to write function 1
5. Once the DMA_INT_EN, it means that the DMA have transfer DMA_BUF_SIZE data, then software should change a new SYS_ADDR to transfer more data.
6. Once the WR_CMP_STA interrupt occurred, then all the data is transferred over

6.14.6.6 Suspend/resume programming guide

1. Initial SDIO slave card
2. Set relative registers based on DMA or NO-DMA transfer mode.
3. SDIO host send CMD53 to read/write function 1
4. During the data block transferred, send a CMD52 write CCCR address 8'h0C with data 8'h02 to request bus release, the R5 response flag will tell the host whether the bus is released and data suspended or not. If the BS bit is set to 1, then the transfer is suspending.
5. There are two way to resume the data transfer. One way is to send a CMD52 write CCCR address 8'h0D with data 8'h01(function 1); the second way is to send a CMD53 with the same configuration as it set previously.

6.15 Efuse

6.15.1 Overview

The electrical fuse is a type of non-volatile memory fabricated in standard CMOS logic process. This electrical fuse macro is widely used in chip ID, memory redundancy, security code, configuration setting, and feature selection, etc.

The efuse controller generates necessary timing and relative control interface to software.

This efuse controller is specially designed for TSMC product of TEF40LP32X8HD,which is a 8*32 bits electrical fuses.

6.15.2 Features

- Meet TEF40LP32X8HD timing requirement
- SW-friendly programming interface, each time 32 bits can be programmed or read
- Build-in programming protect logic, each time before programming controller will first read current efuse memory value and then decide whether programming is needed
- Build-in programming check logic, can read and check the memory data after each programming
- Build-in self-test logic(bist) , can be triggered by SW or tester

6.15.3 Signal Description

6.15.4 Function Description

6.15.4.1 Block Diagram

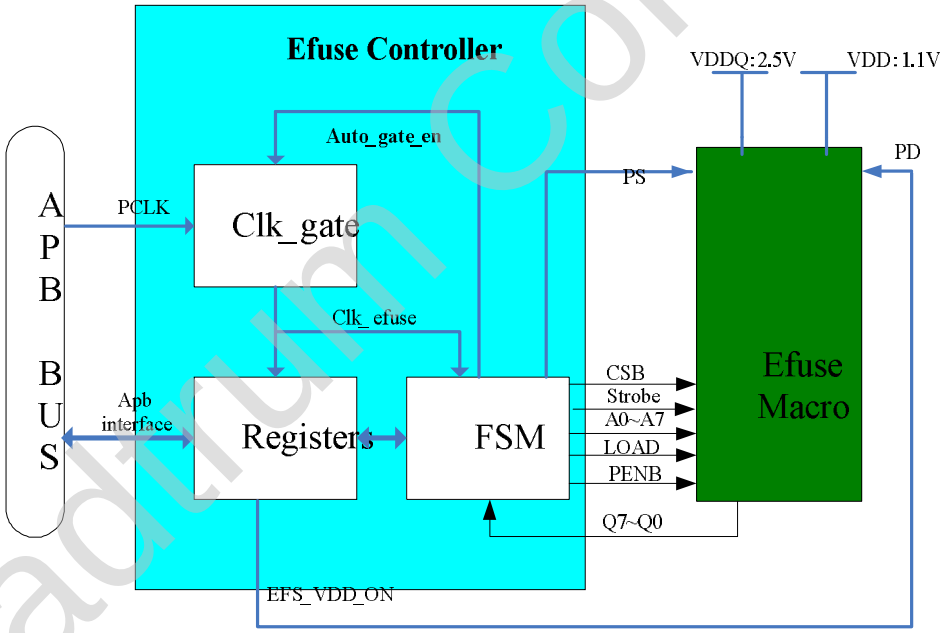


Figure 6-63 Efuse controller block diagram

6.15.4.2 Efuse connection

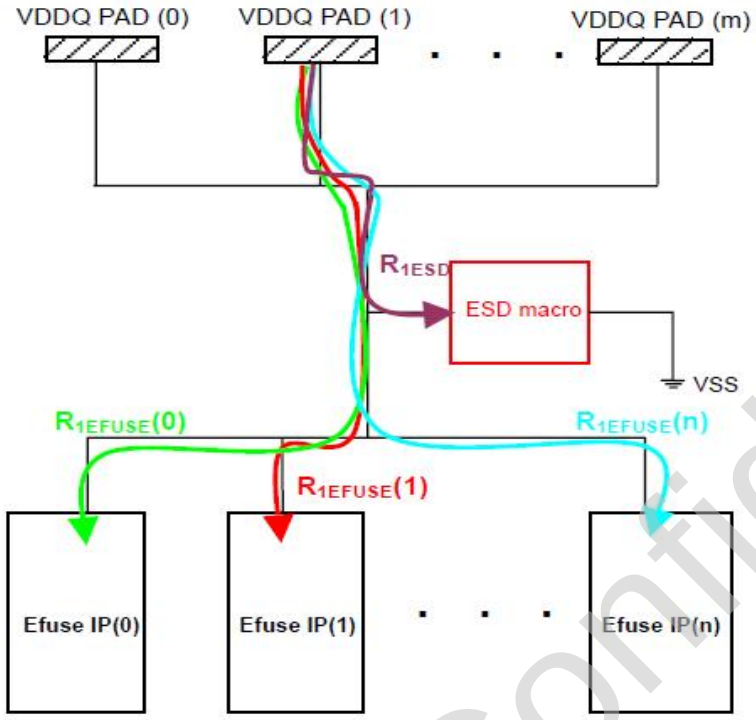


Figure 6-64 multi-efuse macro connection

6.15.4.3 Memory, Clock and Reset

Clk_efuse is the controller clock and it's directly from PCLK or divided into one half from PCLK, There is only one async reset PRESETn in this module.

6.15.5 Control Registers

6.15.5.1 Memory map

ARM base address 0x8900_0000

Offset Address	Name	Description
0x0000	EFUSE_DATA_RD	Data read from efuse memory
0x0004	EFUSE_DATA_WR	Data to be write to efuse memory
0x0008	EFUSE_BLOCK_INDEX	block index for read, program or bist.
0x000C	EFUSE_MODE_CTRL	Mode control of efuse memory
0x0010	EFUSE_PGM_PARA	Timing parameters in PGM and other control

Offset Address	Name	Description
0x0014	EFUSE_STATUS	Efuse controller internal status
0x0018	EFUSE_BLK_FLAGS	Flags for each block
0x001C	EFUSE_BLK_CLR	To clear EFUSE_BLK_FLAGS
0x0020	EFUSE_MAGIC_NUMBER	Magic number to protect efuse from un-intentionally programming

6.15.5.1.1 EFUSE_DATA_RD

Description：Data read from efuse memory

0x0000			Data read from efuse memory(Reset 0x0000_0000)										EFUSE_DATA_RD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	EFUSE_DATA_RD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	EFUSE_DATA_RD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
EFUSE_DATA_RD	[31:0]	RO	32'h0	Efuse data, If SW use efuse controller to send a read command to efuse memory, the return value will store here.

6.15.5.1.2 EFUSE_DATA_WR

Description：Data to be write to efuse memory

0x0004			Data to be write to efuse memory(Reset 0x0000_0000)										EFUSE_DATA_WR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	EFUSE_DATA_WR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	EFUSE_DATA_WR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
EFUSE_DATA_WR	[31:0]	R/W	32'h0	Efuse data to be write. If SW want to program the efuse memory, the data to be programmed will write to this register before SW issue a PGM command

6.15.5.1.3 EFUSE_BLOCK_INDEX

Description：block index for read, program or bist.

0x0008			block index for read, program or bist. (Reset 0x0000_0000)												EFUSE_BLOCK_INDEX	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	BIST_SIZE		BIST_START_INDEX				Reserved							PGM_INDEX		
Type	R/W		R/W				R/W							R/W		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved													READ_INDEX		
Type	R/W													R/W		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
READ_INDEX	[2:0]	R/W	3'h0	The efuse memory block index to be read, when efuse controller read done next time ,the read data is in regiser "EFUSE_DATA_RD ".

				Attention : if Efuse is in PGM_MODE, since the efuse controller will first read the efuse memory, so in this case SW must makesure that read_index equal to pgm_index.
	[15:3]	R/W	13'h0	Reserved
PGM_INDEX	[18:16]	R/W	3'h0	The efuse memory block index to be programmed, when issue a PGM command ,efuse controller will write regiser value of "efuse_data_wr " into efuse data block n.
	[25:19]	R/W	7'h0	Reserved
BIST_START_INDEX	[28:26]	R/W	3'h0	In efuse memory bist test mode, this field indicate the start word index
BIST_SIZE	[31:29]	R/W	3'h0	In efuse memory bist test mode, this field indicate how many words will be checked by bist logic from start index.

6.15.5.1.4 EFUSE_MODE_CTRL

Description：Mode control of efuse memory

0x000C			Mode control of efuse memory (Reset 0x0000_0000)											EFUSE_MODE_CTRL		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	BIST_START	Reserved														
Type	R/W	R/w														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved													EFUSE_STANDBY_START	EFUSE_RD_START	EFUSE_PG_START
Type	R/W													R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
EFUSE_PG_START	[0]	R/W	1'h0	Write 1 to this bit start efuse program process. Read this bit will always get 0
EFUSE_RD_START	[1]	R/W	1'h0	Write 1 to this bit start efuse read process,

				Read this bit will always get 0
EFUSE_STANDBY_START	[2]	R/W	1'h0	Write 1 to this bit will make efuse went to standby mode, Read this bit will always get 0
	[30:3]	R/W	28'h0	Reserved
BIST_START	[31]	R/W	1'h0	When BIST_SW_EN=1, write 1 to this bit will start efuse memory bist test process. this work mode is designed for efuse memory function test when mass production. DON'T active this process in normal working flow.

6.15.5.1.5 EFUSE_PGM_PARA

Description：Timing parameters in PGM and other control

0x0010	Timing parameters in PGM and other control (Reset 0x1000_0107)												EFUSE_PGM_PARA			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	PGM_EN	PCLK_DIV_EN	EFS_VDD_ON	CLK_EFS_EN	BIST_SW_EN	Reserved			BLK7_AUTO_TEST_EN	BLK6_AUTO_TEST_EN	BLK5_AUTO_TEST_EN	BLK4_AUTO_TEST_EN	BLK3_AUTO_TEST_EN	BLK2_AUTO_TEST_EN	BLK1_AUTO_TEST_EN	BLK0_AUTO_TEST_EN
Type	R/W	R/W	R/W	R/W	R/W	R/W			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							TPGM_TIME_CNT								
Type	R/W							R/W								
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1

Field Name	Bit	Type	Reset Value	Description
TPGM_TIME_CNT	[8:0]	R/W	9'h107	Clk_efuse Cycle counter, if set n, the Tpgm time will last for (n+1) clk_efuse cycle, only when PGM_EN=1 can write this field, in general case, DON'T change this field value.
	[15:9]	R/W	7'h0	Reserved
BLK0_AUTO_TEST_EN	[16]	R/W	1'h0	If set this bit, when each time SW program efuse memory block0, the controller will automatically read its value and compare with write value. If not match, the flag bit of "MEM_BLK0_ERR_FLAG" will set
BLK1_AUTO_TEST_EN	[17]	R/W	1'h0	If set this bit, when each time SW program efuse memory block1, the controller will

				automatically read its value and compare with write value. If not match, the flag bit of “MEM_BLK1_ERR_FLAG” will set
BLK2_AUTO_TEST_EN	[18]	R/W	1’h0	If set this bit, when each time SW program efuse memory block2, the controller will automatically read its value and compare with write value. If not match, the flag bit of “MEM_BLK2_ERR_FLAG” will set
BLK3_AUTO_TEST_EN	[19]	R/W	1’h0	If set this bit, when each time SW program efuse memory block3, the controller will automatically read its value and compare with write value. If not match, the flag bit of “MEM_BLK3_ERR_FLAG” will set
BLK4_AUTO_TEST_EN	[20]	R/W	1’h0	If set this bit, when each time SW program efuse memory block4, the controller will automatically read its value and compare with write value. If not match, the flag bit of “MEM_BLK4_ERR_FLAG” will set
BLK5_AUTO_TEST_EN	[21]	R/W	1’h0	If set this bit, when each time SW program efuse memory block5, the controller will automatically read its value and compare with write value. If not match, the flag bit of “MEM_BLK5_ERR_FLAG” will set
BLK6_AUTO_TEST_EN	[22]	R/W	1’h0	If set this bit, when each time SW program efuse memory block6, the controller will automatically read its value and compare with write value. If not match, the flag bit of “MEM_BLK6_ERR_FLAG” will set
BLK7_AUTO_TEST_EN	[23]	R/W	1’h0	If set this bit, when each time SW program efuse memory block7, the controller will automatically read its value and compare with write value. If not match, the flag bit of “MEM_BLK7_ERR_FLAG” will set
	[26:24]	R/W	3’h0	Reserved
BIST_SW_EN	[27]	R/W	1’h0	Write 1 to this bit will enable bist test mode. This mode is for mass production function test, DON’T set this bit in normal working mode.
CLK_EFS_EN	[28]	R/W	1’h1	Set to 1 will open clk_efs This bit must set before efuse controller is in use
EFUSE_VDD_ON	[29]	R/W	1’h0	Set this bit will open 1.1v power supply for efuse memory, before any operation towards to efuse memory this bit have to set to 1.
PCLK_DIV_EN	[30]	R/W	1’h0	When set, the clk_efuse will equal to a half of PCLK, otherwise will equal to PCLK. This bit is for timing adjust and debug use, in most case no need and don’’t change its default value
PGM_EN	[31]	R/W	1’h0	Only set this bit can SW write register field of “TPGM_TIME_CNT” and start PGM

				mode (this bit used to protect software unexpectedly programmed efuse memory)

6.15.5.1.6 EFUSE_STATUS

Description：Efuse controller internal status

0x0014	Efuse controller internal status(Reset 0x0000_0000)												EFUSE_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										BIST_BUSY	BIST_FAIL	Reserved	STANDBY_BUSY	READ_BUSY	PGM_BUSY
Type	R/W										RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
PGM_BUSY	[0]	R0	1'h0	"1" indicate efuse memory in programming mode
READ_BUSY	[1]	R0	1'h0	"1" indicate efuse memory in read mode
STANDBY_BUSY	[2]	R0	1'h0	"1" indicate efuse memory in standby mode
	[3]	R0	1'h0	Reserved
BIST_FAIL	[4]	R0	1'h0	"1" will indicate that bist test failed
BIST_BUSY	[5]	R0	1'h0	"1" will indicate that bist test is in process
	[31:6]	R/W	26'h0	Reserved

6.15.5.1.7 EFUSE_BLK_FLAGS

Description：Flags for each block

0x0018			Flags for each block (Reset 0x0000_0000)										EFUSE_BLK_FLAGS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BLK7_ERR_FLAG	BLK6_ERR_FLAG	BLK5_ERR_FLAG	BLK4_ERR_FLAG	BLK3_ERR_FLAG	BLK2_ERR_FLAG	BLK1_ERR_FLAG	BLK0_ERR_FLAG	BLK7_PROT_FLAG	BLK6_PROT_FLAG	BLK5_PROT_FLAG	BLK4_PROT_FLAG	BLK3_PROT_FLAG	BLK2_PROT_FLAG	BLK1_PROT_FLAG	BLK0_PROT_FLAG
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
BLK0_PROT_FLAG	[0]	R0	1'h0	If the SW send a PGM command to memory block0, and the controller found this memory block need to be protected(which means the highest bit is 1), this bit will set to 1
BLK1_PROT_FLAG	[1]	R0	1'h0	If the SW send a PGM command to memory block1, and the controller found this memory block need to be protected(which means the highest bit is 1), this bit will set to 1
BLK2_PROT_FLAG	[2]	R0	1'h0	If the SW send a PGM command to memory block2, and the controller found this memory block need to be protected(which means the highest bit is 1), this bit will set to 1
BLK3_PROT_FLAG	[3]	R0	1'h0	If the SW send a PGM command to memory block3, and the controller found this memory block need to be protected(which means the highest bit is 1), this bit will set to 1
BLK4_PROT_FLAG	[4]	R0	1'h0	If the SW send a PGM command to memory block4, and the controller found this memory block need to be protected(which means the highest bit is 1), this bit will set to 1
BLK5_PROT_FLAG	[5]	R0	1'h0	If the SW send a PGM command to memory block5, and the controller found this memory block need to be protected(which means the highest bit is 1), this bit will set to 1
BLK6_PROT_FLAG	[6]	R0	1'h0	If the SW send a PGM command to memory block6, and the controller found this memory block need to be protected(which means the highest bit is 1), this bit will set to 1

BLK7_PROT_FLAG	[7]	R0	1'h0	If the SW send a PGM command to memory block7, and the controller found this memory block need to be protected(which means the highest bit is 1), this bit will set to 1
BLK0_ERR_FLAG	[8]	R0	1'h0	If BLK0_AUTO_TEST_EN is set, and controller compared the value read after PGM from the same block, and found the two value not match, this bit will set as an error flag. But if this block is protected, the PGM command in-fact not really send, so this bit will not set.
BLK1_ERR_FLAG	[9]	R0	1'h0	If BLK1_AUTO_TEST_EN is set, and controller compared the value read after PGM from the same block, and found the two value not match, this bit will set as an error flag. But if this block is protected, the PGM command in-fact not really send, so this bit will not set.
BLK2_ERR_FLAG	[10]	R0	1'h0	If BLK2_AUTO_TEST_EN is set, and controller compared the value read after PGM from the same block, and found the two value not match, this bit will set as an error flag. But if this block is protected, the PGM command in-fact not really send, so this bit will not set.
BLK3_ERR_FLAG	[11]	R0	1'h0	If BLK3_AUTO_TEST_EN is set, and controller compared the value read after PGM from the same block, and found the two value not match, this bit will set as an error flag. But if this block is protected, the PGM command in-fact not really send, so this bit will not set.
BLK4_ERR_FLAG	[12]	R0	1'h0	If BLK4_AUTO_TEST_EN is set, and controller compared the value read after PGM from the same block, and found the two value not match, this bit will set as an error flag. But if this block is protected, the PGM command in-fact not really send, so this bit will not set.
BLK5_ERR_FLAG	[13]	R0	1'h0	If BLK5_AUTO_TEST_EN is set, and controller compared the value read after PGM from the same block, and found the two value not match, this bit will set as an error flag. But if this block is protected, the PGM command in-fact not really send, so this bit will not set.
BLK6_ERR_FLAG	[14]	R0	1'h0	If BLK6_AUTO_TEST_EN is set, and controller compared the value read after PGM from the same block, and found the two value not match, this bit will set as an error flag. But if this block is protected, the PGM command in-fact not really send, so this bit will not set.
BLK7_ERR_FLAG	[15]	R0	1'h0	If BLK7_AUTO_TEST_EN is set, and

				controller compared the value read after PGM from the same block, and found the two value not match, this bit will set as an error flag. But if this block is protected, the PGM command in-fact not really send, so this bit will not set.
	[31:16]	R/W	16'h0	Reserved

6.15.5.1.8 EFUSE_BLK_FLAGS_CLR

Description：To clear EFUSE_BLK_FLAGS

0x001C		To clear EFUSE_BLK_FLAGS (Reset 0x0000_0000)											EFUSE_BLK_FLAGS_CLR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BLK7_ERR_FLAG_CLR	BLK6_ERR_FLAG_CLR	BLK5_ERR_FLAG_CLR	BLK4_ERR_FLAG_CLR	BLK3_ERR_FLAG_CLR	BLK2_ERR_FLAG_CLR	BLK1_ERR_FLAG_CLR	BLK0_ERR_FLAG_CLR	BLK7_PROT_FLAG_CLR	BLK6_PROT_FLAG_CLR	BLK5_PROT_FLAG_CLR	BLK4_PROT_FLAG_CLR	BLK3_PROT_FLAG_CLR	BLK2_PROT_FLAG_CLR	BLK1_PROT_FLAG_CLR	BLK0_PROT_FLAG_CLR
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
BLK0_PROT_FLAG_CLR	[0]	R0	1'h0	Write this bit "1" will clear flag bit "BLK0_PROT_FLAG", read this bit will always get 0
BLK1_PROT_FLAG_CLR	[1]	R0	1'h0	Write this bit "1" will clear flag bit "BLK1_PROT_FLAG", read this bit will always get 0
BLK2_PROT_FLAG_CLR	[2]	R0	1'h0	Write this bit "1" will clear flag bit "BLK2_PROT_FLAG", read this bit will always get 0
BLK3_PROT_FLAG_CLR	[3]	R0	1'h0	Write this bit "1" will clear flag bit "BLK3_PROT_FLAG", read this bit will always get 0
BLK4_PROT_FLAG_CLR	[4]	R0	1'h0	Write this bit "1" will clear flag bit "BLK4_PROT_FLAG", read this bit will always get 0
BLK5_PROT_FLAG_CLR	[5]	R0	1'h0	Write this bit "1" will clear flag bit "BLK5_PROT_FLAG", read this bit will always get 0
BLK6_PROT_FLAG_CLR	[6]	R0	1'h0	Write this bit "1" will clear flag bit

				"BLK6_PROT_FLAG", read this bit will always get 0
BLK7_PROT_FLAG_CLR	[7]	R0	1'h0	Write this bit "1" will clear flag bit "BLK7_PROT_FLAG", read this bit will always get 0
BLK0_ERR_FLAG_CLR	[8]	R0	1'h0	Write this bit "1" will clear flag bit "BLK0_ERR_FLAG", read this bit will always get 0
BLK1_ERR_FLAG_CLR	[9]	R0	1'h0	Write this bit "1" will clear flag bit "BLK1_ERR_FLAG", read this bit will always get 0
BLK2_ERR_FLAG_CLR	[10]	R0	1'h0	Write this bit "1" will clear flag bit "BLK2_ERR_FLAG", read this bit will always get 0
BLK3_ERR_FLAG_CLR	[11]	R0	1'h0	Write this bit "1" will clear flag bit "BLK3_ERR_FLAG", read this bit will always get 0
BLK4_ERR_FLAG_CLR	[12]	R0	1'h0	Write this bit "1" will clear flag bit "BLK4_ERR_FLAG", read this bit will always get 0
BLK5_ERR_FLAG_CLR	[13]	R0	1'h0	Write this bit "1" will clear flag bit "BLK5_ERR_FLAG", read this bit will always get 0
BLK6_ERR_FLAG_CLR	[14]	R0	1'h0	Write this bit "1" will clear flag bit "BLK6_ERR_FLAG", read this bit will always get 0
BLK7_ERR_FLAG_CLR	[15]	R0	1'h0	Write this bit "1" will clear flag bit "BLK7_ERR_FLAG", read this bit will always get 0
	[31:16]	R/W	16'h0	Reserved

6.15.5.1.9 EFUSE_MAGIC_NUMBER

Description： magic number to protect efuse from un-intentionally programming

0x0020			magic number to protect efuse from un-intentionally programming (Reset 0x0000_0000)										EFUSE_MAGIC_NUMBER			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	EFUSE_MAGIC_NUMBER															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
EFUSE_MAGIC_NUMBER	[15:0]	R/W	16'h0	Magic number, only when this field is 0x8810, the Efuse programming command can be handle. So if SW want to program efuse memory, except open clocks and power, 2 other conditions must be met : (1) PGM_EN =1; (2) EFUSE_MAGIC_NUMBER = 0x8810
	[31:16]	R/W	16'h0	Reserved

6.15.6 Application Notes

6.15.6.1 Clock structure

Before any operation towards efuse macro through efuse controller, you need set "efs_eb" to open efuse controller clock, and then set "CLK_EFS_EN" to open accelerator clock.

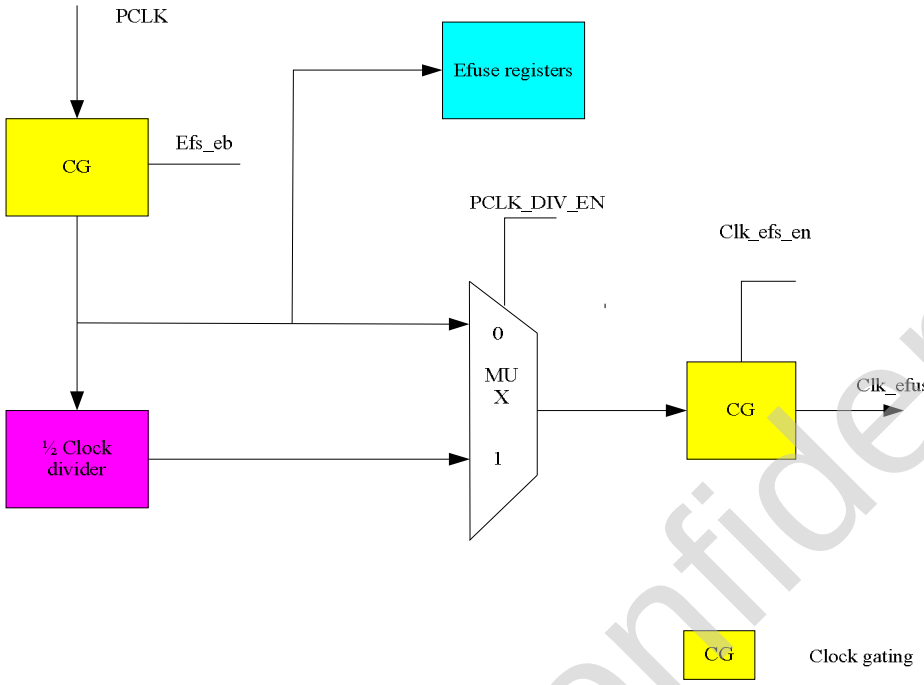


Figure 6-65 clock structure for efuse controller

6.15.6.2 Efuse memory power supply

As specification requires, efuse memory need two power supply : VDDQ @ 2.5V+/- 10% and VDD @ 1.1V+/- 10%, In SC6820, VDDQ use the 2.5V PLL power supply and VDD use 1.1v digital core (40nm technology) power supply.

When EFUSE_VDD_ON is set , the VDD power will open and efuse memory can be ready for programming or read

6.15.6.3 Read mode timing sequence

In physical view, The TEF40LP32X8HD is a 32 rows and 8 columns memory array, each time only one rows can be read at the same time, but this efuse controller re-grouped the memory array and from sofware's perspective, 4 rows are together and each time they can be accessed for read, which are 32bits

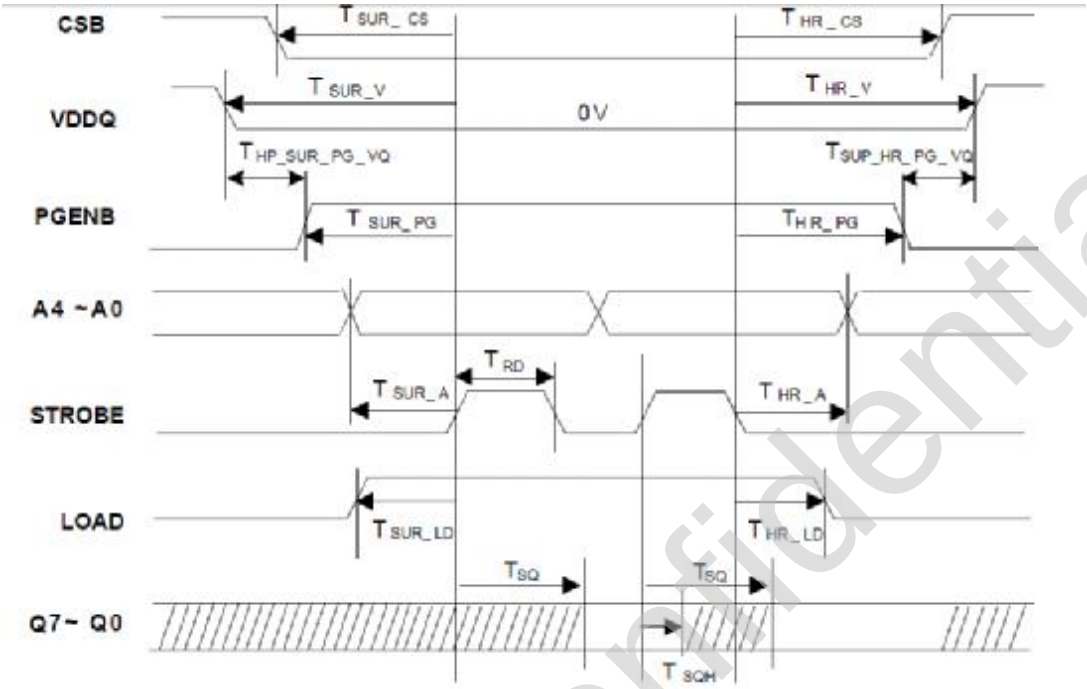


Figure 6-66 efuse memory read timing

6.15.6.4 Programming mode(PGM) timing sequence

In physical, each time only one bit is allowed to be programmed , which is in-fact an irreversible erase process from 1 to 0, efuse controller packaged such process and each time one work, that is 32 bits, can be programmed as your will.

Attention : before efuse controller program a word to relative memory, it will previously read this memory value and if found the highest bit of this memory is 0, then the efuse PGM will abort and no data will write to this memory, this function is the system department's requirement.

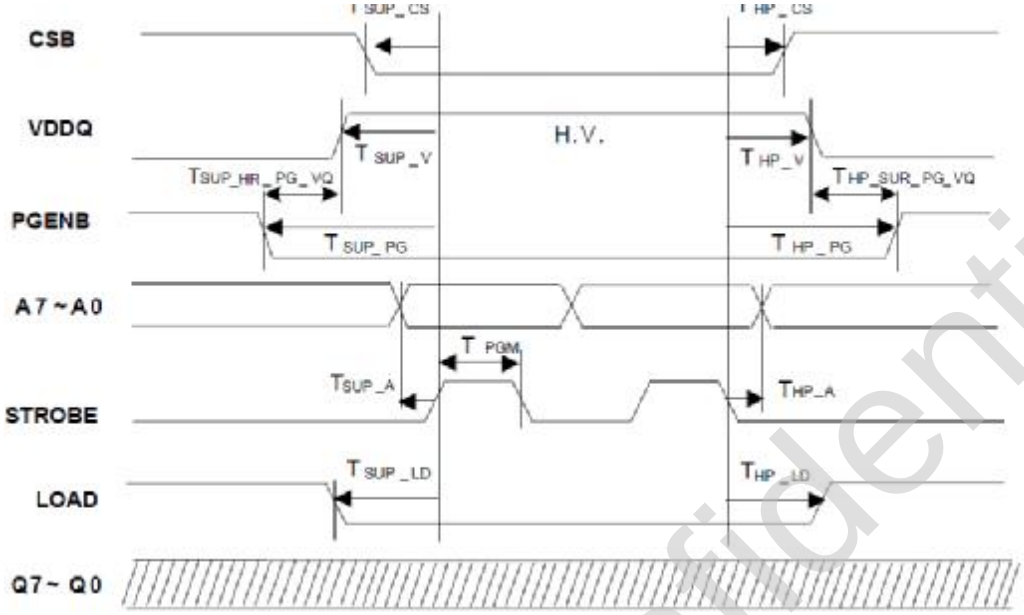


Figure 6-67 efuse memory program timing

6.15.6.5 Standby mode

When CSB = 1, PENB =1 and VDDQ is floating or equal to 0v, the Efuse memory is in standby mode, the power consumption is the smallest in this mode.

6.15.6.6 Program in-active mode

When CSB=1, PENB=0 and VDDQ is 2.5v+/-10%, the efuse memory is in program inactive mode.

6.15.6.7 Programming notes

6.15.6.7.1 Power on & Power off

Before using efuse controller to send any command to efuse memory , SW need to open efuse power according to following steps :

(1) set global control bit of “efs_eb”, that is bit 7 in 0x8b00_0007;
(2) set “EFUSE_VDD_ON” in 0x8900_0010 bit 29, to open power supply for VDD

after finished all operation to efuse memory , then “EFUSE_VDD_ON” and “efs_eb” should be cleared for power saving

6.15.6.7.2 PGM flow

(1) Write “PGM_EN”and “CLK_EFUSE_EN” in “EFUSE_PGM_PARA” register to enable PGM mode. (0x8900_0010 bit 28 & 31)
(2) Write “EFUSE_MAGIC_NUMBER” as 0x8810 (0x8900_0020)
(3) write the value to be programmed to register “Efuse_data_wr” (0x8900_0004)
(4) write the memory index to be programmed to register “PGM_INDEX” (0x8900_0008 bits 16 to 18)
(5) write bit of “EFUSE_PG_START” in register “EFUSE_MODE_CTRL” to 1 to start programming efuse memory (0x8900_000C bit 0)
(6) SW then polling the status of “PGM_BUSY” in “EFUSE_STATUS” register (0x8900_0014 bit 0), if this bit cleared, the programming process finished
(7) After PGM finished, SW can read “BLKX_PROT_FLAG” to know whether the previous programming succeed or not (X equal to the PGM_INDEX value)
(8) clear “PGM_EN” in “EFUSE_PGM_PARA” register to prohibit un-expected programming command

In most case, there is no need to change the TPGM_TIME_CNT and the default value will be OK

6.15.6.7.3 Read flow

After PGM , SW can read the efuse memory value according to the following steps:

(1) Wite “CLK_EFS_EN” in “EFUSE_PGM_PARA” register to pen efuse clock. (0x8900_0010 bit 28)
(2) write “EFUSE_RD_START” in register “EFUSE_MODE_CTRL” to 1 to start reading process from efuse memory(0x8900_000C bit 1)
(3) polling bit of “READ_BUSY” in “EFUSE_STATUS” register(0x8900_0014 bit 1), after it cleared to zero, the read flow is finished and the return value is in “EFUSE_DATA_RD” (0x8900_0000)

6.15.6.7.4 Standby flow

SW can set “EFUSE_STANDBY_START” (0x8900_000C bit 2)to let efuse macro go to standby status. After read/write done, the efuse controller can also control efuse macro go to this mode automatically.

6.15.6.7.5 Software trigger bist process

Software can enable bist test process, to check some content of efuse memory is programmed or not.

(1) SW write register field “BIST_START_INDEX” and “ BIST_END_INDEX”
(2) SW wite “BIST_SW_EN” and “CLK_EFS_EN” to 1
(3) SW write “BIST_START” 1 to start bist check

The bist test process will read the memory value from “BIST_START_INDEX” to “BIST_END_INDEX

” and if find its value are not zero, then an “BIST_FAIL” flag will set after “BIST_BUSY” return to zero.

7 Multi-Media Subsystem

7.1 Dcam

7.1.1 Overview

The DCAM integrates several multimedia hardware accelerator include camera interface, image resizing and videophone path. Both YCbCr and JPEG data can be captured by camera interface. The image signal process such as decimation, trimming, scaling, RGB data conversion and etc functions can be transacted in review module.

Change list:

- New CAP module to support SPI, CCIR 656 1 bit, 2 bit and 4 bit.
- Modify the endian adjustment.
- Support output data YUV420 YUV422 and RGB565 in capture path1.
- Modify the frm_addr from 18 bits to 32 bits.
- Add rotation function in review path.

7.1.2 Features

Camera capture path:

- ITU_R 601/ITU_R 656 format input support. 8 bit YCbCr is supported.
- Support up to 5M pixel CMOS sensor's JPEG compression mode;
- Support SPI Camera Interface.
- Support 601/656 1bit, 2bit, 4bit and 8bit Camera Interface.
- Programmable polarity of Vsync and Href signals.
- Support scaling down/up function, scaling factor from 1/4 to 4;
- The scaling hardware support for output resolutions up to 960 pixel ;
- Support image crop and down sample in camera interface;
- Support frame decimation in camera interface;
- Sensor line and frame data error auto detect;
- Support two separate capture path. one for preview another for capture;if the second camera path is active, the review path must be disabled. If both two capture path is active, trimming of two path must be active, and scaling of them can't be bypassed.

- Support trimming and down sample in both capture path; if enable subsample, trimming must be enabled too.
- Support YUV422 ,RGB565 and YUV420 format data out in both capture path ;

Image resizing path:

- Support two scaling mode: normal and slice;
- Support scaling down/up function, scaling factor from 1/4 to 4;
- in normal mode ,restricted to output width less than 960 pixel for display;
- If using slice review mode, support output horizontal size up to 4092;
- Support different YUV input format, include: YUV422,YUV420,YUV400;
- Support Y,U,V 3 frame data format input scaling;
- Support different output data format, YUV422 and RGB565,and support YUV420 output format in normal scaling mode;
- Support image trimming and down sample in review mode. 1/2, 1/4,1/8,1/16 down sample in X and Y direction;
- Support RGB2YUV and YUV2RGB conversion;
- Support different RGB format input, RGB888, RGB565;
- Support rotation function in resizing path.

Rotation function:

- Support 90 270 180 and horizontal mirror rotation mode;
- Support rotation image width up to 960 pixel;
- The rotation function can only be active in resizing path or capture path 2;

7.1.3 Signal Description

7.1.3.1 Diagram of Camera Interface:

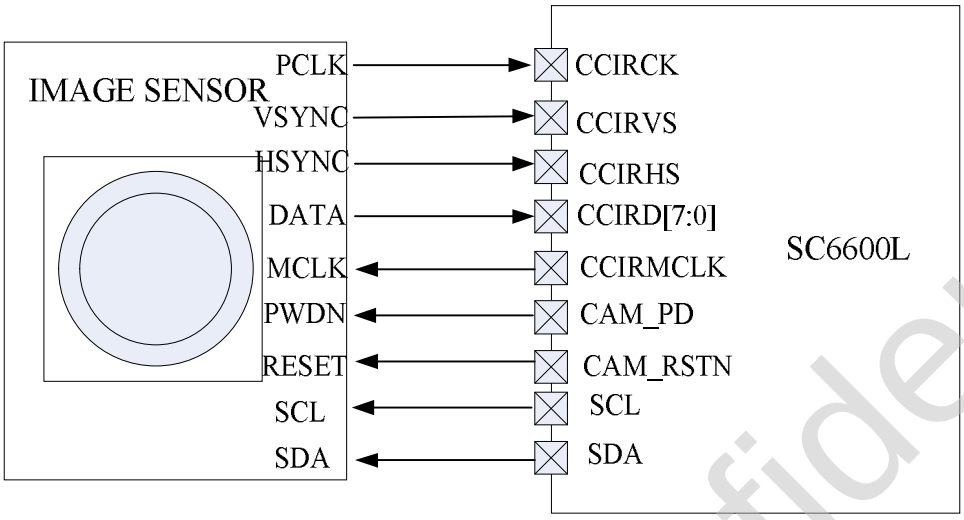


Figure 7.1-1 interface of CAM_IF

7.1.3.2 Signal description

Signal name	I/O	Width	Description
CCIRCK	I	1	Pixel Clock, driven by the Camera Module
CCIRVS	I	1	Frame Sync, driven by the Camera Module
CCIRHS	I	1	Horizontal Sync, driven by the Camera Module
CCIRD	I	[7:0]	Pixel Data driven by the Camera Module
CCIRMCK	O	1	Clock to external Camera
CAM_PD	O	[1:0]	Software Power Down for the Camera Module
CAM_RSTN	O	1	Software Reset for the Camera Module

Camera I/F connections with different mode sensor:

	SPI	CCIR656(4 bits)	CCIR656(2 bits)	CCIR656(1 bits)
CCIRCK	PCLK	PCLK	PCLK	PCLK
CCIRVS	CS			
CCIRHS				
CCIRD[0]	SPID	CCIRD[0]	CCIRD[0]	CCIRD[0]
CCIRD[1]		CCIRD[1]	CCIRD[1]	
CCIRD[2]		CCIRD[2]		

CCIRD[3]		CCIRD[3]		
CCIRD[4]				
CCIRD[5]				
CCIRD[6]				
CCIRD[7]				
SCL	SCL	SCL	SCL	SCL
SDA	SDA	SDA	SDA	SDA

7.1.3.3 Clock of Camera Interface

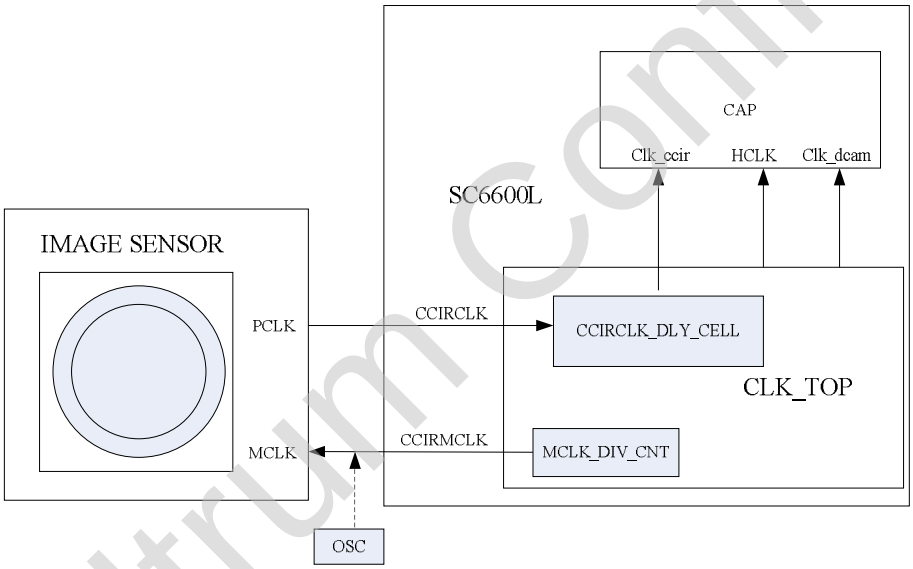


Figure 1.1-2 clock of CAM_IF

Camera Interface includes three clock domains. The AHB bus clock: HCLK; CCIR Clock from sensor: CCIRCK and clock to dcam_top; clk_dcam. The AHB bus clock must be faster than dcam clock. The dcam clock should be faster than Sensor clock.

The AHB slave works in AHB domain. Most DCAM component except some logic in CAP works in DCAM clock domain. The DCAM clock can work at 48M, 64M and 96M.

The MCLK of sensor can be supplied from Chip or external oscillator. A extra CLK DLY cell have been inserted on CCIRCK path, which can adjust the CCIRCK phase.

Note:

- The frequency of sensor clock must slower than dcam clock ;

7.1.3.4 Timing Diagram of Camera IF

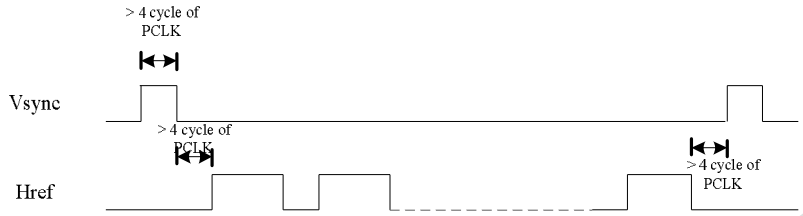


Figure 7.1-3 timing diagram of Sync signal

CCIR601 YUV mode timing diagram:

Vsync/Href (register Sync_polarity =01)

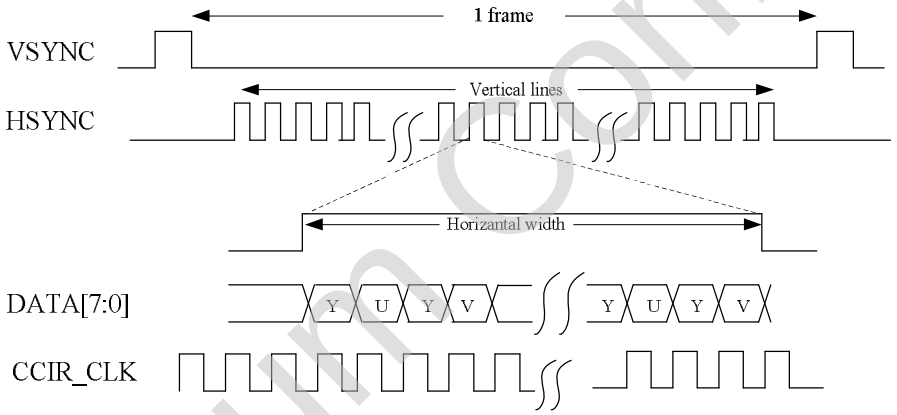


Figure 7.1-4 timing diagram of CAM_IF 601

JPEG data timing diagram is similar with YUV data mode.

Following is an example of Vsynv/Hsync(register Sync_polarity =01):

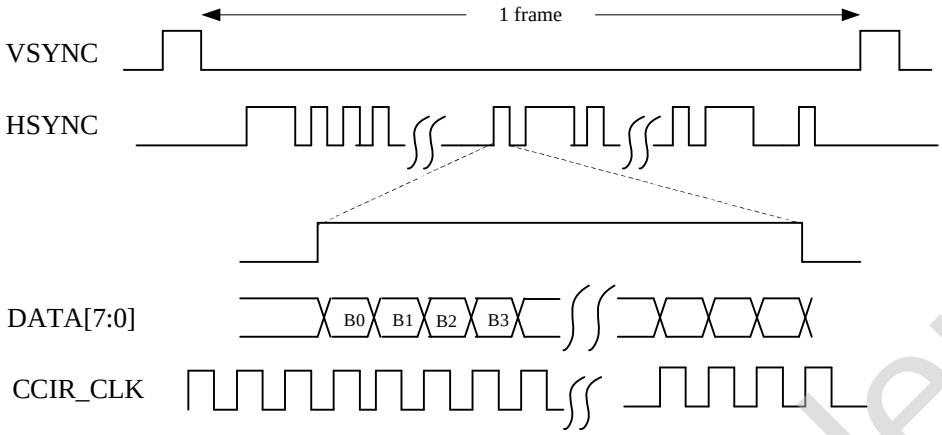


Figure 7.1-5 JPG timing diagram of CAM_IF

SPI mode:

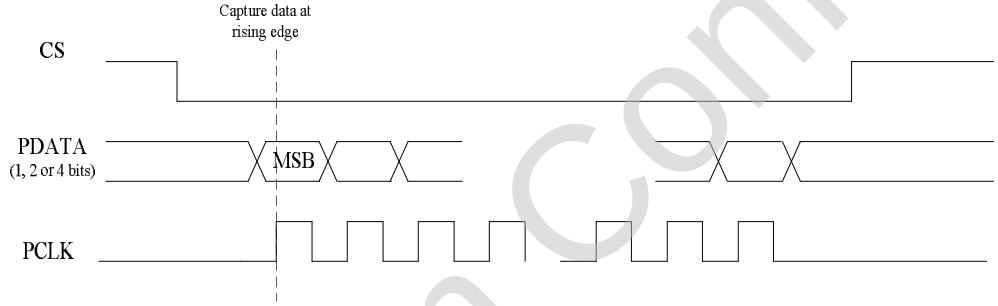
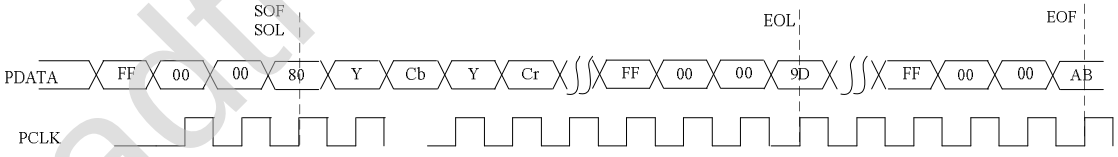


Figure 7.1-6 timing diagram of CAM_IF SPI mode

CCIR 656 mode:



7.1.4 Function Description

7.1.4.1 Diagram of DCAM_TOP

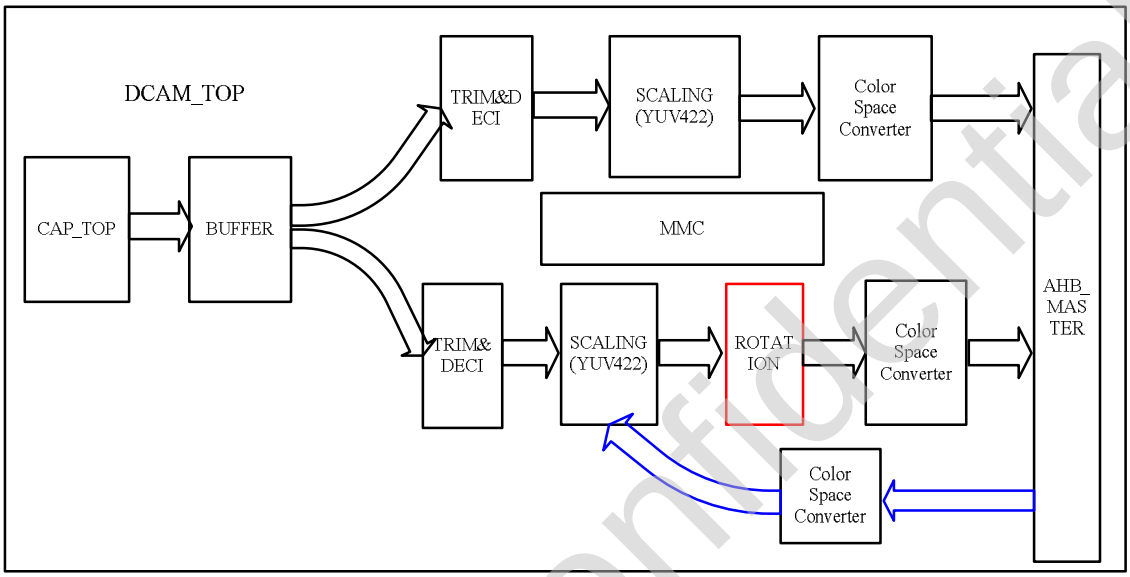


Figure 7.1-8 diagram of DCAM_TOP

CAP_TOP:

This module was in charge of transacting YUV or JPEG data from sensor. It support down-sampling ,image-trimming, frame decimation and etc;

1. Interface timing
1.1. Support YUV4:2:2 and JPEG compression formats;
1.2. Support Vref/Vsync and Href/Hsync.
1.3. Support CCIR656 interface 1bit,2bit and4bit in YUV4:2:2 format.
1.4. Support SPI sensor.
1.5. Support sensor's output clock polarity inversion.
1.6. Sensor's input clock is configurable by ARM.
2. Frame control
2.1. Support decimation on frames. The decimation factors can be configured by ARM.
2.2. Which frame is captured could be configured by ARM.
3. Image Size
3.1. Support YUV4:2:2 format sensors up to 4092x4092.
3.2. Support various image sizes smaller than 4092x4092, which is configured by ARM.

3.3. Support decimation on line and column in YUV4:2:2. The decimation unit on the horizontal and vertical direction are 1. The decimation factors can be configured independently by ARM.

3.4. Support trimming images from the sensor in YUV4:2:2. The start point and the end point are configured by ARM.

4. Whole module could be disabled by ARM based on DCAM working mode.

SCALING:

1. Support unsigned YUV422 input, The input data can be from two source, YUYV DATA from CAP, Y frame and UV frame from AHB Master.
2. Support trimming function before scaling. And the timing size can be programmed by ARM
3. Scaling factor from 1/4 to 4.
4. In slice mode, output horizontal size is up to 4092.
5. Normal mode scaling output horizontal size up to 960.
6. the 2D scalar has such work parameters:

(1) Horizontal scaling

For Y component, using fixed 8-tap and 8-phase filter;

For U/V component, using fixed 4-tap and 8-phase filter;

(2) Vertical scaling down

For Y component, using variable tap and 8-phase filter, $2 <= K_Y <= 4M/N <= 8$;

For U/V component, using variable tap and 8-phase filter, $2 <= K_C = K_Y <= 8$;

(3) Vertical scaling up

For Y component, using 4-tap and 8-phase filter;

For U/V component, using 4-tap and 8-phase filter;

7. Whole module could be disabled bypassed by ARM based on DCAM working mode.

NOTE:

The input and output width of scaling module must be multiple of 4.

The trimming function only be active in review mode. And it the trimming start and trimming size must be 4 aligned.

Color space conversion:

in charge of data format conversion between YUV and RGB.

YUV2RGB: Convert YUV444 to RGB565

- Support YUV422 to RGB565 conversion. The input data format to this module should be YUV 422.The conversion coefficients is fixed .

The algorithm for YUVTORGB is shown below:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & \frac{359}{256} \\ 1 & -\frac{88}{256} & -\frac{183}{256} \\ 1 & \frac{454}{256} & 0 \end{bmatrix} \begin{bmatrix} Y \\ U \\ V \end{bmatrix} + \begin{bmatrix} -180 \\ 136 \\ -227 \end{bmatrix}$$

- Support dithering function and it can be enable or disable by software.

RGB2YUV: Convert RGB888 or RGB565 to YUV422, we use fixed conversion coefficient.

The formula as below shows:

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} \frac{77}{256} & \frac{150}{256} & \frac{29}{256} \\ -\frac{43}{256} & -\frac{85}{256} & \frac{128}{256} \\ \frac{128}{256} & -\frac{107}{256} & -\frac{21}{256} \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix} + \begin{bmatrix} 0 \\ 128 \\ 128 \end{bmatrix}$$

DCAM_AHB_MASTER:

1. There are two output ports and one input port in DCAM AHB Master Interface, only one port can be active at one time.
2. Support an arbiter between Port CAM, Port REV and Port YUV2RGB. The priority of Port CAM is highest.
3. The interval between two burst can be configured by register.
4. The AHB interface, DCAM VDB port and AHB part works in clk_dcam domain,

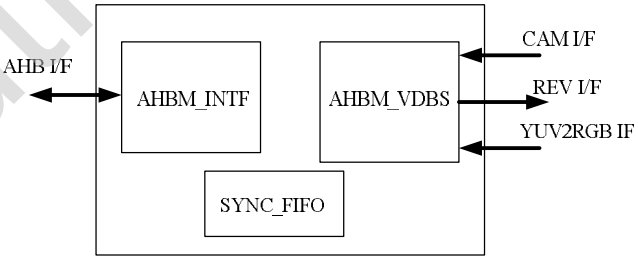


Figure 7.1-9 diagram of AHB master

7.1.4.2 Camera capture path:

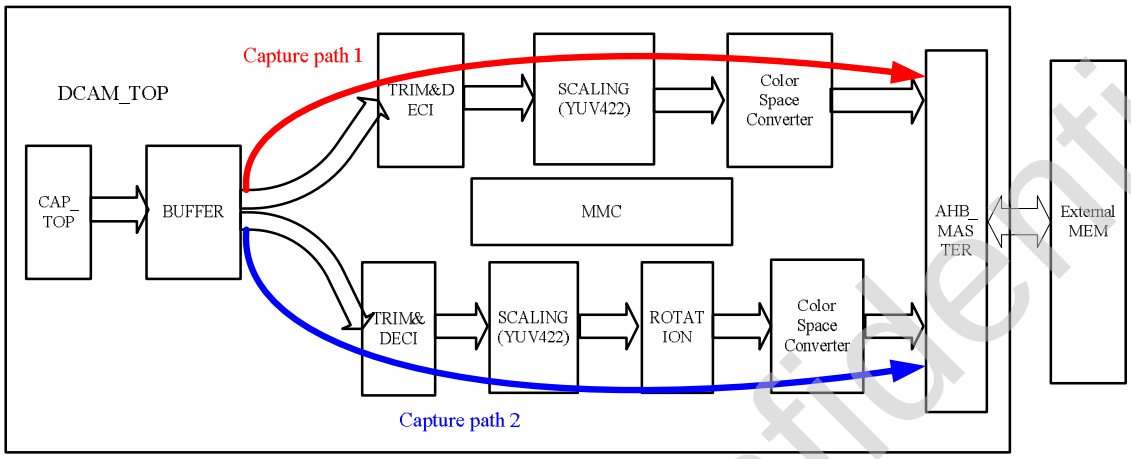


Figure 7.1-10 camera data path

Two separate camera capture path is supported in DCAM module, which can be active simultaneously. Both YUV422 YUV420 RGB565 and JPEG data can be capture by camera path 1.The output data from path1 can be YUV422 YUV420 and RGB565.

7.1.4.3 Image resizing path

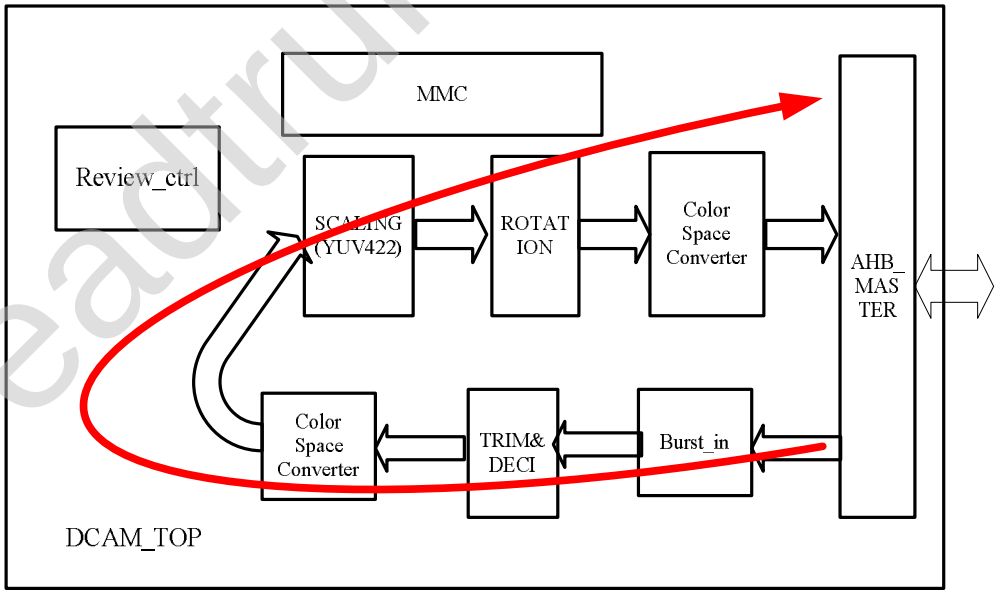


Figure 7.1-11 resizing data path

In image resizing path, support different input data format scaling, include YUV422, YUV420, YUV400, YUV420(3 frame), RGB565 and RGB888. And support different output data format, include YUV422, YUV420 and RGB565. Limited by the size of line buffer, the output width must less than 960 in normal scaling mode. In slice mode, the output data width can be up to 4092.

Image resizing path can't be active if enable camera path 2.

7.1.4.4 Video phone path

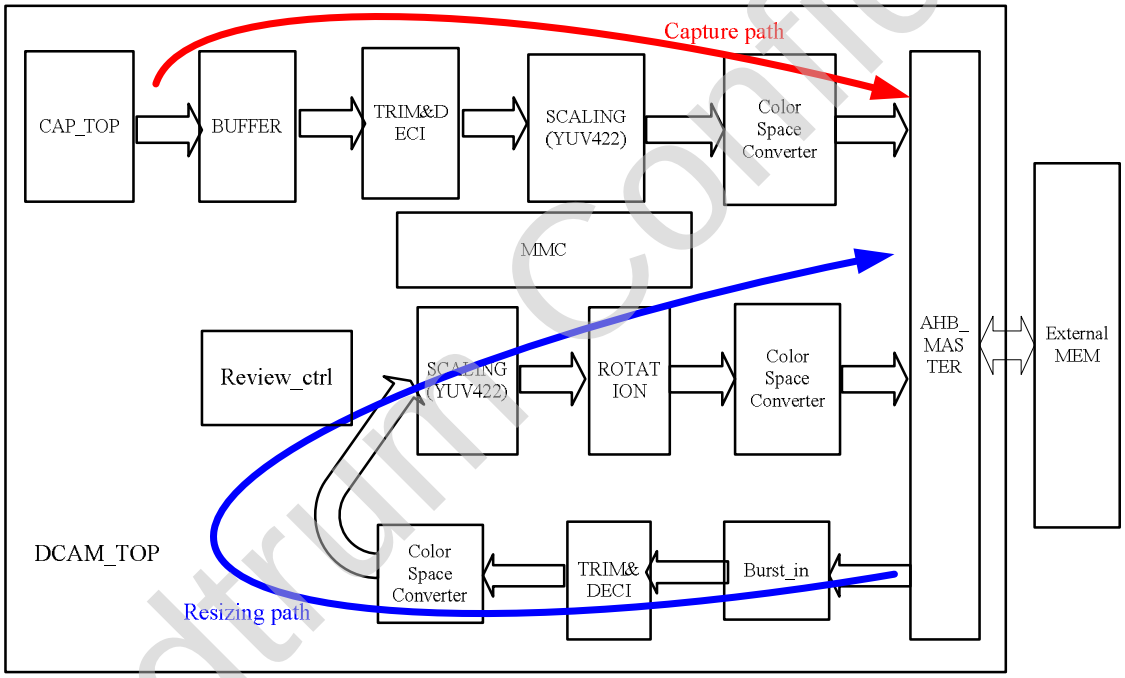


Figure 7.1-12 video phone data path

In Video phone mode, work flow as following figures shows:

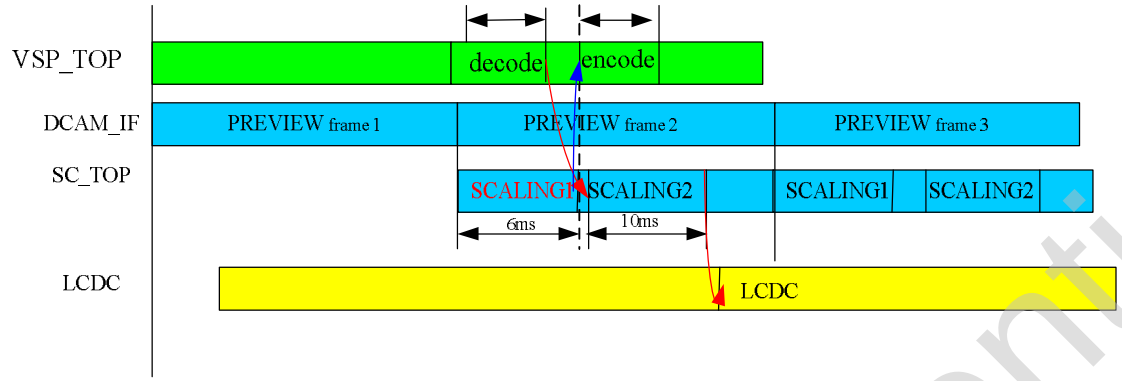


Figure 7.1-13 video phone mode sequence.

7.1.5 Control Registers

7.1.5.1 Memory map

ARM base address: 0x2020_0000

Offset Address	Name	Description
0x0000	DCAM_CFG	DCAM control
0x0004	CAMERA_PATH_CFG	CAMERA PATH control
0x0008	CAM_SRC_SIZE	Camera Source size
0x000C	CAM_DES_SIZE	Camera Destination size
0x0010	CAM1_TRIM_START	CAM1 Trimming start
0x0014	CAM1_TRIM_SIZE	CAM1 Trimming size
0x0018	REVIEW_PATH_CFG	Review control register
0x001C	REV_SRC_SIZE	Review Source size;
0x0020	REV_DES_SIZE	Review Destination size
0x0024	REV_TRIM_START	Review Trimming start
0x0028	REV_TRIM_SIZE	Review Trimming size
0x002C	SLICE_VER_CNT	Slice Vertical line count
0x0030	DCAM_INT_STS	DCAM interrupt status
0x0034	DCAM_INT_MASK	DCAM interrupt mask
0x0038	DCAM_INT_CLR	DCAM interrupt clear

Offset Address	Name	Description
0x003C	DCAM_INT_RAW	DCAM interrupt raw
0x0040	FRM_ADDR_0	Frame address 0
0x0044	FRM_ADDR_1	Frame address 1
0x0048	FRM_ADDR_2	Frame address 2
0x004C	FRM_ADDR_3	Frame address 3
0x0050	FRM_ADDR_4	Frame address 4
0x0054	FRM_ADDR_5	Frame address 5
0x0058	FRM_ADDR_6	Frame address 6
0x005c		
0x0060	BURST_GAP	GAP between two burst
0x0064	ENDIAN_SEL	Endian adjustment
0x0068	AHBM_STS	AHB master status
0x006C	FRM_ADDR_7	Frame address 7
0x0070	FRM_ADDR_8	Frame address 8
0x0074 ~ 0x00FC		reserved
0x0100	CAP_CTRL	Camera interface control
0x0104	CAP_FRM_CTRL	CAP Frame CTRL
0x0108	CAP_START	CAP Start position
0x010C	CAP_END	CAP End position
0x0110	CAP_IMG_DECI	CAP image decimation parameter
0x0114	ATV_MODE_FIX	
0x0118	CAP_OBSERVE	CAP Observing register
0x011C	CAP_JPEG_CTRL	
0x0120	CAP_FRM_SIZE	Current capture size from JPEG or spi sensor
0x0124	CAP_SPI_WIDTH	SPI sensor control
0x0128		reserved

Offset Address	Name	Description
~ 0x01FC		
0x0200 ~ 0x027C	LUMA_HCOEF_1	Luma horizontal coefficient table 1
0x0280 ~ 0x02BC	CHROMA_HCOEF_1	Chroma horizontal coefficient table 1
0x02F0 ~ 0x03FC	VCOEFF_1	Vertical coefficient table 1
0x0400 ~ 0x047C	LUMA_HCOEF_2	Luma horizontal coefficient table 2
0x0480 ~ 0x04BC	CHROMA_HCOEF_2	Chroma horizontal coefficient table 2
0x04F0 ~ 0x05FC	VCOEFF_2	Vertical coefficient table 2
0x2000 ~ 0x23FF	Dcam_mem0	Cap buffer of DCAM
0x2400 ~ 0x25FF	Dcam_mem1	Data buffer of camera path
0x2600 ~ 0x27FF	Dcam_mem2	Data buffer of review path

7.1.5.2 Register Descriptions

7.1.5.2.1 DCAM_CFG Registers

Description：DCAM configuration register

0x0000	DCAM configuration register(Reset 0x0000_0000)													DCAM_CFG		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved									CLK_STATUS2	CLK_STATUS	CLK_SWITCH2	CLK_SWITCH	REV_PATH_EB	CAM_PATH2_EB	CAM_PATH1_EB
Type	RO									RO	RO	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:7]	RO	25'h0	Reserved
CLK_STATUS2	[6]	RO	1'h0	Current status of review path
CLK_STATUS	[5]	RO	1'h0	Current status of camera path 1
CLK_SWITCH2	[4]	R/W	1'h0	Review path or cam path2 clock switch : 1:HCLK; 0:clk_dcam;
CLK_SWITCH	[3]	R/W	1'h0	Camera path 1 clock domain switch; 1:HCLK;0:clk_dcam;
REV_PATH_EB	[2]	R/W	1'h0	Review path enable; 1: enable; 0:disable;
CAM_PATH2_EB	[1]	R/W	1'h0	Camera path 1 enable; 1: enable; 0:disable;
CAM_PATH1_EB	[0]	R/W	1'h0	Camera path 1 enable; 1: enable; 0:disable;

7.1.5.2.2 CAM_PATH_CFG Registers

Description：Camera path configuration register

0x0004	Camera path configuration register(Reset 0x0000_0000)												CAM_PATH_CFG			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CAM1_UV420_AVG_EN	AUTO_COPY_CAP	FRC_COPY_CAP	CAM1_DITHER_EN	CAM1_ODATA_FORMAT		CAM2_DECI_EB	CAM1_TRIM_EB	CAM_SC_VER_TAP[3:0]				CAP_SC_BYPASS	CAM1_DECI_EB	CAP_MODE	CAP_EB
Type	R/W	WO	WO	R/W	R/W		R/W	R/W	R/W				R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	20'h0	Reserved
CAM1_UV420_AVG_EN	[15]	R/W	1'b0	Enable UV average when vertical down sample to YUV420 . only can be set in YUV420 mode
AUTO_COPY_CAP	[14]	WO	1'h0	
FRC_COPY_CAP	[13]	WO	1'h0	
CAM1_DITHER_EN	[12]	R/W	1'b0	1: enable path1 dithering
CAM1_ODATA_FORMAT	[11:10]	R/W	2'b0	Output data format of cam path 1: 00:YUV422 01:YUV420; 10:YUV2RGB 11:reserved

CAM2_DECI_EB	[9]	R/W	1'h0	1:enable path2 1/2 subsample
CAM1_TRIM_EB	[8]	R/W	1'h0	1:enable path1 trimming
CAM_SC_VER_TAP	[7:4]	R/W	4'h0	Vertical tap of scaling
CAM_SC_BYPASS	[3]	R/W	1'h0	1:bypass camera path scaling
CAM1_DECI_EB	[2]	R/W	1'h0	1:enable path1 1/2 subsample
CAP_MODE	[1]	R/W	1'h0	1:capture multi frame; 0: only capture single frame
CAP_EB	[0]	R/W	1'h0	CAP module enable; 1: enable; 0:disable;

7.1.5.2.3 CAM_SRC_SIZE Registers

Description：Camera source image size register.

0x0008					Camera source size (Reset:0x0000_0000)											CAM_SRC_SIZE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				CAM_SRC_SIZE_Y											
Type	RO				W/R											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				CAM_SRC_SIZE_X											
Type	RO				W/R											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
CAM_SRC_SIZE_Y	[27:16]	R/W	12'h0	Height of camera source
	[15:12]	RO	4'h0	Reserved

CAM_SRC_SIZE_X	[11:0]	R/W	12'h0	Width of camera source

7.1.5.2.4 CAM_DES_SIZE Registers

Description：Camera destination image size register.

0x000C			Camera destination size (Reset:0x0000_0000)										CAM_DES_SIZE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				CAM_DES_SIZE_Y											
Type	RO				W/R											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				CAM_DESSRC_SIZE_X											
Type	RO				W/R											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
CAM_DES_SIZE_Y	[27:16]	R/W	11'h0	Height of camera destination
	[15:12]	RO	4'h0	Reserved
CAM_DES_SIZE_X	[11:0]	R/W	11'h0	Width of camera destination

7.1.5.2.5 CAM_TRIM_START Registers

Description：Camera trimming start position register

0x0010			Camera trim start (Reset:0x0FFF_0FFF)													CAM_TRIM_START
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				CAM_TRIM_START_Y											
Type	RO				W/R											
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				CAM_TRIM_START_X											
Type	RO				W/R											
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:28]	RO	4’h0	Reserved
CAM_TRIM_START_Y	[27:16]	R/W	12’hFFF	Vertical start position of camera path 1 trimming
	[15:12]	RO	4’h0	Reserved
CAM_TRIM_START_X	[11:0]	R/W	12’hFFF	Horizontal start position of camera path 1 trimming

7.1.5.2.6 CAM_TRIM_SIZE Registers

Description：Camera trimming size register

0x0014	Camera trim start (Reset:0x0000_0000)															CAM_TRIM_SIZE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				CAM_TRIM_SIZE_Y											
Type	RO				W/R											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				CAM_TRIM_SIZE_X											
Type	RO				W/R											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
CAM_TRIM_SIZE_Y	[27:16]	R/W	12'h0	Height of camera path 1 trimming
	[15:12]	RO	4'h0	Reserved
CAM_TRIM_SIZE_X	[11:0]	R/W	12'h0	Width of camera path 1 trimming

7.1.5.2.7 REV_PATH_CFG Registers

Description：Review path configuration register

0x0018			Review path configuration (Reset 0x0000_0000)											REV_PATH_CFG		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved					ROT_MODE		ROT_EB	Reserved					REV_UV420_AVG_EN	SC_VER_TAP	
Type	RO					R/W		R/W	RO					R/W	R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SC_VER_TAP		RGB_INPUT_FORMAT	YUV_INPUT_FORMATE		SUB_SAMPLE_MODE		DITHERING_EN	OUTPUT_MODE		INPUT_MODE	SCALING_MODE	SCALING_BYPASS	SUB_SAMPLE_EB	REV_TRIM_EB	REVIEW_START
Type	R/W		R/W	R/W	R/W	R/W		R/W	R/W		R/W	R/W	R/W	R/W	R/W	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:27]	RO	14'h0	Reserved
ROT_MODE	[26:25]	R/W	2'b0	Rotation direction: 00: 90 01: 270 10: 180 11: horizon mirror
ROT_EB	[24]	R/W	1'b0	1:enable rotation
	[23:19]	RO		Reserved
REV_UV420_AVG_EN	[18]	R/W	1'b0	Enable UV average when vertical down sample to YUV420 . Can be set, when output YUV420 or rotation 90/270
SC_VER_TAP	[17:14]	R/W	4'h0	Vertical tap of review

				scaling
RGB_INPUT_FORMAT	[13]	RO	1'h0	1: RGB565; 0:RGB888
YUV_INPUT_FORMAT	[12:11]	R/W	2'h0	00:YUV422 01:YUV420 (Y, UV 2 frame) 10:YUV400 11:YUV420 (Y, U, V 3 frame)
SUB_SAMPLE_MODE	[10:9]	R/W	2'h0	00:1/2;01:1/4;10:1/8;11:1/16
DITHERING_EN	[8]	R/W	1'h0	1:ebable dithering
OUTPUT_MODE	[7:6]	R/W	2'h0	00:YUV422 01:YUV420 10:RGB565 11:reserved
INPUT_MODE	[5]	R/W	1'h0	1:RGB 0:YUV;
SCALING_MODE	[4]	R/W	1'h0	1:slice mode; 0:normal mode;
SCALING_BYPASS	[3]	R/W	1'h0	1: bypass scaling;
SUB_SAMPLE_EB	[2]	R/W	1'h0	1: enable sub sample
REV_TRIM_EB	[1]	R/W	1'h0	Trimming enable of review path or camera path 2;
REVIEW_START	[0]	WO	1'h0	1: start review;

7.1.5.2.8 REV_SRC_SIZE Registers

Description：Review source image size register of review path. In capture path2 mode, it indicate

the input size of path2 scaling.

0x001C			Review source size (Reset:0x0000_0000)										REV_SRC_SIZE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				REV_SRC_SIZE_Y											
Type	RO				W/R											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				REV_SRC_SIZE_X											
Type	RO				W/R											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
REV_SRC_SIZE_Y	[27:16]	R/W	12'h0	Source height of review path; Or scaling input height of camera path 2
	[15:12]	RO	4'h0	Reserved
REV_SRC_SIZE_X	[11:0]	R/W	12'h0	Source width of review path; or scaling input width of camera path 2

7.1.5.2.9 REV_DES_SIZE Registers

Description：Review destination image size register. In capture path2 mode, it indicate the output

size of path2 scaling.

0x0020			Review destination size (Reset:0x0000_0000)												REV_DES_SIZE	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				REV_DES_SIZE_Y											
Type	RO				W/R											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				REV_DES_SIZE_X											
Type	RO				W/R											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
REV_DES_SIZE_Y	[27:16]	R/W	12'h0	Source height of review path or camera path 2
	[15:12]	RO	4'h0	Reserved
REV_DES_SIZE_X	[11:0]	R/W	12'h0	Source width of review path or camera path 2

7.1.5.2.10 REV_TRIM_START Registers

Description：Review trimming start position register

0x0024			Review trim start (Reset:0x0FFF_0FFF)													REV_TRIM_START
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				REV_TRIM_START_Y											
Type	RO				W/R											
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				REV_TRIM_START_X											
Type	RO				W/R											
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
REV_TRIM_START_Y	[27:16]	R/W	12'hFFF	Vertical trimming start position of review path or camera path 2
	[15:12]	RO	4'h0	Reserved
REV_TRIM_START_X	[11:0]	R/W	12'hFFF	Horizontal trimming start position of review path or camera path 2

7.1.5.2.11 REV_TRIM_SIZE Registers

Description：Review trimming size register

0x0028			Review trim start (Reset:0x0000_0000)										REV_TRIM_SIZE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				REV_TRIM_SIZE_Y											
Type	RO				W/R											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				REV_TRIM_SIZE_X											
Type	RO				W/R											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
REV_TRIM_SIZE_Y	[27:16]	R/W	12'h0	Trimming height of review path or camera path 2
	[15:12]	RO	4'h0	Reserved
REV_TRIM_SIZE_X	[11:0]	R/W	12'h0	Trimming width of review path or camera path 1

7.1.5.2.12 SLICE_VER_CNT Registers

Description：Slice vertical count register.

0x002C			Slice vertical count (Reset:0x0000_0000)										SLICE_VER_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				SLICE_O_VCNT											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			LAST_BLK_EN	SLICE_I_VCNT											
Type	RO			R/W	R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
SLICE_O_VCNT	[27:16]	RO	12'h0	Current vertical line number of output when current slice mode scaling is done
	[15:13]	RO	3'h0	Reserved
LAST_BLK_EN	[12]	R/W	1'h0	1: indicate current slice is last one
SLICE_I_VCNT	[11:0]	R/W	12'h0	Line number of current slice

7.1.5.2.13 DCAM_INT_STS Registers

Description：DCAM interrupt status register.

0x0030	DCAM interrupt status (Reset 0x0000_0000)														DCAM_INT_STS	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						REV_TX_DONE	JPG_BUF_OVF	CAM_FRM_ERR	CAM_LINE_ERR	CAP_BUF_OVF	CAM_TX_DONE	CAP_EOF	CAP_SOF	SENSOR_EOF	SENSOR_SOF
Type	RO						RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:10]	RO	22h0	Reserved
REV_TX_DONE	[9]	RO	1'h0	Transfer done of review path or camera path 2
JPG_BUF_OVF	[8]	RO	1'h0	JPEG data size exceeded the allocated buffer on SDRAM.
CAM_FRM_ERR	[7]	RO	1'h0	Error is found in current frame
CAM_LINE_ERR	[6]	RO	1'h0	Line error is found in current frame.
CAP_BUF_OVF	[5]	RO	1'h0	Camera Buffer overflow
CAP_TX_DONE	[4]	RO	1'h0	Data transfer done of camera path1
CAP_EOF	[3]	RO	1'h0	Camera Interface's end of frame indication to the next module
CAP_SOF	[2]	RO	1'h0	Camera Interface's start of frame indication to the next module

SENSOR_EOF	[1]	RO	1'h0	Sensor's end of frame indication to Camera Interface module
SENSOR_SOF	[0]	RO	1'h0	Sensor's start of frame indication to Camera Interface module

7.1.5.2.14 DCAM_INT_MASK Registers

Description：DCAM interrupt mask register.

0x0034			DCAM interrupt mask (Reset 0x0000_0000)										DCAM_INT_MASK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						DCAM_INT_MASK									
Type	RO						R/W									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:10]	RO	22h0	Reserved
DCAM_INT_MASK	[9:0]	R/W	10'h0	Bit[i] = 1: DCAM interrupt is enabled for source i Bit[i] = 0: DCAM interrupt is disabled for source i

7.1.5.2.15 DCAM_INT_CLR Registers

Description：DCAM interrupt clear register.

0x0038			DCAM interrupt clear (Reset 0x0000_0000)													DCAM_INT_CLR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						DCAM_INT_CLR									
Type	RO						R/W									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:10]	RO	22h0	Reserved
DCAM_INT_CLR	[9:0]	R/W	10'h0	Write 1 into Bit[i] to clear bit[i] of ISP_INT_RAW register.

7.1.5.2.16 DCAM_INT_RAW Registers

Description：DCAM interrupt raw register.

0x003C			DCAM interrupt raw (Reset 0x0000_0000)													DCAM_INT_RAW
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						DCAM_INT_RAW									
Type	RO						R/W									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset	Description

			Value	
	[31:10]	RO	22h0	Reserved
DCAM_INT_RAW	[9:0]	R/W	10'h0	DCAM interrupt source raw bits

7.1.5.2.17 FRM_ADDR_0 Registers

Description：Frame address 0 register.

0x0040			Frame address 0 (Reset 0x0000_0000)										FRM_ADDR_0			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	FRM_ADDR_0															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FRM_ADDR_0															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
FRM_ADDR_0	[31:0]	R/W	32'h0	BYTE

7.1.5.2.18 FRM_ADDR_1 Registers

Description：Frame address 1 register.

0x0044			Frame address 1 (Reset 0x0000_0000)													FRM_ADDR_1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	FRM_ADDR_1															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FRM_ADDR_1															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
FRM_ADDR_1	[31:0]	R/W	32'h0	BYTE

7.1.5.2.19 FRM_ADDR_2 Registers

Description：Frame address 2 register.

0x0048			Frame address 2 (Reset 0x0000_0000)													FRM_ADDR_2
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	FRM_ADDR_2															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FRM_ADDR_2															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
FRM_ADDR_2	[31:0]	R/W	32'h0	

7.1.5.2.20 FRM_ADDR_3 Registers

Description：Frame address 3 register.

0x004C			Frame address 3 (Reset 0x0000_0000)													FRM_ADDR_3
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	FRM_ADDR_3															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FRM_ADDR_3															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
FRM_ADDR_3	[31:0]	R/W	32’h0	

7.1.5.2.21 FRM_ADDR_4 Registers

Description：Frame address 4 register.

0x0050			Frame address 4 (Reset 0x0000_0000)													FRM_ADDR_4
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	FRM_ADDR_4															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FRM_ADDR_4															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
FRM_ADDR_4	[31:0]	R/W	32’h0	

7.1.5.2.22 FRM_ADDR_5 Registers

Description：Frame address 5 register.

0x0054	Frame address 5 (Reset 0x0000_0000)															FRM_ADDR_5
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	FRM_ADDR_5															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FRM_ADDR_5															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
FRM_ADDR_5	[31:0]	R/W	32'h0	

7.1.5.2.23 FRM_ADDR_6 Registers

Description：Frame address 6 register.

0x0058	Frame address 6 (Reset 0x0000_0000)															FRM_ADDR_6
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	FRM_ADDR_6															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FRM_ADDR_6															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
FRM_ADDR_6	[31:0]	R/W	32'h0	

7.1.5.2.24 BURST_GAP Registers

Description：Burst gap register.

0x0060	Burst gap (Reset 0x0000_0000)												BURST_GAP			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										AHB_HOLD	BURST_GAP				
Type	RO										R/W	R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:6]	RO	26'h0	Reserved
AHBM_HOLD	[5]	R/W	1'b0	1: HOLD DCAM master
BURST_GAP	[4:0]	R/W	5'h0	The interval cycles inserted between two block transfer.

7.1.5.2.25 ENDIAN_SEL Registers

Description：Endian select register.

0x0064			Endian sel (Reset 0x0000_0000)												ENDAIN_SEL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				DCAM_OUT_ENDIAN_UV		DCAM_OUT_ENDIAN_Y		REV_OUT_ENDIAN_UV		REV_OUT_ENDIAN_Y		REV_IN_ENDIAN_UV		REV_IN_ENDIAN_y	
Type	RO				R/W		R/W		R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:12]	RO	20'h0	Reserved
DCAM_OUT_ENDIAN_UV	[11:10]	R/W	2'h0	UV data endian adjust for camera path 1;
DCAM_OUT_ENDIAN_Y	[9:8]	R/W	2'h0	Y or JPEG or RGB565 data endian adjust for camera path 1;
REV_OUT_ENDIAN_UV	[7:6]	R/W	2'h0	UV data endian adjust for rev output path; when write data out: 00: original:{B0,B1,B2,B3} 01:{B3,B2,B1,B0} 10:{B2,B3,B0,B1} 11: {B1,B0,B3,B2}
REV_OUT_ENDIAN_Y	[5:4]	R/W	2'h0	Y or RGB data endian adjust for rev output path; when write data out: 00: original:{B0,B1,B2,B3} 01:{B3,B2,B1,B0} 10:{B2,B3,B0,B1}

				11: {B1,B0,B3,B2}
REV_IN_ENDIAN_UV	[3:2]	R/W	2'h0	UV or U or V data Endian adjust for rev input path ; when read data: 00: original:{B0,B1,B2,B3} 01:{B3,B2,B1,B0} 10:{B2,B3,B0,B1} 11: {B1,B0,B3,B2}
REV_IN_ENDIAN_Y	[1:0]	R/W	2'h0	Y or RGB data Endian adjust for rev input path ; when read data: 00: original:{B0,B1,B2,B3} 01:{B3,B2,B1,B0} 10:{B2,B3,B0,B1} 11: {B1,B0,B3,B2}

7.1.5.2.26 AHBM_STS Registers

Description：AHB master status registers.

0x0068	AHB master status (Reset 0x0000_0000)															AHBM_STS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															AHB M_B USY
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:1]	RO	31'h0	Reserved

AHBM_BUSY	[0]	RO	1'h0	1: busy; 0:idle

7.1.5.2.27 FRM_ADDR_7 Registers

Description：Frame address 7 register.

0x006C			Frame address 7 (Reset 0x0000_0000)										FRM_ADDR_7			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	FRM_ADDR_7															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FRM_ADDR_7															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
FRM_ADDR_7	[31:0]	R/W	32'h0	

7.1.5.2.28 FRM_ADDR_8 Registers

Description：Frame address 8 register.

0x0070			Frame address 8 (Reset 0x0000_0000)										FRM_ADDR_8			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	FRM_ADDR_8															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FRM_ADDR_8															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
FRM_ADDR_8	[31:0]	R/W	32'h0	

Frame address mapping:

In different work mode, we need

Addre Reg Name	Capture path 1	Capture path 2	Review &YUV input	Large size slice mode	Review &YUV (3FRAME)
Frm_addr0		Captured Y0 frame buffer	Source Y0 frame buffer (Source RGB)	Source Y	Source Y frame buffer
Frm_addr1		Captured U0V0 frame buffer	Source U0V0 frame buffer	Source U	Source U frame buffer
Frm_addr2				Temp data Y	Source V frame buffer
Frm_addr3				Temp data U	
Frm_addr4			Destination Y or Destination RGB	Dest Y	Destination Y addr
Frm_addr5			Destination U0V0	Dest U	Destination U0V0
Frm_addr6				Linebufer	
Frm_addr7	Captured Y0 or JPEG frame				
Frm_addr8	Captured U0V0 frame buffer				

7.1.5.2.29 CAP_CTRL

Description：CAP control register.

0x0100	CAP control register(reset 0x0000_0000)															CAP_CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			CAP_CCIR_PD		CAP_CCIR_RST	CAP_IF_MODE		YUV_TYPE		Reserved	Cap_IF_ENDIAN	VSYNC_POL	HSYNC_POL	SENSOR_MODE		CCIR_656
Type	RO		R/W		R/W	R/W		R/W		RO	R/W	R/W	R/W	R/W		R/W
Reset	0	0	X	X	X	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:14]	RO	18'h0	Reserved
CAP_CCIR_PD	[13:12]	R/W	2'hX	Power down signal to sensor
CAP_CCIR_RST	[11]	R/W	1'hX	Reset to sensor.
CAP_IF_MODE	[10:9]	R/W	2'h0	00:8bit interface mode 01:4bit interface mode 10:2bit interface mode 11:1bit interface mode For CCIR656 or CCIR 601
YUV_TYPE	[8:7]	R/W	2'h0	YUV sequence of sensor: 0:Y0U0Y1V1 1:Y0V0Y1U0 2:U0Y0V0Y1 3:V0Y0U0Y1
	[6]	RO	1'h0	Reserved
CAP_IF_ENDIAN	[5]	R/W	1'h0	0:big-endian: 1: little endian Only active for 4 bit 2 bit or 1 bit YUV sensor

VSYNC_POL	[4]	R/W	1'h0	Polarity of Vsync 0: active low 1: active high
HSYNC_POL	[3]	R/W	1'h0	Polarity of Hsync 0: active low 1: active high
SENSOR_MODE	[2:1]	R/W	2'h0	00:YUV, force copy is suggested. 01:SPI :auto copy 10:JPEG autocopy 11:RAW RGB force copy is suggested.
CCIR_656_sel	[0]	R/W	1'h0	1: ccir656 mode In CCIR656, only force copy can be use. 0:ccir601

7.1.5.2.30 CAP_FRM_CTRL

Description：CAP frame count register.

0x0104	CAP frame control (Reset 0x0000_000F)												CAP_FRM_CTRL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved									CAP_FRM_CLR	CAP_FRM_CNT					
Type	RO									WO	RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										CAP_FRM_DECI		PRE_SKIP_CNT			
Type	RO										R/W		R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:23]	RO	9'h0	Reserved
CAP_FRM_CLR	[22]	WO	1'h0	If this bit is 1, the frame-counter will be "0" at the next frame start, and then this bit is self-cleared by HW.
CAP_FRM_CNT	[21:16]	RO	6'h0	The counter is for the frames, which CAP issues to the next modules.
	[15:6]	RO	10'h0	Reserved
CAP_FRM_DECI	[5:4]	R/W	2'h0	00:no deci 01:1/2 10:1/3 11:1/4
PRE_SKIP_CNT	[3:0]	R/W	4'hF	The frame counter to skip sensor's frames.

Note:

- When switch to capture mode, skip a few frame is suggested after configuring sensor, so set the PRE_SKIP_CNT to neglect the frame we not interested .

7.1.5.2.31 CAP_START

Description：CAP start register.

0x0108			CAP start (Reset 0x0080_0080)										CAP_START			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				CAP_START_Y											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			CAP_START_X												
Type	RO			R/W												
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
CAP_START_Y	[27:16]	R/W	12'h80	Start Y position
	[15:13]	RO	3'h0	Reserved
CAP_START_X	[12:0]	R/W	13'h80	Start X position

7.1.5.2.32 CAP_END

Description：CAP end register.

0x010C			CAP end (Reset 0x00FF_00FF)												CAP_END	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				CAP_END_Y											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			CAP_END_X												
Type	RO			R/W												
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
CAP_END_Y	[27:16]	R/W	12'hFF	Start Y position
	[15:13]	RO	3'h0	Reserved
CAP_END_X	[12:0]	R/W	13'hFF	Start X position

7.1.5.2.33 CAP_IMG_DECI

Description：CAP image decimation register.

0x0110			CAP image decimation (Reset 0x0000_0011)												CAP_IMG_DECI	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												CAP_DECI_Y		CAP_DECI_X	
Type	RO												RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:4]	RO	28'h0	Reserved
CAP_DECI_Y	[3:2]	R/W	2'h0	Y direction decimation factor 0: Disable 1: 1/ 2 2: 1/4 3: 1/8
CAP_DECI_X	[1:0]	R/W	2'h0	X direction decimation factor 0: Disable 1: 1/ 2 2: 1/4 3: 1/8

7.1.5.2.34 ATV_MODE_FIX

7.1.5.2.35 CAP_OBSERVE

Description：CAP observe register.

0x00118	CAP observe register (Reset 0x0000_0000)												CAP_OBSERVE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															CAP_OBSERVE_EB
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:1]	RO	31'h0	Reserved

CAP_OBSERVE	[0]	R/W	1'h0	Enable signal for observing

7.1.5.2.36 CAP_JPG_CTL

Description：CAP JPEG control register.

0x011c			CAP JPEG buffer control (Reset 0x0000_0020)										CAP_JPG_CTL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						JPG_MEM_SIZE									
Type	RO						R/W									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:10]	RO	22'h0	Reserved
JPG_buf_SIZE	[9:0]	R/W	10'h0	The JPEG buffer size in external memory, which was prepared by software. (unit:32K BYTE) 0: No limit 1: 23K BYTE . . . N: N * 32K . .

7.1.5.2.37 CAP_FRM_SIZE

Description：CAP frame size register.

0x0120	CAP frame size (Reset 0x0000_0000)														CAP_FRM_SIZE	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved								CAP_FRM_SIZE							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CAP_FRM_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:24]	RO	8'h0	Reserved
CAP_FRM_SIZE	[23:0]	RO	24'h0	Size of current frame, the unit is BYTE,only active in spi or jpeg mode

7.1.5.2.38 CAP_SPI_CFG

Description：SPI original width register.

0x0124	CAP SPI config register(reset 0x0000_0000)														CAP_SPI_CFG	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			SPI_ORIG_WIDTH												
Type	RO			R/W												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset	Description

			Value	
	[31:13]	RO	19'h0	Reserved
SPI_ORIG_WIDTH	[12:0]	R/W	13'h0	Width of SPI sensor original image. n-1 BYTE .

7.1.5.2.39 SCALING COEF TABLE

The scaling coefficient fixed-point precision is 9-bit, range from [-2.0, 1.9921875]

COEF table 1:

Luma horizontal coeffient table: 8X72

0x0200	Luma horizontal coefficient 1 [0] (Reset 0x0000_0000)														LUMA_HCOEF_1[0]	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved														LUMA_HCOEF_1[0][17:0]	
Type	RO														R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LUMA_HCOEF_1[0][17:0]															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x0204	Luma horizontal coefficient 1 [0] (Reset 0x0000_0000)														LUMA_HCOEF_1[0]	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved														LUMA_HCOEF_1[0][35:18]	
Type	RO														R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LUMA_HCOEF_1[0][35:18]															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x0208	Luma horizontal coefficient 1 [0] (Reset 0x0000_0000)														LUMA_HCOEF_1[0]	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved														LUMA_HCOEF_1[0][53:36]	
Type	RO														R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LUMA_HCOEF_1[0][53:36]															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x020C			Luma horizontal coefficient 1 [0] (Reset 0x0000_0000)												LUMA_HCOEF_1[0]	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved														LUMA_HCOEF_1[0][71:54]	
Type	RO														R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LUMA_HCOEF_1[0][71:54]															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

. . .

Chroma horizontal coefficient table: 8X36

0x0280			Chroma horizontal coefficient 1 [0] (Reset 0x0000_0000)												CHROMA_HCOEF_1[0]	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved														CHROMA_HCOEF_1[0][17:0]	
Type	RO														R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHROMA_HCOEF_1[0][17:0]															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x0284			Chroma horizontal coefficient 1 [0] (Reset 0x0000_0000)												CHROMA_HCOEF_1[0]	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved														CHROMA_HCOEF_1[0][35:18]	
Type	RO														R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHROMA_HCOEF_1[0][35:18]															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

. . .

Vertical coefficient table: 68X8

0x02F0			Vertical coefficient (Reset 0x0000_0000)												VCOEF_1[0]	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved														CHROMA_VCOEF_1[0]	
Type	RO														R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHROMA_VCOEF_1[0]							LUMA_VCOEF_1[0]								
Type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

. . .

Address	Register Name	Signal Name	Bits	R/W	Default	Description

Address	Register Name	Signal Name	Bits	R/W	Default	Description
0x0200	LUMA_HCOEFF[0]_1	Video_luma_horizontal_coeff[0]	[17:0]	R/W	18'h0	Video luma horizontal coefficient[17:0]
0x0204	LUMA_HCOEFF[0]_2		[17:0]	R/W	18'h0	Video luma horizontal coefficient[35:18]
0x0208	LUMA_HCOEFF[0]_3		[17:0]	R/W	18'h0	Video luma horizontal coefficient[53:36]
0x020c	LUMA_HCOEFF[0]_4		[17:0]	R/W	18'h0	Video luma horizontal coefficient[71:54]
0x0210	LUMA_HCOEFF[1]_1	Video_luma_horizontal_coeff[1]	[17:0]	R/W	18'h0	Video luma horizontal coefficient[17:0]
0x0214	LUMA_HCOEFF[1]_2		[17:0]	R/W	18'h0	Video luma horizontal coefficient[35:18]
0x0218	LUMA_HCOEFF[1]_3		[17:0]	R/W	18'h0	Video luma horizontal coefficient[53:36]
0x021C	LUMA_HCOEFF[1]_4		[17:0]	R/W	18'h0	Video luma horizontal coefficient[71:54]
0x0220	LUMA_HCOEFF[2]_1	Video_luma_horizontal_coeff[2]	[17:0]	R/W	18'h0	Video luma horizontal coefficient[17:0]
0x0224	LUMA_HCOEFF[2]_2		[17:0]	R/W	18'h0	Video luma horizontal coefficient[35:18]
0x0228	LUMA_HCOEFF[2]_3		[17:0]	R/W	18'h0	Video luma horizontal coefficient[53:36]
0x022C	LUMA_HCOEFF[2]_4		[17:0]	R/W	18'h0	Video luma horizontal coefficient[71:54]
	. . .	. . .				
0x0270	VID_LUMA_HCOEFF[7]_1	Video_luma_horizontal_	[17:0]	R/W	18'h0	Video luma horizontal coefficient[17:0]

Address	Register Name	Signal Name	Bits	R/W	Default	Description
0x0274	VID_LUMA_HCOEFF[7]_2	coeff[7]	[17:0]	R/W	18'h0	Video luma horizontal coefficient[35:18]
0x0278	VID_LUMA_HCOEFF[7]_3		[17:0]	R/W	18'h0	Video luma horizontal coefficient[53:36]
0x027C	VID_LUMA_HCOEFF[7]_4		[17:0]	R/W	18'h0	Video luma horizontal coefficient[71:54]
0x0280	VID_CHROMA_HCOEFF_LOW[0]	Video_chroma_horizontal_coeff_low[0]	[17:0]	R/W	18'h0	Video Chroma horizontal coefficient[17:0]
0x0284	VID_CHROMA_HCOEFF_HIGH[0]	Video_chroma_horizontal_coeff_high[0]	[17:0]	R/W	18'h0	Video chroma horizontal coefficient[17:0]
0x0288	VID_CHROMA_HCOEFF_LOW[1]	Video_chroma_horizontal_coeff_low[7]	[17:0]	R/W	18'h0	Video Chroma horizontal coefficient[17:0]
0x028C	VID_CHROMA_HCOEFF_HIGH[1]	Video_chroma_horizontal_coeff_high[7]	[17:0]	R/W	18'h0	Video chroma horizontal coefficient[17:0]
	. . .	. . .				
0x02B8	VID_CHROMA_HCOEFF_LOW[7]	Video_chroma_horizontal_coeff_low	[17:0]	R/W	18'h0	Video Chroma horizontal coefficient[17:0]
0x02BC	VID_CHROMA_HCOEFF_HIGH[7]	Video_chroma_horizontal_coeff_high	[17:0]	R/W	18'h0	Video chroma horizontal coefficient[17:0]

Address	Register Name	Signal Name	Bits	R/W	Default	Description
0x02F0	VID_VCOEFF[0]	Video_luma_vertical_coeff[0]	[8:0]	R/W	9'h0	Video luma Vertical coefficient[8:0]
		Video_chroma_vertical_coeff[0]	[17:9]	R/W	9'h0	Video Chroma vertical coefficient[8:0]
		Reserved	[31:18]		--	Reserved
0x02F4	VID_VCOEFF[1]	Video_luma_vertical_coeff[1]	[8:0]	R/W	9'h0	Video luma Vertical coefficient[8:0]
		Video_chroma_vertical_coeff[1]	[17:9]	R/W	9'h0	Video Chroma vertical coefficient[8:0]
		Reserved	[31:18]		--	Reserved
	. . .	...	. . .			...
0x03FC	VID_VCOEFF[35]	Video_luma_vertical_coeff[67]	[8:0]	R/W	9'h0	Video luma Vertical coefficient[8:0]
		Video_chroma_vertical_coeff[67]	[17:9]	R/W	9'h0	Video Chroma vertical coefficient
		Reserved	[31:18]		--	Reserved

COEF table 2:

Address	Register Name	Signal Name	Bits	R/W	Default	Description

Address	Register Name	Signal Name	Bits	R/W	Default	Description
0x0400	LUMA_HCOEFF[0]_1	Video_luma_horizontal_coeff[0]	[17:0]	R/W	18'h0	Video luma horizontal coefficient[17:0]
0x0404	LUMA_HCOEFF[0]_2		[17:0]	R/W	18'h0	Video luma horizontal coefficient[35:18]
0x0408	LUMA_HCOEFF[0]_3		[17:0]	R/W	18'h0	Video luma horizontal coefficient[53:36]
0x040c	LUMA_HCOEFF[0]_4		[17:0]	R/W	18'h0	Video luma horizontal coefficient[71:54]
0x0410	LUMA_HCOEFF[1]_1	Video_luma_horizontal_coeff[1]	[17:0]	R/W	18'h0	Video luma horizontal coefficient[17:0]
0x0414	LUMA_HCOEFF[1]_2		[17:0]	R/W	18'h0	Video luma horizontal coefficient[35:18]
0x0418	LUMA_HCOEFF[1]_3		[17:0]	R/W	18'h0	Video luma horizontal coefficient[53:36]
0x041C	LUMA_HCOEFF[1]_4		[17:0]	R/W	18'h0	Video luma horizontal coefficient[71:54]
0x0420	LUMA_HCOEFF[2]_1	Video_luma_horizontal_coeff[2]	[17:0]	R/W	18'h0	Video luma horizontal coefficient[17:0]
0x0424	LUMA_HCOEFF[2]_2		[17:0]	R/W	18'h0	Video luma horizontal coefficient[35:18]
0x0428	LUMA_HCOEFF[2]_3		[17:0]	R/W	18'h0	Video luma horizontal coefficient[53:36]
0x042C	LUMA_HCOEFF[2]_4		[17:0]	R/W	18'h0	Video luma horizontal coefficient[71:54]
	. . .	. . .				
0x0470	VID_LUMA_HCOEFF[7]_1	Video_luma_horizontal_	[17:0]	R/W	18'h0	Video luma horizontal coefficient[17:0]

Address	Register Name	Signal Name	Bits	R/W	Default	Description
0x0474	VID_LUMA_HCOEFF[7]_2	coeff[7]	[17:0]	R/W	18'h0	Video luma horizontal coefficient[35:18]
0x0478	VID_LUMA_HCOEFF[7]_3		[17:0]	R/W	18'h0	Video luma horizontal coefficient[53:36]
0x047C	VID_LUMA_HCOEFF[7]_4		[17:0]	R/W	18'h0	Video luma horizontal coefficient[71:54]
0x0480	VID_CHROMA_HCOEFF_LOW[0]	Video_chroma_horizontal_coeff_low[0]	[17:0]	R/W	18'h0	Video Chroma horizontal coefficient[17:0]
0x0484	VID_CHROMA_HCOEFF_HIGH[0]	Video_chroma_horizontal_coeff_high[0]	[17:0]	R/W	18'h0	Video chroma horizontal coefficient[17:0]
0x0488	VID_CHROMA_HCOEFF_LOW[1]	Video_chroma_horizontal_coeff_low[7]	[17:0]	R/W	18'h0	Video Chroma horizontal coefficient[17:0]
0x048C	VID_CHROMA_HCOEFF_HIGH[1]	Video_chroma_horizontal_coeff_high[7]	[17:0]	R/W	18'h0	Video chroma horizontal coefficient[17:0]
	. . .	. . .				
0x04B8	VID_CHROMA_HCOEFF_LOW[7]	Video_chroma_horizontal_coeff_low	[17:0]	R/W	18'h0	Video Chroma horizontal coefficient[17:0]
0x04BC	VID_CHROMA_HCOEFF_HIGH[7]	Video_chroma_horizontal_coeff_high	[17:0]	R/W	18'h0	Video chroma horizontal coefficient[17:0]

Address	Register Name	Signal Name	Bits	R/W	Default	Description
0x04F0	VID_VCOEFF[0]	Video_luma_vertical_coeff[0]	[8:0]	R/W	9'h0	Video luma Vertical coefficient[8:0]
		Video_chroma_vertical_coeff[0]	[17:9]	R/W	9'h0	Video Chroma vertical coefficient[8:0]
		Reserved	[31:18]		--	Reserved
0x04F4	VID_VCOEFF[1]	Video_luma_vertical_coeff[1]	[8:0]	R/W	9'h0	Video luma Vertical coefficient[8:0]
		Video_chroma_vertical_coeff[1]	[17:9]	R/W	9'h0	Video Chroma vertical coefficient[8:0]
		Reserved	[31:18]		--	Reserved
	. . .	...	. . .			...
0x04FC	VID_VCOEFF[35]	Video_luma_vertical_coeff[67]	[8:0]	R/W	9'h0	Video luma Vertical coefficient[8:0]
		Video_chroma_vertical_coeff[67]	[17:9]	R/W	9'h0	Video Chroma vertical coefficient
		Reserved	[31:18]		--	Reserved

7.1.6 Application Notes

7.1.6.1 Camera capture path

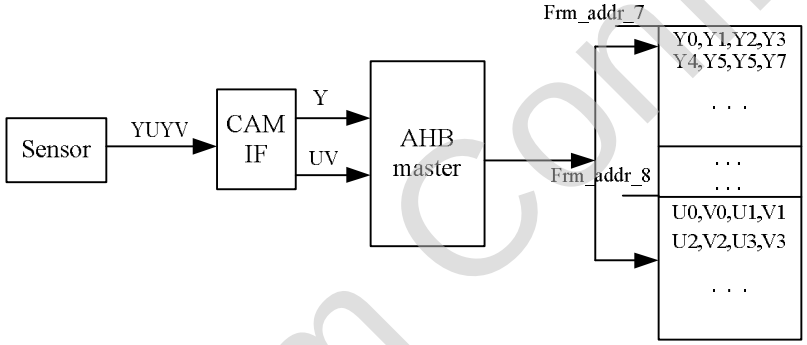
Software operation suggestion:

YUV data format capture:

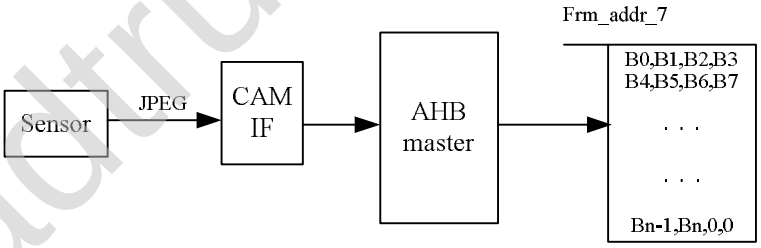
a. Configure sensor via I2C,
b. Enable DCAM module, and clear interrupt and set relative interrupt mask.
c. Configure DCAM global control register and AHB master register. Include DCAM_CFG, CAMER_CFG, CAM_SRC_SIZE, AHB frame address register and CAM_DST_SIZE if enable scaling.
d. If enable scale&trimming in YUV capture mode. Scaling coefficient table 1 is needed.
e. Filled in relative cap registers. Set shadow register, auto copy is suggested.
f. Set cap_eb to start capture.
g. Wait CAP_TX_DONE interrupt.
h. If camera path2 is enabled, wait REV_TX_DONE.

Data store method:

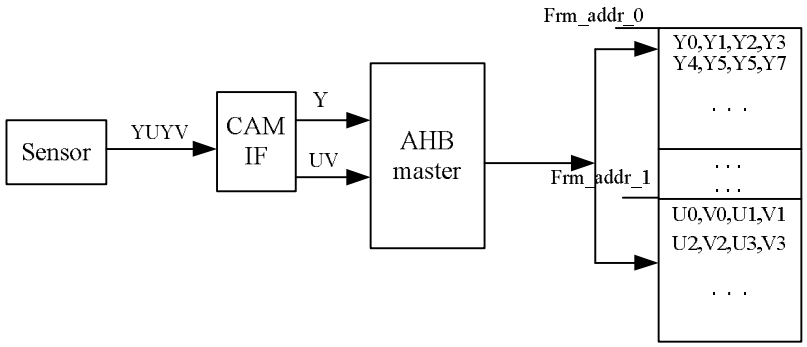
Camera path1:



JPEG capture data memory store:



Camera path 2:



7.1.6.2 Image resizing path

Software operation suggestion:

Normal mode:

a. Enable DCAM module and clear interrupt and set relative interrupt mask.
b. Configure DCAM global control register. Include DCAM_CFG, REVIEW_CFG, REV_SRC_SIZE, REV_DST_SIZE and AHB frame address registers,
c. If enable scaling module. Fill in scaling coefficient table 2 .
d. Set review start.
e. Wait REV_TX_DONE interrupt.

Slice mode operation:

a. Enable DCAM CLK and clear interrupt and set relative interrupt mask.
b. Configure DCAM global control register. Include DCAM_CFG, REV_SRC_SIZE, REV_DST_SIZE and AHB frame address registers,
c. Set frm_addr2, frm_addr3,frm_addr6, If the destination width exceed 960.
d. Fill in scaling coefficient table 2.
e. Enable slice mode and Fill in SLICE_VCNT_INPUT. The standard vertical number 64,128 and 256 is suggested.

Caution: The trim_start_y must be 0, if current slice is not first slice block.

f. Wait REV_TX_DONE interrupt, And check AHBM_STS ,make sure it is IDLE;

So, one slice mode review process completed. Read SLICE_O_VCNT can get the total line numbers hardware have send out.

g. After VSP operation, begin the new slice mode review.
h. Repeat step d, e, f. until the left vertical line is less than standard vertical number.
i. Fill in the left line number to SLIC_VCNT_INPUT.
j. Start review.
k. Wait REV_TX_DONE;

Data store method:

Normal review mode:

Input data: YUV422/YUV420/YUV400;

output data:YUV422

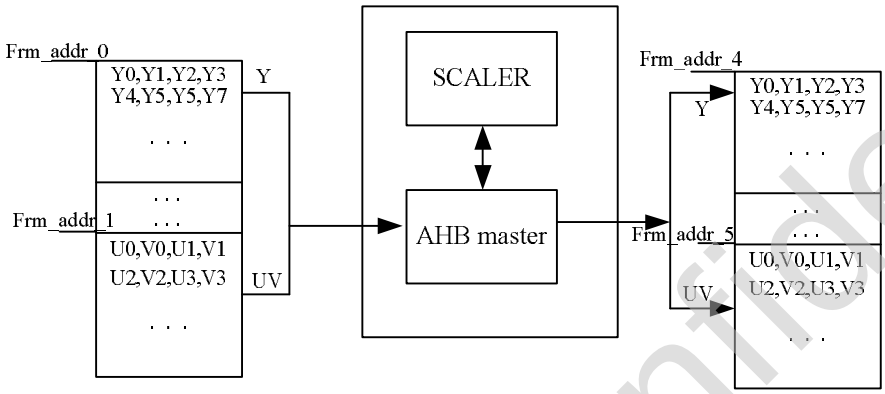


Figure 7.1-13 data store scheme of review mode(a)

Input data: YUV420(3 Frame) ;

output data YUV. (with Scaling enable)

In YUV 3 frame, the input horizontal size must be multiple of 8.

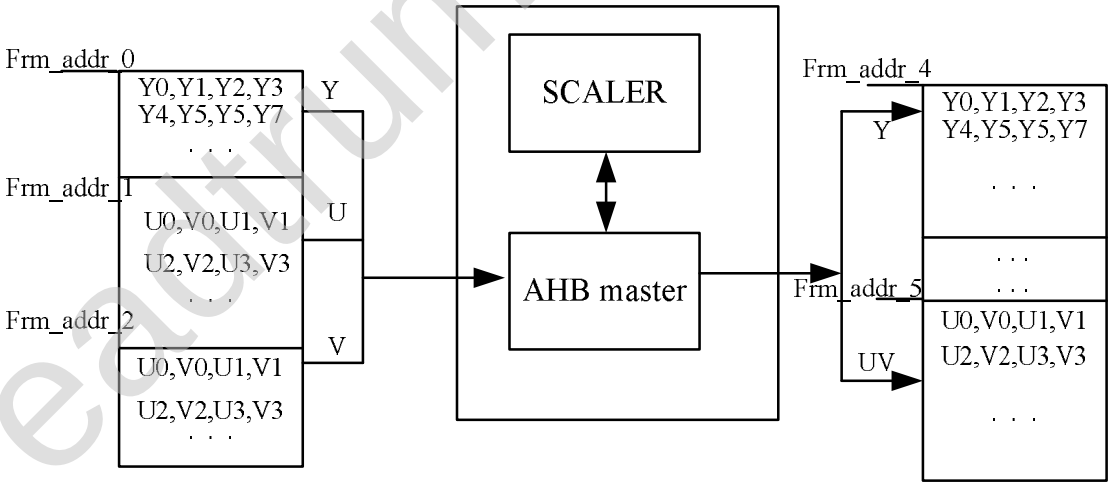


Figure 7.1-14 data store scheme of review mode(b)

Input data: YUV420(3 Frame) ;

output data YUV. (with Scaling bypass).

In YUV 3 frame, the input horizontal size must be multiple of 8.

Caution : in current mode, the yuv2rgb shouldn't be enabled.

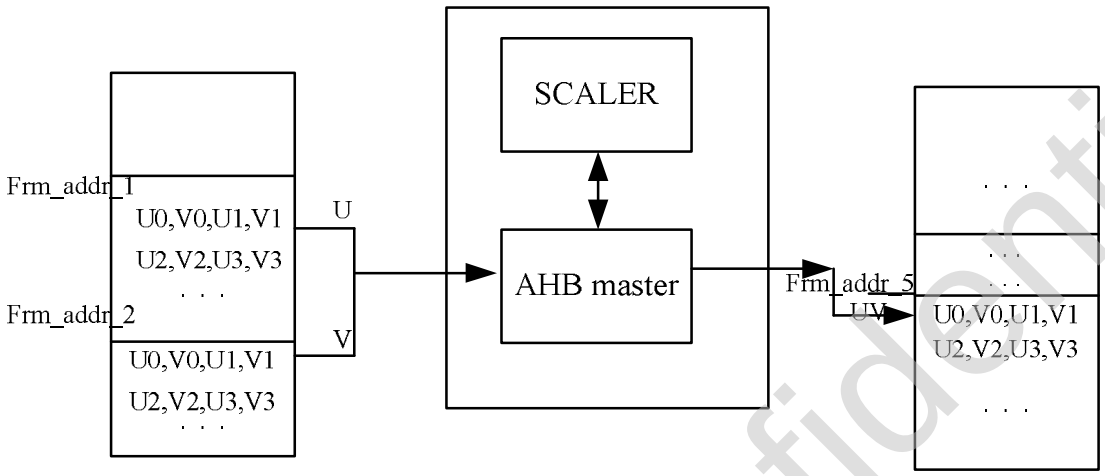


Figure 7.1-15 data store scheme of review mode(c)

Input data YUV;

output data: RGB565.

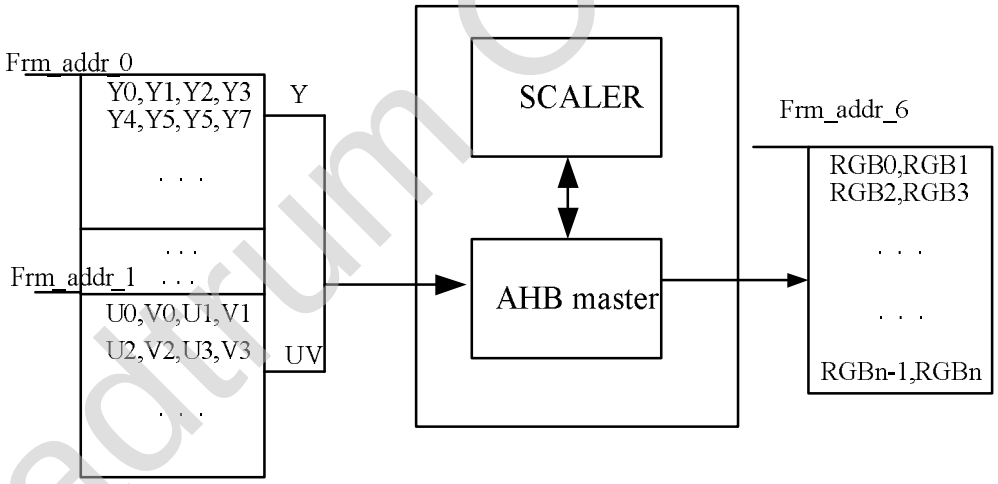


Figure 7.1-16 data store scheme of review mode(d)

Input data: RGB565;

Output data:RGB565

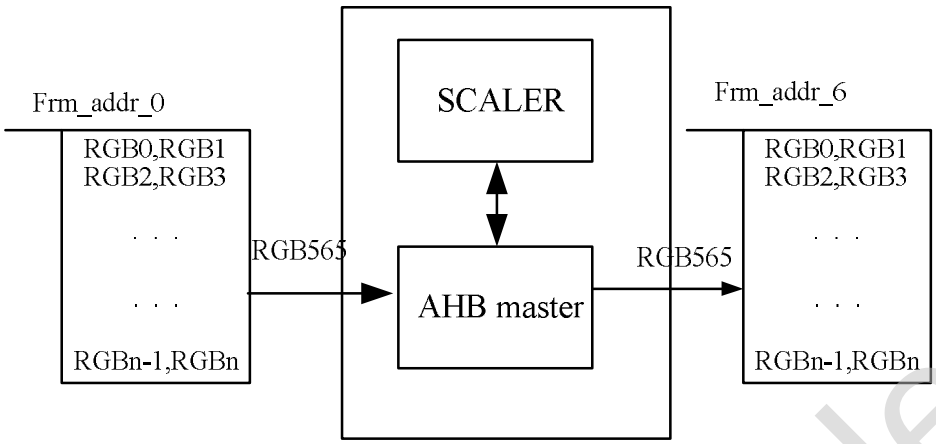


Figure 7.1-17 data store scheme of review mode(e)

Input data:RGB888;

output data RGB565:

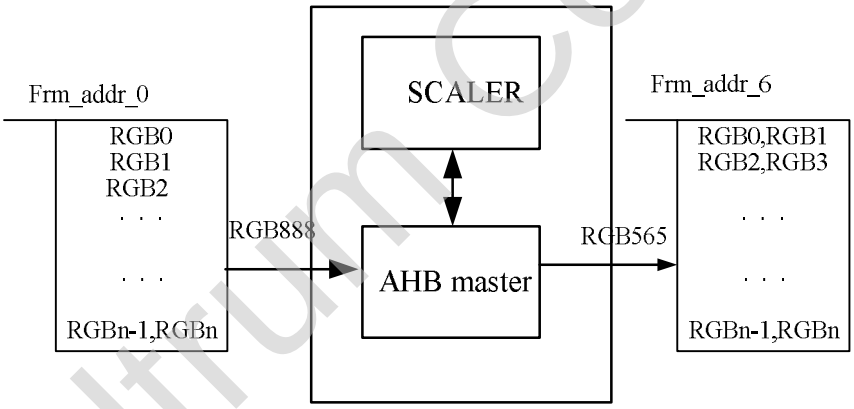


Figure 7.1-18 data store scheme of review mode(f)

RGB888 data format :

[31:24]	[23:16]	[15:8]	[7:0]
reserved	R	G	B

Large size(dst_hor_size>640) slice mode review:

Input data: YUV

Output data:YUV422

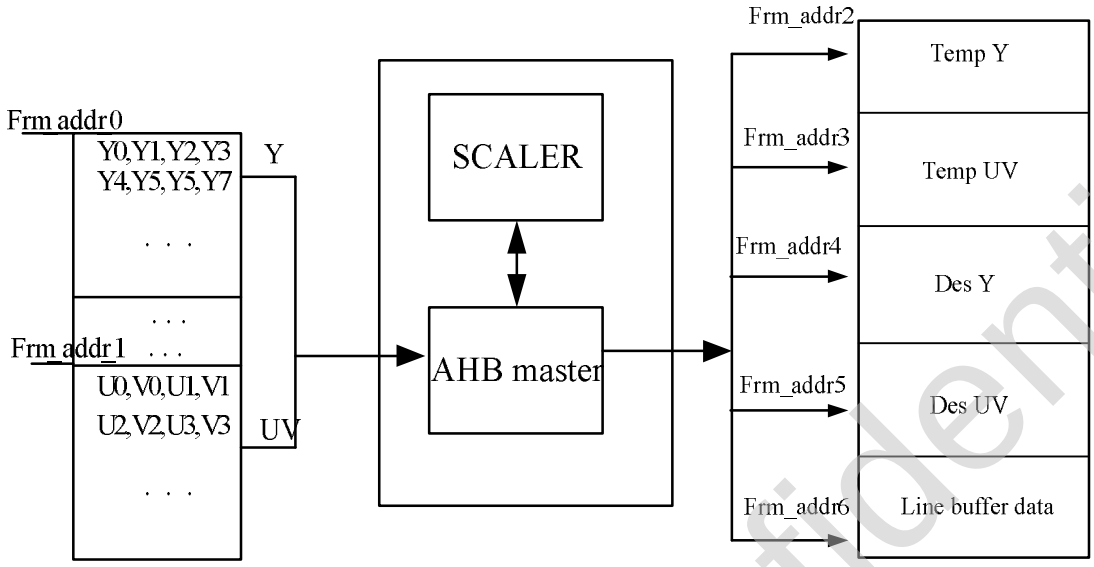


Figure 7.1-19 data store scheme of slice mode(g)

Temp Y size: (dst_size_X * slice_i_vcnt) BYTE;

Temp UV size: (dst_size_X * slice_i_vcnt) BYTE;

Line buffer data size:

Dst_size_y * 8 BYTE;

Input data: RGB565/RGB888

Output data: RGB565

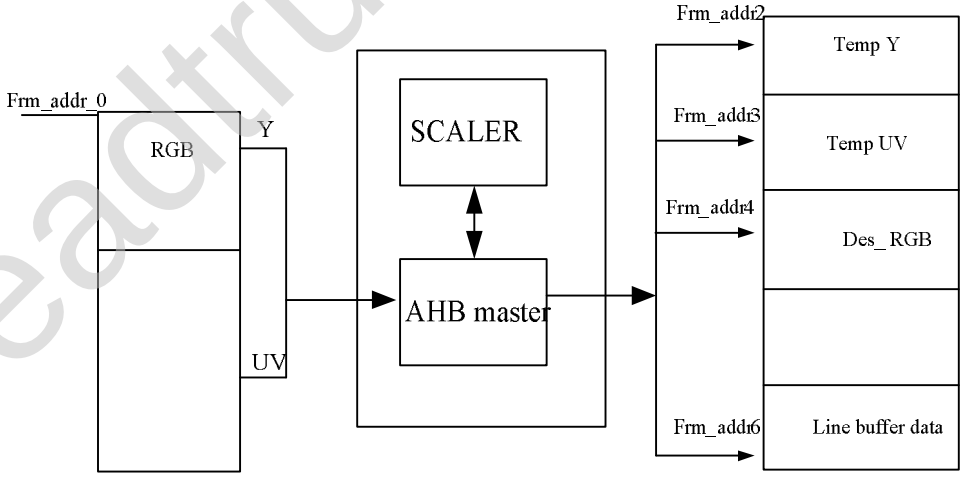


Figure 7.1-20 data store scheme of slice mode(f)

7.2 Rotation

7.2.1 Overview

The module works as accelerator to help software processing image rotation operation.

Change list:

- Add trimming function
- Modify the macro block size to 16X16 to improve the performance.

7.2.2 Features

- Support byte, half word and word format image rotation.
- Support UV 422 data mode rotation.
- Support 90, 270 ,180 and mirror rotation.
- Support image size up to 4092X4092.
- Support image trimming before rotation.

7.2.3 Signal Description

7.2.4 Function Description

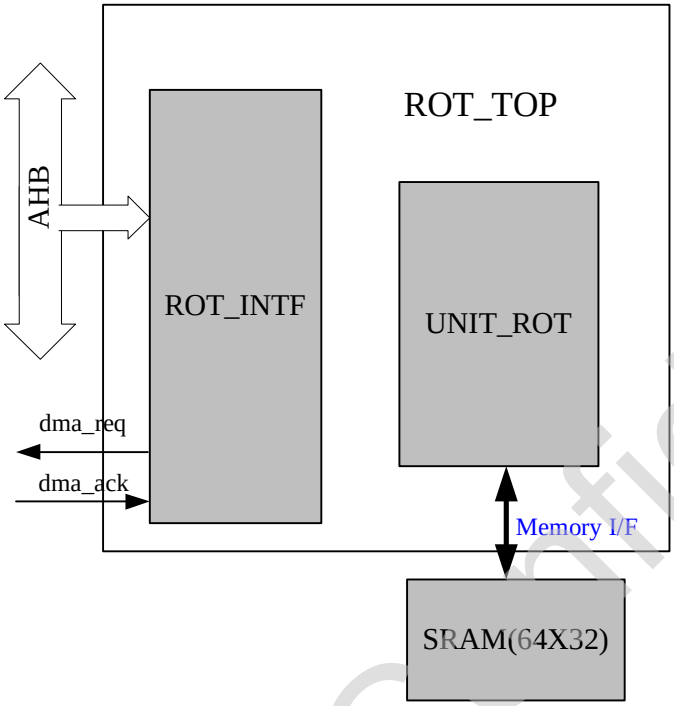


Figure 7.2-1 Diagram of rot_top

The above figure depicts the diagram of ROTATION module. This module contains of 2 units except one 64X32 memory, rot_intf and unit_rot .

7.2.4.1 Rot_intf&unit_rot

This two module is in charge of coordinate rotation.

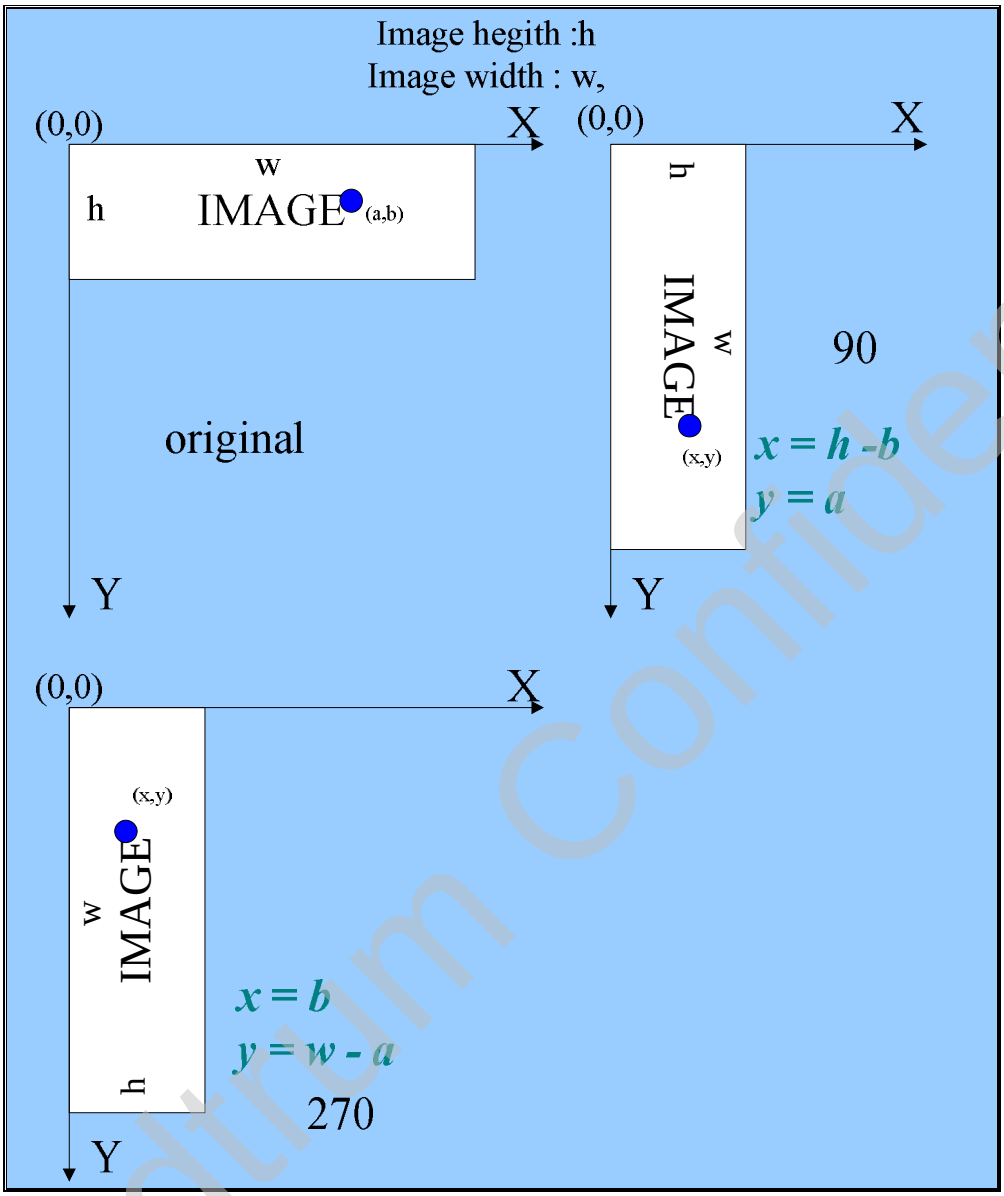


Figure 7.2-2 rotation coordinate

The whole image will be divided into several blocks according to the image size and rotation unit. First, we rotate the block position. Secondly we rotate every pixel in one block.

Rotate 90 degree:

Pixel_addr = h(a + 1) – b (h = (RotationUnit = 0)? 7: 15).

Byte_addr = pixel_addr << PixelFormat (PixelFormat != 3)

Roate 270 degree

Pixel_addr = h(w – a) + b

Byte_addr = pixel_addr << PixelFormat ();

For the pixel with 4bytes, we only need to change its memory position. If one pixel with the following coordinate **(a, b)** enters the rotation module, it will have another coordinate(x, y).

X=8-b; (Suppose that Rotation Unit is 8)

Y=a.

As the result, the memory address will be **8(a+1) –b**; (a[2:0], b[2:0])

After rotation: (a+b*i) * i = -b +a*i;

Coordination shift 8 left: 8-b+a*i;

Index in memory (64X32): 8*a + (8 – b) = 8(a+1) –b.

For the pixel with 2bytes, firstly, we should rotate it, and align the half-word. Suppose pixel position is (a, b), after rotation, the position will be (16-b, a), and the pixel position in memory will be **(8(a+1) –b)/2**.(a[2:0], b[2:0])

After rotation: (a+b*i) * i = -b +a*i;

Coordination shift 8 left: 8-b+a*i;

Index in memory (64X32): 8*a + (8 – b) = 8(a+1) –b.

For the pixel with only one byte, suppose pixel position is (a, b), the finial position will be 16(a+1) –b, and the memory address will be **((16(a+1) –b)/4)**; (a[3:0], b[3:0])

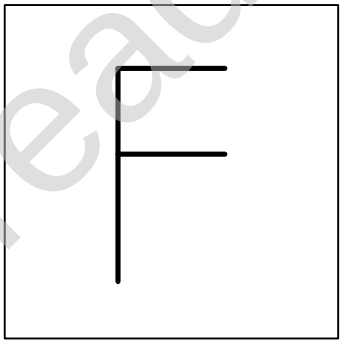
After rotation: (a+b*i) * i = -b +a*i;

Coordination shift 16 left: 16-b+a*i;

Index in memory (64X32): 16*a + (16 – b) = 16(a+1) –b.

7.2.4.2 Rotation mode

Support four rotation modes :



original

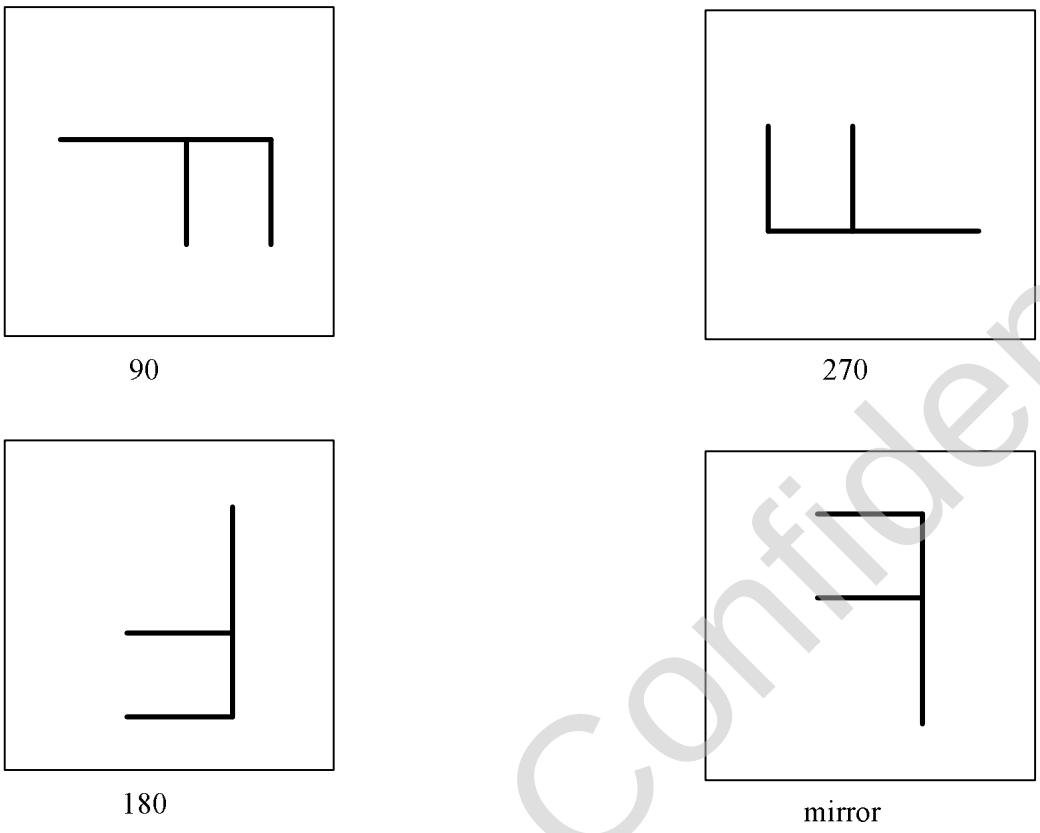


Figure 7.2-3 rotation mode

7.2.5 Control Registers

7.2.5.1 Memory map

ARM base address: 0x2080_0000

Offset Address	Name	Description
0x0400	SrcDataStartAddr	Start address of source
0x0404	DesDataStartAddr	Start address of destination
0x0408	IMGSIZE	Image size
0x040C	ROTCTRL	Rotation control
0x0410	ORIGWIDTH	Original image width
0x0414	ORIGOFFSET	Offset position in original image

Offset Address	Name	Description
0x0420	DMACHnCFG0	DMA channel configuration 0
0x0424	DMACHnCFG1	DMA channel configuration 1
0x0428	DMACHnSrcAddr	DMA channel source address
0x042C	DMACHnDesAddr	DMA channel Destination address
0x0430	DMACHnLLPtr	DMA channel link list pointer
0x0434	DMACHnSDI	DMA channel SDI
0x0438	DMACHnSBP	DMA channel SBD
0x043C	DMACHnDBP	DMA channel DBP

7.2.5.2 Register Descriptions

7.2.5.2.1 SrcDataStartAddr Registers

Description：Source data start address

0x0400			Source data start address(Reset 0x0000_0000)										SrcDataStartAddress			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SrcDataStartAddress															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SrcDataStartAddress															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
SrcDataStartAddr	[31:0]	R/W	32’h0	Start address for raw data in external memory

7.2.5.2.2 DesDataStartAddr Registers

Description：Destination data start address

0x0404			Destination data start address(Reset 0x0000_0000)										DesDataStartAddress			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DesDataStartAddress															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DesDataStartAddress															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
SrcDataStartAddr	[31:0]	R/W	32'h0	destination address in external memory

7.2.5.2.3 IMGSIZE Registers

Description：Source image size register;

0x0408			Source Image size (reset 0x0000_0000)										IMGSIZE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved						PIXELFORMAT									
Type	R/W						R/W		R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	IMGWIDTH				IMGHEIGHT											
Type	R/W				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:26]	RO	6'h0	Reserved

PIXELFORMAT	[25:24]	R/W	2'h0	Pixel format: 2'h0: 1Byte/Pixel 2'h1: 2Byte/Pixle 2'h2: 4Byte/Pixel
IMGWIDTH	[23:12]	R/W	12'h0	Image width of source
IMGHEIGHT	[11:0]	R/W	12'h0	Image height of source

7.2.5.2.4 ROTCTRL Registers

Description：Rotation control registers.

0x040C			Rotation control (Reset 0x0000_0000)											ROTCTRL		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												ROT_EN	ROT_DIR		ROT_MODE
Type	RO												R/W	R/W		R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:4]	RO	28'h0	Reserved
ROT_EN	[3]	R/W	1'h0	Rotation Enable,This bit will be auto cleared after rotation is done.
ROT_DIR	[2:1]	R/W	2'h0	Rotation direction: 00: 90 01: 270 10: 180 11: horizon mirror
ROT_MODE	[0]	R/W	1'h0	Rotation mode:

				1:uv422 mode 0:normal mode

7.2.5.2.5 ORIGWIDTH Registers

Description：Original image width register;

0x0410	Original image width size (reset 0x0000_0000)												ORIGWIDTH			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				ORIGWIDTH											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:12]	RO	6'h0	Reserved
ORIGWIDTH	[11:0]	R/W	12'h0	Width of original image

7.2.5.2.6 ORIGOFFSET Registers

Description：offset position of original iamge register;

0x041C			Offset position of original position (reset 0x0000_0000)												ORIGOFFSET	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved								ORIG_START_Y							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ORIG_START_Y				ORIG_START_X											
Type	R/W				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:26]	RO	6'h0	Reserved
ORIG_START_Y	[23:12]	R/W	12'h0	Start Y position in original iamge
ORIG_START_X	[11:0]	R/W	12'h0	Start X position in original iamge

7.2.5.2.7 DMACHnCFG0 Registers

Description：DMA channel configuration 0 register.

0x0420			DMA channel configuration 0 (Reset 0x0042_0000)												DMAChnCFG0	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LLend	Reserved			SrcDataWidth		DestDataWidth		ReqModeSel		SrcWrapEn	DestWrapEn	Reserved		NoAutoClose	Reserved
Type	RO	RO			RO		RO		RO		RO	RO	RO		RO	RO
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BurstLength															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
LLend	[31]	RO	1'h0	Link list end flag.
	[30:28]	RO	3'h0	Reserved
SrcDataWidth	[27:26]	RO	2'h0	Source data width. 00: byte. 01: half-word. 10: word.
DestDataWidth	[25:24]	RO	2'h0	Destination data width. 00: byte. 01: half-word. 10: word.
ReqModeSel	[23:22]	RO	2'h1	*2'b01: Transaction mode, one request for one transaction.*
SrcWrapEn	[21]	RO	1'h0	*Source Address Wrapping Enable. 1'b0: disable*
DestWrapEn	[20]	RO	1'h0	*Destination Address Wrapping Enable. 1'b0: disable*
	[19:18]	RO	2'h0	Reserved
NoAutoclose	[17]	RO	1'h1	*Channel No Auto-Close* *0: ChnEn is set by ARM and cleared automatically after a request completed.* *1: ChnEn is set and cleared only by ARM.*
	[16]	RO	1'h0	Reserved
Burst_Length	[15:0]	RO	16'h0	Burst Length The unit is BYTE. MUST be ChnSrcDataWidth boundary.

7.2.5.2.8 DMACHnCFG1 Registers

Description：DMA channel configuration 1 register.

0x0424	DMA channel configuration 1 (Reset 0x0000_0000)															DMACHnCFG1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved							TotalTransactionLength								
Type	RO							RO								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TotalTransactionLength															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:25]	RO	7'h0	Reserved
TotalTransactionLength	[24:0]	RO	25'h0	Total Transaction length. Unit is BYTE

7.2.5.2.9 DMACHnSrcAddr Registers

Description：DMA channel source address register.

0x0428	DMA channel source address (Reset 0x0000_0000)															DMACHnSrcAddr
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DMACHnSrcAddr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DMACHnSrcAddr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description

DMACHnSrcAddr	[31:0]	RO	32'h0	DMA channel Source address

7.2.5.2.10 DMACHnDesAddr Registers

Description：DMA channel Destination address register.

0x042C			DMA channel destination address (Reset0x0000_0000)										DMACHnDesAddr			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DMACHnDesAddr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DMACHnDesAddr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
DMACHnDesAddr	[31:0]	RO	32'h0	DMA channel destination address

7.2.5.2.11 DMACHnLLPtr Registers

Description：DMA channel link list pointer register.

0x0430			DMA channel link list pointer (Reset 0x0000_0000)													DMACHnLLPtr
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DMACHnLLPtr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DMACHnLLPtr															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
DMACHnLLPtr	[31:0]	RO	32'h0	*Link list pointer to the next node address.MUST be on 8-word boundary.* *So when writing, bit [4:0] is omitted; When reading, bit [4:0] is 0.* *If LLEnd is set, indicating the current transaction is last one of the list, LLPtr is unused.*

7.2.5.2.12 DMACHnSDI Registers

Description：DMA channel source transfer Interval register.

0x0434			DMA channel source transfer interval (Reset value)													DMACHnSDI
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SrcTransferSel	Reserved	SrcTransferAddrStep													
Type	RO	RO	RO													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DestTransferSel	Reserved	DestTransferAddrStep													
Type	RO	RO	RO													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
srcTransferSel	[31]	RO	1'h0	0:increased;1:decreased;
	[30]	RO	1'h0	Reserved.
SrcTransferAddrStep	[29:16]	RO	14'h0	Source Transfer address step.The unit is BYTE
DestTransferSel	[15]	RO	1'h0	0:increased;1:decreased;
	[14]	RO	1'h0	Reserved.
DestTransferAddrStep	[13:0]	RO	14'h0	Destination Transfer address step.The unit is BYTE

7.2.5.2.13 DMACHnSBP Registers

Description：DMA channel source block post-modification register.

0x0438	DMA channel source block post-modification (Reset 0x1000_0000)	DMACHnSBP

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved	SrcBurstMode			reserved		DMACHnSBP									
Type	RO	RO			RO		RO									
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMACHnSBP															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31]	RO	1'h0	Reserved
SrcBurstMode	[30:28]	RO	3'h1	000 – Single Transfer; NSEQ for each transfer; 001 – INCR for unspecified length 011 – INCR4; 101 – INCR8; 111 – INCR16;
	[27:26]	RO	2'h0	Reserved
DMACHnSBP	[25:0]	RO	26'h0	Sets the post-modification value of the source's current address, between the Read transfer of the last element in a source block to the first element of the next block during a cluster transfer. The value is in 2's complement, which means that both positive and negative values are supported. The

				post-modification value is summed with the source current address following a block Read transfer. **Note:** The value must be set to an integer multiple of the data width; setting it to a different value may yield unexpected behavior.

7.2.5.2.14 DMACHnDBP Registers

Description：DMA channel destination block post-modification register.

0x043C			DMA channel destination block post-modification (Reset value)										DMACHnDBP			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved	DestBurstMode			reserved		DMACHnDBP									
Type	RO	RO			RO		RO									
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DMACHnDBP															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31]	RO	1’h0	Reserved
DestBurstMode	[30:28]	RO	3’h1	000 – Single Transfer; NSEQ for each transfer; 001 – INCR for unspecified length 011 – INCR4; 101 – INCR8; 111 – INCR16;

	[27:26]	RO	2'h0	Reserved
DMACHnDBP	[25:0]	RO	26'h0	Sets the post-modification value of the destination's current address, between the Read transfer of the last element in a source block to the first element of the next block during a cluster transfer. The value is in 2's complement, which means that both positive and negative values are supported. The post-modification value is summed with the source current address following a block Read transfer.

7.2.6 Application Notes

7.3 LCDC

7.3.1 Overview

LCD Controller (LCDC) is used to fetch image data and OSD data, blend these data, and output to LCD panel or write back to memory. There are 6 data sources, one for image source, and five for OSD source, these 6 source data can be blended with alpha simultaneously.

7.3.2 Features

- Support 6 layer alpha blending, 5 for OSD and 1 for image, the image layer is the bottom one, the OSD1 is the more top one, and in turn, the OSD5 is the most top one;

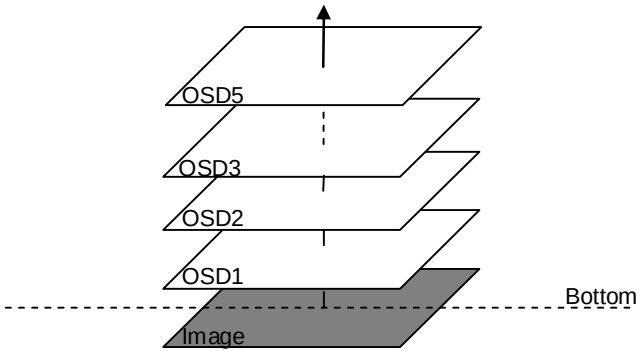


Figure xx Layer Define

- Support YUV422/YUV420/YUV400/RGB888/RGB565/RGB666/RGB555 data format in image layer;
- Support RGB888/RGB565/RGB666/RGB555/GREY data format in OSD1 layer, when in RGB565, it can be with individual alpha data;
- Support RGB888/RGB565/RGB666/RGB555/GREY data format in OSD2/3/4/5 layer, when in RGB565, only support block alpha;

Table xx Data Format

<table>
<tr><th>Format</th><th>Code</th><th>Data Mapping</th></tr>
<tr><td>YUV422</td><td>0000</td><td>
<table>
<tr><td>Y</td><td>[31:24]</td><td>[23:16]</td><td>[15:8]</td><td>[7:0]</td><td>UV</td><td>[31:24]</td><td>[23:16]</td><td>[15:8]</td><td>[7:0]</td></tr>
<tr><td></td><td>Y0</td><td>Y1</td><td>Y2</td><td>Y3</td><td></td><td>U0</td><td>V0</td><td>U2</td><td>V2</td></tr>
<tr><td></td><td>Y4</td><td>Y5</td><td>Y6</td><td>Y7</td><td></td><td>U4</td><td>V4</td><td>U6</td><td>V6</td></tr>
</table>
The U/V data is half of the Y data in horizontal.
Data address should be half-word-aligned, size should be 2x pixels.
</td></tr>
<tr><td>YUV420</td><td>0001</td><td>
<table>
<tr><td>Y</td><td>[31:24]</td><td>[23:16]</td><td>[15:8]</td><td>[7:0]</td><td>UV</td><td>[31:24]</td><td>[23:16]</td><td>[15:8]</td><td>[7:0]</td></tr>
<tr><td></td><td>Y0</td><td>Y1</td><td>Y2</td><td>Y3</td><td></td><td>U0</td><td>V0</td><td>U2</td><td>V2</td></tr>
<tr><td></td><td>Y4</td><td>Y5</td><td>Y6</td><td>Y7</td><td></td><td>U4</td><td>V4</td><td>U6</td><td>V6</td></tr>
</table>
The U/V data is half of the Y data in horizontal and vertical.
Data address should be half-word-aligned, size should be 2x pixels.
</td></tr>
<tr><td>YUV400</td><td>0010</td><td>
<table>
<tr><td>Y</td><td>[31:24]</td><td>[23:16]</td><td>[15:8]</td><td>[7:0]</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td></td><td></td><td>
<table>
<tr><td>Y0</td><td>Y1</td><td>Y2</td><td>Y3</td></tr>
<tr><td>Y4</td><td>Y5</td><td>Y6</td><td>Y7</td></tr>
</table>
No U/V source data in this format, but we replace them with constant 0x80.
Data address should be half-word-aligned, size should be 2x pixels.
</td></tr>
<tr><td>RGB888</td><td>0011</td><td>
<table>
<tr><td>[31:24]</td><td>[23:16]</td><td>[15:8]</td><td>[7:0]</td></tr>
<tr><td>A0</td><td>R0</td><td>G0</td><td>B0</td></tr>
<tr><td>A1</td><td>R1</td><td>G1</td><td>B1</td></tr>
</table>
Ax is pixel alpha.
</td></tr>
<tr><td>RGB666</td><td>0100</td><td>
<table>
<tr><td>[31:24]</td><td>--</td><td>[21:16]</td><td>--</td><td>[13:8]</td><td>--</td><td>[5:0]</td></tr>
<tr><td>A0</td><td>--</td><td>R0</td><td>--</td><td>G0</td><td>--</td><td>B0</td></tr>
<tr><td>A1</td><td>--</td><td>R1</td><td>--</td><td>G1</td><td>--</td><td>B1</td></tr>
</table>
Ax is pixel alpha.
RGB666 to RGB888: R/G/B[5:0] à {R/G/B[5:0], 2{R/G/B[0]}}
</td></tr>
<tr><td>RGB565</td><td>0101</td><td>
<table>
<tr><td>[31:27]</td><td>[26:21]</td><td>[20:16]</td><td>[15:11]</td><td>[10:5]</td><td>[4:0]</td></tr>
<tr><td>R0</td><td>G0</td><td>B0</td><td>R1</td><td>G1</td><td>B1</td></tr>
<tr><td>R2</td><td>G2</td><td>B2</td><td>R3</td><td>G3</td><td>B3</td></tr>
</table>
When in OSD1 layer, it includes the below alpha data.
<table>
<tr><td>[31:24]</td><td>[23:16]</td><td>[15:8]</td><td>[7:0]</td></tr>
<tr><td>A0</td><td>A1</td><td>A2</td><td>A3</td></tr>
<tr><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>
Ax is pixel alpha, Px = {Ax, Rx, Gx, Bx}.
RGB565 to RGB888: R/B[4:0] à {R/B[4:0], 3{R/B[0]}}, G[5:0] à {G[5:0], 2{G[0]}}
</td></tr>
<tr><td>RGB555</td><td>0110</td><td>
<table>
<tr><td>[31]</td><td>[30:26]</td><td>[25:21]</td><td>[20:16]</td><td>[15]</td><td>[14:10]</td><td>[9:5]</td><td>[4:0]</td></tr>
<tr><td>A0</td><td>R0</td><td>G0</td><td>B0</td><td>A1</td><td>R1</td><td>G1</td><td>B1</td></tr>
</table>
Ax is pixel alpha, 0 for 8’h00, 1 for 8’hff.
</td></tr>
</table>

<table>
<tr><td></td><td></td><td>RGB555 to RGB888: R/G/B[4:0] à {R/G/B[4:0], 3{R/G/B[0]}}</td></tr>
<tr><td>GREY</td><td>0111</td><td>
<table>
<tr><td>[31:24]</td><td>[23:16]</td><td>[15:8]</td><td>[7:0]</td></tr>
<tr><td>G0</td><td>G1</td><td>G2</td><td>G3</td></tr>
</table>
Gx is pixel grey, with the constant R, G and B, become a pixel: Px = {Gx, R, G, B}.
</td></tr>
<tr><td>reserved</td><td>1001~
1111</td><td>For future.</td></tr>
<tr><td></td><td></td><td>All data support 3 switch mode
<table>
<tr><td rowspan="3">switch mode</td><td>[31:24]</td><td>[23:16]</td><td>[15:8]</td><td>[7:0]</td></tr>
<tr><td>Byte0</td><td>Byte1</td><td>Byte2</td><td>Byte3</td></tr>
<tr><td colspan="2">Half-word0</td><td colspan="2">Half-word1</td></tr>
<tr><td>0</td><td>Byte0</td><td>Byte1</td><td>Byte2</td><td>Byte3</td></tr>
<tr><td>1</td><td>Byte3</td><td>Byte2</td><td>Byte1</td><td>Byte0</td></tr>
<tr><td>2</td><td colspan="2">Half-word1</td><td colspan="2">Half-word0</td></tr>
<tr><td>reserved</td><td></td><td></td><td></td><td></td></tr>
</table>
</td></tr>
</table>

- Support color key, one layer with same color key value;
- Support dithering, RGB888 to RGB666 or RGB888 to RGB565;
- Support writing back to memory, data can be RGB888/RGB565/RGB666;
- Support 2 panel, and one can be FMARK panel;
- Support MCU I/F, data type can be RGB565/RGB666/RGB888, bus type can be 8bits/9bits/16bits/18bits/24bits;

7.3.3 Signal Description

Table LCDC Signal List

Signal Name	Direction	Width	Description
LCD_CD	O	1	Command or data indication, ‘0’ for command, ‘1’ for data.
LCD_CSN0	O	1	Device select, active low.
LCD_CSN1	O	1	Device select, active low.

LCD_RSTN	O	1	Reset control, active low.
LCD_RDN	O	1	Read control, active low.
LCD_WRN	O	1	Write control, active low.
LCD_D	I/O	18	Input/output data.
LCD_FMARK	I	1	External panel frame sync signal input.

7.3.4 Function Description

The LCDC's application is as below.

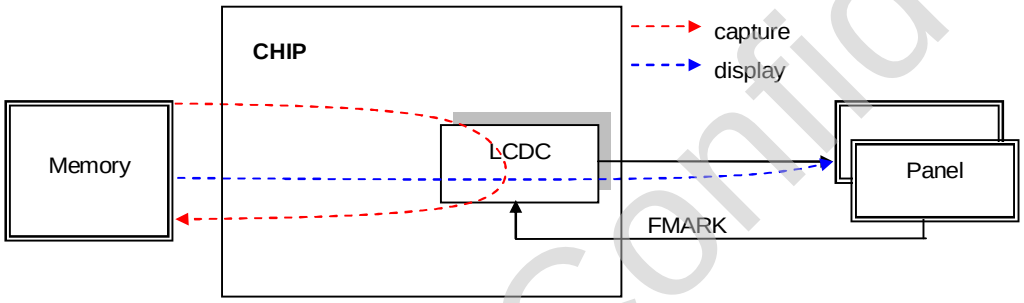


Figure xx LCDC Application

As above diagram, it includes 3 paths, the first one is Memory->LCDC->Memory; the second one is Memory->LCDC->Main Panle; the last one is Memory->LCDC->Sub Panel.

The LCDC's module diagram is shown in Figure xx.

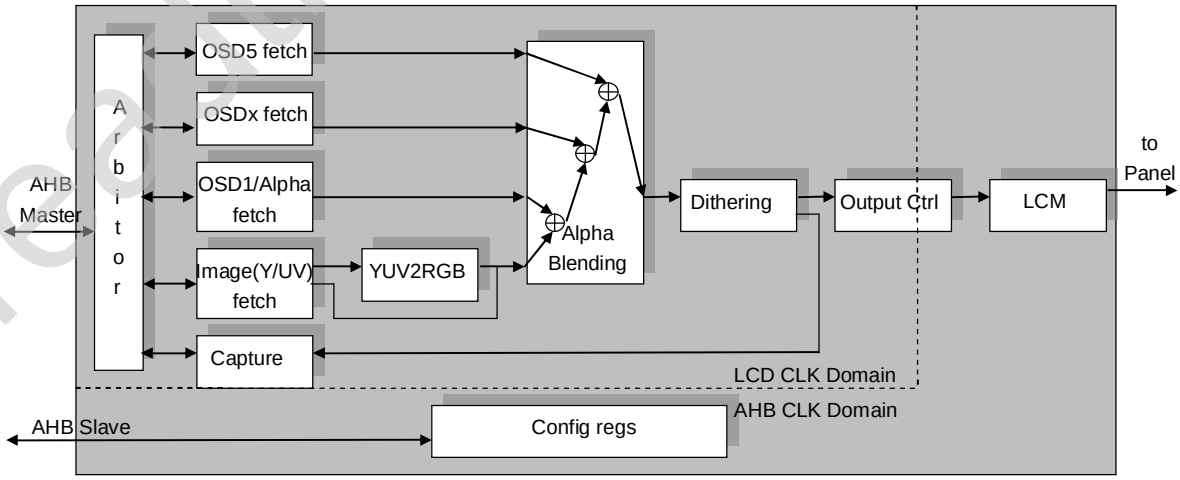


Figure xx LCDC Module Diagram

The LCDC mainly does alpha blending along multi layer data, it supports up to 6 layers simultaneously. As above diagram, the LCDC includes multi clients for AHB master request, so it has an arbiter for AHB master interface, the “OSDx fetch” gets the top layer data and prepares for blending, the “Image fetch” gets bottom layer data and prepares for blending. Because blending only for RGB format data, but image data may be YUV format data, so a YUV2RGB module applied for YUV data. When all data are ready, “alpha blending” fetches all source and formats these data to RGB888, then blends them, if no source in some position, “alpha blending” outputs background color. Blended image may be output to LCM or write back to memory, when write back, the “capture” module will finish this task. For most applications, output may be RGB565 or RGB666, so the ‘dithering’ transform the RGB888 data to RGB565 or RGB666. Before send to LCM, “output ctrl” synchronizes data to cross 2 clock domains (LCM is in AHB clock) and sends to LCM. The LCDC also includes some configure registers.

7.3.4.1 YUV to RGB

The blending only support RGB888 data format, so the YUV image data must be conversed to RGB888 before blend. Before the YUV changed to RGB, YUV can be adjusted for special application, the adjustment as below,

```
Y_tmp = (Y - 128) * contrast / 64 + 128 + brightness;
Y’ = CLIP(Y_tmp, 255, 0);
U_tmp = (U - 128) * saturation / 64 + 128;
U’ = CLIP(U_tmp, 255, 0);
V_tmp = (V - 128) * saturation / 64 + 128;
V’ = CLIP(V_tmp, 255, 0);
```

After this, the Y’U’V’ will be changed to RGB, this conversion uses the constant coefficient matrix calculation, the calculation formula as below.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 359/256 \\ 1 & -88/256 & -183/256 \\ 1 & 454/256 & 0 \end{bmatrix} \begin{bmatrix} Y' \\ U' \\ V' \end{bmatrix} + \begin{bmatrix} -180 \\ 136 \\ -227 \end{bmatrix}$$

As above formula, the input data is YUV444, so the fetched data must be up-sampled to YUV444 before converse.

When the input is YUV422, we need to up-sample UV in horizontal.

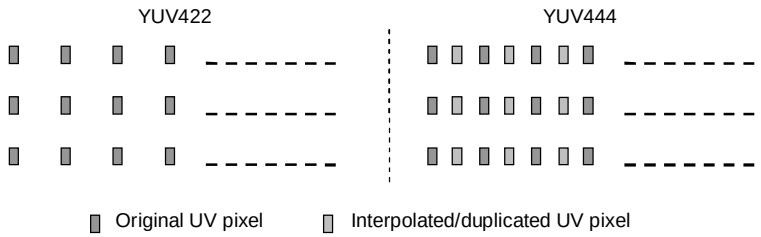


Figure xx YUV422 to YUV444 Conversion

When the input is YUV420, we need to up-sample UV in horizontal, and duplicate UV in vertical.

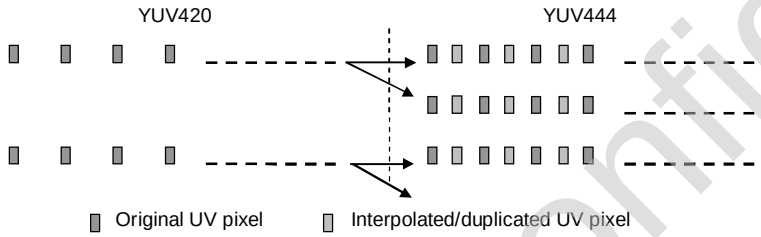


Figure xx YUV420 to YUV444 Conversion

When the input is YUV400, we need to replace the UV with some constant vale, here is 0x80.

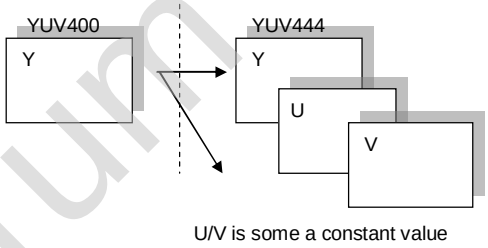


Figure xx YUV400 to YUV444 Conversion

7.3.4.2 Alpha Blending

The main function of this sub-module is blending image and OSD, when no image or OSD, the background will be displayed, the blending is alpha weighed average, a color-key function also implemented in here, when pixel vale is equal to color-key value, the pixel will become zero alpha.

The LCDC supports up to 6 layers blending, so it will do 5 blending,

The first one is blending image and OSD1,

$$blend1 = osd1\_din * osd1\_alpha + img\_din * (1 - osd1\_alpha)$$

$$= (osd1\_din - img\_din) * osd1\_alpha + img\_din$$

The second one is blending blend1 and OSD2,

blend2 = osd2_din * osd2_alpha + blend1 * (1 – osd2_alpha)

= (osd2_din – blend1)*osd2_alpha + blend1

The third one is blending blend2 and OSD3,

blend3 = osd3_din * osd3_alpha + blend2 * (1 – osd3_alpha)

= (osd3_din – blend2)*osd3_alpha + blend2

The fourth one is blending blend3 and OSD4,

blend4 = osd4_din * osd4_alpha + blend3 * (1 – osd4_alpha)

= (osd4_din – blend3)*osd4_alpha + blend3

The fifth one is blending blend4 and OSD5,

blend5 = osd5_din * osd5_alpha + blend4 * (1 – osd5_alpha)

= (osd5_din – blend4)*osd5_alpha + blend4

For less resource, all blending share the same blending logic, the alpha blending as below.

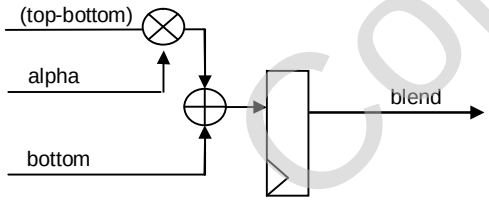


Figure xx Blending Architecture Diagram

Alpha selection is below,

```
if(pixel_dat == color_key)
    alpha = 8'h0;
else if(blk_alpha_sel == 1)
    alpha = block_alpha;
else
    alpha = pixel_alpha;
```

Blending calculation is below,

```
if(alpha == 8'hff)
    blend = top;
else if(alpha == 8'h00)
    blend = bottom;
else
```

```
blend = (top – bottom)*alpha + bottom;
```

Here the top is upper level pixel and the bottom is lower level pixel; alpha is from the upper layer.

The LCDC also supports a new blending mode, it only for 2 layer application, the top layer is a processed result by SW, as a normal layer, it includes RGB data and Alpha data, but the Alpha data is used for bottom layer, the new blending mode is shown below,

blend1 = img_din * osd1_alpha + osd1_din

7.3.4.3 Dithering

Here an threshold-matrix dithering algorithm is presented.

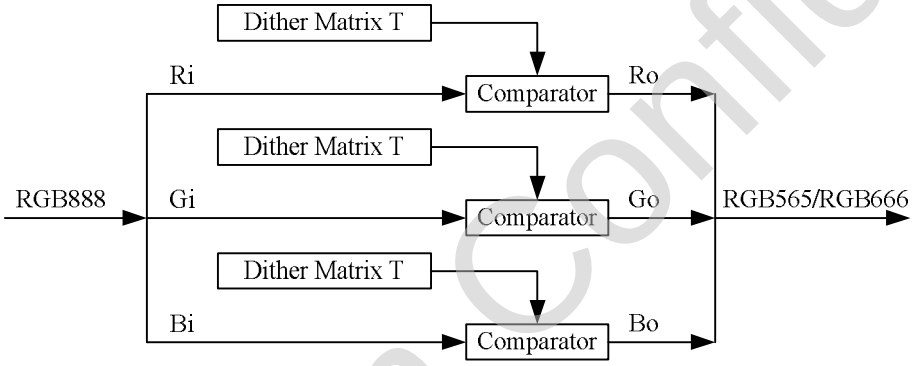


Figure xx Dithering Data Flow

Dithering data flow is shown as Figure xx. In the module which Ri[7:0] is converted to Ro[4:0], the dither matrix T can be a simple 4x4 matrix as follow.

$$\begin{bmatrix} 0 & 4 & 0 & 5 \\ 6 & 2 & 7 & 3 \\ 1 & 5 & 1 & 4 \\ 8 & 3 & 6 & 2 \end{bmatrix}$$

When conversing RGB888 to RGB565, Ri[7:0] is separated to two parts. The first part is the higher five bits Ri[7:3] and the second part is the low three bits Ri[2:0]. The low three bits Ri[2:0] is compared with the corresponding element in the threshold matrix. If Ri[2:0] is bigger than the corresponding element, the Ri[7:3] add 1. Otherwise, Ri[7:3] remains its initial value. The output result Ro[4:0] is equaled with Ri[7:3]. The next pixel does the same cycle processing. In the row direction of image pixel array, column exchange should be done after every four pixel processed. Also namely, the first row move to the fourth row, the rest three rows move forward one by one in order(1->4, 2->1, 3->2, 4->3). After finish four times column exchange, reverse the present threshold matrix, the do the column exchange. In the column direction of image pixel array, row exchange should be done after every four pixel line

processed. After finish four times row exchange, reverse the present threshold matrix, then do the row exchange. The method of row exchange is as same as column exchange which is described above.

When Gi[7:0] is converted to Go[5:0], we the threshold matrix dithering algorithm. The dither matrix T can be a simple 2x2 matrix at follow.

$$\begin{bmatrix} 0 & 2 \\ 3 & 1 \end{bmatrix}$$

Gi[7:0] is separated to two parts. The first part is the higher six bits Gi[7:2] and the second part is the lower two bits Gi[1:0]. The lower two bits Gi[1:0] is compared with the corresponding element in the threshold matrix. If Gi[1:0] is bigger than the corresponding element, the Gi[7:2] adds 1. Otherwise, Gi[7:2] remains it initial value. The output result Go[5:0] is equaled with Gi[7:2].

For Bi[7:0] is converted to Bo[4:0]. We apply the same threshold method for Ri[7:0] to Ro[4:0].

When conversing RGB888 to RGB666, the Ri[7:0], Gi[7:0] and Bi[7:0] all are same as Gi[7:0] at above.

Dithering includes 565 and 666 two modes, when in display mode, the mode decided by LCM's configure; when in capture mode, the mode is decided by capture format.

7.3.4.4 LCM

LCM receives AHB data or LCDC data and transfers them with a specified panel interface. This sub-module's block diagram is shown in below.

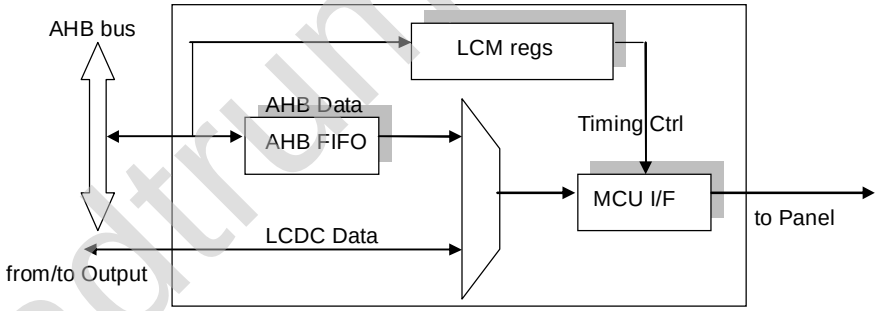


Figure xx LCM Block Diagram

The panel interface is SRAM-like interface, also named MCU interface, it includes 2 types, one is M6800, and the other is I8080. The 8080 and 6800 read/write control is shown as below.

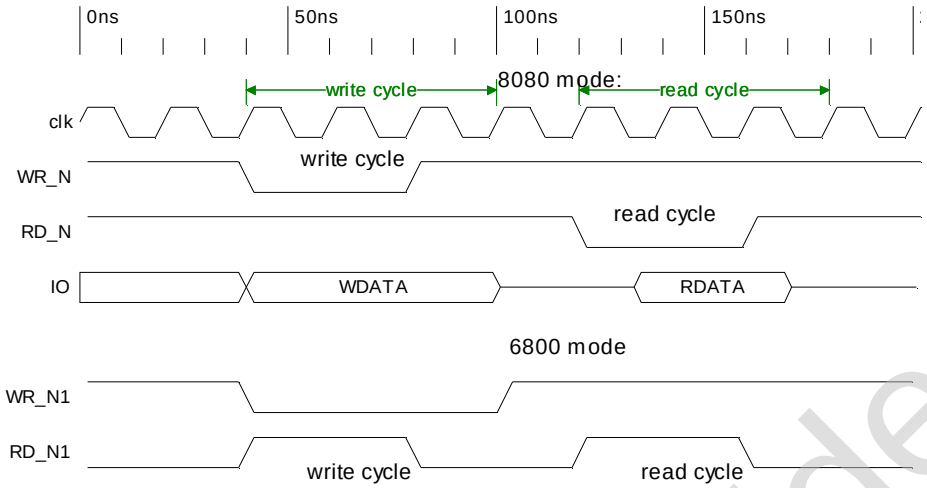


Figure xx 8080/6800 Read/Write Control

The timing of read or write can be configured, the timing parameters are defined below.

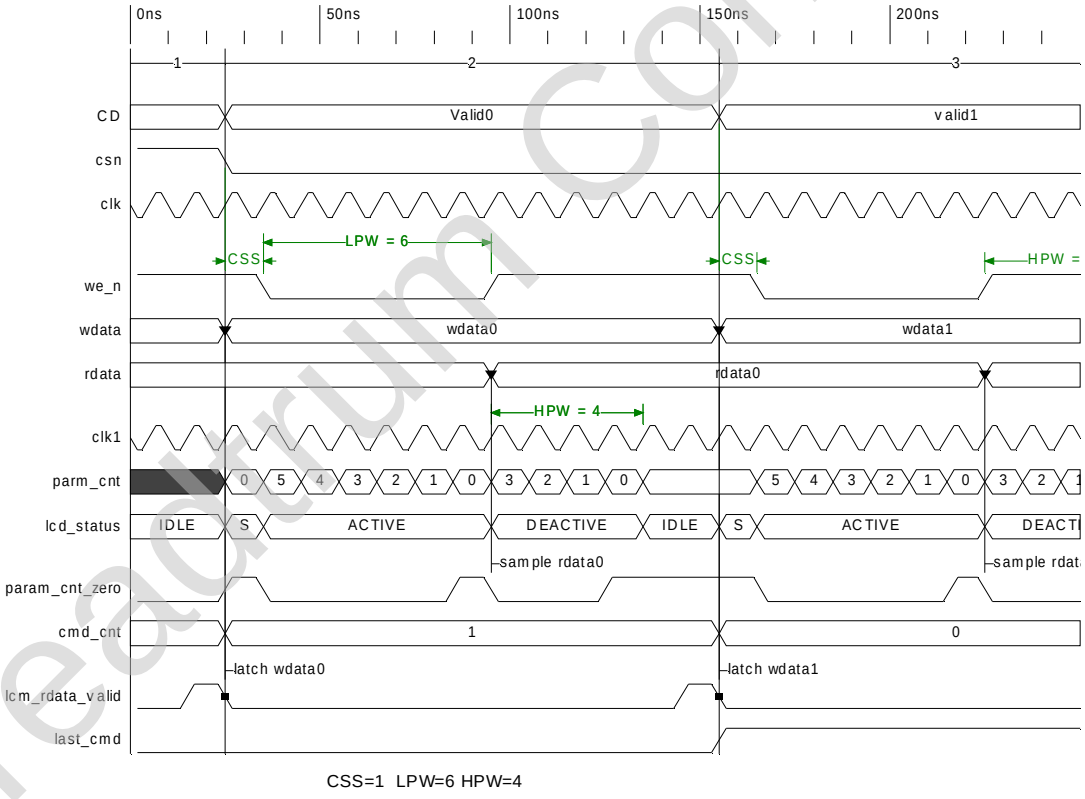


Figure xx LCM Read/Write Timing Parameter Defines

AHB transfer can be used to initialize the panel, test the panel, update few data, read back panel data; LCDC transfer is used for normal display. The AHB data is priority to LCDC data, when LCDC is refreshing, must not send AHB data randomly.

7.3.4.5 Data Flow

The LCDC includes 2 data flow, one is for display, and another is for capture. They are can not work at the same time. They are shown in Figure xx and Figure xx.

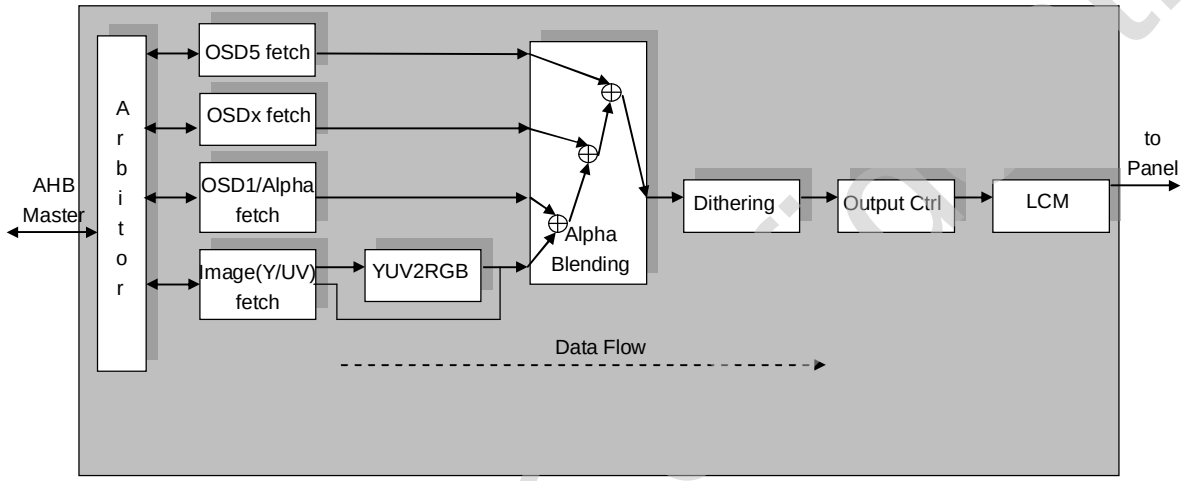


Figure xx Data Flow for Display

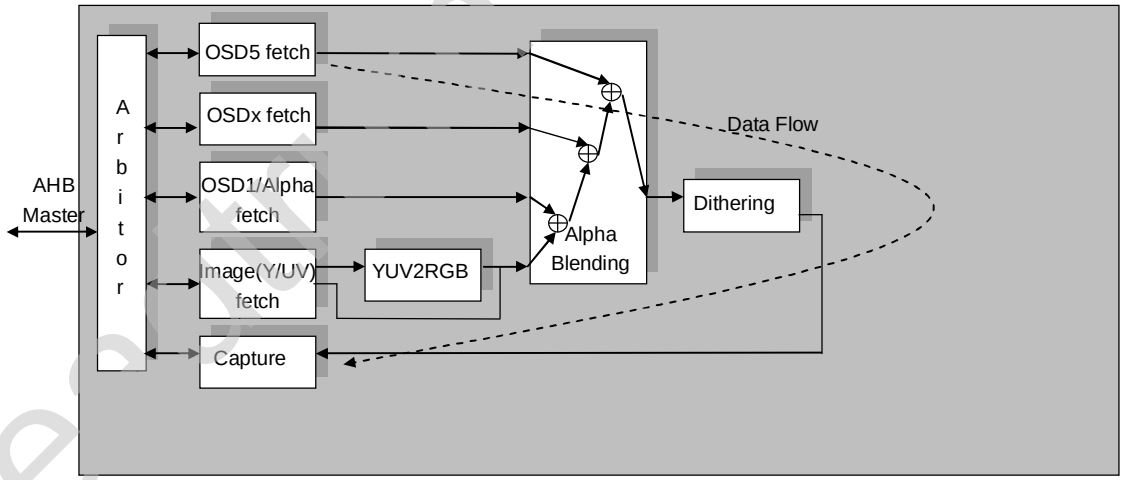


Figure xx Data Flow for Capture

These 2 data flow can separate several stages, following is their detail information.

Data fetch stage:

It includes image fetch and OSD fetch, the image or OSD data stored in memory is linear, this data maybe map to a big picture, but we can trim the picture to our interesting region by configuring a special base address and region size. We must note the next line address should

be added the pitch other than the region's horizontal size. The data view for this stage as below.

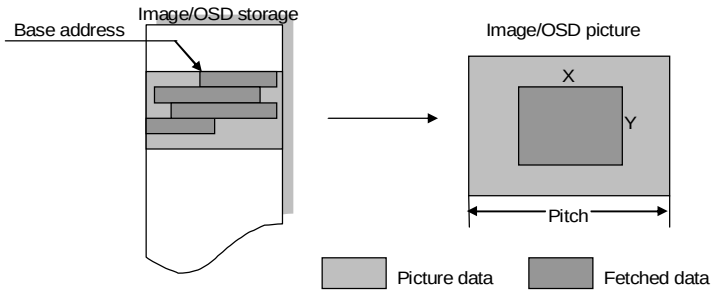


Figure xx Data View in Fetch Stage

Data blending stage:

All active layers data are blended at a work plane based on their owner display start position and size. In single layer region, display the active layer data; in multi layer region, display the blended data; in spare region, display the background. The start position is based the work plane's origin. The data status is shown in Figure xx.

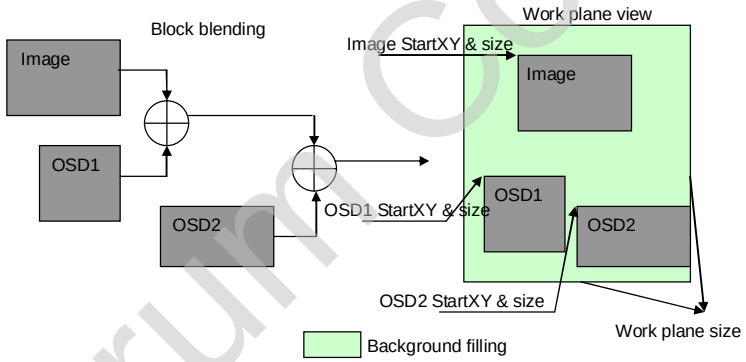


Figure 3.17 Data View in Blending Stage

Data refreshing stage:

After blending, blended data in work plane will be sent to LCM for LCD display. Normally, we update the entire work plane, we also need to update part region for many applications. The LCM window start position and size can decide LCM refreshing region, of course, it can cover the entire plane. The data view as Figure xx.

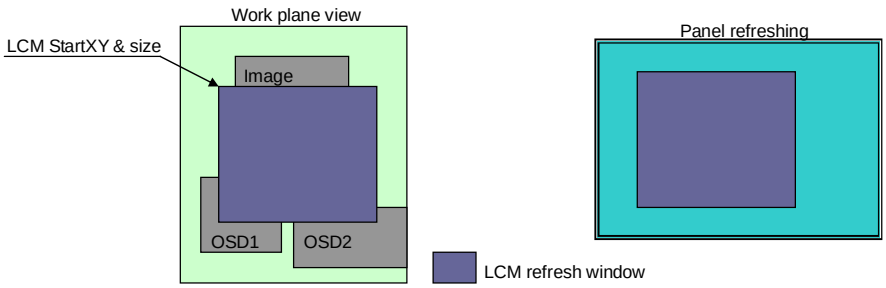


Figure xx Data View in Refreshing Stage

Data capture stage:

In capture mode, the blended data will be wrote back to memory. Normally, we capture the entire picture, but we also need to write back part picture, the capture start position and size can decide our interesting region, the capture base address decide the memory storage position, when write back, the next line address should be added by capture pitch. The data view in capture stage as Figure xx.

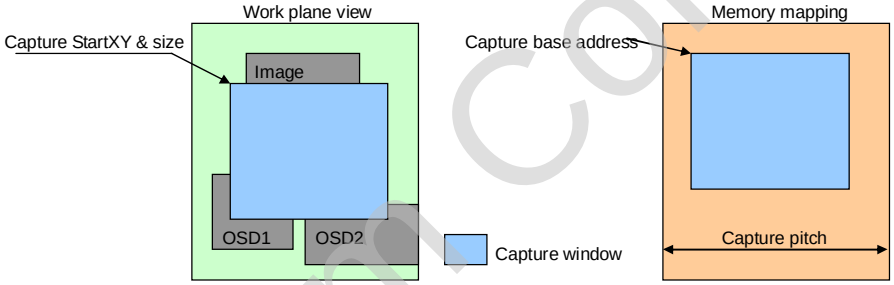


Figure xx Data View in Capture Stage

7.3.5 Control Registers

7.3.5.1 Memory map

ARM Base address: 0x20700000

Table LCDC Control Register Address Map

Offset Address	Name	Description
LCDC Global Control		
0x0000	LCDC_CTRL	LCDC module control
0x0004	LCDC_DISP_SIZE	LCDC work plane size
0x0008	LCDC_LCM_START	LCDC display window start position

0x000c	LCDC_LCM_SIZE	LCDC display window size
0x0010	LCDC_BG_COLOR	LCDC background color
0x0014	LCDC_FIFO_STATUS	LCDC internal FIFO status
Image Layer Control		
0x0020	IMG_CTRL	Image layer configuration
0x0024	IMG_Y_BASE_ADDR	Image layer Y component base address when in YUV format, or image layer base address when in others format.
0x0028	IMG_UV_BASE_ADDR	Image layer UV component base address only when in YUV format.
0x002c	IMG_SIZE_XY	image layer size
0x0030	IMG_PITCH	Image layer pitch
0x0034	IMG_DISP_XY	Image layer start position in work plane.
OSD1 Layer Control		
0x0050	OSD1_CTRL	OSD1 layer configuration
0x0054	OSD1_BASE_ADDR	OSD1 layer data base address
0x0058	OSD1_ALPHA_BASE_ADDR	OSD1 layer alpha data based address only when OSD1 is RGB565 and uses pixel alpha.
0x005c	OSD1_SIZE_XY	OSD1 layer size
0x0060	OSD1_PITCH	OSD1 layer pitch
0x0064	OSD1_DISP_XY	OSD1 layer start position in work plane
0x0068	OSD1_ALPHA	OSD1 layer alpha
0x006c	OSD1_GREY_RGB	OSD1 layer RGB constant of GREY format
0x0070	OSD1_CK	OSD1 layer color-key
OSD2 Layer Control		
0x0080	OSD2_CTRL	OSD2 layer configuration
0x0084	OSD2_BASE_ADDR	OSD2 layer data base address

0x0088	dummy	
0x008c	OSD2_SIZE_XY	OSD2 layer size
0x0090	OSD2_PITCH	OSD2 layer pitch
0x0094	OSD2_DISP_XY	OSD2 layer start position in work plane
0x0098	OSD2_ALPHA	OSD2 layer alpha
0x009c	OSD2_GREY_RGB	OSD2 layer RGB constant of GREY format
0x00a0	OSD2_CK	OSD2 layer color-key
OSD3 Layer Control		
0x00b0	OSD3_CTRL	OSD3 layer configuration
0x00b4	OSD3_BASE_ADDR	OSD3 layer data base address
0x00b8	dummy	
0x00bc	OSD3_SIZE_XY	OSD3 layer size
0x00c0	OSD3_PITCH	OSD3 layer pitch
0x00c4	OSD3_DISP_XY	OSD3 layer start position in work plane
0x00c8	OSD3_ALPHA	OSD3 layer alpha
0x00cc	OSD3_GREY_RGB	OSD3 layer RGB constant of GREY format
0x00d0	OSD3_CK	OSD3 layer color-key
OSD4 Layer Control		
0x00e0	OSD4_CTRL	OSD4 layer configuration
0x00e4	OSD4_BASE_ADDR	OSD4 layer data base address
0x00e8	dummy	
0x00ec	OSD4_SIZE_XY	OSD4 layer size
0x00f0	OSD4_PITCH	OSD4 layer pitch
0x00f4	OSD4_DISP_XY	OSD4 layer start position in work plane
0x00f8	OSD4_ALPHA	OSD4 layer alpha
0x00fc	OSD4_GREY_RGB	OSD4 layer RGB constant of

		GREY format
0x0100	OSD4_CK	OSD4 layer color-key
OSD5 Layer Control		
0x0110	OSD5_CTRL	OSD5 layer configuration
0x0114	OSD5_BASE_ADDR	OSD5 layer data base address
0x0118	dummy	
0x011c	OSD5_SIZE_XY	OSD5 layer size
0x0120	OSD5_PITCH	OSD5 layer pitch
0x0124	OSD5_DISP_XY	OSD5 layer start position in work plane
0x0128	OSD5_ALPHA	OSD5 layer alpha
0x012c	OSD5_GREY_RGB	OSD5 layer RGB constant of GREY format
0x0130	OSD5_CK	OSD5 layer color-key
Capture Control		
0x0140	CAP_CTRL	Capture configuration
0x0144	CAP_BASE_ADDR	Capture base address
0x0148	CAP_START_XY	Capture start position in work plane
0x014c	CAP_SIZE_XY	Capture size
0x0150	CAP_PITCH	Capture pitch
YUV2RGB Control		
0x0160	Y2R_CTRL	YUV to RGB configuration
0x0164	Y2R_CONTRAST	Adjustment value of contrast
0x0168	Y2R_SATURATION	Adjustment value of saturation
0x016c	Y2R_BRIGHTNESS	Adjustment value of brightness
Interrupt Control		
0x0170	LCDC_IRQ_EN	LCDC interrupt enable
0x0174	LCDC_IRQ_CLR	LCDC interrupt clear
0x0178	LCDC_IRQ_STATUS	LCDC masked interrupt
0x017c	LCDC_IRQ_RAW	LCDC raw interrupt

LCM Control		
0x0180	LCM_CTRL	LCM device configuration
0x0184	LCM_TIMING0	Timing setting for CS0 device
0x0188	LCM_TIMING1	Timing setting for CS1 device
0x018c	LCM_RDATA	Read back data from LCM device
0x0190	LCM_RSTN	LCM device reset control
0x01a0	LCM_CMD	AHB channel command
0x01a4	LCM_DATA	AHB channel data

7.3.5.2 Register Descriptions

7.3.5.2.1 LCDC_CTRL

Description: LCDC module control

0x0000			LCDC module control (reset 0x0)												LCDC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	REQ_GAP								Reserved		BLEND_MODE	DITHER_EN	LCDC_RUN	FMARK_POL	FMARK_MODE	LCDC_EN
Type	R/W								RO		R/W	R/W	WO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
REQ_GAP	[15:8]	R/W	8'h0	The interval between 2 AHB master requests.
	[7:6]	RO	2'h0	Reserved

BLEND_MODE	[5]	R/W	1'h0	Blending mode 0- L = L0*(1-alpha) + L1*alpha; 1- L = L0*alpha + L1 (only for 2 layer application).
DITHER_EN	[4]	R/W	1'h0	dithering enable 0-disable; 1-enable. Dithering includes 565 and 666 two modes, when in display mode, the mode decided by LCM setting; when in capture mode, the mode is decided by capture format.
LCDC_RUN	[3]	WO	1'h0	LCDC run, write '1' to run the LCDC, it will be cleared by HW.
FMARK_POL	[2]	R/W	1'h0	Fmark signal polarity control 0-fmark valid at '1'; 1-fmark valid at '0'.
FMARK_MODE	[1]	R/W	1'h0	External FMARK panel setting 0-FMARK device; 1-Non-FMARK device.
LCDC_EN	[0]	R/W	1'h0	LCDC enable control 0-LCDC Disable 1-LCDC Enable;

7.3.5.2.2 LCDC_DISP_SIZE

Description: LCDC work plane size.

0x0004			LCDC work plane size (reset 0x0)													LCDC_DISP_SIZE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				DISP_SIZE_Y											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				DISP_SIZE_X											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
DISP_SIZE_Y	[27:16]	R/W	12'h0	Work plane vertical size, should be >0 and <1024.
	[15:12]	RO	4'h0	Reserved
DISP_SIZE_X	[11:0]	R/W	12'h0	Work plane horizontal size, should be >0 and <1024.

7.3.5.2.3 LCDC_LCM_START

Description: LCDC display window start position.

0x0008			LCDC display window start position (reset 0x0)													LCDC_LCM_START
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				LCM_START_Y											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				LCM_START_X											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
LCM_START_Y	[27:16]	R/W	14'h0	Display window vertical start position, it is based on the top left point of work plane. Please ensure it is in work plane.
	[15:12]	RO	4'h0	Reserved
LCM_START_X	[11:0]	R/W	12'h0	Display window horizontal start position, it is based on the top left point of work plane. Please ensure it is in work plane.

7.3.5.2.4 LCDC_LCM_SIZE

Description: LCDC display window size

0x000c			LCDC display window size (reset 0x0)													LCDC_LCM_SIZE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				LCM_SIZE_Y											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				LCM_SIZE_X											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
LCM_SIZE_Y	[27:16]	R/W	12'h0	Display window vertical size, it is based on the top left point of work plane. Please ensure it is in work plane.
	[15:12]	RO	4'h0	Reserved
LCM_SIZE_X	[11:0]	R/W	12'h0	Display window horizontal size, it is based on the top left point of work plane. Please ensure it is in work plane.

7.3.5.2.5 LCDC_BG_COLOR

Description: LCDC background color.

0x0010			LCDC background color (reset 0x0)													LCDC_BG_COLOR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved								BG_R							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BG_G								BG_B							
Type	R/W								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:24]	RO	8'h0	Reserved
BG_R	[23:16]	R/W	8'h0	Background red
BG_G	[15:8]	R/W	8'h0	Background green
BG_B	[7:0]	R/W	8'h0	Background blue

7.3.5.2.6 LCDC_FIFO_STATUS

Description: LCDC internal FIFO status.

0x0014	LCDC internal FIFO status (reset 0x155555)												LCDC_FIFO_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved										OUTPUT_FIFO_STS		DITHER_FIFO_STS		Y2R_FIFO_STS	
Type	RO										RO		RO		RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	OSD5_FIFO_STS		OSD4_FIFO_STS		OSD3_FIFO_STS		OSD2_FIFO_STS		OSD1_FIFO_STS		OSD1_ALPHA_FIFO_STS		IMG_UV_FIFO_STS		IMG_Y_FIFO_STS	
Type	RO		RO		RO		RO		RO		RO		RO		RO	
Reset	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Field Name	Bit	Type	Reset Value	Description
	[31:22]	RO	10’h0	Reserved
OUTPUT_FIFO_STS	[21:20]	RO	2’h01	Cross domain FIFO info. [21] - FIFO full status, ‘1’ for full; [20] - FIFO empty status, ‘1’ for empty.
DITHER_FIFO_STS	[19:18]	RO	2’h01	Dithering output FIFO info. [19] - FIFO full status, ‘1’ for full; [18] - FIFO empty status, ‘1’ for empty.
Y2R_FIFO_STS	[17:16]	RO	2’h01	YUV to RGB work FIFO info. [17] - FIFO full status, ‘1’ for full; [16] - FIFO empty status, ‘1’ for empty
OSD5_FIFO_STS	[15:14]	RO	2’h01	OSD5 layer FIFO info. [15] - FIFO full status, ‘1’ for full; [14] - FIFO empty status, ‘1’ for empty
OSD4_FIFO_STS	[13:12]	RO	2’h01	OSD4 layer FIFO info. [13] - FIFO full status, ‘1’ for full; [12] - FIFO empty status, ‘1’ for empty
OSD3_FIFO_STS	[11:10]	RO	2’h01	OSD3 layer FIFO info. [11] - FIFO full status, ‘1’ for full;

				[10] - FIFO empty status, ‘1’ for empty
OSD2_FIFO_STS	[9:8]	RO	2’h01	OSD2 layer FIFO info. [9] - FIFO full status, ‘1’ for full; [8] - FIFO empty status, ‘1’ for empty
OSD1_FIFO_STS	[7:6]	RO	2’h01	OSD1 layer FIFO info. [7] - FIFO full status, ‘1’ for full; [6] - FIFO empty status, ‘1’ for empty
OSD1_ALPHA_FIFO_STS	[5:4]	RO	2’h01	OSD1 layer alpha FIFO info, it is active when OSD1 is RGB565 with pixel alpha. [5] - FIFO full status, ‘1’ for full; [4] - FIFO empty status, ‘1’ for empty
IMG_UV_FIFO_STS	[3:2]	RO	2’h01	Image layer UV data FIFO info, it is active when image is YUV422 and YUV420 format. [3] - FIFO full status, ‘1’ for full; [2] - FIFO empty status, ‘1’ for empty.
IMG_Y_FIFO_STS	[1:0]	RO	2’h01	Image layer Y data FIFO info. [1] - FIFO full status, ‘1’ for full; [0] - FIFO empty status, ‘1’ for empty

7.3.5.2.7 IMG_CTRL

Description: Image layer configuration.

0x0020			Image layer configuration (reset 0x0)													IMG_CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				IMG_UV_SWITCH		IMG_RB_SWITCH	IMG_Y_SWITCH		IMG_FORMAT				Reserved		IMG_EN
Type	RO				R/W		R/W	R/W		R/W				RO		R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:12]	RO	20'h0	Reserved
IMG_UV_SWITCH	[11:10]	R/W	2'h0	When image data is RGB format, it is useless; when image data is YUV format, it is image layer UV data byte order in a 32bits word, the source is $B_0B_1B_2B_3$, the destination is: 0-$B_0B_1B_2B_3$; 1-$B_3B_2B_1B_0$; 2-$B_2B_3B_0B_1$; 3-reserved.
IMG_RB_SWITCH	[9]	R/W	1'h0	R/B order switch for RGB data 0- DONOT switch; 1- exchange R and B. Active for RGB888/666/565/555 data.
IMG_Y_SWITCH	[8:7]	R/W	2'h0	Image layer Y/RGB data byte order in a 32bits word, the source is $B_0B_1B_2B_3$, the destination is: 0-$B_0B_1B_2B_3$; 1-$B_3B_2B_1B_0$;

				2-$B_2B_3B_0B_1$; 3-reserved.
IMG_FORMAT	[6:3]	R/W	4'h0	Image layer data format, it supports following ones: 0000-YUV422; 0001-YUV420; 0010-YUV400; 0011-RGB888; 0100-RGB666; 0101-RGB565; 0110-RGB555; Others are invalid.
	[2:1]	RO	2'h0	Reserved
IMG_EN	[0]	R/W	1'h0	Image layer enable 0-disable; 1-enable.

7.3.5.2.8 IMG_Y_BASE_ADDR

Description: Image Y component base address.

0x0024	Image Y component base address (reset 0x0)												IMG_Y_BASE_ADDR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	IMG_Y_BASE_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	IMG_Y_BASE_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
IMG_Y_BASE_ADDR	[31:0]	R/W	32'h0	When image is YUV format, it is Y data base

				address; when image is RGB format, it is RGB data base address.

7.3.5.2.9 IMG_UV_BASE_ADDR

Description: Image UV component base address.

0x0028			Image UV component base address (reset 0x0)										IMG_UV_BASE_ADDR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	IMG_UV_BASE_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	IMG_UV_BASE_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
IMG_UV_BASE_ADDR	[31:0]	R/W	32'h0	When image is YUV format, it is UV data base address; otherwise, it is useless.

7.3.5.2.10 IMG_SIZE_XY

Description: Image layer size.

0x002c			Image layer size (reset 0x0)													IMG_SIZE_XY
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				IMG_SIZE_Y											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				IMG_SIZE_X											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
IMG_SIZE_Y	[27:16]	R/W	12'h0	Image layer vertical size, it is based on the top left point of work plane. Please ensure it is in work plane.
	[15:12]	RO	4'h0	Reserved
IMG_SIZE_X	[11:0]	R/W	12'h0	Image layer horizontal size, it is based on the top left point of work plane. Please ensure it is in work plane, and image data is word aligned.

7.3.5.2.11 IMG_PITCH

Description: Image layer pitch.

0x0030			Image layer pitch (reset 0x0)													IMG_PITCH
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				IMG_PITCH											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:12]	RO	20'h0	Reserved
IMG_PITCH	[11:0]	R/W	12'h0	Image layer pitch.

7.3.5.2.12 IMG_DISP_XY

Description: Image layer start position.

0x0034			Image layer start position (reset 0x0)													IMG_DISP_XY
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				IMG_DISP_Y											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				IMG_DISP_X											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RO	4'h0	Reserved

IMG_DISP_Y	[27:16]	R/W	12'h0	Image layer vertical start position, it is based on the top left point of work plane. Please ensure it is in work plane.
	[15:12]	RO	4'h0	Reserved
IMG_DISP_X	[11:0]	R/W	12'h0	Image layer horizontal start position, it is based on the top left point of work plane. Please ensure it is in work plane.

7.3.5.2.13 OSDx_CTRL

Description: OSD layer configuration, x=1~5.

0x0050	**OSD1 layer configuration (reset 0x0)**															**OSD1_CTRL**
0x0080	**OSD2 layer configuration (reset 0x0)**															**OSD2_CTRL**
0x00b0	**OSD3 layer configuration (reset 0x0)**															**OSD3_CTRL**
0x00e0	**OSD4 layer configuration (reset 0x0)**															**OSD4_CTRL**
0x0110	**OSD5 layer configuration (reset 0x0)**															**OSD5_CTRL**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				OSD1_ALPHA_SWITCH		OSDx_RB_SWITCH	OSDx_SWITCH		OSDx_FORMAT				OSDx_ALPHA_SEL	OSDx_CK_EN	OSDx_EN
Type	RO				R/W		R/W	R/W		R/W				R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:12]	RO	20'h0	Reserved
OSD1_ALPHA_SWITCH	[11:10]	R/W	2'h0	OSD1 layer alpha data byte order in a

				32bits word, the source is $B_0B_1B_2B_3$, the destination is: 0-$B_0B_1B_2B_3$; 1-$B_3B_2B_1B_0$; 2-$B_2B_3B_0B_1$; 3-reserved. NOTE: only OSD1 layer has this field, and it is active when OSD1 layer format is RGB565 with pixel alpha.
OSDx_RB_SWITCH	[9]	R/W	1'h0	R/B order switch for RGB data 0- DONOT switch; 1- exchange R and B. Active for RGB888/666/565/555 data.
OSDx_SWITCH	[8:7]	R/W	2'h0	OSD layer data byte order in a 32bits word, the source is $B_0B_1B_2B_3$, the destination is: 0-$B_0B_1B_2B_3$; 1-$B_3B_2B_1B_0$; 2-$B_2B_3B_0B_1$; 3-reserved.
OSDx_FORMAT	[6:3]	R/W	4'h0	OSD layer data format, it supports following ones: 0011-RGB888; 0100-RGB666; 0101-RGB565; 0110-RGB555; 0111-GREY; Others are invalid.
OSDx_ALPHA_SEL	[2]	R/W	1'h0	OSD layer alpha selection, 0-pixel alpha; 1-block alpha. When RGB565 format, only OSD1 support pixel alpha, others OSD layers will ignore this setting, and use its layer alpha.
OSDx_CK_EN	[1]	R/W	1'h0	OSD layer color key enable,

				0-disable; 1-enable.
OSDx_EN	[0]	R/W	1'h0	OSD layer enable, 0-disable; 1-enable.

7.3.5.2.14 OSDx_BASE_ADDR

Description: OSD layer base address, x=1~5.

0x0054	**OSD1 layer base address (reset 0x0)**														**OSD1_BASE_ADDR**
0x0084	**OSD2 layer base address (reset 0x0)**														**OSD2_BASE_ADDR**
0x00b4	**OSD3 layer base address (reset 0x0)**														**OSD3_BASE_ADDR**
0x00e4	**OSD4 layer base address (reset 0x0)**														**OSD4_BASE_ADDR**
0x0114	**OSD5 layer base address (reset 0x0)**														**OSD5_BASE_ADDR**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	OSDx_BASE_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	OSDx_BASE_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
OSDx_BASE_ADDR	[31:0]	R/W	32'h0	Base address of OSD layer data.

7.3.5.2.15 OSD1_ALPHA_BASE_ADDR

Description: OSD1 layer alpha data base address.

0x0058			OSD1 layer alpha base address (reset 0x0)												OSD1_ALPHA_BASE_ADDR	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	OSD1_ALPHA_BASE_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	OSD1_ALPHA_BASE_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
OSD1_ALPHA_BASE_ADDR	[31:0]	R/W	32'h0	When OSD1 data is RGB565 format, it is base address of OSD1 alpha data, else it is not used.

7.3.5.2.16 OSDx_SIZE_XY

Description: OSD layer size, x=1~5.

0x005c	**OSD1 layer size (reset 0x0)**															**OSD1_SIZE_XY**
0x008c	**OSD2 layer size (reset 0x0)**															**OSD2_SIZE_XY**
0x00bc	**OSD3 layer size (reset 0x0)**															**OSD3_SIZE_XY**
0x00ec	**OSD4 layer size (reset 0x0)**															**OSD4_SIZE_XY**
0x011c	**OSD5 layer size (reset 0x0)**															**OSD5_SIZE_XY**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				OSDx_SIZE_Y											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				OSDx_SIZE_X											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
OSDx_SIZE_Y	[27:16]	R/W	12'h0	OSD layer vertical size, it is based on the top left point of work plane. Please ensure it is in work plane.
	[15:12]	RO	4'h0	Reserved
OSDx_SIZE_X	[11:0]	R/W	12'h0	OSD layer horizontal size, it is based on the top left point of work plane. Please ensure it is in work plane, and OSD data is word aligned.

7.3.5.2.17 OSDx_PITCH

Description: OSD layer pitch, x=1~5.

0x0060			**OSD1 layer pitch (reset 0x0)**													**OSD1_PITCH**
0x0090			**OSD2 layer pitch (reset 0x0)**													**OSD2_PITCH**
0x00c0			**OSD3 layer pitch (reset 0x0)**													**OSD3_PITCH**
0x00f0			**OSD4 layer pitch (reset 0x0)**													**OSD4_PITCH**
0x0120			**OSD5 layer pitch (reset 0x0)**													**OSD5_PITCH**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				OSDx_PITCH											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:12]	RO	20'h0	Reserved
OSDx_PITCH	[11:0]	R/W	12'h0	OSD layer pitch.

7.3.5.2.18 OSDx_DISP_XY

Description: OSD layer start position, x=1~5.

0x0064	OSD1 layer start position (reset 0x0)	OSD1_DISP_XY
0x0094	OSD2 layer start position (reset 0x0)	OSD2_DISP_XY
0x00c4	OSD3 layer start position (reset 0x0)	OSD3_DISP_XY
0x00f4	OSD4 layer start position (reset 0x0)	OSD4_DISP_XY
0x0124	OSD5 layer start position (reset 0x0)	OSD5_DISP_XY

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved				OSDx_DISP_Y											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved				OSDx_DISP_X											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
OSDx_DISP_Y	[27:16]	R/W	12'h0	OSD layer vertical size, it is based on the top left point of work plane. Please ensure it is in work plane.
	[15:12]	RO	4'h0	Reserved
OSDx_DISP_X	[11:0]	R/W	12'h0	OSD layer horizontal size, it is based on the top left point of work plane. Please ensure it is in work plane.

7.3.5.2.19 OSDx_ALPHA

Description: OSD layer alpha, x=1~5.

0x0068			**OSD1 alpha (reset 0x0)**													**OSD1_ALPHA**
0x0098			**OSD2 alpha (reset 0x0)**													**OSD2_ALPHA**
0x00c8			**OSD3 alpha (reset 0x0)**													**OSD3_ALPHA**
0x00f8			**OSD4 alpha (reset 0x0)**													**OSD4_ALPHA**
0x0128			**OSD5 alpha (reset 0x0)**													**OSD5_ALPHA**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								OSDx_ALPHA							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
OSDx_ALPHA	[7:0]	R/W	8'h0	OSD layer alpha.

7.3.5.2.20 OSDx_GREY_RGB

Description: OSD layer RGB constant of GREY format, x=1~5.

0x006c	**OSD1 layer RGB constant of GREY format (reset 0x0)**															**OSD1_GREY_RBG**
0x009c	**OSD2 layer RGB constant of GREY format (reset 0x0)**															**OSD2_GREY_RBG**
0x00cc	**OSD3 layer RGB constant of GREY format (reset 0x0)**															**OSD3_GREY_RBG**
0x00fc	**OSD4 layer RGB constant of GREY format (reset 0x0)**															**OSD4_GREY_RBG**
0x012c	**OSD5 layer RGB constant of GREY format (reset 0x0)**															**OSD5_GREY_RBG**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved								OSDx_GREY_R							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	OSDx_GREY_G								OSDx_GREY_B							
Type	R/W								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:24]	RO	8'h0	Reserved
OSDx_GREY_R	[23:16]	R/W	8'h0	Constant R for GREY data format in OSD layer.
OSDx_GREY_G	[15:8]	R/W	8'h0	Constant G for GREY data format in OSD layer.
OSDx_GREY_B	[7:0]	R/W	8'h0	Constant B for GREY data format in OSD layer.

7.3.5.2.21 OSDx_CK

Description: OSD layer color-key, x=1~5.

0x0070			**OSD1 layer color-key (reset 0x0)**													**OSD1_CK**
0x00a0			**OSD2 layer color-key (reset 0x0)**													**OSD2_CK**
0x00d0			**OSD3 layer color-key (reset 0x0)**													**OSD3_CK**
0x0100			**OSD4 layer color-key (reset 0x0)**													**OSD4_CK**
0x0130			**OSD5 layer color-key (reset 0x0)**													**OSD5_CK**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved								OSDx_CK_R							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	OSDx_CK_G								OSDx_CK_B							
Type	R/W								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:24]	RO	8'h0	Reserved
OSDx_CK_R	[23:16]	R/W	8'h0	Color-key R value for OSD layer.
OSDx_CK_G	[15:8]	R/W	8'h0	Color-key G value for OSD layer.
OSDx_CK_B	[7:0]	R/W	8'h0	Color-key B value for OSD layer.

7.3.5.2.22 CAP_CTRL

Description: Capture configuration.

0x0140	Capture configuration (reset 0x0)												CAP_CTRL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										CAP_RB_SWITCH	CAP_SWITCH		CAP_FORMAT		CAP_EN
Type	RO										R/W	R/W		R/W		R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:6]	RO	26'h0	Reserved
CAP_RB_SWITCH	[5]	R/W	1'h0	R/B order switch for RGB data 0- DONOT switch; 1- exchange R and B.
CAP_SWITCH	[4:3]	R/W	2'h0	Captured data byte order in a 32bits word, the source is $B_0B_1B_2B_3$, the destination is: 0-$B_0B_1B_2B_3$; 1-$B_3B_2B_1B_0$; 2-$B_2B_3B_0B_1$; 3-reserved.
CAP_FORMAT	[2:1]	R/W	2'h0	Data storage format, 00-RGB888; 01-RGB666; 10-RGB565; 11-reserved.
CAP_EN	[0]	R/W	1'h0	Capture enable, 0-disable;

				1-enable

7.3.5.2.23 CAP_BASE_ADDR

Description: Capture base address.

0x0144			Capture base address (reset 0x0)										CAP_BASE_ADDR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	CAP_BASE_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CAP_BASE_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
CAP_BASE_ADDR	[31:0]	R/W	32'h0	Capture base address.

7.3.5.2.24 CAP_START_XY

Description: Capture start position in work plane.

0x0148			Capture start position in work plane (reset 0x0)										CAP_START_XY			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				CAP_START_Y											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				CAP_START_X											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
CAP_START_Y	[27:16]	R/W	12'h0	Capture window start Y position, it is based on the top left point of work plane. Please ensure it is in work plane.
	[15:12]	RO	4'h0	Reserved
CAP_START_X	[11:0]	R/W	12'h0	Capture window start X position, it is based on the top left point of work plane. Please ensure it is in work plane.

7.3.5.2.25 CAP_SIZE_XY

Description: Capture size.

0x014c			Capture size (reset 0x0)													CAP_SIZE_XY
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				CAP_SIZE_Y											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				CAP_SIZE_X											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
CAP_SIZE_Y	[27:16]	R/W	12'h0	Capture window size in Y, it is based on the top left point of work plane. Please ensure it is in work plane.
	[15:12]	RO	4'h0	Reserved
CAP_SIZE_X	[11:0]	R/W	12'h0	Capture window size in X, it is based on the top left point of work plane. Please

				ensure it is in work plane, and image data is word aligned.

7.3.5.2.26 CAP_PITCH

Description: Capture pitch.

0x0150	Capture pitch (reset 0x0)												CAP_PITCH			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				CAP_PITCH											
Type	RO				R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:12]	RO	20'h0	Reserved
CAP_PITCH	[11:0]	R/W	12'h0	Capture pitch.

7.3.5.2.27 Y2R_CTRL

Description: YUV to RGB configuration.

0x0160	YUV to RGB configuration (reset 0x0)															Y2R_CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															Y2R_CTRL
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:1]	RO	31'h0	Reserved
Y2R_CTRL	[0]	R/W	1'h0	UV horizontal up-sampling mode, 0-duplicated; 1-average.

7.3.5.2.28 Y2R_CONTRAST

Description: Adjustment value of contrast.

0x0164	Adjustment value of contrast (reset 0x0)															Y2R_CONTRAST
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								Y2R_CONTRAST							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
Y2R_CONTRAST	[7:0]	R/W	8'h0	Contrast configuration, 0~255.

7.3.5.2.29 Y2R_SATURATION

Description: Adjustment value of saturation.

0x0168	Adjustment value of saturation (reset 0x0)												Y2R_SATURATION			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								Y2R_SATURATION							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
Y2R_SATURATION	[7:0]	R/W	8'h0	Saturation configuration, 0~255.

7.3.5.2.30 Y2R_BRIGHTNESS

Description: Adjustment value of brightness.

0x016c			Adjustment value of brightness (reset 0x0)													Y2R_BRIGHTNESS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							Y2R_BRIGHTNESS								
Type	RO							R/W								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:9]	RO	23'h0	Reserved
Y2R_BRIGHTNESS	[8:0]	R/W	9'h0	Brightness configuration (S9), -256~255.

7.3.5.2.31 LCDC_IRQ_EN

Description: LCDC interrupt enable.

0x0170			LCDC interrupt enable (reset 0x0)												LCDC_IRQ_EN	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														IRQ_FMARK_EN	IRQ_LCDC_DONE_EN
Type	RO														R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:2]	RO	30'h0	Reserved
IRQ_FMARK_EN	[1]	R/W	1'h0	Enable FMARK interrupt, the interrupt is for LCDC detect a FMARK input.
IRQ_LCDC _DONE_EN	[0]	R/W	1'h0	Enable LCDC_DONE interrupt, the interrupt is for LCDC completing display or capture.

7.3.5.2.32 LCDC_IRQ_CLR

Description: LCDC interrupt clear.

0x0174			LCDC interrupt clear (reset 0x0)												LCDC_IRQ_CLR	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														IRQ_FMARK_CLR	IRQ_LCDC_DONE_CLR
Type	RO														WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:2]	RO	30'h0	Reserved
IRQ_FMARK_CLR	[1]	WO	1'h0	Write '1' to clear FMARK interrupt.
IRQ_LCDC_DONE_CLR	[0]	WO	1'h0	Write '1' to clear LCDC_DONE interrupt.

7.3.5.2.33 LCDC_IRQ_STATUS

Description: LCDC masked interrupt status.

0x0178			LCDC masked interrupt status (reset 0x0)													LCDC_IRQ_STATUS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														IRQ_FMARK_STS	IRQ_LCDC_DONE_STS
Type	RO														RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:2]	RO	30'h0	Reserved
IRQ_FMARK_STS	[1]	RO	1'h0	Masked FMARK interrupt.
IRQ_LCDC_DONE_STS	[0]	RO	1'h0	Masked LCDC_DONE interrupt.

7.3.5.2.34 LCDC_IRQ_RAW

Description: LCDC raw interrupt status.

0x017c			LCDC raw interrupt status (reset 0x0)												LCDC_IRQ_RAW	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														IRQ_FMARK_RAW	IRQ_LCDC_DONE_RAW
Type	RO														RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:2]	RO	30'h0	Reserved
IRQ_FMARK_RAW	[1]	RO	1'h0	Raw FMARK interrupt.
IRQ_LCDC_DONE_RAW	[0]	RO	1'h0	Raw LCDC_DONE interrupt.

7.3.5.2.35 LCM_CTRL

Description: LCM control.

0x0180	LCM control (reset 0x0)															LCM_CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved									LCM_STS		AHB_ACT	Reserved			LCM_CS
Type	RO									RO		RO	RO			R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		PIXEL_BITS1		IF_BITS1			IF_TYPE1	Reserved		PIXEL_BITS0		IF_BITS0			IF_TYPE0
Type	RO		R/W		R/W			R/W	RO		R/W		R/W			R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:23]	RO	9'h0	Reserved
LCM_STS	[22:21]	RO	2'h0	LCM work status, only for debug purpose. 0- LCM state is in idle; 1- LCM state is in setup; 2- LCM state is in low; 3- LCM state is in high.
AHB_ACT	[20]	RO	1'h0	AHB channel status in current LCM 0- Idle; 1- Active, some AHB channel CMD/DATA is sending. It is ready to send next CMD/DATA when it is idle, it must inquire this status bit before every AHB channel read/write.
	[19:17]	RO	3'h0	Reserved
LCM_CS	[16]	R/W	1'h0	LCM selection 0- use LCM0 device;

				1- use LCM1 device.
	[15:14]	RO	2'h0	Reserved
PIXEL_BITS1	[13:12]	R/W	2'h0	Panel pixel data bit width for LCM1 device 0- 16bits; 1- 18bits; 2- 24bits; Others are reserved.
IF_BITS1	[11:9]	R/W	3'h0	LCM interface bus width for LCM1 device 0- 8bits; 1- 9bits; 2- 16bits; 3- 18bits; 4- 24bits; Others are reserved.
IF_TYPE1	[8]	R/W	1'h0	LCM interface type for LCM1 device 0- 8080; 1- 6800.
	[7:6]	RO	2'h0	Reserved
PIXEL_BITS0	[5:4]	R/W	2'h0	Panel pixel data bit width for LCM0 device 0- 16bits; 1- 18bits; 2- 24bits; Others are reserved.
IF_BITS0	[3:1]	R/W	3'h0	LCM interface bus width for LCM0 device 0- 8bits; 1- 9bits; 2- 16bits; 3- 18bits; 4- 24bits; Others are reserved.
IF_TYPE0	[0]	R/W	1'h0	LCM interface type for LCM0 device

				0- 8080; 1- 6800.

7.3.5.2.36 LCM_TIMING

Description: LCM read/write timing setting.

0x0184			LCM timing for active LCM0 device (reset 0x0)										LCM_TIMING0			
0x0188			LCM timing for active LCM1 device (reset 0x0)										LCM_TIMING1			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved				RCSS				RLPW				RHPW			
Type	RO				R/W				R/W				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				WCSS				WLPW				WHPW			
Type	RO				R/W				R/W				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RO	4'h0	Reserved
RCSS	[27:24]	R/W	4'h0	Read to CS setup time, it is 0~3.
RLPW	[23:20]	R/W	4'h0	Read low pulse width, it is 0~15.
RHPW	[19:16]	R/W	4'h0	Read high pulse width, it is 0~15.
	[15:12]	RO	4'h0	Reserved
WCSS	[11:8]	R/W	4'h0	Write to CS setup time, it is 0~15.
WLPW	[7:4]	R/W	4'h0	Write low pulse Width, it is 0~15.
WHPW	[3:0]	R/W	4'h0	Write high pulse width, it is 0~15.

NOTE: Above settings all are HCLK unit.

7.3.5.2.37 LCM_RDATA

Description: LCM read back data.

0x018c			LCM read back data (reset 0x0)													LCM_RDATA
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	LCM_RDATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LCM_RDATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
LCM_RDATA	[31:0]	RO	32'h0	Read back data from device.

7.3.5.2.38 LCM_RSTN

Description: External panel reset control.

0x0190			External panel reset control (reset 0x0)													LCM_RSTN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															LCM_RST_N
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

	[31:1]	RO	31'h0	Reserved
LCM_RST_N	[0]	R/W	1'h0	Panel reset control, '0'- reset panel. The watch-dog reset doesn't affect it.

7.3.5.2.39 LCM_CMD

Description: LCM AHB channel command output.

0x01a0			LCM0 AHB channel command (reset 0x0)										LCM_CMD0			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved								LCM_CMD							
Type	RO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LCM_CMD															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:24]	RO	8'h0	Reserved
LCM_CMD	[23:0]	WO	24'h0	Write data to device with CD=0.

7.3.5.2.40 LCM_DATA

Description: LCM AHB channel data output.

0x01a4			LCM0 AHB channel data (reset 0x0)													LCM_DATA0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved							LCM_RW	LCM_DATA							
Type	RO							WO	WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LCM_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:25]	RO	7'h0	Reserved
LCM_RW	[24]	WO	1'h0	Read/write flag, 0- write; 1- read.
LCM_DATA	[23:0]	WO	24'h0	Write data to device with CD=1.

7.3.6 Application Notes

7.3.6.1 Program Flow

Before configure module, set some global parameters,

Set bit[7:6] of 0x8b00_0070 to select LCD clock source;

Set bit[2:0] of 0x8b00_0060 to control the divider value of LCD clock;

Set bit[3] of 0x2090_0200 to enable LCD clock;

Set or reset bit[3] of 0x2090_0210 to reset LCDC module;

Set bit[29] of 0x8000_3008 to enable LCDC global interrupt.

Display mode

- Clear ARM interrupt and LCDC module interrupt, and enable them;
- Enable LCDC, set the bit 0 of LCDC_CTRL to '1';
- Configure layer information, includes format, size, position, address, etc;

- Configure LCM parameters;
- Start LCDC, write '1' to bit[3] of LCDC_CTRL;
- Wait LCDC_DONE interrupt for completing a frame;
- Re-configure parameters, and start a new frame;

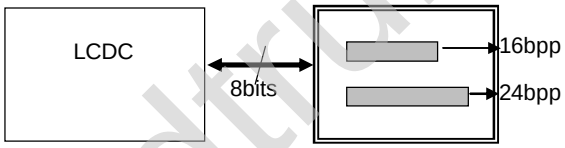
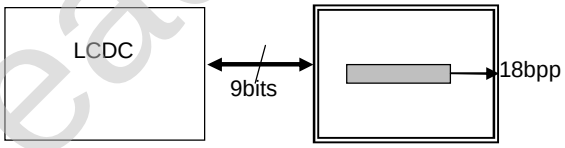
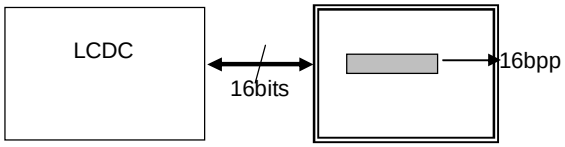
Capture mode

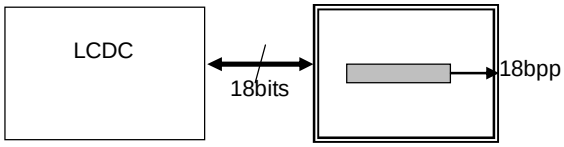
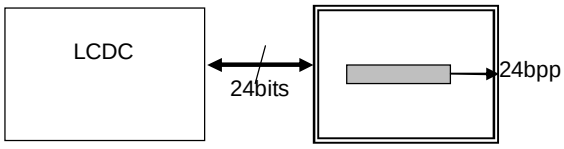
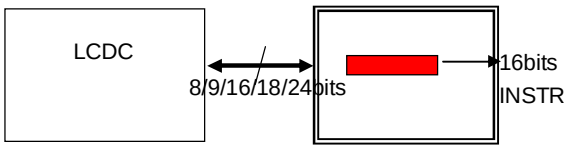
- Clear ARM interrupt and LCDC module interrupt, and enable them;
- Enable LCDC, set the bit 0 of LCDC_CTRL to '1';
- Configure layer information, includes format, size, position, address, etc;
- Enable capture, set the bit[0] of CAP_CTRL to '1';
- Start LCDC, write '1' to bit[3] of LCDC_CTRL;
- Wait LCDC_DONE interrupt for completing a frame;
- Re-configure parameters, and start a new frame;

7.3.6.2 Program Notes

- All address configure all are 8bits byte unit;
- All size or position configure all are pixel unit;
- Image and OSD source data must be with word-aligned pitch;
- When fetched image is YUV data, the position and size of image layer must be even;

Normal IF_BITS and PIX_BITS list

	8bits interface supports 16bits pixel or 24bits pixel panel, it needs 2 or 3 send.
	9bits interface supports 18bits pixel panel, it needs 2 send.
	16bits interface supports 16bits pixel panel, it only needs 1 send.

	18bits interface supports 18bits pixel panel, it only needs 1 send.
	24bits interface supports 24bits pixel panel, it only needs 1 send.
	Instruction can be look as a special pixel, it is 16bits normally, it is set by AHB channel, it can match all kinds if interface width.

7.4 Graphics

7.4.1 Overview

The Mali-300 GPU is a hardware accelerator for 2D and 3D graphics systems.

The GPU consists of:

• a Pixel Processor (PP)

• a Geometry Processor (GP)

• a Level 2 Cache Controller (L2)

• a Memory Management Unit (MMU) for each GP and PP included in the GPU

• a Power Management Unit (PMU).

7.4.2 Pixel processor features

The pixel processor features are:

• programmable fragment shader

• alpha blending

• complete non-power-of-2 texture support

• cube mapping

• fast dynamic branching

• fast trigonometric functions, including arctangent

• full floating-point arithmetic

• framebuffer blend with destination Alpha

• indexable texture samplers

• line, quad, triangle and point sprites

• no limit on program length

• perspective correct texturing

• point sampling, bilinear, and trilinear filtering

• programmable mipmap level-of-detail biasing and replacement

• stencil buffering, 8-bit

• two-sided stencil

• unlimited dependent texture reads

• 4-level hierarchical Z and stencil operations

• Up to 512 times *Full Scene Anti-Aliasing* (FSAA). 4x multisampling times 128x supersampling

• 4-bit per texel compressed texture format.

7.4.3 Geometry processor features

The geometry processor features are:

• programmable vertex shader

• flexible input and output formats

• autonomous operation tile list generation

• indexed and non-indexed geometry input

• primitive constructions with points, lines, triangles and quads.

7.4.4 Level 2 cache controller features

The L2 cache controller features are:

• size is 8KB

• 4-way set-associative

• supports up to 32 outstanding AXI transactions

• implements a standard pseudo-LRU algorithm

• cache line and line fill burst size is 64 bytes

• supports eight to 64bytes uncached read bursts and write bursts

• 64-bit or 128-bit interface to memory sub-system

• support for hit-under-miss and miss-under-miss with the only limitation of AXI ordering rules.

7.4.5 MMU

The MMU features are:

• accesses control registers through the bus infrastructure to configure the memory system.

• each processor has its own MMU to control and translate memory accesses that the GPU initiates.

7.4.6 PMU

The PMU features are:

• programmable power management

• powers up and down the GP, PP and Level 2 cache controller separately

• controls the clock, isolation and power of each device

• provides an interrupt when all requested devices are powered up.

8 Audio Subsystem

8.1 Overview

The audio subsystem is shown in Figure 8-1. It is a mixed mode system that includes both digital and analog components, and can facilitate audio or voice functions. Essentially, the system consists of one uplink Analog to Digital Converter (ADC) channel, two downlink Digital to Analog Converter (DAC) channels, and some additional function circuitry. Both ARM and DSP can control the audio subsystem separately.

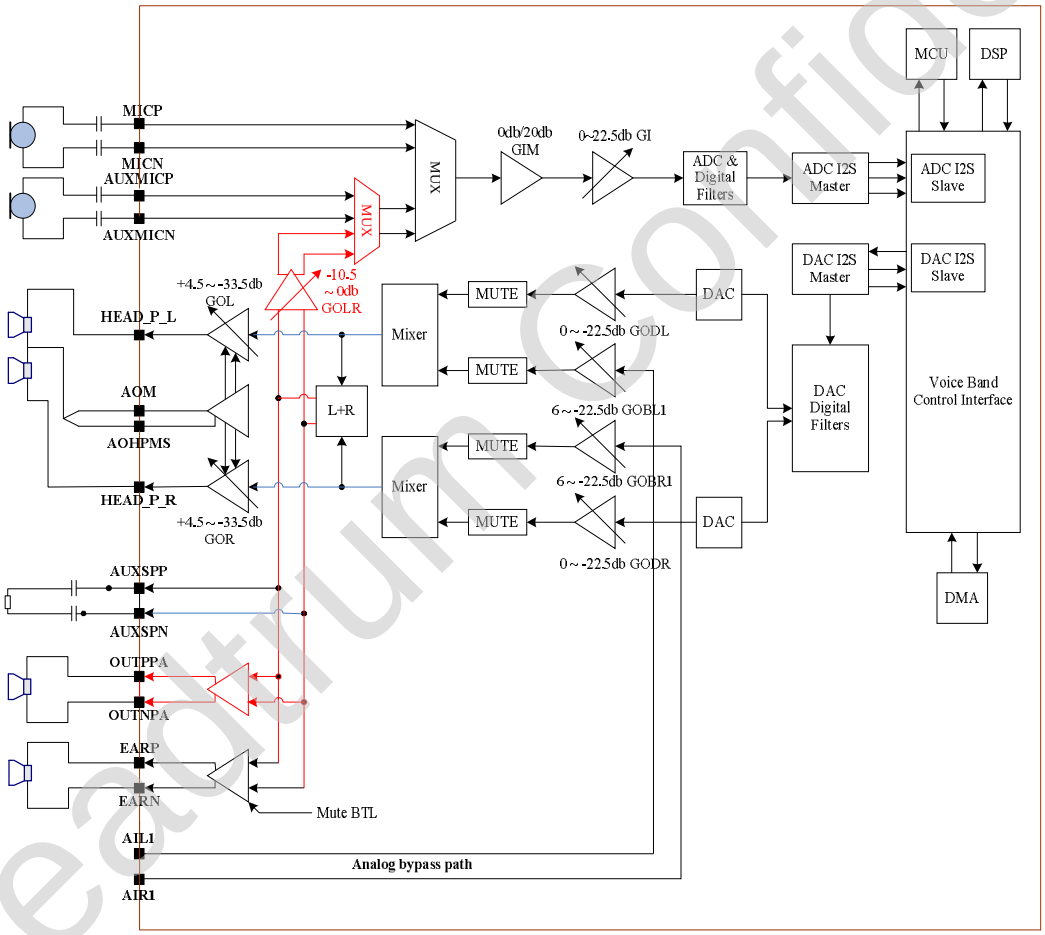


Figure 8-1 Audio subsystem architecture

The mono ADC channel receives signal from an external microphone, converts the analog signal into digital data, and transfers the data to buffers in voice band control (VBC) interface, and finally the data in the buffers will be fetched by software.

The stereo DAC data path is just the opposite of the ADC channel. Software loads voice or audio data into buffers in voice band control interface, and then the data will be converted to analog signals by DAC. Through a mixer that also achieves a low pass filter function, three outputs are supplied: a headphone output for each DAC channel, a differential line output for combined signal of left and right channels, and a BTL output also for combined signal of left and right channels.

An analog line input path (analog bypass path marked in Figure 8-1) is provided. The line-in signals from AIL1 and AIR1 also input to the mixers. The mixers allow signal from either DAC or line-in passing through. Signals output from the mixers goes to three paths, which has been described above.

The line-in recording function is also supported. The line-out signals from PAD AUXSPP/AUXSPN pass through a PGA, a MUX circuit and then into the PAD AUXMICP/AUXMICN, as the input of the ADC channel.

The voice band control (VBC) interface communicates with software or DMA, and this block contains ping-pong buffers for each channel, control registers for the entire audio subsystem, APB bus for ARM, Z bus for DSP, interrupt control, DAI test interface and DMA interface control logic.

Except the VBC interface, all the other parts of the system together constitute the audio codec. Main clock (MCLK) and global reset of audio codec are generated from top-level clock and reset management logic.

Two groups of I2S serial interface connect ADC/DAC of the audio codec with the VBC interface, one is for ADC channel, and the other is for DAC channel. The VBC interface is always the slave, and the audio codec part is the master.

8.2 Features

The audio sub-system provides the following features.

- Mono ADC channel and stereo DAC channels
- Programmable sampling frequency (Fs): 8, 9.6, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, or 96 kHz
- Two differential microphone input with a 0 or 20 dB boost gain stage
- Stereo programmable gain amplifier for headphone output
- Differential line output
- Differential BTL output
- Stereo analog line input
- Stereo analog mixer with programmable gains to select signals coming from the DAC and the analog line-in input
- Support line-in recording
- Internal voltage reference (resistive potential divider) to generate all required internal voltages
- Both ARM and DSP can control the audio subsystem independently, and they are able to access the same control registers
- DMA hard channel provided in ARM control mode
- Audio codec main clock frequency is 12 MHz
- Audio codec and VBC interface can be separately soft reset
- Independent interrupt for ADC and DAC channels
- External I2S interface is provided and can be connected with the audio codec

8.3 Audio Codec Path Details

8.3.1 ADC Path

Two pairs of differential microphone input pads are provided: MICP/MICN, AUXMICP/AUXMICN, and it is configurable which pair is enabled. The differential analog signals are applied through capacitors that remove DC voltage, which allows a more flexible usage by removing the constraint of a specific input common mode voltage.

The ADC path in the audio codec includes:

- A switchable microphone amplifier
- A programmable (4bits) gain amplifier (PGATM)
- A delta-sigma modulator
- A set of digital decimating filters
- An optional high pass filter

The microphone amplifier is switchable with a 0 or 20 dB gain, and the PGATM provides a gain ranges from 0 dB to 22.5 dB with 1.5 dB steps that allows covering a wide range of input levels.

The delta-sigma modulator and the decimating filters belong to the ADC function block. Figure 8-2 shows the ADC block diagram. The Δ-Σ modulator is the analog part, while the decimating filter and the high pass filter form the digital part.

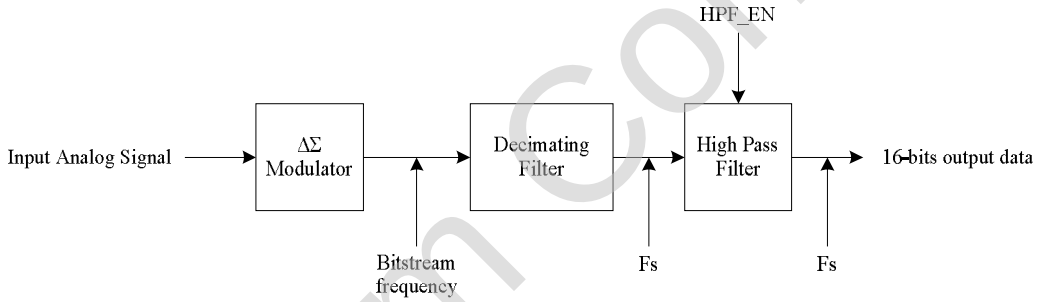


Figure 8-2 ADC function block diagram

The Δ-Σ modulator converts the input amplified analog signal into a succession of 0/1 bit stream. This bit stream is sent to the decimating filters that transform it into a 16 bit signal at the selected Fs frequency. Finally, an optional high pass filter removes the DC component. By IIS serial interface, the output data is sent to the ping-pong buffers in VBC digital interface. Once receiving the ADC interrupt that indicates one buffer is full, ARM or DSP or DMA will read the data out.

Tables 8-1 and 8-2 give the decimating filter and high pass filter characteristics.

Table 8-1 The decimating filter characteristics

For Fs ≤ 48 kHz

Filter characteristics	Min.	Typ.	Max.	Unit
Stop band	0.545Fs (TBC)			Hz
Stop band attenuation	-80 (TBC)			dB
Pass band			0.455Fs (TBC)	Hz
Pass band ripple			+/- 0.05 (TBC)	dB

For Fs = 96 kHz

Filter characteristics	Min.	Typ.	Max.	Unit
Stop band	0.545Fs (TBC)			Hz
Stop band attenuation	-80 (TBC)			dB
Pass band			0.288Fs (TBC)	Hz
Pass band ripple			+/- 0.05 (TBC)	dB

Table 8-2 The high pass filter characteristics (for Fs = 44.1 kHz)

High Pass Filter corner frequency	-0.1dB	24Hz
	-0.5dB	10.5Hz
	-3dB	3.8Hz

8.3.2 DAC Path

The stereo DAC path contains two parallel channels. For each channel, data path function blocks include:

- Optional de-emphasis filter
- Cascaded interpolating filters
- The noise shaper
- The switched capacitor low pass filter (reconstruction filter)
- The output path (headphone output amplifier, line out amplifier, or BTL amplifier)

For the downlink channels, software first loads data into buffers in VBC at the beginning or after receiving interrupt that indicates the data in the ping-pong buffer has been moved out to DAC of

audio codec. The 16-bit data are applied to the input of interpolating filters, followed by a noise shaper to be transformed into a bit stream.

The audio codec DAC function block diagram is shown in Figure 8-3. The digital part includes the optional de-emphasis filter, the cascaded interpolation filters, and the noise shaper. The other part is analog blocks.

A de-emphasis filter is implemented in the input of the DAC path. This enables compatibility with old audio CD records. Due to this, the filter coefficients are fitted to work when Fs = 44.1 kHz. This filter is activated when DEEMPH (ARM 0x8200_3108 or DSP 0xBA42 bit [7]) is set to '1'.

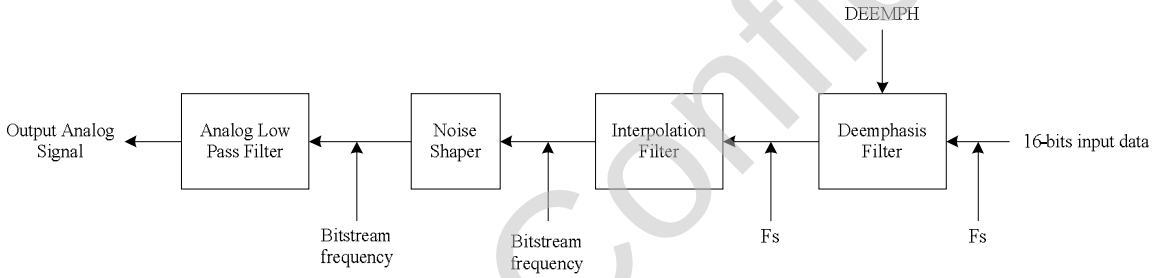


Figure 8-3 DAC function block diagram

The analog part is a switched capacitor low pass filter (reconstruction filter), followed by a continuous time low pass filter which is achieved by the mixer. In addition, before the mixer a PGA is available, this provides programmable attenuation range from 0 dB to -22.5 dB with 1.5 dB steps through a 4-bit word. They allow filtering the out-of-band quantization noise introduced by the digital noise shaper.

Table 8-3 shows the interpolation filter characteristics

Table 8-3 The interpolation filter characteristics

For Fs ≤ 48 kHz

Filter characteristics	Min.	Typ.	Max.	Unit
Stop band	0.545Fs (TBC)			Hz

Stop band attenuation	-90 (TBC)			dB
Pass band			0.455Fs (TBC)	Hz
Pass band ripple			+/- 0.05 (TBC)	dB

For Fs = 96 kHz

Filter characteristics	Min.	Typ.	Max.	Unit
Stop band	0.545Fs (TBC)			Hz
Stop band attenuation	-90 (TBC)			dB
Pass band			0.288Fs (TBC)	Hz
Pass band ripple			+/- 0.05 (TBC)	dB

The output signal from the mixer goes to three ends: headphone output through pads HEAD_P_L and HEAD_P_R, differential line output through pads AUXSPP and AUXSPN, and BTL output through pads EARP and EARN. The following section “Output Branch Description” gives a detailed explanation.

8.3.3 Analog Line-in Path

The analog line-in path, or analog bypass path, is provided for additional applications (for example, FM radio), and includes the Line input buffer, the Mixer, and the output path (headphone output amplifier, line out amplifier, or BTL amplifier).

Analog signal from pads AIL1 (left channel) and AIR1 (right channel) directly input to the two mixers through line input buffers, and the output signal from the mixers pass through three branch and also arrive to three ends.

8.3.4 Mixer Path

Besides allowing a single path (either the DAC output signal or the analog line-in signal) passing through, the Mixers also allow select the signals from the two inputs.

Before inputting to the Mixer, a PGA is used for both paths. For the line-in path, the programmable gain/attenuation range varies from +6 dB to –22.5 dB with 1.5 dB steps through a 5-bit word. For the DAC path, the programmable attenuation range varies from 0 dB to –22.5 dB with 1.5 dB steps through a 4-bit word.

8.3.5 Output Branch Description

The signal output from the Mixer is applied to:

- A headphone output amplifier (PGAT) to drive a low impedance load (down to 16 Ohm) through an external bypass capacitor. This stage allows a programmable gain/attenuation range from +4.5 dB to -33.5 dB with a variable step through a 5-bit word
- A differential line output amplifier to drive a minimum of 10 kOhm load
- A BTL (Bridge Tied Load) driver through the line output amplifier in order to provide 240 mW on an 8 Ohm load

Two mute signals allow suppressing the output signal while the DAC and LPF are still working on mixer and BTL stages.

Note: The headphone output stage is configurable, 3-wire capacitor-less headphone output or 2-wire with bypass capacitors output can be selected by user.

8.4 I2S Serial Interface

8.4.1 General Features

There are two groups of I2S interface signals between the audio codec and the VBC block, one group is for the mono ADC channel, and the other is for the stereo DAC channels. I2S serial communication is performed via three one-bit signals: a clock signal, a data signal and a synchronization signal.

The two groups of I2S serial interface signals are defined as in Table 8-4.

Table 8-4 I2S interface list

Interface Name	Descriptions
ADC_BCLK	ADC bit clock signal
ADC_LRO	ADC synchronization signal
ADC_SDATA	ADC data signal
DAC_BCLK	DAC bit clock signal
DAC_LRO	DAC synchronization signal
DAC_SDATA	DAC data signal

a) **Master and Slave** Audio Codec is the master of the serial interface, meaning that the audio codec initiates data transmission. For the ADC channel, the three signals ADC_BCLK, ADC_LRO, ADC_SDATA are all output from audio codec to VBC interface. For the DAC channel, DAC_BCLK and DAC_LRO are output from audio codec to VBC interface, and DAC_SDATA, which is generated on DAC_BCLK and DAC_LRO by VBC interface, is output from VBC interface to audio codec.

b) **Synchronization** For the ADC channel, ADC_LRO and ADC_SDATA are generated on ADC_BCLK falling edge by the audio codec, and to ensure a data transmission robust to setup/hold requirements, VBC interface samples ADC_SDATA on the rising edge of ADC_BCLK. On the other hand, for the DAC channels, DAC_LRO is generated on DAC_BCLK falling edge by the audio codec, so VBC interface also generates DAC_SDATA on DAC_BCLK falling edge, and the audio codec samples DAC_SDATA on DAC_BCLK rising edge.

c) **Frequency Relationship** The audio codec MCLK (Main Clock) frequency is equal to 12 MHz, and for different audio sampling frequency, Fs, the frequency of BCLK is different. The mean frequency of LRO is equal to Fs, but the delay between two LRO may vary (one BCLK cycle difference max) when Ts (= 1/Fs) is not an integer multiple of MCLK period. For instance, if Fs = 44.1 kHz and BCLK frequency is equal to 3 MHz, the mean LRO period is equal to 68.02721... BCLK periods, and so the number of BCLK cycles between two LRO high-levels varies between 68 and 69. Table 7-5 describes the relation between MCLK, Fs and BCLK frequency.

Table 8-5 The relation between MCLK, Fs and BCLK frequency

MCLK (MHz)	Fs (kHz)	MCLK/BCLK frequency ratio	BCLK/Fs frequency ratio	BCLK frequency (kHz)
12	8	24	62.5	500
12	9.6	20	62.5	600
12	11.025	16	68.0272109	750
12	12	16	62.5	750
12	16	12	62.5	1000
12	22.05	8	68.0272109	1500
12	24	8	62.5	1500
12	32	6	62.5	2000
12	44.1	4	68.0272109	3000
12	48	4	62.5	3000
12	96	2	62.5	6000

The serial interfaces can work in two modes: DSP mode or I2S mode. The mode is selected through the VB_AICR register described in Section 8.6. The following two sections describe the two serial interface modes in detail.

8.4.2 DSP Mode Timing

In DSP mode, DAC_LRO or ADC_LRO signal is a one DAC_BCLK or ADC_BCLK cycle high-level pulse. DAC_SDATA or ADC SDATA transmission has to start one BCLK cycle after LRO rising edge, left channel first, from MSB to LSB, then right channel, from MSB to LSB. There is no delay between left and right channel transmission, so word length (16 bits data width) must be taken into account when transmitting or receiving data. The ADC is mono channel, the same data are sent twice in each cycle. The following two figures show the timing of the DSP interface modes.

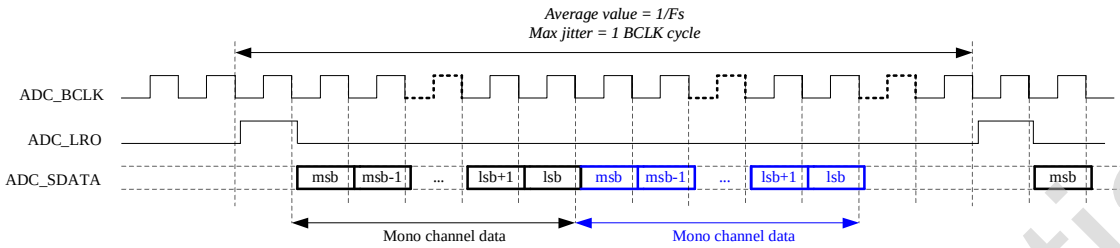


Figure 8-4 ADC serial interface timing in DSP mode

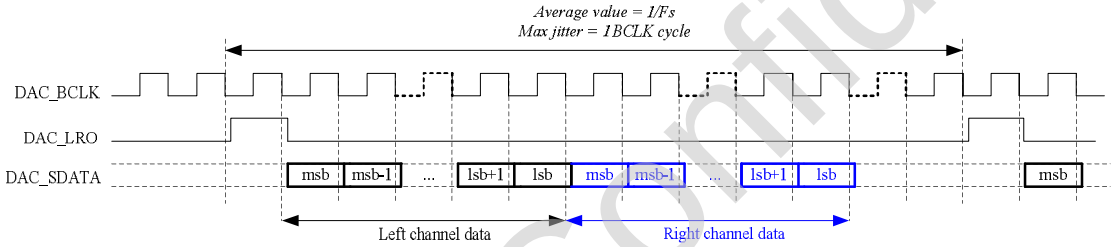


Figure 8-5 DAC serial interface timing in DSP mode

8.4.3 I2S Mode Timing

In I2S mode, DAC_LRO or ADC_LRO signal high-level duration is 32 BCLK cycles, and low-level duration is the remaining BCLK cycles, that is, LRO period in BCLK of the current LRO cycle minus 32. Therefore, duty cycle of LRO is different from 50%. DAC or ADC SDATA transmission has to start one BCLK cycle after LRO edge.

For DAC channels, right channel data are sent after the LRO rising edge, MSB first. Left channel data are sent after the LRO falling edge, MSB first. The ADC is mono channel, and the same data are sent twice in each cycle. Depending on data word length (16 bits supported only), SDATA is filled with '0' until next channel transmission. The following two figures show the timing of the I2S interface modes.

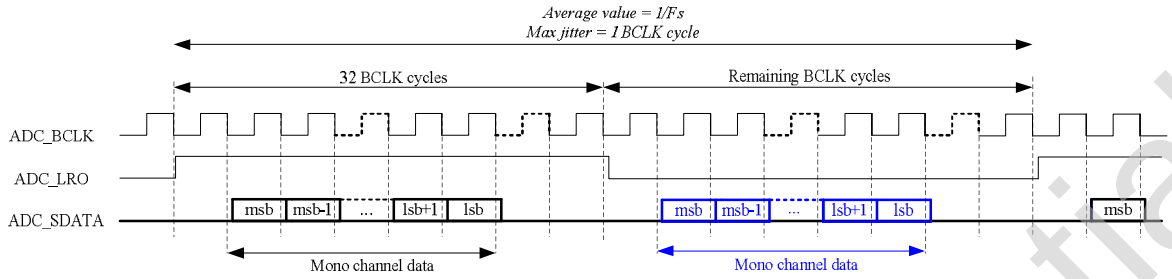


Figure 8-6 ADC serial interface timing in I2S mode

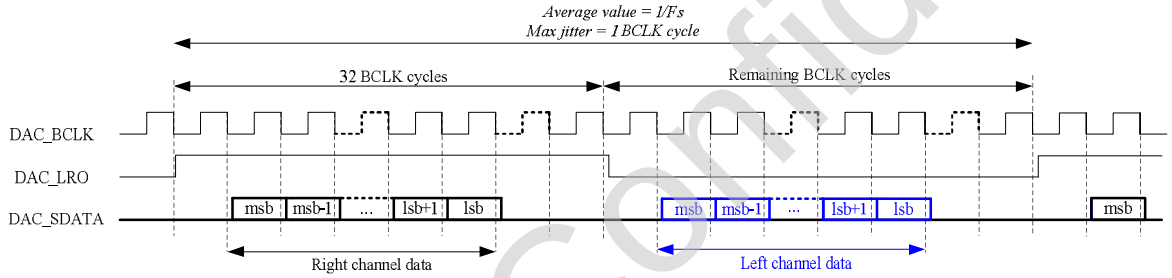


Figure 8-7 DAC serial interface timing in I2S mode

8.5 VBC Interface

8.5.1 Overview

The VBC module is designed as a digital interface, for software control and data handling with Audio Codec. Digital high-pass IIR filters, digital gain, side tone module and loop path are also implemented in VBC for special applications.

8.5.2 Features

- Both ARM and DSP can control Voice Band independently, so both APB bus and DSP Z bus are included in VBC module. They are able to access the same VB control registers
- Support two ADC channels: ADC0 and ADC1(one is reserved)
- Support two DAC channels: DAC0 and DAC1
- Two slave IIS/PCM serial interface for ADC/DAC data
- 2 320x16 SRAM are used as ADC ping-pong buffer, in which address 0~159 is for ADC0, and address 160~319 is for ADC1
- 2 320x16 SRAM are used as DAC0, DAC1 ping-pong buffer, in which address 0~159 is for DAC0, and address 160~319 is for DAC1
- Max buffer size of 4 channels supported is 160
- Support DMA access in ARM control mode
- DAC serial 6th-order IIR filter sections are designed for application such as high-pass filter and EQ
- DAC auto-level control(ALC) is supported
- DAC digital gain is supported
- DAC output limit is supported
- DAC output can be selected as 16 bits or 24 bits
- ADC digital gain is supported
- Side tone is supported
- ADC input signal can be sent to DAC through side tone
- DAC output signal can be loop to ADC
- External IIS serial data can be selected as ADC input
- ADC interrupt to software if one ADC buffer is full
- DAC interrupt to software if one DAC buffer is empty

8.5.3 Signal Description

8.5.4 Function Description

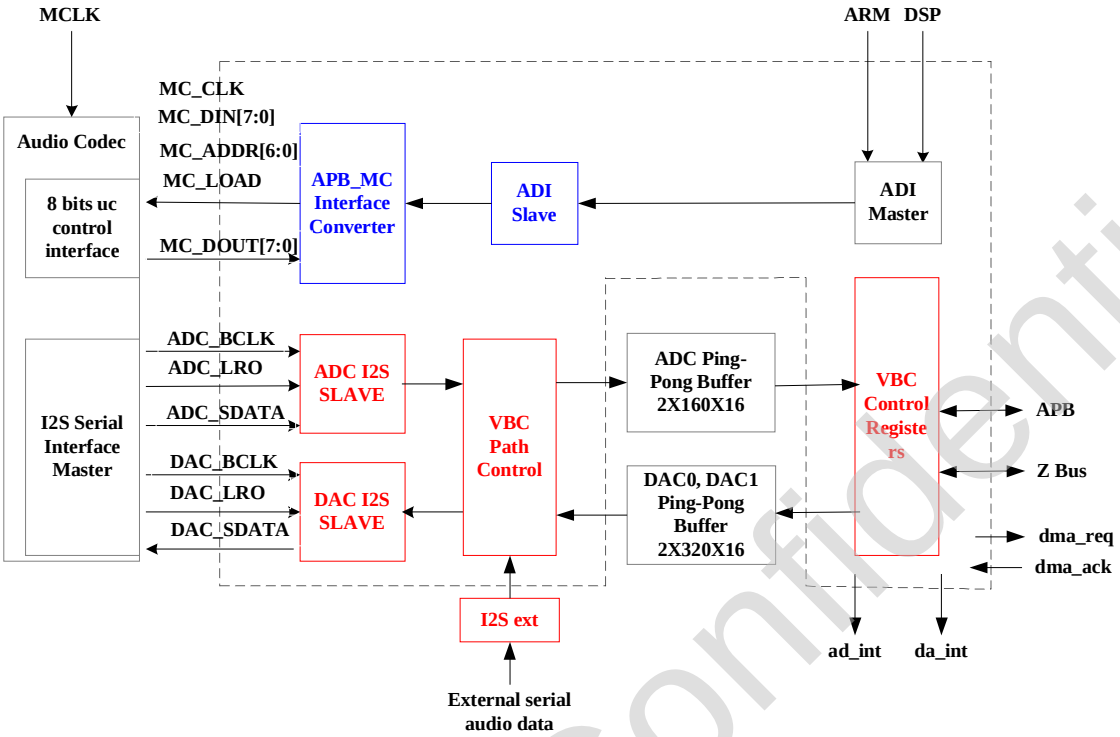


Figure 8-8 Voice Band Digital Interface

In the figure, the red parts belong to VBC module, and the blue part, which converts APB bus to uC bus.

Audio Codec digital interface includes clocks, serial audio interface and control interface. MCLK are generated from clock managing block in the top level of the chip. IIS/PCM serial interface transfer audio data between Codec and 160-word data ping-pong buffer. APB-MC interface converter, together with the ADI interface, work as a data bridge between APB/Z-bus and 8-bit uC interface.

Both ARM and DSP can control Voice Band independently. They are able to access the same VB control register, and control the data interrupt frequency. Through ARM and DSP register, four Voice paths ADC0,ADC1, DAC0, DAC1 can be shut down at different time, VB register access clock can also be shut down. Interrupt will be sent to ARM/DSP after the data in the ping-pong buffer is full for ADC channel, or empty for DAC channel.

In ARM global register 0x8B00_0044, a 1-bit control register “arm_vb_acc” is used to select ARM or DSP control voice band. Default value is 0, allowing DSP controlling.

If ARM controlling is selected, a DMA hardware channel is provided for ADC and DAC respectively. Instead of interrupt, DMA request will be sent to DMA after the data in the ping-pong buffer is full for ADC channel, or empty for DAC channel.

8.5.4.1 Path Control and Function Module

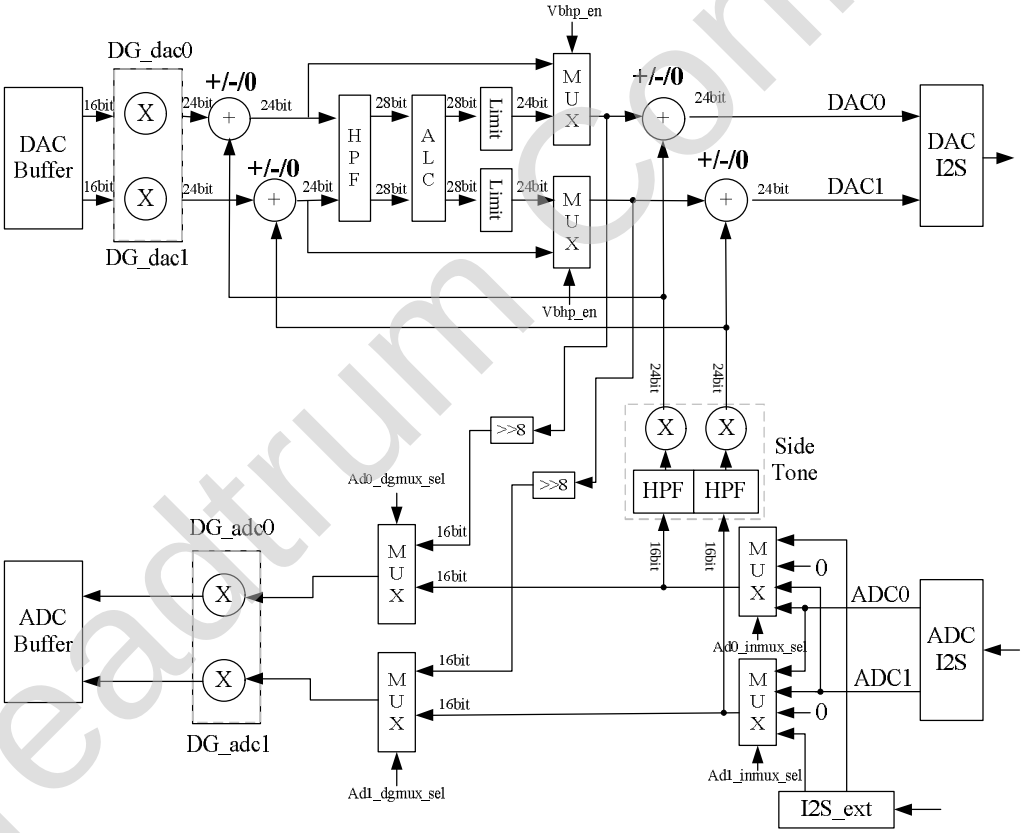


Figure 8-9 VBC Path Control

The above figure describes all VBC data flow paths. Except the direct DAC and ADC paths, several loop paths are added for different application.

- ADC loop to DAC

  Side tone module is implemented between ADC and DAC path, and through the side tone module, ADC data can loop to DAC, either to the input of DAC HPF, or output of DAC channel, added or subtracted by the DAC data.

- DAC loop to ADC

  The output of DAC can also loop to ADC path, after right shifting 8 bits and into the ADC digital gain module

The input data of each ADC channel can be selected between the two input channel, and also an external-chip input is also designed, which is useful when external audio signal is needed to be processed.

A digital gain is implemented for each DAC and ADC channel, and the gain coefficient DG[6:0] is parsed as follows..

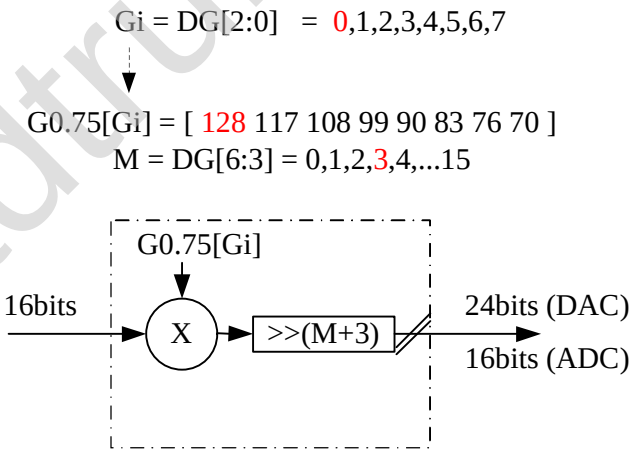


Figure 8-10 VBC Digital Gain

The 6th-order IIR high-pass filter is showed in the following figure. The filter is grouped into 3 parts. Each part is a 2nd-order IIR, and implemented in one module, named vbhp_s01.v, vbhp_s23.v and vbhp_45.v. In each 2nd-order IIR, DAC0 and DAC1 share the hardware, so after a valid-in signal, the DAC0 data are processed first, and then the DAC1 data are processed. After DAC1 data processing finishes, the valid-out signal is generated.

All the data during IIR processing are 34bits. The input 16bits data are left shifted 16bits and extended 2 bits to be 34bits, and the output data are 28bits for ALC module processing.

As for the ALC module, please refer to the document “SC6820 VBC_ALC Design Specification”.

The 8bits hp_limit control register is for the output limit logic. The output signal also can be limited to an expected value, and the value is hp_limit[7:0]<<16+16’hFFFF.

Note 1: The input 16bit data of the 6-band IIR are left shifted 16bits and then extended to be 34bits, but the output 34bits data from the 6-band IIR are first right shifted 6 bits to be 28bits, pass through ALC, clipped to 24bits, and then right shifted 8 bits after the limiter to be 16bits.

Note2: Since the input data is 16bits left shifted, and the output data are 6+8=14bit right shifted, if the digital gain and the 6-band IIR are both configured to be bypass-state, the output of DAC is 4-times amplified.

Note3: If the 6-band IIR is enabled, the following configuration of the 43 HPCOEF registers is corresponding to the bypass-state of the 6-band IIR

HPCOEF0: ‘h1000 HPCOEF1: ‘h4000 HPCOEF2: ’h4000

HPCOEF3: ’h0000 HPCOEF4: ’h0000 HPCOEF5: ’h0000 HPCOEF6: ’h0000

HPCOEF7: ’h1000 HPCOEF8: ’h4000 HPCOEF9: ’h4000

HPCOEF10: ’h0000 HPCOEF11: ’h0000 HPCOEF12: ’h0000 HPCOEF13: ’h0000

HPCOEF14: ’h1000 HPCOEF15: ’h4000 HPCOEF16: ’h4000

HPCOEF17: ’h0000 HPCOEF18: ’h0000 HPCOEF19: ’h0000 HPCOEF20: ’h0000

HPCOEF21: 'h1000 HPCOEF22: 'h4000 HPCOEF23: 'h4000
HPCOEF24: 'h0000 HPCOEF25: 'h0000 HPCOEF26: 'h0000 HPCOEF27: 'h0000

HPCOEF28: 'h1000 HPCOEF29: 'h4000 HPCOEF30: 'h4000
HPCOEF31: 'h0000 HPCOEF32: 'h0000 HPCOEF33: 'h0000 HPCOEF34: 'h0000

HPCOEF35: 'h1000 HPCOEF36: 'h4000 HPCOEF37: 'h4000
HPCOEF38: 'h0000 HPCOEF39: 'h0000 HPCOEF40: 'h0000 HPCOEF41: 'h0000

HPCOEF42: 'h1000

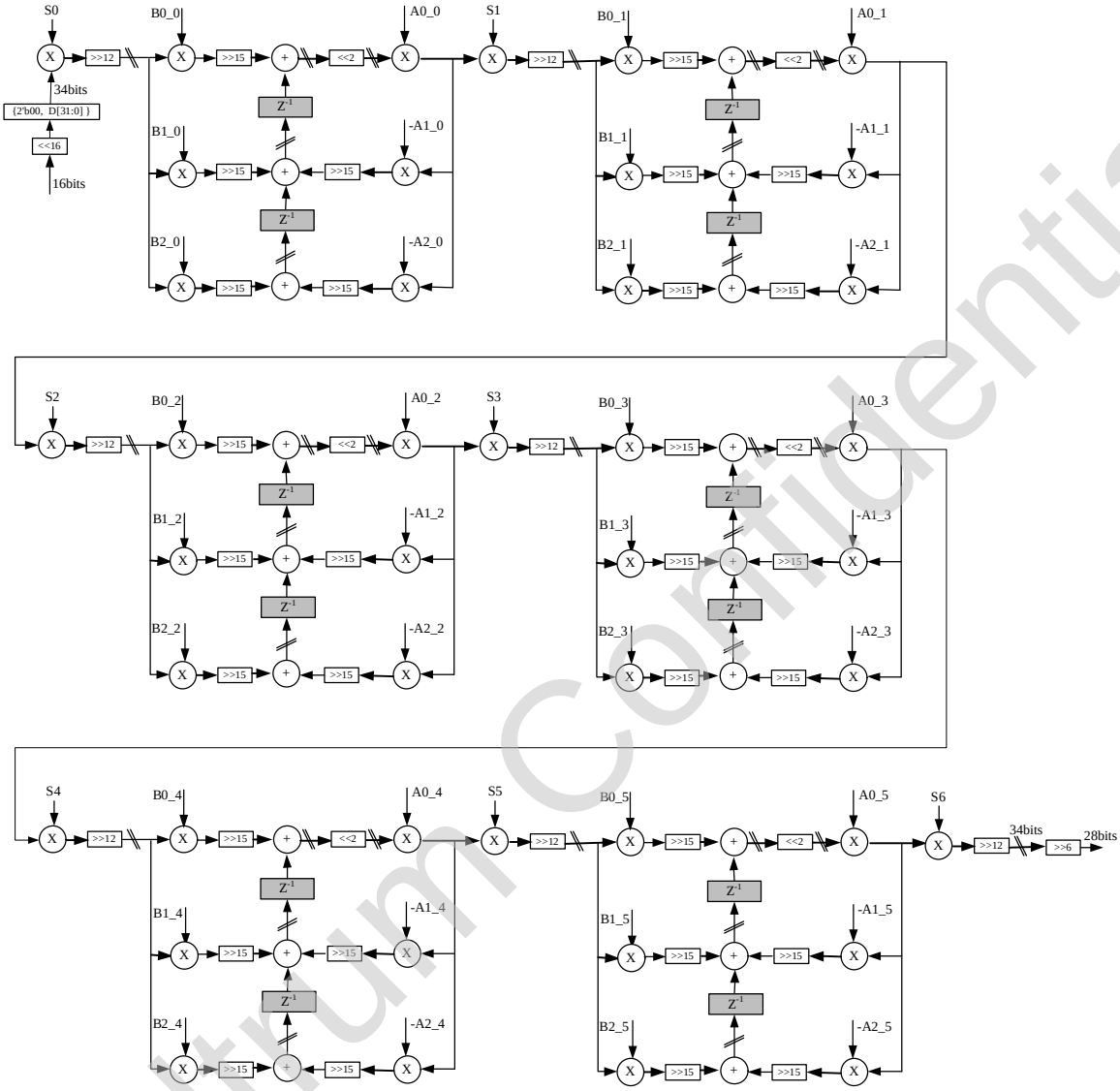


Figure 8-11 VBC 6-order DAC IIR filter

The side tone module includes a high-pass filter and a digital gain. The coefficient N[3:0] of the high-pass filter should be configured by software. The digital gain of side tone is the same with the DAC and ADC channel digital gain.

$$h(z) = (1 - 1>>(N+1)) \frac{1 - Z^{-1}}{1 - (1-1>>N) Z^{-1}}$$

Gi = DG[2:0] = 0,1,2,3,4,5,6,7

G0.75[Gi] = [128 117 108 99 90 83 76 70]

M = DG[6:3] = 0,1,2,3,4,...15

N = HPF[3:0] = 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15

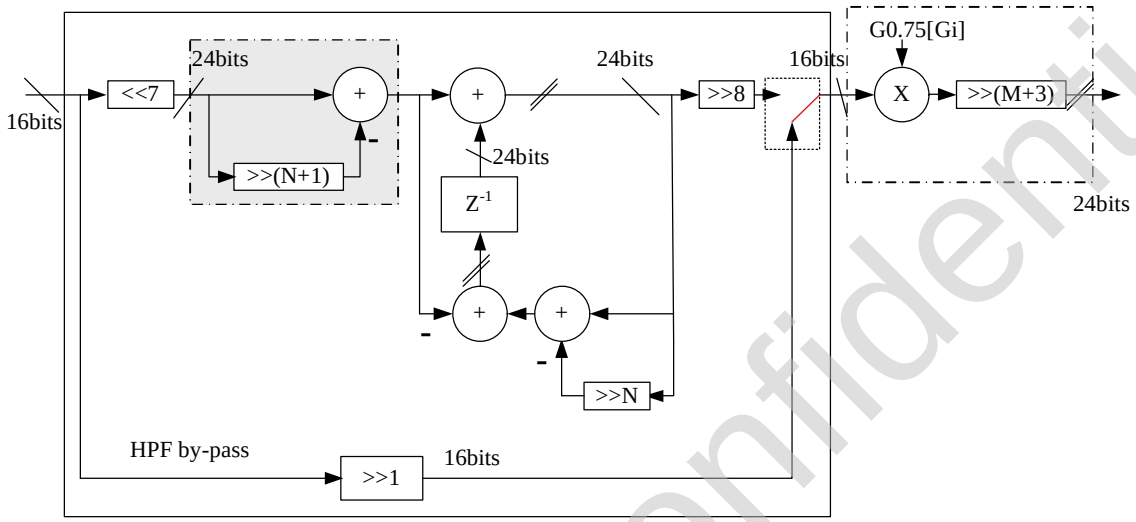


Figure 8-12 VBC Side Tone

8.5.4.2 Clock Domain

Clock for ADC/DAC I2S slave interface and data buffer can be shut down independently. Totally four clocks input to voice band interface:

- ADC_BCLK for ADC I2S Slave block, ADC digital gain and ADC data buffer. Control signal: vb_ad0on and vb_ad1on. If ARM controlling voice band, the two control bits are located in global control register 0x8B00_0044 bit[5:4]. If DSP controlling voice band, the two control bits are located in STC(system timing and controls) control register 0x0064_0294 bit[6:5].
- DAC_BCLK for DAC I2S Slave block, DAC digital gain, DAC high pass filter and DAC data buffer. Control signal: vb_da0on and vb_da1on. If ARM controlling voice band, the two control bits are located in global control register 0x8B00_044 bit[4:3]. If DSP controlling voice band, the two control bits are located in STC(system timing and controls) control register FORCE_PD bit[8:7] .
- APB clock or Z bus clock for ADC,DAC data buffer, selected by arm_vb_acc, global control register 0x8B00_0044 bit[7] .
- .CLK_12M for Audio Codec main clock.

8.5.4.3 I2S Slave Interface

The I2S slave interface receives serial ADC data under the control of ADC_BCLK and ADC_LRO, which are generated by audio codec I2S master interface, and sends serial DAC data under the control of DAC_BCLK and DAC_LRO, which are also generated by audio codec I2S master interface.

8.5.4.4 Audio Codec control Interface

For the control registers located in audio codec, ARM or DSP access them through an 8-bit parallel µC interface. The 8-bit parallel µC interfaces are synchronized to MC_CLK. The other control signals, MC_ADDR, MC_LOAD and MC_DIN, are supposed to be generated on MC_CLK rising edge.

To read registers in the audio codec, ARM/DSP sends a read operation through the ADI interface, and the APB-MC bridge generates MC_ADDR, to the Audio Codec, then the Audio Codec outputs MC_DOUT data after a Tread delay. MC_DOUT can be sampled by the APB-MC bridge just after the Tread delay time (sure on the next rising edge of MC_CLK). MC_DOUT will be sent to ARM/DSP through the ADI interface after word length expanded to 16 bits.

To write registers in the audio codec, ARM/DSP sends a write operation through the ADI interface, and the APB-MC bridge generates MC_ADDR, MC_LOAD and the input data MC_DIN on the MC_CLK rising edge. MC_DIN is sampled by the Codec on the next MC_CLK rising edge.

The following two figures show the read and write timing of the 8-bit parallel µC interfaces.

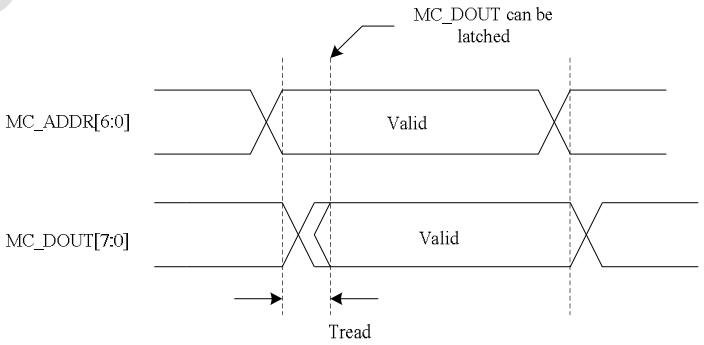


Figure 8-13 Parallel µC Interface Register Read Timing

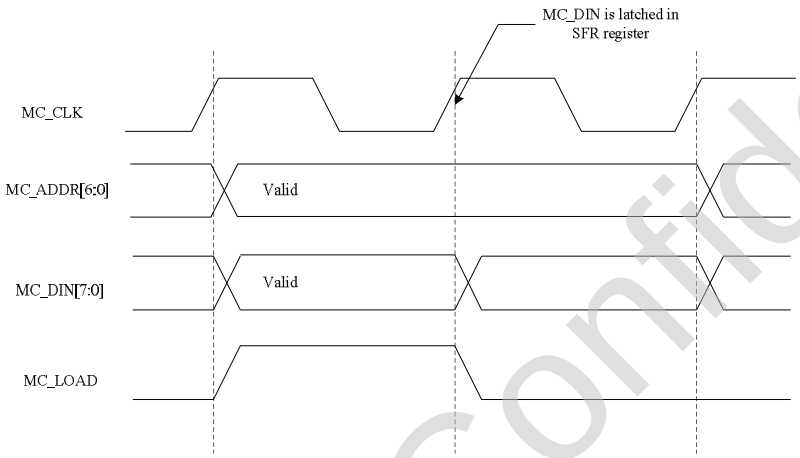


Figure 8-14 Parallel µC Interface Register Write Timing

8.5.4.5 Digital Audio Data Buffer

Two 160x16 bit SRAM work as ping-pong buffers for each channel. The 4 160x16 SRAM for DAC0 and DAC1 ping-pong buffers are combined to 2 320 x 16 SRAM. The address 0 ~ 159 in each SRAM is DAC0 ping-pong buffer, and the address 160~319 in each SRAM is DAC1 ping-pong buffer. It's the same for ADC0 and ADC1 ping-pong buffer.

Received voice data are read out from ADC0 and ADC1 data buffer by software, and data for transmit are sent to DAC0, DAC1 data buffer also by software. Buffer size is programmable from 1 to 160 words. ADC interrupt(shared by ADC0 and ADC1) will be generated when ADC data buffer is full (written by hardware), and DAC interrupt (shared by DAC0 and DAC1) will be generated when DAC data buffer is empty (read by hardware). Voice interrupt frequency can be calculated from the buffer size. For example: when playing voice at 8 kHz sampling rate, buffer size is 160 words, the interval between two interrupt is: 125 us x 160 = 20 ms.

If DAC and ADC buffer sizes are the same, after voice band is enabled, the buffer size is not changed, two interrupts should be synchronized (within one voice sample duration), either one can be used as buffer full/empty interrupt.

Address counter for each path will be reset to zero after interrupt is generated or at VBENABLE register (0xBB06 bit 15) changing from low to high.

8.5.5 Control Registers

8.5.5.1 Memory map

DSP side base address: 0x0063_0000

DSP controls the Voice Band Controller (VBC) by default.

ARM side base address: 0x8200_3000/0x1063_0000

From the ARM side, please set 0x8B00_0044 bit[7] = 1'b1, to enable ARM access to VB

Note:

- ARM can access Voice Band Codec module either through **APB space**, at base address 32'h8200_3000 or through **AHB space** (from ARM matrix to DSP matrix), at base address 32'h1063_0000.
- For all Voice Band Codec registers through AHB space, please use half-word access; byte, word, or double-word accessing is forbidden. If access through APB space, only word access is permitted.

Table 7-6 Voice Band control registers

Offset Address	Name	Description
0x0000(0x0000)	VBDA0	Voice band DAC0 data buffer
0x0004(0x0002)	VBDA1	Voice band DAC1 data buffer
0x0008(0x0004)	VBAD0	Voice band ADC0 data buffer
0x000C(0x0006)	VBAD1	Voice band ADC1 data buffer

Offset Address	Name	Description
0x0010(0x0008)	VBBUFFSIZE	Voice band buffer size
0x0014(0x000A)	VBADBUFFDTA	Voice band AD buffer control
0x0018(0x000C)	VBDABUFFDTA	Voice band DA buffer control
0x001C(0x000E)	VBADCNT	Voice band AD buffer counter
0x0020(0x0010)	VBDACNT	Voice band DA buffer counter
0x0024 ~0x0030 (0x0012~0x0018)		Reserved
0x0034 (0x001A)	VBINTTYPE	Voice band interrupt type
0x0038 ~0x003C (0x001C~0x001E)		Reserved
0x0040(0x0020)	DAPATHCTL	DAC path control
0x0044(0x0022)	DADGCTL	DAC digital gain control
0x0048(0x0024)	DAHPCTL	DAC 6-band IIR high-pass filter control
0x004C(0x0026)	DAALCCTL0	DAC ALC coefficient: hold
0x0050(0x0028)	DAALCCTL1	DAC ALC coefficient: rise
0x0054(0x002A)	DAALCCTL2	DAC ALC coefficient: fall
0x0058(0x002C)	DAALCCTL3	DAC ALC coefficient: limit
0x005C(0x002E)	DAALCCTL4	DAC ALC coefficient: threshold
0x0060(0x0030)	DAALCCTL5	DAC ALC coefficient: ratio
0x0064(0x0032)	DAALCCTL6	DAC ALC coefficient: cg_var
0x0068(0x0034)	DAALCCTL7	DAC ALC coefficient: release_rate
0x006C(0x0036)	DAALCCTL8	DAC ALC coefficient: attack_rate
0x0070(0x0038)	DAALCCTL9	DAC ALC coefficient: release_rate_ex
0x0074(0x003A)	DAALCCTL10	DAC ALC coefficient: attack_rate_ex
0x0078(0x003C)	STCTL0	Side tone control of channel 0
0x007C(0x003E)	STCTL1	Side tone control of channel 1
0x0080(0x0040)	ADPATHCTL	ADC path control

Offset Address	Name	Description
0x0084(0x0042)	ADDGCTL	ADC digital gain control
0x0088 ~ 0x00FC (0x0044 ~ 0x007E)	Reserved	
0x0100 (0x0080)	HPCOEF0	DAC 6 band IIR High-pass filter coefficients s0
0x0104 (0x0082)	HPCOEF1	DAC 6 band IIR High-pass filter coefficients b0_0
0x0108 (0x0084)	HPCOEF2	DAC 6 band IIR High-pass filter coefficients a0_0
0x010C (0x0086)	HPCOEF3	DAC 6 band IIR High-pass filter coefficients b1_0
0x0110 (0x0088)	HPCOEF4	DAC 6 band IIR High-pass filter coefficients a1_0
0x0114 (0x008A)	HPCOEF5	DAC 6 band IIR High-pass filter coefficients b2_0
0x0118 (0x008C)	HPCOEF6	DAC 6 band IIR High-pass filter coefficients a2_0
0x011C (0x008E)	HPCOEF7	DAC 6 band IIR High-pass filter coefficients s1
0x0120 (0x0090)	HPCOEF8	DAC 6 band IIR High-pass filter coefficients b0_1
0x0124 (0x0092)	HPCOEF9	DAC 6 band IIR High-pass filter coefficients a0_1
0x0128 (0x0094)	HPCOEF10	DAC 6 band IIR High-pass filter coefficients b1_1
0x012C (0x0096)	HPCOEF11	DAC 6 band IIR High-pass filter coefficients a1_1
0x0130 (0x0098)	HPCOEF12	DAC 6 band IIR High-pass filter coefficients b2_1
0x0134 (0x009A)	HPCOEF13	DAC 6 band IIR High-pass filter coefficients a2_1
0x0138 (0x009C)	HPCOEF14	DAC 6 band IIR High-pass filter coefficients s2

Offset Address	Name	Description
0x013C (0x009E)	HPCOEF15	DAC 6 band IIR High-pass filter coefficients b0_2
0x0140 (0x00A0)	HPCOEF16	DAC 6 band IIR High-pass filter coefficients a0_2
0x0144 (0x00A2)	HPCOEF17	DAC 6 band IIR High-pass filter coefficients b1_2
0x0148 (0x00A4)	HPCOEF18	DAC 6 band IIR High-pass filter coefficients a1_2
0x014C (0x00A6)	HPCOEF19	DAC 6 band IIR High-pass filter coefficients b2_2
0x0150 (0x00A8)	HPCOEF20	DAC 6 band IIR High-pass filter coefficients a2_2
0x0154 (0x00AA)	HPCOEF21	DAC 6 band IIR High-pass filter coefficients s3
0x0158 (0x00AC)	HPCOEF22	DAC 6 band IIR High-pass filter coefficients b0_3
0x015C (0x00AE)	HPCOEF23	DAC 6 band IIR High-pass filter coefficients a0_3
0x0160 (0x00B0)	HPCOEF24	DAC 6 band IIR High-pass filter coefficients b1_3
0x0164 (0x00B2)	HPCOEF25	DAC 6 band IIR High-pass filter coefficients a1_3
0x0168 (0x00B4)	HPCOEF26	DAC 6 band IIR High-pass filter coefficients b2_3
0x016C (0x00B6)	HPCOEF27	DAC 6 band IIR High-pass filter coefficients a2_3
0x0170 (0x00B8)	HPCOEF28	DAC 6 band IIR High-pass filter coefficients s4
0x0174 (0x00BA)	HPCOEF29	DAC 6 band IIR High-pass filter coefficients b0_4
0x0178 (0x00BC)	HPCOEF30	DAC 6 band IIR High-pass filter coefficients a0_4
0x017C (0x00BE)	HPCOEF31	DAC 6 band IIR High-pass filter coefficients b1_4

Offset Address	Name	Description
0x0180 (0x00C0)	HPCOEF32	DAC 6 band IIR High-pass filter coefficients a1_4
0x0184 (0x00C2)	HPCOEF33	DAC 6 band IIR High-pass filter coefficients b2_4
0x0188 (0x00C4)	HPCOEF34	DAC 6 band IIR High-pass filter coefficients a2_4
0x018C (0x00C6)	HPCOEF35	DAC 6 band IIR High-pass filter coefficients s5
0x0190 (0x00C8)	HPCOEF36	DAC 6 band IIR High-pass filter coefficients b0_5
0x0194 (0x00CA)	HPCOEF37	DAC 6 band IIR High-pass filter coefficients a0_5
0x0198 (0x00CC)	HPCOEF38	DAC 6 band IIR High-pass filter coefficients b1_5
0x019C(0x00CE)	HPCOEF39	DAC 6 band IIR High-pass filter coefficients a1_5
0x01A0 (0x00D0)	HPCOEF40	DAC 6 band IIR High-pass filter coefficients b2_5
0x01A4 (0x00D2)	HPCOEF41	DAC 6 band IIR High-pass filter coefficients a2_5
0x01A8 (0x00D4)	HPCOEF42	DAC 6 band IIR High-pass filter coefficients s6

8.5.5.2 Register Descriptions

8.5.5.2.1 VBDA0

Description：

0x0000 (0x0000) Voice band DAC0 data (reset 0x0000_0000) VBDA0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBDA0															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBDA0	[15:0]	R/W	16'h0	Voice band DAC0 channel data from ARM/DSP. ARM/DSP writes every word of DAC0 data to this control register, and VBC moves the 16bits data to corresponding address of DAC0 buffer one by one

8.5.5.2.2 VBDA1

Description：

0x0004 (0x0002) Voice band DAC1 data (reset 0x0000_0000) VBDA1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VBDA1															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBDA1	[15:0]	R/W	16'h0	Voice band DAC1 channel data from ARM/DSP. ARM/DSP writes every word of DAC1 data to this control register, and VBC moves the 16bits data to corresponding address of DAC1 buffer one by one

8.5.5.2.3 VBAD0

Description：

0x0008 (0x0004) Voice band ADC0 data (reset 0x0000_0000) VBAD0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VBAD0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBAD0	[15:0]	RO	16'h0	ADC0 channel data from Audio CODEC to ARM/DSP. VBC moves every word from ADC0 buffer one by one to this register, and ARM/DSP read the ADC0 data from this register

8.5.5.2.4 VBAD1

Description：

0x000C (0x0006) Voice band ADC1 data (reset 0x0000_0000) VBAD1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VBAD1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBAD1	[15:0]	RO	16'h0	Reserved for voice band another ADC channel input data. 0x0000 will be output if software reads this control register

8.5.5.2.5 VBBUFFSIZE

Description：

0x0010 (0x0008) Voice band buffer size(reset 0x0000_0000) VBBUFFSIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBDABUFFSIZE								VBADBUFFSIZE							
Type	R/W								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBDABUFFSIZE	[15:8]	R/W	8'h0	Voice band DAC0 and DAC1 channel data buffer size, equals to real buffer size minus 1. max 159. 0~159 maps to real buffer size 1~160
VBADBUFFSIZE	[7:0]	R/W	8'h0	Voice band ADC channel data buffer size, equals to real buffer size minus 1. max 159. 0~159 maps to real buffer size 1~160

8.5.5.2.6 VBADBUFFDTA

Description：

0x0014 (0x000A) Voice band buffer and I2S control(reset 0x0000_1000) VBADBUFFDTA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBIIS_LRCK	VBPCM_MODE	VBIIS_DLOOP	VBISAD_DSEL	VBLSB_EB	VBISDACK_INV	VBISADCK_INV	ADBUFF_Δ								
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBIIS_LRCK	[15]	R/W	1'h0	Active level of 0/1 channel for both ADC and DAC channel "0": High for channel 0, low for channel 1 "1": Low for channel 0, high for channel 1
VBPCM_MODE	[14]	R/W	1'h0	I2S interface format for both ADC and DAC channel 0: I2S compatible format 1: PCM compatible format Note: I2S mode is recommended to be compatible with audio CODEC I2S master
VBIIS_DLOOP	[13]	R/W	1'h0	Loop IIS three Tx signals(DA) to IIS 3 Rx signals(AD). 0: normal mode 1: loop mode
VBISAD_DSEL	[12]	R/W	1'h1	Reserved, No use
VBLSB_EB	[11]	R/W	1'h0	I2S serial data transfer order for both ADC and DAC channel 0: MSB first

				1: LSB first Note: must always be programmed to '0'
VBISDACK_INV	[10]	R/W	1'h0	VBC interface reverses DAC I2S BCLK from audio CODEC as its I2S BCLK to send serial data 0: normal mode 1: inverse mode
VBISADCK_INV	[9]	R/W	1'h0	VBC interface reverses ADC I2S BCLK from audio CODEC as its I2S BCLK to receive serial data 0: normal mode 1: inverse mode
ADBUFF_Δ	[8:0]	R/W	9'h0	Voice band ADC channel data buffer size change, 2's compliment number added to VBADBUFFSIZE, control AD data buffer change for next block.

8.5.5.2.7 VBDABUFFDTA

Description:

0x0018 (0x000C) Voice band buffer and mode control(reset 0x0000_0000) VBDABUFFDTA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBENABLE	VBDA1DMA_EN	VBDA0DMA_EN	VBAD1DMA_EN	VBAD0DMA_EN	RAMSW_EN	RAMSW_NUMB	DABUFF_Δ								
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBENABLE	[15]	R/W	1'h0	Enable this bit then VBC interface starts working and software can receive voice band interrupt. Better set this bit after all other register bits are programmed. 0: disable 1: enable
VBDA1DMA_EN	[14]	R/W	1'h0	DMA write DAC1 data buffer enable, set this bit to enable DAC1 DMA mode 0: disable 1: enable
VBDA0DMA_EN	[13]	R/W	1'h0	DMA write DAC0 data buffer enable, set this bit to enable DAC0 DMA mode 0: disable 1: enable
VBAD1DMA_EN	[12]	R/W	1'h0	Reserved for DMA reading ADC1 data buffer enable 0: disable 1: enable Note: No use since there is only one ADC channel
VBAD0DMA_EN	[11]	R/W	1'h0	DMA read ADC0 data buffer enable, set this bit to enable ADC0 DMA mode 0: disable 1: enable
RAMSW_EN	[10]	R/W	1'h0	Software access ping-pong buffer enable when VBENABE bit low(before VBC interface start working), for both ADC and DAC channel(reading ADC data buffer and writing DAC0, DAC1 data buffer) 0: disable 1: enable
RAMSW_NUMB	[9]	R/W	1'h0	Software accessing ping-pong buffer indication, for both ADC and DAC channel(reading ADC data buffer and writing DAC0, DAC1 data

				buffer) 0: software access data buffer 0 1: software access data buffer 1
DABUFF_Δ	[8:0]	R/W	9'h0	Voice band DAC channel data buffer size change, 2's compliment number added to VBDABUFFSIZE, control DA data buffer change for next block.

8.5.5.2.8 VBADCNT

Description：

0x001C (0x000E) Voice band ADC buffer counter(reset 0x0000_0000) VBADCNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VBAD1CNT								VBAD0CNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBAD1CNT	[15:8]	RO	8'h0	Reserved for ADC1 data buffer address counter.
VBAD0CNT	[7:0]	RO	8'h0	ADC0 data buffer address counter (address of VBC interface writing input data from audio CODEC to ADC0 ping-pong buffer)

8.5.5.2.9 VBDACNT

Description：

0x0020 (0x0010) Voice band DAC buffer counter(reset 0x0000_0000) VBDACNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VBDA1CNT								VBDA0CNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBDA1CNT	[15:8]	RO	8'h0	DAC1 data buffer address counter (address of VBC interface reading output data from DAC1 ping-pong buffer to audio CODEC)
VBDA0CNT	[7:0]	RO	8'h0	DAC0 data buffer address counter (address of VBC interface reading output data from DAC0 ping-pong buffer to audio CODEC)

8.5.5.2.10 VBINTTYPE

Description：

0x0034 (0x001A) Voice Band interrupt type(reset 0x0000_0000) VBINTTYPE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved														Da_int_type	Ad_int_type
Type	RO														R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:2]	RO	14'h0	Reserved
Da_int_type	[1]	R/W	1'h0	DAC interrupt type, 1'b0: wide pulse, and the width is 12 DAC IIS bit clock cycles 1'b1: one apb/z-bus clock cycle pulse
Ad_int_type	[0]	R/W	1'h0	ADC interrupt type, 1'b0: wide pulse, and the width is 12 ADC IIS bit clock cycles 1'b1: one apb/z-bus clock cycle pulse

8.5.5.2.11 DAPATHCTL

Description：

0x0040 (0x0020) Voice band DAC path control (reset 0x0000_0000) DAPATHCTL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								Da1_addst_sel		Da0_addst_sel		Da1_addfm_sel		Da0_addfm_sel	
Type	RO								R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:8]	RO	8'h0	Reserved
Da1_addst_sel	[7:6]	R/W	2'h0	2'b00: DAC1 data from ALC directly sent to DAC I2S 2'b01: DAC1 data from ALC added with side tone data, then sent to DAC I2S 2'b10: DAC1 data from ALC subtracted from side tone output data, then sent to DAC I2S 60.96cmb11: Reserved
Da0_addst_sel	[5:4]	R/W	2'h0	2'b00: DAC0 data from ALC directly sent to DAC I2S 2'b01: DAC0 data from ALC added with side tone data, then sent to DAC I2S 2'b10: DAC0 data from ALC subtracted from side tone output data, then sent to DAC I2S 2'b11: Reserved
Da1_addfm_sel	[3:2]	R/W	2'h0	2'b00: DAC1 buffer data directly sent to DAC HPF 2'b01: DAC1 buffer data added with side tone data, then sent to DAC HPF 2'b10: DAC1 buffer data subtracted from side tone output data, then sent to DAC HPF 2'b11: Reserved
Da0_addfm_sel	[1:0]	R/W	2'h0	2'b00: DAC0 buffer data directly sent to DAC HPF 2'b01: DAC0 buffer data added with side tone output data, then sent to DAC HPF 2'b10: DAC0 buffer data subtracted from side

				tone output data, then sent to DAC HPF 2'b11: Reserved

8.5.5.2.12 DADGCTL

Description：

0x0044 (0x0022) Voice band DAC digital gain control (reset 0x0000_1818) DADGCTL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Dadg_en_1	Dadg_dg_1							Dadg_en_0	Dadg_dg_0						
Type	R/W	R/W							R/W	R/W						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dadg_en_1	[15]	R/W	1'h0	DAC1 digital gain enable
Dadg_dg_1	[14:8]	R/W	7'h00	DAC1 digital gain coefficient 7'h18: 0db larger than 7'h18 : amplify the input signal, and the step is 0.75db smaller than 7'h18 : reduce the input signal, and the step is 0.75db
Dadg_en_0	[7]	R/W	1'h0	DAC0 digital gain enable
Dadg_dg_0	[6:0]	R/W	7'h00	DAC0 digital gain coefficient 7'h18: 0db larger than 7'h18 : amplify the input signal, and the step is 0.75db smaller than 7'h18 : reduce the input signal, and the step is 0.75db

8.5.5.2.13 DAHPCTL

Description：

0x0048 (0x0024) **Voice band DAC High pass filter control (reset 0x0000_007F)** **DAHPCTL**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				Dac_alc_en	Vbhp_en	Hp_reg_clr	Wid_sel	R_limit							
Type	RO				R/W	R/W	R/W	R/W	R/W							
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[15:12]	RO	4’h0	Reserved
Dac_alc_en	[11]	R/W	1’h0	1’b0: ALC bypass 1’b1: ALC enable(if vbhp_en=1)
Vbhp_en	[10]	R/W	1’h0	1’b0: 6-band IIR and ALC bypass 1’b1: 6-band IIR and ALC enable
Hp_reg_clr	[9]	R/W	1’h0	Clear all HPF IIR registers, Please write 1’b1 and later write 1’b0 to finish the register clear process
Wid_sel	[8]	R/W	1’h0	1’b0: 16bits output 1’b1: 24bits output
R_limit	[7:0]	R/W	8’h7F	DAC output signal limit, the actual limit value on the 24bits output signal is: r_limit[7:0]<<16+16’hFFFF

8.5.5.2.14 DAALCCTL0

Description：

0x004C (0x0026) Voice band DAC ALC coefficient : hold (reset 0x0000_0000) DAALCCTL0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Dac_alc_hld															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_hld	[15:0]	R/W	16'h0	DAC ALC coefficient: hold

8.5.5.2.15 DAALCCTL1

Description：

0x0050 (0x0028) Voice band DAC ALC coefficient : rise (reset 0x0000_0000) DAALCCTL1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_rise															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_rise	[15:0]	R/W	16'h0	DAC ALC coefficient: rise

8.5.5.2.16 DAALCCTL2

Description：

0x0054 (0x002A) Voice band DAC ALC coefficient : fall (reset 0x0000_0000) DAALCCTL2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_fall															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_fall	[15:0]	R/W	16'h0	DAC ALC coefficient: fall

8.5.5.2.17 DAALCCTL3

Description:

0x0058 (0x002C) Voice band DAC ALC coefficient : limit (reset 0x0000_0000) DAALCCTL3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_lmt															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_lmt	[15:0]	R/W	16'h0	DAC ALC coefficient: limit

8.5.5.2.18 DAALCCTL4

Description:

0x005C (0x002E) **Voice band DAC ALC coefficient : threshold (reset 0x0000_0000)** **DAALCCTL4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_thd															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_thd	[15:0]	R/W	16'h0	DAC ALC coefficient: threshold

8.5.5.2.19 DAALCCTL5

Description：

0x0060 (0x0030) **Voice band DAC ALC coefficient : ratio (reset 0x0000_0000)** **DAALCCTL5**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_ratio															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_ratio	[15:0]	R/W	16'h0	DAC ALC coefficient: ratio

8.5.5.2.20 DAALCCTL6

Description：

0x0064 (0x0032) **Voice band DAC ALC coefficient : cg_var (reset 0x0000_0000)** **DAALCCTL6**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Dac_alc_cg_var															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_cg_var	[15:0]	R/W	16'h0	DAC ALC coefficient: cg_var

8.5.5.2.21 DAALCCTL7

Description：

0x0068 (0x0034) **Voice band DAC ALC coefficient : release rate(reset 0x0000_0000)** **DAALCCTL7**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_rls_rate															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_rls_rate	[15:0]	R/W	16'h0	DAC ALC coefficient: release rate

8.5.5.2.22 DAALCCTL8

Description：

0x006C (0x0036) **Voice band DAC ALC coefficient : attack rate(reset 0x0000_0000)** **DAALCCTL8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_atk_rate															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_atk_rate	[15:0]	R/W	16'h0	DAC ALC coefficient: attack rate

8.5.5.2.23 DAALCCTL9

Description：

0x0070 (0x0038) **Voice band DAC ALC coefficient : release_rate_ex(reset 0x0000_0000)** **DAALCCTL9**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_rls_rate_ex															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_rls_rate_ex	[15:0]	R/W	16'h0	DAC ALC coefficient: release_rate_ex

8.5.5.2.24 DAALCCTL10

Description：

0x0074 (0x003A) **Voice band DAC ALC coefficient : attack_rate_ex(reset 0x0000_0000)** **DAALCCTL10**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_atk_rate_ex															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_atk_rate_ex	[15:0]	R/W	16'h0	DAC ALC coefficient: attack_rate_ex

8.5.5.2.25 STCTL0

Description：

0x0078 (0x003C) **Voice band Side Tone control of channel0(reset 0x0000_0183)** **STCTL0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			Vbst_en_0	Vbst_hpf_en_0	Vbst_hpf_dg_0							Vbst_hpf_n_0			
Type	RO			R/W	R/W	R/W							R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:13]	RO	3'h0	Reserved
Vbst_en_0	[12]	R/W	1'h0	0: Side tone of channel 0 disable 1: Side tone of channel 0 enable
Vbst_hpf_en_0	[11]	R/W	1'h0	0: Side tone HPF of channel 0 disable 1: Side tone HPF of channel 0 enable
Vbst_hpf_dg_0	[10:4]	R/W	7'h0	Side tone gain coefficient of channel 0 7'h18: 0db larger than 7'h18 : amplify the input signal, and the step is 0.75db smaller than 7'h18 : reduce the input signal, and the step is 0.75db
Vbst_hpf_n_0	[3:0]	R/W	4'h0	Side tone high-pass filter coefficient of channel0. If the high-pass filter is enabled, 4'h3 is the typical configuration, and 4'h0 is reserved.

8.5.5.2.26 STCTL1

Description：

0x007C (0x003E) **Voice band Side Tone control of channel1(reset 0x0000_0183)** **STCTL1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			Vbst_en_1	Vbst_hpf_en_1	Vbst_hpf_dg_1							Vbst_hpf_n_1			
Type	RO			R/W	R/W	R/W							R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:13]	RO	3'h0	Reserved
Vbst_en_1	[12]	R/W	1'h0	0: Side tone of channel 1 disable 1: Side tone of channel 1 enable
Vbst_hpf_en_1	[11]	R/W	1'h0	0: Side tone HPF of channel 1 disable 1: Side tone HPF of channel 1 enable
Vbst_hpf_dg_1	[10:4]	R/W	7'h0	Side tone gain coefficient of channel 1 7'h18: 0db larger than 7'h18 : amplify the input signal, and the step is 0.75db smaller than 7'h18 : reduce the input signal, and the step is 0.75db
Vbst_hpf_n_1	[3:0]	R/W	4'h0	Side tone high-pass filter coefficient of channel1. If the high-pass filter is enabled, 4'h3 is the typical configuration, and 4'h0 is reserved.

8.5.5.2.27 ADPATHCTL

Description：

0x0080 (0x0040) Voice band ADC path control(reset 0x0000_0000) ADPATHCTL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										Ad1_dgmux_sel	Ad0_dgmux_sel	Ad1_inmux_sel		Ad0_inmux_sel	
Type	RO										R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:6]	RO	3'h0	Reserved
Ad1_dgmux_sel	[5]	R/W	1'h0	1'b0: ADC data as input of ADC1 DG 1'b1: DAC ALC output data as input of ADC1 DG
Ad0_dgmux_sel	[4]	R/W	1'h0	1'b0: ADC data as input of ADC0 DG 1'b1: DAC ALC output data as input of ADC0 DG
Ad1_inmux_sel	[3:2]	R/W	2'h0	2'b00: I2S ADC1 data as input of ADC1 path 2'b01: I2S ADC0 data as input of ADC1 path 2'b10: Digital TV I2S ADC1 data as input of ADC1 path 2'b11: All zero as input of ADC1 path
Ad0_inmux_sel	[1:0]	R/W	2'h0	2'b00: I2S ADC0 data as input of ADC0 path 2'b01: I2S ADC1 data as input of ADC1 path 2'b10: Digital TV I2S ADC0 data as input of ADC0 path 2'b11: All zero as input of ADC0 path

8.5.5.2.28 ADDGCTL

Description：

0x0084 (0x0042) Voice band ADC digital gain control (reset 0x0000_1818) ADDGCTL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Addg_en_1	Addg_dg_1							Addg_en_0	Addg_dg_0						
Type	R/W	R/W							R/W	R/W						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Addg_en_1	[15]	R/W	1'h0	ADC1 digital gain enable
Addg_dg_1	[14:8]	R/W	7'h00	ADC1 digital gain coefficient 7'h18: 0db larger than 7'h18 : amplify the input signal, and the step is 0.75db smaller than 7'h18 : reduce the input signal, and the step is 0.75db
Addg_en_0	[7]	R/W	1'h0	ADC0 digital gain enable
Addg_dg_0	[6:0]	R/W	7'h00	ADC0 digital gain coefficient 7'h18: 0db larger than 7'h18 : amplify the input signal, and the step is 0.75db smaller than 7'h18 : reduce the input signal, and the step is 0.75db

8.5.5.2.29 HPCOEF0

Description：

0x00100 (0x0080) DAC 6 band IIR HPF coefficient s0(reset 0x0000_0000) HPCOEF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef0															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef0	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient s0

8.5.5.2.30 HPCOEF1

Description:

0x00104 (0x0082) DAC 6 band IIR HPF coefficient b0_0(reset 0x0000_0000) HPCOEF1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef1															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef1	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b0_0

8.5.5.2.31 HPCOEF2

Description：

0x00108 (0x0084) DAC 6 band IIR HPF coefficient a0_0(reset 0x0000_0000) HPCOEF2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef2															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef2	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a0_0

8.5.5.2.32 HPCOEF3

Description：

0x0010C (0x0086) DAC 6 band IIR HPF coefficient b1_0(reset 0x0000_0000) HPCOEF3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef3															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef3	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b1_0

8.5.5.2.33 HPCOEF4

Description：

0x00110 (0x0088) DAC 6 band IIR HPF coefficient a1_0(reset 0x0000_0000) HPCOEF4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef4															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef4	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a1_0

8.5.5.2.34 HPCOEF5

Description：

0x00114 (0x008A) DAC 6 band IIR HPF coefficient b2_0(reset 0x0000_0000) HPCOEF5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Hpcoef5															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef5	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b2_0

8.5.5.2.35 HPCOEF6

Description：

0x00118 (0x008C) DAC 6 band IIR HPF coefficient a2_0(reset 0x0000_0000) HPCOEF6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef6															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef6	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a2_0

8.5.5.2.36 HPCOEF7

Description:

0x0011C (0x008E) DAC 6 band IIR HPF coefficient s1(reset 0x0000_0000) HPCOEF7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef7															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef7	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient s1

8.5.5.2.37 HPCOEF8

Description：

0x00120 (0x0090) DAC 6 band IIR HPF coefficient b0_1(reset 0x0000_0000) HPCOEF8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Hpcoef8															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef8	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b0_1

8.5.5.2.38 HPCOEF9

Description：

0x00124 (0x0092) DAC 6 band IIR HPF coefficient a0_1(reset 0x0000_0000) HPCOEF9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef9															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef9	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a0_1

8.5.5.2.39 HPCOEF10

Description：

0x00128 (0x0094) DAC 6 band IIR HPF coefficient b1_1(reset 0x0000_0000) HPCOEF10

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef10															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef10	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b1_1

8.5.5.2.40 HPCOEF11

Description：

0x0012C (0x0096) DAC 6 band IIR HPF coefficient a1_1(reset 0x0000_0000) HPCOEF11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Hpcoef11															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef11	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a1_1

8.5.5.2.41 HPCOEF12

Description：

0x00130 (0x0098) DAC 6 band IIR HPF coefficient b2_1(reset 0x0000_0000) HPCOEF12

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef12															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef12	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b2_1

8.5.5.2.42 HPCOEF13

Description:

0x00134 (0x009A) DAC 6 band IIR HPF coefficient a2_1(reset 0x0000_0000) HPCOEF13

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef13															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef13	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a2_1

8.5.5.2.43 HPCOEF14

Description：

0x00138 (0x009C) DAC 6 band IIR HPF coefficient s2(reset 0x0000_0000) HPCOEF14

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Hpcoef14															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef14	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient s2

8.5.5.2.44 HPCOEF15

Description：

0x0013C (0x009E) DAC 6 band IIR HPF coefficient b0_2(reset 0x0000_0000) HPCOEF15

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef15															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef15	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b0_2

8.5.5.2.45 HPCOEF16

Description：

0x00140 (0x00A0) DAC 6 band IIR HPF coefficient a0_2(reset 0x0000_0000) HPCOEF16

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef16															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef16	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a0_2

8.5.5.2.46 HPCOEF17

Description：

0x00144 (0x00A2) DAC 6 band IIR HPF coefficient b1_2(reset 0x0000_0000) HPCOEF17

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Hpcoef17															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef17	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b1_2

8.5.5.2.47 HPCOEF18

Description：

0x00148 (0x00A4) DAC 6 band IIR HPF coefficient a1_2(reset 0x0000_0000) HPCOEF18

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef18															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef18	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a1_2

8.5.5.2.48 HPCOEF19

Description:

0x0014C (0x00A6) DAC 6 band IIR HPF coefficient b2_2(reset 0x0000_0000) HPCOEF19

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef19															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef19	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b2_2

8.5.5.2.49 HPCOEF20

Description：

0x00150 (0x00A8) DAC 6 band IIR HPF coefficient a2_2(reset 0x0000_0000) HPCOEF20

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Hpcoef20															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef20	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a2_2

8.5.5.2.50 HPCOEF21

Description：

0x00154 (0x00AA) DAC 6 band IIR HPF coefficient s3(reset 0x0000_0000) HPCOEF21

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef21															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef21	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient s3

8.5.5.2.51 HPCOEF22

Description:

0x00158 (0x00AC) DAC 6 band IIR HPF coefficient b0_3(reset 0x0000_0000) HPCOEF22

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef22															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef22	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b0_3

8.5.5.2.52 HPCOEF23

Description：

0x0015C (0x00AE) DAC 6 band IIR HPF coefficient a0_3(reset 0x0000_0000) HPCOEF23

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Hpcoef23															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef23	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a0_3

8.5.5.2.53 HPCOEF24

Description：

0x00160 (0x00B0) DAC 6 band IIR HPF coefficient b1_3(reset 0x0000_0000) HPCOEF24

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef24															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef24	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b1_3

8.5.5.2.54 HPCOEF25

Description：

0x00164 (0x00B2) DAC 6 band IIR HPF coefficient a1_3(reset 0x0000_0000) HPCOEF25

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef25															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef25	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a1_3

8.5.5.2.55 HPCOEF26

Description：

0x00168 (0x00B4) DAC 6 band IIR HPF coefficient b2_3(reset 0x0000_0000) HPCOEF26

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Hpcoef26															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef26	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b2_3

8.5.5.2.56 HPCOEF27

Description：

0x0016C (0x00B6) DAC 6 band IIR HPF coefficient a2_3(reset 0x0000_0000) HPCOEF27

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef27															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef27	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a2_3

8.5.5.2.57 HPCOEF28

Description:

0x00170 (0x00B8) DAC 6 band IIR HPF coefficient s4(reset 0x0000_0000) HPCOEF28

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef28															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef28	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient s4

8.5.5.2.58 HPCOEF29

Description：

0x00174 (0x00BA) DAC 6 band IIR HPF coefficient b0_4(reset 0x0000_0000) HPCOEF29

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Hpcoef29															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef29	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b0_4

8.5.5.2.59 HPCOEF30

Description：

0x00178 (0x00BC) DAC 6 band IIR HPF coefficient a0_4(reset 0x0000_0000) HPCOEF30

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef30															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef30	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a0_4

8.5.5.2.60 HPCOEF31

Description:

0x0017C (0x00BE) DAC 6 band IIR HPF coefficient b1_4(reset 0x0000_0000) HPCOEF31

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef31															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef31	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b1_4

8.5.5.2.61 HPCOEF32

Description：

0x00180 (0x00C0) DAC 6 band IIR HPF coefficient a1_4(reset 0x0000_0000) HPCOEF32

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Hpcoef32															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef32	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a1_4

8.5.5.2.62 HPCOEF33

Description：

0x00184 (0x00C2) DAC 6 band IIR HPF coefficient b2_4(reset 0x0000_0000) HPCOEF33

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef33															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef33	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b2_4

8.5.5.2.63 HPCOEF34

Description:

0x00188 (0x00C4) DAC 6 band IIR HPF coefficient a2_4(reset 0x0000_0000) HPCOEF34

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef34															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef34	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a2_4

8.5.5.2.64 HPCOEF35

Description：

0x0018C (0x00C6) DAC 6 band IIR HPF coefficient s5(reset 0x0000_0000) HPCOEF35

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Hpcoef35															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef35	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient s5

8.5.5.2.65 HPCOEF36

Description：

0x00190 (0x00C8) DAC 6 band IIR HPF coefficient b0_5(reset 0x0000_0000) HPCOEF36

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef36															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef36	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b0_5

8.5.5.2.66 HPCOEF37

Description:

0x00194 (0x00CA) DAC 6 band IIR HPF coefficient a0_5(reset 0x0000_0000) HPCOEF37

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef37															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef37	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a0_5

8.5.5.2.67 HPCOEF38

Description：

0x00198 (0x00CC) DAC 6 band IIR HPF coefficient b1_5(reset 0x0000_0000) HPCOEF38

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Hpcoef38															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef38	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b1_5

8.5.5.2.68 HPCOEF39

Description：

0x0019C (0x00CE) DAC 6 band IIR HPF coefficient a1_5(reset 0x0000_0000) HPCOEF39

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef39															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef39	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a1_5

8.5.5.2.69 HPCOEF40

Description:

0x001A0 (0x00D0) DAC 6 band IIR HPF coefficient b2_5(reset 0x0000_0000) HPCOEF40

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef40															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef40	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b2_5

8.5.5.2.70 HPCOEF41

Description：

0x001A4 (0x00D2) DAC 6 band IIR HPF coefficient a2_5(reset 0x0000_0000) HPCOEF41

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef41															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef41	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a2_5

8.5.5.2.71 HPCOEF42

Description：

0x001A8 (0x00D4) DAC 6 band IIR HPF coefficient s6(reset 0x0000_0000) HPCOEF42

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef42															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef42	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient s6

8.6 Audio Codec Control Registers

The Audio Coedc control registers base address is 0x8200_0100(ARM) or 0x007F_0100(DSP). The following table lists these control registers.

Offset Address	Name	Description
0x0100	VB_AICR	Voice band Codec AICR
0x0104	VB_CR1	Voice band Codec CR1
0x0108	VB_CR2	Voice band Codec CR2
0x010C	VB_CCR1	Voice band Codec CCR1

Offset Address	Name	Description
0x0110	VB_CCR2	Voice band Codec CCR2
0x0114	VB_PMR1	Voice band Codec PMR1
0x0118	VB_PMR2	Voice band Codec PMR2
0x011C	VB_CRR	Voice band Codec CRR
0x0120	VB_ICR	Voice band Codec ICR
0x0124	VB_IFR	Voice band Codec IFR
0x0128	VB_CGR1	Voice band Codec CGR1
0x012C	VB_CGR2	Voice band Codec CGR2
0x0130	VB_CGR3	Voice band Codec CGR3
0x0134~0x0140	Reserved	
0x0144	VB_CGR8	Voice band Codec CGR8
0x0148	VB_CGR9	Voice band Codec CGR9
0x014C	VB_CGR10	Voice band Codec CGR10
0x0150	VB_TR1	Voice band Codec TR1
0x0154	VB_TR2	Voice band Codec TR2

8.6.1 VB_AICR

0x0100 **Audio Codec interface mode control** **VB_AICR**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								Reserved				DAC_SERIAL	ADC_SERIAL	DAC_I2S	ADC_I2S
Type	RO								R/W				R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:8]	RO	8'h0	Reserved
	[7:4]	R/W	4'h0	Reserved
DAC_SERIAL	[3]	R/W	1'h1	Selection of the DAC digital serial audio interface 0= Parallel interface 1= Serial interface Note: Parallel interface is not supported, this control bit should not be changed from the default value
ADC_SERIAL	[2]	R/W	1'h1	Selection of the ADC digital serial audio interface 0= Parallel interface 1= Serial interface Note: Parallel interface is not supported, this control bit should not be changed from the default value
DAC_I2S	[1]	R/W	1'h0	Working mode of the DAC digital serial audio

				interface 0= DSP mode 1= I2S mode Note: I2S mode is recommended to be compatible with VBC interface I2S slave
ADC_I2S	[0]	R/W	1'h0	Working mode of the ADC digital serial audio interface 0= DSP mode 1= I2S mode Note: I2S mode is recommended to be compatible with VBC interface I2S slave

8.6.2 VB_CR1

0x0104 **Audio Codec mode control** **VB_CR1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								SB_MICBIAS	MONO	DAC_MUTE	HP_DIS	DACSEL	BYPASS	BTL_MUTE	Reserved
Type	RO								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0

Field Name	Bit	Type	Reset Value	Description
	[15:8]	RO	8'h0	Reserved

SB_MICBIAS	[7]	R/W	1'h1	Microphone biasing buffer power-down 0= active 1= power-down
MONO	[6]	R/W	1'h0	Stereo-to-mono conversion for DAC path 0= stereo 1= mono
DAC_MUTE	[5]	R/W	1'h1	DAC soft mute mode 0= mute inactive, digital input signal transmitted to the DAC 1= puts the DAC in soft mute mode
HP_DIS	[4]	R/W	1'h0	Headphone output signal disabled: 0= Signal applied to headphone outputs 1= no signal on headphone outputs, acts as a mute signal
DACSEL	[3]	R/W	1'h1	Mixer input selection 0= DAC output ignored in input of the mixer 1= DAC output selected as an input of the mixer
BYPASS	[2]	R/W	1'h0	Mixer input selection (line) 0= Bypass path ignored in input of the mixer 1= Bypass path selected as an input of the mixer
BTL_MUTE	[1]	R/W	1'h1	BTL mute mode 0= active 1= puts the BTL stage in mute mode
	[0]	R/W	1'h0	Reserved

8.6.3 VB_CR2

0x0108 **Audio Codec mode control** **VB_CR2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								DAC_DEEMP	DAC_ADWL		ADC_ADWL		ADC_HPF	MICSEL	Reserved
Type	RO								R/W	R/W		R/W		R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:8]	RO	8'h0	Reserved
DAC_DEEMP	[7]	R/W	1'h0	DAC De-emphasize filter enable 0= inactive 1= enables the de-emphasis filter
DAC_ADWL	[6:5]	R/W	2'h3	Audio Data Word Length: for DAC paths 00 = 16-bit word length data 01 = 18-bit word length data 10 = 20-bit word length data 11 = 24-bit word length data Note: Only 16-bit word length audio data is supported, so it must be programmed to be 2'b00
ADC_ADWL	[4:3]	R/W	2'h3	Audio Data Word Length: for ADC paths 00 = 16-bit word length data 01 = 18-bit word length data 10 = 20-bit word length data 11 = 24-bit word length data Note: Only 16-bit word length audio data is supported, so it must be programmed to be

				2'b00
ADC_HPF	[2]	R/W	1'h0	ADC High Pass Filter enable 0= inactive 1= enables the ADC High Pass Filter
MICSEL	[1]	R/W	1'h0	selection of the signal converted by the ADC 0 = Microphone input 1 (MICP, MICN) 1 = Microphone input 2 (AUXMICP, AUXMICN)
	[0]	R/W	1'h0	Reserved

8.6.4 VB_CCR1

0x010C **Audio Codec mode control** **VB_CCR1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												CRYSTA			
Type	RO												R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:4]	RO	12'h0	Reserved
CRYSTAL	[3:0]	R/W	4'h0	Selection of the MCLK frequency The sampling frequency value is as following: 0000: 12 MHz 0001:16.9344 MHz (for further use) 0010: 16.9344 MHz (for further use)

				0011: 16.9344 MHz (for further use) 0100 :16.9344 MHz (for further use) 0101 :16.9344 MHz (for further use) 0110 :16.9344 MHz (for further use) 0111 :16.9344 MHz (for further use) 1000 :16.9344 MHz (for further use) 1001 :16.9344 MHz (for further use) 1010 :16.9344 MHz (for further use) 1011 :16.9344 MHz (for further use) 1100 :16.9344 MHz (for further use) 1101 :16.9344 MHz (for further use) 1110 :16.9344 MHz (for further use) 1111 :16.9344 MHz (for further use) Note: Only 12MHz MCLK is supported, so it should be always 4'b0000, please remain the default value unchanged

8.6.5 VB_CCR2

0x0110 **Audio Codec mode control** **VB_CCR2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								DREEQ				AREEQ			
Type	RO								R/W				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:8]	RO	8'h0	Reserved
DFREQ	[7:4]	R/W	4'h0	Selection of the DAC sampling rate (Fs) The sampling frequency value is given in the following: 0000: 96kHz 0001: 48kHz 0010: 44.1kHz 0011: 32kHz 0100: 24kHz 0101: 22.05kHz 0110: 16kHz 0111: 12kHz 1000: 11.025kH 1001: 9.6kHz 1010: 8kHz 1011: 8kHz 1100: 8kHz 1101: 8kHz 1110: 8kHz 1111: 8kHz
AFREQ	[3:0]	R/W	4'h0	Selection of the ADC sampling rate (Fs) The sampling frequency value is given in the following: 0000: 96kHz 0001: 48kHz 0010: 44.1kHz 0011: 32kHz 0100: 24kHz 0101: 22.05kHz 0110: 16kHz 0111: 12kHz 1000: 11.025kH

				1001: 9.6kHz 1010: 8kHz 1011: 8kHz 1100: 8kHz 1101: 8kHz 1110: 8kHz 1111: 8kHz

8.6.6 VB_PMR1

0x0114 **Audio Codec mode control** **VB_PMR1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								SB_DAC	SB_OUT	SB_MIX	SB_ADC	SB_LIN	SB_BTL	SB_LOUT	Reserved
Type	RO								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[15:8]	RO	8'h0	Reserved
SB_DAC	[7]	R/W	1'h1	DAC power-down mode 0= active 1= power-down

SB_OUT	[6]	R/W	1'h1	Output stage power-down mode 0= active 1= power-down
SB_MIX	[5]	R/W	1'h1	Mixer and line output stage power-down 0= active 1= power-down
SB_ADC	[4]	R/W	1'h1	ADC power-down mode 0= active 1= power-down
SB_LIN	[3]	R/W	1'h1	Analog line Input (Bypass) conditioning circuitry power-down mode 0= active 1= power-down
SB_BTL	[2]	R/W	1'h1	BTL output conditioning circuitry power-down mode 0= active 1= power-down
SB_LOUT	[1]	R/W	1'h1	Line out + BTL conditioning circuitry power-down mode 0= active 1= power-down
	[0]	R/W	1'h1	Reserved

8.6.7 VB_PMR2

0x0118 **Audio Codec mode control** **VB_PMR2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										LRGOD	RLGOD	GIM	SB_MC	SB	SB_SLEEP
Type	RO										R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Field Name	Bit	Type	Reset Value	Description
	[15:6]	RO	10'h0	Reserved
LRGOD	[5]	R/W	1'h0	DAC mixing gain coupling 00: Left and right channels gains are independent, respectively given by GODL and GODR 10: Left and right channels gain is given by GODL 01: Left and right channels gain is given by GODR 11: Left and right channels gain is given by GODL

RLGOD	[4]	R/W	1'h0	DAC mixing gain coupling 00: Left and right channels gains are independent, respectively given by GODL and GODR 10: Left and right channels gain is given by GODL 01: Left and right channels gain is given by GODR 11: Left and right channels gain is given by GODL
GIM	[3]	R/W	1'h0	Microphone amplifier gain control 0= 0 dB gain 1= 20 dB gain
SB_MC	[2]	R/W	1'h0	Output Stage common mode buffer power-down 0= active (capacitor less headphone output configuration) 1= power-down (line output configuration)
SB	[1]	R/W	1'h1	complete power-down mode 0= normal mode (active) 1= complete power-down
SB_SLEEP	[0]	R/W	1'h1	sleep mode 0= normal mode (active) 1= sleep mode

8.6.8 VB_CRR

0x011C **Audio Codec mode control** **VB_CRR**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved									RATIO		KFAST			TRESH	
Type	RO									R/W		R/W			R/W	
Reset	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1

Field Name	Bit	Type	Reset Value	Description
	[15:7]	RO	9'h0	Reserved
RATIO	[6:5]	R/W	2'h2	ratio between fast and slow steps 00: Ratio =1 01: Ratio = 2 10: Ratio = 4 (default, remain unchanged) 11: Ratio = 8

KFAST	[4:2]	R/W	3'h4	factor for step time in fast slope part 000: KFast =1 001: KFast = 2 010: KFast = 4 011: KFast = 8 100: KFast =16 (default, remain unchanged) 101: KFast = 32
TRESH	[1:0]	R/W	2'h1	threshold between fast and slow slope parts 00: Threshold = 0 01: Threshold = 32 (default, remain unchanged) 10: Threshold = 64 11: Threshold = 128

8.6.9 VB_ICR

0x0120 **Audio Codec mode control** **VB_ICR**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								INT_FORM		JACK_MASK	CCMC_MASK	RUD_MASK	RDD_MASK	GUD_MASK	GDD_MASK
Type	RO								R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[15:8]	RO	8'h0	Reserved
INT_FORM	[7:6]	R/W	2'h0	Waveform and polarity of the IRQ signal 00: The generated IRQ is a high level 01: The generated IRQ is a low level 10: The generated IRQ is a high level pulse with an 8 MC_CLK cycles duration when using 8-bit parallel control interface or 8 MCLK cycles duration when using I2C control interface 11: The generated IRQ is a low level pulse with an 8 MC_CLK cycles duration when using 8-bit parallel control interface or 8 MCLK cycles duration when using I2C control interface
JACK_MASK	[5]	R/W	1'h1	Mask for the JACK_EVENT flag 0: interrupt enabled 1: interrupt masked (no IRQ generation)

CCMC_MASK	[4]	R/W	1'h1	Mask for the CCMC flag Read/Write 0: interrupt enabled 1: interrupt masked (no IRQ generation)
RUD_MASK	[3]	R/W	1'h1	Mask for the RAMP_UP_DONE flag 0: interrupt enabled 1: interrupt masked (no IRQ generation)
RDD_MASK	[2]	R/W	1'h1	Mask for the RAMP_DOWN_DONE flag 0: interrupt enabled 1: interrupt masked (no IRQ generation)
GUD_MASK	[1]	R/W	1'h1	Mask for the GAIN_UP_DONE flag 0: interrupt enabled 1: interrupt masked (no IRQ generation)
GDD_MASK	[0]	R/W	1'h1	Mask for the GAIN_DOWN_DONE flag 0: interrupt enabled 1: interrupt masked (no IRQ generation)

8.6.10 VB_IFR

0x0124 **Audio Codec mode control** **VB_IFR**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved									JACK	JACK_EVENT	CCMC	RAMP_UP_DONE	RAMP_DOWN_DONE	GAIN_UP_DONE	GAIN_DOWN_DONE
Type	RO									RO	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:7]	RO	9'h0	Reserved
JACK	[6]	RO	1'h0	Output Jack plug detection status Read 0 = no jack 1 = output jack present
JACK_EVENT	[5]	R/W	1'h0	Event on output Jack plug detection status Read 0 = no event 1 = event detected Write 1 = Reset of the flag

CCMC	[4]	R/W	1'h0	Output short circuit detection status - Reserved for future use Read 0 = inactive 1 = indicates that a short circuit has been detected by the output stage. Write 1 = Update of the flag
RAMP_UP_DONE	[3]	R/W	1'h0	End of output stage ramp up flag Read 1 = the ramp-up sequence is completed (output stage is active). Write 1 = Reset of the flag
RAMP_DOWN_DONE	[2]	R/W	1'h0	End of output stage ramp down flag Read 1 = the ramp-down sequence is completed (output stage in stand-by mode). Write 1 = Reset of the flag
GAIN_UP_DONE	[1]	R/W	1'h0	End of mute gain up sequence flag Read 1 = the mute sequence is completed, the DAC input signal is transmitted to the DAC path. Write 1 = Reset of the flag
GAIN_DOWN_DONE	[0]	R/W	1'h0	End of mute gain down sequence flag Bit Read 1 = the mute sequence is completed, a 0 DC signal is transmitted to the DAC path. Interpretation of any unspecified point is absolutely up to the designer of this Virtual Component. Write

				1 = Reset of the flag

8.6.11 VB_CGR1

0x0128 **Audio Codec mode control** **VB_CGR1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								GODR				GODL			
Type	RO								R/W				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:8]	RO	8'h0	Reserved
GODR	[7:4]	R/W	4'h0	DAC mixing right channel gain programming value
GODL	[3:0]	R/W	4'h0	DAC mixing left channel gain programming value

8.6.12 VB_CGR2

0x012C **Audio Codec mode control** **VB_CGR2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								LRGOB/RLGOB		Reserved	GOBL				
Type	RO								R/W		R/W	R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:8]	RO	8'h0	Reserved
LRGOB/RLGOB	[7:6]	R/W	2'h0	Line mixing gain coupling 00: Left and right channels gains are independent, respectively given by GOBL and GOBR 10: Left and right channels gain is given by GOBL 01: Left and right channels gain is given by GOBR 11: Left and right channels gain is given by GOBL
	[5]	R/W	1'h0	Reserved
GOBL	[4:0]	R/W	5'h4	Line mixing left channel gain programming value

8.6.13 VB_CGR3

0x0130 **Audio Codec mode control** **VB_CGR3**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											GOBR				
Type	RO											R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:5]	RO	11'h0	Reserved
GOBR	[4:0]	R/W	5'h4	Line mixing right channel gain programming value

8.6.14 VB_CGR8

0x0144 **Audio Codec mode control** **VB_CGR8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								LRGO/RLGO		Reserved	GOL				
Type	RO								R/W		R/W	R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Field Name	Bit	Type	Reset Value	Description
	[15:8]	RO	8'h0	Reserved
LRGO/RLGO	[7:6]	R/W	2'h0	Output stages gain coupling 00: Left and right channels gains are independent, respectively given by GOL and GOR 10: Left and right channels gain is given by GOL 01: Left and right channels gain is given by GOR 11: Left and right channels gain is given by GOL
	[5]	R/W	1'h0	Reserved
GOL	[4:0]	R/W	5'hA	Output stage left channel gain programming value

8.6.15 VB_CGR9

0x0148 **Audio Codec mode control** **VB_CGR9**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											GOR				
Type	RO											R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Field Name	Bit	Type	Reset Value	Description
	[15:5]	RO	11'h0	Reserved
GOR	[4:0]	R/W	5'hA	Output stage right channel gain programming value

8.6.16 VB_CGR10

0x014C **Audio Codec mode control** **VB_CGR10**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								GI				Reserved			
Type	RO								R/W				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:8]	RO	8'h0	Reserved
GI	[7:4]	R/W	4'h0	ADC channel PGATM input gain programming value
	[3:0]	R/W	4'h0	Reserved

8.6.17 VB_TR1

0x0150 **Audio Codec mode control** **VB_TR1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								STBYO	STBYI	TSTDAC	TSTADC	TEST	STOPULL	NOSC	FAST_ON
Type	RO								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:8]	RO	8'h0	Reserved
STBYO	[7]	R/W	1'h0	analog output stage power down mode 0: in normal mode
STBYI	[6]	R/W	1'h0	analog input stage power down mode 0: in normal mode
TSTDAC	[5]	R/W	1'h0	DAC analog test mode 0: in normal mode
TSTADC	[4]	R/W	1'h0	ADC analog test mode 0: in normal mode
TEST	[3]	R/W	1'h0	Test mode 0: in normal mode
STOPULL	[2]	R/W	1'h0	disables the input circuitry starting system 0: in normal mode
NOSC	[1]	R/W	1'h0	Disable the output short circuit protection 0: in normal mode
FAST_ON	[0]	R/W	1'h0	Disables the pop reduction internal mechanisms

				0: in normal mode

8.6.18 VB_TR2

0x0154 **Audio Codec mode control** **VB_TR2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								FAENDAC	FAENADC	NENCOMP	Reserved	NODEM	HIPAS	NO_RST	UNSTBL
Type	RO								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:8]	RO	8'h0	Reserved
FAENDAC	[7]	R/W	1'h0	Flow adapter command control bit (DAC path) 0: inactive 1: enables the flow adapter working mode
FAENDAC	[6]	R/W	1'h0	Flow adapter command control bit (ADC path) 0: inactive 1: enables the flow adapter working mode
NENCOMP	[5]	R/W	1'h0	Biasing bit control 0: in normal mode

	[4]	R/W	1'h0	Reserved
NODEM	[3]	R/W	1'h0	DAC DEM control 0: in normal mode
HIPAS	[2]	R/W	1'h0	ADC NTF test control 0: in normal mode
NO_RST	[1]	R/W	1'h0	ADC auto reset control 0: in normal mode
UNSTBL	[0]	R/W	1'h0	disables the pop reduction internal mechanisms 0: in normal mode

8.7 Application Note

8.7.1 ARM Control Mode

If the audio system is controlled by ARM, the following programming flow is recommended:

1. Enable VBC and ADI module by setting global register GEN0(0x8B00_0008) bit [23] and bit [6]. Enable and select ADI clock by configuring global register CLK_DLY_CTRL(0x8B00_005C) bit [29:28].
2. Turn on LDO_VB by setting ARM side global control register LDO_PD_CTL (0x8200_0490) bit [14] through ADI.
3. Enable ARM access Audio Codec and MCLK of Audio Codec by setting ARM side global control register CLK_CTL(0x8200_0488) bit [2:1] through ADI.
4. Enable ARM access VBC and necessary audio channels (ADC/DAC0/DAC1) by programming global register BUSCLK (0x8B00_0044) bit [7:1]
5. Program buffer size of AD and DA in register VBBUFFSIZE (0x8200_3010). If needed, program all necessary modes in register VBADBUFFDTA (0x8200_3014).

6. Set bit [10] of register VBDABUFFDTA (0x8200_3018) to enable software initialization of both of the DAC0 and DAC1 ping-pong buffers. Set bit [9] to write buffer 1 and reset bit [9] to write buffer 0.
7. Program necessary VBC path control and HPF control registers.
8. Program necessary control registers of the audio codec.
9. Reset bit [10] and bit [9] of register VBDABUFFDTA to finish the software initialization, and then set bit [15] to enable the voice band process.
10. Wait for interrupt. The interrupt status can be read from global control register INT_CTRL (0x8B00_0010) bits [6:5]. If AD interrupt got, clear it by writing global control register ICLR (0x8B00_0014) bit [5] and read AD data from VBC interface control register VBAD0 (0x8200_3008), and the totally data number is buffer size programmed at step 2. Then wait for the next AD interrupt. If DA interrupt got, clear it by writing global control register INT_CLR (0x8B00_0014) bit [6] and write another block of data, the number of which is also the buffer size, to VBC interface control register VBDA0 (0x8200_3000) and VBDA1 (0x8200_3004). Then wait for the next DA interrupt.

8.7.2 DSP Control Mode

If the audio system is controlled by DSP, the following programming flow is recommended:

1. Enable STC, VBC and ADI module by setting PMU register PLL_CFG0 (0x0013_0000) bit [26], bit [22] and bit [7]. Enable ADI HCLK by resetting PMU register XHPMOD(0x0013_0018) bit [9].
2. Turn on LDO_VB by setting ARM side global control register LDO_PD_CTL (0x8200_0490) bit [14] through ADI.
3. Enable MCLK of Audio Codec by setting DSP side global control register DSP_CTL(0x007F_0528) bit [0] through ADI.
4. Enable necessary audio channels (ADC/DAC0/DAC1) by programming STC control register FORCE_PD (0x0064_0294) bits [8:4].
5. Program buffer size of AD and DA in register VBBUFFSIZE (0x0063_0008). If needed, program all necessary modes in register VBADBUFFDTA (0x0063_000A).
6. Set bit [10] of register VBDABUFFDTA (0x0063_000C) to enable software initialization of both of the DAC0 and DAC1 ping-pong buffers. Set bit [9] to write buffer 1 and reset bit [9] to write buffer 0.
7. Program necessary VBC path control and HPF control registers

8. Program necessary control registers of the audio codec.
9. Enable DAC interrupt by setting STC control register CLK_AGC_LDO (0x0064_02BE) bit [5].
10. Reset bit [10] and bit [9]of register VBDABUFFDTA to finish the software initialization, and then set bit [15] to enable the voice band process.
11. Wait for interrupt. The interrupt status can be read from ICU control register ISR_1 (0x0013_0404) bit [4] and bit [5]. If AD interrupt comes, clear it by writing ICU control register ICR_1 (0x0013_040C) bit [4] and read AD data from VBC interface control register VBAD0 (0x0063_0004), and the total data number is the buffer size programmed at step 2. Then wait for the next AD interrupt. If DA interrupt comes, clear it by writing ICU control register ICR_1 (0x0013_040C) bit [5] and write another block of data, the number of which is also the buffer size, to VBC interface control register VBDA0 (0x0063_0000) and VBDA1 (0x0063_0002). Then wait for the next DA interrupt.

8.7.3 DMA Controlling Mode

If the audio system is controlled by ARM DMA, the following programming flow is recommended:

1. Enable VBC and ADI module by setting global register GEN0(0x8B00_0008) bit [23] and bit [6]. Enable and select ADI clock by configuring global register CLK_DLY_CTRL(0x8B00_005C) bit [29:28].
2. Turn on LDO_VB by setting ARM side global control register LDO_PD_CTL (0x8200_0490) bit [14] through ADI.
3. Enable MCLK of Audio Codec by setting DSP side global control register DSP_CTL(0x007F_0528) bit [0] through ADI.
4. Enable necessary audio channels (ADC/DAC0/DAC1) by programming STC control register FORCE_PD (0x0064_0294) bits [8:4].
5. Program buffer size of AD and DA in register VBBUFFSIZE (0x8200_3010). If needed, program all necessary modes in register VBADBUFFDTA (0x8200_3014).
6. Set bit [10] of register VBDABUFFDTA (0x8200_3018) to enable software initialization (clearing zero is recommended) of both DAC0 and DAC1 ping-pong buffers. Set bit [9] to write buffer 1 and reset bit [9] to write buffer 0.

7. Enable DMA by setting AHB general control register AHB_CTL0 (0x2090_0200) bit [6], and then enable the three DMA channels respectively for VBC ADC, DAC0 and DAC1, by setting DMA control register DMA_Chn_En bits [12:10].
8. Program necessary control registers of the audio codec.
9. Enable DMA All_int by setting DMA control register TRANS_DONE_EN(0x2010_0048) bits [12:10] for the three channels, and enable DMA interrupt in Interrupt control register INTCV_INT_EN (0x8000_3008) bit [21]. Disable VBC interrupt by setting Interrupt control register INTCV_INT_EN_CLR(0x8000_300C) bit [22].
10. Write first block of DAC data (the number of which is integral times of buffer size) into DMA DAC0 and DAC1 source memory.
11. Program DMA VBC DAC0 channel control registers 0x2010_0540 ~ 0x2010_055C, DAC1 channel control registers 0x2010_0560 ~ 0x2010_057C, and ADC0 channel control registers 0x2010_0580 ~ 0x2010_059C.
12. Enable DMA access to VBC ping-pong buffers of three channels by setting VBC control register VBDABUFFDTA (0x8200_3018) bits [14], [13] and [11], Reset bit [10] and bit [9] of register VBDABUFFDTA and set bit [15] to enable the voice band process.
13. Wait for DMA all transfer finish interrupt. ADC0, DAC0 and DAC1 channel interrupt status can be checked by reading DMA control register TRANS_DONE_RAW(0x2010_0068) bits [12:10]. Clear interrupt of the DMA three channels by setting DMA control register TRANS_DONE_CLR (0x2010_0078) bits [12:10].
14. For ADC channel, ARM reads ADC data (the number of which is integral times of buffer size) from DMA ADC0 destination memory, and then program DMA ADC0 channel control registers for the next block. For DAC channels, ARM write next block of DAC data (integral times of buffer size) into DMA DAC0 and DAC1 source memory, and then program DMA DAC0 and DAC1 channel control registers for the next block.
15. Repeat steps 10 and 11 until all ADC data are received by ARM, and all DAC data are sent by ARM. Especially for DAC, ARM should wait for the last two interrupts of VBC. After clearing the last DMA DAC0 and DAC1 interrupts, first clear previous VBC interrupt, and then enable VBC interrupt in Interrupt controller by setting Interrupt control register 0x8000_300C bit [22]. Wait for VBC interrupt, and check if the two DAC channels both finished by reading global register INT_CTRL (0x8B00_0010) bit [6]. Clear the VBC DAC interrupt by setting global

control register INT_CLR (0x8B00_0014) bit [6]. Repeat once more for the last VBC DAC interrupt.

9 Power Management

9.1 Overview

SC6820 integrated power management unit supports direct connection to battery, which means all supply voltages are generated on-chip with integrated linear voltage regulators and DC-DC. The input of these linear voltage regulators is from the battery.

PMU contains the following blocks:

- 25 LDOs.
- 2 DCDC, which supply the digital power
- Battery charger, which can be used with lithium ion batteries.
- Three current sinks for keypad LED, white LED and vibrator control.
- Under/UP Voltage Lock-out Protection
- Over Temperature Protection
- Band-gap
- Power-on reset generator

The integrated power management also provides sophisticated controls for system startup, including start-up with discharged batteries, trickle charging and system reset control. The flexible clock switching options allow minimizing the power consumption during the operation phases. Current consumption in the deep sleep mode is minimized by reducing the clock frequency to 32 kHz and switching most LDOs off for maximum battery life.

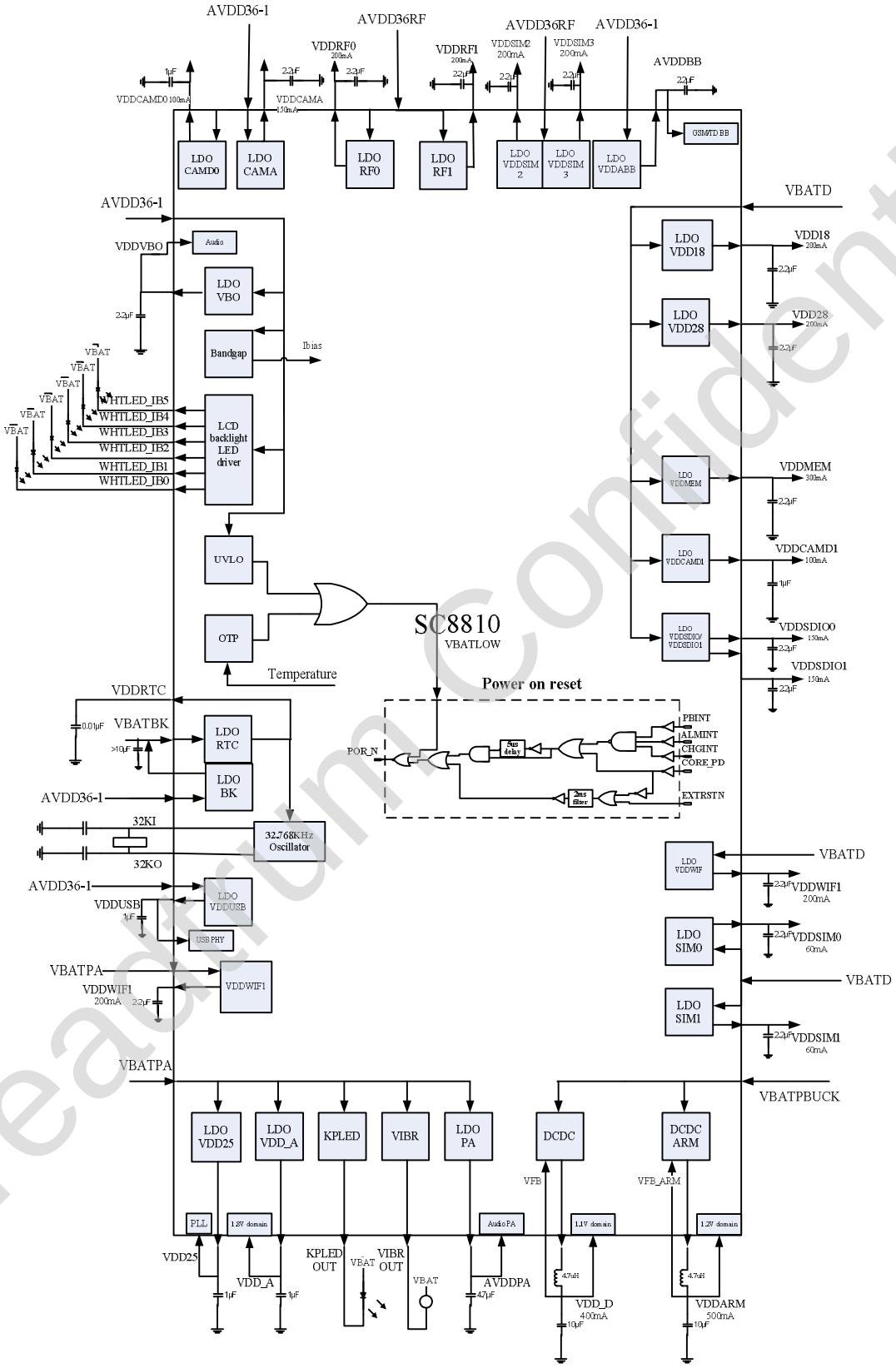


Figure 9-1 SC6820 PMU Architecture

Note1: When VBATLOW signal is high, chip is powered off.

9.2 LDO and DC-DC

SC6820 integrated low-voltage and low quiescent current low dropout regulators (LDO) for power supply and power management purposes. Some extra LDO regulators are designed for external use. All LDOs have their own bypass (power-down) control signals. External tantalum or MLCC ceramic capacitors are recommended to use with the LDOs. SC6820 also intergrated DC-DC as digital power supply. The brief specifications are listed below.

Table 9-1 Performance of the integrated LDO regulators

Parameter	Comments	Min	Typical	Max	Unit
External Memory Voltage(VDDMEM)					
Status after reset	on				
Application	SDRAM				
Output Voltage	0(default)	1.7	1.8	1.9	V
Output Current				300	mA
Line regulation	Vi=3.6V-4.2V;Io=100mA;	5	10	20	mV
Line Transient Response	Vi=3.6V-4.2V;Io=100mA;Tr=10us	25	50	75	mV
Load regulation	Vi=3.8V; Io=0-200mA;	25	50	75	mV
Load Transient Response	Vi=3.8V; Io=0-200mA;Co=2.2uF; Tr=10us	30	60	90	mV
PSRR	F=217Hz,Io=100mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	50	85	120	us
Tpd	Vo=0.1V (Iout=Imax/2)	50	80	120	us
Isleep	Io=0mA	8	10	20	uA

Parameter	Comments	Min	Typical	Max	Unit
Cext	External cap	2.2	2.2	4.7	uF
Digital 2.8V IO Voltage(VDD28)					
Status after reset	on				
Application	IO/ NAND Flash/LCM				
Output Voltage	00(default)	2.7	2.8	2.9	V
	01	2.9	3.0	3.1	V
	10	2.55	2.65	2.75	V
	11	1.75	1.8	1.85	V
Output Current				200	mA
Line regulation	Vi=3.6V-4.2V;Io=100mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=100mA;Tr=10us	15	25	50	mV
Load Regulation	Vi=3.8V; Io=0-200mA;	30	50	75	mV
Load Transient Regulation	Vi=3.8V; Io=0-200mA;Co=2.2uF; Tr=10us	30	50	75	mV
Short current limit		75	90	120	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=100mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	80	100	120	us
Tpd	Vo=0.1V (Iout=Imax/2)	200	300	400	us
Isleep	Io=0mA	12	15	25	uA
Cext	External cap	2.2	2.2	4.7	uF
Digital 1.8V IO Voltage(VDD18)					
Status after reset	on				
Application	IO/ NAND Flash/LCM				
Output Voltage	00(default)	1.75	1.8	1.85	V
	01	2.7	2.8	2.9	V
	10	1.45	1.5	1.55	V

Parameter	Comments	Min	Typical	Max	Unit
	11	1.15	1.2	1.25	V
Output Current				200	mA
Line Regulation	Vi=3.6V-4.2V;Io=100mA;	6	12	24	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=100mA;Tr=10us	10	20	30	mV
Load regulation	Vi=3.8V; Io=0-200mA;	30	60	90	mV
Load Transient Regulation	Vi=3.8V; Io=0-200mA;Co=2.2uF; Tr=10us	30	60	90	mV
Short current limit		75	90	120	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=100mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	90	150	225	us
Tpd	Vo=0.1V (Iout=Imax/2)	90	150	225	us
Isleep	Io=0mA	10	15	25	uA
Cext		2.2	2.2	4.7	uF
LDO for RF0(VDDRF0)					
Status after reset	on				
Application	RF/TCXO				
Output Voltage	00(default)	2.75	2.85	2.95	V
	01	2.85	2.95	3.05	V
	10	2.65	2.75	2.85	V
	11	1.75	1.8	1.85	V
Output Current				200	mA
Line regulation	Vi=3.6V-4.2V;Io=100mA;	3	5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=100mA;Tr=10us	5	10	20	mV
Load regulation	Vi=3.8V; Io=0-200mA;	25	50	75	mV
Load Transient Regulation	Vi=3.8V; Io=0-200mA;Co=2.2uF; Tr=10us	25	50	75	mV

Parameter	Comments	Min	Typical	Max	Unit
PSRR	F=217Hz,Io=100mA,	48	60	72	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	30	50	75	us
Tpd	Vo=0.1V (Iout=Imax/2)	110	160	240	us
Isleep	Io=0mA	30	40	55	uA
Cext		2.2	2.2	4.7	uF
LDO for RF1 (VDDRF1)					
Status after reset	off				
Application	Supply for external terminal				
Output Voltage	00(default)	2.75	2.85	2.95	V
	01	2.85	2.95	3.05	V
	10	2.4	2.5	2.6	V
	11	1.75	1.8	1.85	V
Output Current				200	mA
Line regulation	Vi=3.6V-4.2V;Io=100mA;	3	5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=100mA;Tr=10us	5	10	20	mV
Load regulation	Vi=3.8V; Io=0-100mA;	25	50	75	mV
Load Transient Regulation	Vi=3.8V; Io=0-100mA;Co=2.2uF; Tr=10us	25	50	75	mV
PSRR	F=217Hz,Io=100mA,	48	60	72	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	30	50	75	us
Tpd	Vo=0.1V (Iout=Imax/2)	96	160	240	us
Isleep	Io=0mA	32	40	55	uA
Cext		2.2	2.2	4.7	uF
Digital SDIO0 Voltage (VDDSD0)					
Status after reset	off				
Application	SD Card				
Output Voltage	00(default)	2.7	2.8	2.9	V

Parameter	Comments	Min	Typical	Max	Unit
	01	2.9	3.0	3.1	V
	10	2.4	2.5	2.6	V
	11	1.7	1.8	1.9	V
Output Current				150	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	15	30	45	mV
Load regulation	Vi=3.8V; Io=0-50mA;	15	30	45	mV
Load Transient Regulation	Vi=3.8V; Io=0-50mA;Co=1uF; Tr=10us	25	50	75	mV
Short current limit		75	90	120	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=50mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	20	35	50	us
Tpd	Vo=0.1V (Iout=Imax/2)	110	180	270	us
Isleep	Io=0mA	16	20	30	uA
Cext		1	2.2	4.7	uF
Digital SDIO1 Voltage (VDDSD1)					
Status after reset	off				
Application	SD Card				
Output Voltage	00(default)	2.7	2.8	2.9	V
	01	2.9	3.0	3.1	V
	10	2.4	2.5	2.6	V
	11	1.7	1.8	1.9	V
Output Current				150	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	15	30	45	mV
Load regulation	Vi=3.8V; Io=0-50mA;	15	30	45	mV

Parameter	Comments	Min	Typical	Max	Unit
Load Transient Regulation	Vi=3.8V; Io=0-50mA;Co=1uF; Tr=10us	25	50	75	mV
Short current limit		75	90	120	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=50mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	20	35	50	us
Tpd	Vo=0.1V (Iout=Imax/2)	110	180	270	us
Isleep	Io=0mA	16	20	30	uA
Cext		1	2.2	4.7	uF
General LDO(VDDCAMD0)					
Status after reset	off				
Application	Supply for external sensor				
Output Voltage	00(default)	1.75	1.8	1.85	V
	01	2.7	2.8	2.9	V
	10	1.45	1.5	1.55	V
	11	1.25	1.3	1.35	V
Output Current				100	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	10	20	30	mV
Load regulation	Vi=3.8V; Io=0-50mA;	15	30	45	mV
Load Transient Regulation	Vi=3.8V; Io=0-50mA;Co=1uF; Tr=10us	15	30	45	mV
PSRR	F=217Hz,Io=50mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	12	20	30	us
Tpd	Vo=0.1V (Iout=Imax/2)	110	180	270	us
Isleep	Io=0mA	16	20	30	uA
Cext		1	1	2.2	uF

Parameter	Comments	Min	Typical	Max	Unit
General LDO (VDDCAMDA)					
Status after reset	off				
Application	Supply for external sensor				
Output Voltage	00(default)	2.7	2.8	2.9	V
	01	2.9	3.0	3.1	V
	10	2.4	2.5	2.6	V
	11	1.7	1.8	1.9	V
Output Current				150	mA
Line regulation	Vi=3.6V-4.2V;Io=80mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=80mA;Tr=10us	10	20	30	mV
Load regulation	Vi=3.8V; Io=0-80mA;	15	30	45	mV
Load Transient Regulation	Vi=3.8V; Io=0-80mA;Co=1uF; Tr=10us	15	30	45	mV
PSRR	F=217Hz,Io=50mA,	36	40	50	dB
Cext		1	1	2.2	uF
General LDO (VDDCAMD1)					
Status after reset	off				
Application	Supply for external sensor				
Output Voltage	00(default)	2.7	2.8	2.9	V
	01	3.2	3.3	3.4	V
	10	1.75	1.8	1.85	V
	11	1.15	1.2	1.25	V
Output Current				100	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	10	20	30	mV
Load regulation	Vi=3.8V; Io=0-50mA;	15	30	45	mV
Load Transient Regulation	Vi=3.8V; Io=0-50mA;Co=1uF; Tr=10us	15	30	45	mV

Parameter	Comments	Min	Typical	Max	Unit
PSRR	F=217Hz,Io=50mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	12	20	30	us
Tpd	Vo=0.1V (Iout=Imax/2)	110	180	270	us
Isleep	Io=0mA	16	20	30	uA
Cext		1	1	2.2	uF
Small battery and Real time clock LDO (VDDBK and VDDRTC)					
Status after reset	On				
Application	Supply for small battery and RTC				
VBATBK Output Voltage	00	2.45	2.6	2.75	V
	01 (default)	2.65	2.8	2.95	V
	10	2.85	3.0	3.15	V
	11	3.05	3.2	3.35	V
VBATBK output resistor	00 (default)	160	200	240	Ω
	01	400	500	600	Ω
	10	1200	1500	1800	Ω
	11	1600	2000	2400	Ω
VDDRTC Output Voltage	00(default)	1.75	1.8	1.85	V
	01	1.65	1.7	1.75	V
	10	1.55	1.6	1.65	V
	11	1.45	1.5	1.55	V
Output Current				1	mA
Line regulation	Vi=3.6V-4.2V;Io=0.2mA;	8	15	30	mV
Load regulation	Vi=3.8V; Io=0-0.2mA	5	10	20	mV
Tpu	Supply ramp from 0 to 3.6v in 10µs	50	80	120	us
Isleep	Vbat	15	**18**	24	uA

Parameter	Comments	Min	Typical	Max	Unit
	Vbuk	10	11.5	17	uA
Cext		0.01	0.01	0.047	uF
SIMO LDO (VSIM0)					
Status after reset	On				
Application	Supply for SIM Card				
Output Voltage	00(default)	1.7	1.8	1.9	V
	01	2.8	2.9	3.0	V
	10	2.9	3.0	3.1	V
	11	3.0	3.1	3.2	V
Output Current				60	mA
Line regulation	Vi=3.6V-4.2V;Io=30mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=30mA;Tr=10us	10	20	30	mV
Load regulation	Vi=3.8V; Io=0-30mA;	15	30	45	mV
Load Transient Regulation	Vi=3.8V; Io=0-30mA;Co=1uF; Tr=10us	15	30	45	mV
Short current limit		25	30	45	mA
Current limit	Vi=3.8V	120	150	225	mA
PSRR	F=217Hz,Io=30mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	60	100	150	us
Tpd	Vo=0.1V (Iout=Imax/2)	150	250	375	us
Isleep	Io=0mA	12	15	23	uA
Cext		1	1	2.2	uF
SIM1 LDO (VSIM1)					
Status after reset	Off				
Application	Supply for SIM Card				
Output Voltage	00(default)	1.7	1.8	1.9	V
	01	2.8	2.9	3.0	V
	10	2.9	3.0	3.1	V

Parameter	Comments	Min	Typical	Max	Unit
	11	3.0	3.1	3.2	V
Output Current				60	mA
Line regulation	Vi=3.6V-4.2V;Io=30mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=30mA;Tr=10us	10	20	30	mV
Load regulation	Vi=3.8V; Io=0-30mA;	15	30	45	mV
Load Transient Regulation	Vi=3.8V; Io=0-30mA;Co=1uF; Tr=10us	15	30	45	mV
Short current limit		25	30	45	mA
Current limit	Vi=3.8V	120	150	225	mA
PSRR	F=217Hz,Io=30mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	60	100	150	us
Tpd	Vo=0.1V (Iout=Imax/2)	150	250	375	us
Isleep	Io=0mA	12	15	23	uA
Cext		1	1	2.2	uF
Analog BB Voltage(AVDDBB)					
Status after reset	On				
Application	Supply for BB circuit, for example ADC/DAC//APC				
Output Voltage	00(default)	2.9	3.0	3.1	V
	01	3.0	3.1	3.2	V
	10	2.8	2.9	3.0	V
	11	2.7	2.8	2.9	V
Output Current				60	mA
Line regulation	Vi=3.6V-4.2;Io=50mA;	3	5	10	mV
Line Transient Regulation	Vi=3.6V-4.2;Io=50mA;Tr=10us	5	10	20	mV
Load regulation	Vi=3.8V; Io=0-100mA;	15	30	60	mV
Load Transient Regulation	Vi=3.8V; Io=0-50mA;Co=2.2uF; Tr=10us	25	50	100	mV

Parameter	Comments	Min	Typical	Max	Unit
PSRR	F=217Hz,Io=50mA,	48	60	72	dB
Tpu	Supply ramp from 0 to 3.6v in 10μs	36	60	90	us
Tpd	Vo=0.1V (Iout=Imax/2)	90	150	225	us
Isleep	Io=0mA	32	40	60	uA
Cext		2.2	2.2	4.7	uF
Analog VB Voltage(AVDDVB)					
Status after reset	Off				
Application	VB analog/VB output				
Output Voltage	00(default)	3.2	3.3	3.4	V
	01	3.3	3.4	3.5	V
	10	3.1	3.2	3.3	V
	11	2.8	2.9	3.0	V
Output Current				100	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	3	5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	5	10	20	mV
Load regulation	Vi=3.8V; Io=0-100mA;	8	15	30	mV
Load Transient Regulation	Vi=3.8V; Io=0-50mA;Co=4.7F; Tr=10us	25	50	75	mV
PSRR	F=217Hz,Io=50mA,	48	60	72	dB
Tpu	Supply ramp from 0 to 3.6v in 10μs	30	50	75	us
Tpd	Vo=0.1V (Iout=Imax/2)	210	350	500	us
Isleep	Io=0mA	32	40	60	uA
Cext		2.2	2.2	4.7	uF
USB High Voltage(VDDUSBH)					
Status after reset	Off				
Application	USB IP				
Output Voltage	00 (default)	3.2	3.3	3.4	V

Parameter	Comments	Min	Typical	Max	Unit
	01	3.3	3.4	3.5	V
	10	3.1	3.2	3.3	V
	11	3.0	3.1	3.2	V
Output Current				60	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	10	20	40	mV
Load regulation	Vi=3.8V; Io=0-30mA;	15	30	60	mV
Load Transient Regulation	Vi=3.8V; Io=0-30mA;Co=2.2uF; Tr=10us	15	30	60	mV
PSRR	F=217Hz,Io=50mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	9	15	23	us
Tpd	Vo=0.1V (Iout=Imax/2)	240	400	600	us
Isleep	Io=0mA	12	15	23	uA
Cex		1	1	2.2	uF
VDD25(VDD25)					
Status after reset	On				
Application	PLL and EFUSE				
Output Voltage	00 (default)	2.4	2.5	2.6	V
	01	2.65	2.75	2.85	V
	10	2.9	3.0	3.1	V
	11	2.8	2.9	3.0	V
Output Current				60	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	10	20	40	mV
Load regulation	Vi=3.8V; Io=0-30mA;	20	40	80	mV
Load Transient Regulation	Vi=3.8V; Io=0-30mA;Co=2.2uF; Tr=10us	20	40	80	mV

Parameter	Comments	Min	Typical	Max	Unit
Tpu	Supply ramp from 0 to 3.6v in 10µs	60	100	200	us
PSRR	F=217Hz,Io=30mA,	48	60	72	dB
Cex		2.2	2.2	4.7	uF
DVDD18(VDD_A)					
Status after reset	On				
Application	Analog 1.8V power				
Output Voltage		1.7	1.8	1.9	V
Output Current				80	mA
Line regulation	Vi=3.6V-4.2V;Io=50mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us	10	20	40	mV
Load regulation	Vi=3.8V; Io=0-30mA;	20	40	80	mV
Load Transient Regulation	Vi=3.8V; Io=0-30mA;Co=2.2uF; Tr=10us	20	40	80	mV
PSRR	F=217Hz,Io=50mA,	36	40	50	dB
Cex		1	1	2.2	uF
WIF0 LDO Voltage (VDDWIF0)					
Status after reset	Off				
Application	Supply for external Wif terminal				
Output Voltage	00	2.7	2.8	2.9	V
	01(default)	3.15	3.3	3.45	V
	10	1.7	1.8	1.9	V
	11	1.1	1.2	1.3	V
Output Current				200	mA
Line regulation	Vi=3.6V-4.2V;Io=100mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=100mA;Tr=10us	12	25	50	mV
Load Regulation	Vi=3.8V; Io=0-200mA;	25	50	100	mV
Load Transient	Vi=3.8V; Io=0-200mA;Co=2.2uF;	25	50	100	mV

Parameter	Comments	Min	Typical	Max	Unit
Regulation	Tr=10us				
Short current limit		75	90	120	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=100mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	60	100	150	us
Tpd	Vo=0.1V (Iout=Imax/2)	180	300	450	us
Isleep	Io=0mA	12	15	23	uA
Cext	External cap	2.2	2.2	4.7	uF
WIF1 LDO Voltage (VDDWIF1)					
Status after reset	Off				
Application	Supply for external Wif terminal				
Output Voltage	00	2.7	2.8	2.9	V
	01(default)	3.15	3.3	3.45	V
	10	1.7	1.8	1.9	V
	11	1.1	1.2	1.3	V
Output Current				200	mA
Line regulation	Vi=3.6V-4.2V;Io=100mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=100mA;Tr=10us	12	25	50	mV
Load Regulation	Vi=3.8V; Io=0-200mA;	25	50	100	mV
Load Transient Regulation	Vi=3.8V; Io=0-200mA;Co=2.2uF; Tr=10us	25	50	100	mV
Short current limit		75	90	120	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=100mA,	36	40	50	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	60	100	150	us
Tpd	Vo=0.1V (Iout=Imax/2)	180	300	450	us

Parameter	Comments	Min	Typical	Max	Unit
Isleep	Io=0mA	12	15	23	uA
Cext	External cap	2.2	2.2	4.7	uF
SIM2 LDO (VSIM2)					
Status after reset	Off				
Application	Supply for SIM Card or CMMB RF				
Output Voltage	00	2.7	2.8	2.9	V
	01	2.9	3	3.1	V
	10(default)	1.7	1.8	1.9	V
	11	1.3	1.2	1.1	V
Output Current				200	mA
Line regulation	Vi=3.6V-4.2V;Io=30mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=30mA;Tr=10us	10	20	40	mV
Load regulation	Vi=3.8V; Io=0-30mA;	15	30	60	mV
Load Transient Regulation	Vi=3.8V; Io=0-30mA;Co=1uF; Tr=10us	15	30	60	mV
Short current limit		130	150	200	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=30mA,	48	60	72	dB
Tpu	Supply ramp from 0 to 3.63v in 10μs	72	120	180	us
Tpd	Vo=0.1V (Iout=Imax/2)	150	250	333	us
Isleep	Io=0mA	12	15	23	uA
Cext		2.2	2.2	4.7	uF
SIM3 LDO (VSIM3)					
Status after reset	Off				
Application	Supply for SIM Card or CMMB RF				
Output Voltage	00	2.7	2.8	2.9	V
	01	2.9	3	3.1	V

Parameter	Comments	Min	Typical	Max	Unit
	10(default)	1.7	1.8	1.9	V
	11	1.3	1.2	1.1	V
Output Current				**200**	mA
Line regulation	Vi=3.6V-4.2V;Io=30mA;	5	10	20	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=30mA;Tr=10us	10	20	40	mV
Load regulation	Vi=3.8V; Io=0-30mA;	15	30	60	mV
Load Transient Regulation	Vi=3.8V; Io=0-30mA;Co=1uF; Tr=10us	15	30	60	mV
Short current limit		130	150	200	mA
Current limit	Vi=3.8V	410	480	640	mA
PSRR	F=217Hz,Io=30mA,	48	60	72	dB
Tpu	Supply ramp from 0 to 3.6v in 10µs	72	120	180	us
Tpd	Vo=0.1V (Iout=Imax/2)	150	250	333	us
Isleep	Io=0mA	12	15	23	uA
Cext		2.2	2.2	4.7	uF
LDO_PA					
Status after reset	off				
Application	Audio PA				
Output voltage	000	2.7	2.9	3.1	V
	001	2.8	3.0	3.2	V
	010	2.9	3.1	3.3	V
	011	3.0	3.2	3.4	V
	100(default)	3.1	3.3	3.5	V
	101	3.2	3.4	3.6	V
	110	3.3	3.5	3.6	V
	111	3.4	3.6	-	V
Output current				400	mA

Parameter	Comments	Min	Typical	Max	Unit
Line regulation	Vsupply=3.6->4.2V, Iout=200mA	5	10	20	mV
Line transient regulation	Vsupply=3.6->4.2V, Iout=200mA, Trise=10us	10	20	40	mV
Load regulation	Vsupply=3.8V, Iout=0->400mA	40	80	160	mV
Load transient regulation	Vsupply=3.8V, Iout=0->400mA, Trise=10us	50	100	200	mV
PSRR	Freq=217Hz, Iout=400mA	36	40	50	dB
Time to power up	Vsupply=0->3.8V, Trise=10us	60	100	150	us
Time to power down	Vout=0.1V, Iout=400mA	180	300	450	us
Isleep	Iout=0mA	12	15	23	uA
Output capacitor	Required for stability and ripple rejection	4.7	4.7	10	µF

Table 9-2 Performance of DC-DC circuit

Parameter	Comments/Conditions	Min	Typical	Max	Unit
DCDC for ARM					
Status after reset	on				
Application	Digital core power				
Output voltage	000	0.55	0.65	0.75	V
	001	0.6	0.7	0.8	V
	010	0.7	0.8	0.9	V
	011	0.8	0.9	1	V
	100	0.9	1.0	1.1	V
	101	1	1.1	1.2	V
	110(default)	1.1	1.2	1.3	V
	111	1.2	1.3	1.4	V
Trim voltage	Trim votage step (32 step)	2	3	4	mv
Output current				500	mA
Line regulation	Vsupply=3.6->4.2V, Iout=200mA	5	10	20	mV

Parameter	Comments/Conditions	Min	Typical	Max	Unit
Line transient regulation	Vsupply=3.6->4.2V, Iout=200mA, Trise=10us	15	30	60	mV
Load regulation	Vsupply=3.8V, Iout=0->400mA	40	80	160	mV
Load transient regulation	Vsupply=3.8V, Iout=0->400mA, Trise=10us	50	100	200	mV
Time to power up	Vsupply=0->4.3V, Trise=10us	60	100	150	us
Switching frequency		1	1.5	2.25	MHz
Isleep	Iout=0mA	72	90	100	uA
Effiency	100mA loading	80	85	90	%
Parameter	**Comments/Conditions**	**Min**	**Typical**	**Max**	**Unit**
DCDC for other Core					
Status after reset	on				
Application	Digital core power				
Output voltage	000	0.55	0.65	0.75	V
	001	0.6	0.7	0.8	V
	010	0.7	0.8	0.9	V
	011	0.8	0.9	1	V
	100	0.9	1.0	1.1	V
	101(default)	1	1.1	1.2	V
	110	1.1	1.2	1.3	V
	111	1.2	1.3	1.4	V
Trim voltage	Trim votage step (32 step)	2	3	4	mv
Output current				500	mA
Line regulation	Vsupply=3.6->4.2V, Iout=200mA	5	10	20	mV
Line transient regulation	Vsupply=3.6->4.2V, Iout=200mA, Trise=10us	15	30	60	mV
Load regulation	Vsupply=3.8V, Iout=0->400mA	40	80	160	mV
Load transient regulation	Vsupply=3.8V, Iout=0->400mA, Trise=10us	50	100	200	mV
Time to power up	Vsupply=0->4.3V, Trise=10us	60	100	150	us

Parameter	Comments/Conditions	Min	Typical	Max	Unit
Switching frequency		1	1.5	2.25	MHz
Isleep	Iout=0mA	72	90	100	uA
Effiency	100mA loading	80	85	90	%

Note1: IO voltage can be switched between 1.8V and 2.8V supplied byVDD18 and VDD28.

Note2. There are two structures for these intergrated LDOs.

Note3. The PSRR listed means the worst value for all loading statuses and cover all frequency range.

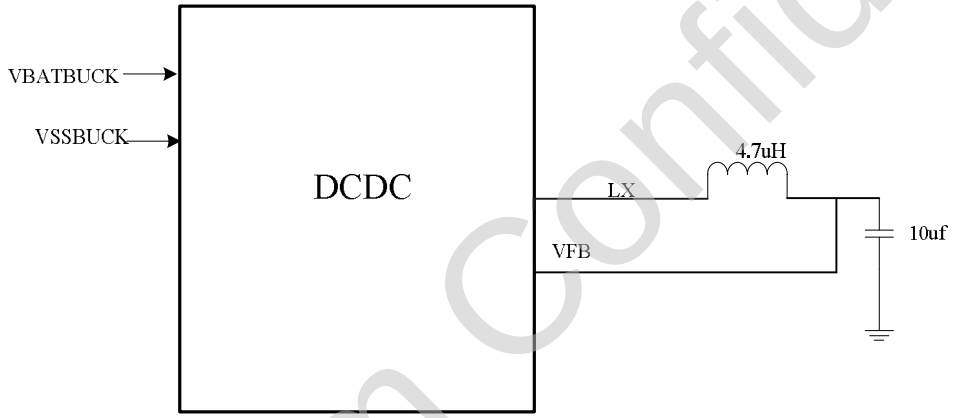


Figure 9-2 DCDC Application diagram

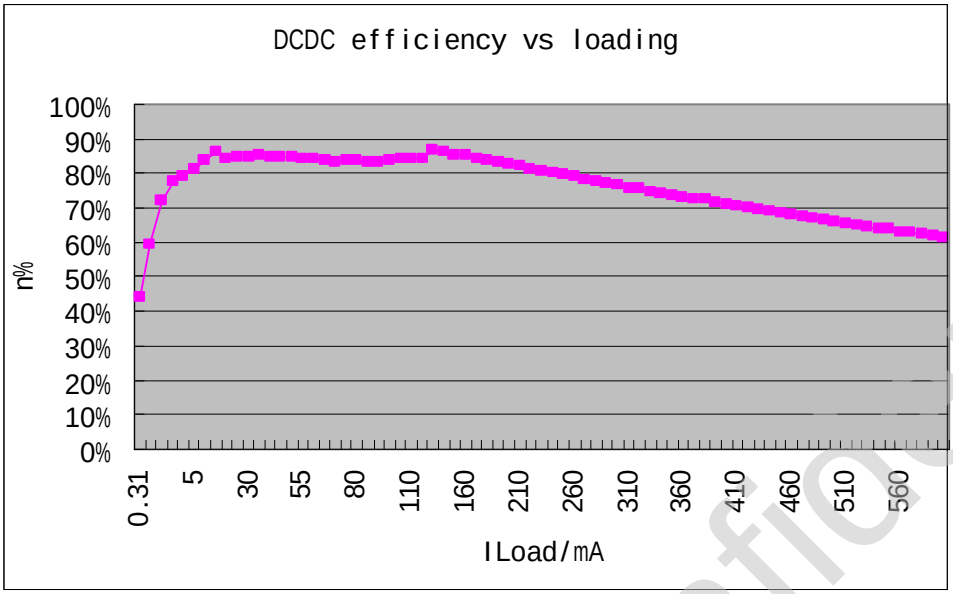


Figure 9-3 DCDC efficiency vs loading

9.3 Charger

SC6820 provides an integrated Li-ion battery charger control module. With an external PMOS transistor and a current sensing resistor, SC6820 can control the charging of Li-ion battery. SC6820 also supports charging from USB port. SC6820 can monitor both charging current and battery voltage with the auxiliary ADC.

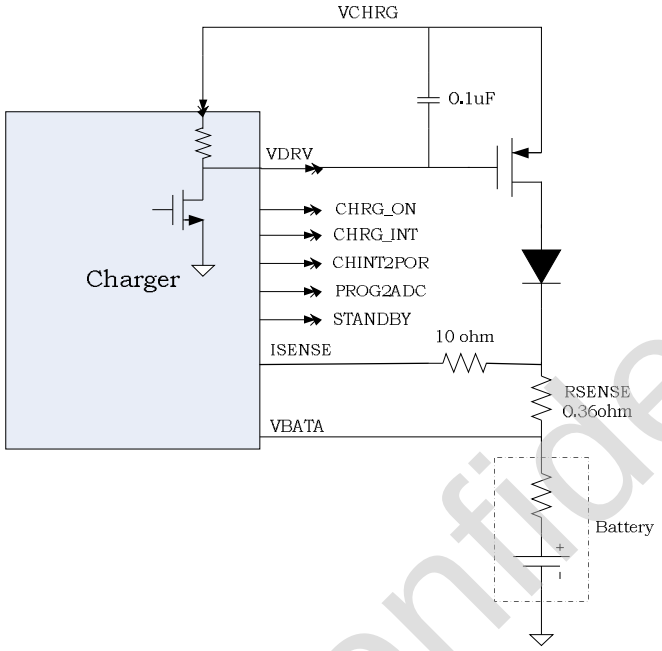


Figure 9-4 Charger application diagram

9.3.1 Charging Process

A charge cycle begins when the voltage at VCHG pin rises above 4.5 V.

If the VBAT is less than 1.1 V, the charger enters activate charge mode. In this mode, charger supplies approximately 5 mA charge current to activate the battery.

If VBAT is more than 1.1 V but less than 2.7 V, the charger enters small current charge mode. In this mode, charger supplies approximately 50 mA charge current to bring the battery voltage up to a safe level for full current charging.

When VBAT voltage rises above 2.7 V, the charger enters full current charge mode. The charger uses a constant-current algorithm in both small current and full charge modes.

When VBAT approaches the final float voltage (4.2 V), the charger enters constant-voltage mode, and the charging current begins to decrease. As the charging current drops to 1/10 of the programmed value, the charge cycle ends.

9.3.2 Programming Charge Current

The charge current is programmed using an internal resistor from the PROG pin to ground. Rint = 3 kΩ. If PROG is 1.2 V, the charge current Ichg = 1.2 * 1000 / 3k = 400 mA.

9.3.3 Charge Standby

When the charge current falls to 1/10 of the programmed current, or when the PROG pin voltage falls bellow 120 mV, the charger goes into standby mode. In standby mode, the charger ceases to provide charge current to the battery.

9.3.4 Recharge Control

If the charger power supply is connected, software can control for recharge after the initial charge is finished. The charger control circuit sends out a signal STANDBY, when the initial charge is done. The charger control circuit accepts a control signal, RECHG, with an initial value of 0. Software can generate an active-high pulse at RECHG when the following conditions are met.

- CHGON = 1, indicating the charger power supply is connected and its voltage is > 4.5 V.
- STANDBY = 1, indicating the initial charge is done.
- VBAT is less than some predetermined value for recharge.

9.3.5 Software Over Current Protection

In charge cycle, if the charge current is above 1.3 times the programmed current, the charger ceases to provide charge current to the battery and enters standby mode.

9.4 LCD Backlight LED Driver

The LCD Backlight module provides four matched current sources, sinks up to 24.75 mA of load current to accommodate each of the four White LEDs. The module uses current mirror to construct LCD backlight driver. The reference current source ISET is set with an external resistor R. Each of the matched current regulators has a 100:1 current ratio between the VLEDx outputs (one channel) and the ISET currents. It requires no charge pump. Brightness can be controlled by software. The module is in shut down mode when the whtled_pd is active.

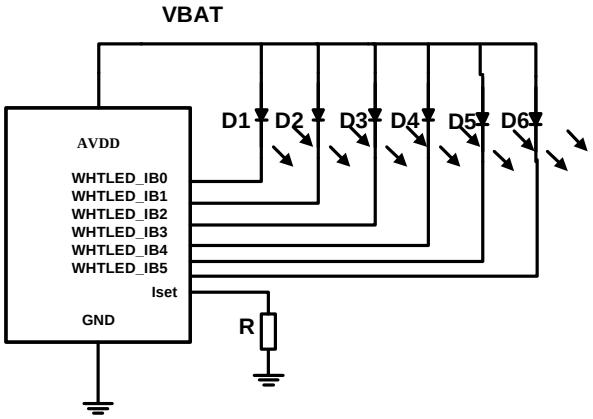


Figure 9-5 LCD backlight LED driver application

Note1: D1 in the diagram must be connected to a LED when in use, otherwise the LED driver current control bits will not be effective.

Table 9-3 Peformance of LCD backlight LED driver

Parameter	Conditions/Comments	Min	Typical	Max	Unit
Status after reset	off				
Output current	00000(min current) (default)		1.5		mA
	00001		2.25		
	00010		3.0		
	00011		3.75		
	00100		4.5		
	00101		5.25		
	00110		6.0		
	00111		6.75		
	01000		7.5		
	01001		8.25		
	01010		9		
	01011		9.75		
	01100		10.5		
	01101		11.25		

	01110		12.0		
	01111		12.75		
	10000		13.5		
Output current	10001		14.25		mA
	10010		15.0		
	10011		15.75		
	10100		16.5		
	10101		17.25		
	10110		18.0		
	10111		18.75		
	11000		19.5		
	11001		20.25		
	11010		21.0		
	11011		21.75		
	11100		22.5		
	11101		23.25		
	11110		24.0		
	11111(max current)		24.75		

9.5 Keypad Backlight LED Driver

The keypad backlight driver is constructed with current mirror.

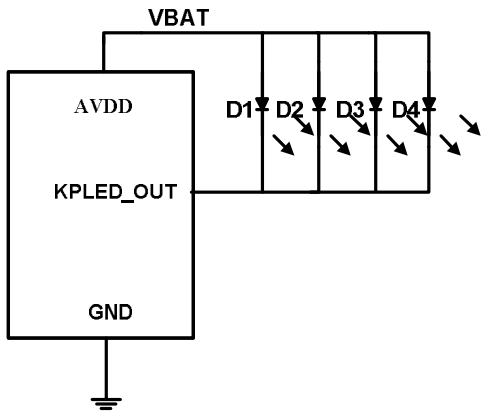


Figure 9-6 Keypad backlight LED driver application

Table 9-4 Performance of Keypad backlight LED driver

Parameter	Conditions/Comments	Min	Typical	Max	Unit
Status after reset	off				
Output current	000(min current) (default)		5		mA
	001		10		
	010		15		
	011		20		
	100		25		
	101		30		
	110		35		
	111		40		

9.6 Vibrator Driver

The vibrator driver is constructed with current mirror.

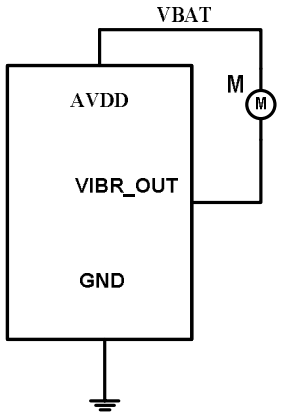


Figure 9-7 Vibrator driver application

Table 9-5 Performance of Vibrator driver

Parameter	Conditions/Comments	Min	Typical	Max	Unit
Status after reset	off				
Output current	0000 (default)		20		mA
	0001		30		
	0010		40		
	0011		50		
	0100		60		
	0101		70		
	0110		80		
	0111		90		
	1000		100		mA
	1001		110		
	1010		120		
	1011		130		
	1100		140		
	1101		150		
	1110		160		
	1111		170		

9.7 UVLO

The UVLO (Under Voltage Lockout) function prevents startup when initial voltage of the main battery is below the 3.1 V threshold. The UVLO circuit is used to provide more stable operation. After turning on power, the UVLO function keeps the internal circuit in the standby state until 128ms after the main battery's voltage reaches the UVLO voltage, there is 3.1V, so as to reduce supply current, avoid mis-operation and prohibit PMU to work when supply is surging. If the main battery's voltage is below 2.7V or above 5.2V for longer than 2ms, the UVLO circuit will give a signal to the internal circuit that the main battery is low/high power, which need to be powered down.

A UVLO filter is designed to remove the glitch under 2ms, and 128ms recovery time is added. Once chip enters UVLO state, it draws very low quiescent current, typically < 50 uA.

The de-glitch function of UVLO can be described as figure16-8:

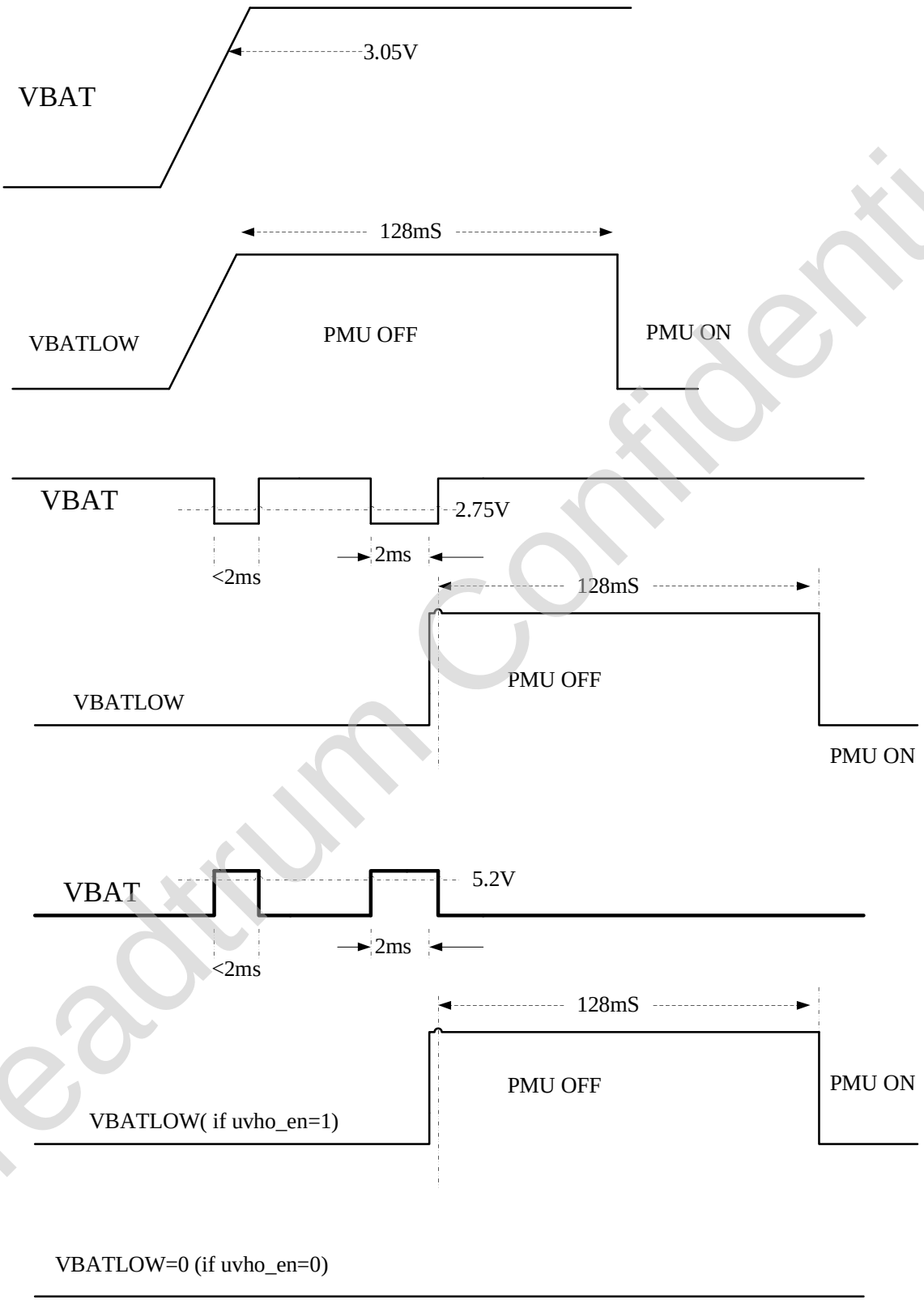


Figure 9-8 UVLO function

9.8 OTP

The OTP (Over Temperature Protection) function in SC6820 will disable all the LDOs except the LDO_RTC if the die temperature exceeds 150 °C. Once the over temperature condition is resolved, a new power on sequence is required to enable the LDOs. And the OTP has 35 °C sluggish.

The OTP function is disabled by default and can be enabled by software.

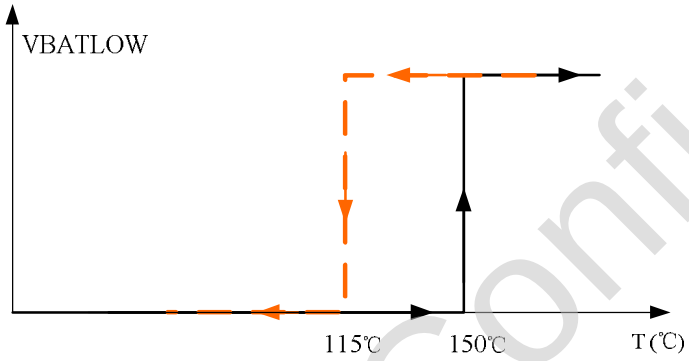


Figure 9-9 OTP operation condition

9.9 Band-Gap

The band gap block provides the first level reference for all LDO's except LDO RTC. When system is reset, it will be on.

Note:

1) When Band-gap is powered off, all LDOs except LDO_RTC will be disabled.
2) When BG is power off, OTP should Power off too. However, when BG is power on, OTP can be either power on or power off.

9.10 Power Control

9.10.1 Power on Procedure

SC6820 can be powered on in four ways, by connecting the battery, by pressing the power button, by inserting the battery charger or by alarm interrupt.

9.10.1.1 Power on by Connecting the Battery

The battery is the master power supply to the entire system. When the battery is connected, the 3.6 V battery voltage should be supplied to the AVDD36 pin.

As the AVDD36 supply voltage goes from 0 to 3.6 V, a power-on-reset (POR) is generated and this POR resets all the control registers, including the one that controls the internal 1.8 V LDO. As soon as the 1.8 V LDO control register is reset, the 1.8 V LDO start to function, providing the 1.8 V power supply to the core. At the end of the POR, basic blocks start to function and the system is considered powered on.

9.10.1.2 Power on by the Power Button

When the system is powered off with the battery still connected, pressing the power button can power on the system. When the power button is pressed, a reset signal is generated and all the control registers get reset, including the one that controls the internal 1.8 V LDO. As soon as the 1.8 V LDO control register is reset, the 1.8 V LDO start to function, providing the 1.8 V power supply to the core. In addition, an interrupt is sent to the MCU. The MCU should check the interrupt source and branch accordingly.

9.10.1.3 Power on by the Charger

When the system is powered off with the battery still connected, inserting the battery charger can also power on the system. When the charger is inserted, a power-on-reset is also triggered, and the system starts with its normal power on procedure. After powered on, the MCU should detect the source of the reset trigger and act accordingly.

9.10.1.4 Power on by Alarm

When the system is powered off with the battery still connected, alarm interrupt from RTC domain can also power on the system. When the alarm interrupt is generated, a power-on-reset is also triggered, and the system starts with its normal power on procedure. After being powered on, the MCU should detect the source of the reset trigger and act accordingly.

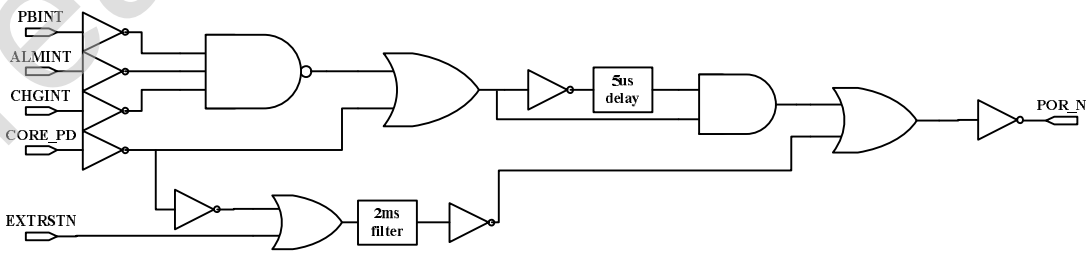
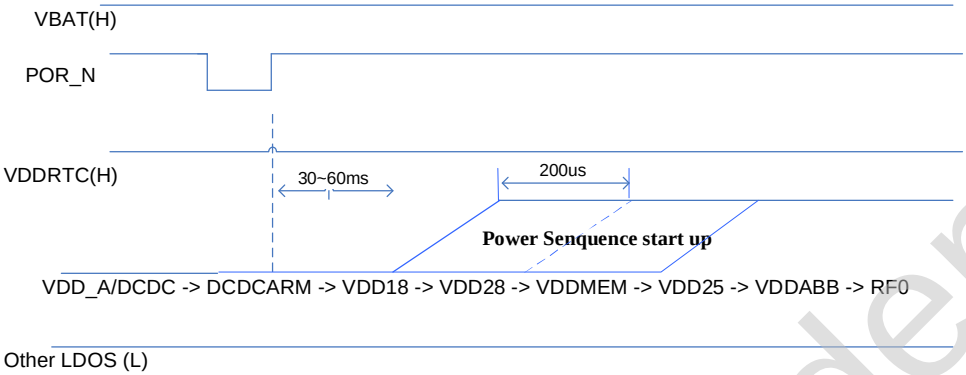


Figure 9-10 Power on reset

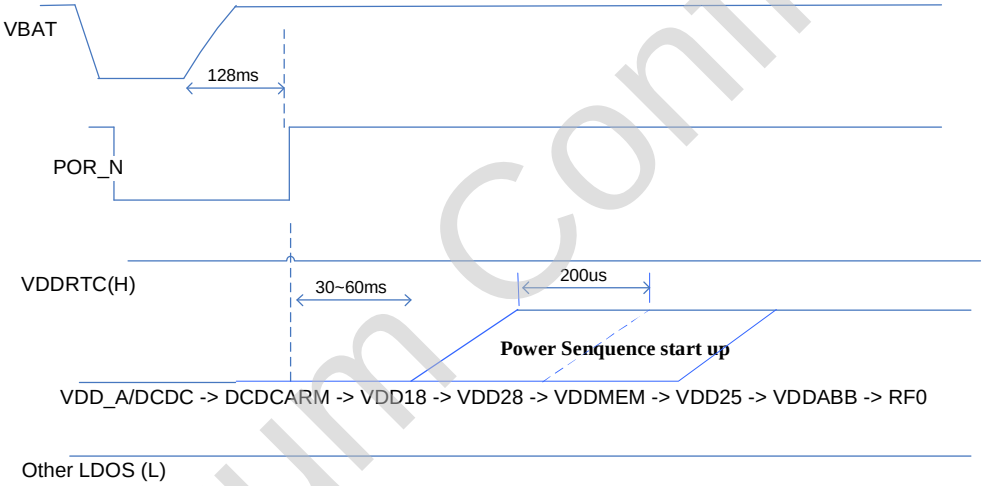
Note1: PBINT, ALMINT, CHGINT symbolize power button interrupt, charger interrupt and charger interrupt separately. CORE_PD is high when the chip is power off. EXTRSTN is the signal from ball B3 and POR_N is internal signal to power up the chip.

9.10.2 Power on Sequence

Normal power up



Power up with backup battery



Power up without backup battery

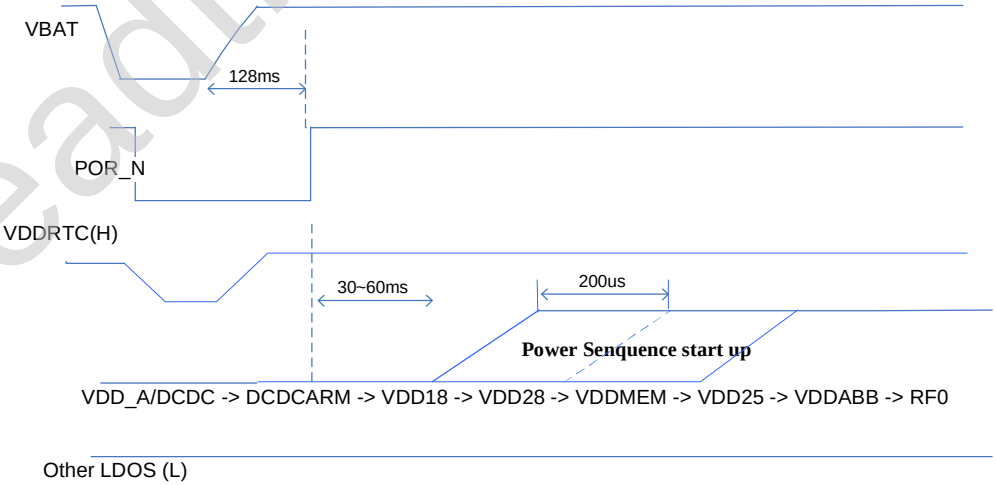


Figure 9-11 Power on sequence

Note: (H) symbolize high voltage, (L) symbolize low voltage

9.10.3 Reset sequence

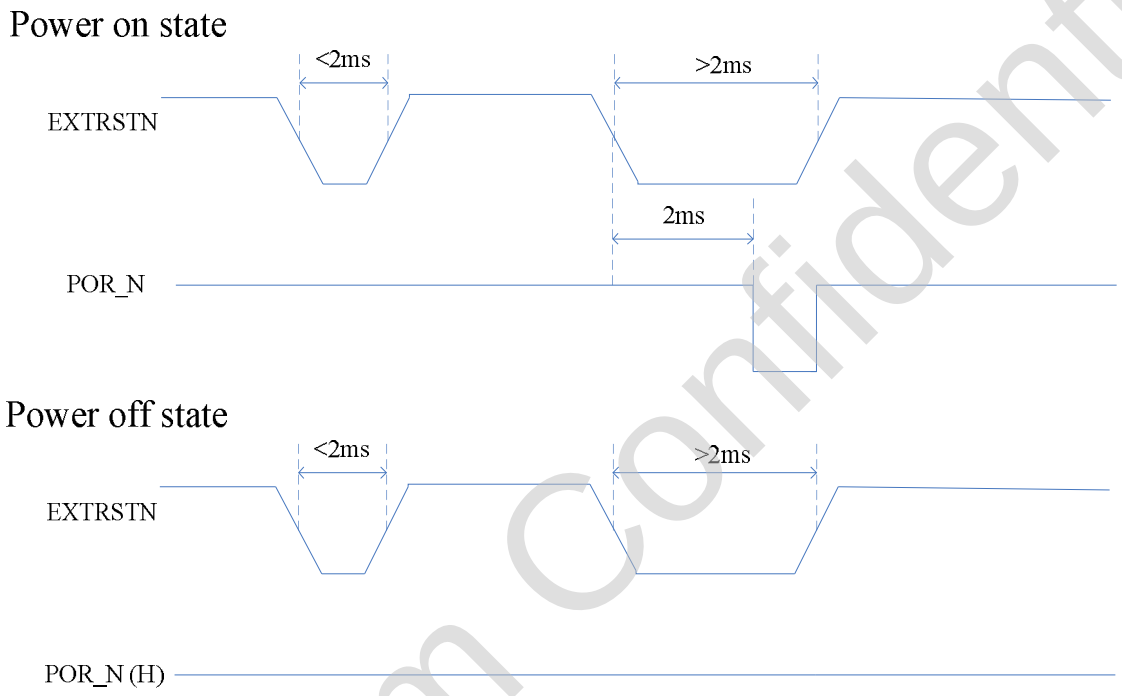


Figure 9-12 Rest sequence

Note1: (H) symbolize high voltage

Note2: Sequence after POR_N, please refer to figure16-10

9.10.4 Clock stable sequence

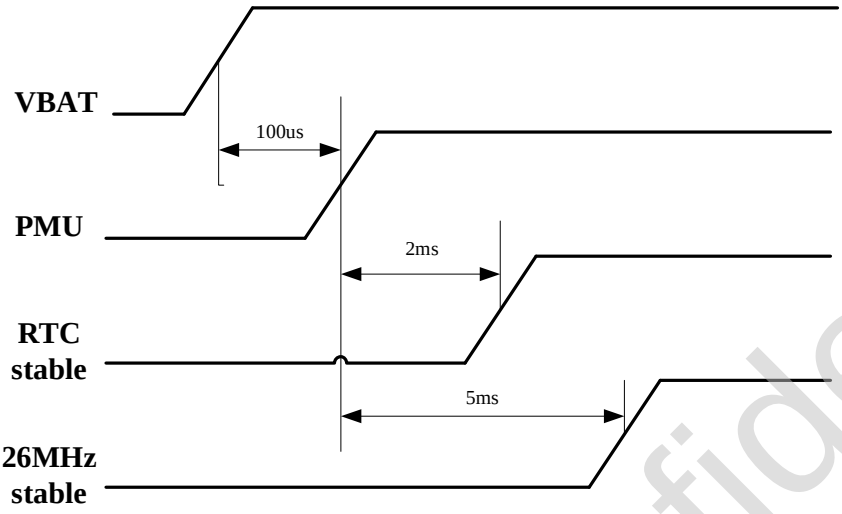


Figure 9-13 Clock stable sequence

10 Analog Control Registers

10.1 Global Register

10.1.1 ARM Side

ARM Base Address: 0x8200_0600

Table 1-1 Analog ARM Global Register

Offset Address	Name	Description
0x00	APB_CLK_EN	APB slave clock enable
0x04	APB_ARM_RST	APB slave ARM soft reset
0x08	LDO_PD_SET	LDO power down set
0x0C	LDO_PD_RST	LDO power down reset
0x10	LDO_PD_CTRL0	LDO power down control0
0x14	LDO_PD_CTRL1	LDO power down control1
0x18	LDO_VCTRL0	LDO voltage control0
0x1C	LDO_VCTRL1	LDO voltage control1
0x20	LDO_VCTRL2	LDO voltage control2
0x24	LDO_VCTRL3	LDO voltage control3
0x28	LDO_VCTRL4	LDO voltage control4
0x2C	LDO_SLP_CTRL0	LDO sleep control0
0x30	LDO_SLP_CTRL1	LDO sleep control1
0x34	LDO_SLP_CTRL2	LDO sleep control2
0x38	DCDC_CTRL	DCDC control
0x3C	DCDC_CTRL_DS	DCDC control in deep sleep
0x40	DCDC_CTRL_CAL	DCDC calibration control
0x44	DCDCARM_CTRL	DCDCARM control

Offset Address	Name	Description
0x48	DCDCARM_CTRL_CAL	DCDCARM calibration control
0x4C	PLL_CTRL	APLL control
0x50	APLLMN	APLL MN control
0x54	APLLWAIT	APLL WAIT control
0x58	RTC_CTRL	RTC OSC/VBAT control
0x5C	TRF_CTRL	Transfer 26M buffer control
0x60	CHGR_CTRL0	Charger control0
0x64	CHGR_CTRL1	Charger control1
0x68	LED_CTRL	LED control
0x6C	VIBRATOR_CTRL0	Vibrator control0
0x70	VIBRATOR_CTRL1	Vibrator control1
0x74	AUDIO_CTRL	Audio general control
0x78	AUDIO_PA_CTRL0	Audio PA control0
0x7C	AUDIO_PA_CTRL1	Audio PA control1
0x80	ANA_MIXED_CTRL	Analog circuit miscellaneous(OTP, BT,26MBUF) control
0x84	ANA_STATUS	Analog circuit（Bonding option, Charger, PA）status
0x88	RST_STATUS	Reset status
0x8C	MCU_WR_PROT	MCU write protection
0x90	VIBR_WR_PROT	VIBR register write protection
0x94	INT_GPI_DEBUG	Analog interrupt and GPI debug
0x98	HWRST_RTC	RTC test register
0x9C	IF_SPR_CTRL	IF_SPR pin control
0xF8	CHIP_ID_LOW	8810 CHIP ID low 16 bits
0xFC	CHIP_ID_HIGH	8810 CHIP ID high 16 bits

10.1.1.1 APB_CLK_EN

Description： APB slave related clock enable

0x0000			APB slave related clock enable (reset 0x0000_0181)													APB_CLK_EN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHGRWDG_EB	CLK_AUXAD_EN	CLK_AUXADC_EN	RTC_TPC_EB	RTC_EIC_EB	RTC_WDG_EB	RTC_RTC_EB	RTC_ARCH_EB	PINREG_EB	GPIO_EB	ADC_EB	TPC_EB	EIC_EB	WDG_EB	RTC_EB	APB_ARCH_EB
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
CHGRWDG_EB	[15]	R/W	1'h0	CHGRWDG APB clock enable
CLK_AUXAD_EN	[14]	R/W	1'h0	Set this bit will enable AUXAD converter clock generation
CLK_AUXADC_EN	[13]	R/W	1'h0	AUXAD controller 6.5M work clock enable
RTC_TPC_EB	[12]	R/W	1'h0	TPC controller RTC clock enable 0: The RTC clock of TPC controller will be off 1: Enable RTC clock of TPC controller
RTC_EIC_EB	[11]	R/W	1'h0	EIC RTC clock enable 0: The RTC clock of EIC will be off 1: Enable RTC clock of EIC
RTC_WDG_EB	[10]	R/W	1'h0	Watch dog RTC clock enable 0: The RTC clock of watch dog will be off 1: Enable RTC clock of watch dog
RTC_RTC_EB	[9]	R/W	1'h0	RTC controller RTC clock enable 0: The RTC clock of RTC controller will be

				off 1: Enable RTC clock of RTC controller
RTC_ARCH_EB	[8]	R/W	1'h1	APB system RTC clock enable 0: disable clock_rtc_arch 1: enable clock_rtc_arch
PINREG_EB	[7]	R/W	1'h1	Pin register APB clock enable
GPIO_EB	[6]	R/W	1'h0	GPIO APB clock enable
ADC_EB	[5]	R/W	1'h0	AUXAD controller APB clock enable
TPC_EB	[4]	R/W	1'h0	Touch panel controller APB clock enable
EIC_EB	[3]	R/W	1'h0	EIC APB clock enable
WDG_EB	[2]	R/W	1'h0	Watch dog APB clock enable
RTC_EB	[1]	R/W	1'h0	RTC controller APB clock enable
APB_ARCH_EB	[0]	R/W	1'h1	APB system clock enable to enable clock for global register, interrupt controller, reset generator Note: This bit could only be modified when MCU_WR_PROT register is released

10.1.1.2 APB_ARM_RST

Description：APB slave ARM soft reset

0x0004			APB slave arm soft reset (reset 0x0000_0000)													APB_ARM_RST
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								GPIO_SOFT_RST	EIC_SOFT_RST	TPC_SOFT_RST	ADC_SOFT_RST	WDG_SOFT_RST	CHGRWDG_SOFT_RST	VBMC_SOFT_RST	RTC_SOFT_RST
Type	RO								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
GPIO_SOFT_RST	[7]	R/W	1'b0	APB slave GPIO soft reset
EIC_SOFT_RST	[6]	R/W	1'b0	APB slave EIC soft reset
TPC_SOFT_RST	[5]	R/W	1'b0	APB slave TPC soft reset
ADC_SOFT_RST	[4]	R/W	1'b0	APB slave ADC soft reset
WDG_SOFT_RST	[3]	R/W	1'b0	APB slave WDG soft reset
CHGRWDG_SOFT_RST	[2]	R/W	1'b0	APB slave CHGRWDG soft reset
VBMC_SOFT_RST	[1]	R/W	1'b0	APB slave VBMC soft reset
RTC_SOFT_RST	[0]	R/W	1'b0	APB slave RTC soft reset

10.1.1.3 LDO_PD_SET

Description：LDO power down set

0x0008			LDO power down set (reset 0x0000_0000)													LDO_PD_SET
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						DCDCARM_PD	LDO_BPVDD25	LDO_BPVDD18	LDO_BPVDD28	LDO_BPAVDDBB	LDO_BPRF1	LDO_BPRF0	LDO_BPMEM	DCDC_PD	PDBG
Type	RO						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:10]	RO	22'h0	Reserved
DCDCARM_PD	[9]	R/W	1'h0	DCDCARM power down
LDO_BPVDD25	[8]	R/W	1'h0	LDO_VDD25_PD. When set, LDO_VDD25 will power down (LDO bypassed).
LDO_BPVDD18	[7]	R/W	1'h0	LDO_VDD18_PD. When set, LDO_VDD18 will power down (LDO bypassed).
LDO_BPVDD28	[6]	R/W	1'h0	LDO_VDD28_PD. When set, LDO_VDD28 will power down (LDO bypassed).
LDO_BPAVDDBB	[5]	R/W	1'h0	LDO_AVDDBB_PD. When set, LDO_AVDDBB will power down (LDO bypassed).
LDO_BPRF1	[4]	R/W	1'h0	LDO_RF1_PD. When set, LDO_RF1 will power down (LDO bypassed).
LDO_BPRF0	[3]	R/W	1'h0	LDO_RF0_PD. When set, LDO_RF0 will power down (LDO bypassed).
LDO_BPMEM	[2]	R/W	1'h0	LDO_MEM power down

DCDC_PD	[1]	R/W	1'h0	DCDC/LDO_DVDD18 power down
PDBG	[0]	R/W	1'h0	Band-Gap power down

10.1.1.4 LDO_PD_RST

Description：LDO power down reset

0x000C			LDO power down reset (reset 0x0000_0000)										LDO_PD_RST			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						DCDCARM_PD_RST	LDO_BPVDD25_RST	LDO_BPVDD18_RST	LDO_BPVDD28_RST	LDO_BPAVDDBB_RST	LDO_BPRF1_RST	LDO_BPRF0_RST	LDO_BPMEM_RST	DCDC_PD_RST	PDBG_RST
Type	RO						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:10]	RO	22'h0	Reserved
DCDCARM_PD_RST	[9]	R/W	1'h0	When set, DCDCARM power on, This bit has higher priority than DCDCARM_ PD.
LDO_BPVDD25_RST	[8]	R/W	1'h0	When set, LDO_VDD25 will power on (LDO bypass reset). This bit has higher priority than LDO_BPVDD25.
LDO_BPVDD18_RST	[7]	R/W	1'h0	When set, LDO_VDD18 will power on (LDO bypass reset). This bit has higher priority than LDO_BPVDD18.
LDO_BPVDD28_RST	[6]	R/W	1'h0	When set, LDO_VDD28 will power on (LDO bypass reset). This bit has higher priority than LDO_BPVDD28.

LDO_BPAVDDBB_RST	[5]	R/W	1'h0	When set, LDO_AVDDBB will power on (LDO bypass reset). This bit has higher priority than LDO_BPAVDDBB.
LDO_BPRF1_RST	[4]	R/W	1'h0	When set, LDO_RF1 will power on (LDO bypass reset). This bit has higher priority than LDO_BPRF1.
LDO_BPRF0_RST	[3]	R/W	1'h0	When set, LDO_RF0 will power on (LDO bypass reset). This bit has higher priority than LDO_BPRF0.
LDO_BPMEM_RST	[2]	R/W	1'h0	When set, LDO_MEM power on, This bit has higher priority than LDOBPMEM.
DCDC_PD_RST	[1]	R/W	1'h0	When set, DCDC/LDO_DVDD18 power on, This bit has higher priority than DCDC_ PD.
PDBG_RST	[0]	R/W	1'h0	When set, Band-Gap power on

10.1.1.5 LDO_PD_CTRL0

Description：LDO power down control0

0x0010	LDO power down control0(reset 0x0000_0000)														LDO_PD_CTRL0	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LDO_BPVB_RST	LDO_BPVB	LDO_BPCAMA_RST	LDO_BPCAMA	LDO_BPCAMD1_RST	LDO_BPCAMD1	LDO_BPCAMD0_RST	LDO_BPCAMD0	LDO_BPSIM1_RST	LDO_BPSIM1	LDO_BPSIM0_RST	LDO_BPSIM0	LDO_BPSDIO0_RST	LDO_BPSDIO0	LDO_BPUSBH_RST	LDO_BPUSBH
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

	[31:16]	RO	16'h0	Reserved
LDO_BPVB_RST	[15]	R/W	1'h0	When set, LDO_VB will power on (LDO bypass reset). This bit has higher priority than LDO_BPVB.
LDO_BPVB	[14]	R/W	1'h0	LDO_VB_PD. When set, LDO_VB will power down (LDO bypassed).
LDO_BPCAMA_RST	[13]	R/W	1'h0	When set, LDO_CAMA will power on (LDO bypass reset). This bit has higher priority than LDO_BPCAMA.
LDO_BPCAMA	[12]	R/W	1'h0	LDO_CAMA_PD. When set, LDO_CAMA will power down (LDO bypassed).
LDO_BPCAMD1_RST	[11]	R/W	1'h0	When set, LDO_CAMD1 will power on (LDO bypass reset). This bit has higher priority than LDO_BPCAMD1.
LDO_BPCAMD1	[10]	R/W	1'h0	LDO_CAMD1_PD. When set, LDO_CAMD1 will power down (LDO bypassed).
LDO_BPCAMD0_RST	[9]	R/W	1'h0	When set, LDO_CAMD0 will power on (LDO bypass reset). This bit has higher priority than LDO_BPCAMD0.
LDO_BPCAMD0	[8]	R/W	1'h0	LDO_CAMD0_PD. When set, LDO_CAMD0 will power down (LDO bypassed).
LDO_BPSIM1_RST	[7]	R/W	1'h0	When set, LDO_SIM1 will power on (LDO bypass reset). This bit has higher priority than LDO_BPSIM1.
LDO_BPSIM1	[6]	R/W	1'h0	LDO_SIM1_PD. When set, LDO_SIM1 will power down (LDO bypassed).
LDO_BPSIM0_RST	[5]	R/W	1'h0	When set, LDO_SIM0 will power on (LDO bypass reset). This bit has higher priority than LDO_BPSIM0.
LDO_BPSIM0	[4]	R/W	1'h0	LDO_SIM0_PD. When set, LDO_SIM0 will power down (LDO bypassed).
LDO_BPSDIO0_RST	[3]	R/W	1'h0	When set, LDO_SDIO0 will power on (LDO bypass reset). This bit has higher priority than LDO_BPSDIO0.

LDO_BPSDIO0	[2]	R/W	1'h0	LDO_SDIO0_PD. When set, LDO_SDIO0 will power down (LDO bypassed).
LDO_BPUSBH_RST	[1]	R/W	1'h0	When set, LDO_USBH will power on (LDO bypass reset). This bit has higher priority than LDO_BPUSBH.
LDO_BPUSBH	[0]	R/W	1'h0	LDO_USBH_PD. When set, LDO_USBH will power down (LDO bypassed).

10.1.1.6 LDO_PD_CTRL1

Description：LDO power down control1

0x0014	LDO power down control1(reset 0x0000_0000)															LDO_PD_CTRL1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						LDO_BPSIM3_RST	LDO_BPSIM3	LDO_BPSIM2_RST	LDO_BPSIM2	LDO_BPWIF1_RST	LDO_BPWIF1	LDO_BPWIF0_RST	LDO_BPWIF0	LDO_BPSDIO1_RST	LDO_BPSDIO1
Type	RO						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:10]	RO	22'h0	Reserved
LDO_BPSIM3_RST	[9]	R/W	1'h0	When set, LDO_SIM3 will power on (LDO bypass reset). This bit has higher priority than LDO_BPSIM3.
LDO_BPSIM3	[8]	R/W	1'h0	LDO_SIM3_PD. When set, LDO_SIM3 will power down (LDO bypassed).
LDO_BPSIM2_RST	[7]	R/W	1'h0	When set, LDO_SIM2 will power on (LDO bypass reset). This bit has higher

				priority than LDO_BPSIM2.
LDO_BPSIM2	[6]	R/W	1'h0	LDO_SIM2_PD. When set, LDO_SIM2 will power down (LDO bypassed).
LDO_BPWIF1_RST	[5]	R/W	1'h0	When set, LDO_WIF1 will power on (LDO bypass reset). This bit has higher priority than LDO_BPWIF1.
LDO_BPWIF1	[4]	R/W	1'h0	LDO_WIF1_PD. When set, LDO_WIF1 will power down (LDO bypassed).
LDO_BPWIF0_RST	[3]	R/W	1'h0	When set, LDO_WIF0 will power on (LDO bypass reset). This bit has higher priority than LDO_BPWIF0.
LDO_BPWIF0	[2]	R/W	1'h0	LDO_WIF0_PD. When set, LDO_WIF0 will power down (LDO bypassed).
LDO_BPSDIO1_RST	[1]	R/W	1'h0	When set, LDO_SDIO1 will power on (LDO bypass reset). This bit has higher priority than LDO_BPSDIO2.
LDO_BPSDIO1	[0]	R/W	1'h0	LDO_SDIO1_PD. When set, LDO_SDIO1 will power down (LDO bypassed).

10.1.1.7 LDO_VCTRL0

Description：LDO voltage control0

0x0018	LDO voltage control0 (reset 0x0000_0000)															LDO_VCTRL0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LDO_AVDDBB_VCTL				LDO_RF1_VCTL				LDO_RF0_VCTL				LDO_RTC_VCTL			
Type	R/W				R/W				R/W				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

	[31:16]	RO	16'h0	Reserved
LDO_AVDDBB_VCTL	[15:12]	R/W	4'h0	LDO_AVDDBB voltage control [15]: ldo_avddbb_b1_rst, set this bit will clear ldo_avddbb_b1 [14]: ldo_avddbb_b1 [13]: ldo_avddbb_b0_rst, set this bit will clear ldo_avddbb_b0 [12]: ldo_avddbb_b0 b1b0: 00-3.0V 01-3.1V 10-2.9V 11-2.8V
LDO_RF1_VCTL	[11:8]	R/W	4'h0	LDO_RF1 voltage control [11]: ldo_rf1_b1_rst, set this bit will clear ldo_rf1_b1 [10]: ldo_rf1_b1 [9]: ldo_rf1_b0_rst, set this bit will clear ldo_rf1_b0 [8]: ldo_rf1_b0 b1b0: 00-2.85V 01-2.95V 10-2.5V 11-1.8V
LDO_RF0_VCTL	[7:4]	R/W	4'h0	LDO_RF0 voltage control [7]: ldo_rf0_b1_rst, set this bit will clear ldo_rf0_b1 [6]: ldo_rf0_b1 [5]: ldo_rf0_b0_rst, set this bit will clear ldo_rf0_b0 [4]: ldo_rf0_b0 b1b0: 00-2.85V 01-2.95V 10-2.75V 11-1.8V
LDO_RTC_VCTL	[3:0]	R/W	4'h0	LDO_RTC voltage control [3]: ldo_rtc_b1_rst, set this bit will clear ldo_rtc_b1 [2]: ldo_rtc_b1 [1]: ldo_rtc_b0_rst, set this bit will clear ldo_rtc_b0 [0]: ldo_rtc_b0 b1b0: 00-1.8V 01-1.7V 10-1.6V 11-1.5V

10.1.1.8 LDO_VCTRL1

Description：LDO voltage control1

0x001C			LDO voltage control1 (reset 0x0000_0000)													LDO_VCTRL1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LDO_SDIO0_VCTL				LDO_VB_VCTL				LDO_SIM1_VCTL				LDO_SIM0_VCTL			
Type	R/W				R/W				R/W				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
LDO_SDIO0_VCTL	[15:12]	R/W	4'h0	LDO_SDIO0 voltage control [15]: ldo_sdio0_b1_rst, set this bit will clear ldo_sdio0_b1 [14]: ldo_sdio0_b1 [13]: ldo_sdio0_b0_rst, set this bit will clear ldo_sdio0_b0 [12]: ldo_sdio0_b0 b1b0: 00-2.8V 01-3.0V 10-2.5V 11-1.8V
LDO_VB_VCTL	[11:8]	R/W	4'h0	LDO_VB voltage control [11]: ldo_vb_b1_rst, set this bit will clear ldo_vb_b1 [10]: ldo_vb_b1 [9]: ldo_vb_b0_rst, set this bit will clear ldo_vb_b0 [8]: ldo_vb_b0 b1b0: 00-3.3V 01-3.4V 10-3.2V 11-2.9V
LDO_SIM1_VCTL	[7:4]	R/W	4'h0	LDO_SIM1 voltage control

				[7]: ldo_sim1_b1_rst, set this bit will clear ldo_sim1_b1 [6]: ldo_sim1_b1 [5]: ldo_sim1_b0_rst, set this bit will clear ldo_sim1_b0 [4]: ldo_sim1_b0 b1b0: 00-1.8V 01-2.9V 10-3.0V 11-3.1V
LDO_SIM0_VCTL	[3:0]	R/W	4'h0	LDO_SIM0 voltage control [3]: ldo_sim0_b1_rst, set this bit will clear ldo_sim0_b1 [2]: ldo_sim0_b1 [1]: ldo_sim0_b0_rst, set this bit will clear ldo_sim0_b0 [0]: ldo_sim0_b0 b1b0: 00-1.8V 01-2.9V 10-3.0V 11-3.1V

10.1.1.9 LDO_VCTRL2

Description：LDO voltage control2

0x0020			LDO voltage control2 (reset 0x0000_0000)												LDO_VCTRL2	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LDO_USBH_VCTL				LDO_CAMA_VCTL				LDO_CAMD1_VCTL				LDO_CAMD0_VCTL			
Type	R/W				R/W				R/W				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
LDO_USBH_VCTL	[15:12]	R/W	4'h0	LDO_USBH voltage control

				[15]: ldo_usbh_b1_rst, set this bit will clear ldo_usbh_b1 [14]: ldo_usbh_b1 [13]: ldo_usbh_b0_rst, set this bit will clear ldo_usbh_b0 [12]: ldo_usbh_b0 b1b0: 00-3.3V 01-3.4V 10-3.2V 11-3.1V
LDO_CAMA_VCTL	[11:8]	R/W	4'h0	LDO_CAMA voltage control [11]: ldo_cama_b1_rst, set this bit will clear ldo_cama_b1 [10]: ldo_cama_b1 [9]: ldo_cama_b0_rst, set this bit will clear ldo_cama_b0 [8]: ldo_cama_b0 b1b0: 00-2.8V 01-3.0V 10-2.5V 11-1.8V
LDO_CAMD1_VCTL	[7:4]	R/W	4'h0	LDO_CAMD1 voltage control [7]: ldo_camd1_b1_rst, set this bit will clear ldo_camd1_b1 [6]: ldo_camd1_b1 [5]: ldo_camd1_b0_rst, set this bit will clear ldo_camd1_b0 [4]: ldo_camd1_b0 b1b0: 00-2.8V 01-3.8V 10-1.8V 11-1.2V
LDO_CAMD0_VCTL	[3:0]	R/W	4'h0	LDO_CAMD0 voltage control [3]: ldo_camd0_b1_rst, set this bit will clear ldo_camd0_b1 [2]: ldo_camd0_b1 [1]: ldo_camd0_b0_rst, set this bit will clear ldo_camd0_b0 [0]: ldo_camd0_b0 b1b0: 00-1.8V 01-2.8V 10-1.5V 11-1.3V

10.1.1.10 LDO_VCTRL3

Description：LDO voltage control3

0x0024	LDO voltage control3 (reset 0x0000_0000)												LDO_VCTRL3			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LDO_SDIO1_VCTL				LDO_VDD25_VCTL				LDO_VDD18_VCTL				LDO_VDD28_VCTL			
Type	R/W				R/W				R/W				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
LDO_SDIO1_VCTL	[15:12]	R/W	4'h0	LDO_SDIO1 voltage control [15]: ldo_sdio1_b1_rst, set this bit will clear ldo_sdio1_b1 [14]: ldo_sdio1_b1 [13]: ldo_sdio1_b0_rst, set this bit will clear ldo_sdio1_b0 [12]: ldo_sdio1_b0 b1b0: 00-2.8V 01-3.0V 10-2.5V 11-1.8V
LDO_VDD25_VCTL	[11:8]	R/W	4'h0	LDO_VDD25 voltage control [11]: ldo_vdd25_b1_rst, set this bit will clear ldo_vdd25_b1 [10]: ldo_vdd25_b1 [9]: ldo_vdd25_b0_rst, set this bit will clear ldo_vdd25_b0 [8]: ldo_vdd25_b0 b1b0: 00-2.5V 01-2.75V 10-3.0V 11-2.9V
LDO_VDD18_VCTL	[7:4]	R/W	4'h0	LDO_VDD18 voltage control

				[11]: ldo_vdd18_b1_rst, set this bit will clear ldo_vdd18_b1 [10]: ldo_vdd18_b1 [9]: ldo_vdd18_b0_rst, set this bit will clear ldo_vdd18_b0 [8]: ldo_vdd18_b0 b1b0: 00-1.8V 01-2.8V 10-1.5V 11-1.2V
LDO_VDD28_VCTL	[3:0]	R/W	4'h0	LDO_VDD28 voltage control [11]: ldo_vdd28_b1_rst, set this bit will clear ldo_vdd28_b1 [10]: ldo_vdd28_b1 [9]: ldo_vdd28_b0_rst, set this bit will clear ldo_vdd28_b0 [8]: ldo_vdd28_b0 b1b0: 00-2.8V 01-3.0V 10-2.65V 11-1.8V

10.1.1.11 LDO_VCTRL4

Description：LDO voltage control4

0x0028	LDO voltage control4 (reset 0x0000_0000)												LDO_VCTRL4			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LDO_SIM3_VCTL				LDO_SIM2_VCTL				LDO_WIF1_VCTL				LDO_WIF0_VCTL			
Type	R/W				R/W				R/W				R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved

LDO_SIM3_VCTL	[15:12]	R/W	4'h0	LDO_SIM3 voltage control [15]: ldo_sim3_b1_rst, set this bit will clear ldo_sim3_b1 [14]: ldo_sim3_b1 [13]: ldo_sim3_b0_rst, set this bit will clear ldo_sim3_b0 [12]: ldo_sim3_b0 b1b0: 00-2.8V 01-3V 10-1.8V 11-1.2V
LDO_SIM2_VCTL	[11:8]	R/W	4'h0	LDO_SIM2 voltage control [11]: ldo_sim2_b1_rst, set this bit will clear ldo_sim2_b1 [10]: ldo_sim2_b1 [9]: ldo_sim2_b0_rst, set this bit will clear ldo_sim2_b0 [8]: ldo_sim2_b0 b1b0: 00-2.8V 01-3V 10-1.8V 11-1.2V
LDO_WIF1_VCTL	[7:4]	R/W	4'h0	LDO_WIF1 voltage control [7]: ldo_wif1_b1_rst, set this bit will clear ldo_wif1_b1 [6]: ldo_wif1_b1 [5]: ldo_wif1_b0_rst, set this bit will clear ldo_wif1_b0 [4]: ldo_wif1_b0 b1b0: 00-2.8V 01-3.3V 10-1.8V 11-1.2V
LDO_WIF0_VCTL	[3:0]	R/W	4'h0	LDO_WIF0 voltage control [3]: ldo_wif0_b1_rst, set this bit will clear ldo_wif0_b1 [2]: ldo_wif0_b1 [1]: ldo_wif0_b0_rst, set this bit will clear ldo_wif0_b0 [0]: ldo_wif0_b0 b1b0: 00-2.8V 01-3.3V 10-1.8V 11-1.2V

10.1.1.12 LDO_SLP_CTRL0

Description：LDO sleep control0

0x002C			LDO sleep control0 (reset 0x0000_A7FF)													LDO_SLP_CTRL0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FSM_LDOSDIO1_BP_EN	Reserved	FSM_LDOVDD25_BP_EN	FSM_LDOVDD18_BP_EN	FSM_LDOVDD28_BP_EN	FSM_LDOAVDDBB_BP_EN	FSM_LDOSDIO0_BP_EN	FSM_LDOVBP_EN	FSM_LDOCAMA_BP_EN	FSM_LDOCAMD1_BP_EN	FSM_LDOCAMD0_BP_EN	FSM_LDOUSBH_BP_EN	FSM_LDO_SIM1_BP_EN	FSM_LDO_SIM0_BP_EN	FSM_LDO_RF1_BP_EN	FSM_LDO_RF0_BP_EN
Type	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
FSM_LDOSDIO1_BP_EN	[15]	R/W	1'h1	When set, LDOSDIO1 automatically power down in chip sleep mode(FSM_SLPPD_EN should be set)
	[14]	RO	1'h0	Reserved
FSM_LDOVDD25_BP_EN	[13]	R/W	1'h1	When set, LDOVDD25 automatically power down in chip sleep mode(FSM_SLPPD_EN should be set)
FSM_LDOVDD18_BP_EN	[12]	R/W	1'h0	When set, LDOVDD18 power down if FSM_SLPPD_EN is active.
FSM_LDOVDD28_BP_EN	[11]	R/W	1'h0	When set, LDOVDD28 power down if FSM_SLPPD_EN is active.

FSM_LDOAVDDBB_BP_EN	[10]	R/W	1'h1	When set, LDOAVDDBB will power down if XTLEN is low(FSM_SLPPD_EN should be set);
FSM_LDOSDIO0_BP_EN	[9]	R/W	1'h1	When set, LDOSDIO0 automatically power down in chip sleep mode(FSM_SLPPD_EN should be set)
FSM_LDOVB_BP_EN	[8]	R/W	1'h1	When set, LDOVB automatically power down in chip sleep mode(FSM_SLPPD_EN should be set)
FSM_CAMA_BP_EN	[7]	R/W	1'h1	When set, LDOCAMA automatically power down in chip sleep mode(FSM_SLPPD_EN should be set)
FSM_CAMD1_BP_EN	[6]	R/W	1'h1	When set, LDOCAMD1 automatically power down in chip sleep mode(FSM_SLPPD_EN should be set)
FSM_CAMD0_BP_EN	[5]	R/W	1'h1	When set, LDOCAMD0 automatically power down in chip sleep mode(FSM_SLPPD_EN should be set)
FSM_USBH_BP_EN	[4]	R/W	1'h1	When set, LDOUSB automatically power down in chip sleep mode(FSM_SLPPD_EN should be set)
FSM_SIM1_BP_EN	[3]	R/W	1'h1	When set, LDOSIM1 automatically power down in chip sleep mode(FSM_SLPPD_EN should be set)
FSM_SIM0_BP_EN	[2]	R/W	1'h1	When set, LDOSIM0 automatically power down in chip sleep mode(FSM_SLPPD_EN should be set)
FSM_RF1_BP_EN	[1]	R/W	1'h1	When set, LDORF1 will power down if XTLEN is low(FSM_SLPPD_EN

				should be set);
FSM_RF0_BP_EN	[0]	R/W	1'h1	When set, LDORF0 will power down if XTLEN is low(FSM_SLPPD_EN should be set);

10.1.1.13 LDO_SLP_CTRL1

Description：LDO sleep control1

0x0030	LDO sleep control1 (reset 0x0000_701F)														LDO_SLP_CTRL1	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FSM_SLPPD_EN	ARMDCDC_PWR_ON_DLY			Reserved							FSM_DCDCARM_BP_EN	FSM_SIM3_BP_EN	FSM_SIM2_BP_EN	FSM_WIF1_BP_EN	FSM_WIF0_BP_EN
Type	R/W	R/W			RO							R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
FSM_SLPPD_EN	[15]	R/W	1'h0	When set, LDOSIM0, LDOSIM1, LDOUSBH, LDOCAMD1, LDOCAMD0, LDOCAMA, LDOVB, LDOSDIO, LDOVDD25, LDOSDIO1, LDOWIF0, LDOWIF1, LDOSIM2, LDOSIM3, DCDCARM automatically power down in chip sleep mode
ARMDCDC_PWR_ON_DLY	[14:12]	R/W	3'h7	
	[11:5]	R/W	10'h0	Reserved

FSM_DCDCARM_BP_EN	[4]	R/W	1'h1	When set, DCDCARM will power down (FSM_SLPPD_EN should be set);
FSM_SIM3_BP_EN	[3]	R/W	1'h1	When set, LDOSIM3 will power down (FSM_SLPPD_EN should be set);
FSM_SIM2_BP_EN	[2]	R/W	1'h1	When set, LDOSIM2 will power down (FSM_SLPPD_EN should be set);
FSM_WIF1_BP_EN	[1]	R/W	1'h1	When set, LDOWIF1 will power down (FSM_SLPPD_EN should be set);
FSM_WIF0_BP_EN	[0]	R/W	1'h1	When set, LDOWIF0 will power down (FSM_SLPPD_EN should be set);

10.1.1.14 LDO_SLP_CTRL2

Description：LDO sleep control2

0x0034	LDO sleep control2(reset 0x0000_FFFF)												LDO_SLP_CTRL2			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ARMDCDC_ISO_ON_NUM								ARMDCDC_ISO_OFF_NUM							
Type	R/W								R/W							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
ARMDCDC_ISO_ON_NUM	[15:8]	R/W	8'hff	Set CLK32K cycles between pd & iso signal when ARMDCDC powered down
ARMDCDC_ISO_OFF_NUM	[7:0]	R/W	8'hff	Set CLK32K cycles between iso &

				pd signal when ARMDCDC powered on.

10.1.1.15 DCDC_CTRL

Description：DCDC control

0x0038	DCDC control (reset 0x0000_0000)												DCDC_CTRL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		DCDC_RESERVE_RST	DCDC_RESERVE	DCDC_DEDTDELAY_RST	DCDC_DEDTDELAY	DCDC_DEDTEN_RST	DCDC_DEDTEN	Reserved	DCDC_CTL_40NM_RST			Reserved	DCDC_CTL_40NM		
Type	RO		R/W	R/W	R/W	R/W	R/W	R/W	RO	R/W			RO	R/W		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:14]	RO	18'h0	Reserved
DCDC_RESERVE_RST	[13]	R/W	1'h0	Set this bit will reset DCDC_RESERVE to 0. This bit has higher priority than DCDC_RESERVE.
DCDC_RESERVE	[12]	R/W	1'h0	DCDC reserve control bit
DCDC_DEDTDELAY_RST	[11]	R/W	1'h0	Set this bit will reset DCDC_DEDTDELAY to 0. This bit has higher priority than DCDC_DEDTDELAY.

DCDC_DEDTDELAY	[10]	R/W	1'h0	DCDC decrease dead-time delay control bit
DCDC_DEDTEN_RST	[9]	R/W	1'h0	Set this bit will reset DCDC_DEDTEN to 0. This bit has higher priority than DCDC_DEDTEN.
DCDC_DEDTEN	[8]	R/W	1'h0	DCDC decrease dead-time enable, High effective
	[7]	RO	1'h0	Reserved
DCDC_CTL_40NM_RST	[6:4]	R/W	3'h0	Set each bit will reset relative bit of DCDC_CTL_40NM
	[3]	RO	1'b0	Reserved
DCDC_CTL_40NM	[2:0]	R/W	3'h0	DC-DC converter control bits(process-40nm) 000: 0.65V 001: 0.7V 010: 0.8V 011: 0.9V 100: 1.0V 101: 1.1V(default) 110: 1.2V 111: 1.3V

10.1.1.16 DCDC_CTRL_DS

Description：DCDC control in deep sleep.

0x003C	DCDC control in deep sleep(reset 0x0000_0300)	DCDC_CTRL_DS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DCDC_LVL_DLY								Reserved	DCDC_CTL_40NM_DS_RST			Reserved	DCDC_CTL_40NM_DS		
Type	R/W								RO	R/W			RO	R/W		
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
DCDC_LVL_DLY	[15:8]	R/W	8'h3	40nm voltage drop count delay time
	[7]	RO	1'b0	Reserved
DCDC_CTL_40NM_DS_RST	[6:4]	R/W	3'h0	Set each bit will reset relative bit of DCDC_CTL_40NM_DS
	[3]	RO	1'b0	Reserved
DCDC_CTL_40NM_DS	[2:0]	R/W	3'h0	DC-DC converter control bits(process-40nm) 000: 0.65V 001: 0.7V 010: 0.8V 011: 0.9V(default) 100: 1.0V 101: 1.1V 110: 1.2V 111: 1.3V

10.1.1.17 DCDC_CTRL_CAL

Description：DCDC calibration control

0x0040	DCDC calibration control(reset 0x0000_0000)												DCDC_CTRL_CAL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			DCDC_CAL_RST					Reserved			DCDC_CAL				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:13]	RO	19'h0	Reserved
DCDC_CAL_RST	[12:8]	R/W	5'h0	Set each bit will reset relative bit of DCDC_CAL
	[7:5]	RO	1'b0	Reserved
DCDC_CAL	[4:0]	R/W	5'h0	DCDC calibration control bits, (default 00000) Small adjust voltage: 100/32 mv

10.1.1.18 DCDCARM_CTRL

Description：DCDCARM control

0x0044			DCDCARM control (reset 0x0000_0000)													DCDC_CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		DCDCARM_RESERVE_RST	DCDCARM_RESERVE	DCDCARM_DEDTDELAY_RST	DCDCARM_DEDTDELAY	DCDCARM_DEDTEN_RST	DCDCARM_DEDTEN	Reserved	DCDCARM_CTL_RST			Reserved	DCDCARM_CTL		
Type	RO		R/W	R/W	R/W	R/W	R/W	R/W	RO	R/W			RO	R/W		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:14]	RO	18'h0	Reserved
DCDCARM_RESERVE_RST	[13]	R/W	1'h0	Set this bit will reset DCDCARM_RESERVE to 0. This bit has higher priority than DCDCARM_RESERVE.
DCDCARM_RESERVE	[12]	R/W	1'h0	DCDCARM reserve control bit
DCDCARM_DEDTDELAY_RST	[11]	R/W	1'h0	Set this bit will reset DCDCARM_DEDTDELAY to 0. This bit has higher priority than DCDCARM_DEDTDELAY.
DCDCARM_DEDTDELAY	[10]	R/W	1'h0	DCDCARM decrease dead-time delay control bit
DCDCARM_DEDTEN_RST	[9]	R/W	1'h0	Set this bit will reset DCDCARM_DEDTEN to 0. This bit has higher priority than

				DCDCARM_DEDTEN.
DCDCARM_DEDTEN	[8]	R/W	1'h0	DCDCARM decrease dead-time enable,high effective
	[7]	RO	1'h0	Reserved
DCDCARM_CTL_RST	[6:4]	R/W	3'h0	Set each bit will reset relative bit of DCDCARM_CTL
	[3]	RO	1'b0	Reserved
DCDCARM_CTL	[2:0]	R/W	3'h0	DC-DC ARM converter control bits 000: 0.65V 001: 0.7V 010: 0.8V 011: 0.9V 100: 1.0V 101: 1.1V 110: 1.2V(default) 111: 1.3V

10.1.1.19 DCDCARM_CTRL_CAL

Description：DCDCARM calibration control

0x0048			DCDCARM calibration control(reset 0x0000_0000)										DCDCARM_CTRL_CAL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			DCDCARM_CAL_RST					Reserved			DCDCARM_CAL				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:13]	RO	19'h0	Reserved
DCDCARM_CAL_RST	[12:8]	R/W	5'h0	Set each bit will reset relative bit of DCDCARM_CAL
	[7:5]	RO	1'b0	Reserved
DCDCARM_CAL	[4:0]	R/W	5'h0	DCDCARM calibration control bits, (default 00000) Small adjust voltage: 100/32 mv

10.1.1.20 PLL_CTRL

Description：PLL control

0x004C	PLL control (reset 0x0000_0004)												PLL_CTRL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												APLLMN_WE	APLL_PD_EN	APLL_FORCE_PD	APLL_FORCE_PD_EN
Type	RO												R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:4]	RO	28'h0	Reserved
APLL_MN_WE	[3]	R/W	1'h0	APLL MN register write enable
APLL_PD_EN	[2]	R/W	1'h1	If true, chip sleep will make APLL power down

APLL_FORCE_PD	[1]	R/W	1'h0	APLL force power down This signal will be active only when APLL_FORCE_PD_EN is set;
APLL_FORCE_PD_EN	[0]	R/W	1'h0	Enable software to power down APLL; This signal should be set at first so that APLL_FORCE_PD will be active

10.1.1.21 APLLMN

Description：APLL MN control

0x0050	APLLMN control (reset 0x0000_68C0)												APLLMN			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	APLLM					APLLN										
Type	R/W					R/W										
Reset	0	1	1	0	1	0	0	0	1	1	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
APLLM	[15:11]	R/W	5'hD	
APLLN	[10:0]	R/W	11'hC0	

APLL frequency = 26 MHz * N / M

ARM can only write this register when PLL_CTRL [3], apllmn_we is high.

10.1.1.22 APLLWAIT

Description：APLL WAIT control

0x0054	APLL WAIT control (reset 0x0000_0032)														APLLWAIT	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								APLL_WAIT							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
APLLWAIT	[7:0]	R/W	8'h32	Number of 26 MHz cycles to wait for APLL to stabilize. The default is about 2 us (0x32).

Note: ARM can only write this register when PLL_CTRL [3], apllmn_we is high.

10.1.1.23 RTC_CTRL

Description：RTC control

0x0058	RTC control (reset 0x0000_0000)														RTC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VBATBK_RES				VBATBK_V				32K_START_CUR							
Type	R/W				R/W				R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
VBATBK_RES	[15:12]	R/W	4'h0	Backup battery output resistor program bits [15]: vbatbk_res_b1_rst, set this bit will clear vbatbk_res_b1 [14]: vbatbk_res_b1 [13]: vbatbk_res_b0_rst, set this bit will clear vbatbk_res_b0 [12]: vbatbk_res_b0 b1b0: 00-200Ω 01-500Ω 10-1.5KΩ 11-2 KΩ
VBATBK_V	[11:8]	R/W	4'h0	Backup battery output program bits [15]: vbatbk_v_b1_rst, set this bit will clear vbatbk_v_b1 [14]: vbatbk_v_b1 [13]: vbatbk_v_b0_rst, set this bit will clear vbatbk_v_b0 [12]: vbatbk_v_b0 b1b0: 00-2.6 01-2.8 10-3.0 11-3.2
32K_START_CUR	[7:0]	R/W	8'h0	This register field controls the 32 kHz oscillator start up current. [7]: XOSC32K_CTRL[3]_RST [6]: XOSC32K_CTRL[3] [5]: XOSC32K_CTRL[2]_RST [4]: XOSC32K_CTRL[2] [3]: XOSC32K_CTRL[1]_RST [2]: XOSC32K_CTRL[1] [1]: XOSC32K_CTRL[0]_RST [0]: XOSC32K_CTRL[0]

XOSC32K_CTRL[3:0]	Start up current
0000	0.6 uA
0001	1.8 uA

0011	4.2 uA
0111	7.8 uA
1111	13.8 uA

10.1.1.24 TRF_CTRL

Description：Transfer 26M buffer control

0x005C			Transfer 26M buffer control (reset 0x0000_0307)										TRF_CTRL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TRF_RESERVE				Reserved		CLK26M_NORMAL_EN	TRF_RC_CAP_EN	TRF_DRIVE_RC_SEL		TRF_TRI_DR		TRF_DCSETUPPADB_EN	TRF_RECTMODEPADB_PD	TRF_RECTMODEPADA_PD	TRF_TRIMODE_PD
Type	R/W				RO		R/W	R/W	R/W		R/W		R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
TRF_RESERVE	[15:12]	R/W	4'h0	26Mhz Buffer Transfer Reserve bits
	[11:10]	RO	2'h0	Reserved
CLK26M_NORMAL_EN	[9]	R/W	1'h1	CLK26M normal path enable: 1: CLK26M digital pad transfer 26M CLK; 0: CLK26M digital pad not transfer 26M CLK;

TRF_RC_CAP_EN	[8]	R/W	1'h1	PAD inner CAP select, 1: 1pf; 0:bypass
TRF_DRIVE_RC_SEL	[7:6]	R/W	2'h0	PAD bypass resistor control REG, 00: 3K; 01: 2K, 10: 1K, 11:bypass
TRF_TRI_DR	[5:4]	R/W	2'h0	Triangle wave 26Mhz buffer output wave
TRF_DCSETUPPADB_EN	[3]	R/W	1'h0	PADB DC output enable, high effective
TRF_RECTMODEPADB_PD	[2]	R/W	1'h1	PADB Rectangle wave power down, high effective
TRF_RECTMODEPADA_PD	[1]	R/W	1'h1	PADA Rectangle wave power down, high effective
TRF_TRIMODE_PD	[0]	R/W	1'h1	Triangle wave 26Mhz buffer power down, high effective

10.1.1.25 CHGR_CTRL0

Description：Charger control0

0x0060	Charger control0 (reset 0x0000_0000)												CHGR_CTRL0			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			RECHG	CHGR_PWM_EN_RST	CHGR_PWM_EN	CHGR_RTCCTL						USB_500MA_EN_RST	USB_500MA_EN	ADAPTER_EN_RST	ADAPTER_EN
Type	RO			R/W	R/W	R/W	R/W						R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:13]	RO	19'h0	Reserved
RECHG	[12]	R/W	1'h0	Main battery recharge control
CHGR_PWM_EN_RST	[11]	R/W	1'h0	When set, limited current charger is disabled. This bit has higher priority than CHGR_PWM_EN.
CHGR_PWM_EN	[10]	R/W	1'h0	Limited current charger enable
CHGR_RTCCTL	[9:4]	R/W	6'h0	CHGR_RTCCTRL[4:0], charger control. This value will be stored in RTC domain register and will not clear after chip power down. Bit[5] 0: keep the design on 6610 1: the V&I curve is sharp than 6610 in CV mode. Bit[4]: Charger power down Bit[3:2]: Adapter charger current 00: 400mA (default) 01: 600mA 10: 800mA 11: 1000mA Bit[1:0]: USB charging current 00: 300mA (default) 01: 400mA 10: 500mA 11: 500mA
USB_500MA_EN_RST	[3]	R/W	1'h0	When set, 500MA USB charge mode is disabled. This bit has higher priority than USB_500MA_EN.
USB_500MA_EN	[2]	R/W	1'h0	500MA USB charge mode enable.
ADATPER_EN_RST	[1]	R/W	1'h0	When set, adapter charge mode is disabled. This bit has higher priority than ADAPTER_EN.
ADATPER_EN	[0]	R/W	1'h0	Adapter charge mode enable

10.1.1.26 CHGR_CTRL1

Description：Charger control1

0x0064	Charger control1 (reset 0x0000_0000)														CHGR_CTRL1	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved									CHGR_CTL						
Type	RO									R/W						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:7]	RO	25'h0	Reserved
CHGR_CTL	[6:0]	R/W	7'h0	Charger control bits Bit[6] is the CHGR_PWM signal Bit[5]: Battery sense offset 0: VL=4v 1: VL=4.1v Bit[4:0]: Battery sense DAC

10.1.1.27 LED_CTRL

Description：LED control

0x0068			LED control (reset 0x0000_0000)													LED_CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			KPLED_PD_RST	KPLED_PD	KPLED_V			Reserved	WHTLED_PD_RST	WHTLED_PD	WHTLED_V				
Type	RO			R/W	R/W	R/W			RO	R/W		R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:13]	RO	19'h0	Reserved
KPLED_PD_RST	[12]	R/W	1'h0	Set this bit will power on the keypad LED. This bit has higher priority than KPLED_PD.
KPLED_PD	[11]	R/W	1'h0	Keypad LED power down
KPLED_V	[10:8]	R/W	3'h0	Keypad LED current control bit. 8 steps Min current: 5mA ("000") Max current: 40mA("111")
	[7]	RO	1'h0	Reserved
WHTLED_PD_RST	[6]	R/W	1'h0	Set this bit will power on the white LED. This bit has higher priority than WHTLED_PD.(WDG reset not active)
WHTLED_PD	[5]	R/W	1'h0	White LED power down(WDG reset not active);
WHTLED_V	[4:0]	R/W	5'h0	White LED current control bit. 32 steps. Min current: 1/2mA ("00000") One step is 1/2mA(WDG reset not active)

10.1.1.28 VIBRATOR_CTRL0

Description：Vibrator control0(Note: this register could only be access when VIBR_WR_PROT released)

0x006C			Vibrator control0 (reset 0x0000_0000)										VIBRATOR_CTRL0			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VIBR_STABLE_V_B				VIBR_INIT_V_A				VIBR_V_BP				VIBR_PD_RST	VIBR_PD	VIBR_BP_EN	RTC_VIBR_EB
Type	R/W				R/W				R/W				R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
VIBR_STABLE_V_B	[15:12]	R/W	4'h0	Vibrator stable current control bit
VIBR_INIT_V_A	[11:8]	R/W	4'h0	Vibrator initial current control bit
VIBR_V_BP	[7:4]	R/W	4'h0	Current Control bit. 8 steps Min current: 20mA ("0000") Max current: 170mA("1111")
VIBR_PD_RST	[3]	R/W	1'h0	Set this bit will power on the vibrator. This bit has higher priority than VIBR_PD.
VIBR_PD	[2]	R/W	1'h0	Vibrator power down
VIBR_BP_EN	[1]	R/W	1'h0	Vibrator current control circuit bypass enable: software control current directly through VIBR_BP_V register
RTC_VIBR_EB	[0]	R/W	1'h0	Vibrator current control circuit 32K clock enable

10.1.1.29 VIBRATOR_CTRL1

Description：Vibrator control1 (Note: this register could only be access when VIBR_WR_PROT released)

0x0070	Vibrator control1 (reset 0x0000_0000)												VIBRATOR_CTRL1			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VIBR_CONVERT_V_COUNT															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
VIBR_CONVERT_V_COUNT	[15:0]	R/W	16'h0	Vibrator current control bit convert threshold: After Vibrator power on, the current control bit will load the stable register when a 16-bit counter's value >= the threshold set by this register

10.1.1.30 AUDIO_CTRL

Description：Audio general control

0x0074			Audio general control (reset 0x0000_0080)											AUDIO_CTRL		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VB_ARM_SOFT_RST	PA_RESERVE							HEADDETECT_PD	LINEINRE_S			LINEINRE_EN	VBMCLK_SOURCE_SEL	VBMCLK_ARM_ACC	VBMCLK_ARM_EN
Type	R/W	RO							R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16h0	Reserved
VB_ARM_SOFT_RST	[15]	R/W	1'h0	ARM soft reset for dolphin
PA_RESERVE	[14:8]	R/W	7'h0	PA reserve interface
HEADDETECT_PD	[7]	R/W	1'h1	Head detection power down
LINEINRE_S	[6:4]	R/W	3'h0	Line in recorder gain program
LINEINRE_EN	[3]	R/W	1'h0	Line in recorder enable, high effective
VBMCLK_SOURCE_SEL	[2]	R/W	1'h0	Source of 12M input clock for audio codec 1: Select external clock from pin 0: Select internal clock on chip
VBMCLK_ARM_ACC	[1]	R/W	1'h0	ARM or DSP control audio codec MCLK and RST; 1: Controlled by ARM; 0: Controlled by DSP;
VBMCLK_ARM_EN	[0]	R/W	1'h0	Activate 12M input clock for audio codec if VBMCLK_ARM_ACC is true

				1: enable VBMCLK 0: disable VBMCLK

10.1.1.31 AUDIO_PA_CTRL0

Description：Audio PA control0

0x0078	Audio PA control0 (reset 0x0000_0180)												AUDIO_PA_CTRL0			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			PA_OCP_I	PA_OTP_PD	PA_OTP_T			PA_PGA_V				PA_VCM_EN	PA_STOP_EN	PA_EN_RST	PA_EN
Type	RO			R/W	R/W	R/W			R/W				R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:13]	RO	19h'0	Reserved
PA_OCP_I	[12]	R/W	1'h0	PA over current protection circuit current select: 0: 500mA (default) 1: 700mA
PA_OTP_PD	[11]	R/W	1'h0	PA over temperature protection circuit power down signal: 0: power on(default) 1: power down
PA_OTP_T	[10:8]	R/W	3'h1	PA over temperature protection circuit temperature select: 000: 104C -> 74C 001:128C -> 98C(default) 010: 152C -> 122C 011: 175C -> 146C

				100: 6C -> -24C 101: 30C -> 0C 110: 55C -> 25C 111: 79C -> 49C
PA_PGA_V	[7:4]	R/W	4'h8	PA PGA select: 0000: mute 0001: -21db 0010: -18db 0011: -15db 0100: -12db 0101: -9db 0110: -6db 0111: -3db 1000: 0db(default) 1001: 3db 1010: 6db 1011: 9db 1100: 12db 1101: 15db 1110: 18db 1111: 21db
PA_VCM_EN	[3]	R/W	1'h0	PA vcom voltage fast start up enable signal: 0: disable(default) 1: enable
PA_STOP_EN	[2]	R/W	1'h0	PA stop enable signal: 0: disable(default) 1: enable
PA_EN_RST	[1]	R/W	1'h0	Set this bit will disable PA. This bit has higher priority than PA_EN.
PA_EN	[0]	R/W	1'h0	PA enable

10.1.1.32 AUDIO_PA_CTRL1

Description: Audio PA control1

0x007C			Audio PA control1 (reset 0x0000_1040)													AUDIO_PA_CTRL1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PA_ABOCP_PD	PA_DOCP_PD	PA_DTRI_F		PA_DEMI_EN	PA_D_EN	PA_LDO_EN_RST	PA_LDO_EN	PA_LDOOCP_PD	PA_LDO_V			Reserved	PA_SWOCP_PD	PA_SW_EN_RST	PA_SW_EN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			RO	R/W	R/W	R/W
Reset	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16h'0	Reserved
PA_ABOCP_PD	[15]	R/W	1'h0	PA class-AB mode over current protection circuit power down signal: 0: power on(default) 1: power down
PA_DOCP_PD	[14]	R/W	1'h0	PA class-D mode over current protection circuit power down signal: 0: power on(default) 1: power down
PA_DTRI_F	[13:12]	R/W	2'h1	PA class-D mode Switching frequency select: 00: 300kHz 01: 590kHz(default) 10: 870kHz 11: 1.1MHz
PA_DEMI_EN	[11]	R/W	1'h0	PA class-D mode reduce EMI enable signal: 0: disable(default) 1: enable
PA_D_EN	[10]	R/W	1'h0	PA class-AB mode enable signal: 0: class-AB(default) 1: class-D
PA_LDO_EN_RST	[9]	R/W	1'h0	Set this bit will disable LDO_PA. This bit

				has higher priority than PA_LDO_EN.
PA_LDO_EN	[8]	R/W	1'h0	LDO_PA enable
PA_LDOOCP_PD	[7]	R/W	1'h0	LDO_PA over current protection circuit power down signal: 0: power on(default) 1: power down
PA_LDO_V	[6:4]	R/W	3'h4	LDO_PA output voltage select: 000: 2.9V 001: 3.0V 010: 3.1V 011: 3.2V 100: 3.3V(default) 101: 3.4V 110: 3.5V 111: 3.6V
	[3]	RO	1'h0	Reserved
PA_SWOCP_PD	[2]	R/W	1'h0	PA power switch over current protection power down signal: 0: power on(default) 1: power down
PA_SW_EN_RST	[1]	R/W	1'h0	Set this bit will disable PA power switch.
PA_SW_EN	[0]	R/W	1'h0	PA power switch enable, 0: disable(default) 1: enable

10.1.1.33 ANA_MIXED_CTRL

Description：analog mixed control

0x0080	Analog mixed control (reset 0x0000_0020)												ANA_MIXED_CTRL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PTEST_PD_SET	Reserved							VIBR_PWR_ERR_CLR	CLKBT_EN	CLK26M_REGS0		UVHO_EN_RST	UVHO_EN	OTP_EN_RST	OTP_EN
Type	R/W	RO							R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16	RO	160	Reserved
PTEST_PD_SET	[15]	R/W	1'b0	PTEST power down set under PTEST mode
	[14:8]	RO	7h0	Reserved
VIBR_PWR_ERR_CLR	[7]	R/W	1'h0	Vibrator current control circuit error clear
CLKBT_EN	[6]	R/W	1'h0	Bluetooth 26MHz output enable "1" 26M clock enable. "0" 26M clock disable. (default)
CLK26M_REGS0	[5:4]	R/W	2'h10	Output voltage swing register of CLK (default CLK26M_RegS0[1:0]=10) for 10pF load, 11: 2V 10: 1.6 (default) 01: 0.9 00: 0.5
UVHO_EN_RST	[3]	R/W	1'h0	When set, UVHO is disabled. This bit has

				higher priority than UVHO_EN.
UVHO_EN	[2]	R/W	1'h0	When set, UVHO is enabled.
OTP_EN_RST	[1]	R/W	1'h0	When set, OTP (Over Temperature Protection) is disabled. This bit has higher priority than OTP_EN.
OTP_EN	[0]	R/W	1'h0	When set, OTP is enabled.

10.1.1.34 ANA_STATUS

Description：analog circuit status

0x0084	Analog circuit status (reset 0x0000_0300)															ANA_STA
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VIBR_PWR_ERR	Reserved				BOND OPT2	VIBR_PD	WHTLED_PD	PA_OCP_FLAG		PA_OTP_FLAG		CHGR_ON	CHGR_STDBY	BONDOPT1	BONDOPT0
Type	RO	RO				RO	RO	RO	RO		RO		RO	RO	RO	RO
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
VIBR_PWR_ERR	[15]	RO	1'h0	Vibrator current control circuit error status
	[14:11]	RO	4'h0	Reserved
BONDOPT2	[10]	RO	1'h0	DCDC ARM OPTION INPUT 1: External ARM DCDC 0: Internal ARM DCDC
VIBR_PD	[9]	RO	1'h1	Vibrator power down status

WHTLED_PD	[8]	RO	1'h1	White LED power down status
PA_OCP_FLAG	[7:6]	RO	2'h0	PA over current protection circuit alert signal: 00: normal 01/10/11: over current
PA_OTP_OTP	[5:4]	RO	2'h0	PA over temperature protection circuit alert signal: 00: normal 01/10/11: over temperature
CHGR_ON	[3]	RO	1'h0	Charger voltage high indicator
CHGR_STDBY	[2]	RO	1'h0	Charging procedure completed
BONDOPT1	[1]	RO	1'h0	LDO power on sequence option: 1: LDO power on at same time 0: LDO power on sequence
BONDOPT0	[0]	RO	1'h0	DCDC OPTION INPUT 1: External DCDC 0: Internal DCDC

10.1.1.35 RST_STATUS

Description：Reset status

0x0088	Reset status(0x0000_0000)												RST_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ALL_HRST_MONITOR				POR_HRST_MONITOR								WDG_HRST_MONITOR			
Type	R/W				R/W								R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:12]	RO	20'h0	Reserved

ALL_HRST_MONITOR	[15:12]	R/W	4'h0	When power on reset or Watch dog reset or Chip pin reset active, this register is reset to 0;
POR_HRST_MONITOR	[11:4]	R/W	8'h0	When power on reset active, this register is reset to 0;
WDG_HRST_MONITOR	[3:0]	R/W	4'h0	When WDG reset active, this register is reset to 0;

10.1.1.36 MCU_WR_PROT

Description：MCU write protect register

0x008C			MCU write protect register (reset 0x0000_0000)										MCU_WR_PROT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MCU_PROT[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
MCU_WR_PROT	[15:0]	WO	16'h0	Write Protection of APB Arch Clock Enable Write 0xc3d4 to release 'arch_eb' bit protection, write others value to protect. Bit[0] can be read as status of apb_arch_wr_prot 0- is proteced; 1- is released.

10.1.1.37 VIBR_WR_PROT

Description：VIBR register write protection

0x0090			VIBR register write protection (reset 0x0000_0000)												VIBR_WR_PROT	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VIBR_WR_PROT[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
VIBR_WR_PROT	[15:0]	WO	16'h0	Write Protection of VIBRATOR_CTRL0 and VIBRATOR_CTRL1 Write 0xa1b2 to release VIBRATOR_CTRL0 and VIBRATOR_CTRL1 protection, write others value to protect. Bit[0] can be read as status of vibr_wr_prot 0- is proteced; 1- is released.

10.1.1.38 INT_GPI_DEBUG

Description：analog interrupt debug

0x0094			Analog interrupt and GPI debug (reset 0x0000_0000)											INT_GPI_DEBUG		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		HEADMIC_DETECTION_DEB	HEAD_BUTTON_DEB	PBINT_DEB	CHGR_OVI_DEB	CHGR_INT_DEB	GPI_DEB_EN	CHGRWDG_INT_DEB	EIC_INT_DEB	TPC_INT_DEB	WDG_INT_DEB	RTC_INT_DEB	GPIO_INT_DEB	ADC_INT_DEB	INT_DEB_EN
Type	RO		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:14]	RO	18'h0	Reserved
HEADMIC_DETECTION_DEB	[13]	R/W	1'h0	When GPI_DEG_EN set, this bit will replace HEADMIC_DETECTION for GPI[5]
HEAD_BUTTON_DEB	[12]	R/W	1'h0	When GPI_DEG_EN set, this bit will replace HEAD_BUTTON for GPI[4]
PBINT_DEB	[11]	R/W	1'h0	When GPI_DEG_EN set, this bit will replace PBINT for GPI[3]
CHGR_OVI_DEB	[10]	R/W	1'h0	When GPI_DEG_EN set, this bit will replace CHGR_OVI for GPI[6]
CHGR_INT_DEB	[9]	R/W	1'h0	When GPI_DEG_EN set, this bit will replace CHGR_INT for GPI[2]
GPI_DEB_EN	[8]	R/W	1'h0	GPI debug enable
CHGRWDG_INT_DEB	[7]	R/W	1'h0	When INT_DEB_EN set, this bit will replace chgrwdg_irq for

				interrupt controller
EIC_INT_DEB	[6]	R/W	1'h0	When INT_DEB_EN set, this bit will replace eic_irq for interrupt controller
TPC_INT_DEB	[5]	R/W	1'h0	When INT_DEB_EN set, this bit will replace tpc_irq for interrupt controller
WDG_INT_DEB	[4]	R/W	1'h0	When INT_DEB_EN set, this bit will replace wdg_irq for interrupt controller
RTC_INT_DEB	[3]	R/W	1'h0	When INT_DEB_EN set, this bit will replace rtc_irq for interrupt controller
GPIO_INT_DEB	[2]	R/W	1'h0	When INT_DEB_EN set, this bit will replace gpio_irq for interrupt controller
ADC_INT_DEB	[1]	R/W	1'h0	When INT_DEB_EN set, this bit will replace adc_irq for interrupt controller
INT_DEB_EN	[0]	R/W	1'h0	Interrupt debug enable

10.1.1.39 HWRST_RTC

Description: RTC test reg

0x0098	RTC test reg(0x0000_0000)	HWRST_RTC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	HWRST_RTC_REG								HWRST_RTC_SET							
Type	RO								R/W							
Reset	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
HWRST_RTC_REG	[15:8]	RO	-	Value will change according to HWRST_RTC_SET in RTC domain
HWRST_RTC_SET	[7:0]	R/W	8'h0	Software set this register to test RTC clock

10.1.1.40 IF_SPR_CTRL

Description： IF_SPR pin control

0x009C			Two IF_SPR pin control (reset 0x0000_0002)											IF_SPR_CTRL		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved													IF_SPR_IN	IF_SPR_OE	IF_SPR_OUT
Type	RO													RO	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
	[31:3]	RO	29'h0	Reserved
IF_SPR_IN	[2]	RO	1'h0	IF_SPR pin input data
IF_SPR_OE	[1]	R/W	1'h1	IF_SPR pin output enable
IF_SPR_OUT	0]	R/W	1'h0	IF_SPR pin output data

10.1.1.41 CHIP_ID_LOW

Description：8810 chip ID low 16 bits

0x00F8	8810 chip ID low 16 bits(reset 0x0000_A000)														CHIP_ID_LOW	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHIP_ID_LOW															
Type	RO															
Reset	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
CHIP_ID_LOW	[15: 0]	RO	16'hA000	8810 chip ID low 16 bits

10.1.1.42 CHIP_ID_HIGH

Description：8810 chip ID high 16 bits

0x00FC	8810 chip ID high 16 bits(reset 0x0000_8810)														CHIP_ID_HIGH	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHIP_ID_HIGH															
Type	RO															
Reset	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Field Name	Bit	Type	Reset	Description

			Value	
	[31:16]	RO	16'h0	Reserved
CHIP_ID_HIGH	[15: 0]	RO	16'h8810	8810 chip ID high 16 bits

Appendix

Acronyms and Abbreviations

Field	Symbol	Acronyous and Abbreviations
A		
	AAC	Advanced Audio Coding
	ADC	Analog Digital Converter
	ADM	Memory Address and data is Mutiple
	ADP	Memory Address and data is Parallel
	AES	Advanced Encryption Standard
	AFC	Auto Frequency Calibration
	AGC	Auto Gain Calibration
	AHB	Advanced Hign performance Bus
	ALC	Auto Level Control
	ALU	Arithmetic and Logical Unit
	AMR	Adaptive Multi-Rate
	APC	Auto Phase Calibration
	ARF	Addressing Register File
	AST	Action start time
	ASU	Add Subtract Unit
B		
	BMU	Bit Manipulation Unit
	BPINT	Breakpoint Interrupt
	BSM	Bit Streaming Module
	BSW	Band-Switch Word
	BTL	Bridge Tied Load
C		
	CDM	Charged-device model
	CIA	Common Information Area
	CIF	common intermediate format
	CIS	Card Information Structure
	CMD	Command
	CSRs	Control and Status Registers
D		
	DAAU	Data Address and Arithmetic Unit
	DAC	Digital Analog Converter
	DAI	Digital Audio Interface

Field	Symbol	Acronyous and Abbreviations
	DBK	De-Blocking
	DCAM	Digital Camera
	DCS	Digital Cellular System
	DCT	Discrete Cosine Transformation
	DDR	Double Data Rate
	DEC	Decode
	DFF	D type flip-flop
	DFT	Design For Test
	DLCH	Down Link Channel
	DMA	Direct Memory Access
	DMEM	DDR Memory
	DQS	Bidirectional data strobe
	DR	Dynamic Range
	DRM	Digital Rights Management
	DSP	Digital Signal Processor
E		
	ECC	Error Checking Code
	EFR	Enhanced Full Rate
	EMC	External Memory Controller
	ENC	Encode
F		
	FBR	Function Basic Registers
	FFT	Fast Fourier Transformation
	FIFO	First In First Out
	FIQ	Fast Interrupt Request
	FIR	Finite Impulse Response
	FMO	Flexible Macroblock Ordering
	FR	Full Rate
	FSM	Finite State Machine
G		
	GEA	Gprs Encryption Algorithm
	GIF	Graphics Interchange Format
	GMSK	Gaussian-filtered Minimum Shift Keying
	GPIO	General Perpose Input/Output
H		
	HBM	Human body model
	HPF	High Pass Filter
	HR	Half Rate
	HSDPA	High Speed Downlink Packet Access
	HSUPA	High Speed Uplink Packet Access

Field	Symbol	Acronyous and Abbreviations
I		
	ICU	Interrupt Control Unit
	IDCT	Inverse Discrete Cosine Transformation
	IFFT	Inverse Fast Fourier Transformation
	I2C	Inter-Integrated Circuit
	IIR	Infinite Impulse Response
	IIS	Integrate Interface of Sound
	IPRED	Intra Prediction
	IQT	Integer Quantization Tranform
	IRQ	Interrupt Request
J		
	JDA	Joint-Detection Accelerator
	JPEG	Joint Photographics Expert Group
	JTAG	Joint Test Cction Group
L		
	LCDC	Liquid Crystal Display Controller
	LRO	Left Right ouput
	LSB	least Significant Bit
	LSE	Least Square Equalizer
M		
	MAP	Maximum A Posteriori
	MBC	Macro Block Compensation
	MCA	Motion Compensation Accelerator
	MCS	Mobile Control Station
	MCU	Micro Control Unit
	MEA	Motion Estimation Accelerator
	MM	Machine Model
	MPEG	Motion Photographics Expert Group
	MSB	Most Significant Bit
	MSL	Moisture Sensitivity Level
N		
	NSEQ	None Sequencial
O		
	OCR	Optical CharacterRrecognition
	OSD	On-Screen Display
	OTP	Over Temperature Protection
P		
	PBINT	Power Button Interrupt
	PCM	Pulse Code Modulation
	PGM	Program

Field	Symbol	Acronyous and Abbreviations
	PIU	Processor Interface Unit
	PLL	Phase Locked Loop
	PNG	Portal Network Graphic
	PSRR	Power Supply Rejection Ratio
	PTEST	Production Test
Q		
	QAM	Quadracture Amplitude Modulation
	QBC	Quarter Bit Clock
	QCIF	Quarter Common Intermediate Format
	QPSK	Quarternary Phase Shift Keying
	QVGA	quarter Video Graphics Array
R		
	RCA	Relative Card Address
	RFT	RF Timing
	RFU	Reserved for Future Use
	RISC	Reduced Instruction Set Computer
	RLC	Radio Link Control
	RMA	Rate Matching Accelerator
	RTC	Real Time Clock
S		
	SBI	Serial Bus Interface
	SCL	Serial Clock lLne
	SDA	Serial Data Address
	SDIO	Secure Digtial Input/Ouput
	SDR	Single Data Rate
	SID	Signal ID
	SIM	Subscriber Identity Module
	SIMD	Single Instruction Multiple Data
	SMEM	SDR Memory
	SNR	Signal to Noise Ratio
	SPI	Serial Peripheral Interface
	SRAM	Static RAM
T		
	TCVCXO	Temperature-Compensated Voltage Controlled Oscillator
	TFCI	Transport Format Combination Indicator
	THD	Total Harmonic Distortion
	TPC	Touch Panel Controller
	TTI	Transmission Time Interval
U		

Field	Symbol	Acronyous and Abbreviations
	UART	Universal Asynchronous Reveiver/Transmitter
	UID	Unique ID
	USB	Univeral Serial Bus
	UVLO	Under Voltage Lock Out
V		
	VDB	Video Data Bus
	VINT	Vector Interrupt
	VLC	Variable Length Code
	VLD	Variable Length Decode
	VLIW	Very Long Instruction Word
W		
	WDT	Watchdog Timer
	WQVGA	Wide Quarter Video Graphics Array