SC6531E and SC6531M Device Specification



www.spreadtrum.com

Spreadtrum Communications, Inc., Confidential and Proprietary

Spreadtrum Confidential
Spreadtrum Confidential For CECT

IMPORTANT NOTICE

COPYRIGHT NOTICE

Copyright © 2016, Spreadtrum Communications, Inc. All rights reserved.

TRADEMARKS

Spreadtrum Communications, Inc. and Spreadtrum Communications, Inc.'s products are exclusively owned by Spreadtrum Communications, Inc. References to other companies and their products use trademarks owned by the respective companies and are for reference purpose only.

WARRANTY DISCLAIMER

Spreadtrum Communications, Inc. makes no representations or warranties, either express or implied, by or with respect to anything in this document, and shall not be liable for any implied warranties of merchantability or fitness for a particular purpose or for any indirect, special or consequential damages.

CONFIDENTIALITY

The information contained herein (including any attachments) is confidential. The recipient hereby acknowledges the confidentiality of this document, and except for the specific purpose, this document shall not be disclosed to any third party.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Revision History

Version	Data	Owner	Note
0.1	1/7/2016	Summer Xi	First draft, based on Jin Ji's email;
0.2	9/18/2016	Wenbing Xu	The First Version
0.21	9/29/2016	Wenbing Xu	1.Change vedio codec from D1 25fps to HVGA 30fps 2.Bus Monitor Register update
0.3	11/23/2016	Wenbing Xu	1.GEA base address update. 2.Add Chapter 4.19
0.4	12/5/2016	Wenbing Xu	1.Delete SC6531F
0.5	01/06/2017	Wenbing Xu	1.Update chapter 12.3

Spreadtrum Confidential
Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Contents

IMPORTANT NOTICE **2**
Revision History **3**
Contents **4**
1 System Overview **22**
1.1 General Description 22
1.2 SC6531 Features 22
1.2.1 Platform Features 23
1.2.2 Modem Features 24
1.2.3 Multimedia Features 24
1.2.3.1 Camera Interface 24
1.2.3.2 LCD Interface 25
1.2.3.3 Image Codec 25
1.2.3.4 Video Codec 25
1.2.3.5 Audio Codec 25
1.2.4 Bluetooth Features 26
1.2.5 FM Features 26
1.3 Chip Architecture 27
1.4 Applications 28
2 Package Information **30**
2.1 Top Marketing Definition 30
2.2 BGA Pinout 31
2.3 Package Outline 32
2.4 Reflow Profile 34
3 Pin Information **36**
3.1 Pin symbol descriptions 36
3.2 Pin List 37
3.2.1 SC6531E 37
3.2.2 SC6531M 47
3.3 Pin Multiplexed Function List 57
3.3.1 SC6531E 57
3.3.2 SC6531M 60
3.4 GPIO List 63
3.4.1 SC6531E 63
3.4.2 SC6531M 65
3.5 Control Registers 67
3.5.1 Memory map 67
3.5.2 Register Description 71
3.5.2.1 Pin_CTRL_REG0 71
3.5.2.2 Pin_CTRL_REG1 73
3.5.2.3 Pin_CTRL_REG2 73
3.5.2.4 Pin_CTRL_REG3 75
3.5.2.5 Pin_CTRL_REG4 76
3.5.2.6 Pin_CTRL_REG5 77

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

3.5.2.7 Pin_CTRL_REG6 77
3.5.2.8 Pin_CTRL_REG7 78
3.5.2.9 Other Pin Control Register 79
3.5.3 Strapping Pins 82
3.5.4 PAD information 82
3.5.4.1 Digital Pad Type Description 82
3.5.4.2 Digital Power / Ground cell 82
3.5.4.3 Power Switch I/O cells 83
3.5.4.4 SPSCBC2_8X_HL/VL 84
3.5.4.5 SPSEBC2_24X_HL/VL 85
3.5.5 AON_TOP_AON_APB_RF Register Address Map 87
3.5.5.1 DDR_ZQ_CONTROL 87
3.5.5.2 DDR_ZQ_CONTROL 87
4 Electrical Specification 89
4.1 DC specification 89
4.1.1 Absolute maximum ratings 89
4.1.2 Recommended operating conditions 89
4.1.3 Thermal characteristics 90
4.1.4 ESD characteristics 90
4.1.5 DC characteristics 90
4.2 AC characteristics 91
4.3 Performance specification 92
4.3.1 Phase-Locked Loop 92
4.3.2 USB 1.1 PHY 93
4.3.3 Automatic power control (APC)DAC 93
5 Micro-Controller Unit Subsystem 94
5.1 Processor 94
5.2 ARM memory map 94
5.2.1 ARM9 AHB Memory Map 94
5.2.2 ARM9 APB Memory Map 99
5.2.3 ARM7 AHB Memory Map 101
5.2.4 ARM7 APB Memory Map 106
5.2.5 CHIP ID 106
5.2.6 Analog Die Digital Memory Map 107
5.2.6.1 ARM side space 107
5.2.6.2 DSP side space 107
5.2.6.3 Access priority setting 107
5.3 Internal memory controller 108
5.3.1 MCU Internal RAM 108
5.3.2 MCU Internal ROM 108
5.3.3 MCU-DSP Switched RAM 108
5.3.3.1 Control Register Descriptions 109
5.3.4 MCU-DSP Shared RAM 110
5.3.4.1 Features 110
5.3.4.2 Functional Description 110
5.3.4.3 Operations 111
5.3.4.4 Programming Notes 111
5.4 LCM controller 112

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.4.1 Overview 112
5.4.2 Features 112
5.4.2.1 AHB Related Features 112
5.4.2.2 External LCM Related Features 112
5.4.3 Signal descriptions 113
5.4.1 Timing Description 113
5.4.2 Control registers 115
5.4.2.1 Memory map 115
5.4.2.2 Register descriptions 115
5.4.3 Application notes 120
5.4.3.1 Application Notes 120
5.5 SRAM Memory controller 121
5.5.1 Overview 121
5.5.2 Features 122
5.5.2.1 AHB Related Features 122
5.5.2.2 External Memory Related Features 122
5.5.3 Signal descriptions 123
5.5.1 Function Description 124
5.5.1.1 Block Diagram 124
5.5.1.2 Operation Descriptions 124
5.6 Serial Flash Controller 208
5.6.1 Overview 209
5.6.2 Features 209
1.1.1.1 Flash Device 209
1.1.1.2 Main features 209
1.1.1.3 Serial Flash Instruction Format 209
1.1.1.4 Interrupt Operation 211
1.1.1.5 Software Program Flow 212
5.6.3 Signal descriptions 213
5.6.4 Funtion description 213
1.1.1.6 Block Diagram 213
1.1.1.1 FSM control 214
1.1.1.2 Timing Parameter 215
5.6.5 Control registers 216
5.6.5.1 Memory map 216
5.6.5.2 Register description 218
5.6.5.3 SFC_CMD_SET 218
5.6.5.4 SFC_SOFT_REQ 219
5.6.5.5 CS0_TBUF_CLR 219
5.6.5.6 SFC_INT_CLR 219
5.6.5.7 SFC_STATUS 219
5.6.5.8 CS0_TIMING_CFG 220
5.6.5.9 CS0_RD_SAMPLE_CFG 220
5.6.5.10 SFC_CLK_CFG 221
5.6.5.11 SFC_CS_CFG 222
5.6.5.12 SFC_LSB_CFG 222
5.6.5.13 SFC_IO_DLY_CFG 222
5.6.5.14 SFC_WP_HLD_INIT_CFG 223

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.6.5.15 SFC_DL0 223
5.6.5.16 SFC_DL1 224
5.6.5.17 SFC_DLL 224
5.6.5.18 CS0_CMD_BUF0 225
5.6.5.19 CS0_CMD_BUF1 225
5.6.5.20 CS0_CMD_BUF2 225
5.6.5.21 CS0_CMD_BUF3 225
5.6.5.22 CS0_CMD_BUF4 225
5.6.5.23 CS0_CMD_BUF5 226
5.6.5.24 CS0_CMD_BUF6 226
5.6.5.25 CS0_CMD_BUF7 226
5.6.5.26 CS0_CMD_BUF8 226
5.6.5.27 CS0_CMD_BUF9 226
5.6.5.28 CS0_CMD_BUF10 227
5.6.5.29 CS0_CMD_BUF11 227
5.6.5.30 CS0_TYPE_INF_BUF0 227
5.6.5.31 CS0_TYPE_INF_BUF1 229
5.6.5.32 CS0_TYPE_INF_BUF2 231
5.6.5.33 CS1_RD_CFG 233
5.6.5.34 CS1_TBUF_CLR 233
5.6.5.35 CS1_TIMING_CFG 233
5.6.5.36 CS1_RD_SAMPLE_CFG 234
5.6.5.37 CS1_CMD_BUF0 235
5.6.5.38 CS1_CMD_BUF1 235
5.6.5.39 CS1_CMD_BUF2 235
5.6.5.40 CS1_CMD_BUF3 235
5.6.5.41 CS1_CMD_BUF4 235
5.6.5.42 CS1_CMD_BUF5 235
5.6.5.43 CS1_CMD_BUF6 236
5.6.5.44 CS1_CMD_BUF7 236
5.6.5.45 CS1_CMD_BUF8 236
5.6.5.46 CS1_CMD_BUF9 236
5.6.5.47 CS1_CMD_BUF10 236
5.6.5.48 CS1_CMD_BUF11 237
5.6.5.49 CS1_TYPE_INF_BUF0 237
5.6.5.50 CS1_TYPE_INF_BUF1 239
5.6.5.51 CS1_TYPE_INF_BUF2 241
5.6.5.52 SFC_CS1_START_ADDR 242
5.6.5.53 SFC_INT_IEN 243
5.6.5.54 SFC_INT_RAW 243
5.6.5.55 SFC_INT_STS 243
5.6.5.56 SFC_DLL_STS 244
5.6.5.57 SFC_FIFO_SYNC_SEL 244
5.6.6 Application notes 244
5.6.6.1 Write enable (06H) 244
5.6.6.2 Program (02H) 245
5.6.6.3 Fast read (0BH) 245
5.6.6.4 PHY configure 245

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.6.6.5 DLL configure 245
5.7 Direct Memory Access 246
5.7.1 Overview 246
5.7.2 Features 247
5.7.3 Funtion description 248
5.7.3.1 General Description 248
5.7.3.2 Standard & Full DMA Channels 248
5.7.3.3 Data Structure 248
5.7.3.4 DMA Pause 249
5.7.3.5 Channel Priority and Arbitration 249
5.7.3.6 Address Fix Mode 249
5.7.3.7 Address Wrap Mode 249
5.7.3.8 Endian & Data Switch 250
5.7.3.9 Un-aligned Word Access 250
5.7.3.10 Word Packing 251
5.7.3.11 Hardware Request Re-allocated 251
5.7.3.12 Error Configuration 251
5.7.4 Control registers 251
5.7.4.1 Memory map 251
5.7.4.2 Register description 255
5.7.5 Application notes 268
5.8 Interrupt Controller (Intc) 268
5.8.1 Overview 268
5.8.2 Features 269
5.8.3 Signal description 269
5.8.4 Interrupt Source Assignment 269
5.8.5 Funtion description 271
5.8.5.1 Hardware-Triggered Channels 271
5.8.5.2 Software-Triggered Channel 272
5.8.5.3 Special Channel 272
5.8.6 Control registers 272
5.8.6.1 Memory map 272
5.8.6.2 Register description 273
5.8.7 Application notes 282
5.9 BUS Monitor 283
5.9.1 Overview 283
5.9.2 Features 283
5.9.3 Bus Monitor Assignment 283
5.9.4 Control registers 285
5.9.4.1 Memory Map 285
5.9.4.2 Register Descriptions 285
5.10 General Purpose Timers 292
5.10.1 Overview 292
5.10.2 Features 292
5.10.3 Signal description 293
5.10.4 Funtion description 293
5.10.4.1 RTC Clock Trigged Timers 293
5.10.4.2 PCLK Trigged Timers 298

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.10.5 Control registers....299
5.10.5.1 Memory map....299
5.10.5.2 Register description....299
5.10.6 Application notes....311
5.10.6.1 RTC Clock Trigged Timers....311
5.10.6.2 PCLK Trigged Timers....312
5.10.7 Implementations(for internal only)....312
5.10.8 Future improvements....313
5.11 System timer....313
5.11.1 Overview....313
5.11.2 Features....313
5.11.3 Signal description....313
5.11.4 Funtion description....313
5.11.5 Control registers....314
5.11.5.1 Memory map....314
5.11.5.2 Register description....314
5.11.6 Application notes....317
5.11.7 Implementations....318
5.11.8 Future improvements....318
5.12 RTC timer....318
5.12.1 Overview....318
5.12.2 Features....318
5.12.3 Funtion description....318
5.12.4 Control registers....319
5.12.4.1 Memory map....319
5.12.4.2 Register description....319
5.12.5 Application notes....330
5.13 Watchdog Timer....331
5.13.1 Overview....331
5.13.2 Features....331
5.13.3 Signal description....331
5.13.4 Funtion description....331
5.13.5 Control registers....332
5.13.5.1 Memory map....332
5.13.5.2 Register description....332
5.13.6 Application notes....342
5.13.7 Implementations....343
5.13.8 Future improvements....343
5.14 Charge Watchdog(for internal only)....344
5.14.1 Overview....344
5.14.2 Features....344
5.14.3 Signal description....344
5.14.4 Funtion description....344
5.14.5 Control registers....345
5.14.5.1 Memory map....345
5.14.5.2 Register description....345
5.14.6 Application notes....350
5.15 LZMA Decompress Accelerator (for internal only)....351

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.15.1 Overview 351
5.15.2 Features 352
5.15.3 Register Address Map 352
5.15.3.1 LZMA_CTRL 353
5.15.3.2 LZMA_CTRL_STS 354
5.15.3.3 LZMA_INT 355
5.15.3.4 LZMA_SRC_SADDR 357
5.15.3.5 LZMA_DST_SADDR 357
5.15.3.6 LZMA_SRC_LEN 358
5.15.3.7 LZMA_DST_LEN 358
5.15.3.8 LZMA_BUFFER_SADDR 358
5.15.3.9 LZMA_BUFFER_LEN 359
5.15.3.10 LZMA_BUFFER_START_LEN 359
5.15.3.11 LZMA_PROC_POS 360
5.15.3.12 LZMA_TRANS_LEN 360
5.15.3.13 LZMA_UNZIP_SIZE 361
5.15.3.14 LZMA_STOP 361
5.15.3.15 LZMA_DEBUG_1 362
5.15.3.16 LZMA_DEBUG_2 363
5.15.3.17 LZMA_DEBUG_3 363
5.15.3.18 LZMA_ENDIAN 363
5.15.4 Application Notes 364
5.16 GEA(EPT) Accelerator (for internal only) 367
5.16.1 Overview 367
5.16.2 Features 367
5.16.3 Control Registers 367
5.16.3.1 Memory map 367
5.16.3.2 Register Descriptions 368
5.16.4 Application Notes 378
5.17 GPIO 379
5.17.1 Overview 379
5.17.2 Features 379
5.17.3 Function Description 380
5.17.4 Control Registers 380
5.17.4.1 Memory map 380
5.17.4.2 Register Descriptions 381
5.17.5 Application Notes 388
5.17.5.1 Programming Notes 388
5.18 EIC 388
5.18.1 Overview 388
5.18.2 Features 389
5.18.2.1 EIC_DBNC 389
5.18.2.2 EIC_LATCH 389
5.18.2.3 EIC_ASYNC 389
5.18.2.4 EIC_SYNC 390
5.18.3 Funtion description 390
5.18.4 Control registers 390
5.18.4.1 Memory map 390

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.18.4.2 Register description 393
5.18.5 Application notes 421
5.18.5.1 Programming Model 421
5.18.5.2 Programming Notes 422
5.19 ARM9/CM4/DSP share UART1 mechanism 422
5.19.1 arch 422
6 Micro-Controller Unit Peripherals 423
6.1 USB 423
6.1.1 Overview 423
6.1.2 Features 423
6.1.2.1 Five Endpoints with FIFO and DMA Interface 423
6.1.2.2 Support Suspending and Resuming 425
6.1.2.3 Support Reset Signal Coming from Host 425
6.1.2.4 Support 6 DMA Channels 425
6.1.2.5 Support Interrupt Enable and State 425
6.1.2.6 Read and Write of Memories 425
6.1.2.7 Support Remote Wakeup 425
6.1.2.8 Integrate USB Transceiver 425
6.1.3 Signal description 425
6.1.4 Control registers 426
6.1.4.1 Memory map 426
6.1.4.2 Register description 428
6.1.5 Application notes 459
6.2 UART and IrDA interface 460
6.2.1 Overview 460
6.2.2 Features 460
6.2.3 Signal description 460
6.2.4 Funtion description 461
6.2.4.1 UART Mode Description 462
6.2.4.1 IRDA Mode Description 465
6.2.4.2 Uart interface timing 466
6.2.5 Control registers 467
6.2.5.1 Memory map 467
6.2.5.2 Register description 467
6.2.6 Application notes 479
6.3 SPI interface 480
6.3.1 Overview 480
6.3.2 Features 480
6.3.3 Signal description 481
6.3.4 Funtion description 481
6.3.4.1 MICROWIRE/PLUS work mode 483
6.3.4.2 Synchronous SPI 485
6.3.4.3 4-wire Serial Interface(s8) 485
6.3.4.4 3-wire Serial interface 486
6.3.4.5 2-data-line Interface 488
6.3.4.6 Dummy control 493
6.3.4.7 SPI Slave Design 493
6.3.5 Control registers 498

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.3.5.1 Memory map 498
6.3.5.2 Register description 499
6.3.5.3 SPI_TXD 499
6.3.5.4 SPI_CLKD 499
6.3.5.5 SPI_CTL0 500
6.3.5.6 SPI_CTL1 501
6.3.5.7 SPI_CTL2 502
6.3.5.8 SPI_CTL3 503
6.3.5.9 SPI_CTL4 503
6.3.5.10 SPI_CTL5 504
6.3.5.11 SPI_INT_EN 505
6.3.5.12 SPI_INT_CLR 506
6.3.5.13 SPI_INT_RAW 507
6.3.5.14 SPI_INT_MASK_STS 508
6.3.5.15 SPI_STS1 509
6.3.5.16 SPI_STS2 509
6.3.5.17 SPI_DSPWAIT 511
6.3.5.18 SPI_STS3 511
6.3.5.19 SPI_CTL6 512
6.3.5.20 SPI_STS4 512
6.3.5.21 SPI_FIFO_RST 513
6.3.5.22 SPI_CTL7 513
6.3.5.23 SPI_STS5 515
6.3.5.24 SPI_CTL8 515
6.3.5.25 SPI_CTL9 516
6.3.5.26 SPI_CTL10 517
6.3.5.27 SPI_CTL11 517
6.3.5.28 SPI_CTL12 518
6.3.5.29 SPI_STS6 518
6.3.5.30 SPI_STS7 519
6.3.5.31 SPI_STS8 519
6.3.5.32 SPI_STS9 520
6.3.6 Application notes 521
6.3.6.1 Programming Model 521
6.3.6.2 GC9304C LCD driver Programming Model 525
6.3.6.3 Programming Notes 528
6.3.7 New feature 528
6.3.8 Clock Path 529
6.3.8.1 Master mode 529
6.3.8.2 Slave low speed mode 530
6.3.8.3 Slave high speed mode 531
6.3.9 Reset 532
6.4 IIS and PCM interface 532
6.4.1 Overview 532
6.4.2 Features 533
6.4.3 Signal description 533
6.4.4 Funtion description 533
6.4.4.1 IIS interface 533

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.4.4.2 PCM interface 536
6.4.4.3 IIS clock path....540
6.4.4.4 Pad IO timing 541
6.4.4.5 Setup time and hold time 542
6.4.5 Control registers....542
6.4.5.1 Memory map 542
6.4.5.2 Register description 543
6.4.6 Application notes....559
6.4.6.1 IIS Program examples 559
6.4.6.2 PCM program examples 560
6.4.6.3 Clock dividing modes 562
6.4.6.4 Working mode examples 565
6.4.6.5 Debug tips....565
6.5 I2C interface 566
6.5.1 Overview 566
6.5.2 Features 566
6.5.3 Signal description....566
6.5.4 Funtion description....567
6.5.4.1 System Configuration....567
6.5.4.2 Wire Serial Protocol 567
6.5.4.3 Arbitration Procedure 569
6.5.4.4 Timing Prameters....569
6.5.5 Control registers....570
6.5.5.1 Memory map 570
6.5.5.2 Register description 571
6.5.6 Application notes....576
6.6 Keypad interface....578
6.6.1 Overview 578
6.6.2 Features 578
6.6.3 Signal description....579
6.6.4 Funtion description....581
6.6.5 Control registers....582
6.6.5.1 Memory map 582
6.6.5.2 Register description 582
6.6.6 Application notes....596
6.6.7 Clock enable 597
6.6.1 KPD configuration 597
6.7 VBC Interface....597
6.7.1 Overview 597
6.7.2 Features 597
6.7.3 Signal Description 598
6.7.4 Function Description 598
6.7.4.1 Path Control and Function Module 599
6.7.4.2 Clock Domain....604
6.7.4.3 I2S Slave Interface....604
6.7.4.4 Audio Codec control Interface....605
6.7.4.5 Digital Audio Data Buffer....606
6.7.5 Control Registers 606

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.7.5.1 Memory map 606
6.7.5.2 Register Descriptions 614
6.8 GPIO 669
6.8.1 Overview 669
6.8.2 Features 670
6.8.3 Funtion description 670
6.8.4 Control registers 670
6.8.4.1 Memory map 670
6.8.4.2 Register description 671
6.8.4.3 GPIODATA 671
6.8.4.4 GPIODMSK 672
6.8.4.5 GPIODIR 672
6.8.4.6 GPIOIS 673
6.8.4.7 GPIOIBE 674
6.8.4.8 GPIOIEV 674
6.8.4.9 GPIOIE 675
6.8.4.10 GPIORIS 676
6.8.4.11 GPIOMIS 676
6.8.4.12 GPIOIC 677
6.8.4.13 GPIOINEN 678
6.8.5 Application notes 678
6.9 EIC 678
6.9.1 Overview 678
6.9.2 Features 679
6.9.2.1 EIC_DBNC 679
6.9.2.2 EIC_LATCH 679
6.9.2.3 EIC_ASYNC 679
6.9.2.4 EIC_SYNC 680
6.9.3 Funtion description 680
6.9.4 Control registers 681
6.9.4.1 Memory map 681
6.9.4.2 Register description 683
6.9.5 Application notes 711
6.9.5.1 Programming Model 711
6.9.5.2 Programming Notes 711
6.10 SDIO Controller 712
6.10.1 Overview 712
6.10.2 Features 712
6.10.3 SDIO Control Registers 713
6.10.3.1 Memory Map 713
6.10.3.2 Register Descriptions 714
7 BlueTooth 746
7.1 BT_TOP 746
7.1.1 Overview 746
7.1.2 Features 746
7.1.3 Signal Description 746
7.1.4 Function Description 748
7.1.5 Memory Map 749

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

7.1.5.1 BT MCU AHB Memory map 749
7.1.5.2 BT MCU APB Memory Map 752
7.1.5.3 CortexCM4 shared irams with ARM9 diagram 753
7.1.5.4 Register Descriptions 753
7.1.6 Boot 753
7.1.6.1 Boot from shared iram 753
7.1.6.2 Boot from EMC or SFC 753
7.1.7 Core Low Power 754
7.1.7.1 Enter Sleep 754
7.1.7.2 Wakeup from sleep 754
7.1.7.3 Wakeup from deepsleep 754
7.1.8 Interrupt Source Assignment 754
7.2 Pending Issues 756
7.2.1 Clock 757
7.2.2 Reset 757
7.2.3 AD/DA Interface 757
7.2.4 DCXO Calibration 758
7.2.5 ADI Master 758
7.2.6 Low Power 758
7.2.7 BT Debug Mode 758
7.2.8 FPGA Test 758
7.2.9 EDA Simulation 759
7.3 General Purpose Timer 759
7.3.1 Overview 759
7.3.2 Features 759
7.3.3 Signal Description 759
7.3.4 Function Description 760
7.3.4.1 Each asynchronous Timers 760
7.3.5 Control Registers 765
7.3.5.1 Memory map 765
7.3.5.2 Register Descriptions 766
7.3.6 Application Notes 776
7.3.6.1 RTC Clock Trigged Timers 776
7.3.7 Implementations 777
7.3.8 Features 777
7.3.9 Signal description 777
7.3.10 Funtion description 777
7.3.11 Control registers 777
7.3.11.1 Memory map 777
7.3.11.2 Register description 777
7.3.12 Application notes 777
7.3.13 Implementations 777
7.3.14 Future improvements 777
8 FM System 778
8.1 Overview 778
8.2 FM Key Function description 782
8.2.1 SEEK/Tune function description 782
8.2.2 RF control 783

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

8.2.3 Calibration Description 784
8.2.4 Ramp Softmute Method 784
8.3 FM Register Address Map 784
8.3.1 FM_CTRL 786
8.3.2 FM_EN 788
8.3.3 RF_INIT_GAIN 788
8.3.4 CHAN 789
8.3.5 AGC_TBL_CLK 789
8.3.6 SEEK_LOOP 790
8.3.7 FMCTL_STI 790
8.3.8 BAND_LMT 791
8.3.9 BAND_SPACE 792
8.3.10 RFCTRL 792
8.3.11 ADCBITMAP 793
8.3.12 INT_EN 793
8.3.13 INT_CLR 794
8.3.14 INT_STS 795
8.3.15 ADC_INFCTRL 795
8.3.16 SEEK_CH_TH 796
8.3.17 AGC_TBL_RFRSSI0 796
8.3.18 AGC_TBL_RFRSSI1 797
8.3.19 AGC_TBL_WBRSSI 797
8.3.20 AGC_IDX_TH 798
8.3.21 AGC_RSSI_TH 798
8.3.22 SEEK_ADPS 799
8.3.23 STER_PWR 799
8.3.24 AGC_CTRL 800
8.3.25 AGC_ITV_TH 800
8.3.26 AGC_ADPS0 801
8.3.27 AGC_ADPS1 801
8.3.28 PDP_TH 802
8.3.29 PDP_DEV 802
8.3.30 ADP_ST_CONF 803
8.3.31 ADP_LPF_CONF 803
8.3.32 DEPHA_SCAL 804
8.3.33 HW_MUTE 804
8.3.34 SW_MUTE 805
8.3.35 UPD_CTRL 805
8.3.36 AUD_BLD0 806
8.3.37 AUD_BLD1 806
8.3.38 AGC_HYS 807
8.3.39 MONO_PWR 807
8.3.40 RF_CFG_DLY 808
8.3.41 AGC_TBL_STS 808
8.3.42 ADP_BIT_SFT 809
8.3.43 SEEK_CNT 810
8.3.44 RSSI_STS 810
8.3.45 CHAN_FREQ_STS 811

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

8.3.46 FREQ_OFF_STS 811
8.3.47 INPWR_STS 812
8.3.48 RF_RSSI_STS 812
8.3.49 NO_LPF_STS 813
8.3.50 SMUTE_STS 813
8.3.51 MISC_STS 814
8.3.52 PILOT_STS 815
8.3.53 IQ_CALI_K1_ADDR 815
8.3.54 IQ_CALI_K2_ADDR 816
8.3.55 CALI_STS_ADDR 816
8.3.56 SPUR_FREQ0 817
8.3.57 SPUR_FREQ1 817
8.3.58 IIS_CONFIG1 818
8.3.59 IIS_CONFIG2 818
8.3.60 IIS_CONFIG3 819
8.3.61 IIS_CONFIG4 819
8.3.62 CIC16_CONFIG1 820
8.3.63 CIC16_CONFIG2 820
8.3.64 CIC16_FREQUENCY 821
8.3.65 REG_CTRL1 821
8.3.66 AMP_ADJ 822
8.3.67 IQ_CALI 822
8.3.68 SINE_GEN_ADDR 823
8.3.69 CALI_CTRL 824
8.3.70 RF_CTRL1 824
8.3.71 RF_CTRL2 825
8.3.72 RF_CTRL3 825
8.3.73 SOFTMUTE0 826
8.3.74 SOFTMUTE1 827
8.3.75 SOFTMUTE2 827
8.3.76 SOFTMUTE3 828
8.3.77 SOFTMUTE4 828
8.3.78 SOFTMUTE5 829
8.3.79 DB_COMP 829
8.4 Application Note 830
9 JTAG Debug 832
9.1 Overview 832
9.2 Signal Descriptions 832
9.2.1 Pin Definitions 832
9.3 Operations 832
10 Boot 833
10.1 Overview 833
10.2 Boot Sequence 833
11 Audio System 835
11.1 Overview 835
11.2 Features 835
11.3 Signal Description 836

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

11.4 Function Description 837
11.4.1 AUD Digital Data Path 837
11.4.2 AUD clock structure 837
11.5 Control Registers 840
11.5.1 Memory map 840
11.5.2 AUD Register Descriptions 840
11.5.2.1 AUD_TOP_CTRL 840
11.5.2.2 AUD_CLR 842
11.5.2.3 AUD_IIS_CTRL 842
11.5.2.4 DAC_SRC_CTL 844
11.5.2.5 DAC_SDM_CTL0 845
11.5.2.6 DAC_SDM_CTL1 845
11.5.2.7 ADC_SRC_CTL 846
11.5.2.8 AUD_LOOP_TEST 847
11.5.2.9 AUD_STS0 848
11.5.2.10 AUD_INT_CLR 848
11.5.2.11 AUD_INT_EN 849
11.5.2.12 AUDIF_FIFO_CTL 850
11.5.2.13 AUD_DMIC_CTL 850
11.5.2.14 DAC_SDM_DC_L 851
11.5.2.15 DAC_SDM_DC_H 852
11.5.2.16 AUDIF_CTL0_ADDR 852
11.5.2.17 ADC_FIFO_STS 853
11.5.2.18 DAC_FIFO_STS 853
11.5.2.19 AUDIF_STS 854
11.5.2.20 AUDIF_RAW_STS 855
11.5.2.21 AUDIF_RAW_STS_CLR 855

12 PMU (Power Management Unit) 857

12.1 Overview 857
12.2 LDO 859
12.3 Charger 868
12.3.1 Charging Process 870
12.3.2 Charge standby 871
12.3.3 Recharge Control 871
12.3.4 Over current protection 871
12.3.5 Over voltage protection (hardware) 871
12.3.6 Calibration table 872
12.4 Charge Detector 874
12.4.1 Time out Detect 874
12.5 LCD Backlight LED Driver 874
12.6 Keypad Backlight LED Driver 876
12.7 Auxiliary Analog-to-Digital Converter (ADC) 876
12.8 UVLO 878
12.9 Band-Gap 880
12.10 RTC Reset 880
12.11 Battery Presence Detection 880
12.12 Power on Control 882
12.12.1 Power on Procedure 882

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

12.12.1.1 Introduction 882
12.12.1.2 Timing 884
12.12.2 Power on Sequence 885
12.12.2.1 Power on with Initial VBAT 885
12.12.2.2 Power on with Stable VBAT 885
12.12.2.3 Power on detail sequence between bandgap and LDO/BUCKS 886
12.12.3 Global Reset 886
12.12.3.1 External Pin Reset 886
12.12.3.2 VBAT Monitor Reset 887
12.12.3.3 Watchdog Reset 887
12.12.3.4 Power Key 7s Reset 887
12.13 Power Sleep Control 894
12.13.1 Introduction 894
12.13.2 Interface 895
12.13.3 Register 895
12.13.4 Application note 904
12.13.4.1 LDOCORE 904
12.13.4.2 Other power 904
13 Analog register 906
13.1 Global Register 906
13.1.1 Register Address Map 906
13.1.1.1 CHIP_ID_LOW 909
13.1.1.2 CHIP_ID_HIGH 910
13.1.1.3 MODULE_EN0 910
13.1.1.4 ARM_CLK_EN0 911
13.1.1.5 RTC_CLK_EN0 912
13.1.1.6 SOFT_RST0 913
13.1.1.7 POWER_PD_SW 914
13.1.1.8 POWER_PD_HW 915
13.1.1.9 RESERVED_REG0 915
13.1.1.10 RESERVED_REG1 916
13.1.1.11 RESERVED_REG2 916
13.1.1.12 RESERVED_REG3 917
13.1.1.13 RESERVED_REG4 917
13.1.1.14 RESERVED_REG5 917
13.1.1.15 LDO_CAMA_REG0 918
13.1.1.16 LDO_CAMA_REG1 919
13.1.1.17 LDO_SIM0_REG0 919
13.1.1.18 LDO_SIM0_REG1 920
13.1.1.19 LDO_SIM0_REG2 920
13.1.1.20 LDO_SIM1_REG0 921
13.1.1.21 LDO_SIM1_REG1 922
13.1.1.22 LDO_SIM1_PD_REG 922
13.1.1.23 LDO_SD_REG0 923
13.1.1.24 LDO_SD_REG1 924
13.1.1.25 LDO_SD_REG2 924
13.1.1.26 LDO_VDD28_REG0 925
13.1.1.27 LDO_VDD28_REG1 925

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

13.1.1.28 LDO_BTPA_REG0 926
13.1.1.29 LDO_BTPA_REG1 927
13.1.1.30 LDO_DCXO_REG0 927
13.1.1.31 LDO_DCXO_REG1 928
13.1.1.32 LDO_USB_REG0....928
13.1.1.33 LDO_USB_REG1....929
13.1.1.34 LDO_CAMD_REG0 930
13.1.1.35 LDO_CAMD_REG1 930
13.1.1.36 LDO_SF_REG0 931
13.1.1.37 LDO_SF_REG1 932
13.1.1.38 LDO_VDD18_REG0 932
13.1.1.39 LDO_VDD18_REG1 933
13.1.1.40 LDO_RF_REG0 934
13.1.1.41 LDO_RF_REG1 934
13.1.1.42 LDO_CORE_REG0 935
13.1.1.43 LDO_CORE_REG1 936
13.1.1.44 RESERVED_REG17 936
13.1.1.45 RESERVED_REG18 937
13.1.1.46 RESERVED_REG19 937
13.1.1.47 RESERVED_REG20 938
13.1.1.48 RESERVED_REG21 938
13.1.1.49 RESERVED_REG22 938
13.1.1.50 LDO_CH_CTRL 939
13.1.1.51 LDO_REFTRIM_REG 940
13.1.1.52 RESERVED_REG24 941
13.1.1.53 RESERVED_REG25 941
13.1.1.54 RESERVED_REG26 942
13.1.1.55 RESERVED_REG27 942
13.1.1.56 SLP_CTRL 943
13.1.1.57 SLP_LDO_PD_CTRL0 943
13.1.1.58 SLP_LDO_LP_CTRL0 944
13.1.1.59 LDO_CORE_SLP_CTRL0 946
13.1.1.60 LDO_CORE_SLP_CTRL1 947
13.1.1.61 LDO_CORE_SLP_CTRL2 947
13.1.1.62 LDO_CORE_SLP_CTRL3 948
13.1.1.63 LDO_XTL_EN0 948
13.1.1.64 LDO_XTL_EN1 950
13.1.1.65 XO_BG_XTL_EN 951
13.1.1.66 RESERVED_REG29 951
13.1.1.67 RESERVED_REG30 952
13.1.1.68 RESERVED_REG31 952
13.1.1.69 RESERVED_REG32 953
13.1.1.70 RESERVED_REG33 953
13.1.1.71 RESERVED_REG34 954
13.1.1.72 CLK32KLESS_CTRL0 954
13.1.1.73 CLK32KLESS_CTRL1 955
13.1.1.74 CLK32KLESS_CTRL2 956
13.1.1.75 CLK32KLESS_CTRL3 956

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

13.1.1.76 CLK32KLESS_CTRL4 957
13.1.1.77 AUXAD_CTL 957
13.1.1.78 XTL_WAIT_CTRL 958
13.1.1.79 IB_CTRL 959
13.1.1.80 WHTLED_CTRL 960
13.1.1.81 KPLED_CTRL 961
13.1.1.82 VIBR_CTRL 961
13.1.1.83 AUDIO_CTRL0 962
13.1.1.84 AUDIO_CTRL1 963
13.1.1.85 CHGR_CTRL0 964
13.1.1.86 CHGR_CTRL1 965
13.1.1.87 CHGR_CTRL2 967
13.1.1.88 CHGR_STATUS 968
13.1.1.89 MIXED_CTRL0 969
13.1.1.90 MIXED_CTRL1 970
13.1.1.91 POR_RST_MONITOR 971
13.1.1.92 WDG_RST_MONITOR 971
13.1.1.93 POR_PIN_RST_MONITOR 972
13.1.1.94 POR_SRC_FLAG 972
13.1.1.95 POR_7S_CTRL 973
13.1.1.96 HWRST_RTC 975
13.1.1.97 ARCH_EN 975
13.1.1.98 MCU_WR_PROT_VALUE 976
13.1.1.99 PWR_WR_PROT_VALUE 976
13.1.1.100 SMPL_CTRL0 977
13.1.1.101 SMPL_CTRL1 978
13.1.1.102 RTC_RST0 979
13.1.1.103 RTC_RST1 979
13.1.1.104 RTC_RST2 980
13.1.1.105 RTC_CLK_STOP 980
13.1.1.106 VBAT_DROP_CNT 981
13.1.1.107 SWRST_CTRL0 981
13.1.1.108 SWRST_CTRL1 982
13.1.1.109 OTP_CTRL 983
13.1.1.110 RESERVED_REG35 983
13.1.1.111 RESERVED_REG36 984
13.1.1.112 LOW_PWR_CLK32K_CTRL 984
13.1.1.113 LOW_PWR_CLK32K_TEST0 986
13.1.1.114 LOW_PWR_CLK32K_TEST1 986
13.1.1.115 LOW_PWR_CLK32K_TEST2 987
13.1.1.116 LOW_PWR_CLK32K_TEST3 987

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

1 System Overview

1.1 General Description

SC6531 is a highly integrated single chip with embedded baseband, flash PSRAM and RF transceiver for GSM/GPRS/BT/FM applications, which is designed to provide a cost-effective, low-power and high-performance solution for mobile phones.

SC6531 consists of two embedded 32-bit microcontrollers and an embedded 16-bit DSP core with the specially optimized architecture and dedicated accelerators.

The integrated several RF transceivers (gsm/bt/fm) provide the function of radio frequency signal transmit and receiving from or to baseband signal. Thereby, a total and low cost communication solution can be provided with this highly integrated chip.

The integrated analog baseband processor provides ADCs and DACs for the baseband and voice band up/down links, power management circuits, PLLs, band-gap references, LDO regulators and other auxiliary drivers.

The system timing control provides clocks for the system and controls the mode of the system operations. The system timing control consists of the following parts:

A master clock input, which is the system clock of normal GSM operations and reference clock of on-chip PLLs

- Two PLLs (phase locked loop), to meet different application requirements.
- A real time clock (RTC), used to count the seconds, minutes and hours and to maintain the system timing during the power-saving (sleep) mode
- A scheduler timer, which generates the GSM-specific timing bases.
- A system state machine, which controls the system's normal operation and power-saving (sleep) modes.

The embedded MCU runs a real-time operation system (RTOS), performs the system control functions according to the GSM/GPRS protocol stack, and serves all peripheral components including man-machine interface.

The embedded DSP provides data processing for GSM/GPRS-specific physical layer signal processing, including power measurement of the serving and neighboring cells, frequency estimation and timing tracking, baseband data interleaving/de-interleaving, burst building, channel estimation/equalization, speech encoding/decoding, etc.

The embedded PSRAM /Serial Flash simplifys the design complexity of PCB and reduce the system cost.

SC6531 integrates digital camera processor, Bluetooth, FM, MPEG4/H.263/JPEG codec engines and a rich set of peripherals for functionality extensions, such as SPI , UART, IIS, PCM, I2C, keypad, SIM card, external serial flash memory interface and USB.

1.2 SC6531 Features

General Features

- Integrated GSM/GPRS/FM/BT radio frequency, GSM/GPRS baseband, multi-media, Bluetooth & FM BB and power management unit

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

- Deep sub-micron mixed signal CMOS technology
- External supply voltages: battery 3.6 V (typical), optional backup battery 3.0 V (typical). Internal supply voltages: analog 3.0 V or 3.3 V, digital I/O 2.8 V or 1.8 V (typical), digital core 1.1 V (typical) and RTC power supply 1.8 V (typical)

1.2.1 Platform Features

MCU subsystem

- ARM926EJ-S® 32-bit RISC processor, up to 208 MHz,
- 8KB I-cache and 8KB D-cache
- 10 KB on-chip SRAM
- 88 KB on-chip ROM
- High performance multi-layer AHB-Lite bus system and low power APB system
- Support 32-bit ARM and 16-bit Thumb instructions
- Support Java extension instruction set
- Support boot from FLASH, USB or UART
- Support memory re-mapping mechanism
- Dedicate DMA with 32 logical request channels
- Two general purpose RTC timers for task schedule and system timing recording
- One system timer with 1ms counting scale
- Watchdog timer for system crash recovery
- JTAG port for in-circuit emulation

Note: ARM926EJ-S® is a registered trademark of Advanced RISC Machines Limited.

PSRAM/Serial Flash Configuration

SC6531 supports different configuration for the embedded 8bits-PSRAM and Serial Flash memory as the following table shows.

Series	Name	Internal NorFlash(Mbit)	Internal pSRAM(Mbit)	external device
SC6531	SC6531E	32	32	Not support
	SC6531M	32	32	No BT, No FM

Embeded PSRAM Memory

- Supports embedded PSRAM memory with size up to 128M Bits
- Supports DDR PSRAM of 8-bit data width
- Asynchronous single access
- Synchronous burst access up to 104MHz SDR/DDR

Serial Flash Memory

- External/Sip serial flash memory supported
- one select (CS) supported, capacity up to 256M bits
- Standard SPI mode, SCLK/SDI/SDO
- Dual SPI mode, SCLK/IO0/IO1
- Quad SPI mode, SCLK/IO0/IO1/IO2/IO3
- QPI mode supported

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

- up to 104Mhz SDR/DDR bus clock frequency supported

Peripherals

- Support SDIO 2.0;
- Auxiliary inputs to a 12-bit analog to digital converter (auxiliary ADC) for measurement purposes
- two SIM card interface, support 1.8 V or 3.0 V SIM cards
- 5-row x 5-column keypad controller, support multiple key presses
- Real Time Clock (RTC) and alarm operating at 32.768 kHz with a separate power supply
- General purpose I/Os (GPIO)
- Pulse Width Modulation (PWM) output
- Full-speed USB 1.1 Device controller
- Two sets of UART up to 4.8M baud rate
- Support IrDA
- one set of SPI, support both two-wire and three-wire serial interfaces
- I2S/PCM, for audio codec connection
- two I2C controller, for, e.g., camera configuration

1.2.2 Modem Features

- Compatible with GSM/GPRS Release 1999, DCS1800 and PCS1900 recommendations
- Dedicated GSM/GPRS signal processing engine for equalization, channel encoding/decoding for all traffic and control channels, GMSK modulation and encryption/decryption (A5/1, A5/2 and A5/3, GEA 1, GEA3 and GEA 3 algorithms)
- GMSK modulator with digital I and Q channel outputs
- Calibration mechanism of offset and gain mismatch for baseband A/D converters and D/A converters
- 10-bit D/A converter for Automatic Power Control
- Programmable radio Rx filter
- GSM system timing
- Complete in-phase and quadrature (I/Q) component interface between the Digital Signal Processor (DSP) and RF module
- Dedicated RF serial control interface and parallel control signals
- Programmable GSM/GPRS modem
- Packet switched data with CS1/CS2/CS3/CS4 coding schemes
- Multi-band support
- Complete voice band codec
- Integrated microphone bias
- GSM/GPRS quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
- Five auxiliary analog inputs to a 10-bit analog-to-digital converter (ADC) for measurement purposes
- Support SAIC(single antenna interference cancellation)

1.2.3 Multimedia Features

1.2.3.1 Camera Interface

- Support 1.3M/2M/3M/5M pixel CMOS sensor's JPEG compression mode
- Support up to 2M CMOS sensor's YUV mode capture (restrict to external memory configuration).
- Support SPI sensor up to 0.3M pixel

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

- Support scaling down/up function, scaling factor from 1/4 to 2 in capture or preview mode.
- Support image crop and down sample in camera interface.
- Support frame decimation in camera interface.
- Support slice mode scaling to minimize storage requirement;
- Support scaling down/up function, scaling factor from 1/4 to 4 in review mode.
- Restricted to output width no larger than 480 pixel for display，in preview mode.
- Restricted to output width no larger than 480 pixel for display，in normal review mode.
- If using slice review mode, support output horizontal size up to 4092.
- In review mode, support different YUV input format, include: YUV422,YUV420,YUV400 in review mode.
- In review mode, support Y,U,V 3 frame data format input scaling.
- Support different output data format, YUV422 and RGB565.
- Support image trimming and down sample in review mode. 1/2, 1/4,1/8,1/16 down sample in X and Y direction.
- Support RGB2YUV and YUV2RGB conversion in review mode.
- In review mode, support different RGB format input, RGB888, RGB565.
- ATV fix mode to resolve analog TV noise issue

1.2.3.2 LCD Interface

- Support 2 layer alpha blending, 1 for OSD and 1 for image
- Support YUV422/YUV420/YUV400/RGB888/RGB565/RGB666/RGB555 data format in image layer;
- Support RGB888/RGB565/RGB666/RGB555/GREY data format in OSD1 layer;
- Support color key, one layer with same color key;
- Support dithering;
- Support writing back to memory, data can be RGB888/RGB565/RGB666;
- Support FMARK panel;
- Support MCU I/F with NLCM, data type can be RGB565/RGB666, bus type can be 8bits/9bits;

1.2.3.3 Image Codec

- Support JPEG decoding, compliant with JPEG baseline profile, support YUV444, YUV422, YUV420, YUV411 and Gray format, up to 2M pixels, supports YUV420, YUV422 and YUV411 output.
- Support JPEG encoding, compliant with JPEG baseline profile, support YUV422 format only, quality is adjustable, up to 2M pixels(restrict to the YUV frame buffer constraint).
- Support pixel domain down sample when JPEG decoding. (1/2 or 1/4 down sample in X and Y direction).
- Support slice level codec switch for JPEG.
- Support JPEG progressive mode.

1.2.3.4 Video Codec

- Support MPEG4 decoding, compliant with ISO/IEC 14496-simple profile.HVGA 30fps.
- Support MPEG4 ASP B frame decoding
- Support H263 decoding, compliant with ITU H.263 profile 0. HVGA 30fps.
- Support Flash video format.

1.2.3.5 Audio Codec

- Wavetable synthesis with up to 64 tones
- Two differential microphone input with a 0~20 dB boost gain stage
- A programmable gain amplifier in front of ADC

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

- An analog stereo mixer with programmable gains to mix signals coming from DAC and the stereo line inputs (analog bypass path)
- A stereo programmable gain amplifier for headphone outputs
- Programmable sampling frequencies (Fs) for ADC and DAC: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, and 48 kHz
- 16-bit linear PCM voice data, programmable DAC/ADC, data buffer sizes from 1 to 160, support DMA
- Both ARM and DSP can control the audio codec

1.2.4 Bluetooth Features

- Compliant with Bluetooth2.1 +EDR specification
- Bluetooth Piconet and Scatternet support
- Receiver with -88dBm sensitivity
- Support BT-WIFI Co-existence with 3-wire/2-wire handshake
- Support AFH
- Low power consumption

1.2.5 FM Features

- Supporting frequency range of 76MHz ~ 108MHz
- 2-bits ΣΔ ADC
- DDFS for 100kHZ IF-signal down-conversion
- CORDIC - based FM detector
- Stereo decoder with weak signal processing
- Stereo Mono blending and auto selectivity
- Noise blanking
- De-emphasis filter can be configured with τ=50μs (Europe and Japan) and τ=75μs
- Soft/Hardware audio mute function
- Signal level detection for FM signal quality information
- AGC control feedback
- Frequency offset cancellation

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

1.3 Chip Architecture

Chip architecture is shown in following diagram, several main sub systems area contained in the chip.

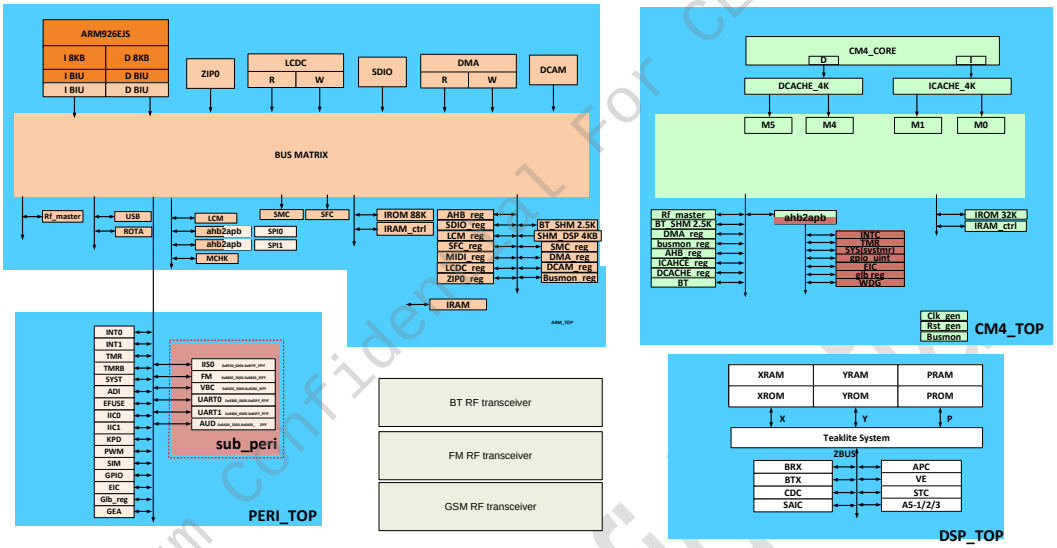


Figure 1-1SC6531 Block diagram

- ARM9 system
- CM4 system
- PERI system
- TEAKLITE system
- BT RF transceiver
- FM RF transceiver
- GSM RF transceiver

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

1.4 Applications

Following figure illustrates a typical application.

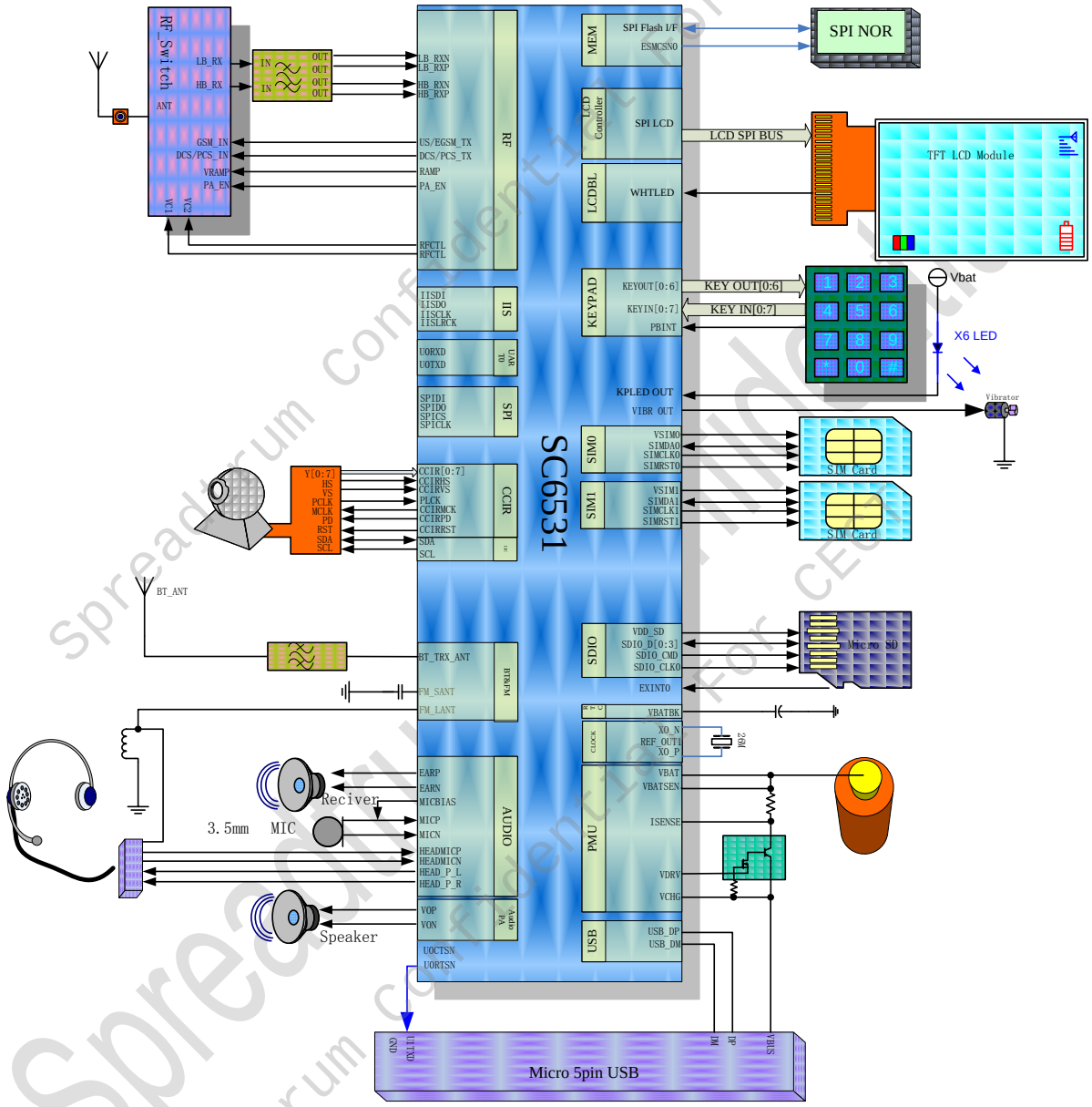


Figure 1-2 Chip Architecture

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

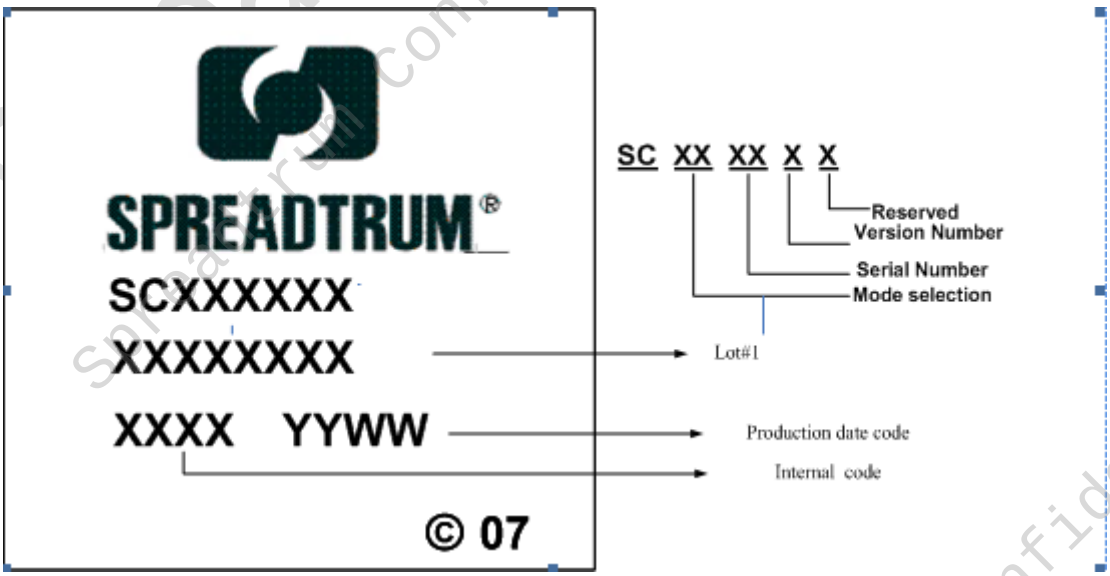
2 Package Information

Plastic-encapsulated surface mount packages are sensitive to damage induced by absorbed moisture and temperature. ALL the chips are MSL 3, which had been marked on the label for every package.

PKG Type	**TF BGA**
Number of Layers	**2**
Device Name	**SC6531E**
Body Size	**7.8X7.8 mm**
Ball count	**175**
Ball Pitch	**0.4mm**
Ball Size	**0.25mm**
Ball Matrix	**19X19**

PKG Type	**TF BGA**
Number of Layers	**2**
Device Name	**SC6531M**
Body Size	**7.8X7.8 mm**
Ball count	**175**
Ball Pitch	**0.4mm**
Ball Size	**0.25mm**
Ball Matrix	**19X19**

2.1 Top Marketing Definition



This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Figure 2-1 Top Marketing Definition

2.2 BGA Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A	NC	U0RTS	CCIRD[4]			CAM_PD	CCIRMCK			SPI1_DO	EXTINT1			NC	NC			SIMRST0	NC	A
B	MTMS	U0TXD	CCIRD[5]	CCIRD[3]		CAM_RSTN	CCIRVS	SCL0		SPI1_CD	SPI1_DI	NC		NC	SPI0_DI	SPI0_CS0		SIMDA0	SIMCLK1	B
C			CCIRHS	CCIRD[1]	CCIRD[2]	CCIRD[0]	SDA0	FMARK	SPI1_CS	SPI1_CLK	EXTINT0		NC	NC	SPI0_DO	SIMCLK0	SIMDA1	SD_CLK	SD_D3	C
D		U0RXD	CCIRD[7]		VCAM	CMPCLK		LCMRSTN	VLCM		PADM_USB		PADP_USB		CLK_AUX0	SPI0_CLK	SIMRST1	SD_CMD		D
E	MTCK	U0CTS	CCIRD[6]														SD_D2			E
F	GPIO_3	GPIO_1	VLCAM													VDDSIM0	SD_D0	IISLRCK	IISDO	F
G			PWM0														SD_D1	IISDI	IISCLK	G
H		GPIO_2	GPIO_0				VDDCORE		VSS	VSS	VSS	VSS					VBATBK	ADCI1		H
J	BT_TRX	FM_LANT	VSS		VSS	VSS			VSS		VSS	VSS					EXTRSTN			J
K		VSS			VSS	VSS			VSS	VSS		VSS				VDDSD	PRODT	BATON	PBINT	K
L	FM_SANT		VRF		VSS				VSS	VSS		VSS					VBATA	VDDCAMA	VDDCAMD	L
M		VSS	VSS									VSS					VDDVIBR	VDDSIM1		M
N	RF_RX_LB_N	RF_RX_LB_P	VSS														VDDSF			N
P	RF_RX_HBP	RF_RX_HBN	VSS	RFPA_EN	APCOUT									VSS			VDDUSB		KPLED_OUT	P
R			RFCTL[0]										VBATB				VBAT_SENSE	VDRV	WHTLED_IB0	R
T	VSS		VSS						VDD28							VSS	ISENSE	VCHG		T
U			VSS	RFCTL[1]	KEYIN[0]	KEYOUT[4]	KEYOUT[2]	KEYOUT[0]	REFOUT	VDD18	EXT_XTL_EN	VDDRF	AGNDVB	AVDDVB	AVDDVBO	HEADP_L	VSSPA	OUTNPA		U
V	RF_TX_LB	RF_RX_HB	KEYIN[1]		KEYIN[3]	KEYOUT[1]		XO_N	XO_P			HEADMICN	HEADMICP	MICN		HEADP_R	EARP		OUTPPA	V
W	NC	RF_TX_HB	KEYIN[2]		KEYIN[4]	KEYOUT[3]			VDDDCXO		MBIAS	HEADMIC_IN		MICP			EARN	VBATPA	NC	W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	

Figure 2-2 SC6531E BGA Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A	NC	U0RTS	CCIRD[4]			CAM_PD	CCIRMCK			SPI1_DO	EXTINT1			NC	NC			SIMRST0	NC	A
B	MTMS	U0TXD	CCIRD[5]	CCIRD[3]		CAM_RSTN	CCIRVS	SCL0		SPI1_CD	SPI1_DI	NC		NC	SPI0_DI	SPI0_CS0		SIMDA0	SIMCLK1	B
C			CCIRHS	CCIRD[1]	CCIRD[2]	CCIRD[0]	SDA0	FMARK	SPI1_CS	SPI1_CLK	EXTINT0		NC	NC	SPI0_DO	SIMCLK0	SIMDA1	SD_CLK	SD_D3	C
D		U0RXD	CCIRD[7]		VCAM	CMPCLK		LCMRSTN	VLCM		PADM_USB		PADP_USB		CLK_AUX0	SPI0_CLK	SIMRST1	SD_CMD		D
E	MTCK	U0CTS	CCIRD[6]														SD_D2			E
F	GPIO_3	GPIO_1	VLCAM													VDDSIM0	SD_D0	IISLRCK	IISDO	F
G			PWM0														SD_D1	IISDI	IISCLK	G
H		GPIO_2	GPIO_0				VDDCORE		VSS	VSS	VSS	VSS					VBATBK	ADCI1		H
J	NC	NC	VSS		VSS	VSS			VSS		VSS	VSS					EXTRSTN			J
K		VSS			VSS	VSS			VSS	VSS		VSS				VDDSD	PRODT	BATON	PBINT	K
L	NC		VRF		VSS				VSS	VSS		VSS					VBATA	VDDCAMA	VDDCAMD	L
M		VSS	VSS									VSS					VDDVIBR	VDDSIM1		M
N	RF_RX_LB_N	RF_RX_LB_P	VSS														VDDSF			N
P	RF_RX_HBP	RF_RX_HBN	VSS	RFPA_EN	APCOUT									VSS			VDDUSB		KPLED_OUT	P
R			RFCTL[0]										VBATB				VBAT_SENSE	VDRV	WHTLED_IB0	R
T	VSS		VSS						VDD28							VSS	ISENSE	VCHG		T
U			VSS	RFCTL[1]	KEYIN[0]	KEYOUT[4]	KEYOUT[2]	KEYOUT[0]	REFOUT	VDD18	EXT_XTL_EN	VDDRF	AGNDVB	AVDDVB	AVDDVBO	HEADP_L	VSSPA	OUTNPA		U
V	RF_TX_LB	RF_RX_HB	KEYIN[1]		KEYIN[3]	KEYOUT[1]		XO_N	XO_P			HEADMICN	HEADMICP	MICN		HEADP_R	EARP		OUTPPA	V
W	NC	RF_TX_HB	KEYIN[2]		KEYIN[4]	KEYOUT[3]			VDDDCXO		MBIAS	HEADMIC_IN		MICP			EARN	VBATPA	NC	W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	

Figure 2-2 SC6531M BGA Pinout

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

2.3 Package Outline

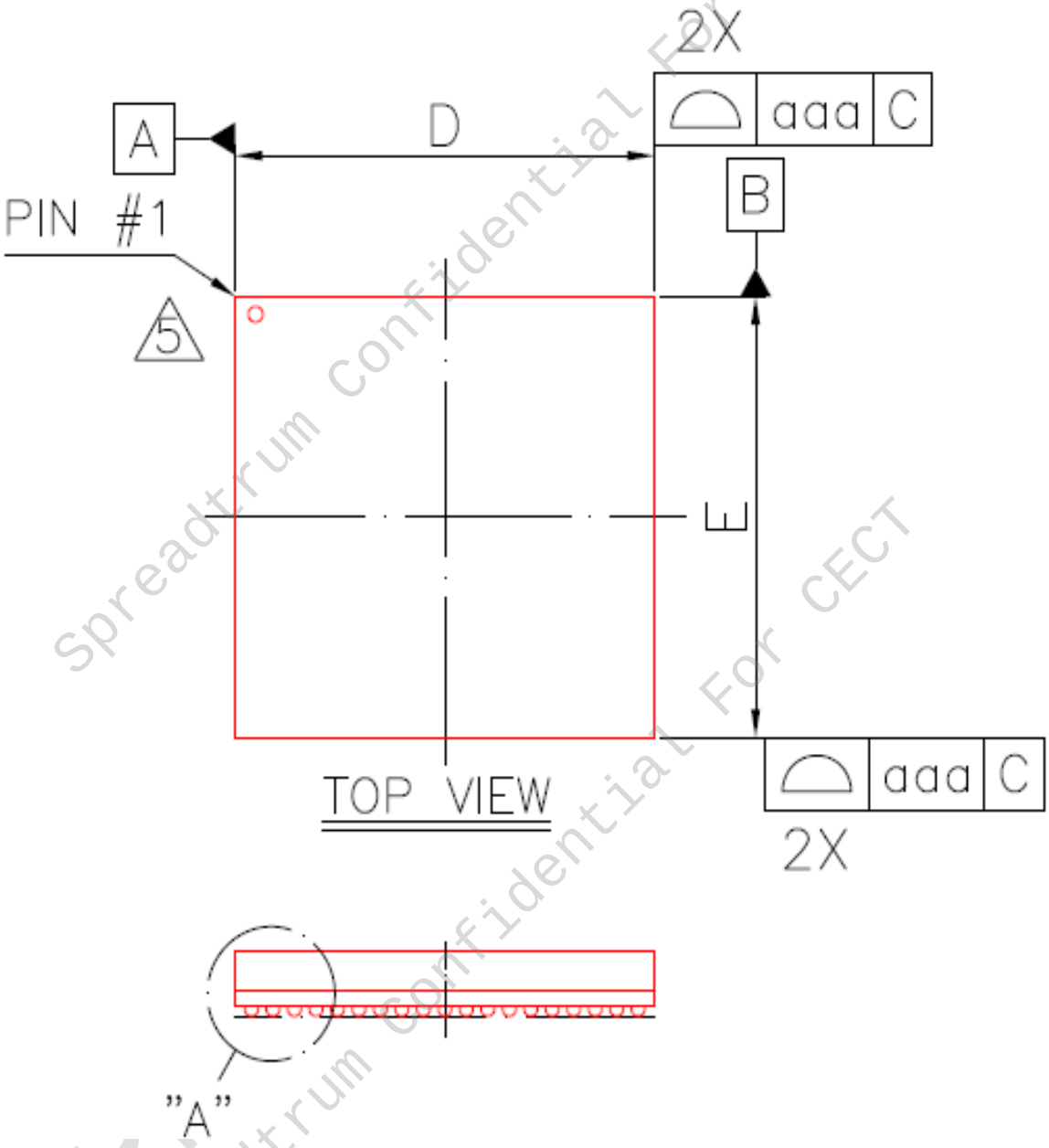


Figure 2-4 Package Outline (Top view)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

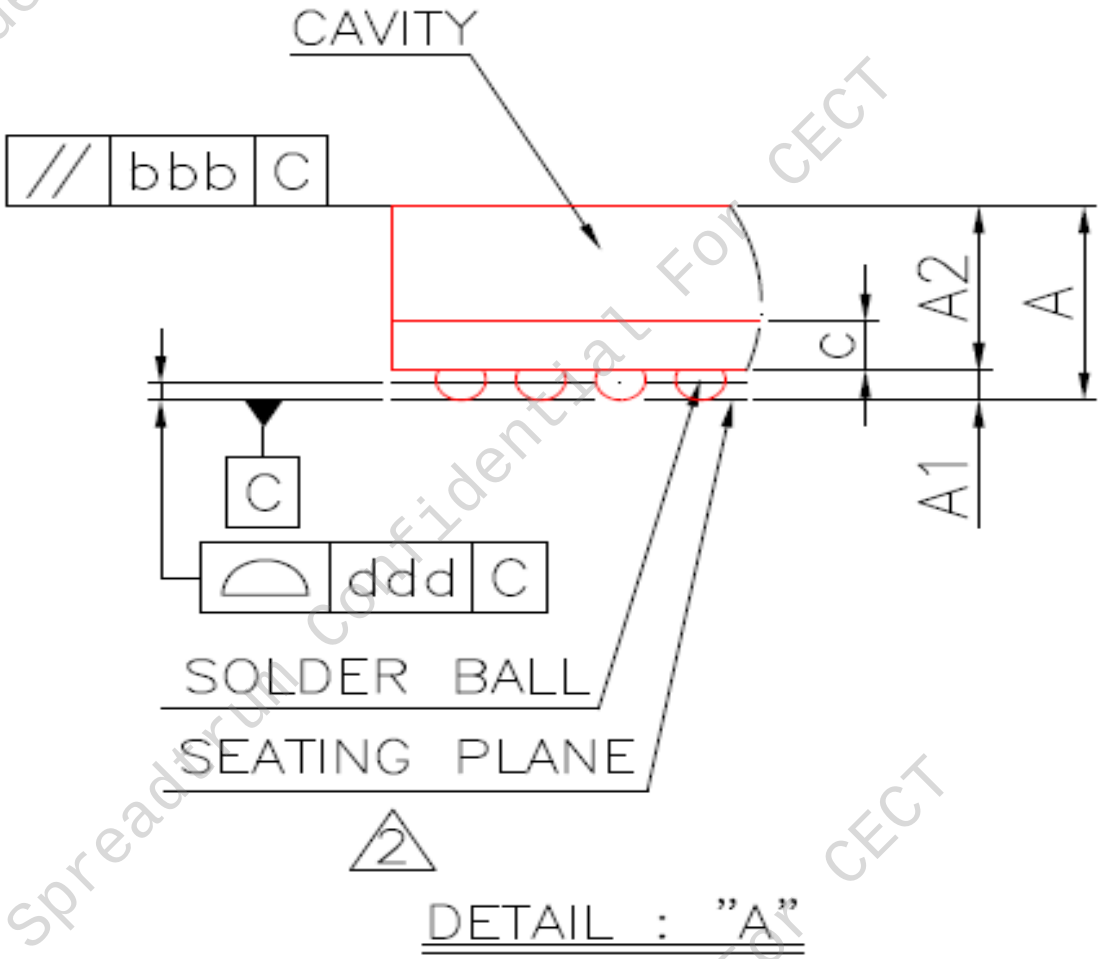


Figure 2-5 Package Outline (Top view)

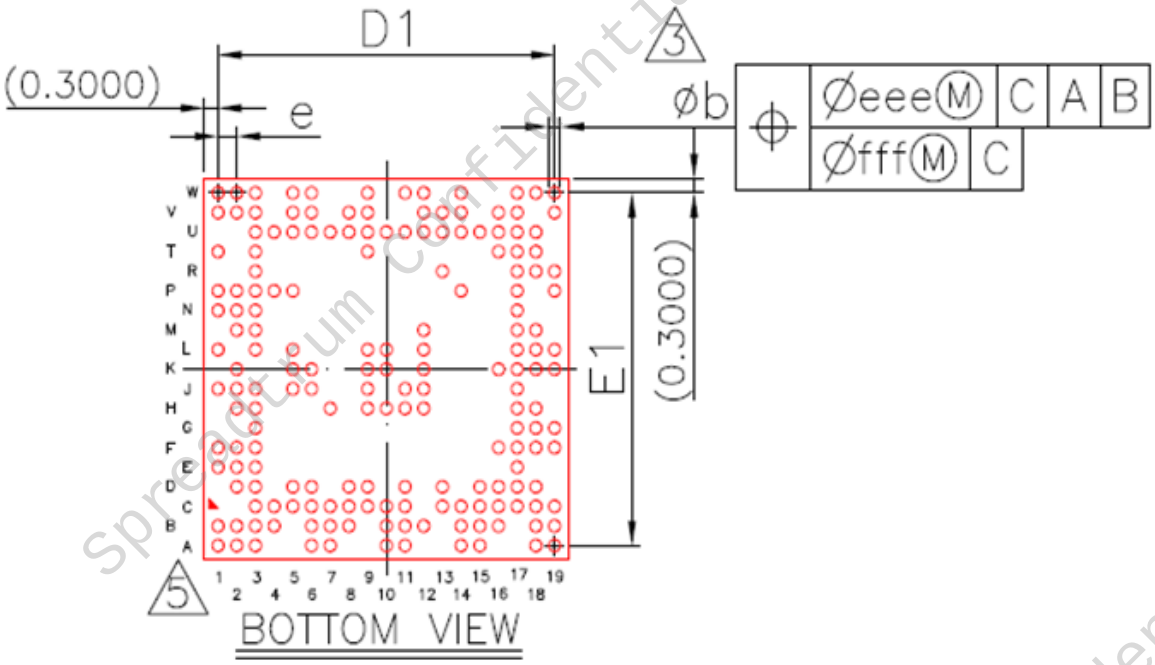


Figure 2-6 Package Outline (Bottom view)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.0690	1.1400	1.2110	0.0421	0.0449	0.0477
A1	0.1300	0.1800	0.2300	0.0051	0.0071	0.0091
A2	0.9100	0.9600	1.0100	0.0358	0.0378	0.0398
c	0.2200	0.2600	0.3000	0.0087	0.0102	0.0118
D	7.7000	7.8000	7.9000	0.3031	0.3071	0.3110
E	7.7000	7.8000	7.9000	0.3031	0.3071	0.3110
D1	---	7.2000	---	---	0.2835	---
E1	---	7.2000	---	---	0.2835	---
e	---	0.4000	---	---	0.0157	---
b	0.2000	0.2500	0.3000	0.0079	0.0098	0.0118
aaa	0.1000			0.0039		
bbb	0.1000			0.0039		
ddd	0.0800			0.0031		
eee	0.1500			0.0059		
fff	0.0500			0.0020		
MD/ME	19/19					

Figure 2-7 Package Outline (Dimension)

2.4 Reflow Profile

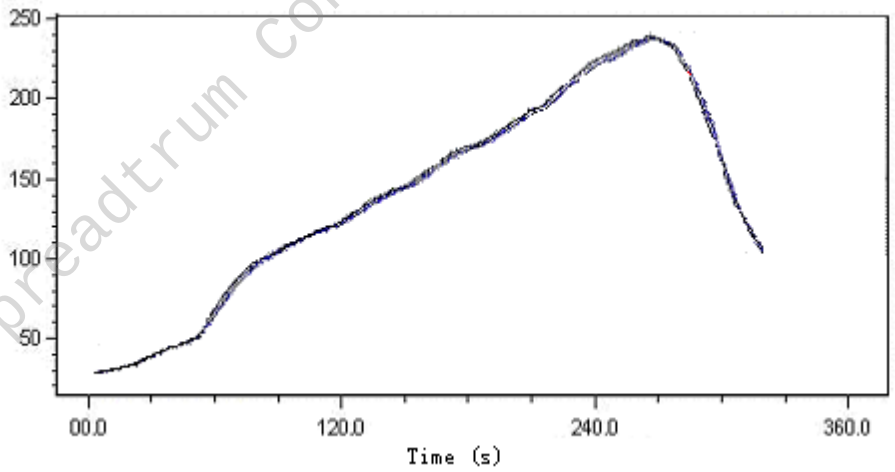


Figure 1-9 Reflow profile

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Note:

1) Recommended reflow profile for lead-free solder paste
- Ramp at 1-2°C per second to 245+/-5°C
- Dwell at 235°C for 10 seconds
- Dwell at 217°C for 30~60s
- Total reflow time is about 220~270 s
- Cold down ramp < 4°C/s

2) Recommended solder paste type
- SnAgCu solder paste
- Metal contents should be about 88.5%

3) Recommended parameter for stencil making
- Metal mask thickness: 5 mils
- Opening area ratio: 100%

Spreadtrum Confidential
Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

3 Pin Information

3.1 Pin symbol descriptions

Field	Symbol	Type Description
Pin Type	I	Digital input
	O	Digital output
	O/T	Digital output with tri-state option
	I/O	Digital bi-directional pin
	I/O/T	Digital bi-directional pin with tri-state option
	PI	Power pin, input from external power supply
	PIO	Power pin, input from external or floating to use internal LDO power supply
	PO	Power pin, output for external devices
	G	Ground pin
	AI	Analog input pin
	AO	Analog output pin
	AIO	Analog bi-directional pin
Pin Value	IPU	Input with pull-up
	IPD	Input with pull-down
	OH	Output “1”
	OL	Output “0”
	Z	Tri-state
Power	VBAT	Battery power supply input
	VDDCORE	Power supply for core, the internal power source are DCDCCORE
	VIO	Power supply for I/O, the internal power source is VDD18 or VDD28
	VDDSD	Power supply for SDIO, the internal power source is VDDSD
	VDDSIM0 /VDDSIM1	Power supply for SIM card 0/1/2, the internal power source are VDDSIM0/VDDSIM1
	VDDSF	Power supply for SPI Flash

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

3.2 Pin List

3.2.1 SC6531E

Ball No	Ball Name	Power	Pull up	Pull down	Driver strength	At reset	After reset	Description
LCM interface								
C8	FMARK	VLCM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd	ie=1,oe=0,wpd	LCM frame mark input
D8	LCMRSTN	VLCM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0	ie=0,oe=1,0	LCM reset output
B11	SPI1_DI	VLCM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=0,wpd	ie=0,oe=0,wpd	LCM write output/ SPI data input
A10	SPI1_DO	VLCM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=0,wpd	ie=0,oe=0,wpd	SPI data output
C10	SPI1_CLK	VLCM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=0,wpd	ie=0,oe=0,wpd	LCM data and command/SPI serial clock output
C9	SPI1_CS	VLCM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=0,wpd	ie=0,oe=0,wpd	LCM chip select/SPI chip select output
B10	SPI1_CD	VLCM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=0,wpd	ie=0,oe=0,wpd	LCM data0/SPI data and command output
Camera interface								
D6	CMPCLK	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera clock input/SPI serial clock
A7	CCIRMCK	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0,fun_sel=1	ie=0,oe=1,0,fun_sel=1	Camera clock output

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

C6	CCIRD0	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data0/SPI data0 input
C4	CCIRD1	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data1/SPI data1 input
C5	CCIRD2	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data2
B4	CCIRD3	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data3
A3	CCIRD4	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data4
B3	CCIRD5	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data5
E3	CCIRD6	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data6
D3	CCIRD7	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data7
C3	CCIRHS	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,fun_sel=0	ie=1,oe=0,fun_sel=0	Camera synchronization input
B7	CCIRVS	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,fun_sel=0	ie=1,oe=0,fun_sel=0	Camera synchronization input/SPI data1 input
A6	CAM_PD	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera power down output
B6	CAM_RSTN	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera reset output
B8	SCL0	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu,fun_sel=3	ie=1,oe=0,wpu,fun_sel=3	IIC clock
C7	SDA0	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu,fun_sel=3	ie=1,oe=0,wpu,fun_sel=3	IIC data
RF interface								
R3	RFCTL0	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	RF control output0
U4	RFCTL1	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	RF control output1
P5	APCOUT	VDD28						RF PA power control output

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

P4	RFPA_EN	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	RF PA enable output
Keypad interface								
U8	KEYOUT0	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0	ie=0,oe=1,0	Keypad output0
V6	KEYOUT1	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=0	ie=0,oe=0	Keypad output1
U7	KEYOUT2	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Keypad output2
W6	KEYOUT3	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Keypad output3
U6	KEYOUT4	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Keypad output4
U5	KEYIN0	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	Keypad input0
V3	KEYIN1	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	Keypad input1
W3	KEYIN2	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Keypad input2
V5	KEYIN3	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Keypad input3
W5	KEYIN4	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Keypad input4
UART interface								
B2	U0TXD	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0, oe=1, 1	ie=0, oe=1, 1	UART serial data output
D2	U0RXD	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	UART serial data input
E2	U0CTS	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	UART clear to send
A2	U0RTS	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=0,oe=1,1	UART require to send
GPIO								
C11	EXTINT0	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	External interrupt channel 0
A11	EXTINT1	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	External interrupt channel 1
H3	GPIO_	VDD	(1.8V,120K/9K)	(1.8V,240K	2/6/12/2	ie=1,oe=0,wp	ie=1,oe=0,wp	General

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	0	28	(3V,60K/4.7K)	)(3V,120K)	4	d,fun_sel=3	d,fun_sel=3	IO
F2	GPIO_1	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	General IO
H2	GPIO_2	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	General IO
F1	GPIO_3	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	General IO
IIS interface								
G18	IISDI	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	IIS data input
F19	IISDO	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	IIS data output
G19	IISCLK	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	IIS system clock
F18	IISLRCK	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	IIS left right select
JTAG interface								
E1	MTCK	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd	ie=1,oe=0,wpd	JTAG test clock input
B1	MTMS	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	JTAG test mode selection input
SPI interface								
D16	SPI0_CLK	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	SPI system clock
B16	SPI0_CS	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	SPI chip select
B15	SPI0_DI	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	SPI data input
C15	SPI0_DO	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	SPI data output
SDIO interface								
C18	SD_CLK	VDDSD	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=1,0	ie=1,oe=1,0	SDIO system clock
D18	SD_CMD	VDDSD	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	SDIO command data output
F17	SD_D0	VDDSD	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	SDIO data0
G17	SD_D1	VDDSD	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	SDIO data1

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

E17	SD_D2	VDD SD	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	SDIO data2
C19	SD_D3	VDD SD	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	SDIO data3
SIM interface								
C16	SIMCLK0	VDD SIM0	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0	ie=0,oe=1,0	SIM0 clock
B18	SIMDA0	VDD SIM0	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	SIM0 data
A18	SIMRST0	VDD SIM0	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0	ie=0,oe=1,0	SIM0 reset
B19	SIMCLK1	VDD SIM1	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0	ie=0,oe=1,0	SIM1 clock
C17	SIMDA1	VDD SIM1	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	SIM1 data
D17	SIMRST1	VDD SIM1	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0	ie=0,oe=1,0	SIM1 reset
Clock interface								
D15	CLK_AUX	VDD 28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0	ie=0,oe=1,0	Aux clock output
G3	PWM	VDD 28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	PWM output
Audio interface								
W11	MBIAS							Micphone power output
W14	MICP							Micphone positive input
V14	MICN							Micphone negative input
V13	HEADMICP							Headmicphone positive input
V12	HEADMICN							Headmicphone negative input
W12	HEADMIC_IN							Headset insert detect
U16	HEADP_L							Headset left

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

								output
V16	HEADP_R							Headset right output
V17	EARP							Receiver positive output
W17	EARN							Receiver negative output
V19	OUTPPA							Speaker PA positive output
U18	OUTNPA							Speaker PA negative output
U17	VSSPA							Speaker PA ground
U13	AGNDVB							Voice band system ground
USB interface								
D13	USB_DP							USB DP
D11	USB_DM							USB DM
System interface								
H18	AUXADC							Aux ADC input
J17	EXTRSTN							External reset input
K19	PBINT							Power on interrupt input
K17	PRODT							Product test mode
U11	EXT_XTL_EN							External wake up input
BT and FM interface								
J1	BT_TRX							BT RF antenna input

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

J2	FM_LANT							FM long antenna input
L1	FM_SANT							FM short antenna input
RF interface								
N2	RF_RX_LB_P							RF receive low band positive input
N1	RF_RX_LB_N							RF receive low band negative input
V2	RF_RX_HB							RF receive high band input to internal balun
P1	RF_RX_HBP							RF receive high band positive input
P2	RF_RX_HBN							RF receive high band negative input
W2	RF_TX_HB							RF transmit high band output
V1	RF_TX_LB							RF transmit low band output
V9	XO_P							26M crystal positive
V8	XO_N							26M

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

								crystal negative
U9	REFOUT							Reference clock output
Power interface								
L17	VBATA							Battery input
R13	VBATB							Battery input
W18	VBATPA							Battery input for audio speaker PA
U15	AVDDVBO							Analog power supply need bypass capacitor
U14	AVDDVB							Analog power supply need bypass capacitor
U12	VDDRF							RF power supply output
U10	VDD18							Digital power 1V8 output
T9	VDD28							Digital power 2V8 output
H7	VDDCORE							Digital core power output
W9	VDDDCXO							DCXO power output
K16	VDDSD							SD power output
L19	VDDC							Camera

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	AMD							digital power output
L18	VDDCAMA							Camera analog power output
F16	VDDSIM0							SIM0 power output
M18	VDDSIM1							SIM1 power output
P17	VDDUSB							USB 3V3 power output
N17	VDDSF							SPI flash power output
M17	VDDVIBR							Vibrator power output
R19	WHTLED_IB							White LED power sink
P19	KPLED_OUT							Keypad LED power input
H17	VBATBK							Button cell power output
Charge interface								
R17	VBAT_SENSE							Battery voltage detect
T17	ISENSE							Charge current detect
R18	VDRV							Charge driver control output
T18	VCHG							Adpater power input
K18	BATDET							Battery present detect
Power input								

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

F3	VLCAM							LCM and Camera power input
D9	VLCM							LCM power input
D5	VCAM							Camera power input
L3	VRF							RF analog power input
System Ground								
H9	VSS							Ground
H10	VSS							Ground
H11	VSS							Ground
H12	VSS							Ground
J3	VSS							Ground
J5	VSS							Ground
J6	VSS							Ground
J9	VSS							Ground
J11	VSS							Ground
J12	VSS							Ground
K2	VSS							Ground
K5	VSS							Ground
K6	VSS							Ground
K9	VSS							Ground
K10	VSS							Ground
K12	VSS							Ground
L5	VSS							Ground
L9	VSS							Ground
L10	VSS							Ground
L12	VSS							Ground
M2	VSS							Ground
M3	VSS							Ground
M12	VSS							Ground
N3	VSS							Ground
P3	VSS							Ground
T1	VSS							Ground
T3	VSS							Ground
U3	VSS							Ground
P14	VSS							Ground
T16	VSS							Ground

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

NC BALL								
A1	NC							NC
A19	NC							NC
W1	NC							NC
W19	NC							NC
B14	NC							NC
C14	NC							NC
A14	NC							NC
A15	NC							NC
B12	NC							NC
C13	NC							NC

3.2.2 SC6531M

Ball No	Ball Name	Power	Pull up	Pull down	Driver strength	At reset	After reset	Description
LCM interface								
C8	FMARK	VLCM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd	ie=1,oe=0,wpd	LCM frame mark input
D8	LCMRSTN	VLCM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0	ie=0,oe=1,0	LCM reset output
B11	SPI1_DI	VLCM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=0,wpd	ie=0,oe=0,wpd	LCM write output/ SPI data input
A10	SPI1_DO	VLCM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=0,wpd	ie=0,oe=0,wpd	SPI data output
C10	SPI1_CLK	VLCM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=0,wpd	ie=0,oe=0,wpd	LCM data and command/SPI serial clock output
C9	SPI1_CS	VLCM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=0,wpd	ie=0,oe=0,wpd	LCM chip select/SPI chip select output
B10	SPI1_CD	VLCM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=0,wpd	ie=0,oe=0,wpd	LCM data0/SPI data and

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

								command output
Camera interface								
D6	CMPCLK	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera clock input/SPI serial clock
A7	CCIRMCK	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0,fun_sel=1	ie=0,oe=1,0,fun_sel=1	Camera clock output
C6	CCIRD0	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data0/SPI data0 input
C4	CCIRD1	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data1/SPI data1 input
C5	CCIRD2	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data2
B4	CCIRD3	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data3
A3	CCIRD4	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data4
B3	CCIRD5	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data5
E3	CCIRD6	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data6
D3	CCIRD7	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera data7
C3	CCIRHS	VLCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,fun_sel=0	ie=1,oe=0,fun_sel=0	Camera synchronization input
B7	CCIRVS	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,fun_sel=0	ie=1,oe=0,fun_sel=0	Camera synchronization input/SPI data1 input
A6	CAM_PD	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera power down output
B6	CAM_RSTN	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Camera reset output
B8	SCL0	VCAM	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu,fun_sel=3	ie=1,oe=0,wpu,fun_sel=3	IIC clock
C7	SDA0	VCA	(1.8V,120K/9K)	(1.8V,240K	2/6/12/2	ie=1,oe=0,wp	ie=1,oe=0,wp	IIC data

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

		M	(3V,60K/4.7K)	)(3V,120K)	4	u,fun_sel=3	u,fun_sel=3	
RF interface								
R3	RFCTL0	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	RF control output0
U4	RFCTL1	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	RF control output1
P5	APCOUT	VDD28						RF PA power control output
P4	RFPA_EN	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	RF PA enable output
Keypad interface								
U8	KEYOUT0	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0	ie=0,oe=1,0	Keypad output0
V6	KEYOUT1	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=0	ie=0,oe=0	Keypad output1
U7	KEYOUT2	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Keypad output2
W6	KEYOUT3	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Keypad output3
U6	KEYOUT4	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Keypad output4
U5	KEYIN0	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	Keypad input0
V3	KEYIN1	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	Keypad input1
W3	KEYIN2	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Keypad input2
V5	KEYIN3	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Keypad input3
W5	KEYIN4	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	Keypad input4
UART interface								
B2	U0TXD	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0, oe=1, 1	ie=0, oe=1, 1	UART serial data output
D2	U0RXD	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	UART serial data input
E2	U0CTS	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	UART clear to send
A2	U0RTS	VDD28	(1.8V,120K/9K) (3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=0,oe=1,1	UART require

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

								to send
GPIO								
C11	EXTINT0	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	External interrupt channel 0
A11	EXTINT1	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	External interrupt channel 1
H3	GPIO_0	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	General IO
F2	GPIO_1	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	General IO
H2	GPIO_2	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	General IO
F1	GPIO_3	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	General IO
IIS interface								
G18	IISDI	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	IIS data input
F19	IISDO	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	IIS data output
G19	IISCLK	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	IIS system clock
F18	IISLRCK	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	IIS left right select
JTAG interface								
E1	MTCK	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd	ie=1,oe=0,wpd	JTAG test clock input
B1	MTMS	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	JTAG test mode selection input
SPI interface								
D16	SPI0_CLK	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	SPI system clock
B16	SPI0_CS	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	SPI chip select
B15	SPI0_DI	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	SPI data input
C15	SPI0_DO	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpd,fun_sel=3	ie=1,oe=0,wpd,fun_sel=3	SPI data output

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SDIO interface								
C18	SD_CLK	VDDSD	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=1,0	ie=1,oe=1,0	SDIO system clock
D18	SD_CMD	VDDSD	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	SDIO command data output
F17	SD_D0	VDDSD	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	SDIO data0
G17	SD_D1	VDDSD	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	SDIO data1
E17	SD_D2	VDDSD	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	SDIO data2
C19	SD_D3	VDDSD	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	SDIO data3
SIM interface								
C16	SIMCLK0	VDDSIM0	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0	ie=0,oe=1,0	SIM0 clock
B18	SIMDA0	VDDSIM0	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	SIM0 data
A18	SIMRST0	VDDSIM0	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0	ie=0,oe=1,0	SIM0 reset
B19	SIMCLK1	VDDSIM1	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0	ie=0,oe=1,0	SIM1 clock
C17	SIMDA1	VDDSIM1	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	SIM1 data
D17	SIMRST1	VDDSIM1	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0	ie=0,oe=1,0	SIM1 reset
Clock interface								
D15	CLK_AUX	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=0,oe=1,0	ie=0,oe=1,0	Aux clock output
G3	PWM	VDD28	(1.8V,120K/9K)(3V,60K/4.7K)	(1.8V,240K)(3V,120K)	2/6/12/24	ie=1,oe=0,wpu	ie=1,oe=0,wpu	PWM output
Audio interface								
W11	MBIAS							Micphone power output
W14	MICP							Micphone positive input
V14	MICN							Micphone negative input
V13	HEADMICP							Head micpho

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

								ne positive input
V12	HEADMICN							Headmicphone negative input
W12	HEADMIC_IN							Headset insert detect
U16	HEADP_L							Headset left output
V16	HEADP_R							Headset right output
V17	EARP							Receiver positive output
W17	EARN							Receiver negative output
V19	OUTPPA							Speaker PA positive output
U18	OUTNPA							Speaker PA negative output
U17	VSSPA							Speaker PA ground
U13	AGNDVB							Voice band system ground
USB interface								
D13	USB_DP							USB DP
D11	USB_DM							USB DM
System interface								
H18	AUXADC							Aux ADC input
J17	EXTRSTN							External reset input
K19	PBINT							Power on

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

								interrupt input
K17	PRODT							Product test mode
U11	EXT_XTL_EN							External wake up input
RF interface								
N2	RF_RX_LB_P							RF receive low band positive input
N1	RF_RX_LB_N							RF receive low band negative input
V2	RF_RX_HB							RF receive high band input to internal balun
P1	RF_RX_HBP							RF receive high band positive input
P2	RF_RX_HBN							RF receive high band negative input
W2	RF_TX_HB							RF transmit high band output
V1	RF_TX_LB							RF transmit low band output
V9	XO_P							26M crystal positive

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

V8	XO_N							26M crystal negative
U9	REFOUT							Reference clock output
Power interface								
L17	VBATA							Battery input
R13	VBATB							Battery input
W18	VBATPA							Battery input for audio speaker PA
U15	AVDDVBO							Analog power supply need bypass capacitor
U14	AVDDVB							Analog power supply need bypass capacitor
U12	VDDRF							RF power supply output
U10	VDD18							Digital power 1V8 output
T9	VDD28							Digital power 2V8 output
H7	VDDCORE							Digital core power output
W9	VDDDCXO							DCXO power output
K16	VDDSD							SD power output

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

L19	VDDCAMD							Camera digital power output
L18	VDDCAMA							Camera analog power output
F16	VDDSIM0							SIM0 power output
M18	VDDSIM1							SIM1 power output
P17	VDDUSB							USB 3V3 power output
N17	VDDSF							SPI flash power output
M17	VDDVIBR							Vibrator power output
R19	WHTLED_IB							White LED power sink
P19	KPLED_OUT							Keypad LED power input
H17	VBATBK							Button cell power output
Charge interface								
R17	VBAT_SENSE							Battery voltage detect
T17	ISENSE							Charge current detect
R18	VDRV							Charge driver control output
T18	VCHG							Adpater power input
K18	BATDET							Battery present detect

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Power input								
F3	VLCAM							LCM and Camera power input
D9	VLCM							LCM power input
D5	VCAM							Camera power input
L3	VRF							RF analog power input
System Ground								
H9	VSS							Ground
H10	VSS							Ground
H11	VSS							Ground
H12	VSS							Ground
J3	VSS							Ground
J5	VSS							Ground
J6	VSS							Ground
J9	VSS							Ground
J11	VSS							Ground
J12	VSS							Ground
K2	VSS							Ground
K5	VSS							Ground
K6	VSS							Ground
K9	VSS							Ground
K10	VSS							Ground
K12	VSS							Ground
L5	VSS							Ground
L9	VSS							Ground
L10	VSS							Ground
L12	VSS							Ground
M2	VSS							Ground
M3	VSS							Ground
M12	VSS							Ground
N3	VSS							Ground
P3	VSS							Ground
T1	VSS							Ground
T3	VSS							Ground
U3	VSS							Ground
P14	VSS							Ground

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

T16	VSS							Ground
NC BALL								
A1	NC							NC
A19	NC							NC
W1	NC							NC
W19	NC							NC
B14	NC							NC
C14	NC							NC
A14	NC							NC
A15	NC							NC
B12	NC							NC
C13	NC							NC
J1	NC							NC
J2	NC							NC
L1	NC							NC

3.3 Pin Multiplexed Function List

3.3.1 SC6531E

Ball No	Ball Name	Function 1	type	Function2	type	Function 3	type	Function4	type
C8	FMARK	FMARK	I					GPIO_29	I/O/T
D8	LCMRSTN	LCMRSTN						GPIO_30	I/O/T
B11	SPI1_DI	SPI1_DI	I/O/T	LCMWR	I/O/T			GPIO_25	I/O/T
A10	SPI1_DO	SPI1_DO	I/O/T					GPIO_26	I/O/T
C10	SPI1_CLK	SPI1_CLK	I/O	LCMCD	I/O/T			GPIO_27	I/O/T
C9	SPI1_CS	SPI1_CS	I/O/T	LCMCS	I/O/T			GPIO_28	I/O/T
B10	SPI1_CD	SPI1_CD	I/O/T	LCMD0	I/O/T			GPIO_64	I/O/T
D6	CMPCLK	CMPCLK	I			SCK	I	GPIO_48	I/O/T
A7	CCIRMCK	CCIRMCK	O	CLK_DSP_DIV	O	CLK_32K_O	O	GPIO_49	I/O/T
C6	CCIRD0	CCIRD0	I			SDI0	I	GPIO_40	I/O/T
C4	CCIRD1	CCIRD1	I	LCMD1	I/O/T	SDI1_0	I	GPIO_41	I/O/T
C5	CCIRD2	CCIRD2	I	LCMD2	I/O/			GPIO_42	I/O/

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					T				T
B4	CCIRD3	CCIRD3	I	LCMD3	I/O/T			GPIO_43	I/O/T
A3	CCIRD4	CCIRD4	I	LCMD4	I/O/T			GPIO_44	I/O/T
B3	CCIRD5	CCIRD5	I	LCMD5	I/O/T			GPIO_45	I/O/T
E3	CCIRD6	CCIRD6	I	LCMD6	I/O/T			GPIO_46	I/O/T
D3	CCIRD7	CCIRD7	I	LCMD7	I/O/T			GPIO_47	I/O/T
C3	CCIRHS	CCIRHS	I	LCMRD	I/O/T			GPIO_50	I/O/T
B7	CCIRVS	CCIRVS	I	SSN	I	SDI1_1	I	GPIO_51	I/O/T
A6	CAM_PD	CAM_PD	O					GPIO_52	I/O/T
B6	CAM_RSTN	CAM_RSTN	O					GPIO_53	I/O/T
B8	SCL0	SCL0	I/O/T					GPIO_54	I/O/T
C7	SDA0	SDA0	I/O/T					GPIO_55	I/O/T
R3	RFCTL0	RFCTL0	O					GPIO_65	I/O/T
U4	RFCTL1	RFCTL1	O					GPIO_66	I/O/T
P4	RFPA_EN	RFPA_EN	O					GPIO_67	I/O/T
U8	KEYOUT0	KEYOUT0	O/T	EXTINT2	I			GPIO_6	I/O/T
V6	KEYOUT1	KEYOUT1	O/T	EXTINT3	I			GPIO_7	I/O/T
U7	KEYOUT2	KEYOUT2	O/T					GPIO_8	I/O/T
W6	KEYOUT3	KEYOUT3	O/T					GPIO_9	I/O/T
U6	KEYOUT4	KEYOUT4	O/T					GPIO_10	I/O/T
U5	KEYIN0	KEYIN0	I	EXTINT4	I			GPIO_11	I/O/T
V3	KEYIN1	KEYIN1	I	EXTINT5	I			GPIO_12	I/O/T
W3	KEYIN2	KEYIN2	I					GPIO_13	I/O/T
V5	KEYIN3	KEYIN3	I	U1TXD_1	O			GPIO_14	I/O/T
W5	KEYIN4	KEYIN4	I	U1RXD_1	I			GPIO_15	I/O/T

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

B2	U0TXD	U0TXD_0	O					GPIO_32	I/O/T
D2	U0RXD	U0RXD_0	I					GPIO_33	I/O/T
E2	U0CTS	U0CTS_0	I	U1RXD_0	I			GPIO_34	I/O/T
A2	U0RTS	U0RTS_0	O	U1TXD_0	O			GPIO_35	I/O/T
C11	EXTINT0	EXTINT0	I					GPIO68	I/O/T
A11	EXTINT1	EXTINT1	I			KEYIN5	I	GPIO69	I/O/T
H3	GPIO_0	GPIO_0	I/O	EXTINT6	I	GPIO_BT_0	I/O/T	GPIO_CM4_0	I/O/T
F2	GPIO_1	GPIO_1	I/O	EXTINT7	I	KEYIN7	I	GPIO_CM4_1	I/O/T
H2	GPIO_2	GPIO_2	I/O	SDA1_2	I/O/T	GPIO_BT_1	I/O/T	GPIO_CM4_2	I/O/T
F1	GPIO_3	GPIO_3	I/O	SCL1_2	I/O/T	GPIO_BT_2	I/O/T	GPIO_CM4_3	I/O/T
G18	IISDI	IISDI	I			KEYOUT6	O	GPIO_16	I/O/T
F19	IISDO	IISDO	O/T	SDA1_1	I/O/T			GPIO_17	I/O/T
G19	IISCLK	IISCLK	I/O	SCL1_1	I/O/T			GPIO_18	I/O/T
F18	IISLRCK	IISLRCK	I/O			KEYIN6	I	GPIO_19	I/O/T
E1	MTCK	MTCK	I	SCL1_0	I/O/T	KEYOUT7	O	GPIO_5	I/O/T
B1	MTMS	MTMS	I/O	SDA1_0	I/O/T	KEYOUT5	O	GPIO_4	I/O/T
D16	SPI0_CLK	SPI0_CLK	I/O	U0TXD_1	O	U1RTS	O	GPIO_21	I/O/T
B16	SPI0_CS	SPI0_CS	I/O/T	U0RXD_1	I	U1CTS	I	GPIO_22	I/O/T
B15	SPI0_DI	SPI0_DI	I/O/T	U0CTS_1	I	U1RXD_2	I	GPIO_23	I/O/T
C15	SPI0_DO	SPI0_DO	I/O/T	U0RTS_1	O	U1TXD_2	O	GPIO_24	I/O/T
C18	SD_CLK	SD_CLK	I/O/T					GPIO_38	I/O/T
D18	SD_CMD	SD_CMD	I/O/T					GPIO_36	I/O/T
F17	SD_D0	SD_D0	I/O/T					GPIO_37	I/O/T
G17	SD_D1	SD_D1	I/O/T					GPIO_56	I/O/T
E17	SD_D2	SD_D2	I/O/T					GPIO_57	I/O/T

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

C19	SD_D3	SD_D3	I/O/T					GPIO_39	I/O/T
C16	SIMCLK0	SIMCLK0	O					GPIO_59	I/O/T
B18	SIMDA0	SIMDA0	I/O/T					GPIO_60	I/O/T
A18	SIMRST0	SIMRST0	O					GPIO_58	I/O/T
B19	SIMCLK1	SIMCLK1	O					GPIO_63	I/O/T
C17	SIMDA1	SIMDA1	I/O/T					GPIO_61	I/O/T
D17	SIMRST1	SIMRST1	O					GPIO_62	I/O/T
D15	CLK_AUX	CLK_AUX	O	CLK_DSP_DIV	O	PWM1	O	GPIO_31	I/O/T
G3	PWM	PWM	O	CLK_AUX 1	O	CLK_32K_O	O	GPIO_20	I/O/T

3.3.2 SC6531M

Ball No	Ball Name	Function 1	type	Function2	type	Function 3	type	Function4	type
C8	FMARK	FMARK	I					GPIO_29	I/O/T
D8	LCMRSTN	LCMRSTN						GPIO_30	I/O/T
B11	SPI1_DI	SPI1_DI	I/O/T	LCMWR	I/O/T			GPIO_25	I/O/T
A10	SPI1_DO	SPI1_DO	I/O/T					GPIO_26	I/O/T
C10	SPI1_CLK	SPI1_CLK	I/O	LCMCD	I/O/T			GPIO_27	I/O/T
C9	SPI1_CS	SPI1_CS	I/O/T	LCMCS	I/O/T			GPIO_28	I/O/T
B10	SPI1_CD	SPI1_CD	I/O/T	LCMD0	I/O/T			GPIO_64	I/O/T
D6	CMPCLK	CMPCLK	I			SCK	I	GPIO_48	I/O/T
A7	CCIRMCK	CCIRMCK	O	CLK_DSP_DIV	O	CLK_32K_O	O	GPIO_49	I/O/T
C6	CCIRD0	CCIRD0	I			SDI0	I	GPIO_40	I/O/T
C4	CCIRD1	CCIRD1	I	LCMD1	I/O/T	SDI1_0	I	GPIO_41	I/O/T
C5	CCIRD2	CCIRD2	I	LCMD2	I/O/			GPIO_42	I/O/

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					T				T
B4	CCIRD3	CCIRD3	I	LCMD3	I/O/T			GPIO_43	I/O/T
A3	CCIRD4	CCIRD4	I	LCMD4	I/O/T			GPIO_44	I/O/T
B3	CCIRD5	CCIRD5	I	LCMD5	I/O/T			GPIO_45	I/O/T
E3	CCIRD6	CCIRD6	I	LCMD6	I/O/T			GPIO_46	I/O/T
D3	CCIRD7	CCIRD7	I	LCMD7	I/O/T			GPIO_47	I/O/T
C3	CCIRHS	CCIRHS	I	LCMRD	I/O/T			GPIO_50	I/O/T
B7	CCIRVS	CCIRVS	I	SSN	I	SDI1_1	I	GPIO_51	I/O/T
A6	CAM_PD	CAM_PD	O					GPIO_52	I/O/T
B6	CAM_RSTN	CAM_RSTN	O					GPIO_53	I/O/T
B8	SCL0	SCL0	I/O/T					GPIO_54	I/O/T
C7	SDA0	SDA0	I/O/T					GPIO_55	I/O/T
R3	RFCTL0	RFCTL0	O					GPIO_65	I/O/T
U4	RFCTL1	RFCTL1	O					GPIO_66	I/O/T
P4	RFPA_EN	RFPA_EN	O					GPIO_67	I/O/T
U8	KEYOUT0	KEYOUT0	O/T	EXTINT2	I			GPIO_6	I/O/T
V6	KEYOUT1	KEYOUT1	O/T	EXTINT3	I			GPIO_7	I/O/T
U7	KEYOUT2	KEYOUT2	O/T					GPIO_8	I/O/T
W6	KEYOUT3	KEYOUT3	O/T					GPIO_9	I/O/T
U6	KEYOUT4	KEYOUT4	O/T					GPIO_10	I/O/T
U5	KEYIN0	KEYIN0	I	EXTINT4	I			GPIO_11	I/O/T
V3	KEYIN1	KEYIN1	I	EXTINT5	I			GPIO_12	I/O/T
W3	KEYIN2	KEYIN2	I					GPIO_13	I/O/T
V5	KEYIN3	KEYIN3	I	U1TXD_1	O			GPIO_14	I/O/T
W5	KEYIN4	KEYIN4	I	U1RXD_1	I			GPIO_15	I/O/T

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

B2	U0TXD	U0TXD_0	O					GPIO_32	I/O/T
D2	U0RXD	U0RXD_0	I					GPIO_33	I/O/T
E2	U0CTS	U0CTS_0	I	U1RXD_0	I			GPIO_34	I/O/T
A2	U0RTS	U0RTS_0	O	U1TXD_0	O			GPIO_35	I/O/T
C11	EXTINT0	EXTINT0	I					GPIO68	I/O/T
A11	EXTINT1	EXTINT1	I			KEYIN5	I	GPIO69	I/O/T
H3	GPIO_0	GPIO_0	I/O	EXTINT6	I	GPIO_BT_0	I/O/T	GPIO_CM4_0	I/O/T
F2	GPIO_1	GPIO_1	I/O	EXTINT7	I	KEYIN7	I	GPIO_CM4_1	I/O/T
H2	GPIO_2	GPIO_2	I/O	SDA1_2	I/O/T	GPIO_BT_1	I/O/T	GPIO_CM4_2	I/O/T
F1	GPIO_3	GPIO_3	I/O	SCL1_2	I/O/T	GPIO_BT_2	I/O/T	GPIO_CM4_3	I/O/T
G18	IISDI	IISDI	I			KEYOUT6	O	GPIO_16	I/O/T
F19	IISDO	IISDO	O/T	SDA1_1	I/O/T			GPIO_17	I/O/T
G19	IISCLK	IISCLK	I/O	SCL1_1	I/O/T			GPIO_18	I/O/T
F18	IISLRCK	IISLRCK	I/O			KEYIN6	I	GPIO_19	I/O/T
E1	MTCK	MTCK	I	SCL1_0	I/O/T	KEYOUT7	O	GPIO_5	I/O/T
B1	MTMS	MTMS	I/O	SDA1_0	I/O/T	KEYOUT5	O	GPIO_4	I/O/T
D16	SPI0_CLK	SPI0_CLK	I/O	U0TXD_1	O	U1RTS	O	GPIO_21	I/O/T
B16	SPI0_CS	SPI0_CS	I/O/T	U0RXD_1	I	U1CTS	I	GPIO_22	I/O/T
B15	SPI0_DI	SPI0_DI	I/O/T	U0CTS_1	I	U1RXD_2	I	GPIO_23	I/O/T
C15	SPI0_DO	SPI0_DO	I/O/T	U0RTS_1	O	U1TXD_2	O	GPIO_24	I/O/T
C18	SD_CLK	SD_CLK	I/O/T					GPIO_38	I/O/T
D18	SD_CMD	SD_CMD	I/O/T					GPIO_36	I/O/T
F17	SD_D0	SD_D0	I/O/T					GPIO_37	I/O/T
G17	SD_D1	SD_D1	I/O/T					GPIO_56	I/O/T
E17	SD_D2	SD_D2	I/O/T					GPIO_57	I/O/T

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

C19	SD_D3	SD_D3	I/O/T					GPIO_39	I/O/T
C16	SIMCLK0	SIMCLK0	O					GPIO_59	I/O/T
B18	SIMDA0	SIMDA0	I/O/T					GPIO_60	I/O/T
A18	SIMRST0	SIMRST0	O					GPIO_58	I/O/T
B19	SIMCLK1	SIMCLK1	O					GPIO_63	I/O/T
C17	SIMDA1	SIMDA1	I/O/T					GPIO_61	I/O/T
D17	SIMRST1	SIMRST1	O					GPIO_62	I/O/T
D15	CLK_AUX	CLK_AUX	O	CLK_DSP_DIV	O	PWM1	O	GPIO_31	I/O/T
G3	PWM	PWM	O	CLK_AUX 1	O	CLK_32K_O	O	GPIO_20	I/O/T

3.4 GPIO List

3.4.1 SC6531E

Ball No	Ball Name	GPIO No	At Reset		After Reset	
			H/L/Hiz	Pin State	H/L/Hiz	Pin State
C8	FMARK	GPIO_29	L	INPUT(WPD)	L	INPUT(WPD)
D8	LCMRSTN	GPIO_30	L	OUTPUT	L	OUTPUT
B11	SPI1_DI	GPIO_25	L	INPUT(WPD)	L	INPUT(WPD)
A10	SPI1_DO	GPIO_26	L	INPUT(WPD)	L	INPUT(WPD)
C10	SPI1_CLK	GPIO_27	L	INPUT(WPD)	L	INPUT(WPD)
C9	SPI1_CS	GPIO_28	L	INPUT(WPD)	L	INPUT(WPD)
B10	SPI1_CD	GPIO_64	L	INPUT(WPD)	L	INPUT(WPD)
D6	CMPCLK	GPIO_48	L	INPUT(WPD)	L	INPUT(WPD)
A7	CCIRMCK	GPIO_49	L	OUTPUT	L	OUTPUT
C6	CCIRD0	GPIO_40	L	INPUT(WPD)	L	INPUT(WPD)
C4	CCIRD1	GPIO_41	L	INPUT(WPD)	L	INPUT(WPD)
C5	CCIRD2	GPIO_42	L	INPUT(WPD)	L	INPUT(WPD)
B4	CCIRD3	GPIO_43	L	INPUT(WPD)	L	INPUT(WPD)
A3	CCIRD4	GPIO_44	L	INPUT(WPD)	L	INPUT(WPD)
B3	CCIRD5	GPIO_45	L	INPUT(WPD)	L	INPUT(WPD)
E3	CCIRD6	GPIO_46	L	INPUT(WPD)	L	INPUT(WPD)
D3	CCIRD7	GPIO_47	L	INPUT(WPD)	L	INPUT(WPD)
C3	CCIRHS	GPIO_50	Hiz	Hiz	Hiz	Hiz
B7	CCIRVS	GPIO_51	Hiz	Hiz	Hiz	Hiz
A6	CAM_PD	GPIO_52	L	INPUT(WPD)	L	INPUT(WPD)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

B6	CAM_RSTN	GPIO_53	L	INPUT(WPD)	L	INPUT(WPD)
B8	SCL0	GPIO_54	H	INPUT(WPU)	H	INPUT(WPU)
C7	SDA0	GPIO_55	H	INPUT(WPU)	H	INPUT(WPU)
R3	RFCTL0	GPIO_65	L	INPUT(WPD)	L	INPUT(WPD)
U4	RFCTL1	GPIO_66	L	INPUT(WPD)	L	INPUT(WPD)
P4	RFPA_EN	GPIO_67	L	INPUT(WPD)	L	INPUT(WPD)
U8	KEYOUT0	GPIO_6	L	OUTPUT	L	OUTPUT
V6	KEYOUT1	GPIO_7	Hiz	Hiz	Hiz	Hiz
U7	KEYOUT2	GPIO_8	L	INPUT(WPD)	L	INPUT(WPD)
W6	KEYOUT3	GPIO_9	L	INPUT(WPD)	L	INPUT(WPD)
U6	KEYOUT4	GPIO_10	L	INPUT(WPD)	L	INPUT(WPD)
U5	KEYIN0	GPIO_11	H	INPUT(WPU)	H	INPUT(WPU)
V3	KEYIN1	GPIO_12	H	INPUT(WPU)	H	INPUT(WPU)
W3	KEYIN2	GPIO_13	L	INPUT(WPD)	L	INPUT(WPD)
V5	KEYIN3	GPIO_14	L	INPUT(WPD)	L	INPUT(WPD)
W5	KEYIN4	GPIO_15	L	INPUT(WPD)	L	INPUT(WPD)
B2	U0TXD	GPIO_32	H	OUTPUT	H	OUTPUT
D2	U0RXD	GPIO_33	H	INPUT(WPU)	H	INPUT(WPU)
E2	U0CTS	GPIO_34	H	INPUT(WPU)	H	INPUT(WPU)
A2	U0RTS	GPIO_35	H	INPUT(WPU)	H	OUTPUT
C11	EXTINT0	GPIO68	L	INPUT(WPD)	L	INPUT(WPD)
A11	EXTINT1	GPIO69	L	INPUT(WPD)	L	INPUT(WPD)
H3	GPIO_0	GPIO_CM4_0	L	INPUT(WPD)	L	INPUT(WPD)
F2	GPIO_1	GPIO_CM4_1	L	INPUT(WPD)	L	INPUT(WPD)
H2	GPIO_2	GPIO_CM4_2	L	INPUT(WPD)	L	INPUT(WPD)
F1	GPIO_3	GPIO_CM4_3	L	INPUT(WPD)	L	INPUT(WPD)
G18	IISDI	GPIO_16	L	INPUT(WPD)	L	INPUT(WPD)
F19	IISDO	GPIO_17	L	INPUT(WPD)	L	INPUT(WPD)
G19	IISCLK	GPIO_18	L	INPUT(WPD)	L	INPUT(WPD)
F18	IISLRCK	GPIO_19	L	INPUT(WPD)	L	INPUT(WPD)
E1	MTCK	GPIO_5	L	INPUT(WPD)	L	INPUT(WPD)
B1	MTMS	GPIO_4	H	INPUT(WPU)	H	INPUT(WPU)
D16	SPI0_CLK	GPIO_21	L	INPUT(WPD)	L	INPUT(WPD)
B16	SPI0_CS	GPIO_22	L	INPUT(WPD)	L	INPUT(WPD)
B15	SPI0_DI	GPIO_23	L	INPUT(WPD)	L	INPUT(WPD)
C15	SPI0_DO	GPIO_24	L	INPUT(WPD)	L	INPUT(WPD)
C18	SD_CLK	GPIO_38	L	OUTPUT	L	OUTPUT
D18	SD_CMD	GPIO_36	H	INPUT(WPU)	H	INPUT(WPU)
F17	SD_D0	GPIO_37	H	INPUT(WPU)	H	INPUT(WPU)
G17	SD_D1	GPIO_56	H	INPUT(WPU)	H	INPUT(WPU)
E17	SD_D2	GPIO_57	H	INPUT(WPU)	H	INPUT(WPU)
C19	SD_D3	GPIO_39	H	INPUT(WPU)	H	INPUT(WPU)
C16	SIMCLK0	GPIO_59	L	OUTPUT	L	OUTPUT
B18	SIMDA0	GPIO_60	H	INPUT(WPU)	H	INPUT(WPU)
A18	SIMRST0	GPIO_58	L	OUTPUT	L	OUTPUT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

B19	SIMCLK1	GPIO_63	L	OUTPUT	L	OUTPUT
C17	SIMDA1	GPIO_61	H	INPUT(WPU)	H	INPUT(WPU)
D17	SIMRST1	GPIO_62	L	OUTPUT	L	OUTPUT
D15	CLK_AUX	GPIO_31	L	OUTPUT	L	OUTPUT
G3	PWM	GPIO_20	H	INPUT(WPU)	H	INPUT(WPU)

3.4.2 SC6531M

Ball No	Ball Name	GPIO No	At Reset		After Reset	
			H/L/Hiz	Pin State	H/L/Hiz	Pin State
B14	ESMCSN	GPIO_70	H	OUTPUT	H	OUTPUT
C14	ESMD0	GPIO_71	Hiz	Hiz	Hiz	Hiz
A14	ESMD1	GPIO_72	Hiz	Hiz	Hiz	Hiz
A15	ESMD2	GPIO_73	H	OUTPUT	H	OUTPUT
B12	ESMD3	GPIO_74	H	OUTPUT	H	OUTPUT
C13	ESMCLK	GPIO_75	L	OUTPUT	L	OUTPUT
C8	FMARK	GPIO_29	L	INPUT(WPD)	L	INPUT(WPD)
D8	LCMRSTN	GPIO_30	L	OUTPUT	L	OUTPUT
B11	SPI1_DI	GPIO_25	L	INPUT(WPD)	L	INPUT(WPD)
A10	SPI1_DO	GPIO_26	L	INPUT(WPD)	L	INPUT(WPD)
C10	SPI1_CLK	GPIO_27	L	INPUT(WPD)	L	INPUT(WPD)
C9	SPI1_CS	GPIO_28	L	INPUT(WPD)	L	INPUT(WPD)
B10	SPI1_CD	GPIO_64	L	INPUT(WPD)	L	INPUT(WPD)
D6	CMPCLK	GPIO_48	L	INPUT(WPD)	L	INPUT(WPD)
A7	CCIRMCK	GPIO_49	L	OUTPUT	L	OUTPUT
C6	CCIRD0	GPIO_40	L	INPUT(WPD)	L	INPUT(WPD)
C4	CCIRD1	GPIO_41	L	INPUT(WPD)	L	INPUT(WPD)
C5	CCIRD2	GPIO_42	L	INPUT(WPD)	L	INPUT(WPD)
B4	CCIRD3	GPIO_43	L	INPUT(WPD)	L	INPUT(WPD)
A3	CCIRD4	GPIO_44	L	INPUT(WPD)	L	INPUT(WPD)
B3	CCIRD5	GPIO_45	L	INPUT(WPD)	L	INPUT(WPD)
E3	CCIRD6	GPIO_46	L	INPUT(WPD)	L	INPUT(WPD)
D3	CCIRD7	GPIO_47	L	INPUT(WPD)	L	INPUT(WPD)
C3	CCIRHS	GPIO_50	Hiz	Hiz	Hiz	Hiz
B7	CCIRVS	GPIO_51	Hiz	Hiz	Hiz	Hiz
A6	CAM_PD	GPIO_52	L	INPUT(WPD)	L	INPUT(WPD)
B6	CAM_RSTN	GPIO_53	L	INPUT(WPD)	L	INPUT(WPD)
B8	SCL0	GPIO_54	H	INPUT(WPU)	H	INPUT(WPU)
C7	SDA0	GPIO_55	H	INPUT(WPU)	H	INPUT(WPU)
R3	RFCTL0	GPIO_65	L	INPUT(WPD)	L	INPUT(WPD)
U4	RFCTL1	GPIO_66	L	INPUT(WPD)	L	INPUT(WPD)
P4	RFPA_EN	GPIO_67	L	INPUT(WPD)	L	INPUT(WPD)
U8	KEYOUT0	GPIO_6	L	OUTPUT	L	OUTPUT
V6	KEYOUT1	GPIO_7	Hiz	Hiz	Hiz	Hiz

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

U7	KEYOUT2	GPIO_8	L	INPUT(WPD)	L	INPUT(WPD)
W6	KEYOUT3	GPIO_9	L	INPUT(WPD)	L	INPUT(WPD)
U6	KEYOUT4	GPIO_10	L	INPUT(WPD)	L	INPUT(WPD)
U5	KEYIN0	GPIO_11	H	INPUT(WPU)	H	INPUT(WPU)
V3	KEYIN1	GPIO_12	H	INPUT(WPU)	H	INPUT(WPU)
W3	KEYIN2	GPIO_13	L	INPUT(WPD)	L	INPUT(WPD)
V5	KEYIN3	GPIO_14	L	INPUT(WPD)	L	INPUT(WPD)
W5	KEYIN4	GPIO_15	L	INPUT(WPD)	L	INPUT(WPD)
B2	U0TXD	GPIO_32	H	OUTPUT	H	OUTPUT
D2	U0RXD	GPIO_33	H	INPUT(WPU)	H	INPUT(WPU)
E2	U0CTS	GPIO_34	H	INPUT(WPU)	H	INPUT(WPU)
A2	U0RTS	GPIO_35	H	INPUT(WPU)	H	OUTPUT
C11	EXTINT0	GPIO68	L	INPUT(WPD)	L	INPUT(WPD)
A11	EXTINT1	GPIO69	L	INPUT(WPD)	L	INPUT(WPD)
H3	GPIO_0	GPIO_CM4_0	L	INPUT(WPD)	L	INPUT(WPD)
F2	GPIO_1	GPIO_CM4_1	L	INPUT(WPD)	L	INPUT(WPD)
H2	GPIO_2	GPIO_CM4_2	L	INPUT(WPD)	L	INPUT(WPD)
F1	GPIO_3	GPIO_CM4_3	L	INPUT(WPD)	L	INPUT(WPD)
G18	IISDI	GPIO_16	L	INPUT(WPD)	L	INPUT(WPD)
F19	IISDO	GPIO_17	L	INPUT(WPD)	L	INPUT(WPD)
G19	IISCLK	GPIO_18	L	INPUT(WPD)	L	INPUT(WPD)
F18	IISLRCK	GPIO_19	L	INPUT(WPD)	L	INPUT(WPD)
E1	MTCK	GPIO_5	L	INPUT(WPD)	L	INPUT(WPD)
B1	MTMS	GPIO_4	H	INPUT(WPU)	H	INPUT(WPU)
D16	SPI0_CLK	GPIO_21	L	INPUT(WPD)	L	INPUT(WPD)
B16	SPI0_CS	GPIO_22	L	INPUT(WPD)	L	INPUT(WPD)
B15	SPI0_DI	GPIO_23	L	INPUT(WPD)	L	INPUT(WPD)
C15	SPI0_DO	GPIO_24	L	INPUT(WPD)	L	INPUT(WPD)
C18	SD_CLK	GPIO_38	L	OUTPUT	L	OUTPUT
D18	SD_CMD	GPIO_36	H	INPUT(WPU)	H	INPUT(WPU)
F17	SD_D0	GPIO_37	H	INPUT(WPU)	H	INPUT(WPU)
G17	SD_D1	GPIO_56	H	INPUT(WPU)	H	INPUT(WPU)
E17	SD_D2	GPIO_57	H	INPUT(WPU)	H	INPUT(WPU)
C19	SD_D3	GPIO_39	H	INPUT(WPU)	H	INPUT(WPU)
C16	SIMCLK0	GPIO_59	L	OUTPUT	L	OUTPUT
B18	SIMDA0	GPIO_60	H	INPUT(WPU)	H	INPUT(WPU)
A18	SIMRST0	GPIO_58	L	OUTPUT	L	OUTPUT
B19	SIMCLK1	GPIO_63	L	OUTPUT	L	OUTPUT
C17	SIMDA1	GPIO_61	H	INPUT(WPU)	H	INPUT(WPU)
D17	SIMRST1	GPIO_62	L	OUTPUT	L	OUTPUT
D15	CLK_AUX	GPIO_31	L	OUTPUT	L	OUTPUT
G3	PWM	GPIO_20	H	INPUT(WPU)	H	INPUT(WPU)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

3.5 Control Registers

3.5.1 Memory map

ARM base address: 0x402A_0000

Address	Name	Reset Value
0x0000	PIN_CTRL_REG0	32'h0
0x0004	PIN_CTRL_REG1	32'h0
0x0008	PIN_CTRL_REG2	32'h0
0x000C	PIN_CTRL_REG3	32'h0
0x0010	PIN_CTRL_REG4	32'h110000
0x0014	PIN_CTRL_REG5	32'h0
0x0018	PIN_CTRL_REG6	32'h0
0x001C	PIN_CTRL_REG7	32'h000F0000
0x0020	RFSDA0	32'h5E070
0x0024	RFSCK0	32'h5E070
0x0028	RFSEN0	32'h5E0B0
0x002C	RFCTL0	32'h5E070
0x0030	RFCTL1	32'h5E070
0x0034	RFCTL2	32'h5E070
0x0038	RFCTL3	32'h5E070
0x003C	RFCTL4	32'h5E070
0x0040	RFCTL5	32'h5E070
0x0044	RFCTL6	32'h5E070
0x0048	RFCTL7	32'h5E070
0x004C	RFCTL8	32'h5E070
0x0050	RFCTL9	32'h5E070
0x0054	RFCTL10	32'h5E070
0x0058	RFCTL11	32'h5E070
0x005C	RFCTL12	32'h5E070
0x0060	RFCTL13	32'h5E070
0x0064	RFCTL14	32'h5E070
0x0068	RFCTL15	32'h5E070
0x006C	PTEST	32'h5E000
0x0070	ANA_INT	32'h5E000
0x0074	EXT_RST_B	32'h5E000
0x0078	CHIP_SLEEP	32'h5E000
0x007C	XTL_BUF_EN0	32'h5E000
0x0080	XTL_BUF_EN1	32'h5E000
0x0084	CLK_32K	32'h5E000

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Address	Name	Reset Value
0x0088	AUD_SCLK	32'h5E000
0x008C	AUD_ADD0	32'h5E000
0x0090	AUD_ADSYNC	32'h5E000
0x0094	AUD_DAD1	32'h5E000
0x0098	AUD_DAD0	32'h5E000
0x009C	AUD_DASYNC	32'h5E000
0x00A0	ADI_D	32'h5E000
0x00A4	ADI_SYNC	32'h5E000
0x00A8	ADI_SCLK	32'h5E000
0x00AC	LCD_RSTN	32'h5E070
0x00B0	LCD_FMARK	32'h5E070
0x00B4	SPI1_CSN	32'h5E0B0
0x00B8	SPI1_DO	32'h5E070
0x00BC	SPI1_DI	32'h5E070
0x00C0	SPI1_CLK	32'h5E070
0x00C4	NFWPN	32'h5E000
0x00C8	NFRBN	32'h5E080
0x00CC	NFCLE	32'h5E000
0x00D0	NFALE	32'h5E000
0x00D4	NFREN	32'h5E000
0x00D8	NFD4	32'h5E040
0x00DC	NFD5	32'h5E040
0x00E0	NFD6	32'h5E040
0x00E4	NFD7	32'h5E040
0x00E8	NFD10	32'h5E040
0x00EC	NFD11	32'h5E040
0x00F0	NFD14	32'h5E040
0x00F4	NFCEN0	32'h5E000
0x00F8	NFCEN1	32'h5E000
0x00FC	NFWEN	32'h5E000
0x0100	NFD0	32'h5E000
0x0104	NFD1	32'h5E000
0x0108	NFD2	32'h5E000
0x010C	NFD3	32'h5E000
0x0110	NFD8	32'h5E040
0x0114	NFD9	32'h5E040
0x0118	NFD12	32'h5E040

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Address	Name	Reset Value
0x011C	NFD13	32'h5E040
0x0120	NFD15	32'h5E040
0x0124	CCIRMCLK	32'h5E010
0x0128	CCIRRST	32'h5E070
0x012C	CCIRPD1	32'h5E070
0x0130	CCIRPD0	32'h5E070
0x0134	SCL0	32'h5E0B0
0x0138	SDA0	32'h5E0B0
0x013C	KEYOUT0	32'h5E000
0x0140	KEYOUT1	32'h5E040
0x0144	KEYOUT2	32'h5E070
0x0148	KEYIN0	32'h5E080
0x014C	KEYIN1	32'h5E080
0x0150	KEYIN2	32'h5E070
0x0154	CLK_AUX0	32'h5E070
0x0158	CLK_AUX1	32'h5E070
0x015C	IIS0DI	32'h5E070
0x0160	IIS0DO	32'h5E070
0x0164	IIS0CLK	32'h5E070
0x0168	IIS0LRCK	32'h5E070
0x016C	MTDO	32'h5E000
0x0170	MTDI	32'h5E080
0x0174	MTCK	32'h5E040
0x0178	MTMS	32'h5E080
0x017C	MTRST_N	32'h5E080
0x0180	TRACECLK	32'h5E070
0x0184	TRACECTRL	32'h5E070
0x0188	TRACEDAT0	32'h5E070
0x018C	TRACEDAT1	32'h5E070
0x0190	TRACEDAT2	32'h5E070
0x0194	TRACEDAT3	32'h5E070
0x0198	TRACEDAT4	32'h5E070
0x019C	TRACEDAT5	32'h5E070
0x01A0	TRACEDAT6	32'h5E070
0x01A4	TRACEDAT7	32'h5E070
0x01A8	U0TXD	32'h5E000
0x01AC	U0RXD	32'h5E080

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Address	Name	Reset Value
0x01B0	U0CTS	32'h5E070
0x01B4	U0RTS	32'h5E070
0x01B8	U1TXD	32'h5E000
0x01BC	U1RXD	32'h5E080
0x01C0	U2TXD	32'h5E070
0x01C4	U2RXD	32'h5E070
0x01C8	U2CTS	32'h5E070
0x01CC	U2RTS	32'h5E070
0x01D0	SCL2	32'h5E0B0
0x01D4	SDA2	32'h5E0B0
0x01D8	EXTINT0	32'h5E070
0x01DC	EXTINT1	32'h5E070
0x01E0	SCL1	32'h5E0B0
0x01E4	SDA1	32'h5E0B0
0x01E8	SIMCLK0	32'h5E070
0x01EC	SIMDA0	32'h5E070
0x01F0	SIMRST0	32'h5E070
0x01F4	SIMCLK1	32'h5E070
0x01F8	SIMDA1	32'h5E070
0x01FC	SIMRST1	32'h5E070
0x0200	SIMCLK2	32'h5E070
0x0204	SIMDA2	32'h5E070
0x0208	SIMRST2	32'h5E070
0x020C	SD1_CLK	32'h5E070
0x0210	SD1_CMD	32'h5E070
0x0214	SD1_D0	32'h5E070
0x0218	SD1_D1	32'h5E070
0x021C	SD1_D2	32'h5E070
0x0220	SD1_D3	32'h5E070
0x0224	SD0_D3	32'h5E070
0x0228	SD0_D2	32'h5E070
0x022C	SD0_CMD	32'h5E070
0x0230	SD0_D0	32'h5E070
0x0234	SD0_D1	32'h5E070
0x0238	SD0_CLK0	32'h5E070
0x023C	RF_ADC_ON	32'h5E070
0x0240	RF_DAC_ON	32'h5E070

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Address	Name	Reset Value
0x0338	CP2_RFCTL0	32'h5E070
0x033C	CP2_RFCTL1	32'h5E070
0x0340	CP2_RFCTL2	32'h5E070

3.5.2 Register Description

3.5.2.1 Pin_CTRL_REG0

Description: Pin global control register0

Field Name	Bit	Type	Reset Value	Description
AP_iis0_internal_loop_sel	[31]	R/W	1'h0	1'b0: Default path. AP iis0 inputs come from pad input. 1'b1: Alternative path. AP iis0 inputs come from CP2 iis output.
CP0_iis0_internal_loop_sel	[30]	R/W	1'h0	1'b0: Default path. CP0 iis0 inputs come from pad input. 1'b1: Alternative path. CP0 iis0 inputs come from CP2 iis output.
CP2_iis_internal_loop_sel	[29:28]	R/W	2'h0	2'b00: Default path. CP2 iis inputs come from pad input. 2'b01: Alternative path1. CP2 iis inputs come from CP0 iis0 output. 2'b1x: Alternative path2. CP2 iis inputs come from AP iis0 output.
	[27:22]	RO	6'h0	Reserved
wrap_dbg_subsys_sel	[21:20]	R/W	2'h0	Debug bus wrap select: 2'b00: WRAP_DBG_BUS= {byte3,byte2,byte1,byte1} 2'b01: WRAP_DBG_BUS= {byte2,byte1,byte0,byte3} 2'b10: WRAP_DBG_BUS= {byte1,byte0,byte3,byte2} 2'b11: WRAP_DBG_BUS= {byte0,byte3,byte2,byte1}
dbg_subsys_sel	[19:16]	R/W	4'h0	Debug bus sub-system select: 4'b0001: from aon_top 4'b0010: from ap_top 4'b0011: from gpu_top 4'b0100: from pub_top 4'b0101: from con_top 4'b0110: from mm_top 4'b0111: from w_cp_top Others: reserved
	[15]	RO	1'h0	Reserved
VIO18_NF_wpdi	[14]	R/W	1'h0	Input VIO18_NF/VDDCORE interface pull-down enable. Active=1. WhenVIO18_NF power down

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
				and VDDCORE power on, set WPDI=1 to prevent leakage current.
VIO18_ADI_wpdi	[13]	R/W	1'h0	Input VIO18_ADI/VDDCORE interface pull-down enable. Active=1. WhenVIO18_ADI power down and VDDCORE power on, set WPDI=1 to prevent leakage current.
VIO18_2_wpdi	[12]	R/W	1'h0	Input VIO18_2/VDDCORE interface pull-down enable. Active=1. WhenVIO18_2 power down and VDDCORE power on, set WPDI=1 to prevent leakage current.
VIO18_1_wpdi	[11]	R/W	1'h0	Input VIO18_1/VDDCORE interface pull-down enable. Active=1. WhenVIO18_1 power down and VDDCORE power on, set WPDI=1 to prevent leakage current.
VDDIO_VMEM_wpdi	[10]	R/W	1'h0	Input VDDIO_VMEM/VDDCORE interface pull-down enable. Active=1. WhenVDDIO_VMEM power down and VDDCORE power on, set WPDI=1 to prevent leakage current.
	[9:6]	RO	4'h0	Reserved
VIO18_3_wpdi	[5]	R/W	1'h0	Input VIO18_3/VDDCORE interface pull-down enable. Active=1. WhenVIO18_3 power down and VDDCORE power on, set WPDI=1 to prevent leakage current.
VIO18_NF1_wpdi	[4]	R/W	1'h0	Input VIO18_NF1/VDDCORE interface pull-down enable. Active=1. WhenVIO18_NF1 power down and VDDCORE power on, set WPDI=1 to prevent leakage current.
	[3:1]	RO	3'h0	Reserved
USB_PORN	[0]	R/W	1'h0	USB power on reset, active low

Pin_CTRL_REG0 [31]	AP iis0 input internal loop sel
[31]	
0	PAD IO → AP IIS0
1	CP2 IIS → AP IIS0

*IIS IO need to be configured as IIS function first

Pin_CTRL_REG0 [30]	CP0 iis0 input internal loop sel
[30]	
0	PAD IO → CP0 IIS0
1	CP2 IIS → CP0 IIS0

*IIS IO need to be configured as IIS function first

Pin_CTRL_REG0 [29:28]		CP2 iis input internal loop sel
[29]	[28]	
0	0	PAD IO → CP2 IIS
0	1	CP0 IIS0 → CP2 IIS

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

1	X	AP IIS0 → CP2 IIS

*IIS IO need to be configured as IIS function first

3.5.2.2 Pin_CTRL_REG1

Description: Pin global control register1

Field Name	Bit	Type	Reset Value	Description
	[31:15]	RO	17'h0	Reserved
iis1lrck_pin_in_sel	[14]	R/W	1'h0	IIS1LRCK source select: 1'b0: from function2 TRACEDATA7 pad 1'b1: from function2 AUD_DASYNC pad
iis1di_pin_in_sel	[13]	R/W	1'h0	IIS1DI source select: 1'b0: from function2 TRACEDA4 pad 1'b1: from function2 AUD_ADD0 pad
iis1clk_pin_in_sel	[12]	R/W	1'h0	IIS1CLK source select: 1'b0: from function2 TRACEDA6 pad 1'b1: from function2 AUD_SCLK pad
	[11:9]	RO	3'h0	Reserved
cp_dtms_pin_in_sel	[8]	R/W	1'h0	CP_DTMS source select: 1'b0: from function3 CCIRRST pad 1'b1: from function2 MTMS pad
cp_dtdi_pin_in_sel	[7]	R/W	1'h0	CP_DTDI source select: 1'b0: from function3 CCIRPD0 pad 1'b1: from function2 MTDI pad
cp_dtck_pin_in_sel	[6]	R/W	1'h0	CP_DTCK source select: 1'b0: from function3 CCIRMCLK pad 1'b1: from function2 MTCK pad
	[5:0]	RO	6'h0	Reserved

3.5.2.3 Pin_CTRL_REG2

Description: Pin global control register2

Field Name	Bit	Type	Reset Value	Description
usb_uart1_sel	[31]	R/W	1'h0	0: Normal UART interface1 function 1: USB DP/DM as UART RXD/TXD as UART interface1
usb_uart_oe	[30:29]	R/W	2'h0	This signal controls the DM data direction at UART function, this signal is valid only when USB20_BYPASS_FS set to 1'b1 0:receiver 1:transmitter
	[28:23]	RO	6'h0	Reserved
sim2_sys_sel	[22]	R/W	1'h0	SIM interface2 (SIMDA2…) select:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
				1'b0: CP0 SIM2 controller 1'b1: AP SIM0 controller
sim1_sys_sel	[21]	R/W	1'h0	SIM interface1 (SIMDA1…) select: 1'b0: CP0 SIM1 controller 1'b1: AP SIM0 controller
sim0_sys_sel	[20]	R/W	1'h0	SIM interface0 (SIMDA0…) select: 1'b0: CP0 SIM0 controller 1'b1: AP SIM0 controller
	[19:13]	RO	7'h0	Reserved
uart2_sys_sel	[12:10]	R/W	3'h0	UART interface2 (U2TXD…) select: 3'b000: AP0 UART2 controller 3'b001: CP0 UART1 controller 3'b010: CP2 UART0 controller 3'b011: CP2 UART1 controller Others: reserved
uart1_sys_sel	[9:7]	R/W	3'h0	UART interface1 (U1TXD…) select: 3'b000: AP0 UART1 controller 3'b001: CP0 UART1 controller 3'b010: CP2 UART0 controller 3'b011: CP2 UART1 controller Others: reserved
uart0_sys_sel	[6:4]	R/W	3'h0	UART interface0 (U0TXD…) select: 3'b000: AP0 UART0 controller 3'b001: CP0 UART0 controller 3'b010: CP2 UART0 controller 3'b011: CP2 UART1 controller Others: reserved
	[3:0]	RO	4'h0	Reserved

Pin_CTRL_REG2 [22:20]				SIM Device matrix mux function
[22]	[21]	[20]		
X	X	1		AP_SIM->SIM0 IO
X	1	0		AP_SIM->SIM1 IO
1	0	0		AP_SIM->SIM2 IO
X	X	0		CP_SIM0 -> SIM0 IO
X	0	X		CP_SIM1 -> SIM1 IO
0	X	X		CP_SIM2 -> SIM2 IO

*SIM0/SIM1/SIM2 IO need to be configured as SIM function first

Pin_CTRL_REG2 [12:4]		UART Device matrix mux function

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

[12:10]	[9:7]	[6:4]		
X	X	0		AP_UART0 -> UART0 IO
X	0	X		AP_UART1 -> UART1 IO
0	X	X		AP_UART2 -> UART2 IO
X	X	1		CP0_UART0 -> UART0 IO
X	1	X		CP0_UART1 -> UART1 IO
1	Not 1	X		CP0_UART1 -> UART2 IO
X	X	2		CP2_UART0 -> UART0 IO
X	2	Not 2		CP2_UART0 -> UART1 IO
2	Not 2	Not 2		CP2_UART0 -> UART2 IO
X	X	3		CP2_UART1 -> UART0 IO
X	3	Not 3		CP2_UART1 -> UART1 IO
3	Not 3	Not 3		CP2_UART1 -> UART2 IO

*UART0/UART1/UART2 IO need to be configured as UART function first

3.5.2.4 Pin_CTRL_REG3

Description: Pin global control register3

Field Name	Bit	Type	Reset Value	Description
wdrst_out_sel	[31]	R/W	1'h0	Watch dog reset source select: 1'b0: from CA7 watch dog 1'b1: from AP watch dog
	[30:19]	RO	12'h0	Reserved
gpio_inf0_sys_sel	[18]	R/W	1'h0	CP_ARM_GPIO select: 1'b0: CP0 GPIO controller 1'b1: CP2 GPIO controller
	[17:10]	RO	8'h0	Reserved
iis1_sys_sel	[9:8]	R/W	2'h0	IIS interface1 (IIS1DI…) select: 2'b00: AP IIS1 controller 2'b01: CP0 IIS1 controller 2'b10: CP2 IIS0 controller 2'b11: VBC IIS0 controller
iis0_sys_sel	[7:6]	R/W	2'h0	IIS interface0 (IIS0DI…) select: 2'b00: AP IIS0 controller 2'b01: CP0 IIS0 controller 2'b10: CP2 IIS0 controller 2'b11: VBC IIS0 controller
	[5:1]	RO	5'h0	Reserved
iis01_loop_sel	[0]	R/W	1'h0	IIS interface0 and interface1 loop select

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

3.5.2.5 Pin_CTRL_REG4

Description: Pin global control register4

Field Name	Bit	Type	Reset Value	Description
	[31:29]	RO	3'h0	Reserved
VIO28_pp1	[28]	R/W	1'h0	VIO28 domain driving boost 0: no boost 1: boost
VIO_SIM2_pp1	[27]	R/W	1'h0	VIO_SIM2 domain driving boost 0: no boost 1: boost
VIO_SIM1_pp1	[26]	R/W	1'h0	VIO_SIM1 domain driving boost 0: no boost 1: boost
VIO_SIM0_pp1	[25]	R/W	1'h0	VIO_SIM0 domain driving boost 0: no boost 1: boost
VIO_SD0_pp1	[24]	R/W	1'h0	VIO_SD0 domain driving boost 0: no boost 1: boost
	[23:21]	RO	3'h0	Reserved
VIO28_ms	[20]	R/W	1'h1	VIO28 domain pad driving level: 0: 1.8V 1: 3.3V
VIO_SIM2_ms	[19]	R/W	1'h0	VIO_SIM2 domain pad driving level: 0: 1.8V 1: 3.3V
VIO_SIM1_ms	[18]	R/W	1'h0	VIO_SIM1 domain pad driving level: 0: 1.8V 1: 3.3V
VIO_SIM0_ms	[17]	R/W	1'h0	VIO_SIM0 domain pad driving level: 0: 1.8V 1: 3.3V
VIO_SD0_ms	[16]	R/W	1'h1	VIO_SD0 domain pad driving level: 0: 1.8V 1: 3.3V
	[15:8]	RO	8'h0	Reserved
test_dbg_mode7	[7]	R/W	1'h0	1’b0: debug mode7 disable 1’b1: debug mode7 enable
test_dbg_mode6	[6]	R/W	1'h0	1’b0: debug mode6 disable 1’b1: debug mode6 enable
test_dbg_mode5	[5]	R/W	1'h0	1’b0: debug mode5 disable 1’b1: debug mode5 enable

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
test_dbg_mode4	[4]	R/W	1'h0	1’b0: debug mode4 disable 1’b1: debug mode4 enable
test_dbg_mode3	[3]	R/W	1'h0	1’b0: debug mode3 disable 1’b1: debug mode3 enable
test_dbg_mode2	[2]	R/W	1'h0	1’b0: debug mode2 disable 1’b1: debug mode2 enable
test_dbg_mode1	[1]	R/W	1'h0	1’b0: debug mode1 disable 1’b1: debug mode1 enable
test_dbg_mode0	[0]	R/W	1'h0	Debug mode selection: 1’b0: debug mode0 disable 1’b1: debug mode0 enable

3.5.2.6 Pin_CTRL_REG5

Description: Pin global control register5

Field Name	Bit	Type	Reset Value	Description
iomux_dmd_sel_wrap[31:0]	[31:0]	R/W	32'h0	DDR EMD source select: 0: from DMC 1: from IOMUX

3.5.2.7 Pin_CTRL_REG6

Description: Pin global control register6

Field Name	Bit	Type	Reset Value	Description
	[31]	RO	1'h0	Reserved
iomux_dmodt_sel_wrap[1:0]	[30:29]	R/W	2'h0	DDR EMODT source select: 0: from DMC 1: from IOMUX
iomux_dmrstn_sel_wrap	[28]	R/W	1'h0	DDR EMRSTN source select: 0: from DMC 1: from IOMUX
iomux_dmrasn_sel_wrap	[27]	R/W	1'h0	DDR EMRASN source select: 0: from DMC 1: from IOMUX
iomux_dmcasn_sel_wrap	[26]	R/W	1'h0	DDR EMCASN source select: 0: from DMC 1: from IOMUX
iomux_dmwen_sel_wrap	[25]	R/W	1'h0	DDR EMWEN source select: 0: from DMC

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
				1: from IOMUX
iomux_dmclkdm_sel_wrap	[24]	R/W	1'h0	DDR EMCLKDM source select: 0: from DMC 1: from IOMUX
iomux_dmclkdp_sel_wrap	[23]	R/W	1'h0	DDR EMCLKDP source select: 0: from DMC 1: from IOMUX
iomux_dmcke_sel_wrap[1:0]	[22:21]	R/W	2'h0	DDR EMCKE source select: 0: from DMC 1: from IOMUX
iomux_dmcsn_sel_wrap[1:0]	[20:19]	R/W	2'h0	DDR EMCSN source select: 0: from DMC 1: from IOMUX
iomux_dmba_sel_wrap[2:0]	[18:16]	R/W	3'h0	DDR EMBA source select: 0: from DMC 1: from IOMUX
iomux_dma_sel_wrap[15:0]	[15:0]	R/W	16'h0	DDR EMA source select: 0: from DMC 1: from IOMUX

3.5.2.8 Pin_CTRL_REG7

Description: Pin global control register7

Field Name	Bit	Type	Reset Value	Description
	[31:21]	RO	11'h0	Reserved
VIO28_pwd	[20]	R/W	1'h0	This register is cooperate with VIO28_ms. VIO28 power down, active high The setting should be as below VIO28:VIO28_ms:VIO_28_pwd 3.3V:1:0 1.8V:0:0 0V:0:1
VIO_SIM2_pwd	[19]	R/W	1'h1	This register is cooperate with VIO_SIM2_ms. VIO_SIM2 power down, active high The setting should be as below VIO_SIM2:VIO_SIM2_ms:VIO_SIM2_pwd 3.3V:1:0 1.8V:0:0 0V:0:1

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
VIO_SIM1_pwd	[18]	R/W	1'h1	This register is cooperate with VIO_SIM1_ms. VIO_SIM1 power down, active high The setting should be as below VIO_SIM1:VIO_SIM1_ms:VIO_SIM1_pwd 3.3V:1:0 1.8V:0:0 0V:0:1
VIO_SIM0_pwd	[17]	R/W	1'h1	This register is cooperate with VIO_SIM0_ms. VIO_SIM0 power down, active high The setting should be as below VIO_SIM0:VIO_SIM0_ms:VIO_SIM0_pwd 3.3V:1:0 1.8V:0:0 0V:0:1
VIO_SD0_pwd	[16]	R/W	1'h1	This register is cooperate with VIO_SD0_ms. VIO_SD0 power down, active high The setting should be as below VIO_SD0:VIO_SD0_ms:VIO_SD0_pwd 3.3V:1:0 1.8V:0:0 0V:0:1
	[15:12]	RO	4'h0	Reserved
iomux_dmdqsn_sel_wrap[3:0]	[11:8]	R/W	4'h0	DDR EMDQSN source select: 0: from DMC 1: from IOMUX
iomux_dmdqs_sel_wrap[3:0]	[7:4]	R/W	4'h0	DDR EMDQS source select: 0: from DMC 1: from IOMUX
iomux_dmdqm_sel_wrap[3:0]	[3:0]	R/W	4'h0	DDR EMDQM source select: 0: from DMC 1: from IOMUX

3.5.2.9 Other Pin Control Register

Description: Other Pin control register share the same bit format shown as below:

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	Reserved*										PIN_NAME_bsr_drv			Reserved	PIN_NAME_dslp_en
Type	RW										RW			RO	RW
Reset	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIN_NAME_dslp_en			PIN_NAME_bsr_wpus	PIN_NAME_bsr_se	Reserved			PIN_NAME_fun_wpu	PIN_NAME_fun_wpdo	PIN_NAME_fun_sel		PIN_NAME_slp_wpu	PIN_NAME_slp_wpdo	PIN_NAME_slp_ie	PIN_NAME_slp_oe
Type	RW			RW	RW	RO			RW	RW	RW		RW	RW	RW	RW
Reset	1	1	1	0	0	0	0	0					0	0	0	0

Note:

- "PIN_NAME" represents each pin. Function 1, 2, 3, 4 of each pin is detailed in Pin Multiplexed Function List, the default value of each control bit is detailed in Memory Map.
- Please don't modify the value in reserved filed. It maybe debug setting for some IOs.

Field Name	Bit	Type	Reset Value	Description
	[31:30]	RO	2'h0	Reserved
PIN_NAME_bsr_drv*1	[20:18]	R/W	3'h1	Drive Strength select
	[17]	RO	1'h0	Reserved
PIN_NAME_dslp_en	[16:13]	R/W	4'hf	Sleep mode enable: BIT0: Sleep with AP sleep BIT1: Sleep with CP0 sleep BIT2: Sleep with CP1 sleep, no function BIT3: Sleep with CP2 sleep
PIN_NAME_bsr_wpus	[12]	R/W	1'h0	Pull up resistor select
PIN_NAME_bsr_se	[11]	R/W	1'h0	Schmitt trigger input enable
	[10:8]	RO	3'h0	Reserved
PIN_NAME_fun_wpu	[7]	R/W		Weak pull up for function mode
PIN_NAME_fun_wpdo	[6]	R/W		Weak pull down for function mode
PIN_NAME_fun_sel	[5:4]	R/W		Function select: 2'b00: Function1 2'b00: Function2 2'b00: Function3 2'b00: Function4
PIN_NAME_slp_wpu	[3]	R/W	1'h0	Weak pull up control in chip deep sleep mode

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

PIN_NAME_slp_wpdo	[2]	R/W	1'h0	Weak pull down control in chip deep sleep mode
PIN_NAME_slp_ie	[1]	R/W	1'h0	Input enable control in chip deep sleep mode
PIN_NAME_slp_oe	[0]	R/W	1'h0	Output enable control in chip deep sleep mode

*1. PIN_NAME_bsr_drv[20] only exist for cell name is SPSEBC2_24X_VL or SPZTRKDSD3LC30X1V

Spreadtrum Confidential
Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

3.5.3 Strapping Pins

Cell Name	Substrate Name	Power	Strapping Pin
SPSEBC2_24X_VL	NFD[0]	VIO18_NF	arm_boot_md0
SPSEBC2_24X_VL	NFD[1]	VIO18_NF	arm_boot_md1
SPSEBC2_24X_VL	NFD[2]	VIO18_NF	arm_boot_md2
SPSEBC2_24X_VL	NFD[3]	VIO18_NF	arm_boot_md3
SPSEBC2_X_VL	U1TXD	VIO18_1	USB download enable

3.5.4 PAD information

3.5.4.1 Digital Pad Type Description

Cell Name	Description
SPSCBC2_8X_HL	Bi-direction Pad with Enable Controlled Pull-Down & Pull-up Resistor., Programmable Driver Strength. No tolerance function. The Schmitt trigger input function can be controlled by the SE signal .SE=1, Schmitt input enable .SE=0 Schmitt input disable. (Horizontal)
SPSCBC2_8X_VL	Bi-direction Pad with Enable Controlled Pull-Down & Pull-up Resistor., Programmable Driver Strength. No tolerance function. The Schmitt trigger input function can be controlled by the SE signal .SE=1, Schmitt input enable .SE=0 Schmitt input disable. (Vertical)
SPSCBC2_8X_W_VL	Base on the SPSCBC2_8X_VL/HL, enlarge the ESD area for SIMcard/Keypad and etc. 8KV ESD performance. (Vertical)
SPSCBC2_8X_IIC_VL	Base on the SPSCBC2_8X_VL/HL, change the soft pull up resistor from 4.7K to 1.8K. (Vertical)
SPSEBC2_24X_VL	Bi-direction Pad with Enable Controlled Pull-Down &Pull-Up Resistor., Programmable Driver Strength. No tolerance function. The Schmitt trigger input function can be controlled by the SE signal .SE=1, Schmitt input enable .SE=0 Schmitt input disable. Using for EMMC/SD interface (VDDIO=1.8V). (Vertical)
SPZTRKDSD3LC30X1V	Programmable 3.0V SD 3.0 bidirectional buffer (Vertical)
SPZTRKD28LC30X1H	Programmable 3.0V bidirectional buffer, staggered, horizontal
SPDDRIO	DDRIO: Data/Address/Command Bi-direction IO. P/G decap:6.15pf
SPDDRIODIF2	DDRIO: CLK/DQS differential input/output P/G decap:2*6.15pf
SPPZQ	DDRIO: Output impedance caliber. IO. P/G decap:2*6.15pf
SPVREF	DDRIO: 1/2*VDDIO reference voltage input IO. P/G decap:6.15pf

3.5.4.2 Digital Power / Ground cell

SPVDD1_HL	VDDCORE 0.9V power pad. (Horizontal)
SPVDD1_VL	VDDCORE 0.9V power pad. (Vertical)
SPVDD1_S3	VDDCORE 1.05V power pad. P/G decap:8pf
SPVSS1_HL	Core ground pad. (Horizontal)
SPVSS1_VL	Core ground pad. (Vertical)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SPVSS1_S3	Core ground pad. P/G decap:10pf
SPVDD2_HL	VDDIO 1.8V power pad. (Horizontal)
SPVDD2_VL	VDDIO 1.8V power pad. (Vertical)
SPVDD2_S3	VDDIO 1.2V power pad, P/G decap:10pf
SPVSS2_HL	VSSIO 1.8V ground pad. (Horizontal)
SPVSS2_VL	VSSIO 1.8V ground pad. (Vertical)
SPVDD2POC_S3	VDDIO 1.2V power on control pad. A power domain must & only have one SPVDD2POC cell. P/G decap:13pf
SPVDD2CAP_S3	VDDIO 1.2V power pad. P/G decap:14pf
SPVSS2_S3	VSSIO 1.2V ground pad. P/G decap:12pf
SPVSS2CAP_S3	VSSIO 1.2V ground pad. P/G decap:12pf
SPVDD1ANA_HL	The 0.9V power supply pad, which supply the 0.9V core voltage to Core Circuit. (Horizontal)
SPVDD2ANA_VL	The 1.8V power supply pad. Only supply the 1.8V to the internal circuit for example Efuse. Need cut the VDDIO power rail using the CUT cell. (Vertical)
SPVDD2POC_HL	VDDIO 1.8V power on control pad. A power domain must & only have one SPVDDPOC cell. (Horizontal)
SPVDD2POC_VL	VDDIO 1.8V power on control pad. A power domain must & only have one SPVDDPOC cell. (Vertical)
VCCKLCH	Power supply for the internal core cells and I/O-to-core interface, staggered, horizontal
VCCKLCV	Power supply for the internal core cells and I/O-to-core interface, staggered, vertical
GNDKLCH	Ground supply for the internal core cell and I/O-to-core interface, staggered, horizontal
GNDKLCV	Ground supply for the internal core cell and I/O-to-core interface, staggered, vertical
GNDIOLCH	Ground supply for the 3.0V input buffer and output buffer, staggered, horizontal
GNDIOLCV	Ground supply for the 3.0V input buffer and output buffer, staggered, vertical

3.5.4.3 Power Switch I/O cells

VCCH30L18PWLCH	Power switch for VCC3OUT (3.0V) and power supply for VCC18U,staggered, horizontal
VCCH30L18PWLCV	Power switch for VCC3OUT (3.0V) and power supply for VCC18U,staggered, vertical
VCC18DPWLCH	Power switch for the VCC18DO input buffer and out buffer, staggered, horizontal
VCC18DPWLCV	Power switch for the VCC18DO input buffer and out buffer, staggered, vertical

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

3.5.4.4 SPSCBC2_8X_HL/VL

Truth Table: Input function: C=PAD&IE, Output function: PAD=A&OE

	A	PAD	C	IE	OE	WPU	WPUS	WPDO	WPDI
Input	X	0	0	1	0	0	X	0	0
	X	1	1	1	0	0	X	0	0
Output	0	0	0	0	1	0	X	0	0
	1	1	0	0	1	0	X	0	0
Inout	0	0	0	1	1	0	X	0	0
	1	1	1	1	1	0	X	0	0
Tri State	X	HZ	0	0	0	0	X	0	0
	X	HZ	0	0	0	0	X	0	0
Pull Up	X	1	0	0	0	1	0: 20K(1.8V) 1:4.7K(1.8V)	0	0
Pull Down	X	0	0	0	0	0	X	1	0
IO Power-down	X	X	1	X	X	X	X	X	1

Driver Strength Select Function:

DRV[1]	DRV[0]	
0	0	2mA
0	1	4mA
1	0	6mA
1	1	8mA

DC Parameter:

	Description	SS	TT	FF
V_T+	Schmitt trig. Low to High threshold point (1.8V)	X	1.20V	X
V_T-	Schmitt trig. High to Low threshold point (1.8V)	X	0.64V	X
RPU	Pull-up resistor (1.8V)	30K/6K	**22K/4.6K**	16K/3.5K
RPD	Pull-down resistor (1.8V)	30K	**40K**	60K
Iavg	Active Current@100MHz, FF Corner, 30pf loading	X	X	4mA
Ist	Standby Current	X	<0.1uA	X
IoZ	Tri-state output leakage current @Vo=3V or 0V	X	<0.1uA	X

AC parameter:

Delay path		Rise Time(ns)	Fall Time(ns)	Rise Delay(ns)	Fall Delay(ns)
PAD→C		0.193	0.198	0.437	0.327
A→PAD	2mA	4.911	4.766	3.379	3.540
	4mA	2.569	2.491	2.452	2.510
	6mA	1.778	1.778	2.168	2.193

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	8mA	2.548	2.548	2.491	2.521

3.5.4.5 SPSEBC2_24X_HL/VL

Truth Table: Input function: C=PAD&IE, Output function: PAD=A&OE

	A	PAD	C	IE	OE	WPU	WPUS	WPDO	WPDI
Input	X	0	0	1	0	0	X	0	0
	X	1	1	1	0	0	X	0	0
Output	0	0	0	0	1	0	X	0	0
	1	1	0	0	1	0	X	0	0
Inout	0	0	0	1	1	0	X	0	0
	1	1	1	1	1	0	X	0	0
Tri State	X	HZ	0	0	0	0	X	0	0
	X	HZ	0	0	0	0	X	0	0
Pull Up	X	1	0	0	0	1	0: 20K(1.8V) 1:4.7K(1.8V)	0	0
Pull Down	X	0	0	0	0	0	X	1	0
IO Power-down	X	X	1	X	X	X	X	X	1

When The VDDIO=1.8V: **SS@125C**

DRV[2]	DRV[1]	DRV[0]	Nominal Impedance	Note
1	0	0	**100ohm**	Option
1	0	1	**66ohm**	Option
1	1	0	**50ohm**	Same the 000
1	1	1	**33ohm**	Same the 001
0	0	0	**50ohm**	Mandatory
0	0	1	**33ohm**	Option
0	1	0	**20ohm**	Option
0	1	1	**10ohm**	Option

DC Parameter:

	Description	SS	TT	FF
V_T+	Schmitt trig. Low to High threshold point (1.8V)	X	1.20V	X
V_T-	Schmitt trig. High to Low threshold point (1.8V)	X	0.64V	X
RPU	Pull-up resistor (1.8V)	30K/6K	**22K/4.6K**	16K/3.5K
RPD	Pull-down resistor (1.8V)	30K	**40K**	60K
Iavg	Active Current@208MHz, FF Corner, 15pf loading	X	X	13mA
Ist	Standby Current	X	<0.1uA	X
IoZ	Tri-state output leakage current @Vo=1.8V or 0V	X	<0.1uA	X

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

AC Parameter:

When VDDIO=1.8V

The data simulation is SS corner, ***clk=208MHz***, Cloading=0.2pf, **post simulation data**.

VDDUI=1.8V, Temp=125C, Rise time and falling time are based in (**10%~90%**)VDD/VDDIO

Delay Path		Cpad	Rise Time(ns)	Fall Time(ns)	Rise Delay(ns)	Fall Delay(ns)
PAD→C			**0.15**	**0.19**	**0.61**	**0.40**
A→PAD	**100ohm**	**3pf**	**1.34**	**1.51**	**1.42**	**1.59**
	66ohm	**5pf**	**1.29**	**1.46**	**1.42**	**1.59**
	50ohm	**8pf**	**1.41**	**1.60**	**1.46**	**1.65**
	33ohm	**10pf**	**1.15**	**1.31**	**1.55**	**1.55**
	20ohm	**15pf**	**1.11**	**1.26**	**1.54**	**1.54**
	10hom	**15pf**	**0.74**	**0.83**	**1.34**	**1.34**

Spreadtrum Confidential
Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

DDR driving strength/calibration flow:

3.5.5 AON_TOP_AON_APB_RF Register Address Map

Base address: 0x402E0000, 0x00001000, 0x00002000

Offset Addr	Name	Description
0x0060	DDR_ZQ_CONTROL	DDR_ZQ_CONTROL

3.5.5.1 DDR_ZQ_CONTROL

0x00000060			DDR_ZQ_CONTROL (0x00010000)									DDR_ZQ_CONTROL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved														DDR_ZQ_CALOVER	DDR_ZQ_PD
Type	RO														RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DDR_ZQ_CAL	DDR_ZQ_ZPROG					DDR_ZQ_DRVP					DDR_ZQ_DRVN				
Type	RW	RW					RW					RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

3.5.5.2 DDR_ZQ_CONTROL

Field Name	Bit	Type	Reset Value	Description
reserved	[31:18]	RO	0x0	Reserved
DDR_ZQ_CALOVER	[17]	RO	0x0	DDR_ZQ_CALOVER Calibration complete output signal
DDR_ZQ_PD	[16]	RW	0x1	Power down 0: Enter calibration mode 1: Power down
DDR_ZQ_CAL	[15]	RW	0x0	DDR_ZQ_CAL 0: Calibrate NMOS 1: Calibrate PMOS
DDR_ZQ_ZPROG	[14:10]	RW	0x0	DDR_ZQ_ZPROG Target voltage programming input
DDR_ZQ_DRVP	[9: 5]	RW	0x0	DDR_ZQ_DRVP PMOS driver programming input
DDR_ZQ_DRVN	[4: 0]	RW	0x0	DDR_ZQ_DRVN

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				NMOS driver programming input

Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

4 Electrical Specification

4.1 DC specification

4.1.1 Absolute maximum ratings

The functionality is subject to the absolute maximum/minimum values listed in Table 4-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 4-1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
VCHG	Charger input voltage from adaptor or USB	-0.3	28	V
VBAT	Supply voltage from a battery	-0.3	6.0	V
V_{DI}	Input voltage on any digital input	-0.3	3.6	V
V_{AI}	Input voltage on any analog input	-0.3	3.6	V
I_{AI2}	DC drive current for EARP, EARN, AUXSPP and AUXSPN		60	mA
$V_{max, ESD}$	Maximum ESD stress voltage, Human Body Model, any pin to any supply pin, either polarity or any pin to all non-supply pins together, either polarity. Three stresses maximum.		2,000	V
$I_{max, DC}$	Maximum DC Input current for any non-supply pin		5	mA
T_a	Ambient temperature	-40	+85	°C
$T_{storage}$	Storage temperature	-40	+125	°C
V_{pulse}, T_{width} *	Voltage surge on vbat		14 10	V μs

Note: Vpulse and Twidth is described below:

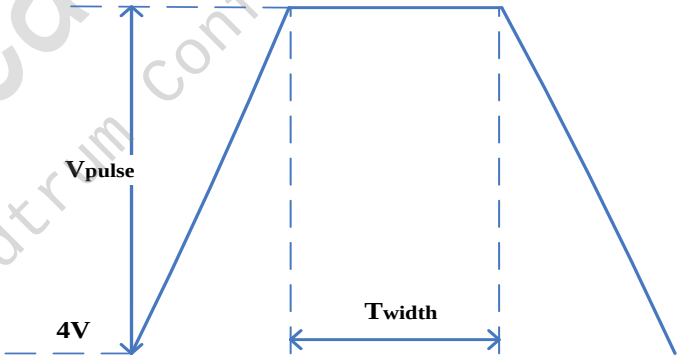


Figure 4-1 Voltage surge on VBAT

4.1.2 Recommended operating conditions

The recommended operating conditions is list in Table 4-2**Error! Reference source not found.**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Table 4-2 Recommended operating conditions

Symbol	Parameter	Min	Typical	Max	Unit
VCHG	Charger input voltage	4.5	5.0	5.5	V
VBAT	Supply voltage from a battery	3.2	3.6	4.5	V
$T_{junction}$	Junction temperature	-20		+125	°C
$T_{ambient}$	Ambient operating temperature	-40		+85	°C

Note1: Hardware stops charging if VCHG is higher than 9.2V and the maximum value of VCHG can be set by software. The higher maximum value of VCHG, the stricter Vds requirement of external MOSFET.

Note2: The value set by software should be 10% higher than maximum value of VCHG listed in table to guarantee all chips can stop charging over the maximum value of VCHG.

4.1.3 Thermal characteristics

The thermal characteristics are as shown in Table 4-3.

Table 4-3 Thermal characteristics

Symbol	Parameter	Condition	Value	Unit
Theta JA	Junction-to-Ambient thermal resistance	Air flow: 0 m/sec	46.6	°C/watt

4.1.4 ESD characteristics

The ESD characteristics are shown in Table 4-4.

Table 4-4 ESD characteristics

Symbol	Parameter	Condition	Value	Unit
HBM	Human body model	MIL STD 883G, method 3015.7	±2K	V
CDM	Charged-device model	JESD22-C101-C	±800	V
MM	Machine model	JESD22-A115-A	±200	V

4.1.5 DC characteristics

SC6531 I/O supply (VDDIO) is typically at 1.8 V. The analog circuits are typically powered at 2.8V/3.0 V. The core and analog power supplies are provided by the on-chip LDOs. The external battery can be connected directly to pins VBATPA, VBATA, VBATB. If not specified, VBAT means all above VBAT. The power pins should be connected with a decoupling capacitor to ground (VSS).

For the following table, T_{amb} = -40 to +85 °C, VSS = 0 V (ground), VBAT = 3.6 V, and all voltages are measured with respect to VSS, unless otherwise specified.

Table 4-5 DC characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
I_{dp}	Deep power-down current	The whole chip is powered down by software		40		uA
Digital supply voltage: pins VDDIO						
VDDIO	Digital supply		1.5	–	2.1	V

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
	voltage					
Digital input						
V_{IL}	Input voltage LOW-level		0	–	0.3 Vpad	V
V_{IH}	Input voltage HIGH-level		0.7 Vpad	–	Vpad	V
I_{LI}	Input leakage current		–	±2	–	μA
Digital output						
V_{OL}	Output voltage LOW-level	At I_{sink} = 2,4,6,10 mA (programmable)	0	–	0.1 Vpad	V
V_{OH}	Output voltage HIGH-level	At I_{source} = 2,4,6,10 mA (programmable)	0.9 Vpad	–	Vpad	V
Analog supply voltage: pins VBAT						
VBAT	Analog supply voltage		3.3	3.6	4.35	V
Analog supply voltage: internal AVDDVB						
AVDDVB	Audio analog core supply voltage		3.1	3.3	3.5	V
RTC supply: pin VBATBK						
VBATBK	Supply voltage			2.8	3.35	V
I_{VBATBK}	Supply current			10		μA

Note1: Vpad means the power supply voltage at the corresponding pad.

Note2: I_{VBATBK} means the VBATBK current consumption in power down mode.

4.2 AC characteristics

A pin's AC characteristics include input and output capacitance, which determine loading for external drivers or other load analysis. The AC characteristics also include a de-rating factor, which indicates how much faster or slower the AC timings get with different loads.

Table 4-6 Standard input, output and I/O pin AC characteristics

Symbol	Parameters	Min	Typical	Max	Units
C_{in}	Input capacitance, all standard input and IO pins			3.5	pF
C_{load}	Output capacitance, all standard output and IO pins			30	pF
T_{dr}	Output de-rating falling edge on all standard output and I/O pins, from 30 pF load		0.166		ns/pF

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Note: The AC specifications are tested with a 30 pF load as indicated in Figure 4-2 Test circuit of an I/O pin

.

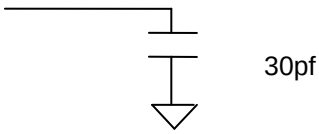


Figure 4-2 Test circuit of an I/O pin

The output capacitance and de-rating falling edge are measured under the condition of maximum driving strength: 24 mA @ 3 V.

For the following tables, T_{amb} = -40 to +85 °C, VSS = 0 V (ground), and all voltages are measured with respect to VSS, unless otherwise specifie

Table 4-7 AC characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
f_{mclk}	Master clock frequency		–	26	–	MHz
f_{rtcclk}	Real-time clock frequency		–	32.768	–	kHz
Digital input						
C_I	Input capacitance		–	3	–	pF
Digital output						
T_R	Output rise time	Output load = 20 pF	2	–	5	ns
T_F	Output fall time	Output load = 20 pF	2	–	5	ns
Master clock input						
$\Delta f/f_{mclk}$	Frequency compensation range		-27		27	ppm
V_{mclk}	Master clock amplitude		0.4	–	2.4	V
δ_{mclk}	Master clock duty cycle		40	–	60	%
Real-time clock input						
$\Delta f/f_{rtclk}$	Frequency tolerance	Standard deviation	-80		80	ppm
δ_{rtclk}	Clock duty cycle		35	–	65	%

Note1: f_{mclk} and f_{rtcclk} are analog pad, so the input and output signal can be sinewave, triangular wave or square wave.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

4.3 Performance specification

4.3.1 Phase-Locked Loop

Table 4-8 Performance of the phase-locked loop

Parameter	Conditions/Comments	Min	Typ	Max	Unit
Power supply	Digital power Analog power		1.1 2.8		V
Input reference			26		MHz
Frequency Range	APLL		624		MHz
	CPLL		832		MHz
Period jitter of PLL	All other circuits on		±50		ps
Settling time			80	200	μs
Sleep mode	Yes				
Iapll(624M)	2.8V		1		mA
Icpll(832M)	2.8V		1		mA
I_{dig}	1.1V		0.2		mA

4.3.2 USB 1.1 PHY

The USB 1.1 PHY in SC6531 is fully compliant with USB 1.1 specifications. Please refer to Universal Serial Bus Specification revision 1.1 at http://www.usb.org/developers/docs

4.3.3 Automatic power control (APC)DAC

One general DAC is used to control power ramping and gain in SC6531. It is a 10 bits D/A converters with a programmable-gain output driver. Special offset cancellation is applied in the DAC.

Table 4-9 Performance of the APC DAC

Parameter	Conditions/Comments	Min	Typical	Max	Unit
Power supply		2.6	2.8	2.85	V
Resolution			10		bits
Differential non-linearity		-1,		+1	LSB
Gain range		1.3	1.5	2	x
Minimum output voltage			50		mV
Minimum load resistance			50		kΩ
Maximum load capacitance			100		pF

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5 Micro-Controller Unit Subsystem

SC6531 has two embedded processor cores: ARM926EJ-S and Teaklite. In general, the MCU and DSP control the operation of various ASIC hardware modules. The MCU or DSP prepares the data that needs the ASIC to process and sets up some control registers that tells the ASIC how to process the data. Therefore, the software control interface consists of data memories and control registers. The software interface sections define the organization of the data memories and the meanings of control register bits.

5.1 Processor

SC6531 contains one 32-bit RSIC core, ARM926EJ-S, which includes features for efficient execution of Java byte codes. The ARM926EJ-S processor supports 32-bit ARM and 16-bit Thumb instruction sets, enabling the users to trade off between high performance and high code density. I t should be noted that VFP coprocessor is removed for cost down.

Arm926EJS processor have many outstanding features:

- 8KB ICache + 8KB DCache
- Frequency is 204Mhz

5.2 ARM memory map

On the ARM side, the address bus is 32-bit wide and the address map is presented in this section. In order to support multiple boot modes, the ARM memory space can be remapped after reset.

5.2.1 ARM9 AHB Memory Map

Table 5-1 MCU AHB address mapping

Address Range	Sector	Description
0x0000_0000 – 0x0FFF_FFFF	External memory space or On-chip ROM space	Remap① = 0: external memory space 0x0000_0000~0x03FF_FFFF : if (pnor_option= 0) SFC memory space else Parallel NOR space (Max 512Mb,128M in SC6531) 0x0400_0000~0x0FFF_FFFF : PSRAM memory space (Max 1536Mb) Remap = 1: on-chip ROM space On-chip ROM space: 0x0000_0000 – 0x0001_5FFF
0x1000_0000 –	On-chip ROM space or	Remap = 0: on-chip ROM space

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1FFF_FFFF	External memory space	On-chip ROM space: 0x1000_0000 – 0x1001_5FFF Remap = 1: external memory space 0x1000_0000~0x13FF_FFFF : if (pnor_option= 0)SFC memory space else Parallel NOR space (Max 512Mb) 0x1400_0000~0x1FFF_FFFF : PSRAM memory space (Max 1536Mb)
0x2000_0000 – 0x200F_FFFF	SMC control registers	
0x2010_0000 – 0x201F_FFFF	DMA control registers	
0x2020_0000 – 0x202F_FFFF	Digital camera space	
0x2030_0000 – 0x203F_FFFF		RESERVED
0x2040_0000 – 0x2040_0FFF	Bus monitor0 space	
0x2040_1000 – 0x2040_1FFF	Bus monitor1 space	
0x2040_2000 – 0x2040_2FFF	Bus monitor2 space	
0x2040_3000 – 0x2040_3FFF	Bus monitor3 space	
0x2040_4000 – 0x2040_FFFF		RESERVED
0x2050_0000 – 0x205F_FFFF	General AHB control registers	1M
0x2060_0000 – 0x206F_FFFF		RESERVED
0x2070_0000 – 0x2070_FFFF	SDIO reg	
0x2080_0000 – 0x208F_FFFF	LCM reg	
0x2090_0000 – 0x209F_FFFF		RESERVED
0x20A0_0000 – 0x20AF_FFFF	SFC reg	
0x20B0_0000 –	MIDI reg	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x20BF_FFFF		
0x20C0_0000 – 0x20CF_FFFF		RESERVED
0x20D0_0000 – 0x20D0_FFFF	LCDC reg	
0x20E0_0000 – 0x20EF_FFFF	LZMA0 reg	
0x20F0_0000 – 0x2FFF_FFFF	Reserved	Was Lzma1 space in 6531
0x3000_0000 – 0x300F_FFFF	Shared memory space0	0x3000_0000 – 0x3000_0FFF For DSP 4KB/64KB:RAL_2Kx16
0x3010_0000 – 0x301F_FFFF	Shared memory space1	0x3010_0000 – 0x3010_03FF For BT 1KB/64KB:256X32BE
0x4000_0000 – 0x4FFF_FFFF	On-chip RAM space	//0x4000_A000 -- 0x4000_FFFF: Switched with BTMemory, IRAM (24KB) //0x4001_0000 -- 0x4001_3FFF: Switched with BT Memory, IRAM (16KB) // for mem first change : ~~0x4000_0000 – 0x4000_3FFF: ARM-dedicated, (16k bytes)~~ ~~0x4000_4000 -- 0x4000_BFFF: 32K IRAM, (cm4 iram , switch with arm9)~~ ~~Include :~~ ~~0x4000_4000 -- 0x4000_97FF: 22K~~ ~~0x4000_9800 -- 0x4000_98FF: 256B~~ ~~0x4000_9900 -- 0x4000_99FF: 256B~~ ~~0x4000_9a00 -- 0x4000_9aFF: 256B~~ ~~0x4000_9b00 -- 0x4000_9bFF: 256B~~ ~~0x4000_9c00 -- 0x4000_abFF: 4KB~~ ~~0x4000_ac00 -- 0x4000_acFF: 256B~~ ~~0x4000_ad00 -- 0x4000_adFF: 256B~~ ~~0x4000_ae00 -- 0x4000_aeFF: 256B~~ ~~0x4000_af00 -- 0x4000_afFF: 256B~~ ~~0x4000_b000 -- 0x4000_bfFF: 4K~~ ~~0x4000_C000 -- 0x4000_CFFF , 4KB Switched with~~ ~~BT Memory, IRAM (4KB)~~ ~~0x4001_D000 -- 0x4000_DFFF: 4KB Switched with BTMemory, IRAM (4KB)~~ // for mem sencond change :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

		~~0x4000_0000 – 0x4000_27FF: ARM-dedicated, (10k bytes)~~ ~~0x4000_2800 -- 0x4000_A7FF: 32K IRAM, (cm4 iram , switch with arm9)~~ ~~Include :~~ ~~0x4000_2800 -- 0x4000_7FFF: 22K~~ ~~0x4000_8000 -- 0x4000_80FF: 256B~~ ~~0x4000_8100 -- 0x4000_81FF: 256B~~ ~~0x4000_8200 -- 0x4000_82FF: 256B~~ ~~0x4000_8300 -- 0x4000_83FF: 256B~~ ~~0x4000_8400 -- 0x4000_93FF: 4KB~~ ~~0x4000_9400 -- 0x4000_94FF: 256B~~ ~~0x4000_9500 -- 0x4000_95FF: 256B~~ ~~0x4000_9600 -- 0x4000_96FF: 256B~~ ~~0x4000_9700 -- 0x4000_97FF: 256B~~ ~~0x4000_9800 -- 0x4000_A7FF: 4K~~ ~~0x4000_A800 -- 0x4000_B7FF , 4KB Switched with BT Memory, IRAM (4KB)~~ ~~0x4001_B800 -- 0x4000_C7FF: 4KB Switched with BTMemory, IRAM (4KB)~~ //----------for cost down , the third change---------// 0x4000_0000 – 0x4000_27FF: ARM-dedicated, (10k bytes) 0x4000_2800 -- 0x4000_7FFF: 22K IRAM, (cm4 iram , switch with arm9) Include : 0x4000_2800 -- 0x4000_6FFF: 18K 0x4000_7000 -- 0x4000_7FFF: 4K for BT calibration 0x4000_8000 -- 0x4000_8FFF , 4KB Switched with BT Memory, IRAM (4KB) for CACHE DATA MEM 0x4000_9000 -- 0x4000_9FFF: 4KB Switched with BTMemory, IRAM (4KB) for CACHE DATA MEM 0x4001_9000 – 0x4001_AFFF : Switched with DSP X memory, sxram2, 8k byte ARM control by default; (8k bytes---RF1SH_2KX32-BE)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

		0x4001_B000 – 0x4002_2FFF : Switched with DSP memory, xram0,xram1, DSP control by default; (32K bytes ---2 RF1SH_8KX16_BE) 0x4002_3000 – 0x4002_EFFF : Switched with DSP memory, pram, DSP control by default
0x5000_0000 – 0x5FFF_FFFF	ARM7 sub-system space	~~Note:~~ ~~Cm4 matrix~~ ~~S1: IROM & IRAM~~ ~~S2: peri~~ ~~S3: shm mem & register~~ Note: Cm4 matrix S1: IROM & IRAM S2: peri & shm mem & register
0x6000_0000 – 0x67FF_FFFF	LCM space	
0x6800_0000 – 0x68FF_FFFF	SPI0 space	
0x6900_0000 – 0x69FF_FFFF	SPI1 space	
0x6C00_0000 – 0x6CFF_FFFF	MCHK space	
0x7000_0000 – 0x7FFF_FFFF	Reserved	
0x8000_0000 – 0x8F00_0FFF	Peripherals space	Apb bus addr space
0x9000_0000 – 0x97FF_FFFF	USB space	
0x9800_0000 – 0x9FFF_FFFF	Rotation space	
0xA000_0000 – 0xBF00_0FFF	Reserved	
0xC000_0000 – 0xDFFF_FFFF	Reserved	
0xE000_0000 – 0xFFFF_FFFB	Reserved	?? code specify address space (0XFFFF_0000 to 0XFFFF_FFFF) to AHB reg
~~0xFFFF_FFFC~~	~~Chip ID~~	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.2.2 ARM9 APB Memory Map

Table 5-2 MCU APB memory address mapping

Address Range	Sector	Description
0x8000_0000 – 0x8000_0FFF	Interrupt controller0	
0x8000_1000 – 0x8000_1FFF	Interrupt controller1	
0x8100_0000 – 0x8100_0FFF	General-purpose timers	
0x8100_1000 – 0x8100_1FFF	Backup General-purpose timers	
0x8100_2000 – 0x8100_2FFF		Reserved
0x8100_3000 – 0x8100_3FFF	System timers	
0x8200_0000 – 0x8200_1FFF	ADI	
0x8200_2000 – 0x8200_2FFF	EFUSE	
0x8200_3000 – 0x8200_3FFF	Voice band controller	
0x8300_0000 – 0x8300_0FFF	UART0	
0x8400_0000 – 0x8400_0FFF	UART1	Shared with DSP
0x8500_0000 – 0x8500_0FFF	UART2	communication with ARM7/BT
0x8600_0000 – 0x8600_0FFF	I2C0	
0x8600_1000 – 0x8600_1FFF	I2C1	
0x8600_2000 – 0x86FF_FFFF	I2C2	RESEVERD
0x8700_0000 – 0x8700_0FFF	Keypad	
0x8700_1000 – 0x8700_2FFF		Reserved
0x8700_3000 –		Reserved,tpc address, have del in 6531

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x8700_3FFF		
0x8800_0000 – 0x8800_0FFF	PWM	
0x8800_2000 – 0x8800_2FFF	FM	
0x8800_3000 – 0x8800_3FFF	ADC	
0x8900_0000 – 0x8900_0FFF	SIM	
0x8900_3000 – 0x89FF_FFFF		Reserved
0x8A00_0000 – 0x8A00_0FFF	GPIO	
0x8A00_1000 – 0x8A00_1FFF	EIC	
0x8A00_2000 – 0x8A00_2FFF	AUD	
0x8A00_3000 – 0x8A00_3FFF	AUDIFD	
0x8A00_4000 – 0x8AFF_FFFF		RESERVERD
0x8B00_0000 – 0x8B00_0FFF	Global control registers	
0x8C00_0000 – 0x8C00_0FFF	PIN control registers	
0x8D01_0000 – 0x8D01_0FFF	GEA	
0x8D02_0000 – 0x8D02_0FFF	AON	
0x8D03_0000 – 0x8DFF_FFFF		RESERVERD
0x8E00_0000 – 0x8E00_0FFF	SPI0	
0x8E00_1000 – 0x8E00_2FFF		reserved
0x8E00_3000 – 0x8E00_3FFF	SPI1	
0x8E00_4000 – 0x8EFF_FFFF		
0x8F00_0000 – 0x8F00_0FFF	IIS0	Shared with DSP
0x8F10_0000 –	IIS1	Shared with DSP

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x8F10_0FFF		
0x8F20_0000 – 0x8FFF_FFFF		RESERVERD

5.2.3 ARM7 AHB Memory Map

Table 5-3 ARM7 System AHB address mapping

Address Range	Sector	Description
0x0000_0000 – 0x0FFF_FFFF	On-chip RAM space	ARM7_boot_sel = 1: 0x0000_0000 – 0x0000_57FF: 22k bytes, shared with ARM9; ARM9 control by default; 0x0000_5800 – 0x0000_58FF: 256 byte, shared with Dcache tag mem0 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_5900 – 0x0000_59FF: 256 byte, shared with Dcache tag mem1 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_5a00 – 0x0000_5aFF: 256 byte, shared with Dcache tag mem2 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_5b00 – 0x0000_5bFF: 256 byte, shared with Dcache tag mem3 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_5c00 – 0x0000_6bFF: 4K byte, shared with Dcache data mem & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_6c00 – 0x0000_6cFF: 256 byte, shared with Icache tag mem0 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_6d00 – 0x0000_6dFF: 256 byte, shared with Icache tag mem1 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_6e00 – 0x0000_6eFF: 256 byte, shared with Icache tag mem2 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

		accessed by ARM7 or ARM9. 0x0000_6f00 – 0x0000_6fFF: 256 byte, shared with Icache tag mem3 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_7000 – 0x0000_8000: 4K byte, shared with Icache data mem & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_8000 – 0x0000_9000: 4k byte, shared with ARM9; ARM9 control by default; If cache enable, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_9000 – 0x0000_a000: 4k byte, shared with ARM9. ARM9 control by default; If cache enable, this 4k byte couldn't be accessed by ARM7 or ARM9. ARM7_boot_sel = 0: external memory space 0x0000_0000~0x0FFF_FFFF // ----------for cost down ----------// ARM7_boot_sel = 1: 0x0000_0000 – 0x0000_57FF , 22k bytes : Ram0 : 0x0000_0000 – 0x0000_47FF: 18k bytes, shared with ARM9, cm4 iram Ram1 : 0x0000_4800 – 0x0000_57FF: 4k bytes, shared with ARM9 and ADDA test , for BT 4K calibration. ARM9 control by default; Ram2 : 0x0000_5800 – 0x0000_67FF: 4k byte, shared with ARM9; ARM9 control by default; If cache enable, this 4k byte couldn't be accessed by ARM7 or ARM9. Ram3: 0x0000_6800 – 0x0000_77FF: 4k byte, shared with ARM9; ARM9 control by default; If cache enable, this 4k byte couldn't be accessed by ARM7 or ARM9. Ram4: 0x0000_7800 – 0x0000_78FF: 256 byte , cache tag mem Ram5: 0x0000_7900 – 0x0000_79FF: 256 byte , cache tag mem Ram6: 0x0000_7a00 – 0x0000_7aFF: 256 byte , cache tag mem Ram7: 0x0000_7b00 – 0x0000_7bFF:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

		256 byte , cache tag mem Ram8: 0x0000_7c00 – 0x0000_7cFF: 256 byte , cache tag mem Ram9: 0x0000_7d00 – 0x0000_7dFF: 256 byte , cache tag mem Ram10: 0x0000_7e00 – 0x0000_7eFF: 256 byte , cache tag mem Ram11: 0x0000_7f00 – 0x0000_7fFF: 256 byte , cache tag mem ARM7_boot_sel = 0: external memory space 0x0000_0000~0x0FFF_FFFF
0x1000_0000 – 0x1EFF_FFFF	External memory space	ARM7_boot_sel = 1: external memory space 0x1000_0000~0x1FFF_FFFF ARM7_boot_sel = 0: 0x1000_0000 – 0x1000_57FF: 22k bytes, shared with ARM9; ARM9 control by default; 0x1000_5800 – 0x1000_58FF: 256 byte, shared with Dcache tag mem0 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_5900 – 0x1000_59FF: 256 byte, shared with Dcache tag mem1 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_5a00 – 0x1000_5aFF: 256 byte, shared with Dcache tag mem2 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_5b00 – 0x1000_5bFF: 256 byte, shared with Dcache tag mem3 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_5c00 – 0x1000_6bFF: 4K byte, shared with Dcache data mem & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_6c00 – 0x1000_6cFF:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

		256 byte, shared with Icache tag mem0 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_6d00 – 0x1000_6dFF: 256 byte, shared with Icache tag mem1 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_6e00 – 0x1000_6eFF: 256 byte, shared with Icache tag mem2 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_6f00 – 0x1000_6fFF: 256 byte, shared with Icache tag mem3 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_7000 – 0x1000_8000: 4K byte, shared with Icache data mem & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_8000 – 0x1000_9000: 4k byte, shared with ARM9; ARM9 control by default; If cache enable, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_9000 – 0x1000_a000: 4k byte, shared with ARM9. ARM9 control by default; If cache enable, this 4k byte couldn't be accessed by ARM7 or ARM9. //----------for cost down ----------// ARM7_boot_sel = 0: 0x0000_0000 – 0x0000_57FF , 22k bytes : Ram0 : 0x1000_0000 – 0x1000_47FF: 18k bytes, shared with ARM9, cm4 iram Ram1 : 0x1000_4800 – 0x1000_57FF: 4k bytes, shared with ARM9 and ADDA test , for BT 4K calibration. ARM9 control by default; Ram2 : 0x1000_5800 – 0x1000_67FF: 4k byte, shared with ARM9; ARM9 control by default; If cache enable, this 4k byte couldn't be accessed by ARM7 or ARM9. Ram3: 0x1000_6800 – 0x1000_77FF: 4k byte, shared with ARM9; ARM9 control by

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

		default; If cache enable, this 4k byte couldn't be accessed by ARM7 or ARM9. Ram4: 0x1000_7800 – 0x1000_78FF: 256 byte , cache tag mem Ram5: 0x1000_7900 – 0x1000_79FF: 256 byte , cache tag mem Ram6: 0x1000_7a00 – 0x1000_7aFF: 256 byte , cache tag mem Ram7: 0x1000_7b00 – 0x1000_7bFF: 256 byte , cache tag mem Ram8: 0x1000_7c00 – 0x1000_7cFF: 256 byte , cache tag mem Ram9: 0x1000_7d00 – 0x1000_7dFF: 256 byte , cache tag mem Ram10: 0x1000_7e00 – 0x1000_7eFF: 256 byte , cache tag mem Ram11: 0x1000_7f00 – 0x1000_7fFF: 256 byte , cache tag mem
0x1F00_0000 – 0x1FFF_FFFF	On-chip ROM space	On-chip ROM space: 0x1F00_0000 – 0x1F00_7FFF(32KB)
0x5000_0000 – 0x500F_FFFF	Share memory	Share memory with ARM9, 1K bytes
0x5010_0000 – 0x501F_FFFF		Reserved
0x5020_0000 – 0x503F_FFFF		Reserved
0x5040_0000 – 0x5040_0FFF	Bus monitor0 space	
0x5040_1000 – 0x5040_1FFF		Reserved
0x5040_2000 – 0x504F_FFFF		Reserved
0x5050_0000 – 0x505F_FFFF	General AHB control registers	
0x5060_0000 – 0x506F_FFFF	Cache registers	
0x5200_0000 – 0x52FF_FFFF	Peripherals space(BT Sys, uart0/1,INTC,APB Reg, Timer,EIC)	
0x5300_0000 – 0x53FF_FFFF:		Only can be accessed by ARM9
Others	The same as ARM9 memory map	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.2.4 ARM7 APB Memory Map

Table 5-4 ARM7 System APB address mapping

Address Range	Sector	Description
0x5200_0000 – 0x5200_FFFF	Interrupt controller	
0x5210_0000 – 0x5210_0FFF	General-purpose timers	
0x5210_1000 – 0x5210_1FFF	Backup General-purpose timers	
0x5210_3000 – 0x5210_3FFF	System timers	
0x5220_0000 – 0x5220_FFFF	ARM7 accesses ADI Master	
0x5230_0000 – 0x5230_FFFF	UART0	
0x5240_0000 – 0x5240_FFFF	UART1	Reserved
0x5250_0000 – 0x525F_FFFF	BT_TOP	Blue tooth sub system
0x5260_0000 – 0x5260_FFFF	EIC	
0x5270_0000 – 0x5270_FFFF	Global control registers	
0x5280_0000 – 0x528F_FFFF		Reserved
0x5290_0000 – 0x529F_FFFF	Watch dog	
0x52A0_0000 – 0x52FF_FFFF		Reserved

5.2.5 CHIP ID

此芯片一共具有六种 ID 类型，具体如下：

1、 chip ID : SC6531 (ASCII :4Eh , 65h , 6Dh , 6Fh , 47h)

2、 platform ID : SC6531 (ASCII :4Eh , 65h , 6Dh , 6Fh , 47h)

3、 project ID : SC6531 (ASCII : 53h , 43h, 36h, 35h, 36h, 32h)

4、 manufacture ID : 101

(bit [15:0] process : 1 40nm lp
Bit[7:0] foundry : 1 umc)

5 \ implementation ID : 201

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

(bit [15:0] memory compiler : 2 synopsys
Bit[7:0] stand cell library founder : 1 arm)
6\ version ID : metal fix + anlg_chip_id
ID Address is base on SC6531 ARM9 APB Control Register. excel

5.2.6 Analog Die Digital Memory Map

5.2.6.1 ARM side space

ARM can access the following module from ADI master side,

Figure 5-1 ARM side module space mapping

ARM address	module	Description
0x8200_0000~0x8200_0fff	D-die ADI mst controller	
0x8200_1000~0x8200_101f	PWM	
0x8200_1020~0x8200_103f	Ana int	
0x8200_1040~0x8200_107f	Watchdog	
0x8200_1080~0x8200_10bf	cal	
0x8200_10C0~0x8200_10ff	Aud if	
0x8200_1100~0x8200_113f	Pin_reg	
0x8200_1140~0x8200_117f	Ptest	
0x8200_1180~0x8200_11ff	Rtc	
0x8200_1200~0x8200_127f	Eic	
0x8200_1280~0x8200_12ff	Aud_dig	
0x8200_1300~0x8200_137f	auxadc	
0x8200_1380~0x8200_13ff	Aud_ana	
0x8200_1400~0x8200_15bc	Glb reg	
0x8200_16c0~0x8200_1fff	reserved	

5.2.6.2 DSP side space

Figure 5-2 DSP side module space mapping

DSP address	module	Description
0xbb00~0xbb1f	Adi master control register	
0xbb20~0xbb3f	Ana share register	
0xbb40~0xbb7f	ANA dsp register	
0xbb80~0xbbbf	Audio if	
0xbbc0~0xbbff	Self_cal	

5.2.6.3 Access priority setting

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

The read or write priority is based on the following rules :

Each master can read other master's space registers. For example, ARM can read dsp side registers and DSP can also read arm side registers. But the read method must obey the notes in "ADI design specification".

Except shared module, each master cannot write other masters' space. So, ARM cannot write dsp register and dsp cannot write ARM side's registers or modules

"share register" and "audio if" are two share blocks which can be write both by ARM and DSP. There are two bits in arm register which are used to control the write ability: "SHARE_REG_MASTER_SEL" and "AUDIFA_MASTER_SEL", when these two bits set to 1, dsp can write the two blocks, otherwise ARM can write these two blocks

For RF pbus space, ARM can write directly from space 0x8200_0800 to 0x8200_0fff, but to DSP, only STC scheduler can write this space with SBI bus, the SBI word send by SBI master will convert to RF Pbus protocol and send to RF side.

5.3 Internal memory controller

5.3.1 MCU Internal RAM

The MCU internal RAM is dedicated for MCU instruction and date. The size of MCU internal dedicated RAM is 16K bytes (4K words of 32 bits). It can be accessed in 32, 16 or 8-bit operations. Further more, another 8K bytes RAM MCU can access which is shared with DSP system.

5.3.2 MCU Internal ROM

The MCU internal ROM has 88K bytes. Part of the ROM is for boot/download purposes and others are for RTOS, multimedia application and other functions.

5.3.3 MCU-DSP Switched RAM

The MCU-DSP switched RAM is designed for MCU and DSP to transfer data bi-directionally. The difference with the MCU-DSP shared RAM is that only one port (MCU or DSP) can access the MCU-DSP switched RAM at certain time.

When there is no need to exchange data between MCU and DSP, the MCU-DSP switched RAM can be used as MCU internal RAM or DSP Data RAM.

Details of RAM size and address mapping as blew :

For ARM SIDE :

1\ 0x4001_9000 – 0x4001_AFFF

Switched with DSP memory, xram2, pls refer to TABLE 2 ---2K XRAM2(nt0), 2K XRAM2(nt1)

ARM control by default;

(8k bytes---RF1SH_2KX32-BE)

2\ 0x4001_B000 – 0x4002_2FFF :

Switched with DSP memory, xram0,xram1, pls refer to TBALE 2 ---8K XRAM0, 8K XRAM1

DSP control by default;

(32K bytes ---2 RF1SH_8KX16_BE)

3\ 0x4002_3000 – 0x4002_EFFF :

Switched with DSP memory, pram, pls refer to TABEL 1 --- 24K PRAM

DSP control by default;

(48K byte ---RA1SL_12288X32_BE)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

TABEL 1 ----- DSP program memory space

<table>
<tr><td colspan="5">SC6531(old)</td><td colspan="5">SC6531(New)</td></tr>
<tr><td>ADDR</td><td>PG0</td><td>PG1</td><td>PG2</td><td>PG3</td><td>ADDR</td><td>PG0</td><td>PG1</td><td>PG2</td><td>PG3</td></tr>
<tr><td>0000~1FFF</td><td colspan="4" rowspan="3">24K PRAM
PART1</td><td>0000~1FFF</td><td colspan="4" rowspan="3">24K PRAM</td></tr>
<tr><td>2000~3FFF</td><td>2000~3FFF</td></tr>
<tr><td>4000~5FFF</td><td>4000~5FFF</td></tr>
<tr><td>6000~7FFF</td><td rowspan="3">（40K-256）
PRAM
PART2</td><td rowspan="5">40K
PROM0
PART1</td><td>16K
PROM0
PART2</td><td rowspan="2">40K
PROM1
PART1</td><td>6000~7FFF</td><td rowspan="3">（40K-256）
PROM2</td><td rowspan="5">40K
PROM0
PART1</td><td>16K
PROM0
PART2</td><td>40K
PROM1
PART1</td></tr>
<tr><td>8000~9FFF</td><td>8000~9FFF</td><td>24K
PROM1
PART2</td></tr>
<tr><td>A000~BFFF</td><td>24K
PROM1
PART2</td><td>A000~BFFF</td></tr>
<tr><td>C000~FEFF</td><td></td><td>C000~FEFF</td><td></td><td></td></tr>
<tr><td>FF00~FFFF</td><td>256 WORDS
BOOT ROM
PROM0 PART3</td><td></td><td></td><td>FF00~FFFF</td><td>256 WORDS
BOOT ROM
PROM0 PART3</td><td></td><td></td><td></td></tr>
</table>

TABEL 2 ----- DSP data memory space

ADDR	PG0	PG1
0000~1FFF	8K XRAM0	
2000~3FFF	8K XRAM1	
4000~47FF	2K(1st)/43K XROM0	
4800~93FF	19K(2nd) /43K XROM0	19K(5th)/43K XROM0
9400~97FF	1K(3rd) /43K XROM0	1K XRAM3
9800~9FFF	2K(4th) /43K XROM0	2K XRAM2(nt0)
A000~A7FF	2K XRAM2(nt1)	
A800~AFFF	2K SHARE MEM Z space	
B000~BFFF	4K Z space	
C000~DFFF	8K YROM0	
E000~EFFF	4K(1st)/12K YRAM0	4K(3rd))/12K YRAM0
F000~FFFF	4K(2nd))/12K YRAM0	

5.3.3.1 Control Register Descriptions

Physical address: 0x8B00_01A0

Description: switch control signal, locates at APB bus in MCU side.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Address	Signal	Bit Pos	name	Default	Description
0x8B00_01A0	APB_MCU_CTL0	[21]	ARM_MEM3_EN	0	Arm_mem3_en If 1: memory is switched to ARM If 0: memory is switched to DSP It is switched to DSP by default.
		[20]	ARM_MEM2_EN	0	It is switched to DSP by default.
		[19]	ARM_MEM1_EN	1	It is switched to ARM by default.

5.3.4 MCU-DSP Shared RAM

The MCU-DSP shared memory acts as a communication bridge between MCU and DSP in both directions. Through it commands and data are transferred/exchanged from one system to another in real time. The size of the MCU-DSP shared memory is 4K bytes (2K words of 16 bits).

The MCU-DSP shared RAM can be accessed by AHB bus and DSP ZBUS.

5.3.4.1 Features

- For MCU and DSP, only half-word (16 bits) access is supported.
- Dedicated reset control is supported.

5.3.4.2 Functional Description

The block diagram is shown in the figure 3-2.

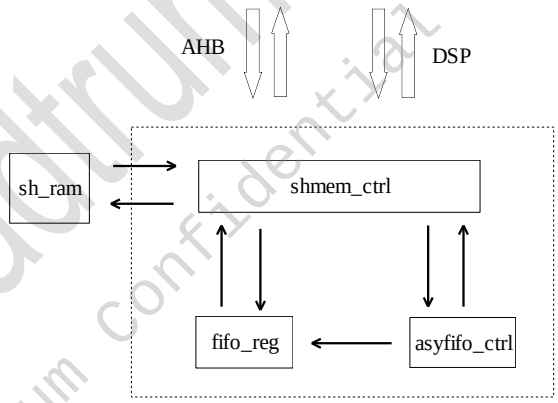


Figure 5-3 Shared memory controller block diagram

sh_ram: single port SRAM,

shmem_ctrl: sub module performs arbitration of the system

FIFO reg: register array, part of asynchronous FIFO

asyfifo_ctrl: control module of asynchronous FIFO

Table 5-3 Shared memory address mapping

MCU address	Shared RAM address	DSP address
0x1000_0000	0x0	0xa800

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1000_0002	0x1	0xa801
……	……	……
……	……	……
0x1000_0ffe	0x7ff	0xafff

5.3.4.3 Operations

5.3.4.3.1 Operation Priority of the MCU-DSP Shared Memory

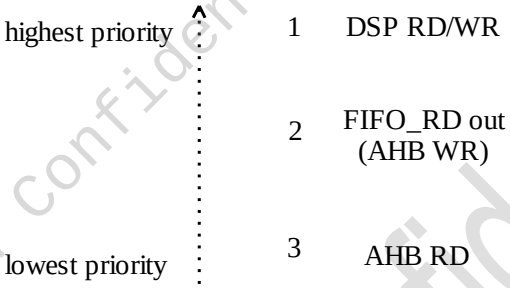


Figure 5-4 Operation priority of MCU-DSP shared memory

5.3.4.3.2 AHB BUS Access and DSP-ZBUS Access

1) DSP read or write : DSP read or write command is responded with the highest priority.
2) AHB write : If the FIFO is not full, AHB write data is written to the FIFO; otherwise, AHB HREADY_out signal is stretched to low until FIFO is not full.
3) If the port of shared RAM is not occupied by DSP operation, the un-empty FIFO data is loaded to the shared RAM.
4) AHB read : AHB read operation is distributed with lowest priority. While port of shared memory is in idle state, the data can be read out. Since HCLK and CLK_DSP are in different clock domains, asynchronous handshaking is necessary.

5.3.4.3.3 Performance of the MCU-DSP Shared Memory Controller

Table 5-4 Performance of the MCU-DSP shared memory controller

		DSP WR/RD	AHB WR	AHB RD
F_{ahb} = 90 MHz F_{dsp} = 90 MHz	HCLK	-	2 cycles while DSP access sh_ram with full-speed	10~11 cycles
	CLK_DSP	Standard z-bus	-	-

5.3.4.4 Programming Notes

- Only AHB half-word access is supported.
- Only AHB big endian is supported.
- Resetting shared memory may change the value in it.
- As to enhance the performance, asynchronous writing FIFO is adopted. So it may be incorrect when reading the same address right after writing opteration, as reading has the higher priority. It's strongly recommended waiting a little time when performing the above operation.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.4 LCM controller

5.4.1 Overview

The LCM is a single-AHB-channel i80-MCU-interface LCM controller

5.4.2 Features

5.4.2.1 AHB Related Features

General features:

1 Support single AHB channel.
2 CS mapping is configurable. Support 4 options: HADDR[27:26], HADDR[26:25], HADDR[25:24], HADDR[24:23].

Write buffer features:

- 8*32 single buffer

5.4.2.2 External LCM Related Features

Device type:

- Only support DBI type B interface, or i80 MCU interface
- Support RGB565 format on 8-bit or 16-bit interface
- Support RGB666 format on 9-bit or 18-bit interface
- Support RGB888 format on 8-bit or 16-bit or 24-bit interface

Operation mode features:

- Up to 4 chip select
- Up to 9-bit address output. Normally only bit-0 output as LCMCD.
- Up to 32-bit data bus. Normally, for different chips, data bus width may be 8-bit, 9-bit, 16-bit, 18-bit or 24-bit.
- 8-bit splitting – one/two/three/four data
- 9-bit splitting – one/two data
- 12-bit splitting – one/two data
- 16-bit splitting – one/two data
- 32-bit splitting (no splitting) – one data
- Asynchronous single read
- Asynchronous single write
- Support FMARK trigging mode during DMA refreshing LCM

Timing features:

Common timing features:

- Read to read turn around: no turn around, 1-cycle, …, 15-cycle
- Read to write turn around: no turn around, 1-cycle, …, 15-cycle
- Write to read turn around: no turn around, 1-cycle, …, 15-cycle
- Write to write turn around: no turn around, 1-cycle, …, 15-cycle

Each CS timing features - writing:

- Asynchronous single write time or CE# low width: 1-cycle, …, 31-cycle
- Access start to WE# low delay time: 0-cycle, 1-cycle, …, 7-cycle
- WE# low width: 0-cycle, 1-cycle, …, 15-cycle
- Access end to output data invalid delay time: 0-cycle, 1-cycle

Each CS timing features - reading:

- Asynchronous single read time or CE# low width: 1-cycle, …, 31-cycle
- Access start to OE# low delay time: 0-cycle, 1-cycle, …, 7-cycle

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.4.3 Signal descriptions

Table 5.4-1 LCM Signal Description

PAD name	Direction	Description	Note
LCMRST#	output	Software-controlled reset	LCMRST# isn't controlled by system reset, and the default value is DON'T KNOWN.
LCMCS# [3:0]	output	chip select, active low	The controller support up to 4 chip select. But for different chips, this number may be different.
LCMRD#	output	read indicate, active low	
LCMWR#	output	write indicate, active low	
LCMCD	output	code/data select	The controller support up to 9-bit address bus width. The chip chooses one bit of address bus as LCMCD, and other bits may be used as extended functions or don't output. Normally, bit-0 is used as LCMCD and other bits don't output.
LCMD	inout	data bus	The controller supports up to 32-bit data bus width. But normally, for different chips, data bus width may be 8-bit, 9-bit, 16-bit, 18-bit or 24-bit.
LCMFMARK	input	fmark indicate	The FMARK function is only used during DMA refreshing LCM.

5.4.1 Timing Description

Table 5.4-2 LCM Timing Parameters

Parameter	Description
tCTC	CS# to CS# turn around time, 1~15 cycles rf_t_rr, rf_t_rw, rf_t_wr, rf_t_ww are used to configure tCTC
tCLPW	CS# Low Pulse Width, 1~31 cycles rf_t_access_r is used to configure tCLPW during reading rf_t_access_w is used to configure tCLPW during writing
tWS	CS# low to WR# low, 0~7 cycles rf_t_we_stp_w is used to configure tWS during writing
tWLPW	WR# Low Pulse Width, 1~15 cycles rf_t_we_wdt_w is used to configure tWLPW during writing
tWH	WR# high to CS# high tWH is (tCLPW – tWS – tWLPW) during writing
tWHPW	WR# High Pulse Width

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	tWHPW is (tWH + tCTC + tWS) during writing
tRS	CS# low to RD# low, 0~7 cycles rf_t_oe_stp_r is used to configure tRS during reading
tRLPW	Read Low Pulse Width tRLPW is (tCLPW – tRS) during reading
tRHPW	Read High Pulse Width tRHPW is (tCTC + tRS) during reading
tWDS	Write Data Valid to WR# High Setup time tWDS is (tWS + tWLPW) during writing
tWDH	WR# High to Write Data Invalid Hold time tWDH is (tWH + rf_t_data_oe_hld_w) during writing
tRDS	Read Data Valid to CS# High Setup time tRDS > 10ns
tRDH	CS# High to Read Data Invalid Hold time tRDH > 0ns

Note: The clock is AHB bus clock, which is different in different chips.

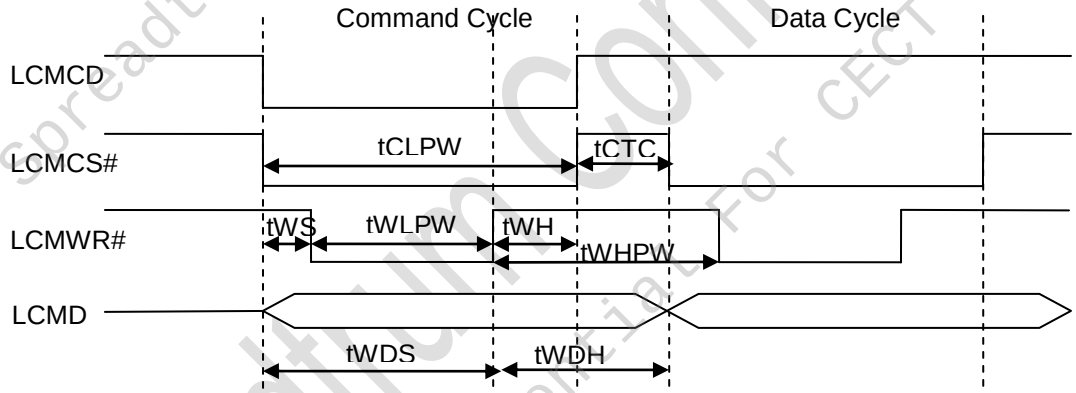


Figure 5-5 LCM Writing Timing Diagram

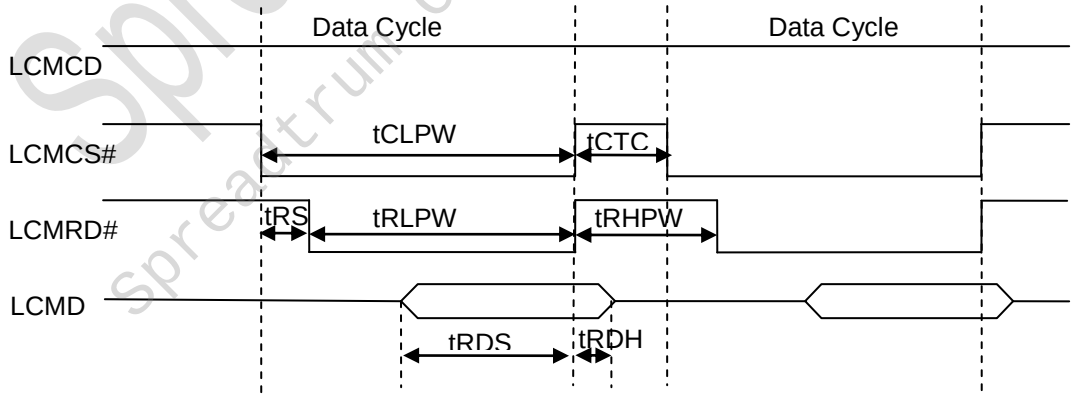


Figure 5-6 LCM Reading Timing Diagram

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.4.2 Control registers

5.4.2.1 Memory map

ARM base address: 0x2080_0000

Offset Address	Name	Description
0x1000	LCM_CFG0	LCM general control register 0
0x1004	Reserved	
0x1008	LCM_STS0	LCM general status register 0
0x100C	Reserved	
0x1010	LCM_CFG0_CS0	LCM CS0 control register 0
0x1014	LCM_CFG1_CS0	LCM CS0 control register 1
0x1018	Reserved	
0x101C	Reserved	
0x1020	LCM_CFG0_CS1	LCM CS1 control register 0
0x1024	LCM_CFG1_CS1	LCM CS1 control register 1
0x1028	Reserved	
0x102C	Reserved	
0x1030	LCM_CFG0_CS2	LCM CS2 control register 0
0x1034	LCM_CFG1_CS2	LCM CS2 control register 1
0x1038	Reserved	
0x103C	Reserved	
0x1040	LCM_CFG0_CS3	LCM CS3 control register 0
0x1044	LCM_CFG1_CS3	LCM CS3 control register 1
0x1048	Reserved	
0x104C	Reserved	

5.4.2.2 Register descriptions

5.4.2.2.1 LCM_CFG0

Description: LCM general control register

This register is LCM general control register, shared by all external LCM.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1000	LCM general control register 0 (Reset 0x33330000)												LCM_CFG0			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	rf_t_ww				rf_t_wr				rf_t_rw				rf_t_rr			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														rf_cs_position	
Type	RO														RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
rf_t_ww	[31:28]	RW	4'h3	rf_t_ww Write to write turn around time 0: no turn around 1: 1 HCLK cycle 2: 2 HCLK cycle … 15: 15 HCLK cycle
rf_t_wr	[27:24]	RW	4'h3	rf_t_wr Write to read turn around time 0: no turn around 1: 1 HCLK cycle 2: 2 HCLK cycle … 15: 15 HCLK cycle
rf_t_rw	[23:20]	RW	4'h3	rf_t_rw Read to write turn around time 0: no turn around 1: 1 HCLK cycle 2: 2 HCLK cycle … 15: 15 HCLK cycle
rf_t_rr	[19:16]	RW	4'h3	rf_t_rr Read to read turn around time 0: no turn around 1: 1 HCLK cycle 2: 2 HCLK cycle … 15: 15 HCLK cycle
Reserved	[15:2]	RO	0	Reserved
rf_cs_position	[1:0]	RW	2'h0	rf_cs_position 0: CS[2:0] mapping to {HADDR[30],HADDR[27:26]} 1: CS[2:0] mapping to HADDR[27:25]

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
				2: CS[2:0] mapping to HADDR[26:24] 3: CS[2:0] mapping to HADDR[25:23]

5.4.2.2.2 **LCM_STS0**

Description: LCM status

This register indicates LCM status.

0x1008			LCM general status register 0 (Reset 0x10000000)												LCM_STS0	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														rfsts_smem_busy	rfsts_wbuf_wr_busy
Type	RO														RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Reserved	[31:2]	RO	0	Reserved
rfsts_smem_busy	[1]	RO	0	rfsts_smem_busy 0: LCM idle 1: LCM access
rfsts_wbuf_wr_busy	[0]	RO	0	rfsts_wbuf_wr_busy 0: write buffer idle or AHB writes write buffer 1: write buffer writes LCM

5.4.2.2.3 **LCM_CFG0_CSx**

Description: LCM CSx control register

This register is used to configure general information for external LCM CSx.

Each CS has an independent registers.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1010 0x1020 0x1030 0x1040 0x1050	LCM CS0 control register 0 (Reset 0x10000000) LCM CS1 control register 0 (Reset 0x10000000) LCM CS2 control register 0 (Reset 0x10000000) LCM CS3 control register 0 (Reset 0x10000000) LCM CS4 control register 0 (Reset 0x10000000)	LCM_CFG0_CS0 LCM_CFG0_CS1 LCM_CFG0_CS2 LCM_CFG0_CS3 LCM_CFG0_CS4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved									rf_data_swt		rf_data_num		rf_data_mode		
Type	RW									RW		RW		RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Reserved	[31:7]	RO	0	Reserved
rf_data_swt	[6:5]	RW	2'h0	rf_data_swt Splitting part transmitting sequence
rf_data_num	[4:3]	RW	2'h0	rf_data_num LCM data splitting number 0: one splitting part is transmitted 1: one splitting part is transmitted 2: one splitting part is transmitted 3: one splitting part is transmitted
rf_data_mode	[2:0]	RW	3'h0	rf_data_mode LCM data splitting mode 0: splitting by 8-bit 1: splitting by 16-bit 2: splitting by 32-bit, or no splitting 3: splitting by 9-bit 4: splitting by 12-bit 5: Reserved 6: Reserved 7: Reserved

5.4.2.2.4 LCM_CFG1_CSx

Description: LCM CSx control register

This register is used to configure general information for external LCM CSx.

Each CS has an independent registers.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1014 0x1024 0x1034 0x1044 0x1054	LCM CS0 control register 1 (Reset 0x03FF0744) LCM CS1 control register 1 (Reset 0x03FF0744) LCM CS2 control register 1 (Reset 0x03FF0744) LCM CS3 control register 1 (Reset 0x03FF0744) LCM CS4 control register 1 (Reset 0x03FF0744)	LCM_CFG1_CS0 LCM_CFG1_CS1 LCM_CFG1_CS2 LCM_CFG1_CS3 LCM_CFG1_CS4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved						rf_t_access_w					rf_t_access_r				
Type	RO						RW					RW				
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rf_t_ce_hld_w	rf_t_ce_hld_r	rf_t_ce_stp_r	rf_t_ce_stp_r	rf_t_we_wdt_w				rf_t_data_oe_hld_w	rf_t_we_stp_w			rf_t_oe_hld_r	rf_t_oe_stp_r		
Type	RW	RW	RW	RW	RW				RW	RW			RW	RW		
Reset	0	0	0	0	0	1	1	1	0	1	0	0	0	1	0	0

Field Name	Bit	Type	Reset Value	Description
Reserved	[31:26]	RO	0	Reserved
rf_t_access_w	[25:21]	RW	5'h1F	rf_t_access_w For write operation: It's access cycle, or CE# low width
rf_t_access_r	[20:16]	RW	5'h1F	rf_t_access_r For read operation: It's access cycle, or CE# low width
rf_t_ce_hld_w	[15]	RW	1'b0	rf_t_ce_hld_w For write operation: It's the delay cycle from CE# high to access end
rf_t_ce_hld_r	[14]	RW	1'b0	rf_t_ce_hld_r For read operation: It's the delay cycle from CE# high to access end
rf_t_ce_stp_w	[13]	RW	1'b0	rf_t_ce_stp_w For write operation: It's the delay cycle from access start to CE# low
rf_t_ce_stp_r	[12]	RW	1'b0	rf_t_ce_stp_r For read operation: It's the delay cycle from access start to CE# low
rf_t_we_wdt_w	[11:8]	RW	4'h7	rf_t_we_wdt_w For write operation: It's the width cycle of WE# low
rf_t_data_oe_hld_w	[7]	RW	1'b0	rf_t_data_oe_hld_w For write operation: It's the delay cycle from CE# high to data output invalid

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
rf_t_we_stp_w	[6:4]	RW	3'h4	rf_t_we_stp_w For write operation: It's the delay cycle from access start to WE# low
rf_t_oe_hld_r	[3]	RW	1'b0	rf_t_oe_hld_r For read operation: It's the delay cycle from OE# high to access end
rf_t_oe_stp_r	[2:0]	RW	3'h4	rf_t_oe_stp_r For read operation: It's the delay cycle from access start to OE# low

5.4.3 Application notes

5.4.3.1 Application Notes

5.4.3.1.1 How to control LCMCD or LCMA[8:0]

LCMCD is LCMA[0], mapped to HADDR[17]. That is, if software write address is (base_addr + 0x10000000 + offset), LCMCD is 0; and if software write address is (base_addr + 0x10020000 + offset), LCMCD is 1.

LCMA[8:0] is mapped to HADDR[25:17]

5.4.3.1.2 How to transmit data to LCMD[31:0]

Refer to the following table:

Table 5.4-3 LCMD Mapping Description

			AHB WORD Write				AHB HALF Write		AHB BYTE Write
			LCM 1st tranmit	LCM 2nd tranmit	LCM 3rd tranmit	LCM 4th tranmit	LCM 1st tranmit	LCM 2nd tranmit	LCM 1st tranmit
data_mode = 0	data_num = 0	data_swt = 0	[7:0]	-	-	-	[7:0]	-	[7:0]
	data_num = 1	data_swt = 0	[7:0]	[15:8]	-	-	[7:0]	[15:8]	-
		data_swt = 1	[15:8]	[7:0]	-	-	[15:8]	[7:0]	-
	data_num = 2	data_swt = 0	[7:0]	[15:8]	[23:16]	-	-	-	-

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

		data_swt = 1	[15:8]	[7:0]	[23:16]	-	-	-	-
		data_swt = 2	[23:16]	[7:0]	[15:8]	-	-	-	-
		data_swt = 3	[23:16]	[15:8]	[7:0]	-	-	-	-
	data_num = 3	data_swt = 0	[7:0]	[15:8]	[23:16]	[31:24]	-	-	-
		data_swt = 1	[15:8]	[7:0]	[31:24]	[23:16]	-	-	-
		data_swt = 2	[23:16]	[31:24]	[7:0]	[15:8]	-	-	-
		data_swt = 3	[31:24]	[23:16]	[15:8]	[7:0]	-	-	-
data_mode = 1	data_num = 0	data_swt = 0	[15:0]	-	-	-	[15:0]	-	-
	data_num = 1	data_swt = 0	[15:0]	[31:16]	-	-	-	-	-
		data_swt = 1	[31:16]	[15:0]	-	-	-	-	-
data_mode = 2	data_num = 0	data_swt = 0	[31:0]						
data_mode = 3	data_num = 0	data_swt = 0	[8:0]	-	-	-	[8:0]	-	-
	data_num = 1	data_swt = 0	[8:0]	[17:9]	-	-	-	-	-
		data_swt = 1	[17:9]	[8:0]	-	-	-	-	-
data_mode = 4	data_num = 0	data_swt = 0	[11:0]	-	-	-	[11:0]	-	-
	data_num = 1	data_swt = 0	[11:0]	[23:12]	-	-	-	-	-
		data_swt = 1	[23:12]	[11:0]	-	-	-	-	-

5.5 SRAM Memory controller

5.5.1 Overview

SMC is a single AHB channel SRAM-like memory controller, supporting 16-bit NOR-Flash, pSRAM, SRAM, and other SRAM-timing-compatible devices.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.5.2 Features

5.5.2.1 AHB Related Features

General features:

1 Support single 32-bit AHB channel.
2 Support all AHB-compatible transaction.
3 Chip select mapping is configurable. Support 4 options: mapping to HADDR[27:26], HADDR[26:25], HADDR[25:24] or HADDR[24:23].
4 For read, support direct read mode and buffered read mode. Two modes can be configured independently according to transaction types – BYTE, HALF or WORD. .
5 For write, support 16-bit buffered write mode and 32-bit buffered write mode. Two modes can be configured independently according to transaction types – BYTE, HALF or WORD.

Read features:

- Direct read mode is more efficient for the cases that AHB data throughput is not less than memory throughput, such as:
  - WORD transactions
  - HALF transactions on SDR or asynchronous memory
  - BYTE transactions on asynchronous memory
- Buffered read mode is more efficient for the cases that AHB data throughput is less than memory throughput, such as:
  - HALF transactions on DDR
  - BYTE transactions on DDR or SDR

Write features:

- 16-bit buffered write mode is used for SDR or asynchronous memory
- 32-bit buffered write mode is used for DDR

5.5.2.2 External Memory Related Features

Device type:

- All kinds of 16-bit NOR-FLASH
- All kinds of 16-bit pSRAM and SRAM
- Other SRAM-timing-like 16-bit devices
- Non-ADMUX (ADP), ADMUX (ADM), AADMUX (AADM)
- Asynchronous mode, synchronous SDR mode, synchronous DDR mode

Operation mode features:

- 4 chip select
- ADP, ADM, AADM
- Only support 16-bit data width
- Asynchronous single read
- Asynchronous page read
- Synchronous burst read - SDR
- Synchronous burst read - DDR
- Synchronous single write
- Synchronous burst write - SDR
- Synchronous burst write - DDR
- Page: 4, 8, 16 or 32
- HCLK mode and HCLK/2 mode
- Wrap burst and increase burst
- Burst length: 4, 8, 16, 32 or continuous
- Fix latency and variable latency
- Support WAIT/RDY for variable latency

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

- Support row boundary auto-detecting for fix latency
- Row length: 64, 128, 256, 512 or 1024
- Support dedicated CRE/P-MODE

Timing features:

Common timing features:

- Read to read turn around: no turn around, 1-cycle, …, 7-cycle
- Read to write turn around: no turn around, 1-cycle, …, 7-cycle
- Write to read turn around: no turn around, 1-cycle, …, 7-cycle
- Write to write turn around: no turn around, 1-cycle, …, 7-cycle

Each CS timing features:

- Asynchronous single read time or CE# width: 1-cycle, …, 31-cycle
- Asynchronous page read first delay time: 1-cycle, …, 31-cycle
- Asynchronous page read next delay time: 1-cycle, …, 15-cycle
- Synchronous burst read first delay time: 1-cycle, …, 31-cycle
- Synchronous burst read next delay time: 1-cycle, …, 15-cycle
- Asynchronous single write time or CE# width: 1-cycle, …, 31-cycle
- Synchronous burst write first delay time: 1-cycle, …, 31-cycle
- Synchronous burst write next delay time: 1-cycle, …, 15-cycle
- ADM: access start to address/data switch point delay time: 0-cycle, 1-cycle, 2-cycle, 3-cycle
- Access start to OE# low delay time: 0-cycle, 1-cycle, …, 7-cycle
- Access start to WE# low delay time: 0-cycle, 1-cycle, …, 7-cycle
- WE# width: 0-cycle, 1-cycle, …, 15-cycle
- Access start to CE# low delay time: 0-cycle, 1-cycle
- ADV# width: 0-cycle, 1-cycle, 2-cycle, 3-cycle

5.5.3 Signal descriptions

Table 5.5-1 SMC signal description

PAD name	Direction	Description	Note
SMRSTN	output	Reset	Only for Flash
SMCLK	output	CLK	
SMCLKN	output	CLK#	Only for DDR
SMCEN [3:0]	output	CE#	
SMADVN	output	ADV#	
SMOEN	output	OE#	
SMWEN	output	WE#	
SMLBN	output	LB#	
SMUBN	output	UB#	
SMCRE	output	CRE	
SMA [24:16]	output	ADP: High bits of address ADM: High bits of address AADM: not used	
SMA [15:0]	output	ADP: low 16 bits of address ADM: not used AADM: not used	
SMD [15:0]	inout	ADP: 16 bits of data ADM: low 16 bits of address and 16 bits of data	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

		AADM: all bits of address and 16 bits of data	
SMDQS[1:0]	inout	DQS	Only for DDR
SMWAIT	input	WAIT	
SMSMP	inout	Dummy PAD for sample clock loop	Internal used

5.5.1 Function Description

5.5.1.1 Block Diagram

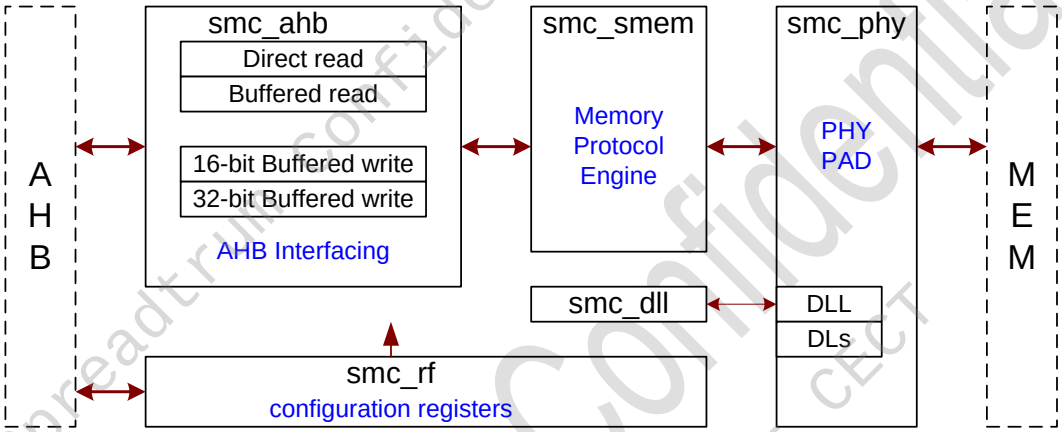


Figure 5-7 SMC block diagram

SMC mainly have five parts:

- smc_ahb is used to interface with AHB.
- smc_smem is used to generate external memory bus sequence.
- smc_dll is used to compensate delay line by DLL.
- smc_rf is configuration registers.
- smc_phy is used to physical PHY interfacing with external memory.

5.5.1.2 Operation Descriptions

5.5.1.2.1 Power Control

All external memory bus PADs and all external memories should be in VDDMEM power domain.

After power-up, VDDMEM is opened automatically. Nor-Flash needs reset, and pSRAM is at asynchronous single mode.

During sleep, VDDMEM should keep opened.

5.5.1.2.2 PAD Driving Strength

The driving strength of external memory bus PADs may be adjusted by different chips because of different supply voltage, SI, impact on RF, timing, etc. Normally, bigger driving strength leads to more impact on RF, but smaller driving strength leads to slower PAD speed. Another issue is SI, that is, driving strength should match loading as possible.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.5.1.2.3 Sleep Management and Power Management

pSRAM has internal refresh engine, so SMC doesn't have to issue special commands to make external memory sleep or wakeup. But SMC still need guarantee last burst completed.

SMC provides a hardware engine to make sleep safely for pSRAM. When system want to enter sleep mode, a hardware request signal is issued from system, and then SMC completes the current burst and holds next bursts. At last, SMC responses ready signal to system to indication SMC is ready for sleeping.

Another issue is from DLL, which must be restarted after wakeup. SMC provides an automatic engine to complete this restarting process, and this hardware process doesn't need taken care of by software.

5.5.1.2.4 SMC-Related in Booting

Boot sequence isn't discussed in this document, and only some issues are mentioned here.

- ADP and ADM should be selected in boot sequence.
- Memory PAD driving strength should be configured
- If on-chip RAM is not enough for boot, external SRAM is used, and chip select assignment for CS0 and CS1 is fixed.
- For ADP, except that rf_admux_en must be cleared, default value of SMC work, but it is not efficient, so software should re-configure SMC as soon as possible.
- For ADM, except that rf_admux_en must be set, default value of SMC work, but it is not efficient, so software should re-configure SMC as soon as possible.
- For AADM, default configuration doesn't work, and the whole SMC should be configured in AADM mode.

5.5.1.2.5 Reset Control

There a reset output in VDDMEM power domain – SMRSTN for Nor-Flash.

- SMRSTN (Active Low)

This PAD is connected with internal core reset signal. After power-up, this PAD issues a low-active reset. The reset width is more than 100ms.

5.5.1.2.6 Configuration Register

Both Nor-Flash and pSRAM have internal configuration registers needing configuring.

Software configures Nor-Flash by pure software command method, so it isn't described here.

For pSRAM, normally there are two methods – CRE-controlled and software-method. And there is another special mode for AADM, some AADM devices support the method that CRE signal is issued on a high-bit of data bus in first address phase instead of separate CRE input.

- CRE-controlled:

By this method, SMCRE PAD is used to distinguish configuration registers accessing from normal accessing. During accessing period, if CRE is active, configuration registers are accessed; otherwise, normal memory space is accessed.

When software configures device, which is in asynchronous mode, SMC should be in asynchronous single mode, that is, rf_mode_r and rf_mode_w are 0. When device is in synchronous mode at that time, SMC should be in synchronous single mode, that is, rf_mode_r and rf_mode_w are 2.

rf_cre_en is used to enable CRE active during accessing on this chip select.

rf_cre_pol is used to indicate CRE polarity. Normally, this bit should be cleared, that is, active high.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

rf_cre_mode is used to select CRE operation mode:
0: auto-controlled CRE: CRE is issued automatically together with CS active if rf_cre_en is set.
1: force-controlled CRE: CRE is controlled directly by rf_cre_en just as a GPIO.
rf_cre_mode is recommended to be cleared.

The following is timing diagram on CRE-controlled method.

ADP Asynchronous Write

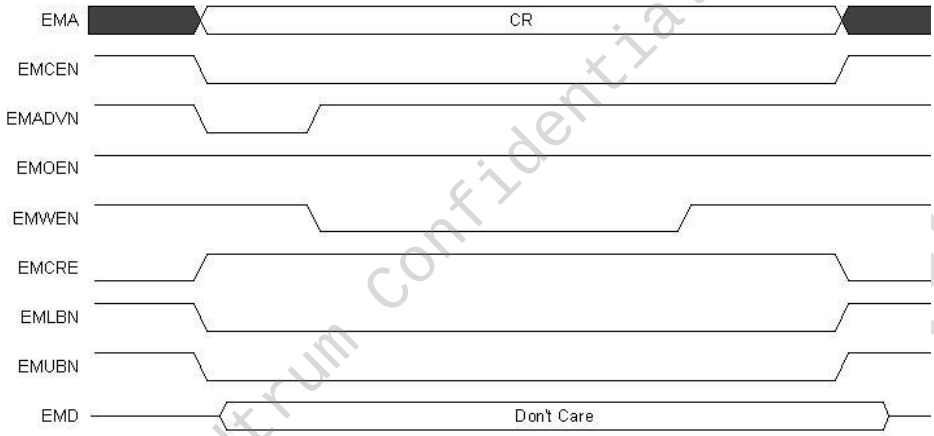


Figure 5-8 ADP asynchronous write CR command

ADP Synchronous Write

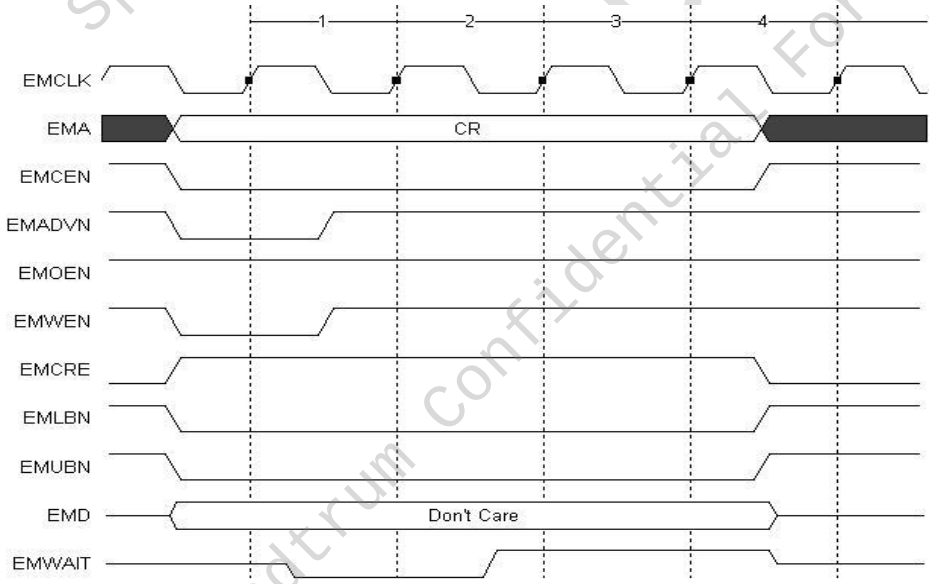


Figure 5-9 ADP synchronous write CR command

Note: First latency is three; WAIT active low; WAIT asserted one cycle before data;

ADM Asynchronous Write

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

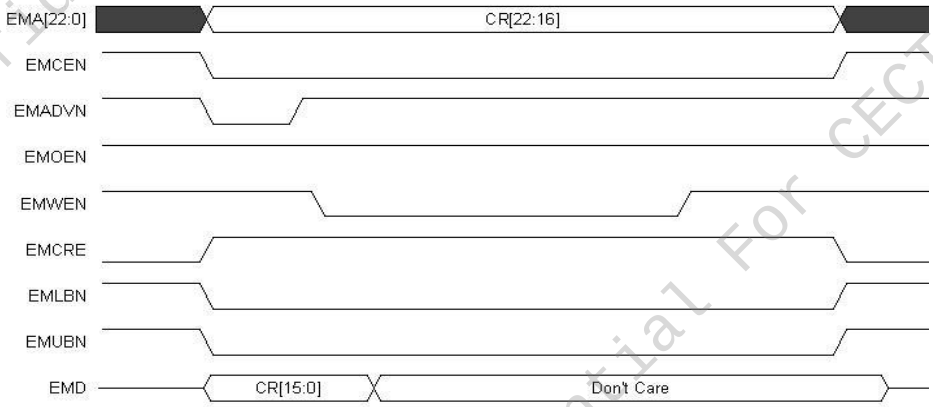


Figure 5-10 ADM asynchronous write CR command

ADM Synchronous Write

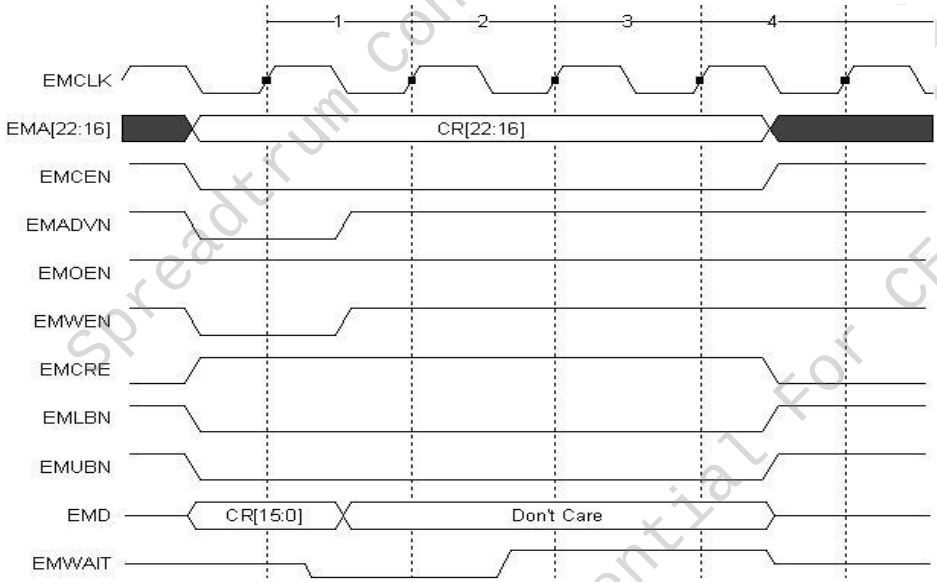
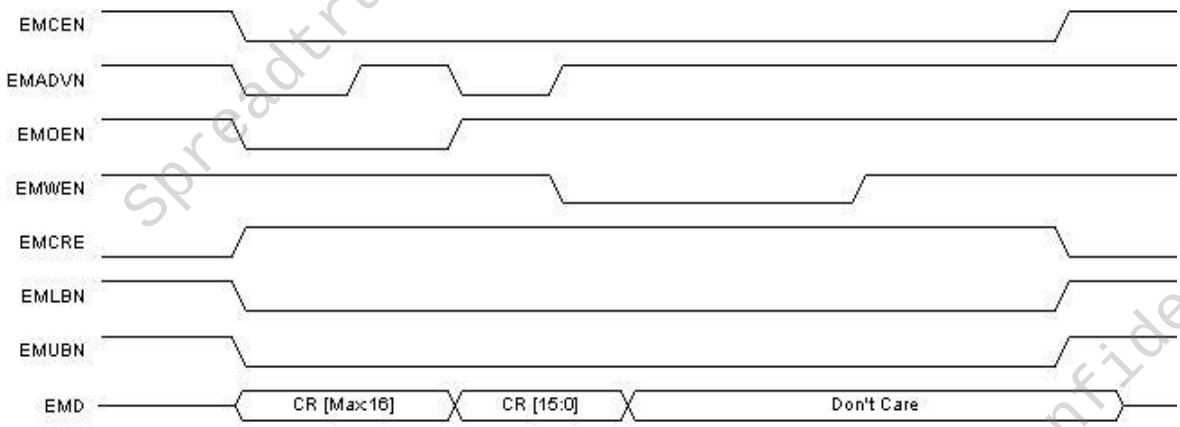


Figure 5-11 ADM synchronous write CR command

Note: First latency is three; WAIT active low; WAIT asserted one cycle before data;

AADM Asynchronous Write



This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Figure 5-12 AADM asynchronous write CR command

AADM Synchronous Write

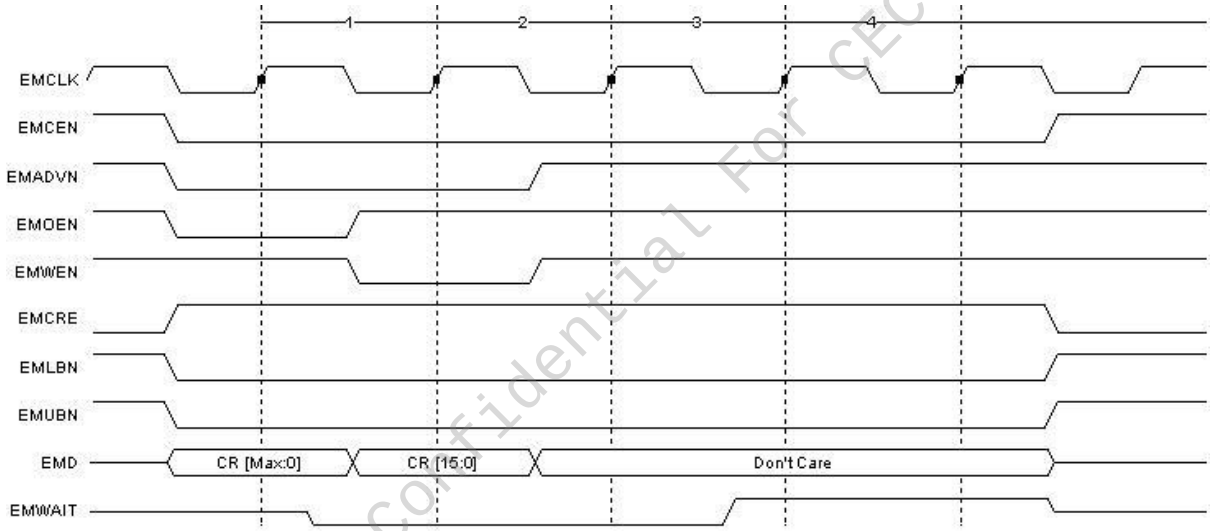


Figure 5-13 AADM synchronous write CR command

Note: First latency is three; WAIT active low; WAIT asserted one cycle before data;

Software-Method:

Asynchronous single mode should be used, and software follows a special sequence to access configuration register. The special sequence can be achieved from device data sheet. There is no special timing requirement for this method.

Address-controlled for AADM:

There is a special method for some AADM devices. CRE signal is issued on a high-bit of data bus in first address phase instead of separate CRE input.

In first address phase, some of high bits are unused because of memory size limitation, so these bits can be used to transform information like CRE, which makes hardware CRE pin saved.

SMC provides these unused high-bit in first address phase configurable, so user can use these configurable registers to mark CRE writing.

The other configurations are the same as generic operations.

ADP/ADM/AADM Asynchronous Single Mode

Asynchronous single mode is basic mode for all external memories. After reset or power-up, Either Nor-Flash or pSRAM is in this mode.

To ADP device, ADV# can be used to latch address, or ADV# is kept during whole accessing period. The address should be checked setup time and hold time to the rising edge of ADV#.

To ADM device, ADV# MUST be used. The behavior is the same as ADP ADV# used.

To AADM device, ADV# MUST be used, and will be active twice. The first ADV# active is used to latch Address [Max:16], and OE# should also be active during the first address latching. The second ADV# active is used to latch Address [15:0], and OE# should be de-active. It's important that OE# should be checked setup time and hold time to the rising edge of ADV# together with address.

To read operations, OE# MUST have a setup time from CE# low for ADM and AADM device to avoid bus conflicting. But for ADP device, OE# can be kept active during the whole accessing period.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

To write operations, data is sampled by WE# rising edge, so WE# high hold time to CE# high should be guarantee. For some devices, WE# low needs setup time from CE# low.

The following is timing diagrams.

ADP Read without ADV#-Used

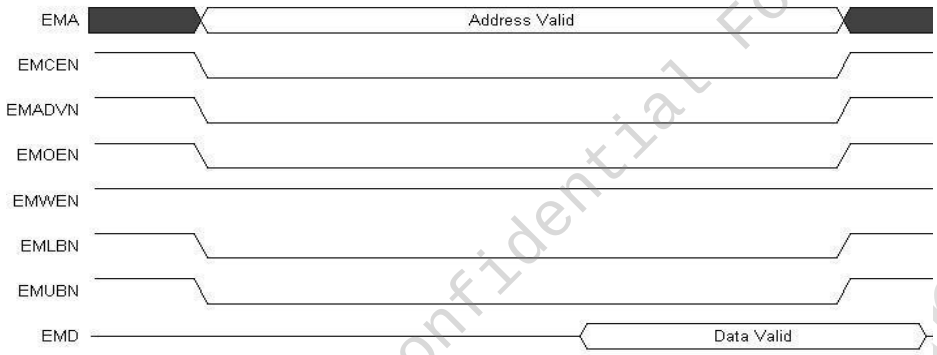


Figure 5-14 ADP asynchronous read without ADV#-used command

ADP Read with ADV#-Used

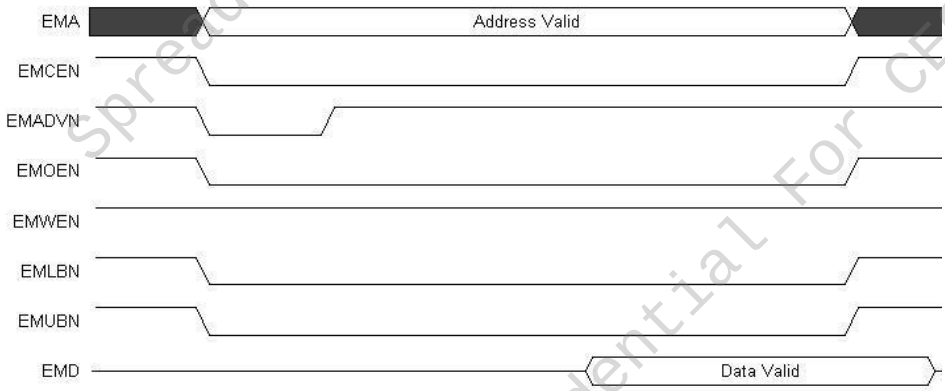


Figure 5-15 ADP asynchronous read with ADV#-used command

ADM Read

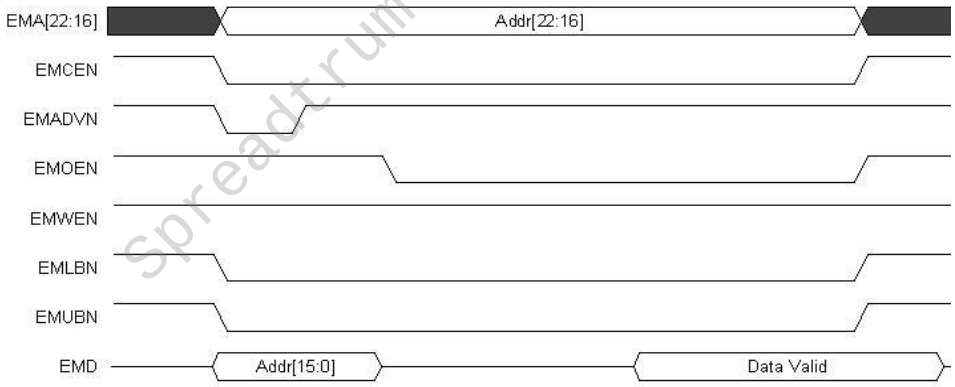


Figure 5-16 ADM asynchronous read command

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

AADM Read

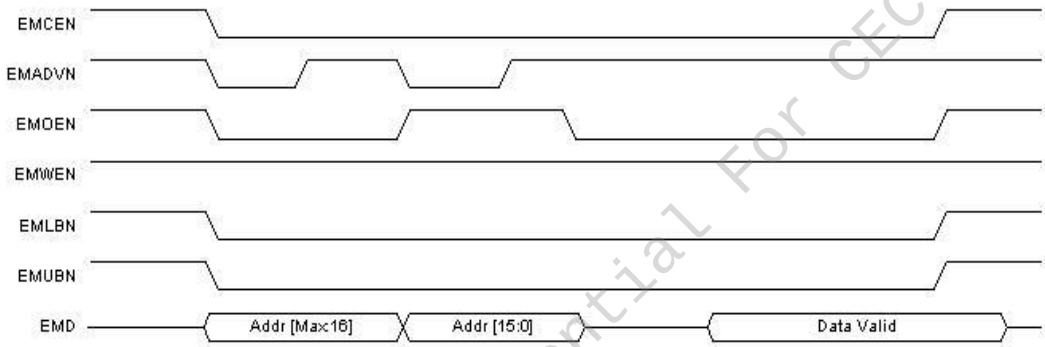


Figure 5-17 AADM asynchronous read command

ADP Write without ADV#-Used

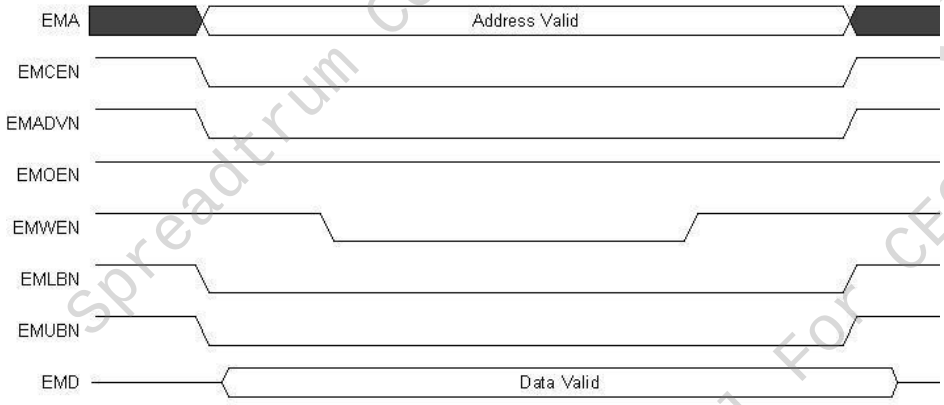


Figure 5-18 ADP asynchronous write without ADV#-used command

ADP Write with ADV#-Used

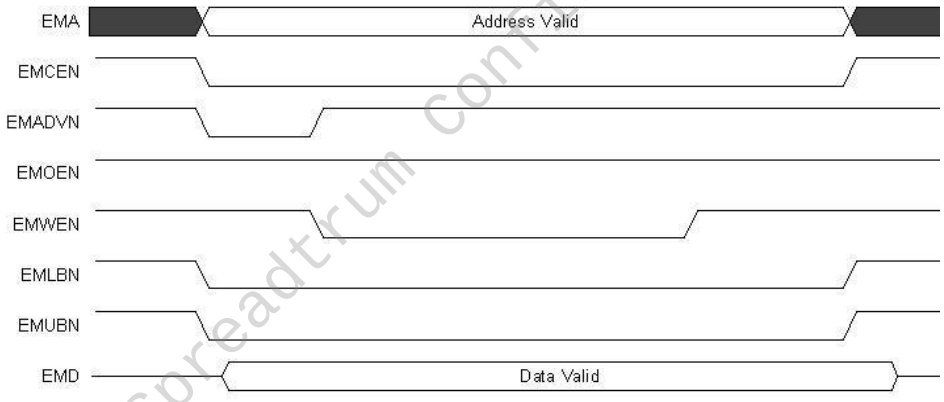


Figure 5-19 ADP asynchronous write with ADV#-used command

ADM Write

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

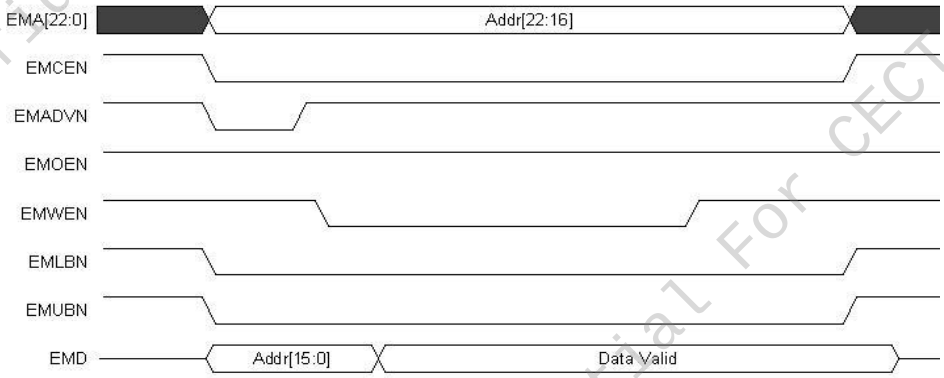


Figure 5-20 ADM asynchronous write command

AADM Write

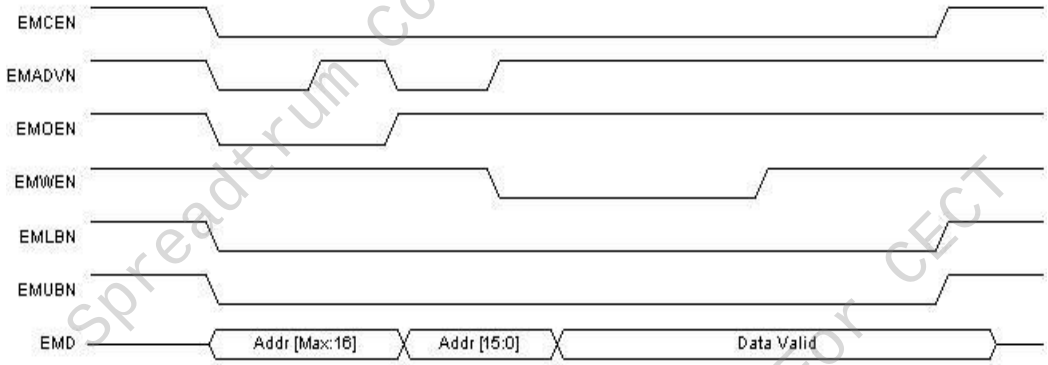


Figure 5-21 AADM asynchronous write command

ADP Asynchronous Page Mode

It's IMPORTANT that page mode is supported only on ADP devices.

Page mode also is an asynchronous mode, so output clock should be closed. And in page mode, write operations is the same as single mode, so only read operation is described here.

rf_t_adv_mode_r MUST be set to 1 to keep ADV# low during whole accessing CE# low period.

rf_burst_mode_r MUST be cleared to 0 to make SMC check page boundary.

rf_burst_length_r should be configured by device page size, which is from device data sheet.

ADP Read

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

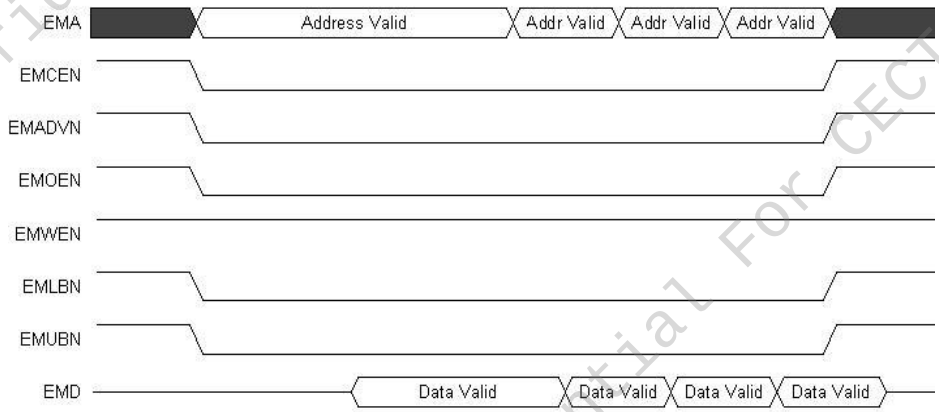


Figure 5-22 ADP page read command

ADP/ADM/AADM Synchronous Burst Mode - SDR

SMC completes synchronous burst mode by two methods – WAIT-used and WAIT-not-used. WAIT-used method means SMC uses WAIT input to sample input data and transmit output data. WAIT-not-used method means SMC uses internal counter to sample input data and transmit output data.

For ADM and AADM devices, OE# MUST have a setup time from CE# low to avoid bus conflicting.

WAIT-Used Method (Recommended)

WAIT is used at indicate first latency and row boundary. So by this method, row boundary detect function can be disabled and read/write first/next time DON'T care. And also, variable first latency can be supported. This method is more efficient than WAIT-not-used. But there is a limitation that device MUST support WAIT one cycle before data mode.

WAIT-Not-Used Method

Device MUST be configured as fixed first latency. Read/write first/next time should be used to count delay time, and they are configured by device first latency. Row detect function also is opened to guarantee bursts can be terminated on row boundary. If Nor-Flash is configured as INCR burst read mode, SMC has to break bursts at Nor burst boundary because of wait time inserted at this boundary. In order to make SMC do this breaking, SMC should be configured to wrap mode, and wrap length is equal to Nor burst length, which is from Nor data sheet.

For AADM device, there are two methods for address loading among different vendors. One is two cycle method, and the other is three cycle method.

Two cycle method means address [max:16] is loaded in first cycle with OE# low and address [15:0] is loaded in second cycle with OE# high.

Three cycle method means address [max:16] is loaded in first cycle with OE# low and address [15:0] is loaded in third cycle with OE# high. The second cycle is idle.

ADP Read

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

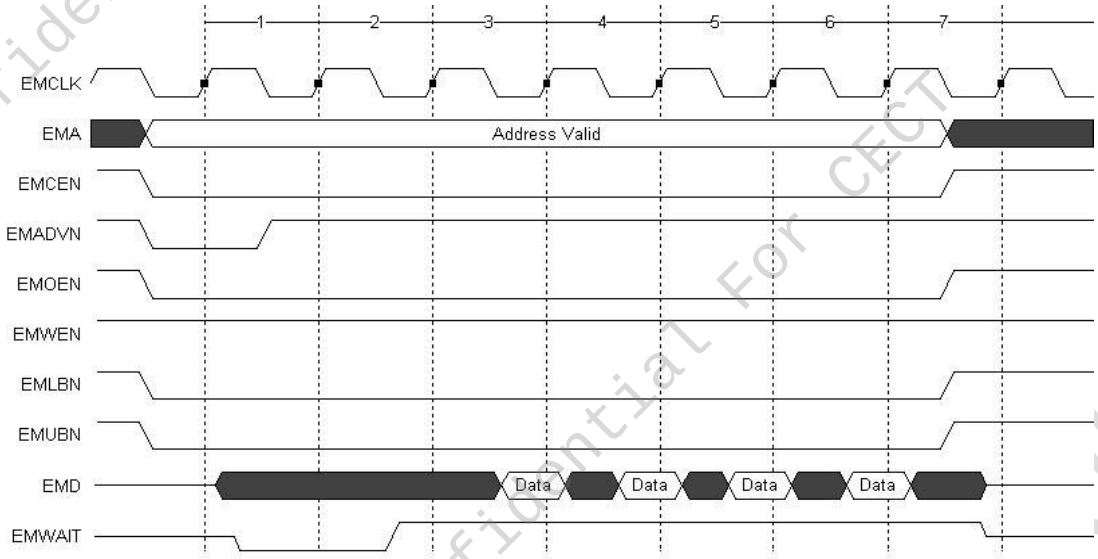


Figure 5-23 ADP SDR burst read command

Note: First latency is three; WAIT active low; WAIT asserted one cycle before data;

ADM Read

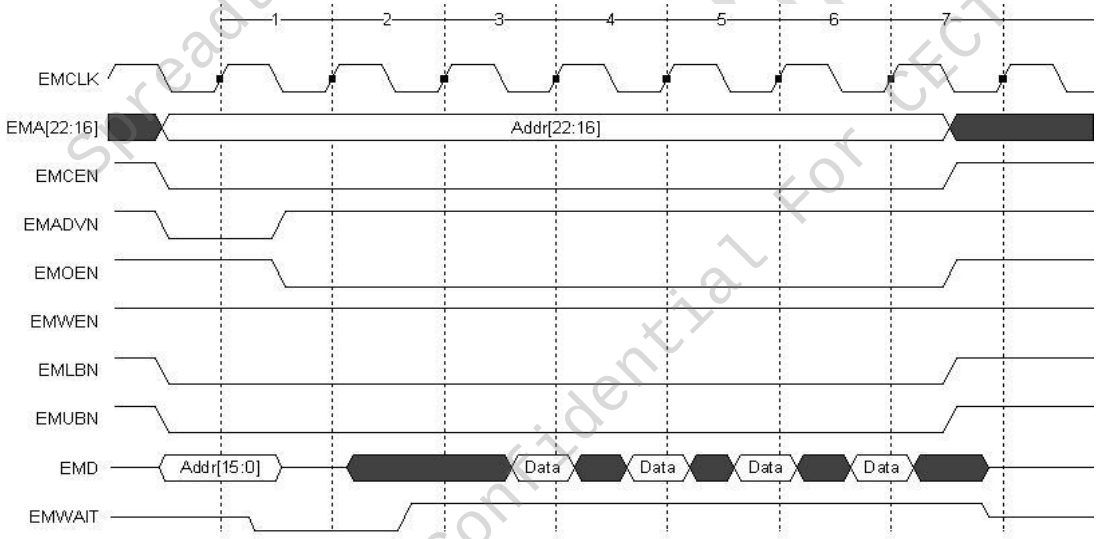


Figure 5-24 ADM SDR burst read command

Note: First latency is three; WAIT active low; WAIT asserted one cycle before data;

AADM Read

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

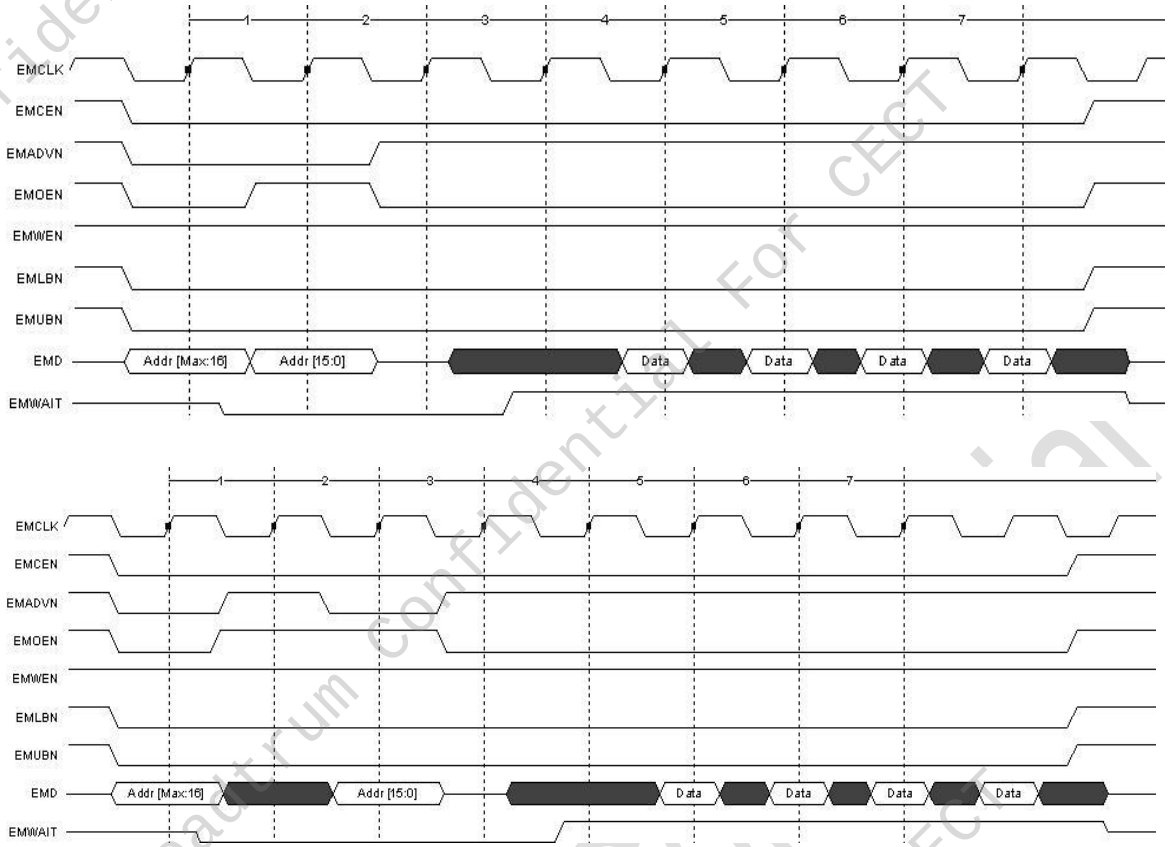


Figure 5-25 AADM SDR burst read command

Note1: First latency is three; WAIT active low; WAIT asserted one cycle before data;

Note2: the first figure is for two cycle address loading, and the second figure is for three cycle address loading.

ADP Write

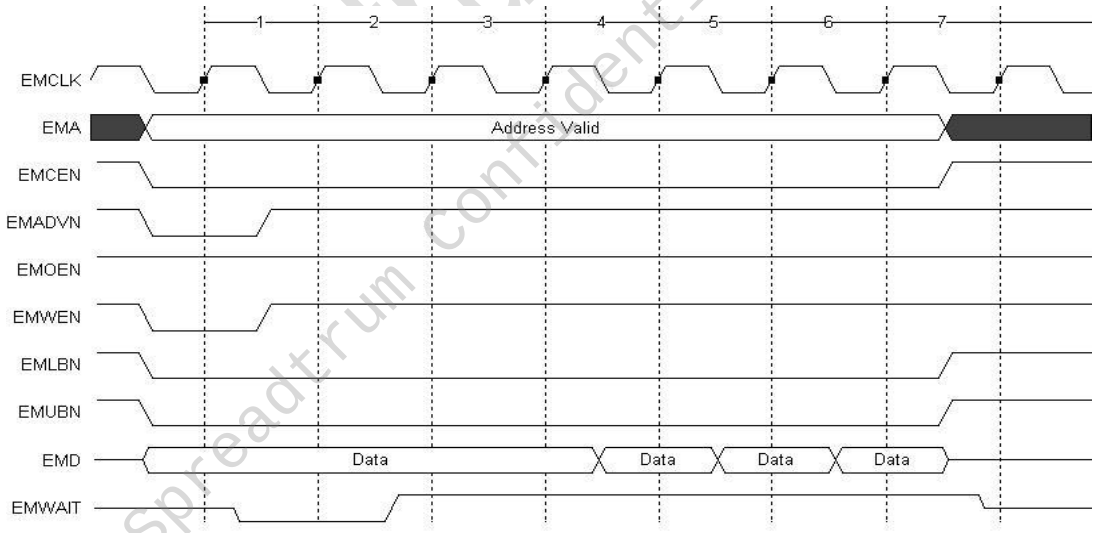


Figure 5-26 ADP SDR burst write command

Note: First latency is three; WAIT active low; WAIT asserted one cycle before data;

ADM Write

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

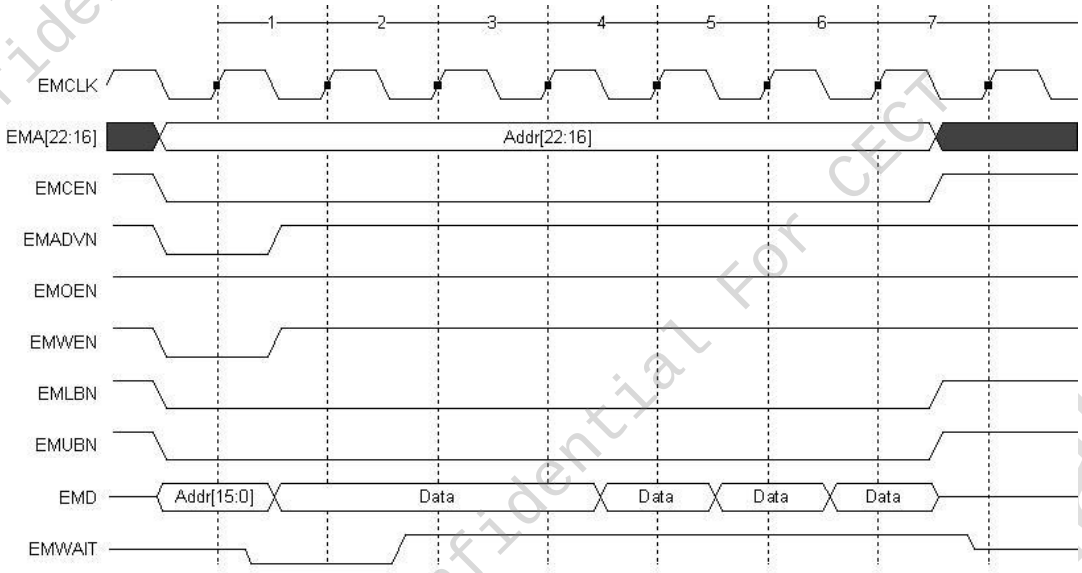


Figure 5-27 ADM SDR burst write command

Note: First latency is three; WAIT active low; WAIT asserted one cycle before data;

AADM Write

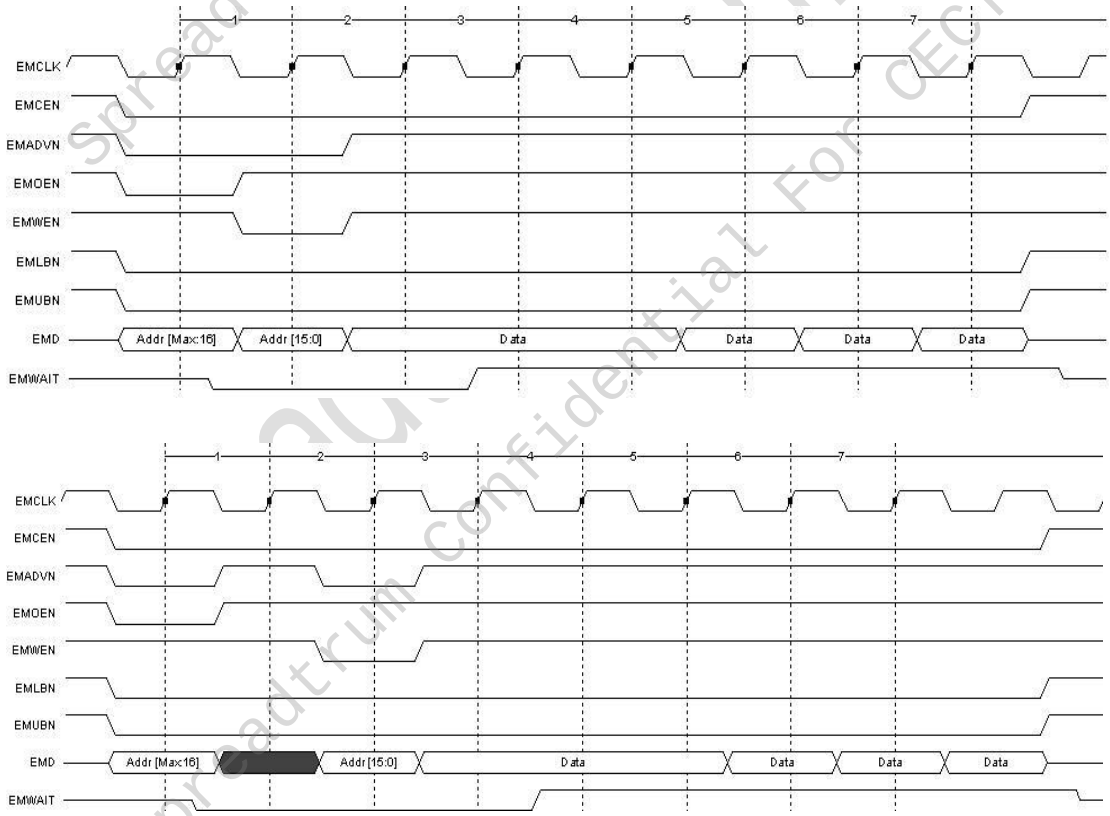


Figure 5-28 AADM SDR burst write command

Note1: First latency is three; WAIT active low; WAIT asserted one cycle before data;

Note2: the first figure is for two cycle address loading, and the second figure is for three cycle address loading.

ADP/ADM/AADM Synchronous Burst Mode - DDR

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

pSRAM DDR mode is not a standard, and there are different protocols among different vendors. So user should check the detailed documents before choosing a new vendor. Basically, there are three more signals added in DDR mode – CLK#, DQS0 and DQS1. The pSRAM DDR mode seems like mixed standard of JEDEC DDR and CellularRAM. The CLK and CLK# are one differential pair, and DQS0 and DQS1 are used for data sampling.

For DDR mode, SMC can be configured as WAIT used or WAIT not used, same as SDR mode. And also, there are two independent select bits for reading and writing transactions.

From current DDR pSRAM spec, read latency can be variable or fixed, but write latency is always fixed. Even if device is configured in variable latency mode, the write latency is fixed. So there is two recommended options for WAIT, one is WAIT used for both read and write, and the other is WAIT used for read and WAIT not used for write.

IMPORTANT: There is no standard for DDR pSRAM, so the device behavior may be different among different vendors, especially WAIT behavior. So it's very important to check the behavior and timing parameter in data sheet for each pSRAM.

ADP Read

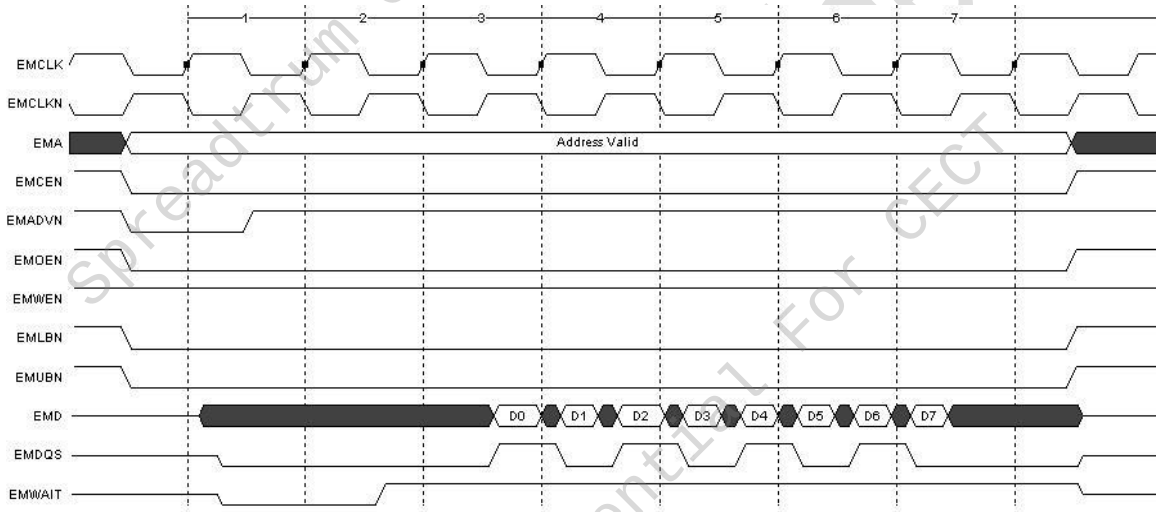


Figure 5-29 ADP DDR burst read command

Note1: First latency is three; WAIT active low; WAIT asserted one cycle before data;

ADM Read

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

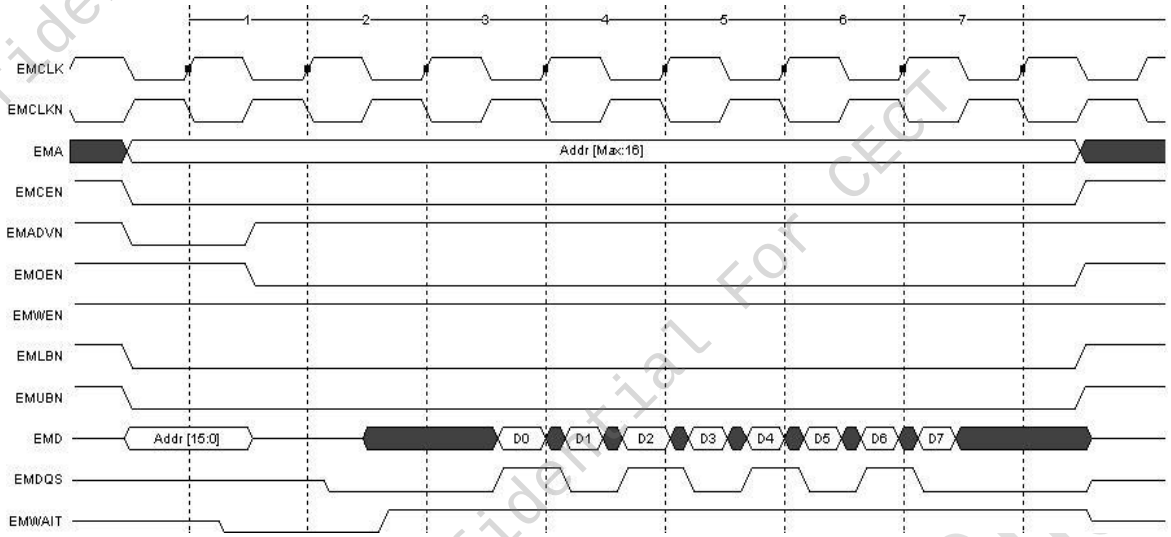


Figure 5-30 ADM DDR burst read command

Note1: First latency is three; WAIT active low; WAIT asserted one cycle before data;

AADM Read

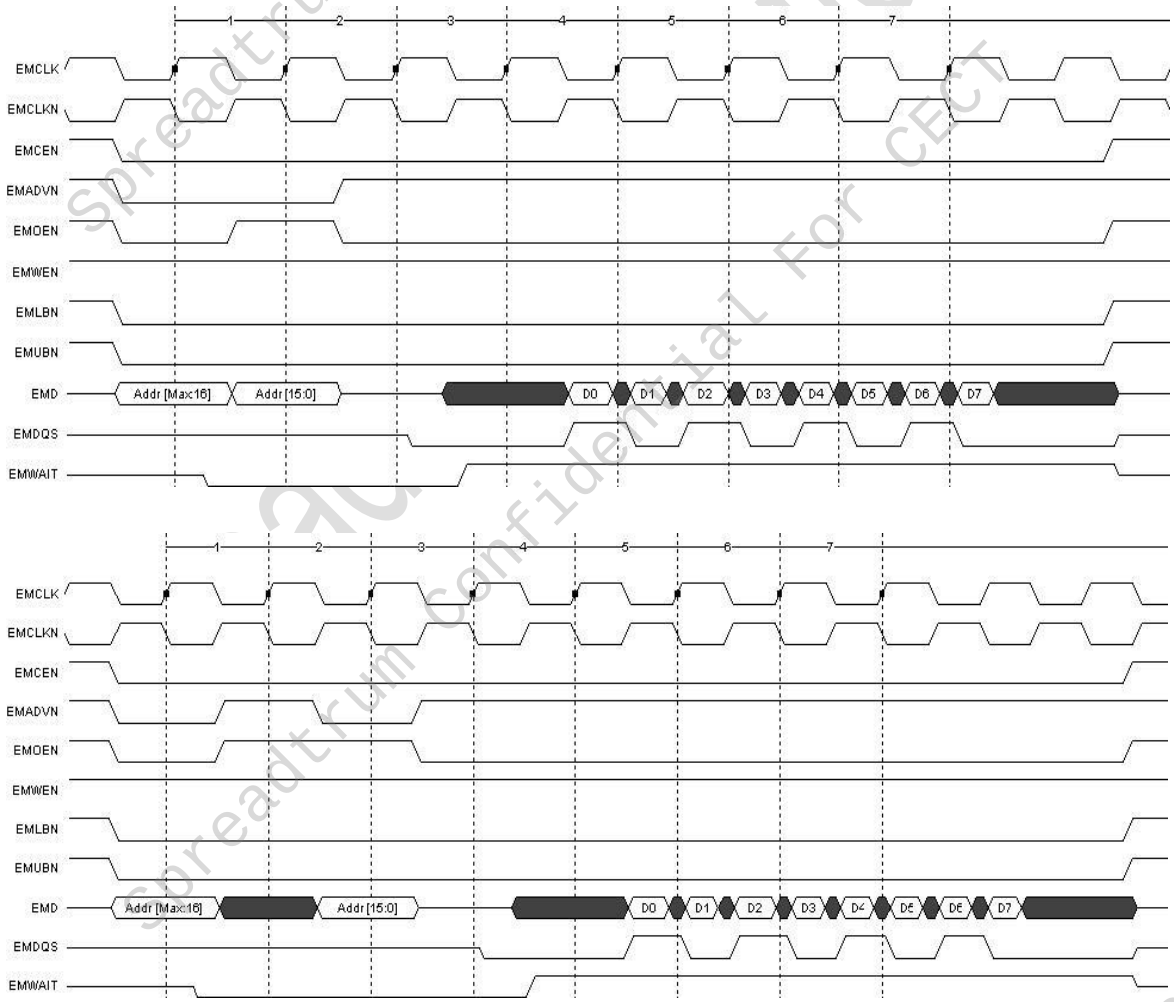


Figure 5-31 AADM DDR burst read command

Note1: First latency is three; WAIT active low; WAIT asserted one cycle before data;

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Note2: the first figure is for two cycle address loading, and the second figure is for three cycle address loading.

ADP Write

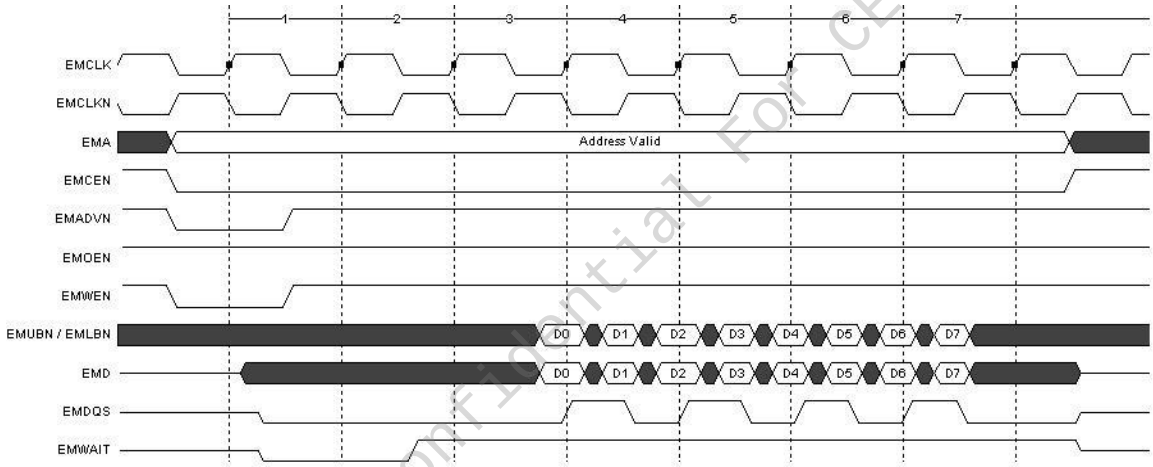


Figure 5-32 ADP DDR burst write command

Note1: First latency is three; WAIT active low; WAIT asserted one cycle before data;

Note2: The WAIT sequence in above figure is an example, not the exact behavior for pSRAM because of different behavior among different vendors.

ADM Write

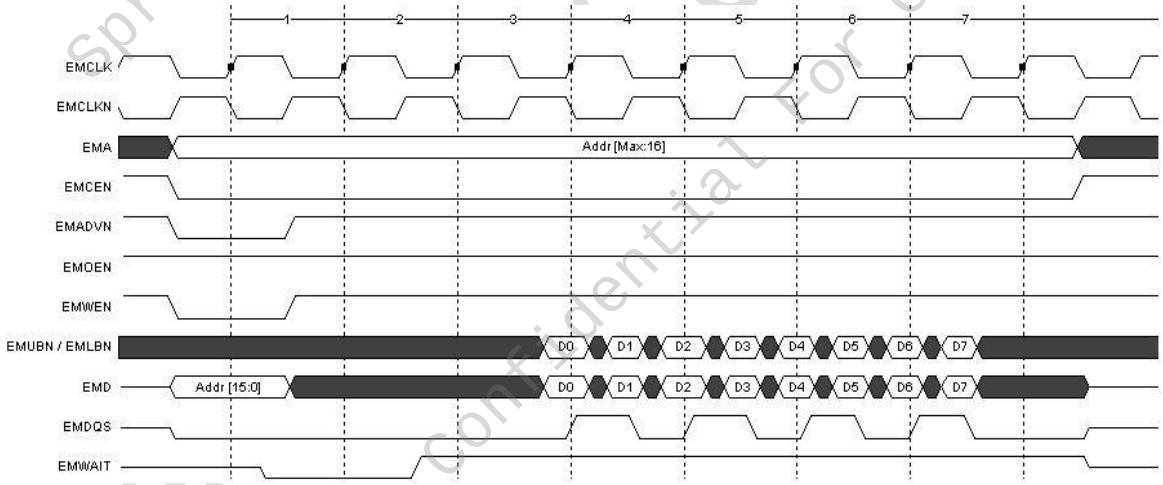


Figure 5-33 ADM DDR burst write command

Note1: First latency is three; WAIT active low; WAIT asserted one cycle before data;

Note2: The WAIT sequence in above figure is an example, not the exact behavior for pSRAM because of different behavior among different vendors.

AADM Write

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

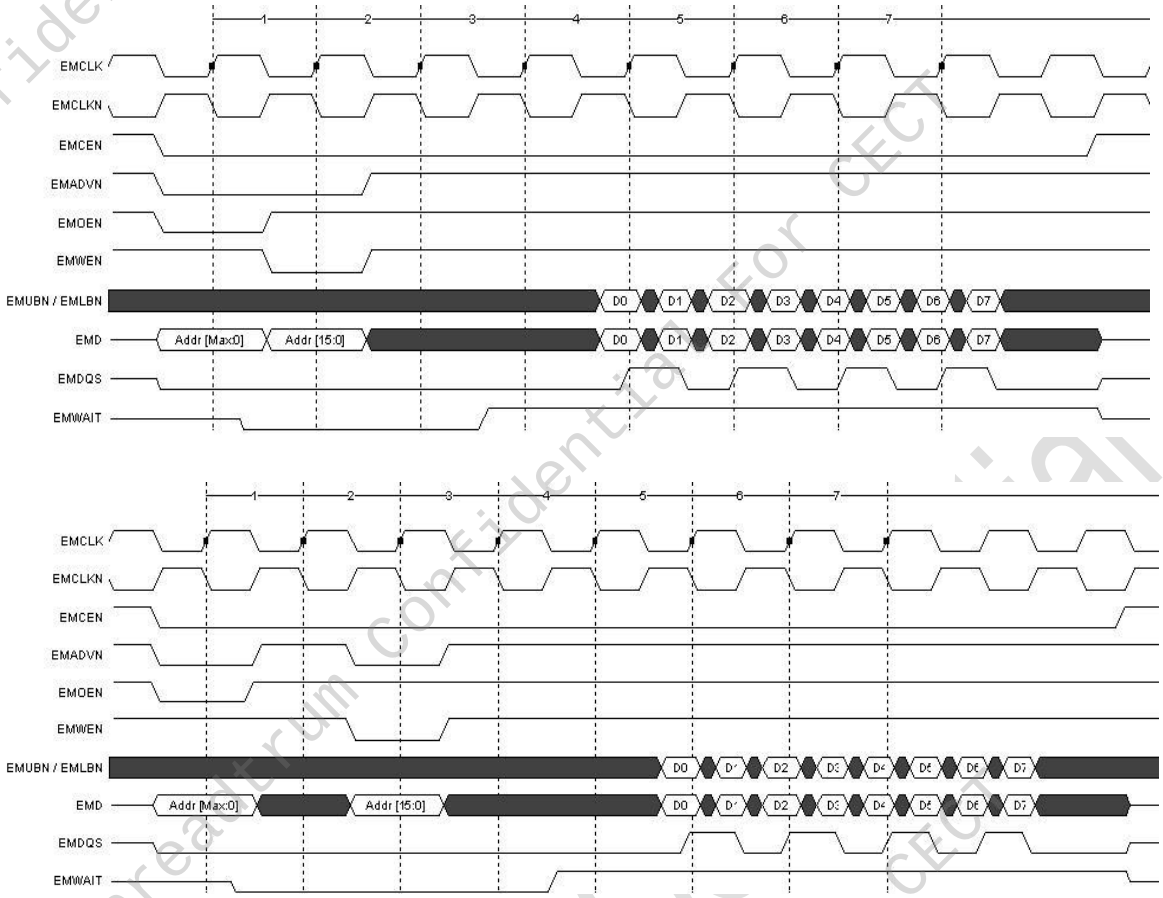


Figure 5-34 AADM DDR burst write command

Note1: First latency is three; WAIT active low; WAIT asserted one cycle before data;

Note2: The WAIT sequence in above figure is an example, not the exact behavior for pSRAM because of different behavior among different vendors.

Note3: the first figure is for two cycle address loading, and the second figure is for three cycle address loading.

ADP/ADM/AADM Nor-Flash Mode or Special pSRAM Mixed Mode

This mode means synchronous burst read and asynchronous single write. According to device requirements, there are two method to complete accessing in this mode.

Some devices don't care about clock during write operations, so SMC can use CLK-run method. These devices include most of Nor-Flash. And another devices require clock MUST be stable during write operations, so SMC has to use CLK-gate method. These device include some of pSRAM.

Because burst mode is used on pSRAM instead of mixed mode in normal condition, so this specification mainly describes CLK-run mode in the following chapters.

CLK-Run mode

Output clock should be opened. Read operations should be configured as burst mode, and the configuration method is the same as burst mode. Write operations should be configured as single mode, and the configuration method is the same as single mode.

CLK-Gate mdoe

rf_clk_out_mode and rf_clk_out_dly should be used to control how to gate output clock.

ADP Read and Write with CLK-Run

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

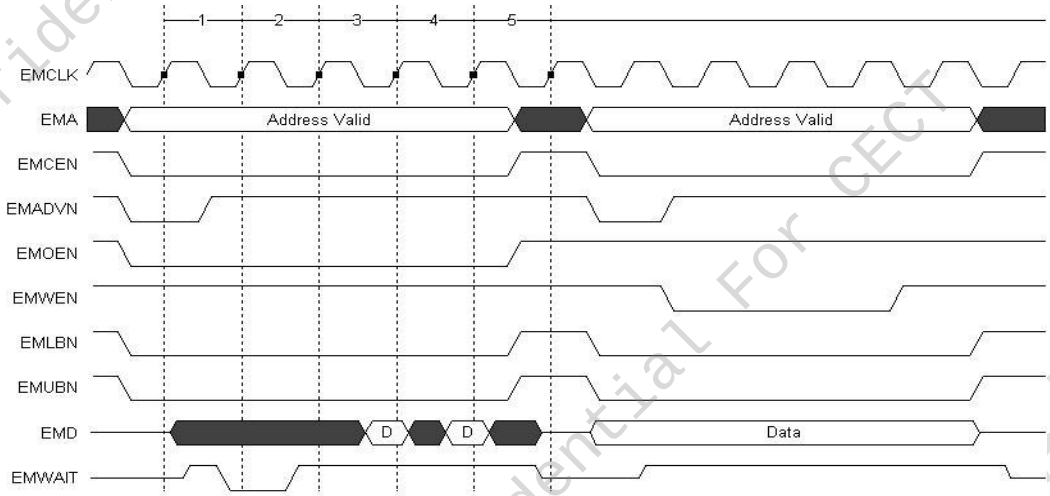


Figure 5-35 ADP read and write with clock-run

Note: First latency is three; WAIT active low; WAIT asserted one cycle before data;

ADM Read and Write with CLK-Run

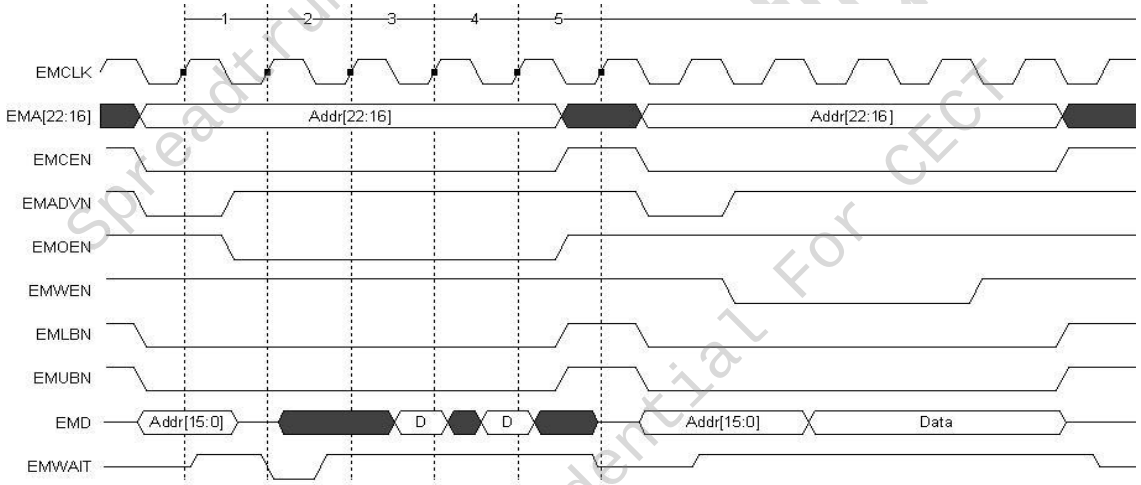


Figure 5-36 ADM read and write with clock-run

Note: First latency is three; WAIT active low; WAIT asserted one cycle before data;

AADM Read and Write with CLK-Run

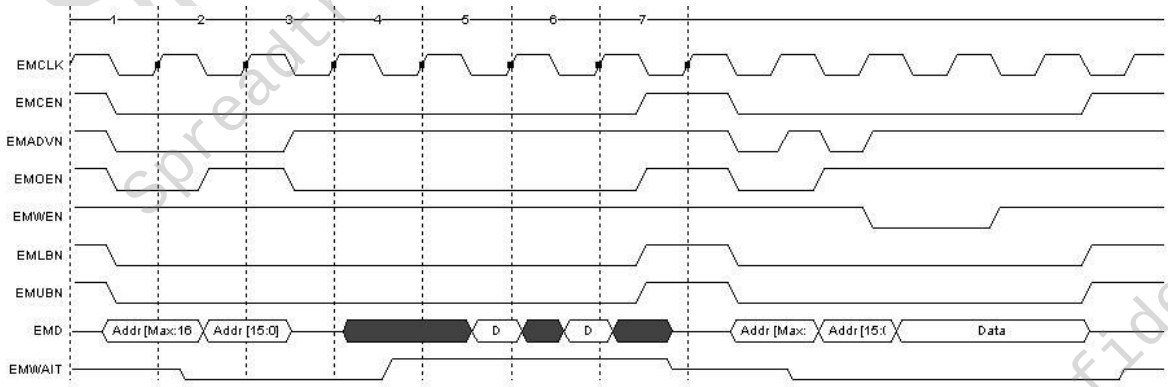


Figure 5-37 AADM read and write with clock-run

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Note: First latency is three; WAIT active low; WAIT asserted one cycle before data;

ADP Read and Write with CLK-Gate

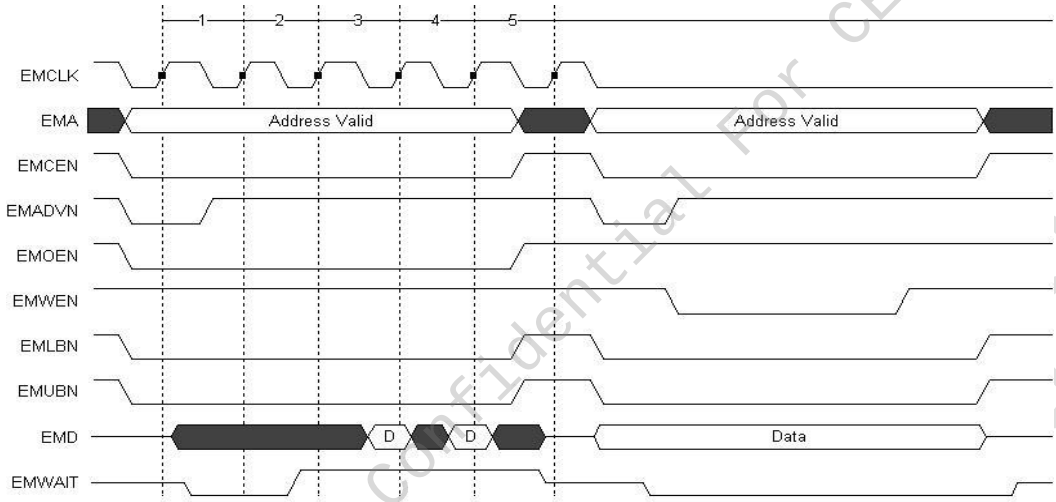


Figure 5-38 ADP read and write with clock-gate

Note: First latency is three; WAIT active low; WAIT asserted one cycle before data;

ADM Read and Write with CLK-Gate

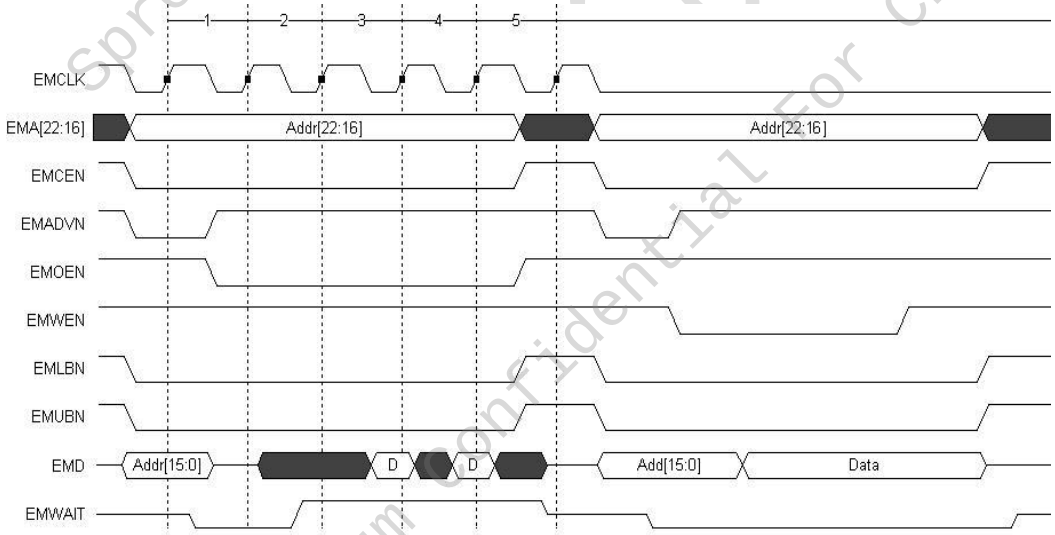


Figure 5-39 ADM read and write with clock-gate

Note: First latency is three; WAIT active low; WAIT asserted one cycle before data;

AADM Read and Write with CLK-Gate

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

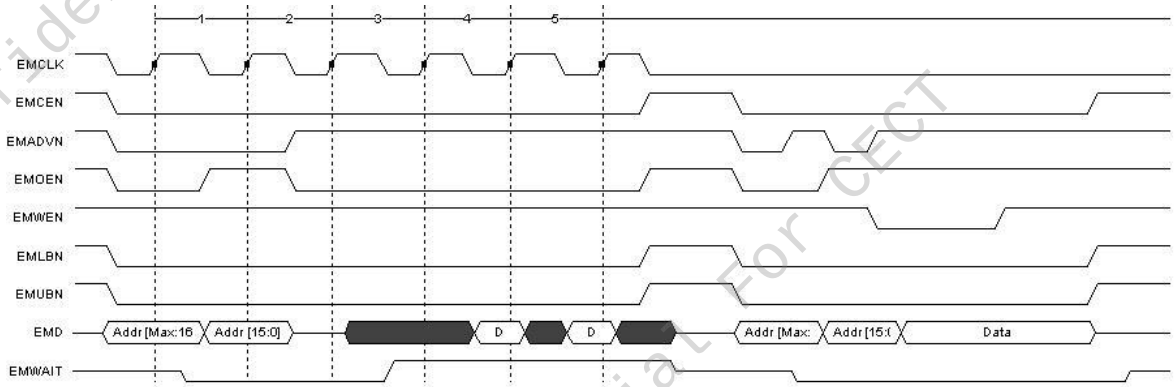


Figure 5-40 AADM read and write with clock-gate

Note: First latency is three; WAIT active low; WAIT asserted one cycle before data;

ADP ADM and AADM

Generally, SMC should be configured as ADP mode when ADP device is connected and as ADM when ADM device is connected.

But SMC also provides other connection methods.

The important one is that SMC is configured as ADM, and device can be connected with either ADP or ADM, only if device supports ADV# input. For ADP device, low 16-bit address should be connected with data bus. That means, if device supports ADV#, 16 PADs can be saved for cost-down.

Another method is that SMC is configured as ADM, and device can be connected with either ADP or ADM. There is no ADV# requirement, but low 16-bit address of device should be connected with SMC address low bits. So no PAD can be saved.

ADM has the same performance as ADP, so ADM is better choice in normal cases to save pins. AADM saves more pins than ADM, but there are one or two cycles increased for first latency. So normally AADM can be used to share bus with 16-bit NAND.

DDR Write Burst Internal Behavior

SMC provides two modes for DDR write burst selected by rf_ddr_wdata_mode. If this bit is cleared to 0, WAIT may be used or not used, but there is a critical timing path from HCLK to HCLK_2x. If this bit is set to 1, there is not timing issue, but WAIT must not be used.

To two modes, most configurations are the same, except the following things.

1. If rf_ddr_wdata_mode is 0, WAIT for write may be used or not used. But if this bit is 1, WAIT for write must not be used.

2. If rf_ddr_wdata_mode is 0, rf_ddr_wdata_dly is 1. If this bit is 1, rf_ddr_wdata_dly is 2.

3. If rf_ddr_wdata_mode is 0, rf_t_first_w should be N for N cycle latency. If this bit is 1, rf_t_first_w is N – 1.

WAIT Operation

WAIT is used to indicate data valid for reading or data request for writing.

During first latency, variable latency configured, WAIT performs an arbitration role when an accessing is issued while an on-chip refresh is in progress. If a collision occurs, WAIT is asserted for additional clock cycles until the refresh has completed.

WAIT is also asserted when a burst crosses a row boundary. The WAIT assertion allows time for the new row to be accessed, and permits any pending refresh operations to be performed.

For Nor Flash, unlike pSRAM, wait time is asserted not only at row boundary, but also at burst boundary, to allows time for following accessing.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

It's important that there are some devices with WAIT don't support row boundary crossing. So SMC row boundary detect function should be opened to break burst at row boundary even if WAIT is used for variable latency.

If WAIT is not used, SMC has to use fixed latency to avoid uncertainty from refresh collision. But fixed latency adds additional clock cycles to all bursts to guarantee refresh times in some of these bursts, and this can lead to lower efficiency.

And if WAIT is not used, SMC has to open row boundary detect function to guarantee all bursts crossing row boundary are broken. This also has small impact on efficiency.

If Nor-Flash is configured as INCR burst read mode, SMC has to break bursts at Nor burst boundary just like row boundary. In order to make SMC do this breaking, SMC should be configured to wrap mode, and wrap length is equal to Nor burst length, which is from Nor data sheet.

From above, it's better to use WAIT to gain higher efficiency except the device cannot support WAIT asserted one cycle before data. And the cause of this limitation is from internal sample logic design.

The SMC supports two bits for WAIT used or not used selection. One bit is for reading and the other is for writing. Reading and writing bursts can be configured independently.

Although write can be variable mode or fixed mode in CellularRAM protocol, but all of current devices only support fixed latency for writing, even if devices are configured in variable mode, which makes reading in variable latency. So for writing bursts, WAIT is used only for row boundary crossing. An example is Aptic DDR pSRAM. The WAIT of Aptic DDR pSRAM is very difficult to be used for writing, so reading bursts are configured as WAIT used, but writing bursts are WAIT not used.

Most devices have configurable WAIT polarity, so it should make sure that SMC has the same WAIT polarity configuration as external device.

DQS Operation

Two DQS pins are needed in DDR mode.

For writing, DQS is controlled by SMC and goes low-Z together with CE# goes low.

For reading, DQS is controlled by device and goes low-Z tCQLZ after the first clock rising. So rf_t_sample_stp should be configured to mask the initial high-Z state.

Burst Control

SMC support two burst modes – wrap mode and increase mode (or no-wrap mode).

For wrap mode, burst length can be configured by 2, 4, 8, 16 and 32

For increase mode, burst length can be configured by 2, 4, 8, 16, 32 and continuous.

SMC is optimized for increase mode. For wrap mode, SMC just breaks bursts at device burst boundary simply. So it's recommended that burst mode is configured by increase mode and burst length is configured as continuous.

It's important that burst mode/length for read can be configured by different parameters with write.

Row Boundary Crossing

Row boundary issues occur at many devices. When a burst crosses a row boundary, wait states should be asserted to hold transfer for some cycles.

There are two methods to resolve this issue. One is to use WAIT, and the other is to break burst. SMC support both two methods.

If the second method is used, row length must be configured, and the row length value can be achieved from device data sheet. SMC support row length of 64, 128, 256, 512 and 1024.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Burst Boundary Crossing

For Nor Flash, unlike pSRAM, wait time is asserted not only at row boundary, but also at burst boundary, to allows time for following accessing.

So if Nor-Flash is configured as INCR burst read mode, and if WAIT is not used, SMC has to break bursts at Nor burst boundary just like row boundary. In order to make SMC do this breaking, SMC should be configured to wrap mode, and wrap length is equal to Nor burst length, which is from Nor data sheet. SMC support wrap burst length of 2, 4, 8, 16 and 32.

First Latency Control

There may be two modes of first latency when external devices are configured in burst mode – fixed latency or variable.

For Nor Flash, only fixed latency mode is used.

For pSRAM, both modes are supported and can be configured through SMC by software.

Fixed First Latency in burst mode

In this mode, first latency is fixed, and WAIT may not be used. But this latency MUST guarantee access cycle and refresh cycle even if there isn't refresh collision in this burst, which lead to lower efficiency.

Variable First Latency in burst mode

In this mode, first latency is variable, and WAIT must be used. When refresh collision occurs, first latency is equal to access cycles plus refresh cycles, and otherwise, only access cycles is inserted.

First Latency for reading and writing

For all of current devices, reading burst latency can be variable or fixed, which depends on configurations.

Writing burst latency is different. Although write can be variable mode or fixed mode in CellularRAM protocol, but all of current devices only support fixed latency for writing, even if devices are configured in variable mode, which makes reading in variable latency.

Turn-Around Time

Some devices have special requirements for turn-around time, so it's very important to check data sheet for these requirements.

All of current devices only support fixed latency for writing, which leads to more critical time than reading when refresh happens at the same time, especially if the two bursts are in different rows. So if devices run very fastly, one cycle turn around time may be not enough to do the things – closing last row, refreshing, activiing next row, and writing.

Device Clock Mode – HCLK and HCLK/2

SMC supports two clock modes. One is external memory clock frequency is equal to HCLK frequency, and the other is equal to HCLK/2 frequency.

Generally, HCLK mode is recommended to be used.

rf_clk_mode

For SDR burst mode, This bit selects external meory clock frequecy.

0: external memory frequency is equal to HCLK frequency.

1: external memory frequency is equal to HCLK/2 frequency.

For DDR burs mode, This bit must be cleared.

There are two implementation options for internal clock control, HCLK_2x used or not. If HCLK_2x is not used, the duty cycle of HCLK must be 50%, because both rising edge and falling edge are used in

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

PHY. If HCLK_2x is used, there is no requirement for HCLK duty cycle, but HCLK_2x and HCLK must be balanced.

For DDR mode, HCLK_2x must be used.

rf_clk_2x_en is to open HCLK_2x mode.

rf_clk_out_2x_en is to enable HCLK_2x to generate output clock.

rf_clk_sample_2x_en is to enable HCLK_2x to generate sample clock.

rf_clk_sample_2x_sampe is to select sample clock phase.

If HCLK_2x is provided from system. rf_clk_2x_en, rf_clk_out_2x_en and rf_clk_sample_2x_en are recommended to be set to prevent from the using of HCLK falling edge.

PHY Working Clock – HCLK and HCLK_2x

If only SDR mode is supported, HCLK_2x may be used or not. When used, SMC doesn't have duty cycle requirement for HCLK. When not used, HCLK should be 50% duty cycle since both edges of HCLK are used.

If DDR mode is supported, HCLK_2x must be used and there is no requirement for HCLK duty cycle.

If HCLK_2x is used, HCLK and HCLK_2x must be balanced.

Output Clock and Output DQS Control

SMCLK output can be controlled by several bits.

rf_clk_out_en

This bit opens or closes the clock output from SMCLK PAD

0: SMCLK PAD no clock output

1: SMCLK PAD output memory clock

rf_clk_mode

For burst mode NOR Flash or pSRAM, This bit selects external meory clock frequecy.

0: external memory frequency is equal to HCLK frequency.

1: external memory frequency is equal to HCLK/2 frequency.

rf_clk_out_2x_en

Both rf_clk_2x_en and rf_clk_out_2x_en should be set to enable HCLK_2x to generate output clock if HCLK_2x is provided.

Otherwise, SMC should use the inverter in delay line to generate output clock.

Summary of above three bits:

HCLK output mode and HCLK_2x not used: rf_clk_out_en is 1, rf_clk_mode is 0, rf_clk_out_2x_en is 0.

HCLK output mode and HCLK_2x used: rf_clk_out_en is 0, rf_clk_mode is 0, rf_clk_out_2x_en is 1.

HCLK/2 output mode: rf_clk_out_en is 0, rf_clk_mode is1

rf_clk_out_mode

If rf_clk_out_en is set, this field indicates output clock modes:

0: output clock is always on

1: output clock is closed during asynchronous accesses, and opened during other time.

2: output clock is opened during synchronous accesses and configurable delay time, and closed during other time.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

3: output clock is closed during asynchronous accesses, and opened during synchronous accesses and configurable delay time, and closed during other time.

If this field is configured as 2 or 3, rf_clk_out_dly is used to select delay cycle number.

rf_clk_out_dly

If rf_clk_out_en is set and rf_clk_out_mode is configured as 2 or 3, this field indicate clock opening delay cycle number from one synchronous burst end:

0: no delay

1: 1 HCLK cycle delay

2: 2 HCLK cycle delay

3: 3 HCLK cycle delay

4: 4 HCLK cycle delay

5: 5 HCLK cycle delay

6: 6 HCLK cycle delay

7: 7 HCLK cycle delay

The delay line of dl_clk_out

If output clock is HCLK mode and HCLK_2x is not used, the delay line of dl_clk_out can be used to adjust output clock timing.

Output DQ and DQM

For SDR, DQ and DQM output are synchronized with HCLK, and there is no special control for them.

For DDR, DQ and DQM output must be delayed for DQS sampling. In SMC, DQ and DQM are synchronized with the clock delayed from HCLK_2x through a delay line.

The delay line of dl_clk_wr

The delay line delays HCLK_2x to generate a clock to synchronize output DQ and DQM. So the delay value of output DQ and DQM can be adjusted through this delay line.

Sampling Clock and Input DQS

For SDR, sampling clock is generated internally through delay line and a dummy PAD.

The delay line of dl_clk_sample

The delay line can be used to adjust sample clock phase.

The dummy PAD for sampling

The dummy PAD is used to compensate the SMCLK PAD output delay and SMD/SMWAIT PAD input delay.

For DDR, sampling clock is from DQS input through four delay lines.

The delay lines of dl_clk_dqs0p, dl_clk_dqs0n, dl_clk_dqs1p and dl_clk_dqs1n

The delay line of dl_clk_dqs0p is used to adjust rising edge of DQS0.

The delay line of dl_clk_dqs0n is used to adjust falling edge of DQS0.

The delay line of dl_clk_dqs1p is used to adjust rising edge of DQS1.

The delay line of dl_clk_dqs1n is used to adjust falling edge of DQS1.

DLL and Delay Line Compensation

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

When pSRAM runs at more than 104MHz, DLL should be considered used to compensate delay line automatically.

In manual mode, delay lines are configured by a fixed number, and this number only indicates the delay step, not the delay time. Unfortunately, the delay time of each step changes in a large range under different conditions, such as process, temperature, supply voltage, etc. So when pSRAM runs at low speed, there still is a data window valid under all conditions. But if pSRAM runs at higher speed, SMC cannot find this kind of common window.

In DLL mode, the step of delay line is compensated dynamically by DLL, which guarantees delay line has a fixed delay time.

DLL is made of a master delay line, a phase detector, a DLL state machine and a delay line compensating engine. The delay line in DLL has the same design as other delay lines, which makes each step from all delay lines the same delay value. The HCLK_2x passes the master delay line, and the DLL state machine controls that the master delay line always delays by one HCLK_2x cycle. DLL can get the step number of master delay line, which indicates the one HCLK_2x cycle time, and then DLL can get the exact delay time of each step. Compensating engine uses this delay time to count the delay steps for all other slave delay lines to meet the required delay time, which is configurable for each delay line.

DLL initialize and re-configure

DLL must be cleared whenever DLL is initialized or re-configured.

DLL restart after sleep and wakeup

SMC provides an automatic engine to complete this restarting process, and this hardware process doesn't need taken care of by software. Software may not use this hardware engine, and software can initialize DLL again to achieve the same result.

Timing Descriptions

ADP/ADM/AADM Asynchronous Single Read

ADP:

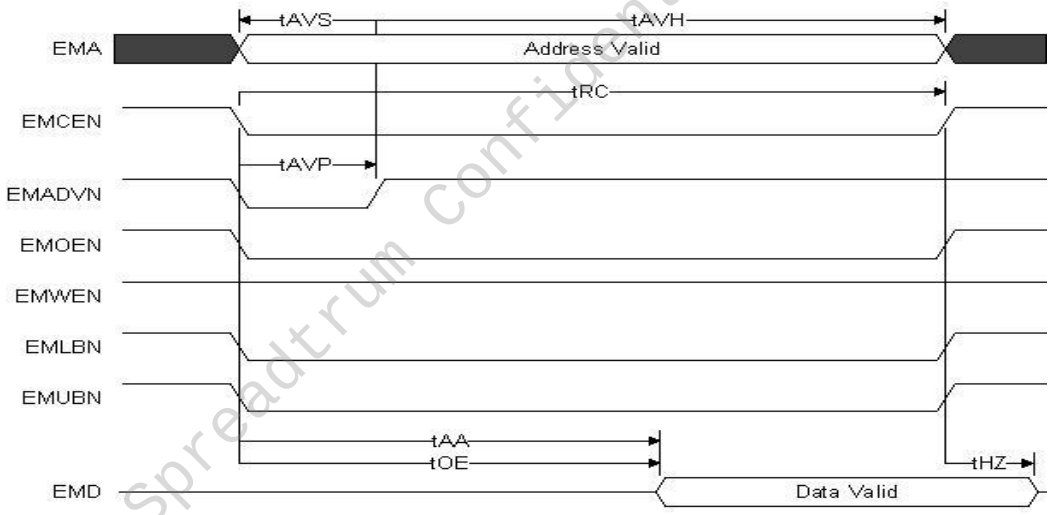


Figure 5-41 ADP asynchronous single read timing diagram

ADM:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

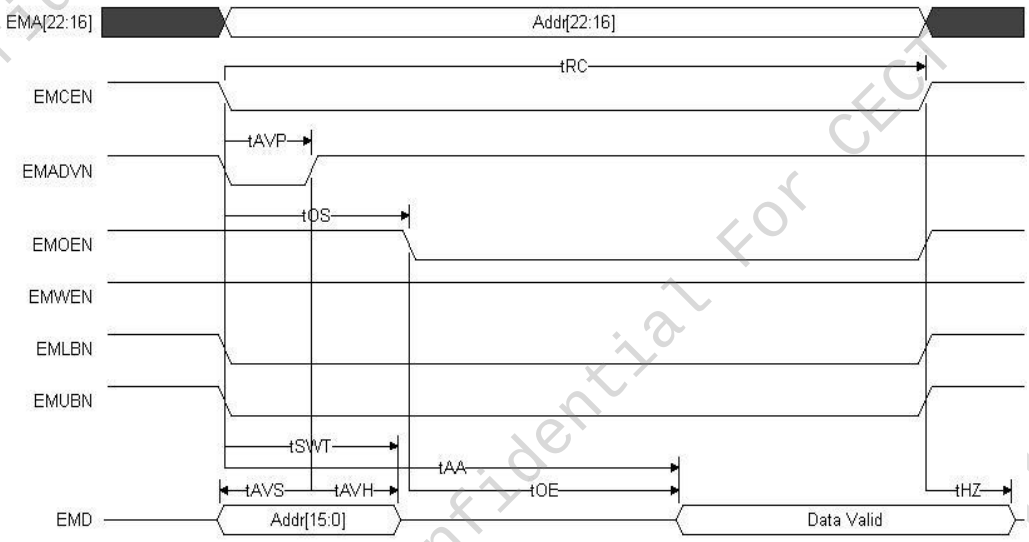


Figure 5-42 ADM asynchronous single read timing diagram

AADM:

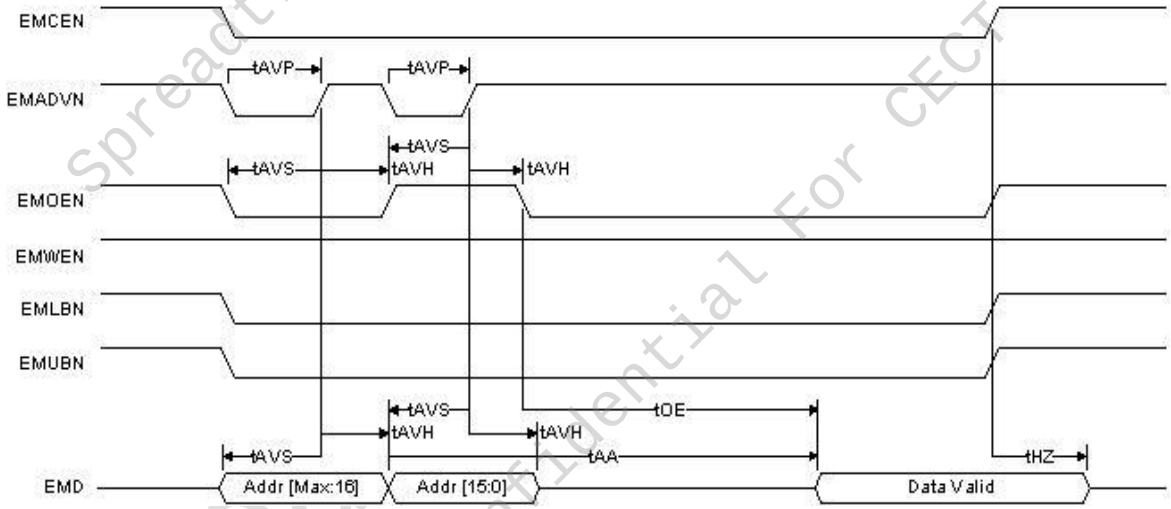


Figure 5-43 AADM asynchronous single read timing diagram

Table 5.5-2 Asynchronous single read timing parameters

Parameter	Description
tRC	tRC indicates CE# low pulse, 1~31 cycles. rf_t_first_r is used to configure tRC
tAVP	tAVP indicates ADV# low pulse, 1~3 cycles. rf_t_adv_wdt_r is used to configure tAVP
tAVS	tAVS indicates address valid to ADV# high, or CE# low to ADV# high, 0~1 cycles. If rf_t_adv_mode_r is 0, tAVS is equal to (rf_t_adv_stp_r + rf_t_adv_wdt_r). In normal conditions, rf_t_adv_stp_r is configured to 0, so tAVS is the same as tAVP.
tAVH	tAVH indicates ADV# high to address invalid, or ADV# high to CE# high, 1~2

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	cycles For ADP, address is kept until CE# goes high, so it's big enough for all devices. For ADM and AADM, tAVH is equal to (rf_t_adswt_r - rf_t_adv_stp_r - rf_t_adv_wdt_r), which is 1 or 2 cycles.
tAA	tAA indicates CE# low to data valid, or accessing time, referred to memory data sheet. This parameter is used by SMC to generate rf_t_first_r, and rf_t_first_r is equal to (tAA + tPCB + tCHIP). tPCB is PCB delay time, about 0.2ns. And tCHIP is on-chip delay, about 10ns. rf_t_first_r can be 1~31 cycles. tAA must be less than 150ns.
tOS	tOS indicates CE# low to OE#, 1~7 cycles. rf_t_oe_stp_r is used to configure tOS.
tOE	tOE indicates OE# low to data valid, referred to memory data sheet.. rf_t_first_r should guarantee not only tAA, but also tOE. tOE must be less than 150ns.
tSWT	tSWT indicates Address/Data switching point, 1~3 cycles. rf_t_adswt_r is used to configure tSWT.
tHZ	tHZ indicates CE# to data high-Z, referred to memory data sheet.. rf_t_rw should guarantee bus confliction doesn't occur. rf_t_rw can be 1~7 cycles. tHZ must be less than 35ns.

ADP/ADM/AADM Asynchronous Single Write

ADP:

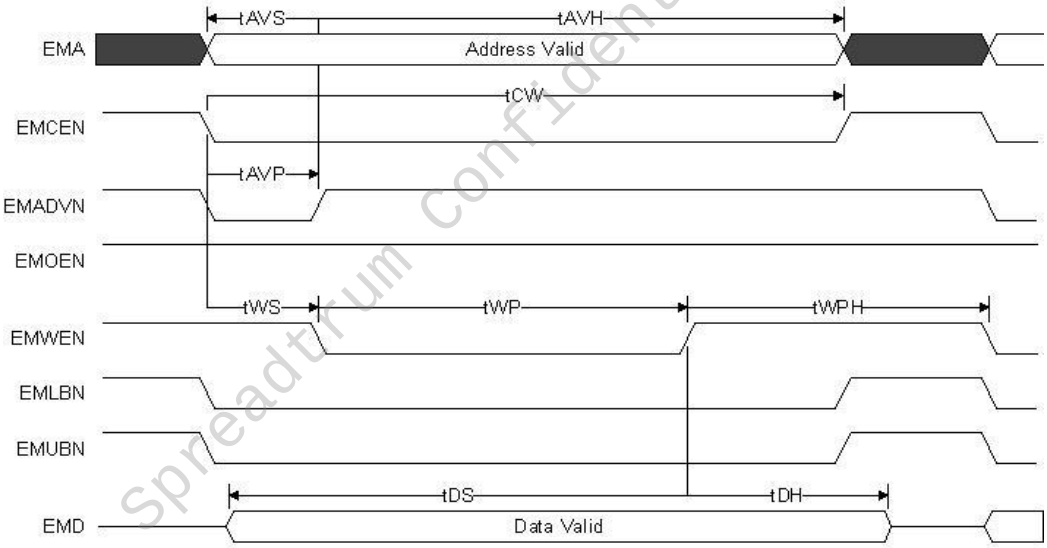


Figure 5-44 ADP asynchronous single write timing diagram

ADM:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

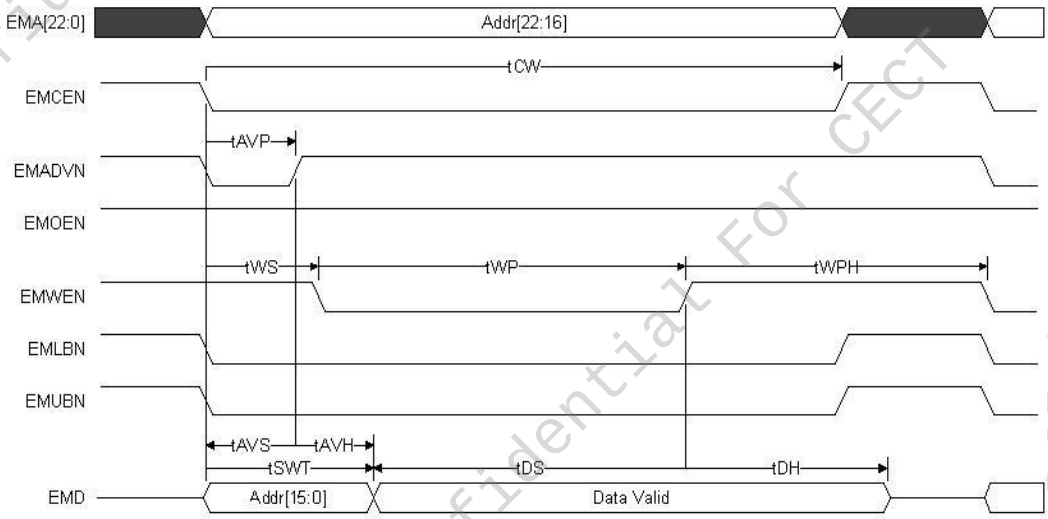


Figure 5-45 ADM asynchronous single write timing diagram

AADM:

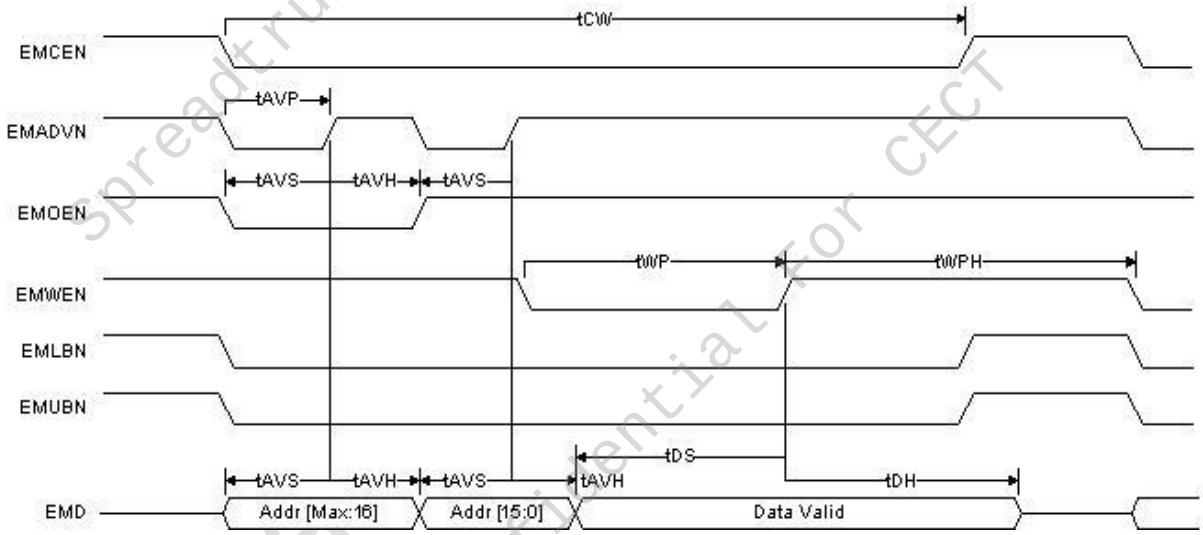


Figure 5-46 AADM asynchronous single write timing diagram

Table 5.5-3 Asynchronous single write timing parameters

Parameter	Description
tCW	tCW indicates CE# low pulse, 1~31 cycles rf_t_first_w is used to configure tCW.
tAVP	tAVP indicates ADV# low pulse, 1~3 cycles. rf_t_adv_wdt_w is used to configure tAVP
tAVS	tAVS indicates address valid to ADV# high, or CE# low to ADV# high, 0~1 cycles. If rf_t_adv_mode_w is 0, tAVS is equal to (rf_t_adv_stp_w + rf_t_adv_wdt_w). In normal conditions, rf_t_adv_stp_w is configured to 0, so tAVS is the same as tAVP.
tAVH	tAVH indicates ADV# high to address invalid, or ADV# high to CE# high, 1~2 cycles

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	For ADP, address is kept until CE# goes high, so it's big enough for all devices. For ADM and AADM, tAVH is equal to (rf_t_adswt_w - rf_t_adv_stp_w - rf_t_adv_wdt_w), which is 1 or 2 cycles.
tWS	tWS indicates CE# low to WE#, 1~7 cycles. rf_t_we_stp_w is used to configure tWS.
tWP	tWP indicates WE# low pulse, 1~15 cycles. rf_t_we_wdt_w is used to configure tWP.
tWPH	tWPH indicates WE# high pulse, 1~15 cycles. This parameter should be guaranteed from (rf_t_first_w + turn around time – rf_t_we_stp_w – rf_t_we_wdt_w).
tDS	tDS indicates data valid to WE# high, 1~15 cycles. This parameter should be guaranteed from (rf_t_we_stp_w + rf_t_we_wdt_w - rf_t_adswt_w), and rf_t_adswt_w is 0 for ADP.
tDH	tDH indicates WE# high to data invalid, 1~15 cycles. This parameter should be guaranteed from (rf_t_first_w + turn around time – rf_t_we_stp_w – rf_t_we_wdt_w).
tSWT	tSWT indicates Address/Data switching point, 1~3 cycles. rf_t_adswt_w is used to configure tSWT.

ADP Asynchronous Page Read

ADP:

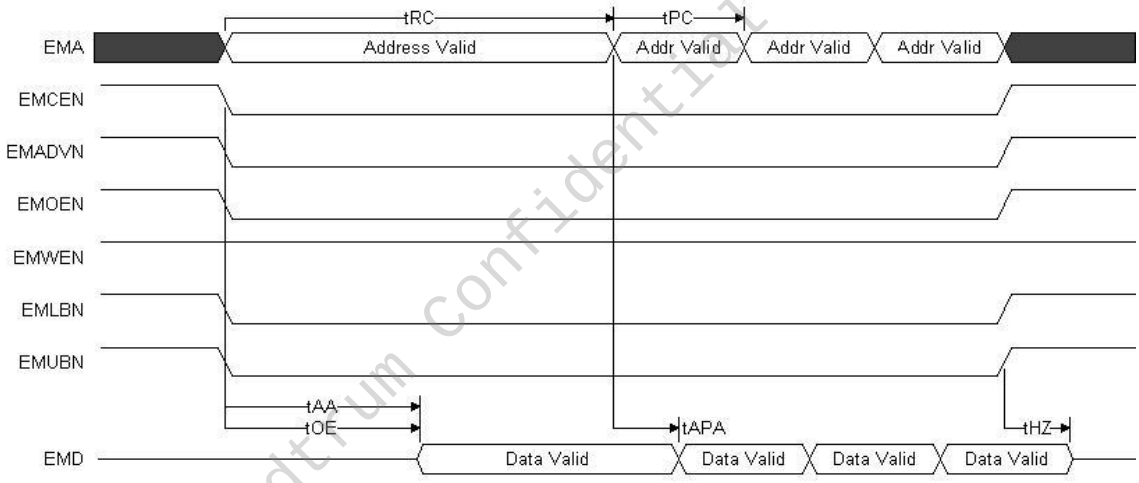


Figure 5-47 ADP asynchronous page read timing diagram

Table 5.5-4 Asynchronous page read timing parameters

Parameter	Description
tRC	tRC indicates first data accessing time, 1~31 cycles. rf_t_first_r is used to configure tRC
tPC	tPC indicates next data accessing time, 1~15 cycles. rf_t_next_r is used to configure tPC

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

tAA	tAA indicates CE# low to first data valid, or first data accessing time, referred to memory data sheet. This parameter is used by SMC to generate rf_t_first_r, and rf_t_first_r is equal to (tAA + tPCB + tCHIP). tPCB is PCB delay time, about 0.2ns. And tCHIP is on-chip delay, about 10ns. rf_t_first_r can be 1~31 cycles. tAA must be less than 150ns.
tAPA	tAPA indicates address changing to next data valid, or next data accessing time, referred to memory data sheet. This parameter is used by SMC to generate rf_t_next_r, and rf_t_next_r is equal to (tAPA + tPCB + tCHIP). tPCB is PCB delay time, about 0.2ns. And tCHIP is on-chip delay, about 10ns. rf_t_next_r can be 1~15 cycles. tAPA must be less than 65ns.
tOE	tOE indicates OE# low to data valid, referred to memory data sheet.. rf_t_first_r should guarantee not only tAA, but also tOE. tOE must be less than 150ns.
tHZ	tHZ indicates CE# to data high-Z, referred to memory data sheet.. rf_t_rw should guarantee bus confliction doesn't occur. rf_t_rw can be 1~7 cycles. tHZ must be less than 35ns.

ADP/ADM/AADM Synchronous Burst Read - SDR

ADP:

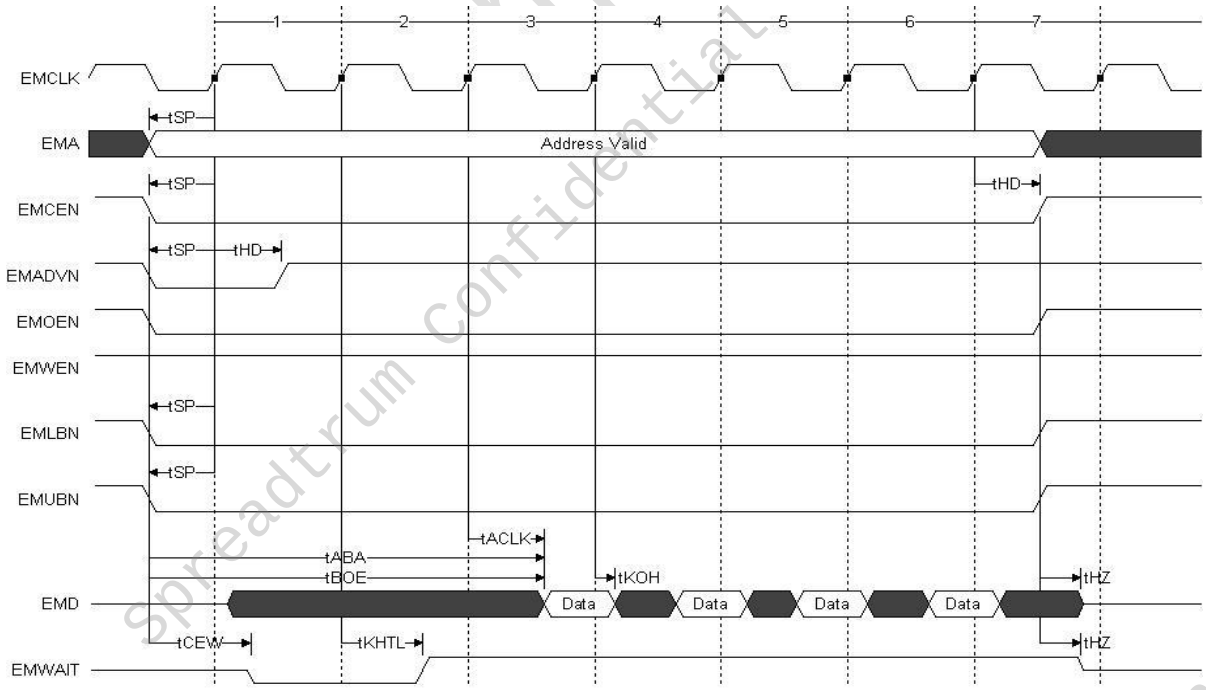


Figure 5-48 ADP synchronous SDR burst read timing diagram

ADM:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

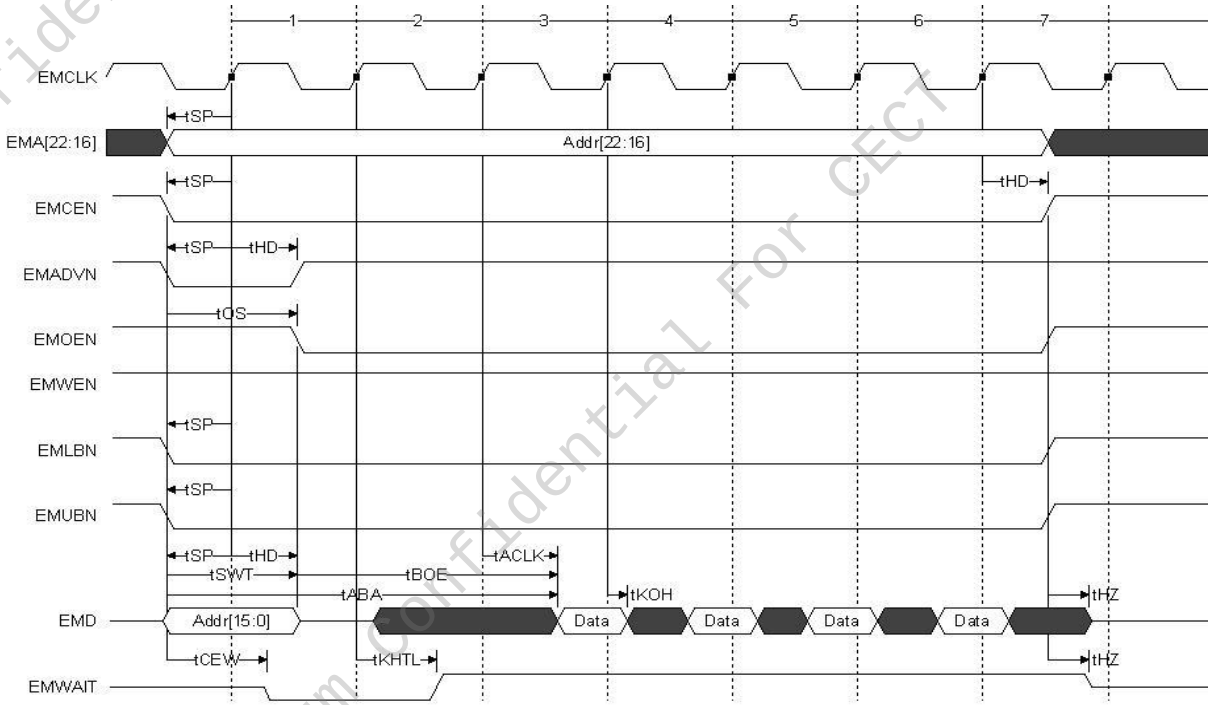


Figure 5-49 ADM synchronous SDR burst read timing diagram

AADM:

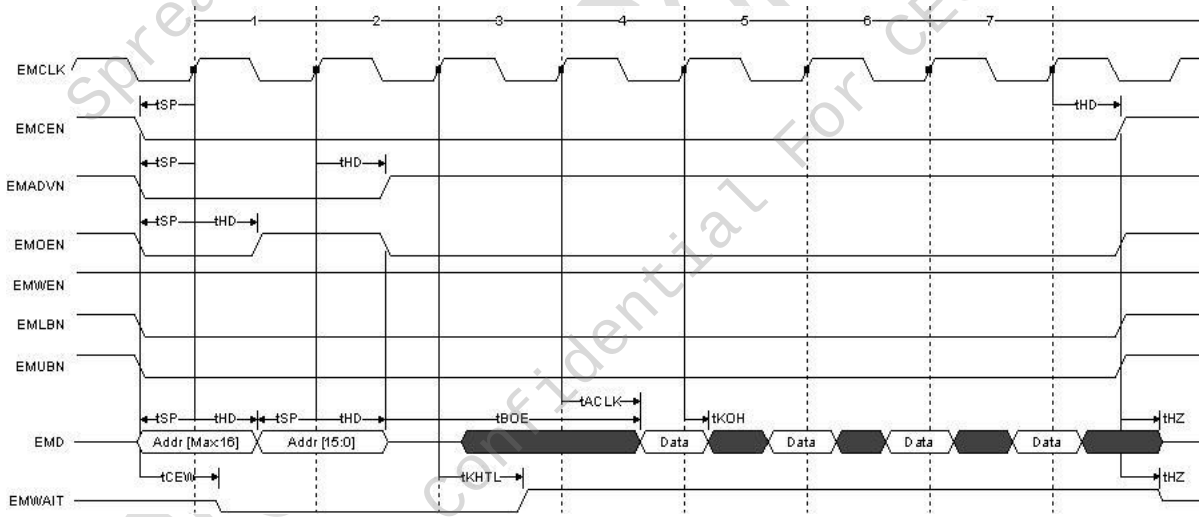


Figure 5-50 AADM synchronous SDR burst read timing diagram

Table 5.5-5 Synchronous burst read (SDR) timing parameters

Parameter	Description
tSP	tSP indicates setup time to CLK rising edge. tSP > (half cycle - 1ns). This parameter is guaranteed by SMC.
tHD	tHD indicates hold time to CLK rising edge. tHD > (half cycle - 1ns). This parameter is guaranteed by SMC.
tABA	tABA indicates CE# low to first data valid. This parameter should be guaranteed by first latency configuration on memory device. If WAIT isn't used by SMC, first latency configuration on memory device should be used to generate rf_t_first_r, which is first latency

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	value plus two.
tBOE	tBOE indicates OE# low to data valid. rf_t_first_r should guarantee not only tABA, but also tBOE.
tOS	tOS indicates CE# low to OE#, 1~7 cycles. rf_t_oe_stp_r is used to configure tOS.
tACLK	tACLK indicates CLK rising to data valid, referred to memory data sheet. This parameter is used by timing counting on SMC PHY sampling circuit. tACLK must be less than (1 cycle - 1ns).
tKHTL	tKHTL indicates CLK rising to WAIT de-asserted, referred to memory data sheet. This parameter is used by timing counting on SMC PHY sampling circuit. tKHTL must be less than (1 cycle - 1ns).
tKOH	tKOH indicates CLK rising to data invalid, referred to memory data sheet. This parameter is used by timing counting on SMC PHY sampling circuit. tKOH must be more than 1ns.
tCEW	tCEW indicates CE# low to WAIT asserted, referred to memory data sheet. This time should be masked during WAIT sampling. rf_t_sample_stp is used to generate mask signal. rf_t_sample_stp can be 1~7 cycles. tCEW must be less than 35ns.
tSWT	tSWT indicates Address/Data switching point, 1~3 cycles. rf_t_adswt_r is used to configure tSWT.
tHZ	tHZ indicates CE# to data/WAIT high-Z, referred to memory data sheet.. rf_t_rw should guarantee bus confliction doesn't occur. rf_t_rw can be 1~7 cycles. tHZ must be less than 35ns.

ADP/ADM/AADM Synchronous Burst Write - SDR

ADP:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

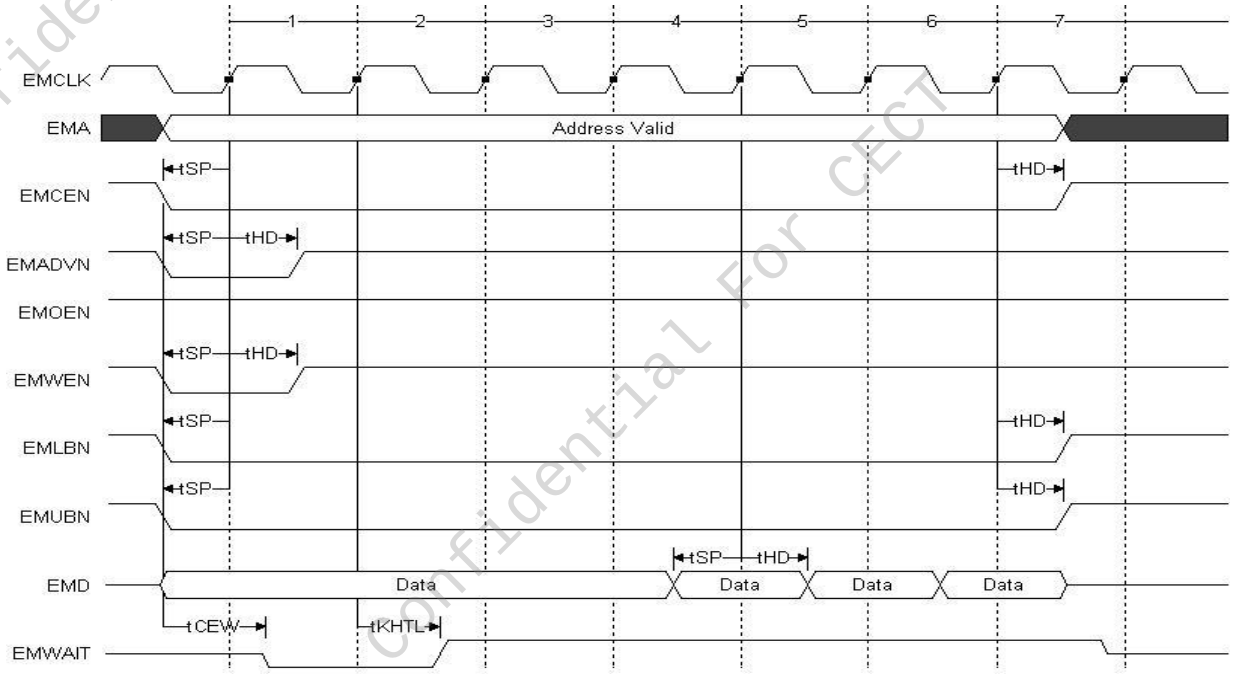


Figure 5-51 ADP synchronous SDR burst write timing diagram

ADM:

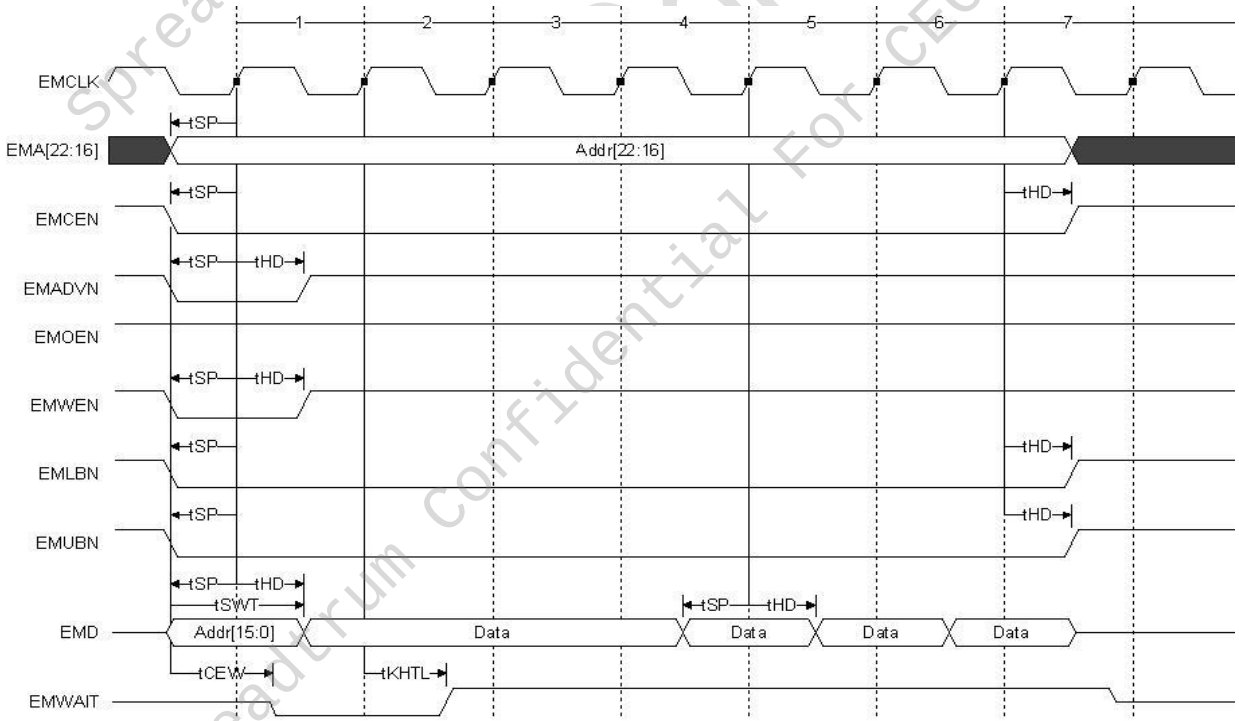


Figure 5-52 ADM synchronous SDR burst write timing diagram

AADM:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

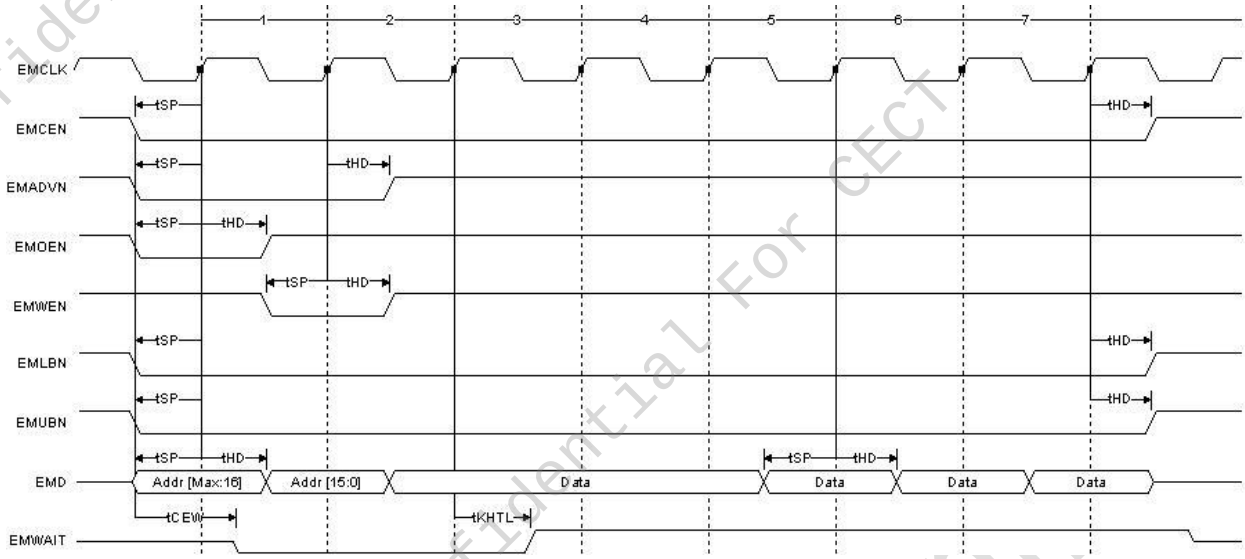


Figure 5-53 AADM synchronous SDR burst write timing diagram

Table 5.5-6 Synchronous burst write (SDR) timing parameters

Parameter	Description
tSP	tSP indicates setup time to CLK rising edge. tSP > (half cycle - 1ns). This parameter is guaranteed by SMC.
tHD	tHD indicates hold time to CLK rising edge. tHD > (half cycle - 1ns). This parameter is guaranteed by SMC.
tKHTL	tKHTL indicates CLK rising to WAIT de-asserted, referred to memory data sheet. This parameter is used by timing counting on SMC PHY sampling circuit. tKHTL must be less than (1 cycle - 1ns).
tCEW	tCEW indicates CE# low to WAIT asserted, referred to memory data sheet. This time should be masked during WAIT sampling. rf_t_sample_stp is used to generate mask signal. rf_t_sample_stp can be 1~7 cycles. tCEW must be less than 35ns.
tSWT	tSWT indicates Address/Data switching point, 1~3 cycles. rf_t_adswt_w is used to configure tSWT.

ADP/ADM/AADM Synchronous Burst Read - DDR

ADP:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

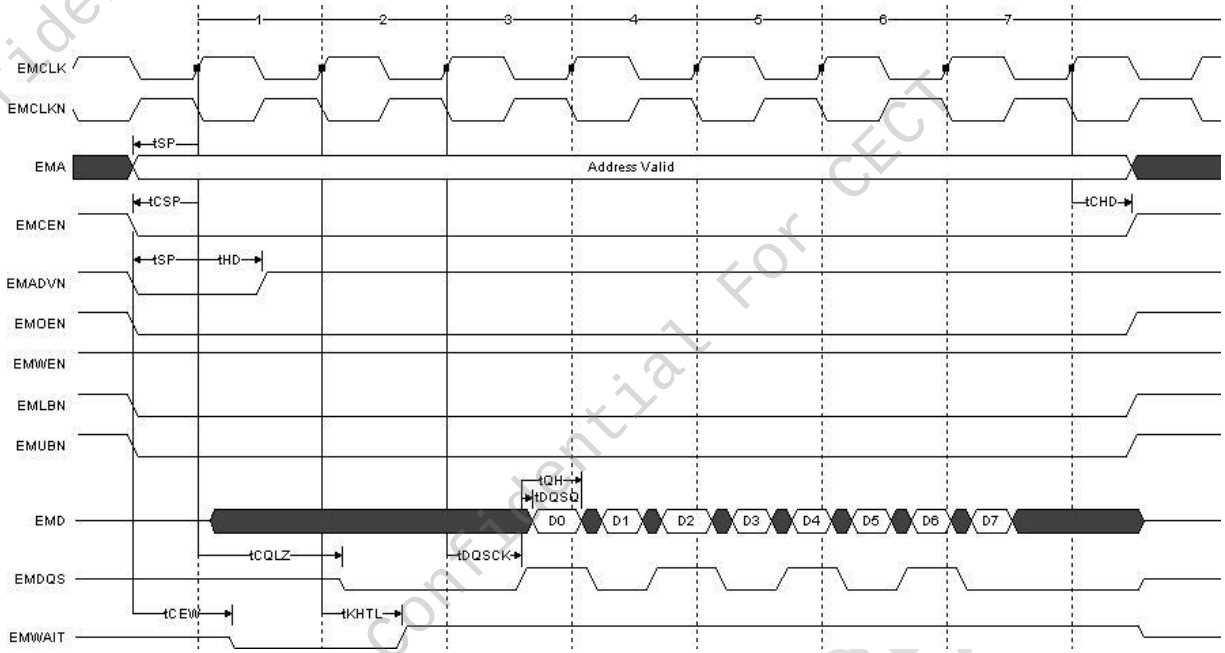


Figure 5-54 ADP synchronous DDR burst read timing diagram

ADM:

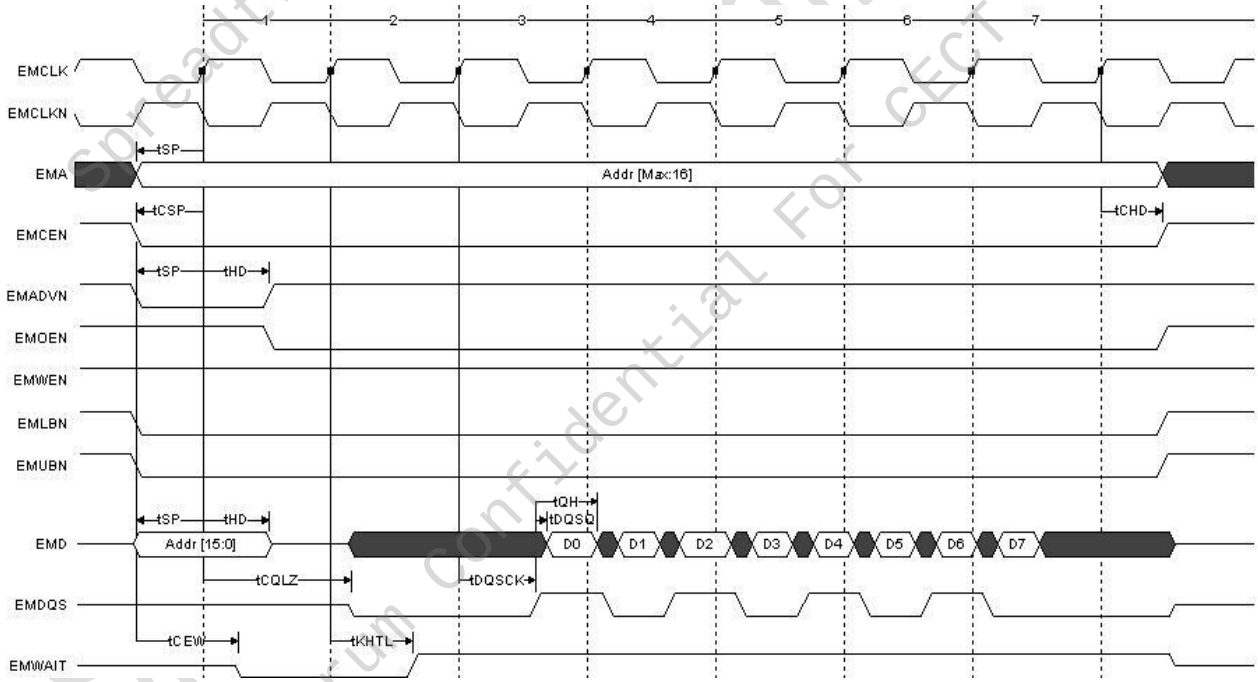


Figure 5-55 ADM synchronous DDR burst read timing diagram

AADM:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

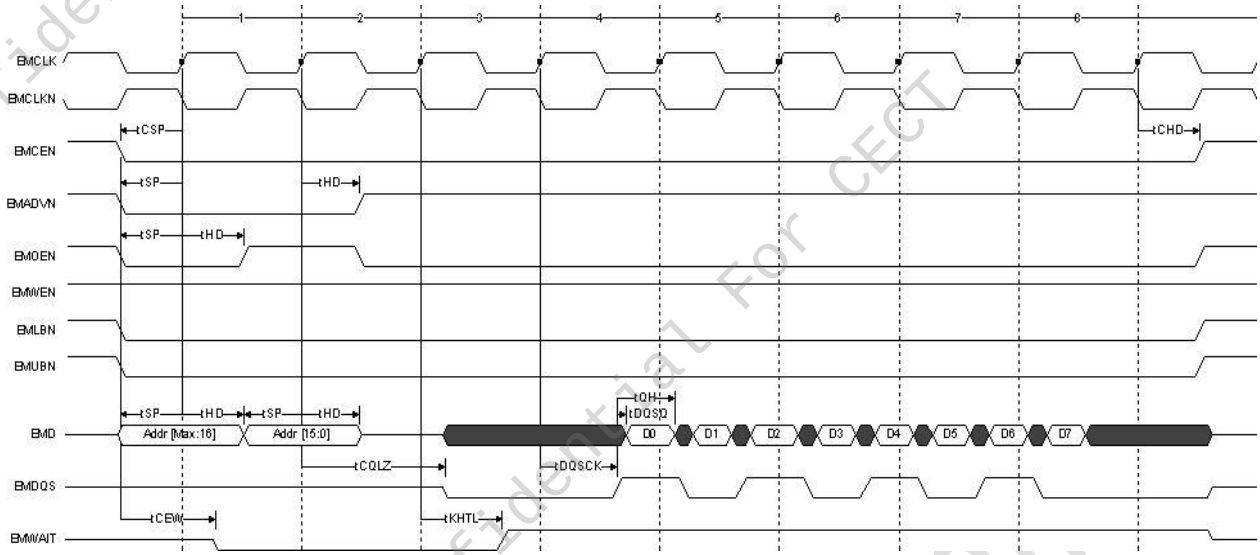


Figure 5-56 AADM synchronous DDR burst read timing diagram

Table 5.5-7 Synchronous burst read (DDR) timing parameters

Parameter	Description
tSP	tSP indicates setup time to CLK rising edge. tSP > (half cycle - 1ns). This parameter is guaranteed by SMC.
tHD	tHD indicates hold time to CLK rising edge. tHD > (half cycle - 1ns). This parameter is guaranteed by SMC.
tCSP	tCSP indicate tSP of CE#. This parameter is separated because normally this parameter is more difficult to meet than tSP. tCSP > (half cycle - 1ns). This parameter is guaranteed by SMC.
tCHD	tCHD indicate tHD of CE#. This parameter is separated because normally this parameter is more difficult to meet than tHD. tCHD > (half cycle - 1ns). This parameter is guaranteed by SMC.
tKHTL	tKHTL indicates CLK rising to WAIT de-asserted, referred to memory data sheet. This parameter is used by timing counting on SMC PHY sampling circuit. tKHTL must be less than (1 cycle - 1ns).
tCEW	tCEW indicates CE# low to WAIT asserted, referred to memory data sheet. This time should be masked during WAIT sampling. rf_t_sample_stp is used to generate mask signal. rf_t_sample_stp can be 1~7 cycles. tCEW must be less than 35ns.
tCQLZ	tCQLZ indicates first clock rising edge to DQS low-Z during reading, referred to memory data sheet. This time should be masked. rf_t_sample_stp is also used to generate mask signal. rf_t_sample_stp can be 1~7 cycles. tCQLZ must be less than 35ns.
tDQSCK	tDQSCK indicates clock rising edge to DQS rising edge, referred to memory data sheet.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	This parameter changes during a large range normally, so for sampling FIFO during PHY, DDR device needs more delay cycles between data sampling to data output than SDR device, and DDR sampling FIFO has three entries when SDR has two entries. That is reason why only DQS can be used as sampling clock instead of internal sampling clock like SDR. tDQSCK must be less than 1 cycle.
tDQSQ	tDQSQ indicates DQS edge to data valid, referred to memory data sheet. For 200MHz, tDQSQ must be less than 0.6ns For 166MHz, tDQSQ must be less than 0.7ns For 133MHz, tDQSQ must be less than 0.8ns For 100MHz, tDQSQ must be less than 1.0ns
tQH	tQH indicates DQS edge to data invalid, referred to memory data sheet. tQH is equal to (half cycle - tQHS). For 200MHz, tQHS must be less than 0.7ns For 166MHz, tQHS must be less than 0.8ns For 133MHz, tQHS must be less than 0.9ns For 100MHz, tQHS must be less than 1.1ns
	Data valid window is (tQH – tDQSQ)

ADP/ADM/AADM Synchronous Burst Write - DDR

ADP:

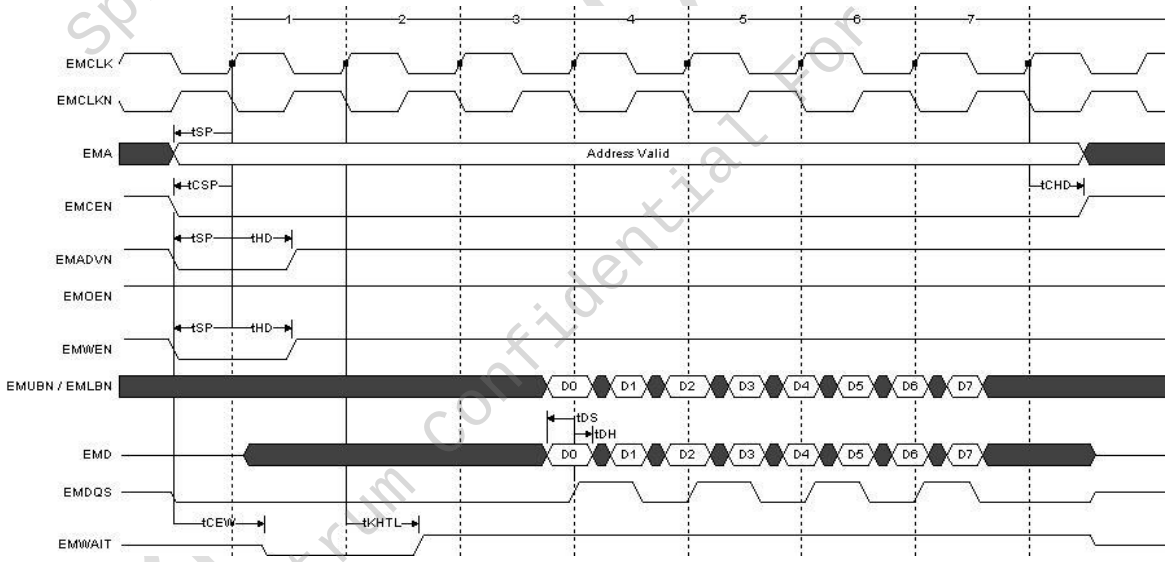


Figure 5-57 ADP synchronous DDR burst write timing diagram

ADM:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

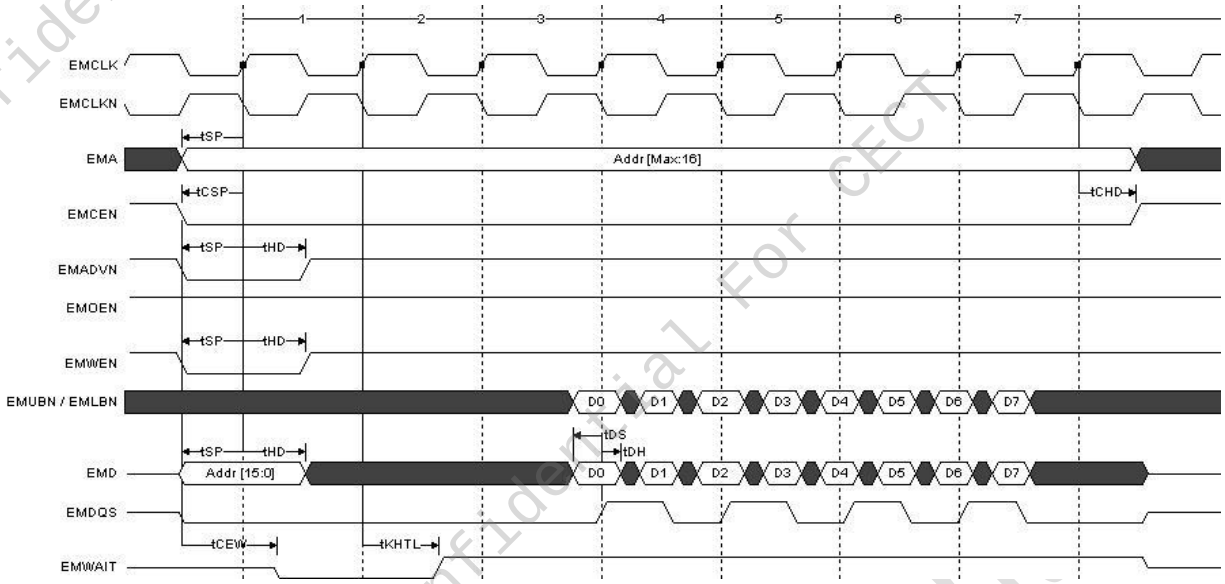


Figure 5-58 ADM synchronous DDR burst write timing diagram

AADM:

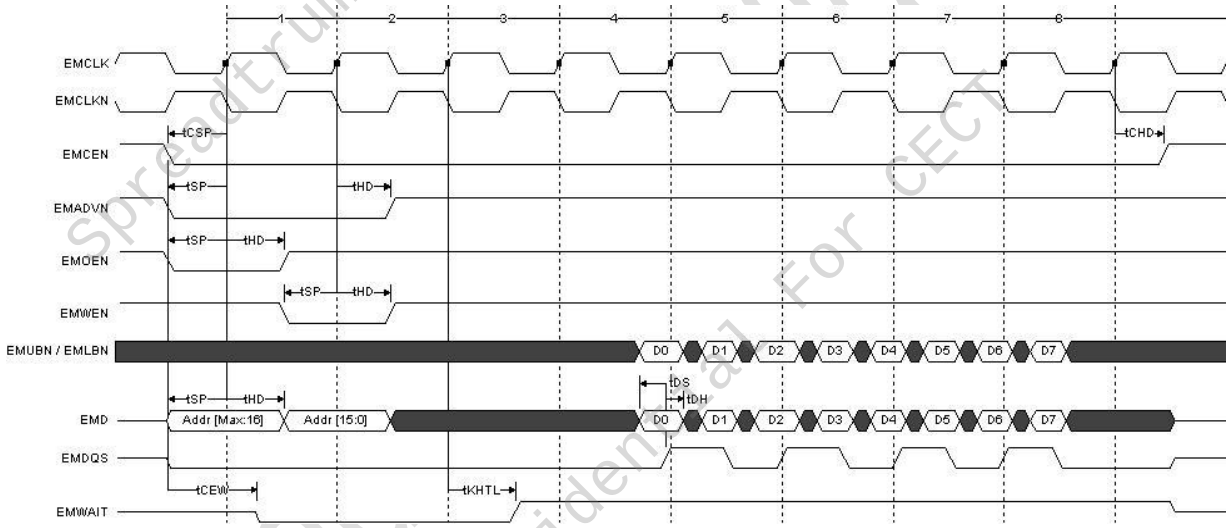


Figure 5-59 AADM synchronous DDR burst write timing diagram

Table 5.5-8 Synchronous burst write (DDR) timing parameters

Parameter	Description
tSP	tSP indicates setup time to CLK rising edge. tSP > (half cycle - 1ns). This parameter is guaranteed by SMC.
tHD	tHD indicates hold time to CLK rising edge. tHD > (half cycle - 1ns). This parameter is guaranteed by SMC.
tCSP	tCSP indicate tSP of CE#. This parameter is separated because normally this parameter is more difficult to meet than tSP. tCSP > (half cycle - 1ns). This parameter is guaranteed by SMC.
tCHD	tCHD indicate tHD of CE#. This parameter is separated because normally this parameter is more difficult to meet than tHD.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	tCHD > (half cycle - 1ns). This parameter is guaranteed by SMC.
tKHTL	tKHTL indicates CLK rising to WAIT de-asserted, referred to memory data sheet. This parameter is used by timing counting on SMC PHY sampling circuit. tKHTL must be less than (1 cycle - 1ns).
tCEW	tCEW indicates CE# low to WAIT asserted, referred to memory data sheet. This time should be masked during WAIT sampling. rf_t_sample_stp is used to generate mask signal. rf_t_sample_stp can be 1~7 cycles. tCEW must be less than 35ns.
tDS	tDS indicates DQ and DQM valid to DQS edge. For 200MHz, tDS > 0.8ns For 166MHz, tDS > 0.9ns For 133MHz, tDS > 1.0ns For 100MHz, tDS > 1.2ns
tDH	tDH indicates DQS edge to DQ and DQM invalid. For 200MHz, tDH > 0.8ns For 166MHz, tDH > 0.9ns For 133MHz, tDH > 1.0ns For 100MHz, tDH > 1.2ns

Control Registers

Memory map

ARM base address: 0x2000_0000

Offset Address	Name	Description
0x1000	SMC_CFG0	SMC general control register 0
0x1004	SMC_CFG1	SMC general control register 1
0x1008	SMC_CFG2	SMC general control register 2
0x100C	Reserved	
0x1010	Reserved	
0x1014	Reserved	
0x1018	Reserved	
0x101C	SMC_STS0	SMC general status register 0
0x1020	SMC_DL0	SMC delay line register 0 – clk_out
0x1024	SMC_DL1	SMC delay line register 1 – clk_sample
0x1028	SMC_DL2	SMC delay line register 2 – clk_wr

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x102C	SMC_DL3	SMC delay line register 3 – clk_dqs0p
0x1030	SMC_DL4	SMC delay line register 4 – clk_dqs0n
0x1034	SMC_DL5	SMC delay line register 5 – clk_dqs1p
0x1038	SMC_DL6	SMC delay line register 6 – clk_dqs1n
0x103C	Reserved	
0x1040	SMC_CFG0_CS0	SMC CS0 control register 0
0x1044	SMC_CFG1_CS0	SMC CS0 control register 1
0x1048	SMC_CFG2_CS0	SMC CS0 control register 2
0x104C	SMC_CFG3_CS0	SMC CS0 control register 3
0x1050	SMC_CFG0_CS1	SMC CS1 control register 0
0x1054	SMC_CFG1_CS1	SMC CS1 control register 1
0x1058	SMC_CFG2_CS1	SMC CS1 control register 2
0x105C	SMC_CFG3_CS1	SMC CS1 control register 3
0x1060	SMC_CFG0_CS2	SMC CS2 control register 0
0x1064	SMC_CFG1_CS2	SMC CS2 control register 1
0x1068	SMC_CFG2_CS2	SMC CS2 control register 2
0x106C	SMC_CFG3_CS2	SMC CS2 control register 3
0x1070	SMC_CFG0_CS3	SMC CS3 control register 0
0x1074	SMC_CFG1_CS3	SMC CS3 control register 1
0x1078	SMC_CFG2_CS3	SMC CS3 control register 2
0x107C	SMC_CFG3_CS3	SMC CS3 control register 3

Register Descriptions

SMC_CFG0

Description: SMC general control register
This register is SMC general control register, shared by all external memories.

0x1000	SMC general control register 0 (Reset 0x33330000)												SMC_CFG0			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved	rf_t_ww			Reserved	rf_t_wr			Reserved	rf_t_rw			Reserved	rf_t_rr		
Type	RO	RW			RO	RW			RO	RW			RO	RW		
Reset	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	rf_sample_auto_rst_en	rf_clk_sample_sel	rf_clk_out_dly			rf_data_src_mode		rf_sample_rst	rf_clk_out_mode		rf_clk_out_en	rf_clk_mode	Reserved		rf_cs_position	
Type	RW	RW	RW			RW		RW	RW		RW	RW	RO		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Reserved	[31]	RO	0	Reserved
rf_t_ww	[30:28]	RW	3'h3	rf_t_ww Write to write turn around time 0: no turn around 1: 1 HCLK cycle 2: 2 HCLK cycle … 7: 7 HCLK cycle
Reserved	[27]	RO	0	Reserved
rf_t_wr	[26:24]	RW	3'h3	rf_t_wr Write to read turn around time 0: no turn around 1: 1 HCLK cycle 2: 2 HCLK cycle … 7: 7 HCLK cycle
Reserved	[23]	RO	0	Reserved
rf_t_rw	[22:20]	RW	3'h3	rf_t_rw Read to write turn around time 0: no turn around 1: 1 HCLK cycle 2: 2 HCLK cycle … 7: 7 HCLK cycle
Reserved	[19]	RO	0	Reserved
rf_t_rr	[18:16]	RW	3'h3	rf_t_rr Read to read turn around time 0: no turn around 1: 1 HCLK cycle 2: 2 HCLK cycle … 7: 7 HCLK cycle

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
rf_sample_auto_rst_en	[15]	RW	1'b0	rf_sample_auto_rst_en Sample FIFO pointer automatically reset during IDLE 0: disable automatically reset 1: enable automatically reset For SDR, this function should be used only during debug. For DDR, this bit MUST be set.
rf_clk_sample_sel	[14]	RW	1'b0	rf_clk_sample_sel Sample clock source select. 0: loop through a dummy PAD 1: NOT loop through PAD
rf_clk_out_dly	[13:11]	RW	3'h0	rf_clk_out_dly If rf_clk_out_en or rf_clk_out_2x_en is set and rf_clk_out_mode is configured as 2 or 3, this field indicate clock opening delay cycle number from one synchronous burst end: 0: no delay 1: 1 HCLK cycle delay 2: 2 HCLK cycle delay 3: 3 HCLK cycle delay 4: 4 HCLK cycle delay 5: 5 HCLK cycle delay 6: 6 HCLK cycle delay 7: 7 HCLK cycle delay
rf_data_src_mode	[10:9]	RW	2'h0	rf_data_src_mode If related rf_data_sel of operating CS is set: 0: SMA[15:0] output address during burst interval 1: SMA[15:0] output from high-Z to address one cycle delay 2: SMA[15:0] is high-Z during burst interval
rf_sample_rst	[8]	RW	1'b0	rf_sample_rst Sample FIFO pointer reset. Active high.
rf_clk_out_mode	[7:6]	RW	2'h0	rf_clk_out_mode If rf_clk_out_en or rf_clk_out_2x_en is set, this field indicate output clock modes: 0: output clock is always on 1: output clock is closed during asynchronous accesses, and opened during other time. 2: output clock is opened during synchronous accesses and configurable delay time, and closed during other time. 3: output clock is closed during asynchronous accesses, and opened during synchronous accesses and configurable delay time, and closed during other time. If this field is configured as 2 or 3, rf_clk_out_dly is

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
				used to select delay cycle number.
rf_clk_out_en	[5]	RW	1'b0	rf_clk_out_en If HCLK_2x isn't used: 0: SMCLK PAD no clock output 1: SMCLK PAD output memory clock
rf_clk_mode	[4]	RW	1'b0	rf_clk_mode 0: HCLK 1: HCLK/2
Reserved	[3:2]	RO	0	Reserved
rf_cs_position	[1:0]	RW	2'h0	rf_cs_position 0: CS[1:0] mapping to HADDR[27:26] 1: CS[1:0] mapping to HADDR[26:25] 2: CS[1:0] mapping to HADDR[25:24] 3: CS[1:0] mapping to HADDR[24:23]

SMC_CFG1

Description: SMC general control register
This register is SMC general control register, shared by all external memories.

0x1004	SMC general control register 1 (Reset 0x10000010)												SMC_CFG1			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved									rf_ddr_wdata_mode	rf_ddr_wdata_dly		rf_clk_sample_2x_phase	rf_clk_sample_2x_en	rf_clk_out_2x_en	rf_clk_2x_en
Type	RO									RW	RW		RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
Reserved	[31:7]	RO	0	Reserved
rf_ddr_wdata_mode	[6]	RW	1'b0	rf_ddr_wdata_mode This field is to control the internal behavior for DDR write burst. 0: mode 0. If this bit is 0, WAIT for write can be used or not used, and rf_ddr_wdata_dly should be 1. 1: mode 1. If this bit is 1, WAIT for write must not be used, and rf_ddr_wdata_dly should be 2. It's important that there are different configurations on rf_t_first_w for the same latency between different value of this bit.
rf_ddr_wdata_dly	[5:4]	RW	2'h1	rf_ddr_wdata_dly This field is to control the behavior at the end of DDR write burst. This filed should be 1, if rf_ddr_wdata_mode is 0. This filed should be 2, if rf_ddr_wdata_mode is 1. There is a debug mode that this field is 0 and rf_ddr_wdata_mode is 0.
rf_clk_sample_2x_phase	[3]	RW	1'b0	rf_clk_sample_2x_phase If rf_clk_sample_2x_en is set, this bit is used to select phase when 1X sample clock is generated by 2X HCLK_2x.
rf_clk_sample_2x_en	[2]	RW	1'b0	rf_clk_sample_2x_en If rf_clk_2x_en is set, this bit is to enable HCLK_2x using to generate sample clock. 0: HCLK used to generate sample clock 1: HCLK_2x used to generate sample clock rf_clk_2x_en MUST be set before setting rf_clk_sample_2x_en. For DDR, this bit is to control WAIT sampling, and is recommended to be set. For SDR, this bit is to control Data and WAIT sampling, and is recommended to be set if HCLK_2x is provided.
rf_clk_out_2x_en	[1]	RW	1'b0	rf_clk_out_2x_en If rf_clk_2x_en is set, this bit is to enable HCLK_2x using to generate output clock. 0: HCLK used to generate output clock 1: HCLK_2x used to generate output clock rf_clk_2x_en MUST be set before setting rf_clk_out_2x_en. For DDR, this be MUST be set. For SDR, it's recommended to set this bit if HCLK_2x is provided.
rf_clk_2x_en	[0]	RW	1'b0	rf_clk_2x_en This bit is used to enable HCLK_2x using in SMC 0: HCLK_2x not used, HCLK MUST be 50% duty cycle

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
				1: HCLK_2x used, and no duty cycle requirement for HCLK For DDR, this be MUST be set.

SMC_CFG2

Description: SMC general control register

This register is SMC general control register, shared by all external memories.

0x1008			SMC general control register 2 (Reset 0x10000000)										SMC_CFG2			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rfsts_dll_locked	Reserved	rfsts_dll_phase2	rfsts_dll_phase1	rfsts_dll_error	rfsts_dll_cnt							rf_dll_search_mode	rf_dll_phase_interval		
Type	RO	RO	RO	RO	RO	RO							RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rf_dll_cpst_thr				rf_dll_cpst_start	rf_dll_cpst_en	rf_dll_auto_clr_en	rf_dll_clr	rf_dll_en	rf_dll_init						
Type	RW				WO	RW	RW	RW	RW	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
rfsts_dll_locked	[31]	RO	1'b0	rf_dll_locked DLL locked indicator
Reserved	[30]	RO	0	Reserved
rfsts_dll_phase2	[29]	RO	1'b0	rf_dll_phase2 DLL phase detector
rfsts_dll_phase1	[28]	RO	1'b0	rf_dll_phase1 DLL phase detector
rfsts_dll_error	[27]	RO	1'b0	rfsts_dll_error

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
				DLL error indicator
rfsts_dll_cnt	[26:20]	RO	7'h0	rfsts_dll_cnt DLL counter status
rf_dll_search_mode	[19]	RW	1'b0	rf_dll_search_mode DLL search stage mode control It's recommended to configure to 0.
rf_dll_phase_interval	[18:16]	RW	3'h2	rf_dll_phase_interval DLL phase detector interval step number It's usually configured to 1 or 2.
rf_dll_cpst_thr	[15:12]	RW	4'h0	rf_dll_cpst_thr This filed is to prevent compensating engine from changing too frequently. A threshold can be configured to the engine, and only if DLL counter changes more than threshold, the engine is trigged.
rf_dll_cpst_start	[11]	WO	1'b0	rf_dll_cpst_start This bit is used to force to start one compensation. This bit is only for debug.
rf_dll_cpst_en	[10]	RW	1'b0	rf_dll_cpst_en This bit is to enable the function of compensating Delay Line automatically by DLL. This bit is just to enable the whole compensating engine, not for each delay line. There are other independent enable bits for each delay line. If any delay line is configured as automatically compensating, this bit MUST be set, and also DLL MUST be open.
rf_dll_auto_clr_en	[9]	RW	1'b0	rf_dll_auto_clr_en This bit is to enable the function of resetting DLL automatically during system sleep
rf_dll_clr	[8]	RW	1'b0	rf_dll_clr DLL clear bit set this bit to reset DLL
rf_dll_en	[7]	RW	1'b0	rf_dll_en DLL enable bit This bit is just to enable DLL engine, which doesn't have any effect on controller. If any delay line shall be compensated automatically by DLL, rf_dll_cpst_en should be set to start compensating engine.
rf_dll_init	[6:0]	RW	7'h0	rf_dll_init DLL counter initial value

SMC_STS0

Description: SMC status

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

This register indicates SMC status.

0x101C			SMC general status register 0 (Reset 0x10000000)										SMC_STS0			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															rf_sts_cpst_st
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rfsts_dll_st				Reserved		rfsts_smem_st		Reserved			rfsts_wbuf32_wait	rfsts_wbuf16_wait	rfsts_rbuf_term	rfsts_rbuf_wait	rfsts_rbuf_active
Type	RO				RO		RO		RO			RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Reserved	[31:17]	RO	0	Reserved
rfsts_cpst_st	[16]	RO	0	For debug
rfsts_dll_st	[15:12]	RO	0	For debug
Reserved	[11:10]	RO	0	Reserved
rfsts_smem_st	[9:8]	RO	0	For debug
Reserved	[7:5]	RO	0	Reserved
rfsts_wbuf32_wait	[4]	RO	0	For debug
rfsts_wbuf16_wait	[3]	RO	0	For debug
rfsts_rbuf_term	[2]	RO	0	For debug
rfsts_rbuf_wait	[1]	RO	0	For debug
rfsts_rbuf_active	[0]	RO	0	For debug

SMC_DLx

Description: SMC delay line control register
This register is SMC delay line control register, shared by all external memories.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1020 0x1024 0x1028 0x102C 0x1030 0x1034 0x1038	SMC delay line reg0 – clk_out (Reset 0x10000000) SMC delay line reg1 – clk_sample (Reset 0x10000000) SMC delay line reg2 – clk_wr (Reset 0x10000000) SMC delay line reg3 – clk_dqs0p (Reset 0x10000000) SMC delay line reg4 – clk_dqs0n (Reset 0x10000000) SMC delay line reg5 – clk_dqs1p (Reset 0x10000000) SMC delay line reg6 – clk_dqs1n (Reset 0x10000000)	SMC_DL0 SMC_DL1 SMC_DL2 SMC_DL3 SMC_DL4 SMC_DL5 SMC_DL6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved	rfsts_dlx_dly_cnt							Reserved							
Type	RO	RO							RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved							rf_dlx_dly_cpst_en	rf_dlx_dly_inv	rf_dlx_dly_sel						
Type	RO							RW	RW	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Reserved	[31]	RO	0	Reserved
rfsts_dlx_dly_cnt	[30:24]	RO	7'h0	rfsts_dlx_dly_cnt This filed indicates the current delay line step.
Reserved	[23:9]	RO	0	Reserved
rf_dlx_dly_cpst_en	[8]	RW	1'b0	rf_dlx_dly_cpst_en This bit is to enable automatically compensating delay line by DLL. rf_dll_cpst_en MUST be set before this bit is set.
rf_dlx_dly_inv	[7]	RW	1'b0	rf_dlx_dly_inv This bit is to enable an inverter in delay line.
rf_dlx_dly_sel	[6:0]	RW	7'h0	rf_dlx_dly_sel If rf_dlx_dly_cpst_en is cleared, this filed is to control delay line step directly. If rf_dlx_dly_cpst_en is set, this filed indicates the

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
				percentage of one HCLK_2x cycle time that delay line should be delayed. The function is: rf_dlx_dly_sel = (delay time) * 128 / (HCLK_2x cycle time)

SMC_CFG0_CSx

Description: SMC CSx control register
This register is used to configure general information for external memory CSx.
Each CS has an independent registers.

0x1040 0x1050 0x1060 0x1070			SMC CS0 control register 0 (Reset 0x10904FF0) SMC CS1 control register 0 (Reset 0x10904FF0) SMC CS2 control register 0 (Reset 0x10904FF0) SMC CS3 control register 0 (Reset 0x10904FF0)						SMC_CFG0_CS0 SMC_CFG0_CS1 SMC_CFG0_CS2 SMC_CFG0_CS3							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rf_t_data_out_sel_hld	rf_t_ublb_sel_hld	rf_t_ublb_end_mode	rf_t_ublb_str_mode	rf_ddr_en	rf_aadmux_addr_swt	rf_aadmux_en	rf_data_src_sel	rf_admux_en	rf_row_length			rf_row_detect_en_w	rf_row_detect_en_r	rf_cre_en	rf_cre_mode
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rf_cre_pol	rf_wait_pol	rf_wait_en_w	rf_wait_en_r	rf_burst_mode_w	rf_burst_length_w			rf_burst_mode_r	rf_burst_length_r			rf_mode_w		rf_mode_r	
Type	RW	RW	RW	RW	RW	RW			RW	RW			RW		RW	
Reset	0	1	0	0	1	1	1	1	1	1	1	1	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
rf_t_data_out_sel_hld	[31]	RW	1'b0	rf_t_data_out_sel_hld For DDR write burst, this bit indicates the data switching time between normal clock and delayed clock at the end of the burst

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
				0: switching at the same time with CE# going high 1: switching one cycle delayed after CE# going high
rf_t_ublb_sel_hld	[30]	RW	1'b0	rf_t_ublb_sel_hld For DDR write burst, this bit indicates the UB#/LB# switching time between normal clock and delayed clock at the end of the burst 0: switching at the same time with CE# going high 1: switching one cycle delayed after CE# going high
rf_t_ublb_end_mode	[29]	RW	1'b0	rf_t_ublb_end_mode For DDR write burst, this bit indicates the UB#/LB# last cycle status at the end of the burst. 0: DON'T CARE 1: force to high
rf_t_ublb_str_mode	[28]	RW	1'b0	rf_t_ublb_str_mode For ADMUX DDR, this bit indicates the UB#/LB# status during address output at the first cycle. 0: DON'T CARE 1: force to low
rf_ddr_en	[27]	RW	1'b0	rf_ddr_en DDR enable bit. If this bit is set, SMC MUST be configured in synchronous burst mode.
rf_aadmux_addr_swt	[26]	RW	1'b0	rf_aadmux_addr_swt This bit indicates the sequence of address output. 0: address[Max:16] output firstly, then address[15:0] 1: address[15:0] output firstly, then address[Max:16]
rf_aadmux_en	[25]	RW	1'b0	rf_aadmux_en AADMUX enable bit. If this bit is set, rf_admux_en MUST also be set.
rf_data_src_sel	[24]	RW	1'b0	rf_data_src_sel 0: related data ports are connected with SMD[15:0] 1: related data ports are connected with SMA[15:0] Note, if this bit is set, SMC only supports asynchronous ADP device on this CS.
rf_admux_en	[23]	RW	1'b1	rf_admux_en 0: ADP 1: ADM Note, this bit is only used for CS1-CS4; For CS0, this bit is READ-Only, and the ADP/ADM select is strapping input from PAD.
rf_row_length	[22:20]	RW	3'h1	rf_row_length Row length: 0: 64 16-bit 1: 128 16-bit 2: 256 16-bit

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
				3: 512 16-bit 4: 1024 16-bit 5: reserved 6: reserved 7: reserved
rf_row_detect_en_w	[19]	RW	1'b0	rf_row_detect_en_w Burst write row boundary detect enable. If set, when a row boundary is detected, current device burst is terminated, and a new device burst is issued. If rf_wait_en_w is cleared, rf_row_detect_en_w is recommended to set.
rf_row_detect_en_r	[18]	RW	1'b0	rf_row_detect_en_r Burst read row boundary detect enable. If set, when a row boundary is detected, current device burst is terminated, and a new device burst is issued. If rf_wait_en_r is cleared, rf_row_detect_en_r is recommended to set.
rf_cre_en	[17]	RW	1'b0	rf_cre_en 0: normal access 1: configuration register access
rf_cre_mode	[16]	RW	1'b0	rf_cre_mode 0: auto-controlled CRE 1: force-controlled CRE
rf_cre_pol	[15]	RW	1'b0	rf_cre_pol 0: active-HIGH 1: active-LOW
rf_wait_pol	[14]	RW	1'b1	rf_wait_pol 0: active low 1: active high
rf_wait_en_w	[13]	RW	1'b0	rf_wait_en_w Burst Write WAIT enable
rf_wait_en_r	[12]	RW	1'b0	rf_wait_en_r Burst read WAIT enable
rf_burst_mode_w	[11]	RW	1'b1	rf_burst_mode_w Burst write mode: 0: wrap 1: increase
rf_burst_length_w	[10:8]	RW	3'h7	rf_burst_length_w Burst write length: 0: reserved 1: 4 16-bit 2: 8 16-bit

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
				3: 16 16-bit 4: 32 16-bit 5: reserved 6: reserved 7: continuous
rf_burst_mode_r	[7]	RW	1'b1	rf_burst_mode_r Burst read mode: 0: wrap 1: increase
rf_burst_length_r	[6:4]	RW	3'h7	rf_burst_length_r Burst read length: 0: reserved 1: 4 16-bit 2: 8 16-bit 3: 16 16-bit 4: 32 16-bit 5: reserved 6: reserved 7: continuous
rf_mode_w	[3:2]	RW	2'h0	rf_mode_w 2'b00: asynchronous single-mode write 2'b01: reserved 2'b10: synchronous single-mode write 2'b11: synchronous burst-mode write
rf_mode_r	[1:0]	RW	2'h0	rf_mode_r 2'b00: asynchronous single-mode read 2'b01: asynchronous page-mode read 2'b10: synchronous single-mode read 2'b11: synchronous burst-mode read

SMC_CFG1_CSx

Description: SMC CSx control register
This register is used to configure general information for external memory CSx.
Each CS has an independent registers.

0x1044 0x1054 0x1064 0x1074			SMC CS0 control register 1 (Reset 0x0153FFFF) SMC CS1 control register 1 (Reset 0x0153FFFF) SMC CS2 control register 1 (Reset 0x0153FFFF) SMC CS3 control register 1 (Reset 0x0153FFFF)									SMC_CFG1_CS0 SMC_CFG1_CS1 SMC_CFG1_CS2 SMC_CFG1_CS3			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	rf_t_first_w [4]	rf_t_first_r [4]	rf_t_sample_phase_w	rf_t_sample_phase_r	rf_t_wait_dly_w		rf_t_wait_dly_r		rf_t_sample_dly_w		rf_t_sample_dly_r		rf_t_sample_stp			
Type	RW	RW	RW	RW	RW		RW		RW		RW		RW			
Reset	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rf_t_next_w				rf_t_first_w [3:0]				rf_t_next_r				rf_t_first_r [3:0]			
Type	RW				RW				RW				RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
rf_t_first_w [4]	[31]	RW	1'b0	rf_t_first_w [4] For write operation: First data delay – bit 4
rf_t_first_r [4]	[30]	RW	1'b0	rf_t_first_r [4] For read operation: First data delay – bit 4
rf_t_sample_phase_w	[29]	RW	1'b0	rf_t_sample_phase_w For write operation: In HCLK/2 mode, it's used to select sample phase. In HCLK mode, it's not used.
rf_t_sample_phase_r	[28]	RW	1'b0	rf_t_sample_phase_r For read operation: In HCLK/2 mode, it's used to select sample phase. In HCLK mode, it's not used.
rf_t_wait_dly_w	[27:26]	RW	2'h0	rf_t_wait_dly_w For write operation: It's the delay cycle between input WAIT and output data
rf_t_wait_dly_r	[25:24]	RW	2'h1	rf_t_wait_dly_r For read operation: It's the delay cycle between input WAIT and input data
rf_t_sample_dly_w	[23:22]	RW	2'h1	rf_t_sample_dly_w For write operation: It's the delay cycle of input WAIT sample logic
rf_t_sample_dly_r	[21:20]	RW	2'h1	rf_t_sample_dly_r For read operation: It's the delay cycle of input data and WAIT sample

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
				logic
rf_t_sample_stp	[19:16]	RW	4'h3	rf_t_sample_stp Input data and WAIT sample setup time. It's the delay cycle from CE# active to sample start. For SDR, it's used to mask WAIT high-Z state. For DDR, it's used to mask WAIT and DQS high-Z state.
rf_t_next_w	[15:12]	RW	4'hF	rf_t_next_w For write operation: Next data delay
rf_t_first_w [3:0]	[11:8]	RW	4'hF	rf_t_first_w [3:0] For write operation: First data delay – bit 0-3
rf_t_next_r	[7:4]	RW	4'hF	rf_t_next_r For read operation: Next data delay
rf_t_first_r [3:0]	[3:0]	RW	4'hF	rf_t_first_r [3:0] For read operation: First data delay – bit 0-3

SMC_CFG2_CSx

Description: SMC CSx control register
This register is used to configure general information for external memory CSx.
Each CS has an independent registers.

0x1048 0x1058 0x1068 0x1078	SMC CS0 control register 2 (Reset 0x10A0744F) SMC CS1 control register 2 (Reset 0x10A0744F) SMC CS2 control register 2 (Reset 0x10A0744F) SMC CS3 control register 2 (Reset 0x10A0744F)	SMC_CFG2_CS0 SMC_CFG2_CS1 SMC_CFG2_CS2 SMC_CFG2_CS3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rf_t_adv_stp_w			rf_t_adv_stp_r			rf_t_adv_mode_w	rf_t_adv_mode_r	rf_t_adv_wdt_w		rf_t_adv_wdt_r		rf_t_ce_hld_w	rf_t_ce_hld_r	rf_t_ce_stp_w	rf_t_ce_stp_r
Type	RW			RW			RW	RW	RW		RW		RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	rf_t_we_wdt_w				rf_t_data_oe_hld_w	rf_t_we_stp_w			rf_t_oe_hld_r	rf_t_oe_stp_r			rf_t_adswt_w		rf_t_adswt_r	
Type	RW				RW	RW			RW	RW			RW		RW	
Reset	0	1	1	1	0	1	0	0	0	1	0	0	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
rf_t_adv_stp_w	[31:29]	RW	3'h0	rf_t_adv_stp_w For write operation: It's the delay cycle from access start to ADV# low Note: this registers is used only if rf_t_adv_mode_w is cleared
rf_t_adv_stp_r	[28:26]	RW	3'h0	rf_t_adv_stp_r For read operation: It's the delay cycle from access start to ADV# low Note: this registers is used only if rf_t_adv_mode_r is cleared
rf_t_adv_mode_w	[25]	RW	1'b0	rf_t_adv_mode_w For write operation: ADV# timing control mode 0: ADV# timing is controlled by rf_t_adv_wdt_w 1: ADV# is same with CE#
rf_t_adv_mode_r	[24]	RW	1'b0	rf_t_adv_mode_r For read operation: ADV# timing control mode 0: ADV# timing is controlled by rf_t_adv_wdt_r 1: ADV# is same with CE#
rf_t_adv_wdt_w	[23:22]	RW	2'h2	rf_t_adv_wdt_w For write operation: It's the width cycle of ADV# low Note: this registers is used only if rf_t_adv_mode_w is cleared
rf_t_adv_wdt_r	[21:20]	RW	2'h2	rf_t_adv_wdt_r For read operation: It's the width cycle of ADV# low Note: this registers is used only if rf_t_adv_mode_r is cleared
rf_t_ce_hld_w	[19]	RW	1'b0	rf_t_ce_hld_w For write operation: It's the delay cycle from CE# high to access end Note, this register must be configured to 0, if current

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
				CS is not in asynchronous single mode.
rf_t_ce_hld_r	[18]	RW	1'b0	rf_t_ce_hld_r For read operation: It's the delay cycle from CE# high to access end Note, this register must be configured to 0, if current CS is not in asynchronous single mode.
rf_t_ce_stp_w	[17]	RW	1'b0	rf_t_ce_stp_w For write operation: It's the delay cycle from access start to CE# low
rf_t_ce_stp_r	[16]	RW	1'b0	rf_t_ce_stp_r For read operation: It's the delay cycle from access start to CE# low
rf_t_we_wdt_w	[15:12]	RW	4'h7	rf_t_we_wdt_w For write operation: It's the width cycle of WE# low
rf_t_data_oe_hld_w	[11]	RW	1'b0	rf_t_data_oe_hld_w For write operation: It's the delay cycle from CE# high to data output high-Z
rf_t_we_stp_w	[10:8]	RW	3'h4	rf_t_we_stp_w For write operation: It's the delay cycle from access start to WE# low
rf_t_oe_hld_r	[7]	RW	1'b0	rf_t_oe_hld_r For read operation: It's the delay cycle from OE# high to access end Note, this register must be configured to 0, if current CS is not in asynchronous single mode.
rf_t_oe_stp_r	[6:4]	RW	3'h4	rf_t_oe_stp_r For read operation: It's the delay cycle from access start to OE# low
rf_t_adswt_w	[3:2]	RW	2'h3	rf_t_adswt_w For write operation: It's the delay cycle from access start to address/data switch point Only used for ADM
rf_t_adswt_r	[1:0]	RW	2'h3	rf_t_adswt_r For read operation: It's the delay cycle from access start to address/data switch point Only used for ADM

SMC_CFG3_CSx

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Description: SMC CSx control register
This register is used to configure general information for external memory CSx.
Each CS has an independent registers.

0x104C 0x105C 0x106C 0x107C			SMC CS0 control register 3 (Reset 0x10000000) SMC CS1 control register 3 (Reset 0x10000000) SMC CS2 control register 3 (Reset 0x10000000) SMC CS3 control register 3 (Reset 0x10000000)										SMC_CFG3_CS0 SMC_CFG3_CS1 SMC_CFG3_CS2 SMC_CFG3_CS3			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rf_ahb_wbuf32_en			rf_ahb_rbuf_en			rf_t_sample_dly_ddr		rf_aadmux_addr_high							
Type	RW			RW			RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rf_ta_we_wdt		rf_ta_oe_wdt		rf_ta_adv_wdt_w		rf_ta_adv_wdt_r		rf_ta_we_stp	rf_ta_oe_stp	rf_ta_adv_stp_w	rf_ta_adv_stp_r	rf_ta_aadswt_w		rf_ta_aadswt_r	
Type	RW		RW		RW		RW		RW	RW	RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
rf_ahb_wbuf32_en	[31:29]	RW	3'h0	rf_ahb_wbuf32_en This filed indicates the select between 16-bit write buffer and 32-bit write buffer bit-2 for WORD bit-1 for HALF bit-0 for BYTE 0: 16-bit write buffer 1: 32-bit write buffer It's recommended that: For SDR, all are configured to 0 For DDR, all are configured to 1
rf_ahb_rbuf_en	[28:26]	RW	3'h0	rf_ahb_rbuf_en This filed indicates the select between direct read and buffered read bit-2 for WORD bit-1 for HALF bit-0 for BYTE 0: direct read 1: buffered read

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
				It's recommended that: For SDR, WORD and HALF are configured to 0, and BYTE can be 1 or 0. For DDR, WORD are configured to 0, and HALF and BYTE are configured to 1.
rf_t_sample_dly_ddr	[25:24]	RW	2'h0	rf_t_sample_dly_ddr For DDR, it's the delay cycle of input data sample logic
rf_aadmux_addr_high	[23:16]	RW	8'h0	rf_aadmux_addr_high For AADMUX, this field indicates the high bits on DQ when output the address [MAX:16].
rf_ta_we_wdt	[15:14]	RW	2'h0	rf_ta_we_wdt For AADMUX read and write, this filed indicates the first pulse width on WE#
rf_ta_oe_wdt	[13:12]	RW	2'h0	rf_ta_oe_wdt For AADMUX read and write, this filed indicates the first pulse width on OE#
rf_ta_adv_wdt_w	[11:10]	RW	2'h0	rf_ta_adv_wdt_w For AADMUX write, this filed indicates the first pulse width on ADV#
rf_ta_adv_wdt_r	[9:8]	RW	2'h0	rf_ta_adv_wdt_r For AADMUX read, this filed indicates the first pulse width on ADV#
rf_ta_we_stp	[7]	RW	1'b0	rf_ta_we_stp For AADMUX read and write, this filed indicates the cycle from CE# low to first WE# low
rf_ta_oe_stp	[6]	RW	1'b0	rf_ta_oe_stp For AADMUX read and write, this filed indicates the cycle from CE# low to first OE# low
rf_ta_adv_stp_w	[5]	RW	1'b0	rf_ta_adv_stp_w For AADMUX write, this filed indicates the cycle from CE# low to first ADV# low
rf_ta_adv_stp_r	[4]	RW	1'b0	rf_ta_adv_stp_r For AADMUX read, this filed indicates the cycle from CE# low to first ADV# low
rf_ta_aadswt_w	[3:2]	RW	2'h0	rf_ta_aadswt_w For AADMUX write, this filed indicates the cycle from CE# low to first address switch
rf_ta_aadswt_r	[1:0]	RW	2'h0	rf_ta_aadswt_r For AADMUX read, this filed indicates the cycle from CE# low to first address switch

Application Notes

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SMC Configurations

pSRAM or Nor-Flash Asynchronous Single Mode

Condition:
pSRAM or Nor-Flash
ADP or ADM or AADM
Asynchronous single mode
Suppose memory is connected on CS1

ADP:

```
0x10    --      0x11110000
0x04    --      0x10000010
0x50    --      0x10104FF0
0x54    --      0x0151F0F0    + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58    --      0x10000000    + (rf_t_adv_width_w<<22)
                                    + (rf_t_adv_width_r<<20)
                                    + (rf_t_we_width_w<<12)
                                    + (rf_t_we_stp_w<<8)
0x5C    --      0x10000000
```

ADM:

```
0x10    --      0x11110000
0x04    --      0x10000010
0x50    --      0x10904FF0
0x54    --      0x0151F0F0    + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58    --      0x10000000    + (rf_t_adv_width_w<<22)
                                    + (rf_t_adv_width_r<<20)
                                    + (rf_t_we_width_w<<12)
                                    + (rf_t_we_stp_w<<8)
                                    + (rf_t_oe_stp_r<<4)
                                    + (rf_t_adswt_w<<2)
                                    + (rf_t_adswt_r<<0)
0x5C    --      0x10000000
```

AADM:

```
0x10    --      0x11110000
0x04    --      0x10000010
0x50    --      0x02904FF0
0x54    --      0x0151F0F0    + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58    --      0x10000000    + (rf_t_adv_stp_w<<29)
                                    + (rf_t_adv_stp_r<<26)
                                    + (rf_t_adv_width_w<<22)
                                    + (rf_t_adv_width_r<<20)
```


This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
+ (rf_t_oe_stp_r<<4)
+ (rf_t_adswt_w<<2)
+ (rf_t_adswt_r<<0)

0x5C -- 0x10000000 + (rf_ta_oe_wdt<<12)
+ (rf_ta_adv_width_w<<10)
+ (rf_ta_adv_width_r<<8)
+ (rf_ta_aadswt_w<<2)
+ (rf_ta_aadswt_r<<0)

Description:

rf_t_first_w: writing operation cycle time, also is, CE# low time. See device spec for this time. rf_t_first_w = [Time / T_cycle] + 1. Time is spec-defined time value. T_cycle is HCLK cycle time.

rf_t_first_r: reading operation cycle time, also is, CE# low time. See device spec for this time. rf_t_first_r = [(Time + T_delay) / T_cycle] + 1. T_delay is on-chip delay time, and it can be set to 11ns.

rf_t_adv_width_w: ADV# low width for writing operation. See device spec for this time. rf_t_adv_width_w = [Time / T_cycle] + 1.

rf_t_adv_width_r: ADV# low width for reading operation. See device spec for this time. rf_t_adv_width_r = [Time / T_cycle] + 1.

rf_t_we_width_w: WE# low width for writing operation. See device spec for this time. rf_t_we_width_w = [Time / T_cycle] + 1.

rf_t_we_stp_w: CE# low to WE# low time for writing operation. See device spec for this time. rf_t_we_stp_w = [Time / T_cycle] + 1.

rf_t_oe_stp_r: CE# low to OE# low time for reading operation. See device spec for this time. rf_t_oe_stp_r = [Time / T_cycle] + 1.

rf_t_adswt_w: CE# low to Address/Data switching time for writing operation. See device spec for this time. rf_t_adswt_w = [Time / T_cycle] + 1.

rf_t_adswt_r: CE# low to Address/Data switching time for reading operation. See device spec for this time. rf_t_adswt_r = [Time / T_cycle] + 1.

Note1: rf_t_oe_stp_r, rf_t_adswt_r and rf_t_adswt_w can be set the same value, and they should be larger than rf_t_adv_width_r and rf_t_adv_width_w.

pSRAM or Nor-Flash Asynchronous Page Mode

Condition:

pSRAM or Nor-Flash

ADP

Asynchronous page mode

Suppose memory is connected on CS1

ADP:

0x10 -- 0x11110000

0x04 -- 0x10000000

0x50 -- 0x10104F01 + (rf_burst_length_r<<4)

0x54 -- 0x0151F000 + (rf_t_first_w<<8)
+ (rf_t_next_r<<4)
+ (rf_t_first_r<<0)

0x58 -- 0x01100000 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

+ (rf_t_we_stp_w<<8)

0x5C -- 0x10000000

ADM:

ADM device cannot support asynchronous page mode.

Description:

rf_burst_length_r: page size. See device spec for page size.

rf_t_first_w: writing operation cycle time, also is, CE# low time. See device spec for this time. rf_t_first_w = [Time / T_cycle] + 1. Time is spec-defined time value. T_cycle is HCLK cycle time.

rf_t_next_r: reading operation intra-page access time. See device spec for this time. rf_t_next_r = [(Time + T_delay) / T_cycle] + 1. T_delay is on-chip delay time, and it can be set to 11ns.

rf_t_first_r: reading operation first access time. See device spec for this time. rf_t_first_r = [(Time + T_delay) / T_cycle] + 1. T_delay is on-chip delay time, and it can be set to 11ns.

rf_t_adv_width_w: ADV# low width for writing operation. See device spec for this time. rf_t_adv_width_w = [Time / T_cycle] + 1.

rf_t_we_width_w: WE# low width for writing operation. See device spec for this time. rf_t_we_width_w = [Time / T_cycle] + 1.

rf_t_we_stp_w: CE# low to WE# low time for writing operation. See device spec for this time. rf_t_we_stp_w = [Time / T_cycle] + 1.

pSRAM Synchronous Burst SDR Mode

Condition:

pSRAM

ADP or ADM or AADM

Synchronous burst SDR mode

HCLK or HCLK/2

HCLK_2x used or not used

Read WAIT used or not

Write WAIT used or not

Suppose memory is connected on CS1

ADP, HCLK, HCLK_2x not used,

Variable latency, Read WAIT used, Write WAIT used:

0x10 -- 0x111111E0

0x20 -- 0x10000080

0x24 -- 0x10000080

0x04 -- 0x10000010

0x50 -- 0x10003FFF + (rf_row_length<<20)
+ (rf_row_detect_en_w<<19)
+ (rf_row_detect_en_r<<18)

0x54 -- 0x0152FFFF (or 0x0151FFFF)

0x58 -- 0x10501000

0x5C -- 0x10000000 (or 0x04000000)

0x10 -- 0x111110E0

ADM, HCLK, HCLK_2x not used,

Variable latency, Read WAIT used, Write WAIT used:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x10 -- 0x111111E0
0x20 -- 0x10000080
0x24 -- 0x10000080
0x04 -- 0x10000010
0x50 -- 0x10803FFF + (rf_row_length<<20)
+ (rf_row_detect_en_w<<19)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x0152FFFF (or 0x0151FFFF)
0x58 -- 0x10501015
0x5C -- 0x10000000 (or 0x04000000)
0x10 -- 0x111110E0

ADP, HCLK, HCLK_2x used,
Variable latency, Read WAIT used, Write WAIT used:
0x10 -- 0x111111C0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000017
0x50 -- 0x10003FFF + (rf_row_length<<20)
+ (rf_row_detect_en_w<<19)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x0102FFFF (or 0x0101FFFF)
0x58 -- 0x10501000
0x5C -- 0x10000000 (or 0x04000000)
0x10 -- 0x111110C0

ADM, HCLK, HCLK_2x used,
Variable latency, Read WAIT used, Write WAIT used:
0x10 -- 0x111111C0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000017
0x50 -- 0x10803FFF + (rf_row_length<<20)
+ (rf_row_detect_en_w<<19)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x0102FFFF (or 0x0101FFFF)
0x58 -- 0x10501015
0x5C -- 0x10000000 (or 0x04000000)
0x10 -- 0x111110C0

AADM, HCLK, HCLK_2x used,
Variable latency, Read WAIT used, Write WAIT used:
0x10 -- 0x111111C0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000017
0x50 -- 0x02803FFF + (rf_row_length<<20)
+ (rf_row_detect_en_w<<19)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

+ (rf_row_detect_en_r<<18)
0x54 -- 0x0102FFFF
0x58 -- 0x24501125
0x5C -- 0x10001505
0x10 -- 0x111110C0

ADP, HCLK, HCLK_2x not used,
Variable latency, Read WAIT used, Write WAIT not used:
0x10 -- 0x111111E0
0x20 -- 0x10000080
0x24 -- 0x10000080
0x04 -- 0x10000010
0x50 -- 0x10081FFF + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x015210FF + (rf_t_first_w<<8)
0x58 -- 0x10501000
0x5C -- 0x10000000
0x10 -- 0x111110E0

ADM, HCLK, HCLK_2x not used,
Variable latency, Read WAIT used, Write WAIT not used:
0x10 -- 0x111111E0
0x20 -- 0x10000080
0x24 -- 0x10000080
0x04 -- 0x10000010
0x50 -- 0x10881FFF + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x015210FF + (rf_t_first_w<<8)
0x58 -- 0x10501015
0x5C -- 0x10000000
0x10 -- 0x111110E0

ADP, HCLK, HCLK_2x used,
Variable latency, Read WAIT used, Write WAIT not used:
0x10 -- 0x111111C0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000017
0x50 -- 0x10081FFF + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x010210FF + (rf_t_first_w<<8)
0x58 -- 0x10501000
0x5C -- 0x10000000
0x10 -- 0x111110C0

ADM, HCLK, HCLK_2x used,
Variable latency, Read WAIT used, Write WAIT not used:
0x10 -- 0x111111C0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000017
0x50 -- 0x10881FFF + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x010210FF + (rf_t_first_w<<8)
0x58 -- 0x10501015
0x5C -- 0x10000000
0x10 -- 0x111110C0

AADM, HCLK, HCLK_2x used,
Variable latency, Read WAIT used, Write WAIT not used:
0x10 -- 0x111111C0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000017
0x50 -- 0x02881FFF + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x010210FF + (rf_t_first_w<<8)
0x58 -- 0x24501125
0x5C -- 0x10001505
0x10 -- 0x111110C0

ADP, HCLK, HCLK_2x not used,
Fixed latency, Read WAIT not used, Write WAIT not used:
0x10 -- 0x111111E0
0x20 -- 0x10000080
0x24 -- 0x10000080
0x04 -- 0x10000010
0x50 -- 0x100C0FFF + (rf_row_length<<20)
0x54 -- 0x01521010 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58 -- 0x10501000
0x5C -- 0x10000000
0x10 -- 0x111110E0

ADM, HCLK, HCLK_2x not used,
Fixed latency, Read WAIT not used, Write WAIT not used:
0x10 -- 0x111111E0
0x20 -- 0x10000080
0x24 -- 0x10000080
0x04 -- 0x10000010
0x50 -- 0x108C0FFF + (rf_row_length<<20)
0x54 -- 0x01521010 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58 -- 0x10501015
0x5C -- 0x10000000
0x10 -- 0x111110E0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

ADP, HCLK, HCLK_2x used,
Fixed latency, Read WAIT not used, Write WAIT not used:

```
0x10    --      0x111111C0
0x20    --      0x10000000
0x24    --      0x10000000
0x04    --      0x10000017
0x50    --      0x100C0FFF   + (rf_row_length<<20)
0x54    --      0x01021010   + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58    --      0x10501000
0x5C    --      0x10000000
0x10    --      0x111110C0
```

ADM, HCLK, HCLK_2x used,
Fixed latency, Read WAIT not used, Write WAIT not used:

```
0x10    --      0x111111C0
0x20    --      0x10000000
0x24    --      0x10000000
0x04    --      0x10000017
0x50    --      0x108C0FFF   + (rf_row_length<<20)
0x54    --      0x01021010   + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58    --      0x10501015
0x5C    --      0x10000000
0x10    --      0x111110C0
```

AADM, HCLK, HCLK_2x used,
Fixed latency, Read WAIT not used, Write WAIT not used:

```
0x10    --      0x111111C0
0x20    --      0x10000000
0x24    --      0x10000000
0x04    --      0x10000017
0x50    --      0x028C0FFF   + (rf_row_length<<20)
0x54    --      0x01021010   + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58    --      0x24501125
0x5C    --      0x10001505
0x10    --      0x111110C0
```

ADP, HCLK/2, HCLK_2x not used,
Variable latency, Read WAIT used, Write WAIT used:

```
0x10    --      0x111121F0
0x20    --      0x10000000
0x24    --      0x10000080
0x04    --      0x10000010
0x50    --      0x10003FFF   + (rf_row_length<<20)
```


This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

+ (rf_row_detect_en_w<<19)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x0A52FFFF
0x58 -- 0x10A02000
0x5C -- 0x10000000
0x10 -- 0x111120F0

ADM, HCLK/2, HCLK_2x not used,
Variable latency, Read WAIT used, Write WAIT used:
0x10 -- 0x111121F0
0x20 -- 0x10000000
0x24 -- 0x10000080
0x04 -- 0x10000010
0x50 -- 0x10803FFF + (rf_row_length<<20)
+ (rf_row_detect_en_w<<19)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x0A52FFFF
0x58 -- 0x10A0202A
0x5C -- 0x10000000
0x10 -- 0x111120F0

ADP, HCLK/2, HCLK_2x used,
Variable latency, Read WAIT used, Write WAIT used:
0x10 -- 0x111121D0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000015
0x50 -- 0x10003FFF + (rf_row_length<<20)
+ (rf_row_detect_en_w<<19)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x0A02FFFF
0x58 -- 0x10A02000
0x5C -- 0x10000000
0x10 -- 0x111120D0

ADM, HCLK/2, HCLK_2x used,
Variable latency, Read WAIT used, Write WAIT used:
0x10 -- 0x111121D0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000015
0x50 -- 0x10803FFF + (rf_row_length<<20)
+ (rf_row_detect_en_w<<19)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x0A02FFFF
0x58 -- 0x10A0202A
0x5C -- 0x10000000
0x10 -- 0x111120D0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

ADP, HCLK/2, HCLK_2x not used,
Variable latency, Read WAIT used, Write WAIT not used:
0x10 -- 0x111121F0
0x20 -- 0x10000000
0x24 -- 0x10000080
0x04 -- 0x10000010
0x50 -- 0x10081FFF + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x0A5220FF + (rf_t_first_w<<8)
0x58 -- 0x10A02000
0x5C -- 0x10000000
0x10 -- 0x111120F0

ADM, HCLK/2, HCLK_2x not used,
Variable latency, Read WAIT used, Write WAIT not used:
0x10 -- 0x111121F0
0x20 -- 0x10000000
0x24 -- 0x10000080
0x04 -- 0x10000010
0x50 -- 0x10881FFF + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x0A5220FF + (rf_t_first_w<<8)
0x58 -- 0x10A0202A
0x5C -- 0x10000000
0x10 -- 0x111120F0

ADP, HCLK/2, HCLK_2x used,
Variable latency, Read WAIT used, Write WAIT not used:
0x10 -- 0x111121D0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000015
0x50 -- 0x10081FFF + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x0A0220FF + (rf_t_first_w<<8)
0x58 -- 0x10A02000
0x5C -- 0x10000000
0x10 -- 0x111120D0

ADM, HCLK/2, HCLK_2x used,
Variable latency, Read WAIT used, Write WAIT not used:
0x10 -- 0x111121D0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000015
0x50 -- 0x10881FFF + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x54 -- 0x0A0220FF + (rf_t_first_w<<8)
0x58 -- 0x10A0202A
0x5C -- 0x10000000
0x10 -- 0x111120D0

ADP, HCLK/2, HCLK_2x not used,
Fixed latency, Read WAIT not used, Write WAIT not used:
0x10 -- 0x111121F0
0x20 -- 0x10000000
0x24 -- 0x10000080
0x04 -- 0x10000010
0x50 -- 0x100C0FFF + (rf_row_length<<20)
0x54 -- 0x0A522020 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58 -- 0x10A02000
0x5C -- 0x10000000
0x10 -- 0x111120F0

ADM, HCLK/2, HCLK_2x not used,
Fixed latency, Read WAIT not used, Write WAIT not used:
0x10 -- 0x111121F0
0x20 -- 0x10000000
0x24 -- 0x10000080
0x04 -- 0x10000010
0x50 -- 0x108C0FFF + (rf_row_length<<20)
0x54 -- 0x0A522020 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58 -- 0x10A0202A
0x5C -- 0x10000000
0x10 -- 0x111120F0

ADP, HCLK/2, HCLK_2x used,
Fixed latency, Read WAIT not used, Write WAIT not used:
0x10 -- 0x111121D0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000015
0x50 -- 0x100C0FFF + (rf_row_length<<20)
0x54 -- 0x0A022020 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58 -- 0x10A02000
0x5C -- 0x10000000
0x10 -- 0x111120D0

ADM, HCLK/2, HCLK_2x used,
Fixed latency, Read WAIT not used, Write WAIT not used:
0x10 -- 0x111121D0
0x20 -- 0x10000000

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x24 -- 0x10000000
0x04 -- 0x10000015
0x50 -- 0x108C0FFF + (rf_row_length<<20)
0x54 -- 0x0A022020 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58 -- 0x10A0202A
0x5C -- 0x10000000
0x10 -- 0x111120D0

Description:

rf_row_detect_en_r: for reading, if device cannot support row boundary crossing, this bit should be set to stop reading burst at row boundary.

rf_row_detect_en_w: for writing, if device cannot support row boundary crossing, this bit should be set to stop writing burst at row boundary.

rf_row_length: See device spec for this information. If either rf_row_detect_en_r or rf_row_detect_en_w is set, rf_row_lendth should be configured.

rf_t_first_w: first latency of writing burst operation. This parameter depends on device wait state cycles. If device wait state cycles are configured to N, For HCLK mode, rf_t_first_w = N + 1; For HCLK/2 mode, rf_t_first_w = 2*N + 2.

rf_t_first_r: first latency of reading burst operation. This parameter depends on device wait state cycles. If device wait state cycles are configured to N, For HCLK mode, rf_t_first_r = N + 2; For HCLK/2 mode, rf_t_first_r = 2*N + 2.

Note1: if WAIT valid depends on OE# low, rf_t_sample_stp = rf_t_oe_stp_r + 1, otherwise, rf_t_sample_stp = 1. Based on current spec, Spansion FLASH and ST FLASH have this dependency, and pSRAM doesn't have it.

Note2: rf_t_sample_stp should be used to mask WAIT High-Z state, so this value should be more than the time from CE# low to WAIT low-Z. Based on current spec, the maximum value is 7.5ns, so if clock frequency is less than 133MHz, rf_t_sample_stp can be configure to 1, otherwise, it must be 2.

Note3: rf_ahb_rbuf_en[0] indicates BYTE reading is through direct mode or buffered mode. Buffered reading improves burst efficiency but lead to bigger first latency. And direct read has smaller first latency but it breaks burst into single transaction because of lower speed of AHB than memory. Ether choice may be acceptable since most of BYTE transactions are single.

pSRAM Synchronous Burst DDR Mode

Condition:
pSRAM
ADP or ADM or AADM
Synchronous burst DDR mode
HCLK
HCLK_2x used
Read WAIT used or not
Write WAIT used or not
Suppose memory is connected on CS1

ADP,
Variable latency, Read WAIT used, Write WAIT used:
0x10 -- 0x111191C0
0x28 -- 0x10000000 + (delay value<<0)
0x2C -- 0x10000000 + (delay value<<0)
0x30 -- 0x10000000 + (delay value<<0)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x34 -- 0x10000000 + (delay value<<0)
0x38 -- 0x10000000 + (delay value<<0)
0x04 -- 0x10000017
0x50 -- 0x08003FFF + (rf_row_length<<20)
+ (rf_row_detect_en_w<<19)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x0202FFFF (or 0x0201FFFF)
0x58 -- 0x10501000
0x5C -- 0xED000000
0x10 -- 0x111190C0

ADM,
Variable latency, Read WAIT used, Write WAIT used:
0x10 -- 0x111191C0
0x28 -- 0x10000000 + (delay value<<0)
0x2C -- 0x10000000 + (delay value<<0)
0x30 -- 0x10000000 + (delay value<<0)
0x34 -- 0x10000000 + (delay value<<0)
0x38 -- 0x10000000 + (delay value<<0)
0x04 -- 0x10000017
0x50 -- 0x08803FFF + (rf_row_length<<20)
+ (rf_row_detect_en_w<<19)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x0202FFFF (or 0x0201FFFF)
0x58 -- 0x10501015
0x5C -- 0xED000000
0x10 -- 0x111190C0

AADM,
Variable latency, Read WAIT used, Write WAIT used:
0x10 -- 0x111191C0
0x28 -- 0x10000000 + (delay value<<0)
0x2C -- 0x10000000 + (delay value<<0)
0x30 -- 0x10000000 + (delay value<<0)
0x34 -- 0x10000000 + (delay value<<0)
0x38 -- 0x10000000 + (delay value<<0)
0x04 -- 0x10000017
0x50 -- 0x0A803FFF + (rf_row_length<<20)
+ (rf_row_detect_en_w<<19)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x0202FFFF (or 0x0201FFFF)
0x58 -- 0x24501125
0x5C -- 0xED001505
0x10 -- 0x111190C0

ADP,
Variable latency, Read WAIT used, Write WAIT not used:
0x10 -- 0x111191C0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x28 -- 0x10000000 + (delay value<<0)
0x2C -- 0x10000000 + (delay value<<0)
0x30 -- 0x10000000 + (delay value<<0)
0x34 -- 0x10000000 + (delay value<<0)
0x38 -- 0x10000000 + (delay value<<0)
0x04 -- 0x10000017
0x50 -- 0x08081FFF + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x020210FF + (rf_t_first_w<<8)
0x58 -- 0x10501000
0x5C -- 0xED000000
0x10 -- 0x111190C0

ADM,
Variable latency, Read WAIT used, Write WAIT not used:
0x10 -- 0x111191C0
0x28 -- 0x10000000 + (delay value<<0)
0x2C -- 0x10000000 + (delay value<<0)
0x30 -- 0x10000000 + (delay value<<0)
0x34 -- 0x10000000 + (delay value<<0)
0x38 -- 0x10000000 + (delay value<<0)
0x04 -- 0x10000017
0x50 -- 0x08881FFF + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x020210FF + (rf_t_first_w<<8)
0x58 -- 0x10501015
0x5C -- 0xED000000
0x10 -- 0x111190C0

AADM,
Variable latency, Read WAIT used, Write WAIT not used:
0x10 -- 0x111191C0
0x28 -- 0x10000000 + (delay value<<0)
0x2C -- 0x10000000 + (delay value<<0)
0x30 -- 0x10000000 + (delay value<<0)
0x34 -- 0x10000000 + (delay value<<0)
0x38 -- 0x10000000 + (delay value<<0)
0x04 -- 0x10000017
0x50 -- 0x0A881FFF + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x54 -- 0x020210FF + (rf_t_first_w<<8)
0x58 -- 0x24501125
0x5C -- 0xED001505
0x10 -- 0x111190C0

ADP,
Fixed latency, Read WAIT not used, Write WAIT not used:
0x10 -- 0x111191C0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x28 -- 0x10000000 + (delay value<<0)
0x2C -- 0x10000000 + (delay value<<0)
0x30 -- 0x10000000 + (delay value<<0)
0x34 -- 0x10000000 + (delay value<<0)
0x38 -- 0x10000000 + (delay value<<0)
0x04 -- 0x10000017
0x50 -- 0x080C0FFF + (rf_row_length<<20)
0x54 -- 0x02021010 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58 -- 0x10501000
0x5C -- 0xED000000
0x10 -- 0x111190C0

ADM,
Fixed latency, Read WAIT not used, Write WAIT not used:
0x10 -- 0x111191C0
0x28 -- 0x10000000 + (delay value<<0)
0x2C -- 0x10000000 + (delay value<<0)
0x30 -- 0x10000000 + (delay value<<0)
0x34 -- 0x10000000 + (delay value<<0)
0x38 -- 0x10000000 + (delay value<<0)
0x04 -- 0x10000017
0x50 -- 0x088C0FFF + (rf_row_length<<20)
0x54 -- 0x02021010 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58 -- 0x10501015
0x5C -- 0xED000000
0x10 -- 0x111190C0

AADM,
Fixed latency, Read WAIT not used, Write WAIT not used:
0x10 -- 0x111191C0
0x28 -- 0x10000000 + (delay value<<0)
0x2C -- 0x10000000 + (delay value<<0)
0x30 -- 0x10000000 + (delay value<<0)
0x34 -- 0x10000000 + (delay value<<0)
0x38 -- 0x10000000 + (delay value<<0)
0x04 -- 0x10000017
0x50 -- 0x0A8C0FFF + (rf_row_length<<20)
0x54 -- 0x02021010 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58 -- 0x24501125
0x5C -- 0xED001505
0x10 -- 0x111190C0

Description:
rf_row_detect_en_r: for reading, if device cannot support row boundary crossing, this bit should be set to stop reading burst at row boundary.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

rf_row_detect_en_w: for writing, if device cannot support row boundary crossing, this bit should be set to stop writing burst at row boundary.

rf_row_length: See device spec for this information. If either rf_row_detect_en_r or rf_row_detect_en_w is set, rf_row_lendth should be configured.

rf_t_first_w: first latency of writing burst operation. This parameter depends on device wait state cycles. If device wait state cycles are configured to N, rf_t_first_w = N. If rf_ddr_wdata_mode is 1 and rf_ddr_wdata_dly is 2, rf_t_first_w = N – 1.

rf_t_first_r: first latency of reading burst operation. This parameter depends on device wait state cycles. If device wait state cycles are configured to N, rf_t_first_r = N + 3.

Note1: rf_t_sample_stp should be used to mask WAIT High-Z state and reading DQS High-Z state, so this value should be more than the time from CE# low to WAIT low-Z, and also more than the time from CE# low to DQS low-Z during reading. Based on current spec, the maximum tCEW value is 7.5ns. But about DQS, related timing parameter is tCQLZ, which is from CLK rising to DQS low-Z. This parameter from Winbond is 3ns, and from Aptic is 7.5ns. So rf_t_sample_stp should be configured to 2 for Aptic and can be 1 for Winbond.

Note 2: SMC support two internal modes for write burst selected by rf_ddr_write_mode, only mode 0 is described in this chapter. For mode 1, other configurations are the same, except four parts. WAIT for write must not be used. rf_ddr_write_mode is 1. rf_ddr_write_dly is 2. rf_t_first_w should be N – 1 instead of N.

Nor-Flash Synchronous Burst SDR Mode

Condition:
Nor-Flash
ADP or ADM or AADM
Synchronous burst SDR mode
HCLK or HCLK/2
HCLK_2x used or not used
Read WAIT used or not
Suppose memory is connected on CS0

ADP, HCLK, HCLK_2x not used,
Variable latency, Read WAIT used:

```
0x10    --      0x111111E0
0x20    --      0x10000080
0x24    --      0x10000080
0x04    --      0x10000010
0x40    --      0x10001FF3    + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x44    --      0x0152F0FF    + (rf_t_first_w<<8)
0x48    --      0x10100000    + (rf_t_adv_width_w<<22)
                                    + (rf_t_we_width_w<<12)
                                    + (rf_t_we_stp_w<<8)
0x4C    --      0x10000000
0x10    --      0x111110E0
```

ADM, HCLK, HCLK_2x not used,
Variable latency, Read WAIT used:

```
0x10    --      0x111111E0
0x20    --      0x10000080
0x24    --      0x10000080
```


This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x04 -- 0x10000010
0x40 -- 0x10801FF3 + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x44 -- 0x0152F0FF + (rf_t_first_w<<8)
0x48 -- 0x10100011 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
+ (rf_t_adswt_w<<2)
0x4C -- 0x10000000
0x10 -- 0x111110E0

ADP, HCLK, HCLK_2x used,
Variable latency, Read WAIT used:
0x10 -- 0x111111C0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000017
0x40 -- 0x10001FF3 + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x44 -- 0x0102F0FF + (rf_t_first_w<<8)
0x48 -- 0x10100000 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
0x4C -- 0x10000000
0x10 -- 0x111110C0

ADM, HCLK, HCLK_2x used,
Variable latency, Read WAIT used:
0x10 -- 0x111111C0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000017
0x40 -- 0x10801FF3 + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x44 -- 0x0102F0FF + (rf_t_first_w<<8)
0x48 -- 0x10100011 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
+ (rf_t_adswt_w<<2)
0x4C -- 0x10000000
0x10 -- 0x111110C0

ADP, HCLK, HCLK_2x not used,
Fixed latency, Read WAIT not used:
0x10 -- 0x111111E0
0x20 -- 0x10000080
0x24 -- 0x10000080
0x04 -- 0x10000010

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x40 -- 0x10040FF3 + (rf_row_length<<20)
0x44 -- 0x0152F010 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x48 -- 0x10100000 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
0x4C -- 0x10000000
0x10 -- 0x111110E0

ADM, HCLK, HCLK_2x not used,
Fixed latency, Read WAIT not used:
0x10 -- 0x111111E0
0x20 -- 0x10000080
0x24 -- 0x10000080
0x04 -- 0x10000010
0x40 -- 0x10840FF3 + (rf_row_length<<20)
0x44 -- 0x0152F010 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x48 -- 0x10100011 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
+ (rf_t_adswt_w<<2)
0x4C -- 0x10000000
0x10 -- 0x111110E0

ADP, HCLK, HCLK_2x used,
Fixed latency, Read WAIT not used:
0x10 -- 0x111111C0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000017
0x40 -- 0x10040FF3 + (rf_row_length<<20)
0x44 -- 0x0102F010 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x48 -- 0x10100000 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
0x4C -- 0x10000000
0x10 -- 0x111110C0

ADM, HCLK, HCLK_2x used,
Fixed latency, Read WAIT not used:
0x10 -- 0x111111C0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000017
0x40 -- 0x10840FF3 + (rf_row_length<<20)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x44 -- 0x0102F010 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x48 -- 0x10100011 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
+ (rf_t_adswt_w<<2)
0x4C -- 0x10000000
0x10 -- 0x111110C0

ADP, HCLK/2, HCLK_2x not used,
Variable latency, Read WAIT used:
0x10 -- 0x111121F0
0x20 -- 0x10000000
0x24 -- 0x10000080
0x04 -- 0x10000010
0x40 -- 0x10001FF3 + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x44 -- 0x0A52F0FF + (rf_t_first_w<<8)
0x48 -- 0x10200000 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
0x4C -- 0x10000000
0x10 -- 0x111120F0

ADM, HCLK/2, HCLK_2x not used,
Variable latency, Read WAIT used:
0x10 -- 0x111121F0
0x20 -- 0x10000000
0x24 -- 0x10000080
0x04 -- 0x10000010
0x40 -- 0x10801FF3 + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x44 -- 0x0A52F0FF + (rf_t_first_w<<8)
0x48 -- 0x10200022 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
+ (rf_t_adswt_w<<2)
0x4C -- 0x10000000
0x10 -- 0x111120F0

ADP, HCLK/2, HCLK_2x used,
Variable latency, Read WAIT used:
0x10 -- 0x111121D0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000015
0x40 -- 0x10001FF3 + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x44 -- 0x0A02F0FF + (rf_t_first_w<<8)
0x48 -- 0x10200000 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
0x4C -- 0x10000000
0x10 -- 0x111120D0

ADM, HCLK/2, HCLK_2x used,
Variable latency, Read WAIT used:
0x10 -- 0x111121D0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000015
0x40 -- 0x10801FF3 + (rf_row_length<<20)
+ (rf_row_detect_en_r<<18)
0x44 -- 0x0A02F0FF + (rf_t_first_w<<8)
0x48 -- 0x10200022 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
+ (rf_t_adswt_w<<2)
0x4C -- 0x10000000
0x10 -- 0x111120D0

ADP, HCLK/2, HCLK_2x not used,
Fixed latency, Read WAIT not used:
0x10 -- 0x111121F0
0x20 -- 0x10000000
0x24 -- 0x10000080
0x04 -- 0x10000010
0x40 -- 0x10040FF3 + (rf_row_length<<20)
0x44 -- 0x0A52F020 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x48 -- 0x10200000 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
0x4C -- 0x10000000
0x10 -- 0x111120F0

ADM, HCLK/2, HCLK_2x not used,
Fixed latency, Read WAIT not used:
0x10 -- 0x111121F0
0x20 -- 0x10000000
0x24 -- 0x10000080
0x04 -- 0x10000010
0x40 -- 0x10840FF3 + (rf_row_length<<20)
0x44 -- 0x0A52F020 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x48 -- 0x10200022 + (rf_t_adv_width_w<<22)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
+ (rf_t_adswt_w<<2)

0x4C -- 0x10000000
0x10 -- 0x111120F0

ADP, HCLK/2, HCLK_2x used,
Fixed latency, Read WAIT not used:

0x10 -- 0x111121D0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000015
0x40 -- 0x10040FF3 + (rf_row_length<<20)
0x44 -- 0x0A02F020 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x48 -- 0x10200000 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
0x4C -- 0x10000000
0x10 -- 0x111120D0

ADM, HCLK/2, HCLK_2x used,
Fixed latency, Read WAIT not used:

0x10 -- 0x111121D0
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000015
0x40 -- 0x10840FF3 + (rf_row_length<<20)
0x44 -- 0x0A02F020 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x48 -- 0x10200022 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
+ (rf_t_adswt_w<<2)
0x4C -- 0x10000000
0x10 -- 0x111120D0

Description:

rf_row_detect_en_r: for reading, if device cannot support row boundary crossing, this bit should be set to stop reading burst at row boundary.

rf_row_length: See device spec for this information. If rf_row_detect_en_r is set, rf_row_lendth should be configured.

rf_t_first_w: writing operation cycle time, also is, CE# low time. See device spec for this time.
rf_t_first_w = [Time / T_cycle] + 1. Time is spec-defined time value. T_cycle is HCLK cycle time.

rf_t_first_r: first latency of reading burst operation. This parameter depends on device wait state cycles. If device wait state cycles are configured to N, For HCLK mode, rf_t_first_r = N + 2; For HCLK/2 mode, rf_t_first_r = 2*N + 2.

rf_t_adv_width_w: ADV# low width for writing operation. See device spec for this time.
rf_t_adv_width_w = [Time / T_cycle] + 1.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

rf_t_we_width_w: WE# low width for writing operation. See device spec for this time. rf_t_we_width_w = [Time / T_cycle] + 1.

rf_t_we_stp_w: CE# low to WE# low time for writing operation. See device spec for this time. rf_t_we_stp_w = [Time / T_cycle] + 1.

rf_t_adswt_w: CE# low to Address/Data switching time for writing operation. See device spec for this time. rf_t_adswt_w = [Time / T_cycle] + 1.

Note1: if WAIT valid depends on OE# low, rf_t_sample_stp = rf_t_oe_stp_r + 1, otherwise, rf_t_sample_stp = 1. Based on current spec, Spansion FLASH and ST FLASH have this dependency, and pSRAM doesn't have it.

Note2: rf_t_adswt_w should be larger than rf_t_adv_width_w.

DLL and Delay Line Configurations

Delay lines are configured by two methods. One is manual configuring and the other is DLL compensating. Each delay line can be selected in either mode independently. And DLL must be opened when any delay line is in DLL compensating mode.

Manual Configuring

DLL doesn't need opened. The delay step values of all delay lines can be configured directly.

DLL configuration:

0x08 -- 0x10000000 (it's default value)

Delay line configuration:

DLx -- 0x10000000 + (delay step value<<0)

DLx is from 0x20 to 0x3C. But only the delay lines that are used should be configured.

DLL Compensating

If any delay line is in DLL compensating mode, DLL must be opened. But even if DLL is opened and some of delay lines are in DLL compensating mode, other delay lines can still be configured in manual mode.

Delay line configuration:

DLx -- 0x10000100 + (delay percentage<<0)

DLL configuration:

0x08 -- 0x10000580 + (rf_dll_phase_interval<<16)
+ (rf_dll_cpst_thr<<12)
+ (rf_dll_auto_clr_en<<9)

0x08 -- 0x10000480 + (rf_dll_phase_interval<<16)
+ (rf_dll_cpst_thr<<12)
+ (rf_dll_auto_clr_en<<9)

Description:

delay percentage is (delay time) * 128 / (HCLK_2x cycle time)

rf_dll_phase_interval is recommended to be from 1 to 2.

rf_dll_cpst_thr is recommended to be from 2 to 4.

rf_dll_auto_clr_en indicates whether DLL is cleared automatically during chip sleep or not. If this bit is set, software doesn't need take care of DLL operation after chip waking up. Otherwise, software should restart DLL manually.

External Memory Configurations

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

CellularRAM CRE-Control

For CellularRAM, CRE pin is used to distinguish memory configuring with normal operations. SMC configuration is the same as normal operation mode configuration, except rf_cre_en is set to 1.

Software-Method

For some memories, a special transaction sequence may be used to program memory registers. User can refer to memory data sheet for the detailed sequence.

During software-method configuring, SMC configuration is the same as normal operation mode.

Address-Control for AADM

There is a special method for some AADM devices. CRE signal is issued on a high-bit of data bus in first address phase instead of separate CRE input.

In first address phase, some of high bits are unused because of memory size limitation, so these bits can be used to transform information like CRE, which makes hardware CRE pin saved.

SMC provides these unused high-bit in first address phase configurable – rf_aadmux_addr_high, so user can use these configurable registers to mark CRE writing.

The other configurations are the same as generic operations.

Initialization Examples

Example 1

Condition:

HCLK

HCLK_2x not used

CS0: ADP Nor-Flash, burst mode, WAIT used.

CS1: ADP CellularRAM, burst mode, WAIT used, CRE used

Configuration

Initialize SMC for configuring Nor-Flash and CellularRAM

```
0x10    --      0x11110000
0x20    --      0x10000000
0x24    --      0x10000000
0x04    --      0x10000010
0x40    --      0x10104FF0
0x44    --      0x0151F0F0    + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x48    --      0x10000000    + (rf_t_adv_width_w<<22)
                              + (rf_t_adv_width_r<<20)
                              + (rf_t_we_width_w<<12)
                              + (rf_t_we_stp_w<<8)
0x4C    --      0x10000000
0x50    --      0x10124FF0
0x54    --      0x0151F0F0    + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58    --      0x10000000    + (rf_t_adv_width_w<<22)
                              + (rf_t_adv_width_r<<20)
                              + (rf_t_we_width_w<<12)
```


This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

+ (rf_t_we_stp_w<<8)

0x5C -- 0x10000000

Configure Nor-Flash into burst mode

Configure CellularRAM into burst mode

Wait for about 40 cycles. For example, for(i=0;i<10;i++)

Initialize SMC for normal accessing

0x10 -- 0x111111E0
0x20 -- 0x10000080
0x24 -- 0x10000080
0x04 -- 0x10000010
0x40 -- 0x10101FF3
0x44 -- 0x0152F0FF + (rf_t_first_w<<8)
0x48 -- 0x10100000 + (rf_t_adv_width_w<<22)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
0x4C -- 0x10000000
0x50 -- 0x10103FFF
0x54 -- 0x0152FFFF
0x58 -- 0x10501000
0x5C -- 0x10000000
0x10 -- 0x111110E0

Example 2

Condition:
HCLK
HCLK_2x used
CS0: ADM Nor-Flash, burst mode, WAIT used.
CS1: ADM CellularRAM, burst mode, WAIT used, CRE used

Configuration

Initialize SMC for configuring Nor-Flash and CellularRAM

0x10 -- 0x11110000
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000010
0x40 -- 0x10904FF0
0x44 -- 0x0151F0F0 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x48 -- 0x10000000 + (rf_t_adv_width_w<<22)
+ (rf_t_adv_width_r<<20)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

```
                                    + (rf_t_oe_stp_r<<4)
                                    + (rf_t_adswt_w<<2)
                                    + (rf_t_adswt_r<<0)
0x4C    --      0x10000000
0x50    --      0x10924FF0
0x54    --      0x0151F0F0  + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58    --      0x10000000  + (rf_t_adv_width_w<<22)
                                    + (rf_t_adv_width_r<<20)
                                    + (rf_t_we_width_w<<12)
                                    + (rf_t_we_stp_w<<8)
                                    + (rf_t_oe_stp_r<<4)
                                    + (rf_t_adswt_w<<2)
                                    + (rf_t_adswt_r<<0)
0x5C    --      0x10000000
```

Configure Nor-Flash into burst mode

Configure CellularRAM into burst mode

Wait for about 40 cycles. For example, for(i=0;i<10;i++)

Initialize SMC for normal accessing

```
0x10    --      0x111111C0
0x20    --      0x10000000
0x24    --      0x10000000
0x04    --      0x10000017
0x40    --      0x10901FF3
0x44    --      0x0102F0FF  + (rf_t_first_w<<8)
0x48    --      0x10100011  + (rf_t_adv_width_w<<22)
                                    + (rf_t_we_width_w<<12)
                                    + (rf_t_we_stp_w<<8)
                                    + (rf_t_adswt_w<<2)
0x4C    --      0x10000000
0x50    --      0x10903FFF
0x54    --      0x0102FFFF
0x58    --      0x10501015
0x5C    --      0x10000000
0x10    --      0x111110C0
```

Example 3

Condition:
HCLK
HCLK_2x used
CS1: ADM CellularRAM, SDR burst mode, WAIT used, CRE used

Configuration

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Initialize SMC for configuring CellularRAM

```
0x10    --      0x11110000
0x20    --      0x10000000
0x24    --      0x10000000
0x04    --      0x10000010
0x50    --      0x10924FF0
0x54    --      0x0151F0F0    + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58    --      0x10000000    + (rf_t_adv_width_w<<22)
                                + (rf_t_adv_width_r<<20)
                                + (rf_t_we_width_w<<12)
                                + (rf_t_we_stp_w<<8)
                                + (rf_t_oe_stp_r<<4)
                                + (rf_t_adswt_w<<2)
                                + (rf_t_adswt_r<<0)
0x5C    --      0x10000000
```

Configure CellularRAM into burst mode

Wait for about 40 cycles. For example, for(i=0;i<10;i++)

Initialize SMC for normal accessing

```
0x10    --      0x111111C0
0x20    --      0x10000000
0x24    --      0x10000000
0x04    --      0x10000017
0x50    --      0x10903FFF
0x54    --      0x0102FFFF
0x58    --      0x10501015
0x5C    --      0x10000000
0x10    --      0x111110C0
```

Example 4

Condition:
CS1: ADM CellularRAM, DDR burst mode, Read WAIT used, Write WAIT not used
DLL not used

Configuration

Initialize SMC for configuring CellularRAM

```
0x10    --      0x11110000
0x04    --      0x10000010
0x50    --      0x10924FF0
0x54    --      0x0151F0F0    + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58    --      0x10000000    + (rf_t_adv_width_w<<22)
```


This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

+ (rf_t_adv_width_r<<20)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
+ (rf_t_oe_stp_r<<4)
+ (rf_t_adswt_w<<2)
+ (rf_t_adswt_r<<0)

0x5C -- 0x10000000

Configure CellularRAM into DDR burst mode

Wait for about 40 cycles. For example, for(i=0;i<10;i++)

Initialize SMC for normal accessing

0x10 -- 0x111191C0
0x28 -- 0x10000000 + (delay value<<0)
0x2C -- 0x10000000 + (delay value<<0)
0x30 -- 0x10000000 + (delay value<<0)
0x34 -- 0x10000000 + (delay value<<0)
0x38 -- 0x10000000 + (delay value<<0)
0x04 -- 0x10000017
0x50 -- 0x08881FFF + (rf_row_length<<20)
0x54 -- 0x020210FF + (rf_t_first_w<<8)
0x58 -- 0x10501015
0x5C -- 0xED000000
0x10 -- 0x111190C0

Example 5

Condition:
HCLK
HCLK_2x used
CS1: ADM CellularRAM, SDR burst mode, WAIT used, CRE used
DLL used

Configuration

Initialize SMC for configuring CellularRAM

0x10 -- 0x11110000
0x20 -- 0x10000000
0x24 -- 0x10000000
0x04 -- 0x10000010
0x50 -- 0x10924FF0
0x54 -- 0x0151F0F0 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58 -- 0x10000000 + (rf_t_adv_width_w<<22)
+ (rf_t_adv_width_r<<20)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

+ (rf_t_oe_stp_r<<4)
+ (rf_t_adswt_w<<2)
+ (rf_t_adswt_r<<0)

0x5C -- 0x10000000

Configure CellularRAM into burst mode

Wait for about 40 cycles. For example, for(i=0;i<10;i++)

Initialize DLL and delay lines

0x20 -- 0x10000100 + (delay percentage<<0)
0x24 -- 0x10000100 + (delay percentage<<0)
0x08 -- 0x10000580 + (rf_dll_phase_interval<<16)
+ (rf_dll_cpst_thr<<12)
+ (rf_dll_auto_clr_en<<9)
0x08 -- 0x10000480 + (rf_dll_phase_interval<<16)
+ (rf_dll_cpst_thr<<12)
+ (rf_dll_auto_clr_en<<9)

Initialize SMC for normal accessing

0x10 -- 0x111111C0
0x04 -- 0x10000017
0x50 -- 0x10903FFF
0x54 -- 0x0102FFFF
0x58 -- 0x10501015
0x5C -- 0x10000000
0x10 -- 0x111110C0

Example 6

Condition:
CS1: ADM CellularRAM, DDR burst mode, Read WAIT used, Write WAIT not used
DLL used

Configuration

Initialize SMC for configuring CellularRAM

0x10 -- 0x11110000
0x04 -- 0x10000010
0x50 -- 0x10924FF0
0x54 -- 0x0151F0F0 + (rf_t_first_w<<8)
+ (rf_t_first_r<<0)
0x58 -- 0x10000000 + (rf_t_adv_width_w<<22)
+ (rf_t_adv_width_r<<20)
+ (rf_t_we_width_w<<12)
+ (rf_t_we_stp_w<<8)
+ (rf_t_oe_stp_r<<4)
+ (rf_t_adswt_w<<2)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

+ (rf_t_adswt_r<<0)

0x5C -- 0x10000000

Configure CellularRAM into DDR burst mode

Wait for about 40 cycles. For example, for(i=0;i<10;i++)

Initialize DLL and delay lines

0x24 -- 0x10000100 + (delay percentage<<0)
0x28 -- 0x10000100 + (delay percentage<<0)
0x2C -- 0x10000100 + (delay percentage<<0)
0x30 -- 0x10000100 + (delay percentage<<0)
0x34 -- 0x10000100 + (delay percentage<<0)
0x38 -- 0x10000100 + (delay percentage<<0)
0x08 -- 0x10000580 + (rf_dll_phase_interval<<16)
+ (rf_dll_cpst_thr<<12)
+ (rf_dll_auto_clr_en<<9)
0x08 -- 0x10000480 + (rf_dll_phase_interval<<16)
+ (rf_dll_cpst_thr<<12)
+ (rf_dll_auto_clr_en<<9)

Initialize SMC for normal accessing

0x10 -- 0x111191C0
0x04 -- 0x10000017
0x50 -- 0x08881FFF + (rf_row_length<<20)
0x54 -- 0x020210FF + (rf_t_first_w<<8)
0x58 -- 0x10501015
0x5C -- 0xED000000
0x10 -- 0x111190C0

5.6 Serial Flash Controller

Table 5-9 Pin mapping

Ball	Pin Name	Function1	Typ	Function2	Typ	Function3	Typ	Func4	Typ
T21	ESMCSN0	ESMCSN0	O						
T20	ESMCSN1	ESMCSN1	O						
R22	ESMD0	ESMD0	I/O						
R20	ESMD1	ESMD1	I/O						
R21	ESMD2	ESMD2	I/O						
P22	ESMD3	ESMD3	I/O						
P21	ESMCLK	ESMCLK	O						

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.6.1 Overview

The main function of Serial Flash controller are transmitting command and data to flash and receiving data or status from flash, in 1 bit or 4 bit mode. Serial Flash Controller (SFC) Controls the serial flash read and write operations

5.6.2 Features

1.1.1.1 Flash Device

Supports Device list:

- MXIC
- WINBOND
- EON
- NUMONYX

Giga Device

1.1.1.2 Main features

- Supports up to 156MHz serial bus clock frequency
- Supports 2 flash CS
- Supports up to 256Mbit spi nor flash memory when single CS
- Supports configurable dummy clocks
- Supports up to 40 bytes one time program

Supports Standard SPI / Dual / Quad SPI mode

Supports QPI mode

1.1.1.3 Serial Flash Instruction Format

Command code	Address bytes	Dummy bytes	Data bytes
1 bytes	optional	Optional	optional
Write	write	Write	Read/write

- Supports instruction with 1 byte command only.
- supports instruction with 1 byte command, n bytes data write
- Supports instruction with 1 byte command, 24 bit address, and n bytes data program
- Supports instruction with 1 byte command, 24 bit address, and n bytes data read
- Supports instruction with 1 byte command, m bytes status information read.

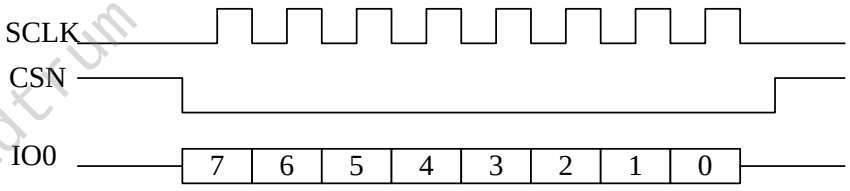


Figure 5-60 1 byte instruction in 1 bit mode

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

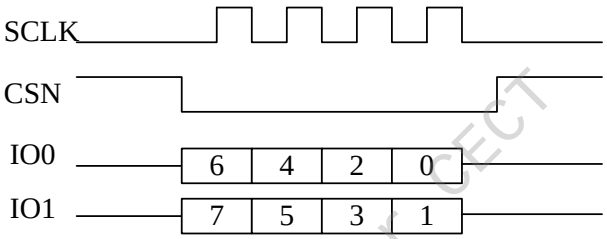


Figure 5-61 1 byte instruction in 2 bit mode

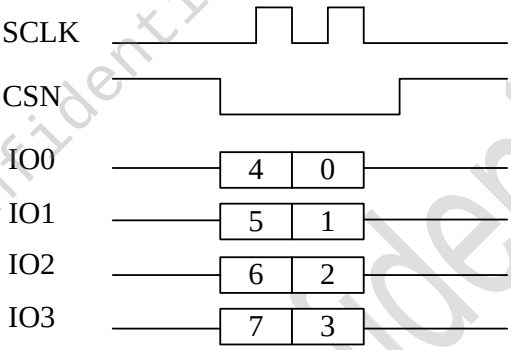


Figure 5-62 1 byte instruction in 4 bit mode

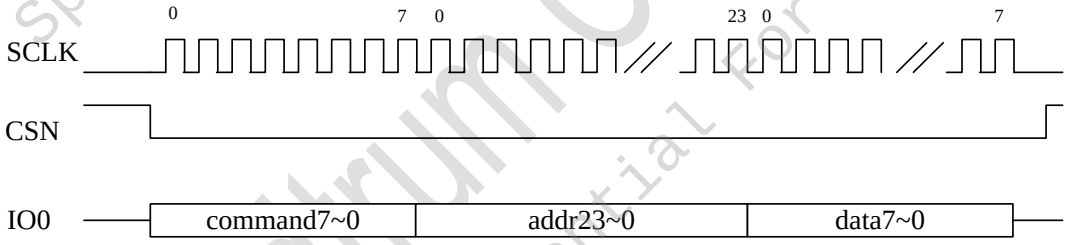


Figure 5-63 program instruction with N byte data in 1 bit mode (N=1)

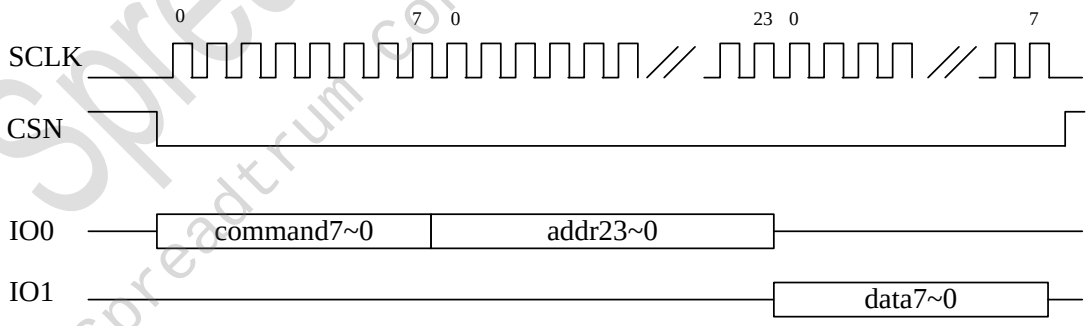


Figure 5-64 read instruction with M byte data in 1 bit mode (M=1)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

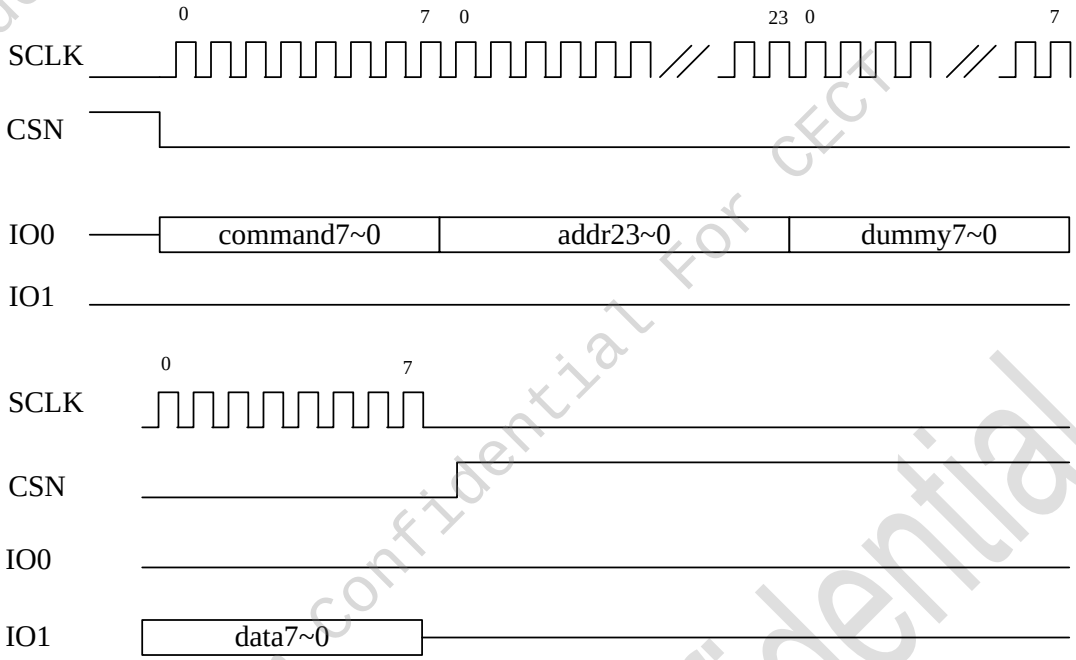


Figure 5-65 read instruction with L byte dummy and M byte data in 1 bit mode (L=1,M=1)

1.1.1.4 Interrupt Operation

- After 1 frame instruction transmission, one interrupt will send to system, and software could read this interrupt.

Spreadtrum Confidential
Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

1.1.1.5 Software Program Flow

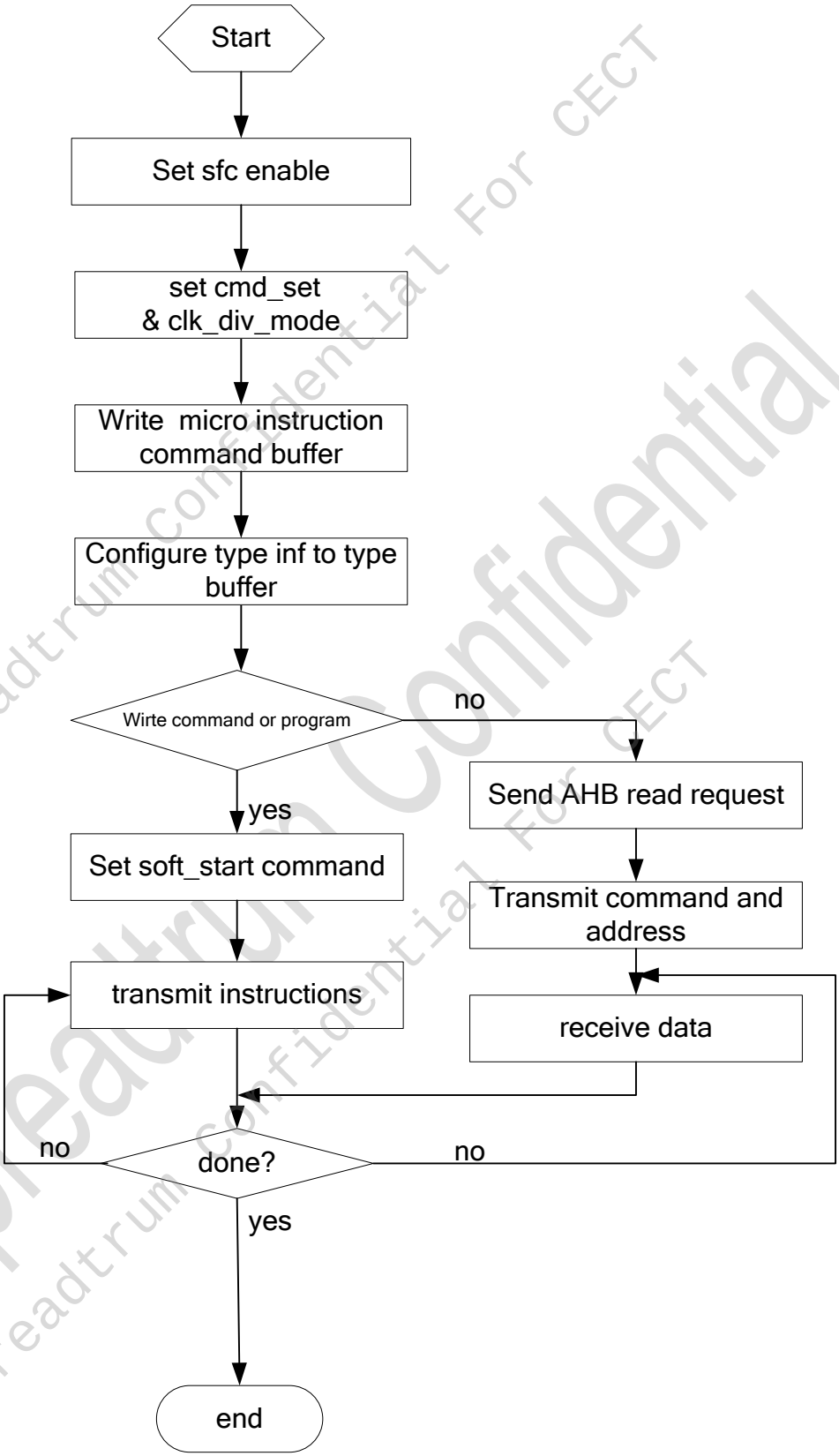


Figure 5-66 software program flow

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.6.3 Signal descriptions

Pin Name	I/O	Function
CS_n[3:0]	O	Serial Flash Chip Select
SCLK	O	Serial Clock output
IO0	I/O	Serial input output 0
IO1	I/O	Serial input output 1
IO2	I/O	serial input output 2
IO3	I/O	serial input output 3

5.6.4 Funtion description

1.1.1.6 Block Diagram

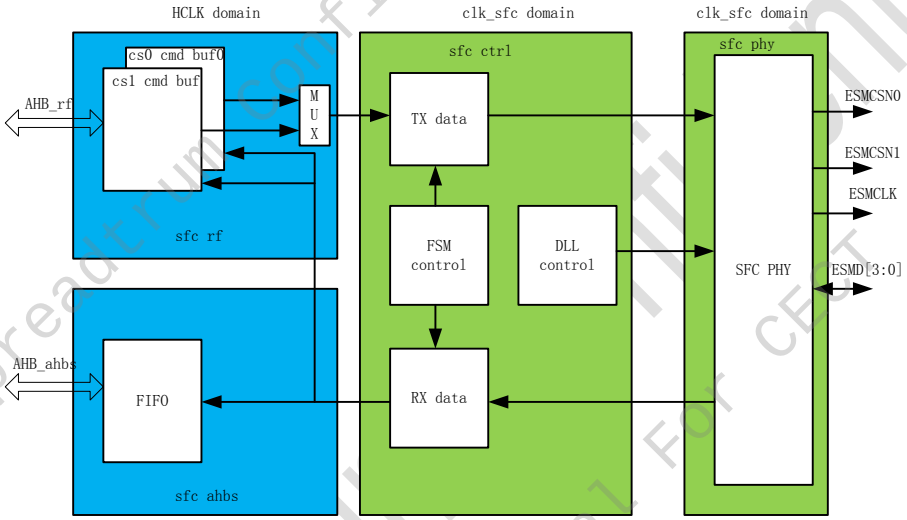


Figure 5-67 SFC Block diagram

SFC is partitioned to two clock domain: HCLK and clk_sfc.

AHB can access SFC in HCLK domain , while SFC control and PHY can work in clk_sfc. So system can work in Higher frequency, not limited by SFC work frequency.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

1.1.1.1 FSM control

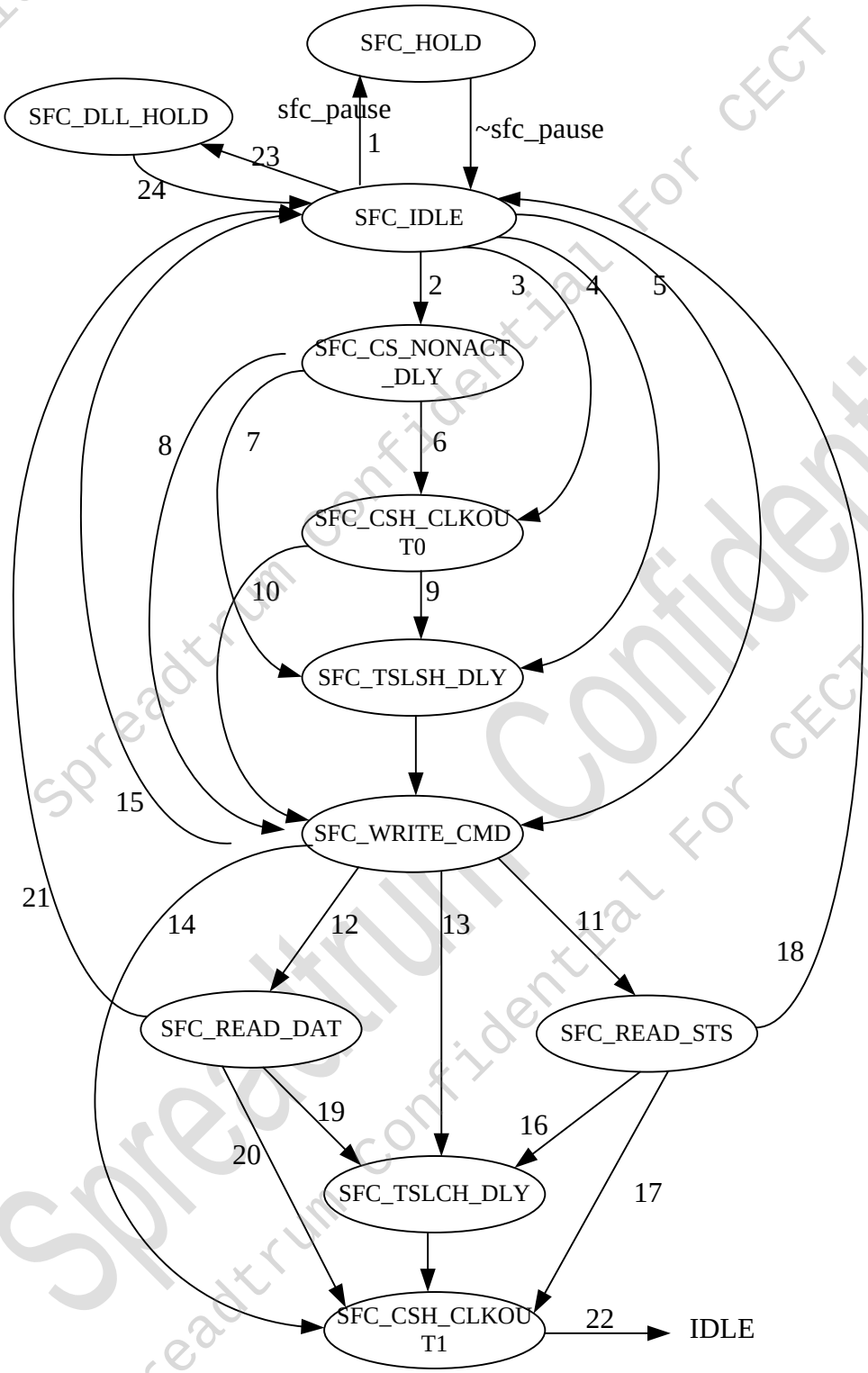


Figure 5-68 SFC FSM chart

Status transition description:

SFC_IDLE: during this status, sfc stops work.

SFC_DLL_HOLD: during this status , dll is working.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SFC_HOLD: during this status, sfc stops work.

SFC_CS_NONACT_DLY: during this status, CS is high.

SFC_CSH_CLKOUT0: during this status, enable the output serial clock.

SFC_TSLSH_DLY: during this status, mask the output serial clock

SFC_WRITE_CMD: during this status, sfc write command, or program data to Flash.

SFC_READ_STS: during this status, sfc read status information or other important information from FLASH.

SFC_READ_DAT: during this status, sfc read data from FLASH.

SFC_TSLCH_DLY: during this status, mask the output serial clock.

SFC_CSH_CLKOUT1: during this status, enable the output serial clock

Condition description:

Condition 1: sfc_pause = 1

Condition 2: (sfc_request | sfc_req_after_hol) && (rf_tshsl_dly_num != 0)

Condition 3: (sfc_request | sfc_req_after_hol) && (rf_tshsl_dly_num == 0) && rf_csh_clkout0_en

Condition 4: (sfc_request | sfc_req_after_hol) && (rf_tshsl_dly_num == 0) && (rf_csh_clkout0_en==0) && rf_tslsh_dly

Condition 5: (sfc_request | sfc_req_after_hol) && (rf_tshsl_dly_num == 0) && (rf_csh_clkout0_en==0) && (rf_tslsh_dly==0)

Condition 6: tshsl_dly_end && rf_csh_clkout0_en

Condition 7: tshsl_dly_end && (rf_csh_clkout0_en==0) && rf_tslsh_dly

Condition 7: tshsl_dly_end && (rf_csh_clkout0_en==0) && (rf_tslsh_dly==0)

Condition 9: csh_clkout0_cnt_end && rf_tslsh_dly

Condition 10: csh_clkout0_cnt_end && (rf_tslsh_dly==0)

Condition 11: rd_sts_st==1

Condition 12 (rd_sts_st==0) && rd_dat_st

Condition 13 (rd_sts_st==0) && (rd_dat_st==0)&&write_end

Condition 14 (rd_sts_st==0) && (rd_dat_st==0)&&write_end && rf_csh_clkout1_en

Condition 15 (rd_sts_st==0) && (rd_dat_st==0)&&write_end && (rf_csh_clkout1_en==0)

Condition 16 rd_sts_end && rf_tshch_dly

Condition 17 rd_sts_end && (rf_tshch_dly==0) && rf_csh_clkout1_en

Condition 18 rd_sts_end && (rf_tshch_dly==0) && (rf_csh_clkout1_en==0)

Condition 19 : rd_dat_end && rf_tshch_dly

Condition 20: rd_dat_end && rf_tshch_dly==0) && rf_csh_clkout1_en

Condition 21: rd_dat_end && rf_tshch_dly==0) && (rf_csh_clkout1_en==0)

Condition 22: csh_clkout1_cnt_end==1

Condition 23: dll_pause_req = 1

Condition 24: dll_pause_req = 0

1.1.1.2 Timing Parameter

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

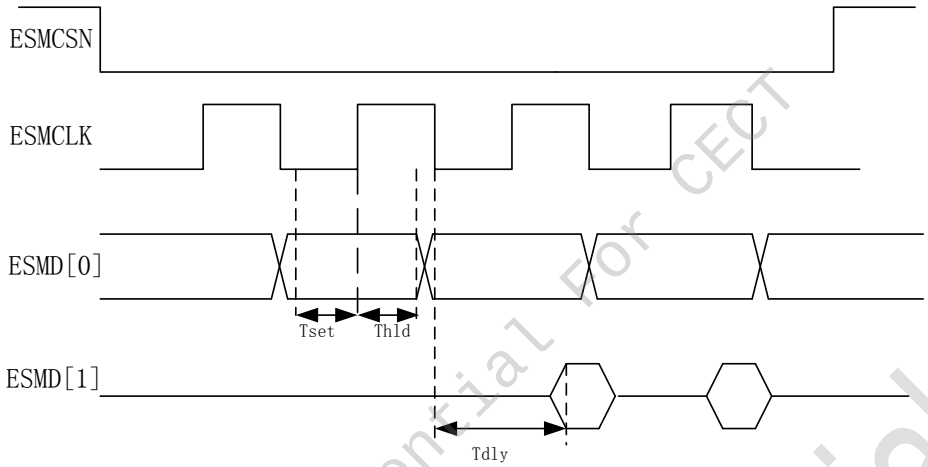


Figure 5-69 SFC Timing Chart

Symbol	Parameter	Min	Max
fESMCLK	SFC output clock frequency		156MHz
Tset	SFC output data setup time	3ns	
Thld	SFC output data hold time	3ns	
Tdly	Flash output delay		4.5ns

5.6.5 Control registers

5.6.5.1 Memory map

ARM base address: 020A0_0000

Offset Address	Name	Description**(detail of abbreviation of this control register)**
0x1000	SFC_CMD_SET	Sfc operation control set
0x1004	SFC_SOFT_REQ	Sfc soft request
0x100C	SFC_INT_CLR	Sfc interrupt clear for cs0 and cs1
0x1010	SFC_STATUS	
0x101C	SFC_CLK_CFG	
0x1020	SFC_CS_CFG	
0x1024	SFC_LSB_CFG	
0x1028	SFC_IO_DLY_CFG	
0x102C	SFC_WP_HLD_INIT	
0x1030	SFC_DL0	
0x1034	SFC_DL1	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description**(detail of abbreviation of this control register)**
0x1038	SFC_DLL	
0x1000	SFC_CS0_RD_CFG	
0x1008	SFC_CS0_TBUF_CLR	Clear sfc type buffer
0x1014	SFC_CS0_CS_TIMING_CFG	Control timing of CSn
0x1018	SFC_CS0_RD_SAMPLE_CFG	Read sample control
0x1040	SFC_CS0_CMD_BUF0	Command buffer 0
0x1044	SFC_CS0_CMD_BUF1	Command buffer 1
0x1048	SFC_CS0_CMD_BUF2	Command buffer 2
0x104C	SFC_CS0_CMD_BUF3	Command buffer 3
0x1050	SFC_CS0_CMD_BUF4	Command buffer 4
0x1054	SFC_CS0_CMD_BUF5	Command buffer 5
0x1058	SFC_CS0_CMD_BUF6	Command buffer 6
0x105C	SFC_CS0_CMD_BUF7	Command buffer 7
0x1060	SFC_CS0_CMD_BUF8	Command buffer 8
0x1064	SFC_CS0_CMD_BUF9	Command buffer 9
0x1068	SFC_CS0_CMD_BUF10	Command buffer 10
0x106C	SFC_CS0_CMD_BUF11	Command buffer 11
0x1070	SFC_CS0_TYPE_BUF0	Type buffer 0
0x1074	SFC_CS0_TYPE_BUF1	Type buffer 1
0x1078	SFC_CS0_TYPE_BUF2	Type buffer 2
0x1080	SFC_CS1_RD_CFG	Cs1 read config
0x1088	SFC_CS1_TBUF_CLR	Clear sfc type buffer
0x1094	SFC_CS1_CS_TIMING_CFG	Control timing of CSn
0x1098	SFC_CS1_RD_SAMPLE_CFG	Read sample control
0x10C0	SFC_CS1_CMD_BUF0	Command buffer 0
0x10C4	SFC_CS1_CMD_BUF1	Command buffer 1
0x10C8	SFC_CS1_CMD_BUF2	Command buffer 2
0x10CC	SFC_CS1_CMD_BUF3	Command buffer 3
0x10D0	SFC_CS1_CMD_BUF4	Command buffer 4
0x10D4	SFC_CS1_CMD_BUF5	Command buffer 5
0x10D8	SFC_CS1_CMD_BUF6	Command buffer 6
0x10DC	SFC_CS1_CMD_BUF7	Command buffer 7
0x10E0	SFC_CS1_CMD_BUF8	Command buffer 8
0x10E4	SFC_CS1_CMD_BUF9	Command buffer 9
0x10E8	SFC_CS1_CMD_BUF10	Command buffer 10

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description**(detail of abbreviation of this control register)**
0x10EC	SFC_CS1_CMD_BUF11	Command buffer 11
0x10F0	SFC_CS1_TYPE_BUF0	Type buffer 0
0x10F4	SFC_CS1_TYPE_BUF1	Type buffer 1
0x10F8	SFC_CS1_TYPE_BUF2	Type buffer 2
0x0200	SFC_CS1_START_ADDR	Flash 1 start address 8bit
0x0204	SFC_IEN	Sfc interrupt enable
0x0208	SFC_INT_RAW	Sfc interrupt raw status
0x020c	SFC_INT_STS	Sfc interrupt mask status
0x0210	SFC_DLL_STS	Sfc dll status
0x021C	SFC_FIFO_SYNC_SEL	

5.6.5.2 Register description

5.6.5.3 SFC_CMD_SET

Address : 0x20A0_0000

Description：The register is used to configure command mode

Field Name	Bit	Type	Reset Value	Description
	[31:8]			Reserved
DATA_RD_INT_MASK	[7]	R/W	1'h0	**0: mask read int flag** **1: unmask read int flag**
AHB_RD_FLG_SEL	[6]	R/W	1'h0	**0: ahb_rdata_vld = 0 when write mode** **1: ahb_rdata_vld = 1 when write mode**
SFC_RD_ALIGN	[5]	R/W	1'h0	0: sfc read flash word align 1: sfc read flash random
CS0_STS_INI_ADDR_SEL	[4:3]	R/W	2'h0	Read back status information initial address selection signal: 0: command buffer 7 1: command buffer 6 2: command buffer 5 3: command buffer 4
CS0_RDATA_BIT_MODE	[2:1]	R/W	2'h0	AHB read data bit mode: 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
CMD_SET	[0]	R/W	1'h1	0: software write serial flash register, or program ,or read status information 1: AHB read data from serial flash

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.6.5.4 SFC_SOFT_REQ

Address : 0x20A0_0004

Description：The register is used to configure soft request

Field Name	Bit	Type	Reset Value	Description
SOFT_REQ	[0]	WO	1'h0	Soft request to sfc for write command or program.

5.6.5.5 CS0_TBUF_CLR

Address : 0x20A0_0008

Description：The register is used to configure type information buffer clear

Field Name	Bit	Type	Reset Value	Description
TBUF_CLR	[0]	WO	1'h0	Type buffer clear control register

5.6.5.6 SFC_INT_CLR

Address : 0x20A0_000C

Description：The register is used to configure interrupt clear

Field Name	Bit	Type	Reset Value	Description
INT_CLR0	[0]	WO	1'h0	Sfc cs0 int clear control register
INT_CLR1	[1]	WO	1'h0	Sfc cs1 int clear control register

5.6.5.7 SFC_STATUS

Address : 0x20A0_0010

Description：The register is used to storage sfc status.

Field Name	Bit	Type	Reset Value	Description
int_req_sfc	[0]	RO	1'h0	Sfc interrupt request signal
Sfc_idle	[1]	RO	1'h0	0: sfc is busy 1: sfc is idle
Cur_sfc_state	[5:2]	RO	4'h0	Sfc current state

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

sfc_cs_sel[1:0]	[7:6]	RO	2'h0	Sfc cs select
[31:8]				Reserved

5.6.5.8 CS0_TIMING_CFG

Address : 0x20A0_0014

Description：The register is used to configure CS timing

Field Name	Bit	Type	Reset Value	Description
Tslch_dly	[0]	R/W	0	Sfc cs active setup time delay control 0: no delay 1: delay 1 clk
Tshch_dly	[1]	R/W	1	Sfc cs not active setup time delay control 0: no delay 1: delay 1 clk
Csh_clkout0_en	[2]	R/W	0	First clk out enable when cs high 0: not enable 1: enable
Csh_clkout1_en	[3]	R/W	0	Last clk out enable when cs high 0: not enable 1: enable
Tslsh_dly_num	[6:4]	R/W	3	CS deselect time delay num. 0: no delay 1: delay 1 clk …
CS_DLY_SEL	[8:7]	R/W	1	CS delay sel 0: no delay 1: delay 1 hclk 2: delay 2 hclk …
[31:9]				Reserved

5.6.5.9 CS0_RD_SAMPLE_CFG

Address : 0x20A0_0018

Description：The register is used to configure read sample control registers

Field Name	Bit	Type	Reset Value	Description
	[31:13]			Reserved
byte_sample_vld_dly_sel	[12:10]	R/W	4	byte sample valid delay sel 0: no delay

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				1: delay 1 hclk 2: delay 2 hclk ..,
Bit_sample_vld_dly_sel	[9:7]	R/W	3	Bit sample valid delay sel 0: no delay 1: delay 1 hclk 2: delay 2 hclk ..,
Sample_rst	[6]	R/W	0	Sfc if read buffer sample reset
t_sample_dly_w	[5:3]	R/W	1	Sfc if read buffer write enable delay control

5.6.5.10 SFC_CLK_CFG

Address : 0x20A0_001C

Description：The register is used to configure clock configuration registers

Field Name	Bit	Type	Reset Value	Description
	[31:11]			Reserved
CLK_2X_EN	[10]	R/W	1'h0	Sfc sample 2x en in sfc control , when sample clock use 2x ,this bit should enable
CLK_OUT_2X_EN	[9]	R/W	1'h0	Sfc phy clock out use 2x: 0: not 2x 1: use 2x
CLK_SAMPLE_2X_PHASE	[8]	R/W	1'h0	Sfc phy sample 2x clock phase: 0: phase 0 1: phase 1
CLK_SAMPLE_2X_EN	[7]	R/W	1'h0	Sfc phy sample clock use 2x
CLK_SAMPLE_SEL	[6]	R/W	1'h0	Sfc read sample clock select 0: clock from loop pad 1: clock from dly line
CLK_OUT_EN_SEL	[5:3]	R/W	3'h0	Clk out enable delay sel 0: no delay 1: delay 1 hclk 2: delay 2 hlck …
CLK_POLARITY	[2]	R/W	2'h0	Serial Clock polarity 0: neg 1: pos
CLK_DIV_MODE	[1:0]	R/W	2'h2	0: sfc output serial clock frequency equals to

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				sfc work clock frequency 1: sfc output serial clock frequency equals to 1/2 sfc work clock frequency 2: sfc output serial clock frequency equals to 1/4 sfc work clock frequecny

5.6.5.11 SFC_CS_CFG

Address : 0x20A0_0020

Description：The register is used to configure flash CS selection control information

Field Name	Bit	Type	Reset Value	Description
	[31:2]			Resrved
SOFT_CS	[1:0]	R/W	2'h0	0: select chip 0 1: select chip 1 …

5.6.5.12 SFC_LSB_CFG

Address : 0x20A0_0024

Description：The register is used to configure spi bus endian control

Field Name	Bit	Type	Reset Value	Description
	[31:2]			Resrved
SPI_ENDIAN_RX	[1]	R/W	1'h0	0: Spi rx bit MSB first 1: spi rx bit LSB first
SPI_ENDIAN_TX	[0]	R/W	1'h0	0: Spi tx bit MSB first 1: spi tx bit LSB first

5.6.5.13 SFC_IO_DLY_CFG

Address : 0x20A0_0028

Description：The register is used to configure SFC IO delay

Field Name	Bit	Type	Reset Value	Description
	[31:7]			Resrved
DO_DLY_SEL	[6:5]	R/W	2'h0	Sfc data out delay sel 0: no delay 1: delay 1 hclk

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				2: delay 2 hclk …
DATA_IE_WIDTH_CTRL	[4]	R/W	0	0: data ie is sfc_data_ie 1: data ie is sfc_data_ie | sfc_data_ie_d1
DATA_IE_DLY_SEL	[3:2]	R/W	2'h0	Data ie delay sel 0: no delay 1: delay 1 hclk 2: delay 2 hclk …
DATA_OE_DLY_SEL	[1:0]	R/W	2'h0	Data oe delay sel 0: no delay 1: delay 1 hclk 2: delay 2 hclk …

5.6.5.14 SFC_WP_HLD_INIT_CFG

Address : 0x20A0_002C

Description：The register is used to configure SPI bus WP/Hold initial

Field Name	Bit	Type	Reset Value	Description
	[31:2]			Resrved
HLD_INIT	[1]	R/W	1'h1	0: HLDn initial value is 0 1: HLDn initial value is 1
WP_INIT	[0]	R/W	1'h1	0: WPn initial value is 0 1: WPn initial value is 1

5.6.5.15 SFC_DL0

Address : 0x20A0_0030

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:9]			Resrved
DL0_DLY_CPST_EN	[8]	R/W	1'h0	0: manual compensation by software 1: auto compensation by dll
DL0_DLY_INV	[7]	R/W	1'h0	0: sample clock not invert 1: sample clock invert
DL0_DLY_SEL	[6:0]	R/W	7'h0	DL0 dly number for manual set

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.6.5.16 SFC_DL1

Address : 0x20A0_0034

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:9]			Resrved
DL1_DLY_CPST_EN	[8]	R/W	1'h0	0: manual compensation by software 1: auto compensation by dll
DL1_DLY_INV	[7]	R/W	1'h0	0: sample clock not invert 1: sample clock invert
DL1_DLY_SEL	[6:0]	R/W	7'h0	DL1 dly number for manual set

5.6.5.17 SFC_DLL

Address : 0x20A0_0038

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:9]			Resrved
DLL_CPST_THR	[15:12]	R/w	3'h0	Dll compensation threshold value
DLL_CPST_START	[11]	R/W	1'h0	0: Dll compensation start by hardware 1: dll compensation start by software
DLL_CPST_EN	[10]	R/W	1'h0	Dll compensation enable
DLL_AUTO_CLR_EN	[9]	R/W	1'h0	DLL auto clear by hardware
DLL_CLR	[8]	R/W	1'h0	Dll clear by software 0: not clear 1: clear
DLL_EN	[7]	R/W	1'h0	0: dll disable 1: dll enable
DLL_INIT	[6:0]	R/W	7'h0	Dll initial set

t_sample_dly_r	[2:0]	R/W	2	Sfc if read buffer read enable delay control

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.6.5.18 CS0_CMD_BUF0

Address : 0x20A0_0040

Description：The register is used to configure command buffer 0

Field Name	Bit	Type	Reset Value	Description
cmd_buf0	[31:0]	R/W	32'h0000_0003	Command buffer 0

5.6.5.19 CS0_CMD_BUF1

Address : 0x20A0_0044

Description：The register is used to configure command buffer 1

Field Name	Bit	Type	Reset Value	Description
cmd_buf1	[31:0]	R/W	32'h0000_0000	Command buffer 1

5.6.5.20 CS0_CMD_BUF2

Address : 0x20A0_0048

Description：The register is used to configure command buffer 2

Field Name	Bit	Type	Reset Value	Description
cmd_buf2	[31:0]	R/W	32'h0000_0000	Command buffer 2

5.6.5.21 CS0_CMD_BUF3

Address : 0x20A0_004C

Description：The register is used to configure command buffer 3

Field Name	Bit	Type	Reset Value	Description
cmd_buf3	[31:0]	R/W	32'h0000_0000	Command buffer 3

5.6.5.22 CS0_CMD_BUF4

Address : 0x20A0_0050

Description：The register is used to configure command buffer 4

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

cmd_buf4	[31:0]	R/W	32'h0000_0000	Command buffer 4

5.6.5.23 CS0_CMD_BUF5

Address : 0x20A0_0054

Description：The register is used to configure command buffer 5

Field Name	Bit	Type	Reset Value	Description
cmd_buf5	[31:0]	R/W	32'h0000_0000	Command buffer 5

5.6.5.24 CS0_CMD_BUF6

Address : 0x20A0_0058

Description：The register is used to configure command buffer 6

Field Name	Bit	Type	Reset Value	Description
cmd_buf6	[31:0]	R/W	32'h0000_0000	Command buffer 6

5.6.5.25 CS0_CMD_BUF7

Address : 0x20A0_005C

Description：The register is used to configure command buffer 7

Field Name	Bit	Type	Reset Value	Description
cmd_buf7	[31:0]	R/W	32'h0000_0000	Command buffer 7

5.6.5.26 CS0_CMD_BUF8

Address : 0x20A0_0060

Description：The register is used to configure command buffer 8

Field Name	Bit	Type	Reset Value	Description
cmd_buf8	[31:0]	R/W	32'h0000_0000	Command buffer 8

5.6.5.27 CS0_CMD_BUF9

Address : 0x20A0_0064

Description：The register is used to configure command buffer 9

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

cmd_buf9	[31:0]	R/W	32'h0000_0000	Command buffer 9

5.6.5.28 CS0_CMD_BUF10

Address : 0x20A0_0068

Description：The register is used to configure command buffer 10

Field Name	Bit	Type	Reset Value	Description
cmd_buf10	[31:0]	R/W	32'h0000_0000	Command buffer 10

5.6.5.29 CS0_CMD_BUF11

Address : 0x20A0_006C

Description：The register is used to configure command buffer 11

Field Name	Bit	Type	Reset Value	Description
cmd_buf11	[31:0]	R/W	32'h0000_0000	Command buffer 11

5.6.5.30 CS0_TYPE_INF_BUF0

Address : 0x20A0_0070

Description：The register is used to configure type information buffer 0

Field Name	Bit	Type	Reset Value	Description
Valid0	[0]	R/W	1	0: command buffer0 is invalid 1: command buffer0 is valid
Bit_mode0	[2:1]	R/w	0	Command buffer0 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num0	[4:3]	R/W	0	Command buffer 0 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status0	[6:5]	R/W	0	Command buffer 0 operation status: 0: write 1: read 2: High-Z
Byte_send_mode0	[7]	R/W	0	Command buffer 0 byte send mode: 0: byte0,1,2,3 order

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				1: byte3,2,1,0 order
Valid1	[8]	R/W	1	0: command buffer 1 is invalid 1: command buffer 1 is valid
Bit_mode1	[10:9]	R/w	0	Command buffer 1 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num1	[12:11]	R/W	2	Command buffer 1 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status1	[14:13]	R/W	0	Command buffer 1 operation status: 0: write 1: read 2: High-Z
Byte_send_mode1	[15]	R/W	1	Command buffer 1 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid2	[16]	R/W	0	0: command buffer 2 is invalid 1: command buffer 2 is valid
Bit_mode2	[18:17]	R/w	0	Command buffer 2 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num2	[20:19]	R/W	0	Command buffer 2 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status2	[22:21]	R/W	0	Command buffer 2 operation status: 0: write 1: read 2: High-Z
Byte_send_mode2	[23]	R/W	0	Command buffer 2 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid3	[24]	R/W	0	0: command buffer 3 is invalid 1: command buffer 3 is valid
Bit_mode3	[26:25]	R/w	0	Command buffer 3 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num3	[28:27]	R/W	0	Command buffer 3 byte number:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status3	[30:29]	R/W	0	Command buffer 3 operation status: 0: write 1: read 2: High-Z
Byte_send_mode3	[31]	R/W	0	Command buffer 3 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order

5.6.5.31 CS0_TYPE_INF_BUF1

Address : 0x20A0_0074

Description：The register is used to configure type information buffer 1

Field Name	Bit	Type	Reset Value	Description
Valid4	[0]	R/W	0	0: command buffer 4 is invalid 1: command buffer 4 is valid
Bit_mode4	[2:1]	R/w	0	Command buffer 4 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num4	[4:3]	R/W	0	Command buffer 4 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status4	[6:5]	R/W	0	Command buffer 4 operation status: 0: write 1: read 2: High-Z
Byte_send_mode4	[7]	R/W	0	Command buffer 4 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid5	[8]	R/W	0	0: command buffer 5 is invalid 1: command buffer 5 is valid
Bit_mode5	[10:9]	R/w	0	Command buffer 5 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Byte_num5	[12:11]	R/W	0	Command buffer 5 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status5	[14:13]	R/W	0	Command buffer 5 operation status: 0: write 1: read 2: High-Z
Byte_send_mode5	[15]	R/W	0	Command buffer 5 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid6	[16]	R/W	0	0: command buffer 6 is invalid 1: command buffer 6 is valid
Bit_mode6	[18:17]	R/w	0	Command buffer 6 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num6	[20:19]	R/W	0	Command buffer 6 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status6	[22:21]	R/W	0	Command buffer 6 operation status: 0: write 1: read 2: High-Z
Byte_send_mode6	[23]	R/W	0	Command buffer 6 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid7	[24]	R/W	0	0: command buffer 7 is invalid 1: command buffer 7 is valid
Bit_mode7	[26:25]	R/w	0	Command buffer 7 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num7	[28:27]	R/W	0	Command buffer 7 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status7	[30:29]	R/W	0	Command buffer 7 operation status: 0: write 1: read 2: High-Z

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Byte_send_mode7	[31]	R/W	0	Command buffer 7 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order

5.6.5.32 CS0_TYPE_INF_BUF2

Address : 0x20A0_0078

Description：The register is used to configure type information buffer 2

Field Name	Bit	Type	Reset Value	Description
Valid8	[0]	R/W	0	0: command buffer 8 is invalid 1: command buffer 8 is valid
Bit_mode8	[2:1]	R/w	0	Command buffer 8 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num8	[4:3]	R/W	0	Command buffer 8 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status8	[6:5]	R/W	0	Command buffer 8 operation status: 0: write 1: read 2: High-Z
Byte_send_mode8	[7]	R/W	0	Command buffer 8 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid9	[8]	R/W	0	0: command buffer 9 is invalid 1: command buffer 9 is valid
Bit_mode9	[10:9]	R/w	0	Command buffer 9 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num9	[12:11]	R/W	0	Command buffer 9 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status9	[14:13]	R/W	0	Command buffer 9 operation status: 0: write 1: read

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				2: High-Z
Byte_send_mode9	[15]	R/W	0	Command buffer 9 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid10	[16]	R/W	0	0: command buffer 10 is invalid 1: command buffer 10 is valid
Bit_mode10	[18:17]	R/w	0	Command buffer 10 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num10	[20:19]	R/W	0	Command buffer 10 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status10	[22:21]	R/W	0	Command buffer 10 operation status: 0: write 1: read 2: High-Z
Byte_send_mode10	[23]	R/W	0	Command buffer 10 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid11	[24]	R/W	0	0: command buffer 11 is invalid 1: command buffer 11 is valid
Bit_mode11	[26:25]	R/w	0	Command buffer 11 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num11	[28:27]	R/W	0	Command buffer 11 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status11	[30:29]	R/W	0	Command buffer 11 operation status: 0: write 1: read 2: High-Z
Byte_send_mode11	[31]	R/W	0	Command buffer 11 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.6.5.33 CS1_RD_CFG

Address : 0x20A0_0080

Description：The register is used to configure command mode

Field Name	Bit	Type	Reset Value	Description
	[31:5]			Reserved
STS_INI_ADDR_SEL	[4:3]	R/W	2'h0	Read back status information initial address selection signal: 0: command buffer 7 1: command buffer 6 2: command buffer 5 3: command buffer 4
RDATA_BIT_MODE	[2:1]	R/W	2'h0	AHB read data bit mode: 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode

5.6.5.34 CS1_TBUF_CLR

Address : 0x20A0_0088

Description：The register is used to configure type information buffer clear

Field Name	Bit	Type	Reset Value	Description
TBUF_CLR	[0]	WO	1'h0	Type buffer clear control register

5.6.5.35 CS1_TIMING_CFG

Address : 0x20A0_0094

Description：The register is used to configure CS timing

Field Name	Bit	Type	Reset Value	Description
Tslch_dly	[0]	R/W	0	Sfc cs active setup time delay control 0: no delay 1: delay 1 clk
Tshch_dly	[1]	R/W	1	Sfc cs not active setup time delay control 0: no delay 1: delay 1 clk

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Csh_clkout0_en	[2]	R/W	0	First clk out enable when cs high 0: not enable 1: enable
Csh_clkout1_en	[3]	R/W	0	Last clk out enable when cs high 0: not enable 1: enable
Tslsh_dly_num	[6:4]	R/W	3	CS deselect time delay num. 0: no delay 1: delay 1 clk …
CS_DLY_SEL	[8:7]	R/W	1	CS delay sel 0: no delay 1: delay 1 hclk 2: delay 2 hclk …
[31:7]				Reserved

5.6.5.36 CS1_RD_SAMPLE_CFG

Address : 0x20A0_0098

Description：The register is used to configure read sample control registers

Field Name	Bit	Type	Reset Value	Description
	[31:13]			Reserved
byte_sample_vld_dly_sel	[12:10]	R/W	4	byte sample valid delay sel 0: no delay 1: delay 1 hclk 2: delay 2 hclk ..,
Bit_sample_vld_dly_sel	[9:7]	R/W	3	Bit sample valid delay sel 0: no delay 1: delay 1 hclk 2: delay 2 hclk ..,
Sample_rst	[6]	R/W	0	Sfc if read buffer sample reset
T_sample_dly_w	[5:3]	R/W	1	Sfc if read buffer write enable delay control
T_sample_dly_r	[2:0]	R/W	2	Sfc if read buffer read enable delay control

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.6.5.37 CS1_CMD_BUF0

Address : 0x20A0_00C0

Description：The register is used to configure command buffer 0

Field Name	Bit	Type	Reset Value	Description
cmd_buf0	[31:0]	R/W	32'h0000_0003	Command buffer 0

5.6.5.38 CS1_CMD_BUF1

Address : 0x20A0_00C4

Description：The register is used to configure command buffer 1

Field Name	Bit	Type	Reset Value	Description
cmd_buf1	[31:0]	R/W	32'h0000_0000	Command buffer 1

5.6.5.39 CS1_CMD_BUF2

Address : 0x20A0_00C8

Description：The register is used to configure command buffer 2

Field Name	Bit	Type	Reset Value	Description
cmd_buf2	[31:0]	R/W	32'h0000_0000	Command buffer 2

5.6.5.40 CS1_CMD_BUF3

Address : 0x20A0_00CC

Description：The register is used to configure command buffer 3

Field Name	Bit	Type	Reset Value	Description
cmd_buf3	[31:0]	R/W	32'h0000_0000	Command buffer 3

5.6.5.41 CS1_CMD_BUF4

Address : 0x20A0_00D0

Description：The register is used to configure command buffer 4

Field Name	Bit	Type	Reset Value	Description
cmd_buf4	[31:0]	R/W	32'h0000_0000	Command buffer 4

5.6.5.42 CS1_CMD_BUF5

Address : 0x20A0_00D4

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Description：The register is used to configure command buffer 5

Field Name	Bit	Type	Reset Value	Description
cmd_buf5	[31:0]	R/W	32'h0000_0000	Command buffer 5

5.6.5.43 CS1_CMD_BUF6

Address : 0x20A0_00D8

Description：The register is used to configure command buffer 6

Field Name	Bit	Type	Reset Value	Description
cmd_buf6	[31:0]	R/W	32'h0000_0000	Command buffer 6

5.6.5.44 CS1_CMD_BUF7

Address : 0x20A0_00DC

Description：The register is used to configure command buffer 7

Field Name	Bit	Type	Reset Value	Description
cmd_buf7	[31:0]	R/W	32'h0000_0000	Command buffer 7

5.6.5.45 CS1_CMD_BUF8

Address : 0x20A0_00E0

Description：The register is used to configure command buffer 8

Field Name	Bit	Type	Reset Value	Description
cmd_buf8	[31:0]	R/W	32'h0000_0000	Command buffer 8

5.6.5.46 CS1_CMD_BUF9

Address : 0x20A0_00E4

Description：The register is used to configure command buffer 9

Field Name	Bit	Type	Reset Value	Description
cmd_buf9	[31:0]	R/W	32'h0000_0000	Command buffer 9

5.6.5.47 CS1_CMD_BUF10

Address : 0x20A0_00E8

Description：The register is used to configure command buffer 10

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
cmd_buf10	[31:0]	R/W	32'h0000_0000	Command buffer 10

5.6.5.48 CS1_CMD_BUF11

Address : 0x20A0_00EC

Description：The register is used to configure command buffer 11

Field Name	Bit	Type	Reset Value	Description
cmd_buf11	[31:0]	R/W	32'h0000_0000	Command buffer 11

5.6.5.49 CS1_TYPE_INF_BUF0

Address : 0x20A0_00F0

Description：The register is used to configure type information buffer 0

Field Name	Bit	Type	Reset Value	Description
Valid0	[0]	R/W	1	0: command buffer0 is invalid 1: command buffer0 is valid
Bit_mode0	[2:1]	R/w	0	Command buffer0 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num0	[4:3]	R/W	0	Command buffer 0 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status0	[6:5]	R/W	0	Command buffer 0 operation status: 0: write 1: read 2: High-Z
Byte_send_mode0	[7]	R/W	0	Command buffer 0 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid1	[8]	R/W	1	0: command buffer 1 is invalid 1: command buffer 1 is valid
Bit_mode1	[10:9]	R/w	0	Command buffer 1 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Byte_num1	[12:11]	R/W	2	Command buffer 1 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status1	[14:13]	R/W	0	Command buffer 1 operation status: 0: write 1: read 2: High-Z
Byte_send_mode1	[15]	R/W	1	Command buffer 1 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid2	[16]	R/W	0	0: command buffer 2 is invalid 1: command buffer 2 is valid
Bit_mode2	[18:17]	R/w	0	Command buffer 2 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num2	[20:19]	R/W	0	Command buffer 2 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status2	[22:21]	R/W	0	Command buffer 2 operation status: 0: write 1: read 2: High-Z
Byte_send_mode2	[23]	R/W	0	Command buffer 2 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid3	[24]	R/W	0	0: command buffer 3 is invalid 1: command buffer 3 is valid
Bit_mode3	[26:25]	R/w	0	Command buffer 3 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num3	[28:27]	R/W	0	Command buffer 3 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status3	[30:29]	R/W	0	Command buffer 3 operation status: 0: write 1: read 2: High-Z

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Byte_send_mode3	[31]	R/W	0	Command buffer 3 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order

5.6.5.50 CS1_TYPE_INF_BUF1

Address : 0x20A0_00F4

Description：The register is used to configure type information buffer 1

Field Name	Bit	Type	Reset Value	Description
Valid4	[0]	R/W	0	0: command buffer 4 is invalid 1: command buffer 4 is valid
Bit_mode4	[2:1]	R/w	0	Command buffer 4 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num4	[4:3]	R/W	0	Command buffer 4 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status4	[6:5]	R/W	0	Command buffer 4 operation status: 0: write 1: read 2: High-Z
Byte_send_mode4	[7]	R/W	0	Command buffer 4 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid5	[8]	R/W	0	0: command buffer 5 is invalid 1: command buffer 5 is valid
Bit_mode5	[10:9]	R/w	0	Command buffer 5 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num5	[12:11]	R/W	0	Command buffer 5 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status5	[14:13]	R/W	0	Command buffer 5 operation status: 0: write 1: read

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				2: High-Z
Byte_send_mode5	[15]	R/W	0	Command buffer 5 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid6	[16]	R/W	0	0: command buffer 6 is invalid 1: command buffer 6 is valid
Bit_mode6	[18:17]	R/w	0	Command buffer 6 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num6	[20:19]	R/W	0	Command buffer 6 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status6	[22:21]	R/W	0	Command buffer 6 operation status: 0: write 1: read 2: High-Z
Byte_send_mode6	[23]	R/W	0	Command buffer 6 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid7	[24]	R/W	0	0: command buffer 7 is invalid 1: command buffer 7 is valid
Bit_mode7	[26:25]	R/w	0	Command buffer 7 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num7	[28:27]	R/W	0	Command buffer 7 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status7	[30:29]	R/W	0	Command buffer 7 operation status: 0: write 1: read 2: High-Z
Byte_send_mode7	[31]	R/W	0	Command buffer 7 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.6.5.51 CS1_TYPE_INF_BUF2

Address : 0x20A0_00F8

Description：The register is used to configure type information buffer 2

Field Name	Bit	Type	Reset Value	Description
Valid8	[0]	R/W	0	0: command buffer 8 is invalid 1: command buffer 8 is valid
Bit_mode8	[2:1]	R/w	0	Command buffer 8 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num8	[4:3]	R/W	0	Command buffer 8 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status8	[6:5]	R/W	0	Command buffer 8 operation status: 0: write 1: read 2: High-Z
Byte_send_mode8	[7]	R/W	0	Command buffer 8 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid9	[8]	R/W	0	0: command buffer 9 is invalid 1: command buffer 9 is valid
Bit_mode9	[10:9]	R/w	0	Command buffer 9 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num9	[12:11]	R/W	0	Command buffer 9 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status9	[14:13]	R/W	0	Command buffer 9 operation status: 0: write 1: read 2: High-Z
Byte_send_mode9	[15]	R/W	0	Command buffer 9 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid10	[16]	R/W	0	0: command buffer 10 is invalid 1: command buffer 10 is valid

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Bit_mode10	[18:17]	R/w	0	Command buffer 10 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num10	[20:19]	R/W	0	Command buffer 10 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status10	[22:21]	R/W	0	Command buffer 10 operation status: 0: write 1: read 2: High-Z
Byte_send_mode10	[23]	R/W	0	Command buffer 10 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order
Valid11	[24]	R/W	0	0: command buffer 11 is invalid 1: command buffer 11 is valid
Bit_mode11	[26:25]	R/w	0	Command buffer 11 bit mode 0: 1 bit mode 1: 2 bit mode 2: 4 bit mode
Byte_num11	[28:27]	R/W	0	Command buffer 11 byte number: 0: 1 byte 1: 2 byte 2: 3 byte 3: 4 byte
Operation_status11	[30:29]	R/W	0	Command buffer 11 operation status: 0: write 1: read 2: High-Z
Byte_send_mode11	[31]	R/W	0	Command buffer 11 byte send mode: 0: byte0,1,2,3 order 1: byte3,2,1,0 order

5.6.5.52 SFC_CS1_START_ADDR

Address : 0x20A0_0200

Description：The register is used to configure cs1 flash start address

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

rf_cs1_start_addr	[7:0]	R/W	8'h4	8'h01: cs0 space size = 8 M bit 8'h02: cs0 space size = 16 M bit 8'h04: cs0 space size = 32 M bit 8'h08: cs0 space size = 64 M bit 8'h10: cs0 space size = 128 M bit 8'h20: cs0 space size = 256 M bit 8'h40: cs0 space size = 512 M bit 8'h80: not support dual CS

5.6.5.53 SFC_INT_IEN

Address : 0x20A0_0204

Description：The register is used to configure interrupt enable

Field Name	Bit	Type	Reset Value	Description
SFC_INT_IEN	[7:0]	R/W	**8'h0**	[0] : for cs0 interrupt [1] : for cs1 interrupt

5.6.5.54 SFC_INT_RAW

Address : 0x20A0_0208

Description：The register is used to output sfc int raw

Field Name	Bit	Type	Reset Value	Description
SFC_INT_RAW	[7:0]	RO	8'h0	[0] : cs0 interrupt status raw [1] : cs1 interrupt status raw

5.6.5.55 SFC_INT_STS

Address : 0x20A0_020C

Description：The register is used to output sfc int status

Field Name	Bit	Type	Reset Value	Description
SFC_INT_STS	[7:0]	RO	8'h0	[0] : cs0 interrupt status after mask [1] : cs1 interrupt status after mask

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.6.5.56 SFC_DLL_STS

Address : 0x20A0_0210

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:27]			Reserved
DL1_DLY_SEL	[26:20]	RO		DL1 dly number
DL0_DLY_SEL	[19:13]	RO		DL0 dly number
DLL_CPST_ST	[12]	RO		DLL compensation FSM status
DLL_ST	[11:9]	RO		DLL FSM status
DLL_CNT	[8:2]	RO		DLL counter value
DLL_ERROR	[1]	RO	1'h0	0: dll no error 1: when dll unlock
DLL_LOCK	[0]	RO	1'h0	0 : dll not lock 1 : dll locked

5.6.5.57 SFC_FIFO_SYNC_SEL

Address : 0x20A0_0214

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:1]			Reserved
SYNC_SEL	**[0]**	**R/W**	**1'h0**	**0 : sfc in asynchronous read mode** **1 : sfc in synchronous read mode**

5.6.6 Application notes

Including RAM input and output formats, special requirement, software control flow, description, etc.

5.6.6.1 Write enable (06H)

standard spi mode

- ✓ Write [0x20A0_0000] = 0x1000_0000
- ✓ Write [0x20A0_0040] = 0x1000_0006
- ✓ Write [0x20A0_0070] = 0x1000_0001
- ✓ Write [0x20A0_0004] = 0x1000_0001

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

QPI mode

- ✓ Write [0x20A0_0000] = 0x1000_0000
- ✓ Write [0x20A0_0040] = 0x1000_0006
- ✓ Write [0x20A0_0070] = 0x1000_0005
- ✓ Write [0x20A0_0004] = 0x1000_0001

5.6.6.2 Program (02H)

Before program, polling sfc status , if sfc busy, wait sfc idle , then program start.

standard spi mode : 1 word

- ✓ Write [0x20A0_0000] = 0x1000_0000
- ✓ Write [0x20A0_0040] = 0x1000_0002
- ✓ Write [0x20A0_0070] = 0x1019_9101
- ✓ Write [0x20A0_0004] = 0x1000_0001

QPI mode : 1 word

- ✓ Write [0x20A0_0000] = 0x1000_0000
- ✓ Write [0x20A0_0040] = 0x1000_0002
- ✓ Write [0x20A0_0070] = 0x101D_9505
- ✓ Write [0x20A0_0004] = 0x1000_0001

5.6.6.3 Fast read (0BH)

Before read, polling flash status, if last command is finished , then read start

QPI mode:

- ✓ First Set Sample_rst = 1, then set Sample_rst = 0 (clear buffer in PHY)
- ✓ Write [0x20A0_0000] = 0x1000_0005
- ✓ Write [0x20A0_0040] = 0x1000_000B
- ✓ Write [0x20A0_0070] = 0x1000_9505

5.6.6.4 PHY configure

When sfc supports 133MHz:

- ✓ Set CLK_DIV_MODE = 0
- ✓ Set CLK_OUT_2X_EN = 1
- ✓ Set CLK_SAMPLE_2X_EN = 1
- ✓ Set CLK_2X_EN = 1

5.6.6.5 DLL configure

Set DLL configure

- ✓ Set DLL_EN = 1;
- ✓ Set DLL_INIT
- ✓ Set DLL_CLR = 1 then DLL_CLR =0
- ✓ Set DLL_CPST_EN = 1;
- ✓ Set DLL_CPST_THR

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Set DL1 configure for data sample

- ✓ Set DL1_DLY_SEL
- ✓ Set DL1_DLY_CPST_EN = 1

5.7 Direct Memory Access

5.7.1 Overview

Table 5-10 Dma request channel list

Channel ID	Module	
0	software	
1	Uart0(TX)	
2	Uart0(RX)	
3	Uart1(TX)	
4	Uart1(RX)	
5	Spi0(TX)	
6	Spi0(RX)	
7	Spi1(TX)	
8	Spi1(RX)	
9	Iis(TX)	
10	Iis(RX)	
11	Sim(TX)	
12	Sim(RX)	
13	Vbc(AD0)	
14	Vbc(AD1)	
15	Vbc(DA0)	
16	Vbc(DA1)	
17	Usb(EP0)	
18	Usb(EP1)	
19	Usb(EP2)	
20	Usb(EP3)	
21	Usb(EP4)	
22	Usb(EP5)	
23	MIDI0	
24	MIDI1	
25	Rotation	
26	Gea	
27	Fmark_lcm	
28	Uart2(TX)	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

29	Uart2(RX)	
30	SDIO_WR	
31	reserved	

Note: The CHID is the ID inside the DMA, not req or ack id

5.7.2 Features

- AMBA2.0 AHB Specification.
- Two 32-bit AHB masters for read and write operation.
- One AHB 32-bit slave for configuration only supports word access to AHB slave port.
- Support Byte/Half-word/word transfer on AHB Read/Write Master.
- Not support AMBA ERROR/RETRY/SPLIT response.
- Support AMBA NSEQ/INCR4/INCR8 transaction, INCR4/INCR8 configurable.
- AHB Master Big-endian or Little-endian.
- Support 32 channels assigned to hardware request by Channel ID;
- One physical channel shared by 32 Logic channels.
- 4-level configurable priority. 0 has the lowest and 3 have the highest priority. For the channels with the same priority, robin-round would be preferred.
- A-synchronized/Synchronized hand-shake request & acknowledge.
- Accept request from both hardware and software.
- Un-aligned word accesses, for both read and write operation.
- Byte/Half-word switch scheme.
- Support link list for scatter and gather transfer.
- Configurable fragment wait time between two successive fragments.
- One request for fragment/block/transaction/link-list.
- Automatically disable channel after requests done.
- Support 128K-1 byte fragment length.
- Support 128K-1 byte block length (Block length may be less than fragment length in Standard Channel, while forbidden in Full channel).
- Support 256M-1 byte transaction length.
- Support transfer step, ranged from – (32K-1) bytes to (32K-1) bytes, only for full DMA channel.
- Support fragment step, ranged from – (32K-1) bytes to (32K-1) bytes, only for full DMA channel.
- Support block step, ranged from – (128M-1) bytes to (128M-1) bytes, only for full DMA channel.
- Address-fix transfer for either Source side or destination side.
- Address-wrap transfer for either Source side or destination side.
- Pause DMA or pause logical channel.
- Interrupt of fragment, block, transaction and link list, with raw and masked status.
- Interrupt of Error configuration, and support errors status.
- Support hardware request to be re-allocated by Channel ID.
- Support automatically sleep when all requests served, and wakeup when hardware request active;
- Support software retention if power domain of DMA shut down;

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.7.3 Funtion description

5.7.3.1 General Description

DMA Controller support fast data transfers to off-load the processor. With DMA, specific devices on AHB and APB can complete quick data movement from/to memories, internal RAM or External SRAM. DMA Controller can also be used to connect any two devices other than memories, as long as they can be addressed in memory space.

5.7.3.2 Standard & Full DMA Channels

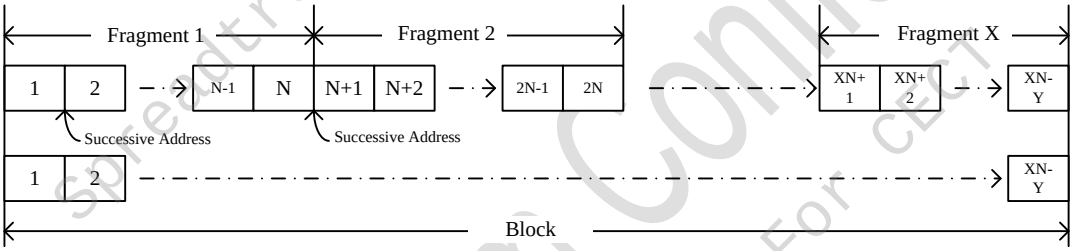
There are two types of DMA channels. One is called “Standard” DMA channel, and the other is “Full” DMA channel.

For most applications, a standard DMA channel would be sufficient, with least configurations and simplest control flow. AHB sequential transfer and FIFO transfer would be efficiently managed, with byte, half-word or word size.

For special applications, such as image rotation or complex data arrangement, Full DMA channel support address wrap transfer, configurable transfer step and link list mode.

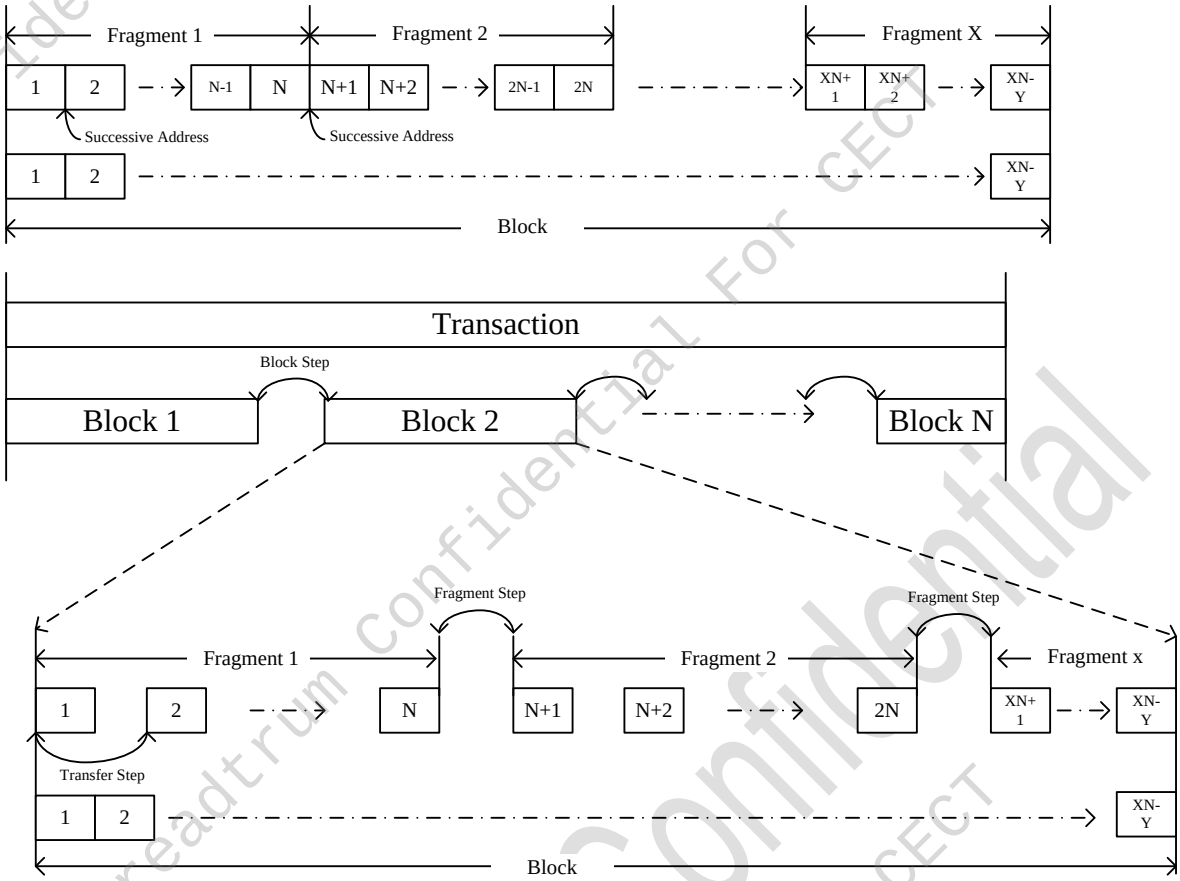
5.7.3.3 Data Structure

For Standard DMA channel



For Full DMA channel

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.



5.7.3.4 DMA Pause

There are two levels of pause action implemented in DMA controller.

One is “controller pause” suitable for the whole DMA controller. Once the controller pause occurred, the DMA controller would stop all the channels after the current fragment/block completed, hold the accepted and subsequently requests. DMA would not sleep during pause state.

The other is “channel pause” suitable for the single DMA channel. When the channel pause occurred, the channel would be temporarily hold and stop all the transfer action.

5.7.3.5 Channel Priority and Arbitration

Each channel may be configured to be one of total 4 level priorities, to effective manage the bandwidth among all logical channels. If there is more than one request occurring, DMA controller would firstly judge their priorities and then select the highest one to serve.

For the channels having the same level priority, DMA controller would serve them by Round-robin way.

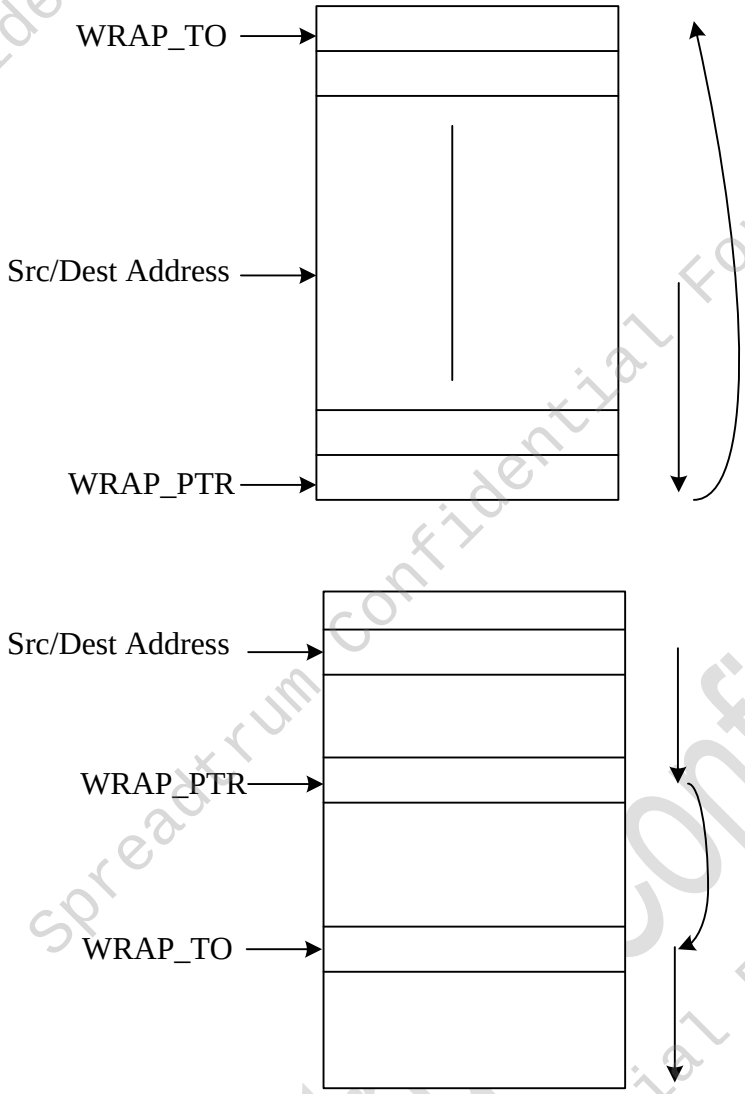
5.7.3.6 Address Fix Mode

Both Standard and Full DMA channel support address-fix transfer, on either source or destination side. This mode is optimized for UART/SPI etc peripherals, and fragment length “FRAG_LEN” would be configured equal to the FIFO watermark.

5.7.3.7 Address Wrap Mode

Full-DMA channel support data movement of ring-buffer and double-buffer, as illustrated below. Once the address reaches the “WPPT”, the next address jumps to the “WPTO” address after completing the “WPPT” data transfer.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.



5.7.3.8 Endian & Data Switch

DMA controller would be configured to be big-endian or little-endian on AHB master ports. The detailed information on AHB big-endian and little-endian would be preferred to AMBA2.0 Specifications.

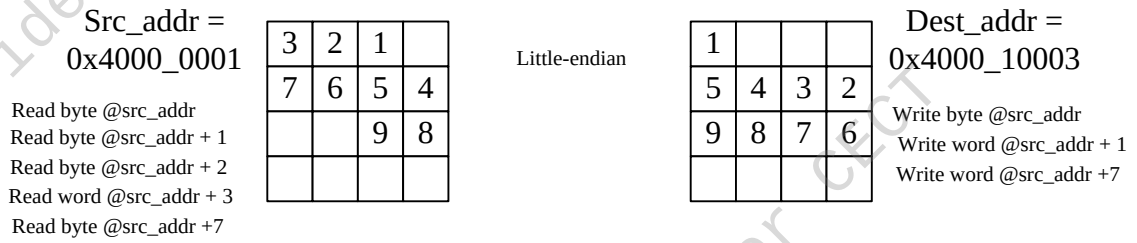
Beside AHB master endian configuration, each channel would separately switch data as scheme below:

5.7.3.9 Un-aligned Word Access

Word access on AHB bus must be address aligned to word boundary. If DMA was configured to read/write un-aligned address with word size, DMA would first read/write 1-3 bytes, and then move word by word. For the last 1-3 bytes, DMA probably had to read/write them by bytes, as illustrated below.

To improve bus efficiency, DMA would directly read unaligned address with word size, and discard redundancy byte when writing to the destination address.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.



For the memory space with un-aligned word access, Byte/Half-word/Word size access must be supported.

For Full DMA channel, if the step of transfer different with the data size (the address is not successive), un-aligned word access would turn to be total byte access.

5.7.3.10 Word Packing

To maximum utilizing internal FIFO, and reduce AHB wait for un-aligned word access, byte or half-word would be packed into word internal DMA.

5.7.3.11 Hardware Request Re-allocated

Every device (peripherals or accelerators) would be assigned to a hardware request, when DMA was implemented in SOC. DMA controller support each hardware request to be re-allocated to the Standard or Full DMA channels.

5.7.3.12 Error Configuration

1. Unaligned word access with un-successive address.
2. Request for transaction or link list in Standard DMA channel.
3. Zero Fragment/block length.
4. Address wrap for Standard Channel.

5.7.4 Control registers

5.7.4.1 Memory map

ARM base address:

Offset Addr	Name	Description
0x1000	DMA_PAUSE	Active High, pause all channels.
0x1004	DMA_FRAG_WAIT	DMA Wait Time Configure
0x1008	REQ_PEND_EN	Pending Requests Enable
0x100C	DMA_INT_RAW_STATUS	DMA Interrupt Raw Status.
0x1010	DMA_INT_MASK_STATUS	DMA Interrupt Mask Status.
0x1014	DMA_REQ_STATUS	DMA Request status.
0x1018	DMA_EN_STATUS	DMA Enable Status.
0x101C	DMA_BEBUG_STATUS	DMA Debug Status
0x1020	DMA_ARB_SEL_STATUS	DMA Arbitrator Selection Status
0x1020–0x0FFC		Reserved.
0x1000 – 0x103C	CHN1 Configure Registers	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Addr	Name	Description
0x1040–0x107C	CHN2 Configure Registers	
0x1080–0x10BC	CHN3 Configure Registers	
0x10C0–0x10FC	CHN4 Configure Registers	
0x1100–0x113C	CHN5 Configure Registers	
0x1140–0x117C	CHN6 Configure Registers	
0x1180–0x11BC	CHN7 Configure Registers	
0x11C0–0x11FC	CHN8 Configure Registers	
0x1200–0x123C	CHN9 Configure Registers	
0x1240–0x127C	CHN10 Configure Registers	
0x1280–0x12BC	CHN11 Configure Registers	
0x12C0–0x12FC	CHN12 Configure Registers	
0x1300–0x133C	CHN13 Configure Registers	
0x1340–0x137C	CHN14 Configure Registers	
0x1380–0x13BC	CHN15 Configure Registers	
0x13C0–0x13FC	CHN16 Configure Registers	
0x1400–0x143C	CHN17 Configure Registers	
0x1440–0x147C	CHN18 Configure Registers	
0x1480–0x14BC	CHN19 Configure Registers	
0x14C0–0x14FC	CHN20 Configure Registers	
0x1500–0x153C	CHN21 Configure Registers	
0x1540–0x157C	CHN22 Configure Registers	
0x1580–0x15BC	CHN23 Configure Registers	
0x15C0–	CHN24 Configure Registers	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Addr	Name	Description
0x15FC		
0x1600–0x163C	CHN25 Configure Registers	
0x1640–0x167C	CHN26 Configure Registers	
0x1680–0x16BC	CHN27 Configure Registers	
0x16C0–0x16FC	CHN28 Configure Registers	
0x1700–0x173C	CHN29 Configure Registers	
0x1740–0x177C	CHN30 Configure Registers	
0x1780–0x17BC	CHN31 Configure Registers	
0x17C0–0x17FC	CHN32 Configure Registers	
0x1800-0x1FFC		Reserved.
0x2000	REQ1_CID	Channel ID for request 1 assignment. Corresponding channel would serve the request 1 after properly configured.
0x2004	REQ2_CID	Same means as “REQ1_CID”
0x2008	REQ3_CID	Same means as “REQ1_CID”
0x200C	REQ4_CID	Same means as “REQ1_CID”
0x2010	REQ5_CID	Same means as “REQ1_CID”
0x2014	REQ6_CID	Same means as “REQ1_CID”
0x2018	REQ7_CID	Same means as “REQ1_CID”
0x201C	REQ8_CID	Same means as “REQ1_CID”
0x2020	REQ9_CID	Same means as “REQ1_CID”
0x2024	REQ10_CID	Same means as “REQ1_CID”
0x2028	REQ11_CID	Same means as “REQ1_CID”
0x202C	REQ12_CID	Same means as “REQ1_CID”
0x2030	REQ13_CID	Same means as “REQ1_CID”
0x2034	REQ14_CID	Same means as “REQ1_CID”
0x2038	REQ15_CID	Same means as “REQ1_CID”
0x203C	REQ16_CID	Same means as “REQ1_CID”
0x2040	REQ17_CID	Same means as “REQ1_CID”
0x2044	REQ18_CID	Same means as “REQ1_CID”
0x2048	REQ19_CID	Same means as “REQ1_CID”

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Addr	Name	Description
0x204C	REQ20_CID	Same means as “REQ1_CID”
0x2050	REQ21_CID	Same means as “REQ1_CID”
0x2054	REQ22_CID	Same means as “REQ1_CID”
0x2058	REQ23_CID	Same means as “REQ1_CID”
0x205C	REQ24_CID	Same means as “REQ1_CID”
0x2060	REQ25_CID	Same means as “REQ1_CID”
0x2064	REQ26_CID	Same means as “REQ1_CID”
0x2068	REQ27_CID	Same means as “REQ1_CID”
0x206C	REQ28_CID	Same means as “REQ1_CID”
0x2070	REQ29_CID	Same means as “REQ1_CID”
0x2074	REQ30_CID	Same means as “REQ1_CID”
0x2078	REQ31_CID	Same means as “REQ1_CID”
0x207C	REQ32_CID	Same means as “REQ1_CID”
0x2080	REQ33_CID	
0x2084	REQ34_CID	
0x2088	REQ35_CID	
0x208C	REQ36_CID	
0x2090	REQ37_CID	
0x2094	REQ38_CID	
0x2098	REQ39_CID	
0x209C	REQ40_CID	
0x20A0	REQ41_CID	
0x20A4	REQ42_CID	
0x20A8	REQ43_CID	
0x20AC	REQ44_CID	
0x20B0	REQ45_CID	
0x20B4	REQ46_CID	
0x20B8	REQ47_CID	
0x20BC	REQ48_CID	
0x20C0	REQ49_CID	
0x20C4	REQ50_CID	
0x20C8	REQ51_CID	
0x20CC	REQ52_CID	
0x20D0	REQ53_CID	
0x20D4	REQ54_CID	
0x20D8	REQ55_CID	
0x20DC	REQ56_CID	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Addr	Name	Description
0x20E0	REQ57_CID	
0x20E4	REQ58_CID	
0x20E8	REQ59_CID	
0x20EC	REQ60_CID	
0x20F0	REQ61_CID	
0x20F4	REQ62_CID	
0x20F8	REQ63_CID	
0x20FC	REQ64_CID	

5.7.4.2 Register description

5.7.4.2.1 **DMA_PAUSE**

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:17]	RO	15'b0	Reserved.
DMA_PAUSE_STATUS	[16]	RO	1'b0	DMA Pause status. 0 : In active state. 1 : In Pause state.
	[15:1]	RO	15'b0	Reserved.
DMA_PAUSE	[0]	RW	1'b0	Active High, pause all the channels. Note: If "DMA_PAUSE" asserted active when the DMA is busy, DMA would finish the current fragment before enter Pause State.

Note:

5.7.4.2.2 **DMA_FRAG_WAIT**

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	32'b0	Reserved.
DMA_FRAG_WAIT	[15:0]	RW	15'b0	Fragment Wait Time. With unit of AHB clock.

Note:

5.7.4.2.3 **REQ_PEND_EN**

Description：

Field Name	Bit	Type	Reset Value	Description
REQ_PEND_EN	[31:0]	RW	32'b0	Requests Pending Enable.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				Acitve high, enable DMA_REQ[31:0] to wakeup DMA, when MCU deep sleep;

Note:

5.7.4.2.4 **DMA_INT_RAW_STATUS**

Description：

Field Name	Bit	Type	Reset Value	Description
DMA_INT_RAW_STATUS	[31:0]	RO	32'b0	DMA 32 Channels Interrupt Raw Status. 0 : No Interrupt need to be served. 1 : Interrupt need to be served.

Note:

5.7.4.2.5 **DMA_INT_MASK_STATUS**

Description：

Field Name	Bit	Type	Reset Value	Description
DMA_INT_MASK_STATUS	[31:0]	RO	32'b0	DMA 32 Channels Interrupt Mask Status. 0 : No Interrupt need to be served. 1 : Interrupt need to be served.

Note:

5.7.4.2.6 **DMA_REQ_STATUS**

Description：

Field Name	Bit	Type	Reset Value	Description
DMA_REQ_STATUS	[31:0]	RO	32'b0	DMA 32 Channels Request Status. 0 : No Request need to be served. 1 : Request need to be served.

Note:

5.7.4.2.7 **DMA_EN_STATUS**

Description：

Field Name	Bit	Type	Reset Value	Description
DMA_EN_STATUS	[31:0]	RO	32'b0	DMA 32 Channels Enable Status. 0 : Channel Not Enabled. 1 : Channel Enabled.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Note:

5.7.4.2.8 **DMA_DEBUG_STATUS**

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:21]	RO	11'b0	Reserved.
DMA_BUSY	[20]	RO	1'b0	DMA Busy Status.
	[19:18]	RO	2'b0	Reserved.
SRC_HREADY	[17]	RO	1'b1	Source Side HREADY status.
DEST_HREADY	[16]	RO	1'b1	Destination Side HREADY status.
	[15:13]	RO	3'b0	Reserved.
MAIN_FSM_STATUS	[12:8]	RO	5'b0	MAIN FSM status.
SRC_FSM_STATUS	[7:4]	RO	4'b0	Source Side FSM status.
DEST_FSM_STATUS	[3:0]	RO	4'b0	Destination Side FSM status.

Note:

5.7.4.2.9 **DMA_ARB_SEL_STATUS**

Field Name	Bit	Type	Reset Value	Description
	[31:6]	RO	26'b0	Reserved.
CHN_ARB_SEL	[5:0]	RO	6'b0	Channel Arbitrator Selection Status;

5.7.4.2.10 **STD_CHN_PAUSE**

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:17]	RO	15'b0	Reserved.
CHN_PAUSE_STATUS	[16]	RO	1'b0	Channel Pause status. If pause the current busy channel, "CHN_PAUSE_STATUS" would be observed after the fragment completed. Otherwise, "CHN_PAUSE_STATUS" would be updated as soon as CHN_PAUSE changed.
	[15:1]	RO	15'b0	Reserved.
CHN_PAUSE	[0]	RW	1'b0	Channel Pause Enable. 0 : Channel in active mode. 1 : Channel pause. Active high, only pause the channel. If the CHN_PAUSE asserted when the channel is busy, it should be paused after the current fragment

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				finished.

Note:

5.7.4.2.11 **STD_CHN_REQ**

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:1]	RO	31'b0	Reserved.
CHN_REQ	[0]	RW	1'b0	Channel Request.

Note:

5.7.4.2.12 **STD_CHN_CFG**

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:24]	RO	8'b0	Reserved.
ERR_TYPE_STATUS	[23:20]	RO	4'b0	Error Configure，which would be cleared when "ERR_INT_STATUS" cleared: 4'b0001 : Addr Wrap Error Configure; 4'b0010 : Request Mode Error Configure; 4'b0100 : Length Error Configure; 4'b1000 :Unalign Error Configure;
	[19:17]	RO	12'b0	
AHB_BURST_SEL	[16]	RW	1'b0	AMBA Burst Select : 1'b0 : INCR8; 1'b1 : INCR4;
	[15:14]	RO	2'b0	Reserved.
CHN_PRIORITY	[13:12]	RW	2'b0	Channel Request Priority. Four level of Priority supported as list : 2'b00 : Lowest priority. 2'b01 : Secondary lowest priority. 2'b10 : Tertiary lowest priority. 2'b11 : Highest priority.
	[11:9]	RO	3'b0	Reserved.
	[8]	RO	1'b0	Reserved for Full DMA channel.
	[7:5]	RO	3'b0	Reserved.
	[4]	RO	1'b0	Reserved for Full DMA channel.
	[3:1]	RO	3'b0	Reserved.
CHN_EN	[0]	RW	1'b0	Channel Enable: 0 : Disable the channel.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				1 : Enable the channel.

Note:

5.7.4.2.13 **STD_CHN_INT**

Description :

Field Name	Bit	Type	Reset Value	Description
	[31:29]	RO	3'b0	Reserved.
CHN_CFG_ERR_INT_CLR	[28]	WO	1'b0	Error interrupt clear.
	[27]	WO	1'b0	Reserved.
	[26]	WO	1'b0	Reserved.
CHN_BLK_INT_CLR	[25]	WO	1'b0	Block done interrupt clear.
CHN_FRAGMENT_INT_CLR	[24]	WO	1'b0	Fragment done interrupt clear.
	[23:21]	RO	3'b0	Reserved.
CHN_CFG_ERR_INT_MASK_STATUS	[20]	RO	1'b0	Configuration error masked interrupt status.
	[19]	RO	1'b0	Reserved.
	[18]	RO	1'b0	Reserved.
CHN_ BLK INT_ MASK _STATUS	[17]	RO	1'b0	Channel Block Masked interrupts status.
CHN_ FRAGMENT_INT_ MASK _STATUS	[16]	RO	1'b0	Channel Fragment Masked interrupts status.
	[15:13]	RO	3'b0	Reserved.
CHN_CFG_ERR_INT_RAW_STATUS	[12]	RO	1'b0	Configuration error raw interrupts status.
	[11]	RO	1'b0	Reserved.
	[10]	RO	1'b0	Reserved.
CHN_ BLK INT_RAW_STATUS	[9]	RO	1'b0	Block done interrupt status.
CHN_ FRAGMENT INT_RAW_STATUS	[8]	RO	1'b0	Fragment done Raw interrupt status.
	[7:5]	RO	3'b0	Reserved.
CHN_CFG_ERR_INT_EN	[4]	RW	1'b0	Configuration error interrupt enable.
	[3]	RO	1'b0	Reserved.
	[2]	RO	1'b0	Reserved.
CHN_BLK_INT_EN	[1]	RW	1'b0	Block done interrupt enable.
CHN_FRAGMENT_INT_EN	[0]	RW	1'b0	Fragment done interrupt enable.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Note:

5.7.4.2.14 **STD_CHN_SRC_ADDR**

Description：

Field Name	Bit	Type	Reset Value	Description
CHN_SRC_ADDR	[31:0]	WR	32’bx	Channel Source Address

Note:

5.7.4.2.15 **STD_CHN_DEST_ADDR**

Description：

Field Name	Bit	Type	Reset Value	Description
CHN_DEST_ADDR	[31:0]	RW	32’bx	Channel Destination Address

Note:

5.7.4.2.16 **STD_CHN_FRAG_LEN**

Description：

Field Name	Bit	Type	Reset Value	Description
SRC_SIZE	[31:30]	RW	2’bx	Source AHB Size. 2’b00 : Byte; 2’b01 : Half Word 2’b10 : Word 2’b11 : Forbidden.
DEST_SIZE	[29:28]	RW	2’bx	Destination AHB Size. 2’b00 : Byte; 2’b01 : Half Word 2’b10 : Word 2’b11 : Forbidden.
SWT_MODE	[27:26]	RW	2’bx	Data Switch mode selection. 2’b00 : ABCD => ABCD; 2’b01 : ABCD => DCBA 2’b10 : ABCD => BADC; 2’b11 : ABCD => CDAB
REQ_MODE	[25:24]	RW	2’bx	Request mode, For Standard DMA channel: 2’b00 : Fragment; 2’b01 : Block; 2’b10 : Forbidden in Standard DMA channel; 2’b11 : Forbidden in Standard DMA channel;
	[23]	RW	1’bx	Reserved for Full DMA channel “WRAP_SEL”. Un-available in Standard DMA channel.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[22]	RW	1'bx	Reserved for Full DMA channel "WRAP_EN". Un-available in Standard DMA channel.
ADDR_FIX_SEL	[21]	RW	6'bx	Selection of the side using Address Fixed mode. 0 : Address Fixed on Source. 1 : Address Fixed on Destination. Only one side of a DMA channel can activate address-Fixed mode at a time.
ADDR_FIX_EN	[20]	RW	1'bx	Address Fixed Enable: 0 : Disable Address Fixed mode. 1 : Enable Address Fixed mode. Active High would make address fixed within the fragment, while "FRAG_STEP" and "BLK_STEP" would be applied to address after fragment done;
	[19]	RW	1'bx	Reserved for Link list end flag. Un-available in Standard DMA channel.
	[18:17]	RW	2'bx	Reserved
FRG_LEN	[16:0]	RW	16'bx	Fragment Length, with byte unit. (Max 128K-1 bytes)

Note:

5.7.4.2.17 **STD_CHN_BLK_LEN**

Description :

Field Name	Bit	Type	Reset Value	Description
	[31:17]	RW	16'bx	Reserved
BLK_LEN	[16:0]	RW	16'bx	Block Length, with byte unit. (Max 128K-1 bytes)

Note:

5.7.4.2.18 **FULL_CHN_PAUSE**

Description :

Field Name	Bit	Type	Reset Value	Description
	[31:17]	RO	15'b0	Reserved.
CHN_PAUSE_STATUS	[16]	RO	1'b0	Channel Pause status.
	[15:1]	RO	15'b0	Reserved.
CHN_PAUSE	[0]	RW	1'b0	Channel Pause Enable. 0 : Channel in active mode. 1 : Channel pause. Active high, only pause the channel. If the CHN_PAUSE asserted when the channel is busy,

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				it should be paused after the current fragment finished.

Note:

5.7.4.2.19 **FULL_CHN_REQ**

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:1]	RO	31'b0	Reserved.
CHN_REQ	[0]	RW	1'b0	Channel Request.

Note:

5.7.4.2.20 **FULL_CHN_CFG**

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:24]	RO	8'b0	Reserved.
ERR_TYPE_STATUS	[23:20]	RO	4'b0	Error Configure，which would be cleared when "ERR_INT_STATUS" cleared: 4'b0001 : Addr Wrap Error Configure; 4'b0010 : Request Mode Error Configure; 4'b0100 : Length Error Configure; 4'b1000 :Unalign Error Configure;
	[19:17]	RO	3'b0	
AHB_BURST_SEL	[16]	RW	1'b0	AMBA Burst Select： 1'b0 : INCR8 ; 1'b1 : INCR4;
	[15:14]	RO	3'b0	Reserved.
CHN_PRIORITY	[13:12]	RW	2'b0	Channel Request Priority. Four level of Priority supported as list : 2'b00 : Lowest priority. 2'b01 : Secondary lowest priority. 2'b10 : Tertiary lowest priority. 2'b11 : Highest priority.
	[11:9]	RO	3'b0	Reserved.
LLIST_CFG_VALID	[8]	RW	1'b0	If "LLIST_EN" asserted, active high indicates Link list configure valid. 0 : Link list configure in-valid. DMA controller need obtain link list configure information by link list pointer. 1 : link list configure information valid. DMA controller would continue to complete the node

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				and clear this bit. Note: Strongly recommend to observe only. Carefully writing to this bit, which may cause DMA crashed. If had to do so, pause this channel before changing.
	[7:5]	RO	3'b0	Reserved.
LLIST_EN	[4]	RW	1'b0	Link list Enable, only available for full DMA channel. 0 : Disable the link list. 1 : Enable the link list.
	[3:1]	RO	3'b0	Reserved.
CHN_EN	[0]	RW	1'b0	Channel Enable: 0 : Disable the channel. 1 : Enable the channel.

Note:

5.7.4.2.21 **FULL_CHN_INT**

Description :

Field Name	Bit	Type	Reset Value	Description
	[31:29]	RO	3'b0	Reserved.
CHN_CFG_ERR_INT_CLR	[28]	WO	1'b0	Configuration error interrupt clear.
CHN_LLIST_INT_ CLR	[27]	WO	1'b0	Link list done interrupt clear
CHN_TRSC_INT_ CLR	[26]	WO	1'b0	Transaction done interrupt clear
CHN_BLK_INT_ CLR	[25]	WO	1'b0	Block done interrupt clear.
CHN_FRAGMENT_INT_ CLR	[24]	WO	1'b0	Fragment done interrupt clear.
	[23:21]	RO	3'b0	Reserved.
CHN_CFG_ERR_INT_MASK_STATUS	[20]	RO	1'b0	Configuration error masked interrupt status.
CHN_ LLIST INT_MASK_STATUS	[19]	RO	1'b0	Channel Link list Masked interrupt status.
CHN_ TRSC INT_ MASK _STATUS	[18]	RO	1'b0	Channel Transaction Masked interrupts status.
CHN_ BLK_INT_ MASK _STATUS	[17]	RO	1'b0	Channel Block Masked interrupts status.
CHN_ FRAGMENT_INT_ MASK _STATUS	[16]	RO	1'b0	Channel Fragment Masked interrupts status.
	[15:13]	RO	3'b0	Reserved.
CHN_CFG_ERR_INT_RAW_STATUS	[12]	RO	1'b0	Configuration error raw interrupts status.
CHN_ LLIST INT_RAW_STATUS	[11]	RO	1'b0	Channel Link List interrupts status.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

CHN_ TRSC INT_RAW_STATUS	[10]	RO	1'b0	Channel Transaction interrupts status.
CHN_ BLK_INT_RAW_STATUS	[9]	RO	1'b0	Block done interrupt status.
CHN_FRAGMENT_INT_RAW_STATUS	[8]	RO	1'b0	Fragment done Raw interrupt status.
	[7:5]	RO	3'b0	Reserved.
CHN_CFG_ERR_INT_EN	[4]	RW	1'b0	Configuration error interrupt enable.
CHN_LLIST_INT_EN	[3]	RW		Link list done interrupt enable
CHN_TRSC_INT_EN	[2]	RW		Transaction done interrupt enable
CHN_BLK_INT_EN	[1]	RW	1'b0	Block done interrupt enable.
CHN_FRAGMENT_INT_EN	[0]	RW	1'b0	Fragment done interrupt enable.

Note:

5.7.4.2.22 **FULL_CHN_SRC_ADDR**

Description :

Field Name	Bit	Type	Reset Value	Description
CHN_SRC_ADDR	[31:0]	WR	32'bx	Channel Source Address

Note:

5.7.4.2.23 **FULL_CHN_DEST_ADDR**

Description :

Field Name	Bit	Type	Reset Value	Description
CHN_DEST_ADDR	[31:0]	RW	32'bx	Channel Destination Address

Note:

5.7.4.2.24 **FULL_CHN_FRAG_LEN**

Description :

Field Name	Bit	Type	Reset Value	Description
SRC_SIZE	[31:30]	RW	2'bx	Source AHB Size. 2'b00 : Byte; 2'b01 : Half Word 2'b10 : Word 2'b11 : Forbidden.
DEST_SIZE	[29:28]	RW	2'bx	Destination AHB Size.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				2'b00 : Byte; 2'b01 : Half Word 2'b10 : Word 2'b11 : Forbidden.
SWT_MODE	[27:26]	RW	2'bx	Data Switch mode selection. 2'b00 : ABCD => ABCD; 2'b01 : ABCD => DCBA 2'b10 : ABCD => BADC; 2'b11 : ABCD => CDAB
REQ_MODE	[25:24]	RW	2'bx	Request mode, For Full DMA channel: 2'b00 : Fragment; 2'b01 : Block; 2'b10 : Transaction; 2'b11 : Link List;
ADDR_WRAP_SEL	[23]	RW	1'bx	Selection of the side using Address wrap mode. 0 : Address wrap on Source. 1 : Address wrap on Destination. Only one side of a DMA channel can activate address-wrapping mode at a time.
ADDR_WRAP_EN	[22]	RW	1'bx	Active High enable Address-wrapping for ring buffer. The next address of DMA jumps to "WRAP_START_ADDR" address when the current address matches "WRAP_END_ADDR" address: 0 : Disable address wrap mode. 1 : Enable address wrap mode. "WRAP_START_ADDR" and "WRAP_END_ADDR" would be used to limit the address space of either Source or Destination.
ADDR_FIX_SEL	[21]	RW	6'bx	Selection of the side using Address Fix mode. 0 : Address Fix on Source. 1 : Address Fix on Destination. Only one side of a DMA channel can activate address- Fix mode at a time.
ADDR_FIX_EN	[20]	RW	1'bx	Address Fix Enable: 0 : Disable Address Fix mode. 1 : Enable Address Fix mode. Active High would make address fixed within the fragment, while "FRAG_STEP" and "BLK_STEP" would be applied to address after fragment done;
LLIST_END	[19]	RW	1'bx	Link list end flag. Active only when "LLIST_EN" asserted.
BLK_LEN_REC_H	[18:17]	RW	2'bx	Block counter[16:15], update after each fragment done; Note: Normally configured to 2'b0. Only to be configured other value during state retention after wake up
FRG_LEN	[16:0]	RW	17'bx	Fragment Length, with byte unit. (Max 128K-1

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				bytes)

Note:

5.7.4.2.25 **FULL_CHN_BLK_LEN**

Description：

Field Name	Bit	Type	Reset Value	Description
BLK_LEN_REC_L	[31:17]	RW	15'bx	Block counter[14:0], update after each fragment done; Note: Normally configured to 15'b0. Only to be configured other value during state retention after wake up
BLK_LEN	[16:0]	RW	17'bx	Block Length, with byte unit. (Max 128K-1 bytes)

Note:

5.7.4.2.26 **FULL_CHN_TRSC_LEN**

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RW	4'bx	Reserved.
TRSC_LEN	[27:0]	RW	28'bx	Transaction Length, with byte unit. (Max 256M-1 bytes)

Note:

5.7.4.2.27 **FULL_CHN_TRSF_STEP**

Description：

Field Name	Bit	Type	Reset Value	Description
DEST_TRSF_STEP	[31:16]	RW	16'bx	Channel Source side transfer step, with byte unit.
SRC_TRSF_STEP	[15:0]	RW	16'bx	Channel destination side transfer step, with byte unit.

Note:

5.7.4.2.28 **FULL_CHN_WRAP_PTR**

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RW	4'bx	Reserved.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

WRAP_PTR	[27:0]	RW	28'bx	Wrap jump pointer address. Once the transfer address reaches WPPT, the next address jumps to the WPTO address after completing the WPPT data transfer.

Note:

5.7.4.2.29 **FULL_CHN_WRAP_TO**

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RW	4'bx	Reserved.
WRAP_TO	[27:0]	RW	28'bx	Wrap jump-to address. Once the transfer address reaches WPPT, the next address jumps to the WPTO address after completing the WPPT data transfer.

Note:

5.7.4.2.30 **FULL_CHN_LLIST_PTR**

Description：

Field Name	Bit	Type	Reset Value	Description
LLIST_PTR	[31:0]	RW	26'bx	Link List pointer.

Note:

5.7.4.2.31 **FULL_CHN_FRAG_STEP**

Description：

Field Name	Bit	Type	Reset Value	Description
DEST_FRAG_STEP	[31:16]	RW	16'bx	Channel Destination side transfer step. With byte unit.
SRC_FRAG_STEP	[15:0]	RW	16'bx	Channel Source side transfer step. With byte unit.

Note:

5.7.4.2.32 **FULL_CHN_SRC_BLK_STEP**

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RW	4'bx	Reserved.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

CHN_SRC_BLK_STEP	[27:0]	RW	32'bx	Channel Source block step. With byte unit.

Note:

5.7.4.2.33 **FULL_CHN_DEST_BLK_STEP**

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:28]	RW	4'bx	Reserved.
CHN_DEST_BLK_STEP	[27:0]	RW	32'bx	Channel Destination block step. With byte unit.

Note:

5.7.4.2.34 **REQ1_CID**

Description：

Field Name	Bit	Type	Reset Value	Description
	[31:5]	RW	26'b0	Reserved.
REQ1_CID	[5:0]	RW	6'b0	REQ1 Channel Identified Number.

5.7.5 Application notes

Fix 'dma_busy' issue when channel pause.

Extend "frag_len" and "blk_len" from 16 bit to 17 bits;

Fix Definition issue.

In Standard Channel, "frag_len" would be larger or smaller or equal to "blk_len", and "blk_len" would be updated after each "frag_len" completed. "blk_cnt" would be no longer exists. "blk_len_rec_h/l" not available in Standard Channel.

In Full Channel, "Frag_len", "blk_len" and "trsc_len" would be any relationship of size. "blk_len" would not be updated after "frag_len" completed and "blk_len_rec_h/l" would be updated.

Register "STD_CHN_FRAG_LEN" and "STD_CHN_BLK_LEN" changed.

5.8 Interrupt Controller (Intc)

5.8.1 Overview

Interrupt Controller generate a IRQ and FIQ to MCU from 32 IRQ and 32 FIQ channels.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.8.2 Features

- Provide 30 hardware-triggered IRQ channels from IRQ channel 2 to channel 31
- Provide 30 hardware-triggered FIQ channels from FIQ channel 2 to channel 31
- Provide 1 software-triggered IRQ channel from IRQ channel 1
- Provide 1 software-triggered FIQ channel from FIQ channel 1
- Provide 1 special IRQ channel from IRQ channel 0
- Provide 1 special FIQ channel from FIQ channel 0
- Each IRQ or FIQ channel can be enabled or disabled independently
- Provide raw status for each IRQ or FIQ channel
- Provide masked status for each IRQ or FIQ channel

5.8.3 Signal description

Null

5.8.4 Interrupt Source Assignment

The following table shows the detailed channel assignment for both IRQ and FIQ.

Table 5-11 Interrupt Source Map

Channel Number	Source	
0	Special latch channel	0: UART0 RXD
		1: UART0 CTSN
		2: UART1 RXD
		3: UART2 RXD
		4: UART2 CTSN
		5: USB Input SE0
1	Software-trigged channel	
2	COMMRX	
3	COMMTX	
4	Tmr0_irq	
5	Tmr1_irq	
6	Tmr2_irq	
7	Tmr3_irq	
8	Tmr4_irq	
9	Tmr5_irq	
10	Gpio_irq	
11	eic_dbc_irq | Eic_sync_irq | eic_async_irq	
12	Kpd_irq	
13	I2c0_irq	
14	i2c1_irq	
15	i2c2_irq	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

16	aud_irq
17	SIM Interrupt
18	Uart0_irq
19	Uart1_irq
20	Uart2_irq
21	DSP IRQ or DSP FIQ
22	Lcdc_irq
23	Gea_irq
24	Sys_tmr
25	Spi0_irq
26	Spi1_irq
27	Bus monitor0 irq
28	Bus monitor1 irq
29	Bus monitor2 irq
30	Bus monitor3 irq
31	DMA irq
32	Reseved
33	Reserved
34	VBC irq
35	ADI irq
36	Ana_irq
37	USBD_irq
38	DCAM_irq
39	IIS Interrupt
40	SDIO_irq
41	ARM7 irq/frq
42	ARM7 timer irq
43	MIDI_irq
44	FM_irq|
45	ZIP0_irq
46	ZIP1_irq
47	SFC_irq
48	ARM7 Watch Dog irq
49-63	Reserved

Spreadtrum Confidential

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.8.5 Funtion description

Interrupt Controller generate a IRQ to MCU from 32 IRQ channels, including 30 hardware-triggered IRQ channels, 1 software-triggered IRQ channel and 1 special IRQ channel.

Interrupt Controller also generate a FIQ to MCU from 32 FIQ channels, including 30 hardware-triggered FIQ channels, 1 software-triggered FIQ channel and 1 special FIQ channel.

32 IRQ channels are independent from 32 FIQ channels; they can be connected or configured independently. Following is the function diagram of Interrupt Controller.

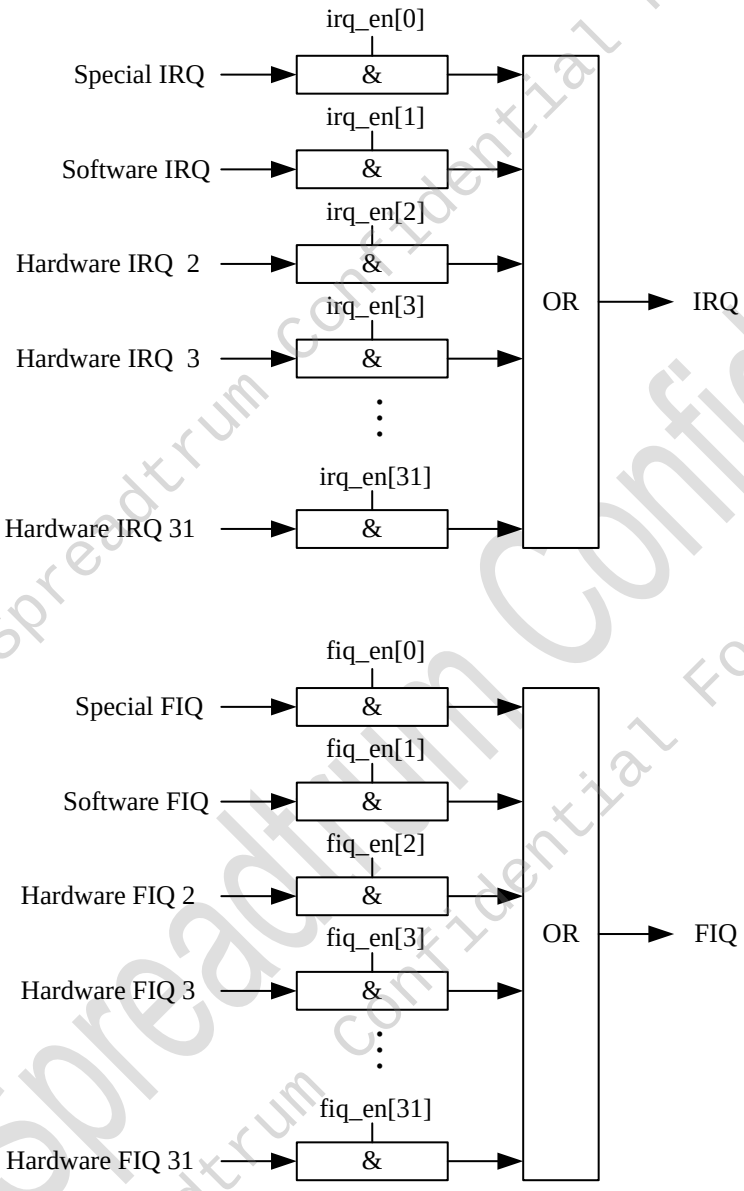


Figure 5-70 function diagram of Interrupt Controller

5.8.5.1 Hardware-Triggered Channels

There are 30 hardware-triggered IRQ channels, from IRQ channels 2 to IRQ channel 31. Also there are 30 hardware-triggered FIQ channels, from FIQ channels 2 to FIQ channel 31. They are independent from each other and can be connected to different hardware module interrupt.

The hardware-triggered function is the main function provided by the interrupt controller. The controller collects interrupt trigger signals from different hardware modules, applies mask on them and generates MCU FIQ and IRQ. The controller only supports level

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

triggering, and triggering level is high active. There is no DFF or latch to keep status on the hardware-triggered channel path. So this controller can be used to wakeup MCU sub-system during sleep with no working clock, but it needs each source latches the interrupt status.

Each Hardware-Triggered channel can have more than 1 interrupt sources if they are “OR” together.

5.8.5.2 Software-Triggered Channel

There is one software-triggered IRQ channel and FIQ channel, assigned on IRQ channel 1 and FIQ channel 1. These two software-triggered are independent and can be set or clear individually. The function is similar to other hardware interrupts. The difference between them is that the software-triggered interrupt is issued in interrupt controller by setting one bit. Similarly, this interrupt can be cleared by just clearing this bit. This interrupt cannot wake up the system.

5.8.5.3 Special Channel

There is one special IRQ channel and FIQ channel, assigned on IRQ channel 0 and FIQ channel 0. These two channels are special because they are connected with off-chip interrupt to wakeup MCU sub-system. However inside the Interrupt Controller they are the same priority and function with other channels.

5.8.6 Control registers

5.8.6.1 Memory map

ARM base address: 0x8000_0000

Offset Address	Name	Description
0x1000	INT_IRQ_MASK_STS	IRQ masked status
0x1004	INT_IRQ_RAW_STS	IRQ raw status
0x1008	INT_IRQ_ENABLE	IRQ enable control
0x100C	INT_IRQ_DISABLE	IRQ disable control
0x1010	INT_IRQ_SOFT	IRQ software interrupt trig
0x1014	INT_IRQ_TEST_SRC	IRQ test source generating
0x1018	INT_IRQ_TEST_SEL	IRQ test select
0x1020	INT_FIQ_MASK_STS	FIQ masked status
0x1024	INT_ FIQ_RAW_STS	FIQ raw status
0x1028	INT_ FIQ_ENABLE	FIQ enable control
0x102C	INT_ FIQ_DISABLE	FIQ disable control
0x1030	INT_ FIQ_SOFT	FIQ software interrupt trig
0x1034	INT_ FIQ_TEST_SRC	FIQ test source generating
0x1038	INT_ FIQ_TEST_SEL	FIQ test select

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.8.6.2 Register description

5.8.6.2.1 INT_IRQ_MASK_STS

Description：IRQ masked status

0x1000			IRQ masked status (reset 0x0)										INT_IRQ_MASK_STS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_IRQ_MASK_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_IRQ_MASK_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_IRQ_MASK_STS	[31:0]	RO	32'h0	IRQ interrupt channel masked status One bit for one channel Active high

5.8.6.2.2 INT_IRQ_RAW_STS

Description：IRQ raw status

0x1004			IRQ raw status (reset 0x0)										INT_IRQ_RAW_STS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_IRQ_RAW_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_IRQ_RAW_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
INT_IRQ_RAW_STS	[31:0]	RO	32'h0	IRQ interrupt channel raw status One bit for one channel Active high

5.8.6.2.3 **INT_IRQ_ENABLE**

Description：IRQ enable control

0x1008	IRQ enable control (reset 0x0)															**INT_IRQ_ENABLE**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_IRQ_ENABLE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_IRQ_ENABLE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_IRQ_ENABLE	[31:0]	R/W	32'h0	IRQ interrupt channel enable One bit for one channel Write 1 to corresponding bit to enable the corresponding interrupt channel. Write 0 to any bit is DO NOT CARE. Write 1 to corresponding bit in INT_IRQ_DISABLE to clear enable bit. Read status: 0: related channel is disabled 1: related channel is enabled

5.8.6.2.4 **INT_IRQ_DISABLE**

Description：IRQ disable control

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x100c		IRQ disable control (reset 0x0)										INT_IRQ_DISABLE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_IRQ_DISABLE															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_IRQ_DISABLE															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_IRQ_DISABLE	[31:0]	WO	32'h0	IRQ interrupt channel disable One bit for one channel Write 1 to corresponding bit to disable the corresponding interrupt channel. Write 0 to any bit is DO NOT CARE.

5.8.6.2.5 **INT_IRQ_SOFT**

Description：IRQ software interrupt

0x1010		IRQ software interrupt (reset 0x0)													INT_IRQ_SOFT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														INT_IRQ_SOFT	Reserved
Type	RO														WO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
	[31:2]	RO	30'h0	Reserved
INT_IRQ_SOFT	[1]	WO	1'h0	IRQ software interrupt Write 1 to active the software interrupt. Write 0 to clear the software interrupt.
	[0]	RO	1'h0	Reserved

5.8.6.2.6 **INT_IRQ_TEST_SRC**

Description：Test mode control: source generating

0x1014	IRQ test source generating (reset 0x0)															**INT_IRQ_TEST_SRC**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_IRQ_TEST_SRC															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_IRQ_TEST_SRC														Reserved	INT_IRQ_TEST_SRC
Type	R/W														RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_IRQ_TEST_SRC	[31:0]	R/W	32'h0	IRQ test mode control for source generating One bit for one channel, the bit[1] is reserved. This register is only used in test mode. When INT_IRQ_TEST_SEL is 1, Write 1 to corresponding bit to generate INT_IRQ_RAW_STS. If the corresponding channel is enabled, IRQ to MCU and INT_IRQ_MASK_STS is also generated.

5.8.6.2.7 **INT_IRQ_TEST_SEL**

Description：Test mode control: test select

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1018			IRQ test select (reset 0x0)										INT_IRQ_TEST_SEL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															INT_IRQ_TEST_SEL
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

~~Field Name~~	Bit	Type	Reset Value	Description
	[31:1]	RO	31'h0	Reserved
INT_IRQ_TEST_SEL	[0]	R/W	1'h0	IRQ test mode enable Write 1 to enter test mode. In normal condition, this register MUST be configured to 0.

5.8.6.2.8 **INT_FIQ_MASK_STS**

Description：FIQ masked status

0x1020			FIQ masked status (reset 0x0)										INT_FIQ_MASK_STS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_FIQ_MASK_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_FIQ_MASK_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
INT_FIQ_MASK_STS	[31:0]	RO	32'h0	FIQ interrupt channel masked status One bit for one channel Active high

5.8.6.2.9 **INT_FIQ_RAW_STS**

Description：FIQ raw status

0x1024	FIQ raw status (reset 0x0)												**INT_FIQ_RAW_STS**			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_FIQ_RAW_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_FIQ_RAW_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_FIQ_RAW_STS	[31:0]	RO	32'h0	FIQ interrupt channel raw status One bit for one channel Active high

5.8.6.2.10 **INT_FIQ_ENABLE**

Description：FIQ enable control

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1028			FIQ enable control (reset 0x0)										INT_FIQ_ENABLE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_FIQ_ENABLE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_FIQ_ENABLE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_FIQ_ENABLE	[31:0]	R/W	32'h0	FIQ interrupt channel enable One bit for one channel Write 1 to corresponding bit to enable the corresponding interrupt channel. Write 0 to any bit is DO NOT CARE. Write 1 to corresponding bit in INT_FIQ_DISABLE to clear enable bit. Read status: 0: related channel is disabled 1: related channel is enabled

5.8.6.2.11 **INT_FIQ_DISABLE**

Description：FIQ disable control

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x102c			FIQ disable control (reset 0x0)													INT_FIQ_DISABLE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_FIQ_DISABLE															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_FIQ_DISABLE															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_FIQ_DISABLE	[31:0]	WO	32'h0	FIQ interrupt channel disable One bit for one channel Write 1 to corresponding bit to disable the corresponding interrupt channel. Write 0 to any bit is DO NOT CARE.

5.8.6.2.12 **INT_FIQ_SOFT**

Description：FIQ software interrupt

0x1030			FIQ software interrupt (reset 0x0)													INT_FIQ_SOFT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														INT_FIQ_SOFT	Reserved
Type	RO														WO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
	[31:2]	RO	30'h0	Reserved
INT_FIQ_SOFT	[1]	WO	1'h0	FIQ software interrupt Write 1 to active the software interrupt. Write 0 to clear the software interrupt.
	[0]	RO	1'h0	Reserved

5.8.6.2.13 **INT_FIQ_TEST_SRC**

Description：Test mode control: source generating

0x1034	FIQ test source generating (reset 0x0)														INT_FIQ_TEST_SRC	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_FIQ_TEST_SRC															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	INT_FIQ_TEST_SRC														Reserved	INT_FIQ_TEST_SRC
Type	R/W														RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_FIQ_TEST_SRC	[31:0]	R/W	32'h0	IRQ test mode control for source generating One bit for one channel, the bit[1] is reserved. This register is only used in test mode. When INT_FIQ_TEST_SEL is 1, Write 1 to corresponding bit to generate INT_FIQ_RAW_STS. If the corresponding channel is enabled, FIQ to MCU and INT_FIQ_MASK_STS is also generated.

5.8.6.2.14 **INT_FIQ_TEST_SEL**

Description：Test mode control: test select

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1038			FIQ test select (reset 0x0)													INT_FIQ_TEST_SEL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															INT_FIQ_TEST_SEL
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:1]	RO	31'h0	Reserved
INT_FIQ_TEST_SEL	[0]	R/W	1'h0	FIQ test mode enable Write 1 to enter test mode. In normal condition, this register MUST be configured to 0.

5.8.7 Application notes

Interrupt Control's PCLK is open by default, so Software needs not to enable any bit and can access the register directly.

For IRQ and FIQ, the most important function is in the 30 hardware channel. They are connected to different hardware module. Make sure that all the hardware modules' interrupt is level triggering, and triggering level is active high. Once interrupt is generated, it should kept high until software clear it by setting interrupt clear bit in corresponding module. Following is the recommended flow for hardware channels.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

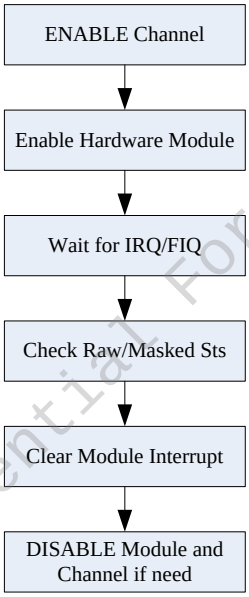


Figure 5-71 recommended flow for hardware channels

5.9 BUS Monitor

5.9.1 Overview

SC6531 contains multi-layer AHB bus, and each layer contains AHB masters and slaves. Bus monitors could monitor the bus access and provide the interrupts when a target data reading from or writing to a target address. Only CHN_INT register(0x10) could be cleared after reset, other registers would not be effected by reset.

Besides, bus monitors provide the bus uasage to analyze system performace.

5.9.2 Features

SC6531 bus monitor supports the following features:

- Support AMBA AHB bus Read and Write monitoring;
- Support AHB byte/half-word/word access monitoring;
- Support AHB 32-bit data bus monitoring, by 32-bit data mask;
- Support AHB 32-bit address space monitoring, for any address between minimal and maximum setting;
- Support interrupt raw/mask status and interrupt enable;
- Support triggered HADDR/HDATA/HSIZE/HBURST status.

5.9.3 Bus Monitor Assignment

SC6531 ARM9 side contains 13 AHB masters and 4 bus monitors, that is, only 4 AHB masteres can be monitored at a given timen. The bus moitors assignment is illustrated below.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Table 5-12 ARM9 Side Bus Monitor Assignment

~~Busmon Num~~	~~CH0~~	~~CH1~~	~~CH2~~	~~CH3~~
~~Bus Monitor0~~	~~ARM926EJ-S Data AHB master~~	~~LZMA1~~	~~Master Port for ARM7 to access EMC space~~	~~Master Port for ARM7 to access none EMC space~~
~~Bus Monitor1~~	~~LCDC acess to EMC~~	~~LCDC acess to LCM~~	~~DMAR~~	~~DMAW~~
~~Bus Monitor2~~	~~SDIO~~	~~DCAM~~	~~MIDI~~	~~ARM926EJ-S Instruction AHB master~~
~~Bus Monitor3~~	~~LZMA0~~	~~REV~~	~~REV~~	~~REV~~

~~Matrix have 12 masters, busmon1/2/3 have been delete, only busmon0 left.~~

~~Busmon chn~~	~~Busmon0_chn_mux=1~~	~~Busmon0_chn_mux=0~~ ~~Busmon0_chn0_mux=1~~ ~~Busmon0_chn1_mux=1~~ ~~Busmon0_chn2_mux=1~~	~~Busmon0_chn_mux=0~~ ~~Busmon0_chn0_mux=0~~ ~~Busmon0_chn1_mux=1~~ ~~Busmon0_chn2_mux=1~~
~~Chn 0~~	~~ARM926EJ-S Data AHB master~~	~~SDIO~~	~~LZMA0~~
~~Chn 1~~	~~ARM926EJ-S Instruction AHB master~~	~~DCAM~~	~~LCDC acess to EMC~~
~~Chn 2~~	~~Master Port for ARM7 to access EMC space~~	~~Master Port for ARM7 to access none EMC space~~	~~LCDC acess to LCM~~
~~Chn 3~~	~~DMAW~~	~~DMAR~~	~~REV~~

Matrix have 12 masters, busmon1/2/3 have been delete, only busmon0 left.

Busmon chn	Busmon0_chn_mux=1	Busmon0_chn_mux=0 Busmon0_chn0_mux=1	Busmon0_chn_mux=0 Busmon0_chn0_mux=0
Chn 0	ARM926EJ-S Data AHB master	SDIO	LZMA0
Chn 1	ARM926EJ-S Instruction AHB master	DCAM	LCDC acess to EMC
Chn 2	Master Port for ARM7 to access EMC space	Master Port for ARM7 to access none EMC space	LCDC acess to LCM
Chn 3	DMAW	DMAR	REV

There are one bus monitors in the system and the address mapping as the follows.

Table 5-13 ARM9 Side Bus Monitors Address Map

Busmon Num	Offset Address Range
ARM Bus Monitor0	0x2040_0000 - 0x2040_0028

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

~~ARM Bus Monitor1~~	~~0x2040_1000 - 0x2040_1024~~
~~ARM Bus Monitor2~~	~~0x2040_2000 - 0x2040_2024~~
~~ARM Bus Monitor3~~	~~0x2040_3000 - 0x2040_3024~~

SC6531 ARM7 side contains 3 AHB masters and 1 bus monitors, that is. The bus moitors assignment is illustrated below.

Table 5-17 ARM7 Side Bus Monitor Assignment

Busmon Num	CH0	CH1	CH2	CH3
Bus Monitor0	CM4 I cache	CM4 D cahce	CM4 S(addr > 0x20000000)(M2)	ARM9 to CM4 Master(M3)

There is one bus monitorsin the system and the address mapping as the follows.

Table 5-18 ARM7 Side Bus Monitors Address Map

Busmon Num	Offset Address Range
ARM Bus Monitor0	0x5040_0000 –0x5040_0FFF

5.9.4 Control registers

5.9.4.1 Memory Map

ARM base address: 0x2040_0000

Offset Address	Register Name	Register Description
0x0000	CHN_INT	Channel interrupt configure.
0x0004	CHN_CFG	AHB feature configure.
0x0008	ADDR_MIN	Minimum address for monitoring.
0x000C	ADDR_MAX	Maximum address for monitoring.
0x0010	ADDR_MASK	Addr mask for monitoring.
0x0014	DATA_MIN	Minimum data for monitoring.
0x0018	DATA_MAX	Maximum data for monitoring.
0x001C	DATA_MASK	Data mask for monitoring.
0x0020	MATCH_ADDR	Matched address which triggered interrupt.
0x0024	MATCH_DATA	Matched data which triggered interrupt.
0x0028	BUSMON_CNT	Performance counter.

5.9.4.2 Register Descriptions

5.9.4.2.1 CHN_INT

Description：Channel interrupt configure.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0000			Channel interrupt configure. (Reset to 0x1000_0000)													CHN_INT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	INT_MASK_STATUS	INT_RAW_STATUS	INT_CLR	INT_EN	Reserved.											
Type	RO	RO	WO	RW	RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved.										CNT_SEL		CNT_CLR	CNT_HOLD	CNT_EN	CHN_EN
Type	RO										RW		WO	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
INT_MASK_STATUS	[31]	RO	‘b0	Interrupt Mask status and should be cleared by asserting INT_CLR; Only would be active when INT_EN active high.
INT_RAW_STATUS	[30]	RO	‘b0	Interrupt raw status and should be cleared by asserting INT_CLR;
INT_CLR	[29]	WO	‘b0	Writing “1” to this bit will clear the interrupt raw status;
INT_EN	[28]	RW	‘b0	0 : By default, disable busmon interrupt; 1 : Enable busmon interrupt;
	[27:6]	RO	‘b0	Reserved.
CNT_SEL	[5:4]	RW	‘b0	Counter type as following: 2’b00: Busmon Enable; 2’b01: AHB Transcation; 2’b10: AHB Transcation with HREADY; 2’b11: Data Size;
CNT_CLR	[3]	RW	‘b0	Busmon Cnt clear, writing “1” to this bit will clear busmon cnt to zero;
CNT_HOLD	[2]	RW	‘b0	Transaction Counter hold, active HIGH will hold the counter;
CNT_EN	[1]	RW	‘b0	Transaction Counter Enable; 0 : Disable counter; 1 : Enable counter;
CHN_EN	[0]	RW	‘b0	Channel enable: 0: by default, disable bus monitor; 1: Enable bus monitor;

5.9.4.2.2 **CHN_CFG**

Description：AHB feature configure.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0004			AHB feature configure. (Reset to 0x1000_0000)										CHN_CFG			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved.												BURST_CFG			BURST_EN
Type	RO												RW			RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MASTER_CFG				Reserved.			MASTER_EN	SIZE_CFG			SIZE_EN	Reserved		WRITE_CFG	WRITE_EN
Type	RW				RO			RW	RW			RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:20]	RO	‘b0	Reserved.
BURST_CFG	[19:17]	RW	‘b0	AHB HBURST definition: 3’b000 : Single; 3’b001 : INCR; 3’b010 : WRAP4; 3;b011 : INCR4; 3’b100 : WRAP8; 3’b101 : INCR8; 3’b110 : WRAP16; 3’b111 : INCR16;
BURST_EN	[16]	RW	‘b0	HBURST type monitoring enable: 0 : Disable HBURST monitoring; 1 : Enable HBURST monitoring;
MASTER_CFG	[15:12]	RW	‘b0	HMASTER.
	[11:9]	RO	‘b0	Reserved.
MASTER_EN	[8]	RW	‘b0	AHB Hmaster enable, Must be set as default 0.
SIZE_CFG	[7:5]	RW	‘b0	AHB HSIZE monitoring: 000: Byte; 001: Half-word; 010: Word; Others: reserved.
SIZE_EN	[4]	RW	‘b0	HSIZE type monitoring enable; 0 : Disable HSIZE monitoring; 1 : Enable HSIZE monitoring;
	[3:2]	RW	‘b0	Reserved
WRITE_CFG	[1]	RW	‘b0	HWRITE for monitoring:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				0 : HWRITE = 1'b0, read transaction; 1: HWRITE = 1'b1, write transaction;
WRITE_EN	[0]	RW	'b0	HWRITE type monitoring enable; 0 : Dis-able HWRITE monitoring; 1 : Enable HWRITE monitoring;

5.9.4.2.3 **ADDR_MIN**

Description：Minimum address for monitoring.

0x0008			**Minimum address for monitoring. (Reset to 0x1000_0000)**													**ADDR_MIN**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	ADDR_MIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ADDR_MIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
ADDR_MIN	[31: 0]	RW	'b0	AHB minimal address for monitoring; Any access between Max and Min address space may trigger interrupt;

5.9.4.2.4 **ADDR_MAX**

Description：Maximum address for monitoring.

0x000C			**Maximum address for monitoring. (Reset to 0x1000_0000)**													**ADDR_MAX**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	ADDR_MAX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ADDR_MAX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
ADDR_MAX	[31: 0]	RW	'b0	AHB maxium address for monitoring; Any access between Max and Min address

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				space may trigger interrupt;

5.9.4.2.5 **ADDR_MASK**

Description：

0x0010			. (Reset to X)													ADDR_MASK
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	ADDR_MASK															
Type	RW															
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ADDR_MASK															
Type	RW															
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Field Name	Bit	Type	Reset Value	Description
ADDR_MASK	[31: 0]	RW	32‘hx	Address_mask, active high makes the address of corresponding bits to be masked, and ignored during comparation.

5.9.4.2.6 **DATA_MIN**

Description：Minimum data for monitoring.

0x0014			Minimum data for monitoring. (Reset to 0x1000_0000)													DATA_MIN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DATA_MIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DATA_MIN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
DATA_MIN	[31: 0]	RW	‘b0	AHB minimal DATA for monitoring; Any access between Max and Min data space may trigger interrupt;

5.9.4.2.7 **DATA_MAX**

Description：Maximum data for monitoring.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0018			Maximum data for monitoring. (Reset to 0x1000_0000)										DATA_MAX			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DATA_MAX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DATA_MAX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
DATA_MAX	[31: 0]	RW	‘b0	AHB maxium Data for monitoring; Any access between Max and Min Data space may trigger interrupt;

5.9.4.2.8 **DATA_MASK**

Description：Data mask for monitoring.

0x001C			Data mask for monitoring. (Reset to 0x1000_0000)										DATA_MASK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DATA_MASK															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DATA_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
DATA_MASK	[31: 0]	RW	‘b0	Data_mask

5.9.4.2.9 **MATCH_ADDR**

Description：Matched address which triggered interrupt.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0020			Matched address which triggered interrupt. (Reset to 0x1000_0000)										MATCH_ADDR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	MATCH_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MATCH_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
MATCH_ADDR	[31: 0]	RO	‘b0	Captured Address, which triggered interrupt;

5.9.4.2.10 **MATCH_DATA**

Description： Matched data which triggered interrupt.

0x0024			Matched data which triggered interrupt. (Reset to 0x1000_0000)										MATCH_DATA			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	MATCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MATCH_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
MATCH_DATA	[31: 0]	RO	‘b0	Captured Data, which triggered interrupt;

5.9.4.2.11 **BUSMON_CNT**

Description：Performance counter.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0028			Performance counter. (Reset to 0x1000_0000)										BUSMON_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	BUSMON_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BUSMON_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
BUSMON_CNT	[31: 0]	RO	‘b0	Transaction counter;

5.10 General Purpose Timers

In SC6531, two groups of General Purpose Timer are designed, they are entirely same except the base address. One is named timer and another is named timer_bk.

Table 5-20 base address

	Base address
Timer	0x8100_0000
Timer_bk	0x8100_1000

5.10.1 Overview

Each group of timer includes three general-purpose timers, two RTC-clock trigged asynchronous timers, and one PCLK trigged synchronous timer.

5.10.2 Features

RTC clock trigged timers:

- Two independent RTC clock trigged timers
- 32-bit decreasing counter
- Support one-time mode and period mode

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

- Support configurable counting value
- Can be used as wakeup source during deep sleep
- Support single read : no need to double read when reading counter value
- Support multiple load : no need to check busy bit before load tmr
- Support read counter value immediately after loading tmr: once tmr is loaded, the counter value is updated immediately

PCLK clock trigged timer:

- One PCLK clock trigged timer
- 32-bit decreasing counter
- Support one-time mode and period mode
- Support configurable counting value
- Cannot be used as wakeup source during deep sleep

5.10.3 Signal description

Null

5.10.4 Funtion description

The MCU sub-system provides three general-purpose timers. Timer 0 and Timer 1 are trigged by RTC clock, which is 32.768KHz, and Timer 2 is trigged by PCLK, which is 26MHz. These three timers can be controlled independently

5.10.4.1 RTC Clock Trigged Timers

Timer 0 and Timer 1 are trigged by RTC clock, which is 32.768KHz. So the counting step is about 30.5us.

Each timer has a 32-bit decreasing counter. This kind of timer provides two operating modes: one-time mode and period mode.

If the timer is configured in one-time mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued. This interrupt is hold until software clears it by writing corresponding clear bit. The counter also stays at 0 until software load it again.

If the timer is configured in period mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued. Then counter goes back to setting value again, and continues to decrease from setting value. The interrupt will hold until software clears it by writing corresponding clear bit.

Because trigging clock is RTC clock, these two timers can be used to wake up system during deep sleep.

Since the frequency of clk_rtc is much slower than that of PCLK, there are three issues in the r1p0 version of timer, the solution also list here:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

- **Double read to read counter value**: in r1p0, counter value belongs to clk_rtc domain, but it connect to PCLK directly, so when read the counter value, metastable state may occur, and the read result is wrong. In r1p0, double read is utilized to solve the problem. It read the counter value for two times(double read), if the two result is same, no metastable state is occurred, if they are different, metastable may be occurred so software should discard the read result and double read again until the results is same. So we can see that double read solve the problem of metastable at the cost of increasing software complexity.

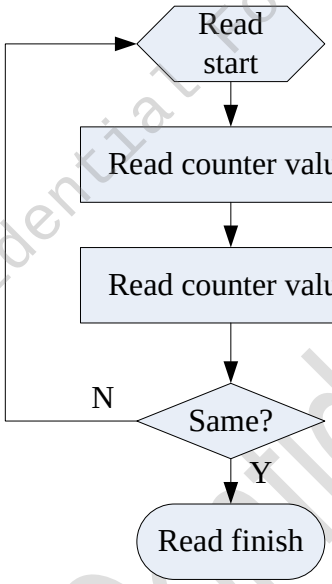


Figure 5-72 Double read flow

Solution to double read: In r2p0, a 32bit counter named tmr_cnt_shdw is used to solve this problem. It is in PCLK domain and once the tmr_cnt_value (clk_rtc) changes; it will also follow the change. Just as its name, it is the shadow of tmr_cnt_value which reflect the tmr_cnt_value accurately. Since it is in PCLK, metastable state can be avoided. In the case of deep sleep. PCLK is closed, tmr_cnt_shdw also stop following. Once PCLK is open, it quickly updates its value in 3 PCLK cycle. Figure 5-73 is the diagram of this solution, Figure 5-74 is the waveform of the updating process. Figure 5-75 illustrates the updating process when PCLK is closed.

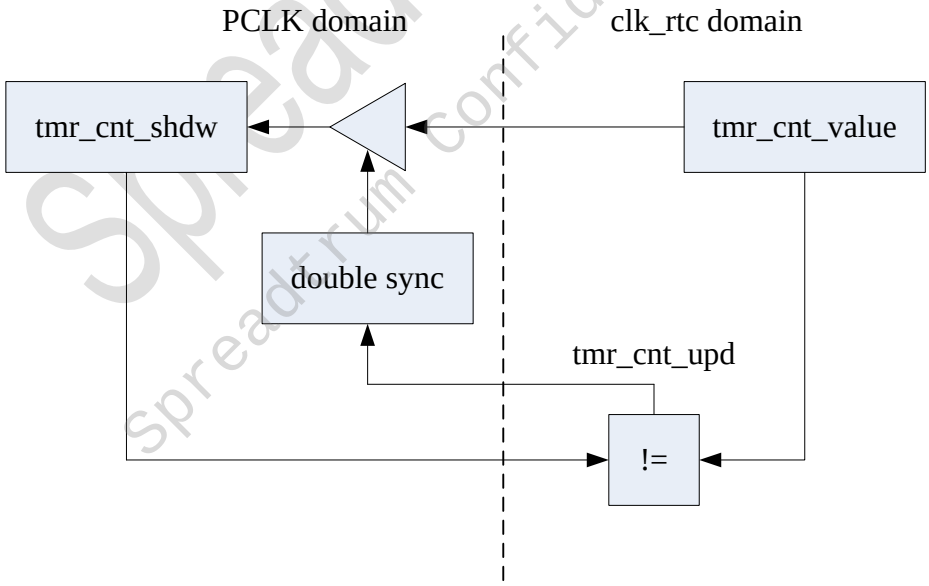
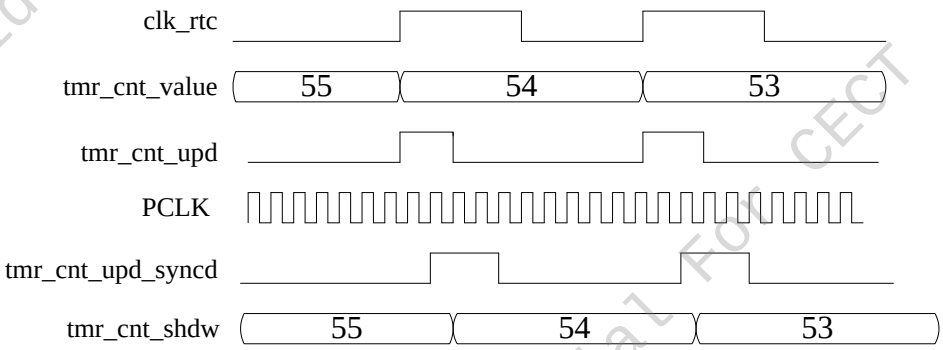


Figure 5-73 Principle of tmr_cnt_shdw

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.



Requirement:
tmr_cnt_value should be stable before the first load(**Synthesis at 26M**)

Figure 5-74 waveform of tmr_cnt_shdw (PCLK open)

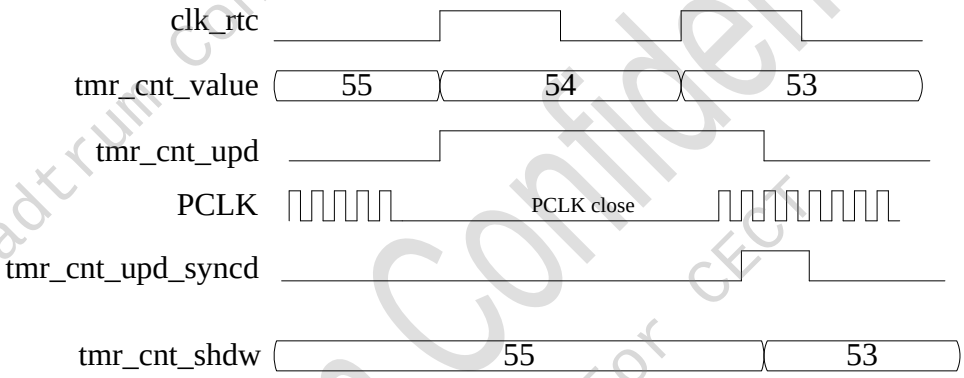
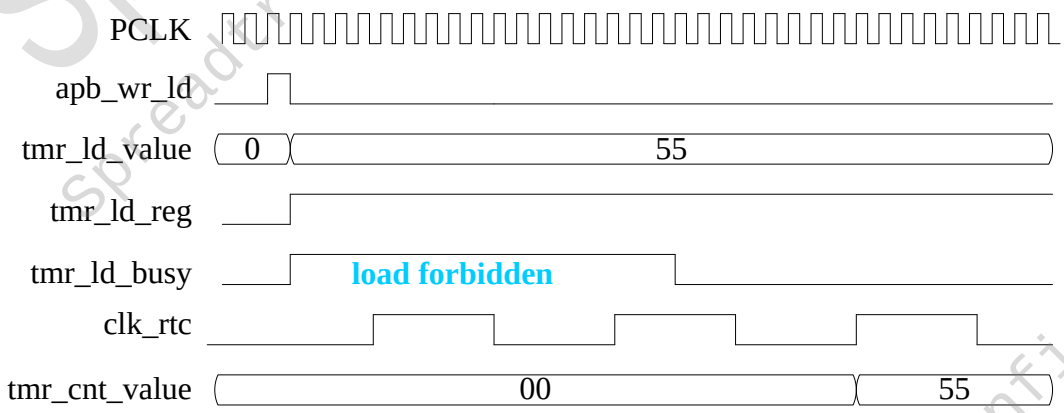


Figure 5-75 waveform of tmr_cnt_shdw (PCLK close)

- **Check busy bit before any load**: in r1p0, one bit signal tmr_ld_reg is used to record the load operation. When there is a load, tmr_ld_reg will toggle (0->1 or 1->0) which indicate a new load is taken place. However, tmr_ld_reg should hold this value until the load value is successfully loaded into counter which belongs to clk_rtc. If not, tmr_ld_reg will toggle back to original status which forms a narrow pulse that cannot be sampled by clk_rtc. That is to say, clk_rtc will not know a new load is happen. To avoid this problem, a busy bit named tmr_ld_busy is provided to indicate that timer is now busy with loading; further loading should not happen in this period. So this method confines the software by not allowing loading when tmr_ld_busy is 1. Figure 5-76 demonstrates that when tmr_ld_busy is 1, no load is permitted.



This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Figure 5-76 Check busy bit

- **Solution to check busy bit**: In r1p0, 1-bit signal tmr_ld_reg is used to record the load status, if multiple load occurs in a short time, it may miss the status. Therefore, a 8-bit signal tmr_ld_idx in PCLK domain is used here to solve the problem. Whenever software write the tmr_ld_value, tmr_ld_idx increase 1 to indicate that a new load is taken place. In clk_rtc domain, there is also 8-bit signal named tmr_ld_idx_shdw_rtc, which is the shadow of tmr_ld_idx in clk_rtc domain. When a new load happen, tmr_ld_idx and tmr_ld_idx_shdw are different, then tmr_ld_idx_shdw and tmr_cnt_value will update at the same time. Figure 5-77 is the circuit diagram, Figure 5-78 is the waveform of single load, from which we can see that maximum delay between tmr_ld_value and tmr_cnt_value is 5 clk_rtc delays. Figure 5-77 is the waveform of multiple loads, notice that we no longer check tmr_ld_busy, instead, we have multiple loads in a short time and the last load value (77) is loaded.

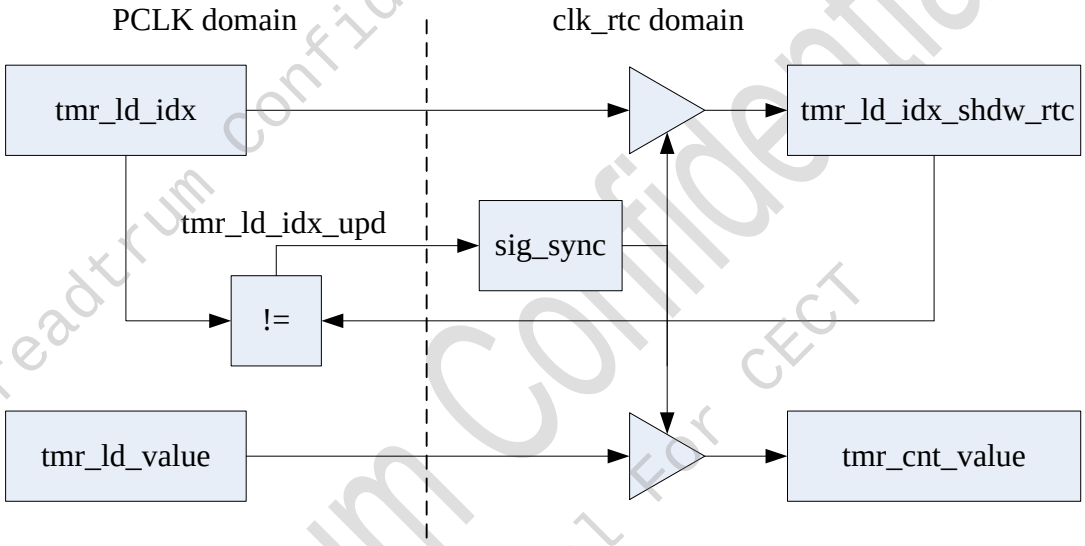
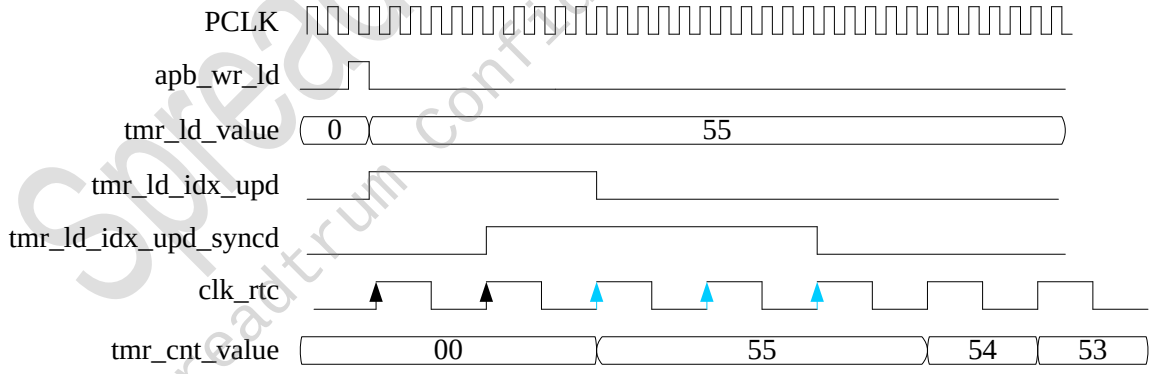


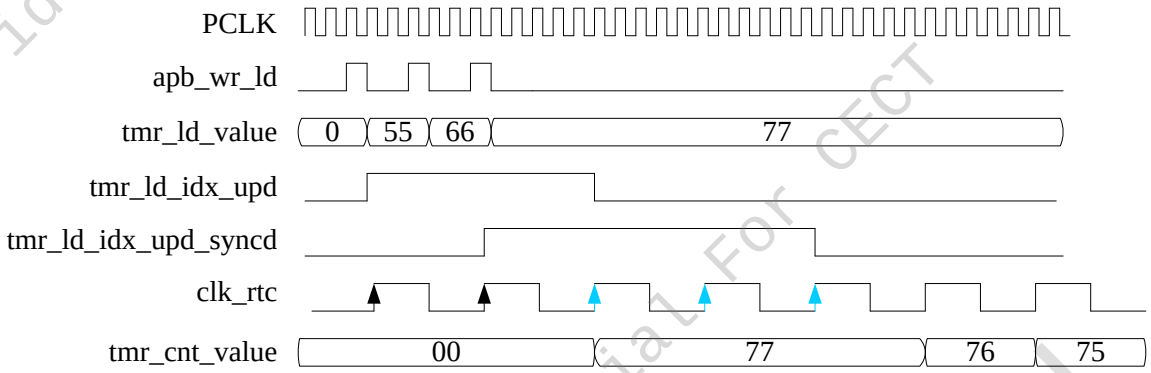
Figure 5-77 Solution of multiple load



Maximum delay is 5 clk_rtc

Figure 5-78 Single load

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.



Last load value(77) is loaded into tmr_cnt_value

Figure 5-79 multiple load

- **Waiting before read counter value**: In software, write and then read is commonly used to check whether a register is written correctly. However, when this method is used in timer, more attention should be paid. Because the load need 3 clk_rtc to finish, read value before that is illegal. Furthermore, there is no signal to indicate load is finish. Software has to count 3 clk_rtc by itself or wait 1 clk_rtc after tmr_ld_busy change to 0.

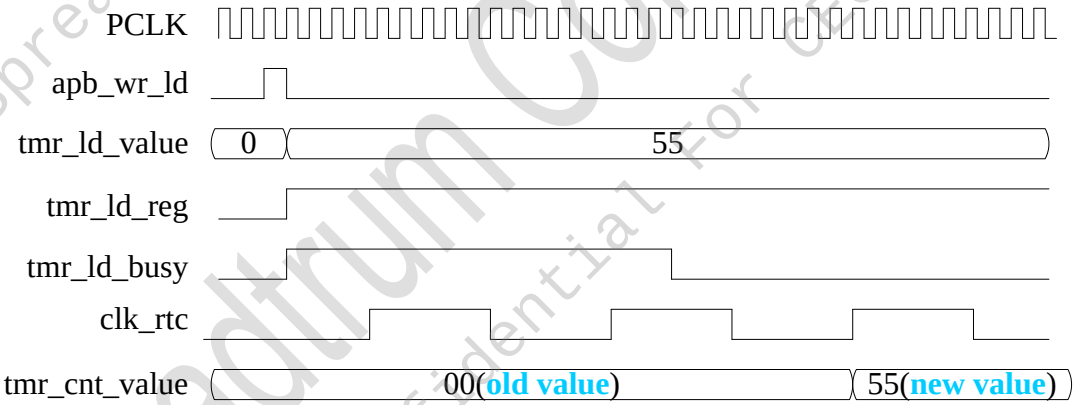


Figure 5-80 Wait 3 cycle to get new value

- **Solution to Waiting**: The solution is based on the knowledge that before load is done, we can use tmr_ld_value for read, and after load is done we can use tmr_cnt_shdw. To determine when the load is done, we sync tmr_ld_idx_shdw_rtc back to PCLK domain, and the synced signal is tmr_ld_idx_shdw_pclk. If tmr_ld_idx_shdw_pclk is equal to tmr_ld_idx, current load is done (tmr_loading = 0). This method works in the case of PCLK closed or auto-gated. After PCLK is open again, tmr_ld_idx_shdw_pclk can quickly sample the tmr_ld_idx_shdw_rtc and tmr_loading is updated. This only needs three PCLK. Usually software read happens after that period of time, so the read result is accurate. In following figure, the signal synchronization circuit using shadow mechanism circuit is not showed for simplicity.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

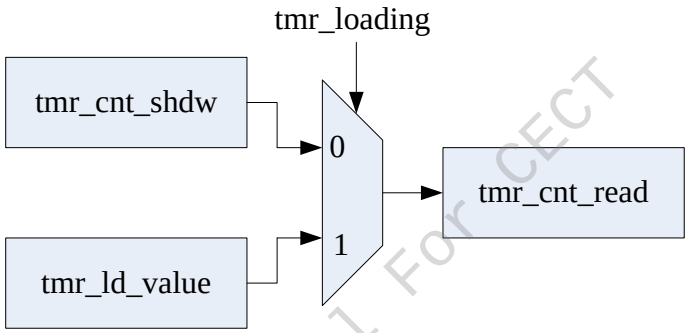


Figure 5-81 Solution to wait certain time

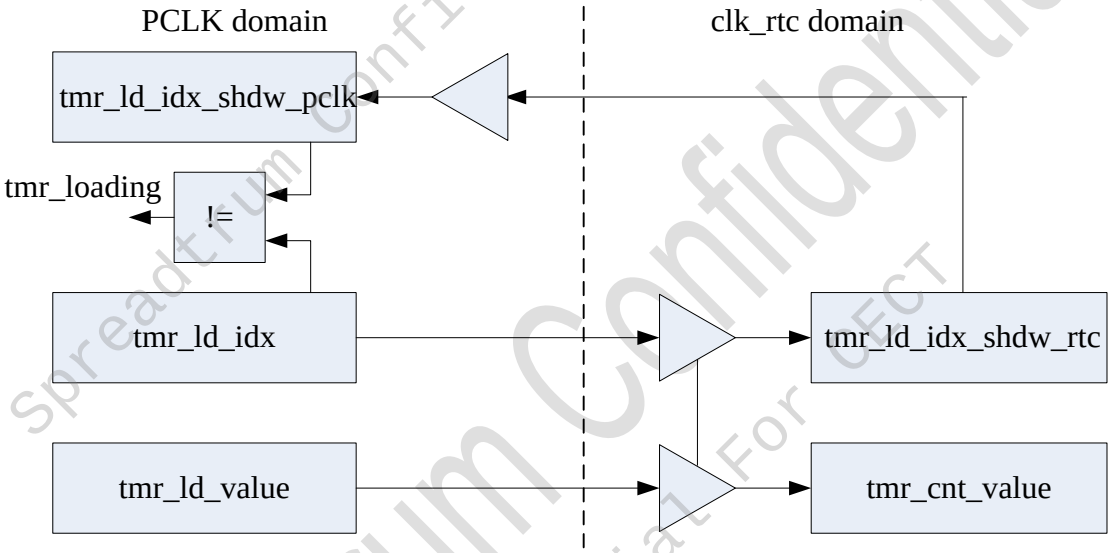


Figure 5-82 Waveform of tmr_loading

5.10.4.2 PCLK Trigged Timers

Timer 2 is trigged by PCLK, which is 26MHz. So the counting step is about 38.5ns.

This timer has a 32-bit decreasing counter. This timer provides two operating modes: one-time mode and period mode.

If the timer is configured in one-time mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued. This interrupt is hold until software clears it by writing corresponding clear bit. The counter stays at 0 until software load it again.

If the timer is configured in period mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued, and counter goes back to setting value again, and

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

continues to decrease from setting value. The interrupt will hold until software clears it by writing corresponding clear bit.

Because trigging clock is PCLK, this timer cannot be used to wake up system during deep sleep.

5.10.5 Control registers

5.10.5.1 Memory map

Table 5-14 Timer0:

Offset Address	Name	Description
0x1000	TIMER0_LOAD	Timer0 load value
0x1004	TIMER0_VALUE	Timer0 counter value
0x1008	TIMER0_CTL	Timer0 control registers
0x100C	TIMER0_INT	Timer0 interrupt
0x1010	TIMER0_CNT_RD	Timer0 counter value for read

Table 5-15 Timer1:

Offset Address	Name	Description
0x1020	TIMER1_LOAD	Timer1 load value
0x1024	TIMER1_VALUE	Timer1 counter value
0x1028	TIMER1_CTL	Timer1 control registers
0x102C	TIMER1_INT	Timer1 interrupt
0x1030	TIMER1_CNT_RD	Timer1 counter value for read

Table 5-16 Timer2:

Offset Address	Name	Description
0x1040	TIMER2_LOAD	Timer2 load value
0x1044	TIMER2_VALUE	Timer2 counter value
0x1048	TIMER2_CTL	Timer2 control registers
0x104C	TIMER2_INT	Timer2 interrupt

5.10.5.2 Register description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.10.5.2.1 **TIMER0_LOAD**

Description: Timer0 load value

0x1000	Timer0 load value (Reset 0x1000_0000)												**TIMER0_LOAD**			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer0_load															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer0_load															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer0_load	[31:0]	RW	32'h0	Timer0 load value Write to this register will reload the timer with the new value. In one-time mode, this value is the first counting start number. In periodic mode, this value is each counting start number.

5.10.5.2.2 **TIMER0_VALUE**

Description: Timer0 counter value

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1004			Timer0 counter value (Reset 0x1000_0000)													**TIMER0_VALUE**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer0_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer0_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer0_value	[31:0]	RO	32'h0	Timer0 counter value This read-only register indicates current counter value. It's not recommended to read this register in normal usage. Because the counter is in different clock domain with APB, software needs use double-reading method to read this value, like system timer.

5.10.5.2.3 **TIMER0_CTL**

Description: Timer0 control registers

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1008	Timer0 control register (Reset 0x1000_0000)															TIMER0_CTL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							Timer0_ne	timer0_run	timer0_mode	Reserved					
Type	RO							RW	RW	RW	RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:9]	RO	23'h0	Reserved
timer0_new	[8]	RW	1'h0	Timer0 version 0: timer use old behavior, this is for backward compatibility. 1: timer uses new behavior, such as multiple loads without checking busy bit, only need to read once to get timer counter value.
timer0_run	[7]	RW	1'h0	Timer0 open bit 0: timer stops 1: timer runs
timer0_mode	[6]	RW	1'h0	Timer0 mode select 0: one-time mode 1: period mode
	[5:0]	RO	6'h0	Reserved

5.10.5.2.4 **TIMER0_INT**

Description: Timer0 interrupt

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x100C			Timer0 interrupt (Reset 0x1000_0000)													**TIMER0_INT**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											timer0_ld_busy	timer0_int_clr	timer0_int_mask_sts	timer0_int_raw_sts	timer0_int_en
Type	RO											RO	WO	RO	RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:5]	RO	27'h0	Reserved
timer0_ld_busy	[4]	RO	1'h0	Timer0 load busy status 0: Timer is ready for new loading 1: Last loading is not completed Software must not load new value when this bit is busy, that is, this bit should be checked before any new loading. This bit is set after a new loading, and lasts two or three RTC clock cycles, about 60us - 92us.
timer0_int_clr	[3]	WO	1'h0	Timer0 Interrupt clear Write 1 to this bit to clear interrupt
timer0_int_mask_sts	[2]	RO	1'h0	Timer0 interrupt masked status
timer0_int_raw_sts	[1]	RO	1'h0	Timer0 interrupt raw status
timer0_int_en	[0]	RW	1'h0	Timer0 interrupt enable

5.10.5.2.5 **TIMER0_CNT_RD**

Description: Timer0 counter value for read

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1010			Timer0 counter value for read(Reset 0x1000_0000)											TIMER0_CNT_RD		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer0_cnt_rd															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer0_ cnt_rd															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer0_cnt_rd	[31:0]	RO	32'h0	Timer0 counter value for read. Only valid when tmr_new = 1. If tmr_new = 0, don't read this register. This read-only register indicates current counter value. The advantage of this register is software can read the counter value immediately after load, without waiting for the load done. Also, software just needs to read once instead of double read.

5.10.5.2.6 **TIMER1_LOAD**

Description: Timer1 load value

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1020	Timer1 load value (Reset 0x1000_0000)														TIMER1_LOAD	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer1_load															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer1_load															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer1_load	[31:0]	RW	32'h0	Timer1 load value Write to this register will reload the timer with the new value. In one-time mode, this value is the first counting start number. In period mode, this value is each counting start number.

5.10.5.2.7 **TIMER1_VALUE**

Description: Timer1 counter value

0x1024	Timer1 counter value (Reset 0x1000_0000)														TIMER1_VALUE	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer1_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer1_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Reset Value	Description
timer1_value	[31:0]	RO	32'h0	Timer1 counter value This read-only register indicates current counter value. It's not recommended to read this register in normal usage. Because the counter is in different clock domain with APB, software needs use double-reading method to read this value, like system timer.

5.10.5.2.8 **TIMER1_CTL**

Description: Timer1 control registers

0x1028	Timer1 control register (Reset 0x1000_0000)												TIMER1_CTL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							Timer1_new	Timer1_run	Timer1_mode	Reserved					
Type	RO							RW	RW	RW	RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:9]	RO	23'h0	Reserved
Timer1_new	[8]	RW	1'h0	Timer1 version 0: timer use old behavior, this is for backward compatibility. 1: timer uses new behavior, such as multiple loads without checking busy bit, only need to read once to get timer counter value.
timer1_run	[7]	RW	1'h0	Timer1 open bit

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Default Value	Description
				0: timer stops 1: timer runs
timer1_mode	[6]	RW	1'h0	Timer1 mode select 0: one-time mode 1: period mode
	[5:0]	RO	6'h0	Reserved

5.10.5.2.9 **TIMER1_INT**

Description: Timer1 interrupt

0x102C			Timer1 interrupt (Reset 0x1000_0000)													**TIMER1_INT**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											timer1_ld_busy	timer1_int_clr	timer1_int_mask_sts	timer1_int_raw_sts	timer1_int_en
Type	RO											RO	WO	RO	RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:5]	RO	27'h0	Reserved
timer1_ld_busy	[4]	RO	1'h0	Timer1 load busy status 0: Timer is ready for new loading 1: Last loading is not completed Software must not load new value when this bit is busy, that is, this bit should be checked before any new loading. This bit is set after a new loading, and lasts two or three RTC clock cycles, about 60us - 92us.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Default Value	Description
timer1_int_clr	[3]	WO	1'h0	Timer1 Interrupt clear Write 1 to this bit to clear interrupt
timer1_int_mask_sts	[2]	RO	1'h0	Timer1 interrupt masked status
timer1_int_raw_sts	[1]	RO	1'h0	Timer1 interrupt raw status
timer1_int_en	[0]	RW	1'h0	Timer1 interrupt enable

5.10.5.2.10 **TIMER1_CNT_RD**

Description: Timer1 counter value for read

0x1030			Timer1 counter value for read(Reset 0x1000_0000)										**TIMER1_CNT_RD**			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer1_cnt_rd															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer1_ cnt_rd															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer1_cnt_rd	[31:0]	RO	32'h0	Same as timer0_cnt_rd

5.10.5.2.11 **TIMER2_LOAD**

Description: Timer2 load value

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1040	Timer2 load value (Reset 0x1000_0000)															**TIMER2_LOAD**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer2_load															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer2_load															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer2_load	[31:0]	WO	32'h0	Timer2 load value Write to this register will reload the timer with the new value. In one-time mode, this value is the first counting start number. In period mode, this value is each counting start number.

5.10.5.2.12 **TIMER2_VALUE**

Description: Timer2 counter value

0x1044	Timer2 counter value (Reset 0x1000_0000)															**TIMER2_VALUE**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer2_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer2_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Reset Value	Description
timer2_value	[31:0]	RO	32'h0	Timer2 counter value This read-only register indicates current counter value.

5.10.5.2.13 **TIMER2_CTL**

Description: Timer2 control registers

0x1048	Timer2 control register (Reset 0x1000_0000)												**TIMER2_CTL**			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								timer2_run	Timer2_mode	Reserved					
Type	RO								RW	RW	RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:8]	RO	24'h0	Reserved
timer2_run	[7]	RW	1'h0	Timer2 open bit 0: timer stops 1: timer runs
Timer2_mode	[6]	RW	1'h0	Timer2 mode select 0: one-time mode 1: period mode
	[5:0]	RO	6'h0	Reserved

5.10.5.2.14 **TIMER2_INT**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Description: Timer2 interrupt

0x104C			Timer2 interrupt (Reset 0x1000_0000)													TIMER2_INT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												timer2_int_clr	timer2_int_mask_sts	timer2_int_raw_sts	timer2_int_en
Type	RO												WO	RO	RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:4]	RO	28'h0	Reserved
timer2_int_clr	[3]	WO	1'h0	Timer2 Interrupt clear Write 1 to this bit to clear interrupt
timer2_int_mask_sts	[2]	RO	1'h0	Timer2 interrupt masked status
timer2_int_raw_sts	[1]	RO	1'h0	Timer2 interrupt raw status
timer2_int_en	[0]	RW	1'h0	Timer2 interrupt enable

5.10.6 Application notes

5.10.6.1 RTC Clock Trigged Timers

When software uses RTC clock trigged timer, it should set tmr_eb bit and tmr_rtc_eb bit in global control register.

Before opening timer0_run or timer1_run, software should configure all control registers – timer0_load or timer1_load, timer0_mode or timer1_mode, timer0_int_en or timer1_int_en, timer0_new or timer1_new.

Then timer0_run or timer1_run is set to 1 to open corresponding timer.

After receiving interrupt issued by a timer, software can check interrupt status by reading timer0_int_mask_sts or timer1_int_mask_sts, and can clear interrupt by writing 1 to timer0_int_clr or timer1_int_clr.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

When software completes using RTC clock trigged timer, it should disable timer0_run or timer1_run firstly, then it disable tmr_rtc_eb and tmr_eb in global control registers.

It's IMPORTANT that there are 3~5 RTC clock cycles delay from setting timer0_load or timer1_load to counter setting success(refer to Figure 5-78), that is, if N is configured in timer0_load or timer1_load, real counting number is N+3 or N+4 or N+5.

When timer0_new or timer1_new = 0, software must check timer0_ld_busy or timer1_ld_busy before loading. When timer0_new or timer1_new =1, software need not check it. Loading is permitted at any time.

If the timer is configured in one-time mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued. The counter stays at 0 until software load it again.

If the timer is configured in period mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued, and counter is reloaded by setting value, and then counter continues to decrease from setting value.

5.10.6.2 PCLK Trigged Timers

When software uses PCLK trigged timer, it should set tmr_eb bit in global control register.

Before opening timer2_run, software should configure all control registers – timer2_load, timer2_mode, timer2_int_en.

Then timer2_run is set to 1 to open the timer.

After receiving interrupt issued by a timer, software can check interrupt status by reading timer2_int_mask_sts, and can clear interrupt by writing 1 to timer2_int_clr.

When software completes using PCLK trigged timer, it should disable timer2_run firstly, and then it disable tmr_eb in global control registers.

If the timer is configured in one-time mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued. The counter stays at 0 until software load it again.

If the timer is configured in period mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued, and counter is reloaded by setting value, and then counter continues to decrease from setting value.

5.10.7 Implementations(for internal only)

Logic in clk_rtc domain should be synthesized at least 26M.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

when tmr_cnt_value change, it will be sampled to tmr_cnt_shdw after 3 PCLK. So tmr_cnt_value must be stable before that. For safety, we require that all logic in clk_rtc domain should be synthesized at 26M.

5.10.8 Future improvements

- There are 3-5 RTC clock cycles delay from setting timer0_load or timer1_load to counter setting success because of different clock domains and usage of feedback.
- In current design, when PCLK is closed, timer0_cnt_rd and timer1_cnt_rd is not accurate. That is because the counter for waiting 3 clk_rtc is stopped when PCLK is closed. So the design cannot count how much time is used.

5.11 System timer

ARM base address: 0x8100_3000

5.11.1 Overview

System timer is a 32-bit free-running increasing timer with 1ms step.

5.11.2 Features

- RTC-clock trigged
- 32-bit free-running increasing timer
- 1ms step
- Support one configurable alarm, and support alarm interrupt generating
- Alarm interrupt can be used as wakeup source during deep sleep
- Support single read : no need to double read when reading counter value

5.11.3 Signal description

Null

5.11.4 Funtion description

After hardware reset, system timer is 0. And after being enabled, system timer runs from 0 to the maximum, 2^32-1. If system timer gets to the maximum, it returns to 0 again and then continues increasing. If no new hardware reset occurs and system timer is kept enabled, nothing can stop system timer.

The counting step is 1ms, that is, the timer increases by 1 per 1ms.

The timer value can be read by software. If software read SYST_VALUE, double-reading method must be used because of different clock domains. If software read SYST_CNT_SHDW, only one read is enough.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Based on system timer free running, it provides an alarm function. When system timer value is equal to alarm value, an interrupt is issued, and this interrupt can be used for system wakeup source during deep sleep.

5.11.5 Control registers

5.11.5.1 Memory map

Offset Address	Name	Description
0x1000	SYST_ALARM	System timer alarm
0x1004	SYST_VALUE	System timer value
0x1008	SYST_INT	System timer interrupt
0x100C	SYST_VALUE_SHDW	Shadow of SYST_VALUE

5.11.5.2 Register description

5.11.5.2.1 SYST_ALARM

Description: System timer alarm

0x1000	System timer alarm (Reset 0x1000_FFFF)												SYST_ALARM			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	syst_alarm															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	syst_alarm															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
syst_alarm	[31:0]	RW	32'h0000FFFF	System timer alarm value: If system timer is equal to

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Reset Value	Description
				system alarm, one interrupt is issued.

5.11.5.2.2 **SYST_VALUE**

Description: System timer value

0x1004			System timer value (Reset 0x1000_0000)										SYST_VALUE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	syst_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	syst_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
syst_value	[31:0]	RO	32'h0	System timer value Double-reading method MUST be used to read this register.

5.11.5.2.3 **SYST_INT**

Description: System timer interrupt

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x100C			System timer interrupt (Reset 0x1000_0000)													SYST_INT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											syst_int_pls_sts	syst_int_clr	syst_int_mask_sts	syst_int_raw_sts	syst_int_en
Type	RO											RO	WO	RO	RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:5]	RO	27'h0	Reserved
syst_int_pls_sts	[4]	RO	1'h0	System timer interrupt pulse status This bit is used only for debugging.
syst_int_clr	[3]	WO	1'h0	System timer Interrupt clear Write 1 to this bit to clear interrupt
syst_int_mask_sts	[2]	RO	1'h0	System timer interrupt masked status
syst_int_raw_sts	[1]	RO	1'h0	System timer interrupt raw status
syst_int_en	[0]	RW	1'h0	System timer interrupt enable

5.11.5.2.4 **SYST_VALUE_SHDW**

Description: Shadow of SYST_VALUE

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x100C			Shadow of SYST_VALUE (Reset 0x1000_0000)										SYST_VALUE_SHDW			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	syst_value_shdw															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	syst_value_shdw															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
syst_value_shdw	[31:0]	RO	32'h0	Shadow of SYST_VALUE One read will get accurate value.

5.11.6 Application notes

When software begins to use system timer, it should set sys_eb bit and sys_rtc_eb bit in global control register.

When software completes using system timer, it should disable sys_eb bit and sys_rtc_eb bit in global control registers.

When software uses alarm function, it should configure sys_alarm and sys_int_en.

After receiving interrupt issued by a system timer, software can check interrupt status by reading sys_int_mask_sts, and can clear interrupt by writing 1 to sys_int_clr.

IMPORTANT:

If software read SYST_VALUE, double-reading method MUST be used to read this register. If software read SYST_VALUE_SHDW, only one read can get accurate counter value.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.11.7 Implementations

Logic in clk_rtc domain should be synthesized at 26M. Just as implementation requirement of timer.

5.11.8 Future improvements

- IIn current design, alarm registers are implemented in PCLK domain and used in RTC-clock domain. This design leads to two potential issues, one is timing issue on interrupt register. The other issue is more serious, false interrupt may be trigged. We can use shadow register in RTC clock domain to solve these potential issues, and the related impact also is area because of one extra groups of 32-bit shadow DFFs.

5.12 RTC timer

5.12.1 Overview

SC6531 provides an always-powered-on region to count second, minute, hour and day, and to perform alarm functions.

5.12.2 Features

- Second counter: 0 – 59
- Minute counter: 0 – 59
- Hour counter: 0 – 23
- Day counter: 0 – 65535
- Second, minute, hour and day numbers can be changed by software
- Provide second interrupt, minute interrupt, hour interrupt and day interrupt
- Provide configurable alarm function
- All interrupts can be used to wakeup system from deep sleep
- Alarm interrupt can be used to power up system from power-down status
- RTCVDD is the power supply for second counter, minute counter, hour counter, day counter, and alarm function. And this power is always on.

5.12.3 Funtion description

SC6531 provides a very small always-powered-on region supplied by RTCVDD. Second counter, minute counter, hour counter, day counter, and alarm function are put in this region, so these functions always work even if the base band chip enters power-down mode.

Second counter, minute counter, hour counter and day counter are used to count second, minute, hour and day values, and to issue second, minute, hour and day interrupts. The value of these four counters can be changed by software, but the changing time is very long, about 125 ms. In order to improve software efficiency, SC6531 provides four interrupts to inform software changing completion. The changes to four counters are independent, and it does not need waiting for first changing to complete before changing next one.

Alarm function is used to generate alarm interrupt to inform software, to wake up system, or to power up system. Alarm second, minute, hour and day values are stored in the RTCVDD power domain, and these four registers can be changed by

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

software. It also takes long time to change these registers, and another set of four interrupts are provided for changing completion. Same as the above, the changes to the four registers are independent, and it does not need waiting for first changing to complete before changing next one.

Because RTC timers are in RTC clock domain, all interrupts can be used to wakeup system from deep sleep. Another important function is alarm interrupt can power up base band from power-down mode.

5.12.4 Control registers

5.12.4.1 Memory map

Table 5-17 RTC Timer Control Register Address Map

Address Offset	Register Name	Default Value
0x1000	RTC_SEC_CNT	-
0x1004	RTC_MIN_CNT	-
0x1008	RTC_HOUR_CNT	-
0x100C	RTC_DAY_CNT	-
0x1010	RTC_SEC_CNT_UPD	32’h00000000
0x1014	RTC_MIN_ CNT_UPD	32’h00000000
0x1018	RTC_HOUR_ CNT_UPD	32’h00000000
0x101C	RTC_DAY_ CNT_UPD	32’h00000000
0x1020	RTC_SEC_ALM_UPD	32’h00000000
0x1024	RTC_MIN_ALM_UPD	32’h00000000
0x1028	RTC_HOUR_ALM_UPD	32’h00000000
0x102C	RTC_DAY_ALM_UPD	32’h00000000
0x1030	RTC_INT_EN	32’h00000000
0x1034	RTC_INT_RAW_STS	32’h00000000
0x1038	RTC_INT_CLR	32’h00000000
0x103C	RTC_INT_MASK_STS	32’h00000000

5.12.4.2 Register description

5.12.4.2.1 RTC_SEC_CNT

Physical Address: 0x89000000

Description: Current second counter value

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1000	RTC Second Counter														RTC_SEC_CNT	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										RTC_SEC_CNT					
Type	RO										RO					
Reset	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-

Field Name	Bit	R/W	Default Value	Description
RTC_SEC_CNT	[5:0]	RO	-	Current second counter value
	[31:6]	**RO**		Reserved

5.12.4.2.2 **RTC_MIN_CNT**

Physical Address: 0x89000004

Description: Current minute counter value

0x1004	RTC Minute Counter														RTC_MIN_CNT	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										RTC_MIN_CNT					
Type	RO										RO					
Reset	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-

Field Name	Bit	R/W	Default Value	Description
RTC_MIN_CNT	[5:0]	RO	-	Current minute counter value
	[31:6]	**RO**		Reserved

5.12.4.2.3 **RTC_HOUR_CNT**

Physical Address: 0x89000008

Description: Current hour counter value

0x1008	RTC Hour Counter														RTC_HRS_CNT	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											RTC_HRS_CNT				
Type	RO											RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	-	-	-	-	

Field Name	Bit	R/W	Default Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Default Value	Description
RTC_HRS_CNT	[4:0]	RO	-	Current hour counter value
	[31:5]	**RO**		Reserved

5.12.4.2.4 **RTC_DAY_CNT**

Physical Address: 0x8900000C

Description: Current day counter value

0x100C	**RTC Day Counter**															**RTC_DAY_CNT**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_CNT															
Type	RO															
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Field Name	Bit	R/W	Default Value	Description
RTC_DAY_CNT	[15:0]	RO	-	Current day counter value
	[31:16]	**RO**		Reserved

5.12.4.2.5 **RTC_SEC_CNT_UPD**

Physical Address: 0x89000010

Description: Current second counter update

0x1010	**RTC Second Counter Update (reset 0x1000_0000)**															**RTC_SEC_CNT_UPD**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										RTC_SEC_CNT_UPD					
Type	RO										R/W					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
RTC_SEC_CNT_UPD	[5:0]	RW	6'h0	Current second counter update Write new counter value to this register to start an second counter updating operation in RTCVDD domain. Reading this register can get recent updating value
	[31:6]	**RO**		Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.12.4.2.6 RTC_MIN_CNT_UPD

Physical Address: 0x89000014

Description: Current minute counter update

0x1014	RTC Minute Counter Update (reset 0x1000_0000)														RTC_MIN_CNT_UPD	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										RTC_MIN_CNT_UPD					
Type	RO										R/W					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
RTC_MIN_CNT_UPD	[5:0]	RW	6'h0	Current minute counter update Write new counter value to this register to start an minute counter updating operation in RTCVDD domain. Reading this register can get recent updating value
	[31:6]	**RO**		Reserved

5.12.4.2.7 RTC_HOUR_CNT_UPD

Physical Address: 0x89000018

Description: Current hour counter update

0x1018	RTC Hour Counter Update (reset 0x1000_0000)														RTC_HRS_CNT_UPD	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											RTC_HRS_CNT_UPD				
Type	RO											R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
RTC_HRS_CNT_UPD	[4:0]	RW	5'h0	Current hour counter update Write new counter value to this register to start an hour counter updating operation in RTCVDD domain. Reading this register can get recent updating value
	[31:5]	**RO**		Reserved

5.12.4.2.8 RTC_DAY_CNT_UPD

Physical Address: 0x8900001C

Description: Current day counter update

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x101C			RTC Day Counter Update (reset 0x1000_0000)										RTC_DAY_CNT_UPD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_CNT_UPD															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
RTC_DAY_CNT_UPD	[15:0]	RW	16'h0	Current day counter update Write new counter value to this register to start an day counter updating operation in RTCVDD domain. Reading this register can get recent updating value
	[31:16]	**RO**		Reserved

5.12.4.2.9 **RTC_SEC_ALM_UPD**

Physical Address: 0x89000020

Description: Current second alarm update

0x1020			RTC Second Alarm Update (reset 0x1000_0000)										RTC_SEC_ALM_UPD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										RTC_SEC_ALM_UPD					
Type	RO										R/W					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
RTC_SEC_ALM_UPD	[5:0]	RW	6'h0	Current second alarm update Write new counter value to this register to start an second alarm updating operation in RTCVDD domain. Reading this register can get recent updating value
	[31:6]	**RO**		Reserved

5.12.4.2.10 **RTC_MIN_ALM_UPD**

Physical Address: 0x89000024

Description: Current minute alarm update

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1024			RTC Minute Alarm Update (reset 0x1000_0000)										RTC_MIN_ALM_UPD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										RTC_MIN_ALM_UPD					
Type	RO										R/W					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
RTC_MIN_ALM_UPD	[5:0]	RW	6'h0	Current minute alarm update Write new counter value to this register to start an minute alarm updating operation in RTCVDD domain. Reading this register can get recent updating value
	[31:6]	**RO**		Reserved

5.12.4.2.11 **RTC_HOUR_ALM_UPD**

Physical Address: 0x89000028

Description: Current hour alarm update

0x1028			RTC Hour Alarm Update (reset 0x1000_0000)										RTC_HRS_ALM_UPD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											RTC_HRS_ALM_UPD				
Type	RO											R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
RTC_HUS_ALM_UPD	[4:0]	RW	5'h0	Current hour alarm update Write new counter value to this register to start an hour alarm updating operation in RTCVDD domain. Reading this register can get recent updating value
	[31:5]	**RO**		Reserved

5.12.4.2.12 **RTC_DAY_ALM_UPD**

Physical Address: 0x8900002C

Description: Current day alarm update

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x102C			RTC Day Alarm Update (reset 0x1000_0000)										RTC_DAY_ALM_UPD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_ALM_UPD															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
RTC_DAY_ALM_UPD	[15:0]	RW	16'h0	Current day alarm update Write new counter value to this register to start an day alarm updating operation in RTCVDD domain. Reading this register can get recent updating value
	[31:16]	**RO**		Reserved

5.12.4.2.13 **RTC_INT_EN**

Physical Address: 0x89000030

Description: Interrupt enable and hour format control

Description：Interrupt enable and hour format control

0x1030			RTC Day Counter										RTC_DAY_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_ALM_UPD_INT_EN	RTC_HOUR_ALM_UPD_INT_EN	RTC_MIN_ALM_UPD_INT_EN	RTC_SEC_ALM_UPD_INT_EN	RTC_DAY_CNT_UPD_INT_EN	RTC_HOUR_CNT_UPD_INT_EN	RTC_MIN_CNT_UPD_INT_EN	RTC_SEC_CNT_UPD_INT_EN	Reserved		RTC_HOUR_FORMAT_SEL	RTC_ALM_INT_EN	RTC_DAY_INT_EN	RTC_HOUR_INT_EN	RTC_MIN_INT_EN	RTC_SEC_INT_EN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
RTC_DAY_ALM_UPD_INT_EN	[15]	RW	1'h0	Day alarm updating complete interrupt enable

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				0: disabled 1: enabled
RTC_HOUR_ALM_UPD_INT_EN	[14]	RW	1'h0	Hour alarm updating complete interrupt enable
RTC_MIN_ALM_UPD_INT_EN	[13]	RW	1'h0	Minute alarm updating complete interrupt enable
RTC_SEC_ALM_UPD_INT_EN	[12]	RW	1'h0	Second alarm updating complete interrupt enable
RTC_DAY_CNT_UPD_INT_EN	[11]	RW	1'h0	Day counter updating complete interrupt enable
RTC_HOUR_CNT_UPD_INT_EN	[10]	RW	1'h0	Hour counter updating complete interrupt enable
RTC_MIN_CNT_UPD_INT_EN	[9]	RW	1'h0	Minute counter updating complete interrupt enable
RTC_SEC_CNT_UPD_INT_EN	[8]	RW	1'h0	Second counter updating complete interrupt enable
	[7:6]	RO	2'h0	Reserved
	[5]	RW	1'h0	Hour format select 0: The read back hour count is formatted as 0 to 23. 1: The read back hour count is formatted as 0 to 11, and bit 4 represent AM or PM – AM is 0 and PM is 1.
RTC_ALM_INT_EN	[4]	RW	1'h0	alarm interrupt enable
RTC_DAY_INT_EN	[3]	RW	1'h0	day interrupt enable
RTC_HOUR_INT_EN	[2]	RW	1'h0	hour interrupt enable
RTC_MIN_INT_EN	[1]	RW	1'h0	minute interrupt enable
RTC_SEC_INT_EN	[0]	RW	1'h0	Second interrupt enable

5.12.4.2.14 **RTC_INT_RAW_STS**

Physical Address: 0x89000034

Description: Interrupt raw status

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1034			RTC Day Counter										RTC_DAY_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_ALM_UPD_INT_RAW_STS	RTC_HOUR_ALM_UPD_INT_RAW_STS	RTC_MIN_ALM_UPD_INT_RAW_STS	RTC_SEC_ALM_UPD_INT_RAW_STS	RTC_DAY_CNT_UPD_INT_RAW_STS	RTC_HOUR_CNT_UPD_INT_RAW_STS	RTC_MIN_CNT_UPD_INT_RAW_STS	RTC_SEC_CNT_UPD_INT_RAW_STS	Reserved		RTC_ALM_INT_RAW_STS_ORI	RTC_ALM_INT_RAW_STS	RTC_DAY_INT_RAW_STS	RTC_HOUR_INT_RAW_STS	RTC_MIN_INT_RAW_STS	RTC_SEC_INT_RAW_STS
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
RTC_DAY_ALM_UPD_INT_RAW_STS	[15]	RW	1'h0	Day alarm updating complete interrupt raw status
RTC_HOUR_ALM_UPD_INT_RAW_STS	[14]	RW	1'h0	Hour alarm updating complete interrupt raw status
RTC_MIN_ALM_UPD_INT_RAW_STS	[13]	RW	1'h0	Minute alarm updating complete interrupt raw status
RTC_SEC_ALM_UPD_INT_RAW_STS	[12]	RW	1'h0	Second alarm updating complete interrupt raw status
RTC_DAY_CNT_UPD_INT_RAW_STS	[11]	RW	1'h0	Day counter updating complete interrupt raw status
RTC_HOUR_CNT_UPD_INT_RAW_STS	[10]	RW	1'h0	Hour counter updating complete interrupt raw status
RTC_MIN_CNT_UPD_INT_RAW_STS	[9]	RW	1'h0	Minute counter updating complete interrupt raw status
RTC_SEC_CNT_UPD_INT_RAW_STS	[8]	RW	1'h0	Second counter updating complete interrupt raw status
	[7:6]	RO	3'h0	Reserved
RTC_ALM_INT_RAW_STS_ORI	[5]	RW	1'h0	alarm interrupt raw status, source to analog.
RTC_ALM_INT_RAW_STS	[4]	RW	1'h0	alarm interrupt raw status
RTC_DAY_INT_RAW_STS	[3]	RW	1'h0	day interrupt raw status
RTC_HOUR_INT_RAW_STS	[2]	RW	1'h0	hour interrupt raw status

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

RTC_MIN_INT_RAW_STS	[1]	RW	1'h0	minute interrupt raw status
RTC_SEC_INT_RAW_STS	[0]	RW	1'h0	Second interrupt raw status

5.12.4.2.15 **RTC_INT_CLR**

Physical Address: 0x89000038

Description: Interrupt clear

0x1038	RTC Day Counter												RTC_DAY_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_ALM_UPD_INT_CLR	RTC_HOUR_ALM_UPD_INT_CLR	RTC_MIN_ALM_UPD_INT_CLR	RTC_SEC_ALM_UPD_INT_CLR	RTC_DAY_CNT_UPD_INT_CLR	RTC_HOUR_CNT_UPD_INT_CLR	RTC_MIN_CNT_UPD_INT_CLR	RTC_SEC_CNT_UPD_INT_CLR	Reserved			RTC_ALM_INT_CLR	RTC_DAY_INT_CLR	RTC_HOUR_INT_CLR	RTC_MIN_INT_CLR	RTC_SEC_INT_CLR
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO			R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
RTC_DAY_ALM_UPD_INT_CLR	[15]	RW	1'h0	Day alarm updating complete interrupt clear Write 1 to this bit to clear corresponding interrupt
RTC_HOUR_ALM_UPD_INT_CLR	[14]	RW	1'h0	Hour alarm updating complete interrupt clear
RTC_MIN_ALM_UPD_INT_CLR	[13]	RW	1'h0	Minute alarm updating complete interrupt clear
RTC_SEC_ALM_UPD_INT_CLR	[12]	RW	1'h0	Second alarm updating complete interrupt clear
RTC_DAY_CNT_UPD_INT_CLR	[11]	RW	1'h0	Day counter updating complete interrupt clear
RTC_HOUR_CNT_UPD_INT_CLR	[10]	RW	1'h0	Hour counter updating complete interrupt clear
RTC_MIN_CNT_UPD_INT_CLR	[9]	RW	1'h0	Minute counter updating complete interrupt clear
RTC_SEC_CNT_UPD_INT_CLR	[8]	RW	1'h0	Second counter updating complete interrupt clear
	[7:5]	RO	3'h0	Reserved
RTC_ALM_INT_CLR	[4]	RW	1'h0	alarm interrupt clear
RTC_DAY_INT_CLR	[3]	RW	1'h0	day interrupt clear
RTC_HOUR_INT_CLR	[2]	RW	1'h0	hour interrupt clear

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

RTC_MIN_INT_CLR	[1]	RW	1'h0	minute interrupt clear
RTC_SEC_INT_CLR	[0]	RW	1'h0	Second interrupt clear

5.12.4.2.16 **RTC_INT_MASK_STS**

Physical Address: 0x8900003C

Description: Interrupt masked status

0x103C			RTC Day Counter										RTC_DAY_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_DAY_ALM_UPD_INT_MASK_STS	RTC_HOUR_ALM_UPD_INT_MASK_STS	RTC_MIN_ALM_UPD_INT_MASK_STS	RTC_SEC_ALM_UPD_INT_MASK_STS	RTC_DAY_CNT_UPD_INT_MASK_STS	RTC_HOUR_CNT_UPD_INT_MASK_STS	RTC_MIN_CNT_UPD_INT_MASK_STS	RTC_SEC_CNT_UPD_INT_MASK_STS	Reserved			RTC_ALM_INT_MASK_STS	RTC_DAY_INT_MASK_STS	RTC_HOUR_INT_MASK_STS	RTC_MIN_INT_MASK_STS	RTC_SEC_INT_MASK_STS
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO			R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
RTC_DAY_ALM_UPD_INT_MASK_STS	[15]	RW	1'h0	Day alarm updating complete interrupt masked status Write 1 to this bit to masked status corresponding interrupt
RTC_HOUR_ALM_UPD_INT_MASK_STS	[14]	RW	1'h0	Hour alarm updating complete interrupt masked status
RTC_MIN_ALM_UPD_INT_MASK_STS	[13]	RW	1'h0	Minute alarm updating complete interrupt masked status
RTC_SEC_ALM_UPD_INT_MASK_STS	[12]	RW	1'h0	Second alarm updating complete interrupt masked status
RTC_DAY_CNT_UPD_INT_MASK_STS	[11]	RW	1'h0	Day counter updating complete interrupt masked status
RTC_HOUR_CNT_UPD_INT_MASK_STS	[10]	RW	1'h0	Hour counter updating complete interrupt masked status
RTC_MIN_CNT_UPD_INT_MASK_STS	[9]	RW	1'h0	Minute counter updating complete interrupt masked status

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

RTC_SEC_CNT_UPD_INT_MASK_STS	[8]	RW	1'h0	Second counter updating complete interrupt masked status
	[7:5]	RO	3'h0	Reserved
RTC_ALM_INT_MASK_STS	[4]	RW	1'h0	alarm interrupt masked status
RTC_DAY_INT_MASK_STS	[3]	RW	1'h0	day interrupt masked status
RTC_HOUR_INT_MASK_STS	[2]	RW	1'h0	hour interrupt masked status
RTC_MIN_INT_MASK_STS	[1]	RW	1'h0	minute interrupt masked status
RTC_SEC_INT_MASK_STS	[0]	RW	1'h0	Second interrupt masked status

5.12.5 Application notes

Second counter, minute counter, hour counter and day counter always run in RTCVDD domain. However, if software wants to access or control these functions, it should set rtc_eb and rtc_rtc_eb first.

After setting rtc_eb and rtc_rtc_eb, software can get second, minute, hour and day counter values by reading rtc_sec_cnt, rtc_min_cnt, rtc_hour_cnt and rtc_day_cnt. Double-reading method is still recommended, like the system timer reading.

RTC timers provide second interrupt, minute interrupt, hour interrupt and day interrupt. Software can enable these interrupts by setting 1 to rtc_sec_int_en, rtc_min_int_en, rtc_sec_hour_en and rtc_day_int_en, check status by reading rtc_sec_int_mask_sts, rtc_min_int_mask_sts, rtc_hour_int_mask_sts and rtc_day_int_mask_sts, and clear these interrupts by writing 1 to rtc_sec_int_clr, rtc_min_int_clr, rtc_hour_int_clr and rtc_day_int_clr.

Software can update the four counter values by writing new value to rtc_sec_cnt_upd, rtc_min_cnt_upd, rtc_hour_cnt_upd or rtc_day_cnt_upd. However, the changing time is very long, about 125 ms. In order to improve software efficiency, RTC timer provides four interrupts to inform software changing completion. Software can enable these interrupts by setting rtc_sec_cnt_upd_int_en, rtc_min_cnt_upd_int_en, rtc_hour_cnt_upd_int_en and rtc_day_cnt_upd_int_en, check status by reading rtc_sec_cnt_upd_int_mask_sts, rtc_min_cnt_upd_int_mask_sts, rtc_hour_cnt_upd_int_mask_sts and rtc_day_cnt_upd_int_mask_sts, and clear these interrupts by writing 1 to rtc_sec_cnt_upd_int_clr, rtc_min_cnt_upd_int_clr, rtc_cnt_upd_hour_int_clr and rtc_day_cnt_upd_int_clr. The changes to four counters are independent, and it does not need waiting for first changing to complete before changing next one.

RTC timer provides an alarm function. If an alarm occurs, alarm interrupt is issued. Software can enable this interrupt by setting rtc_alm_int_en, check status by reading rtc_alm_int_mask_sts, and clear these interrupts by writing 1 to rtc_alm_int_clr.

Alarm value can be configured by writing expected value to rtc_sec_alm_upd, rtc_min_alm_upd, rtc_hour_alm_upd and rtc_day_alm_upd. However, the changing time is very long, about 125 ms. In order to improve software efficiency, RTC timer provides four interrupts to inform software changing completion. Software can enable these interrupts by setting rtc_sec_alm_upd_int_en, rtc_min_alm_upd_int_en,

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

rtc_hour_alm_upd_int_en and rtc_day_alm_upd_int_en, check status by reading rtc_sec_alm_upd_int_mask_sts, rtc_min_alm_upd_int_mask_sts, rtc_hour_alm_upd_int_mask_sts and rtc_day_alm_upd_int_mask_sts, and clear these interrupts by writing 1 to rtc_sec_alm_upd_int_clr, rtc_min_alm_upd_int_clr, rtc_alm_upd_hour_int_clr and rtc_day_alm_upd_int_clr. The changes to the four counters are independent, and it does not need waiting for first changing to complete before changing next one.

Because RTC timers are in RTC clock domain, all interrupts can be used to wakeup system from deep sleep. Another important function is alarm interrupt can power up base band chip from power-down mode.

5.13 Watchdog Timer

ARM base address: 0x8200_1480

5.13.1 Overview

Watchdog timer is a 32-bit decreasing timer with RTC-clock trigged, and this timer can be used to issue system reset.

5.13.2 Features

- RTC-clock trigged
- 32-bit decreasing timer
- Support 32-bit timer value loading
- Support reset mode for watchdog function
- Support interrupt mode for debug function and timer function
- Support combined mode: first generate interrupt, and then generate reset.
- Support single read : no need to double read when reading counter value
- Support multiple load : no need to check busy bit before load tmr
- Support read counter value immediately after loading tmr: once tmr is loaded, the counter value is updated immediately

5.13.3 Signal description

Null

5.13.4 Funtion description

After hardware reset, watchdog timer is 32'hFFFF_FFFF.

And after enabled, watchdog timer decreases from the reset value or from software-loading value.

The counting step is one RTC clock cycle.

For reset mode, whenever watchdog timer gets to 0, system reset is issued. Then system reboots, and watchdog timer comes back to 32'hFFFF_FFFF, and all controlled registers and status also come back to reset value, except interrupt raw status. Interrupt raw status can be used to judge if or not system rebooting comes from watchdog reset.

For interrupt mode, watchdog timer runs as a periodic generic timer. If watchdog timer gets to 0, an interrupt is issued, and then the timer is reloaded automatically.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

For combined mode, it can be considered as the combination of reset mode and interrupt mode. Interrupt will be generated first if software doesn't feed wdg. Then software should stop wdg so that wdg reset is not generated. If software cannot response to this interrupt, then wdg reset will be generated finally when wdg_cnt decease to 0 which reboots the entire system.

After enabled, watchdog timer can be loaded at any time, and software should guarantee the timer is loaded before it decreases to 0.

Reset mode is used as normal watchdog function. And interrupt mode is used as debug mode or as a generic periodic timer.

5.13.5 Control registers

5.13.5.1 Memory map

Offset Address	Name	Description
0x1000	WDG_LOAD_LOW	Low 16 bit of watchdog load value
0x1004	WDG_LOAD_HIGH	High16 bit of watchdog load value
0x1008	WDG_CTRL	Watchdog control**(add wdg_new wdg_rst_en)**
0x100C	WDG_INT_CLR	Watchdog interrupt clear**(add wdg_rst_clr)**
0x1010	WDG_INT_RAW	Watchdog interrupt raw status**(add wdg_rst_raw)**
0x1014	WDG_INT_MASK	Watchdog interrupt masked status
0x1018	WDG_CNT_LOW	Low 16 bit of watchdog counter value
0x101C	WDG_CNT_HIGH	High16 bit of watchdog counter value
0x1020	WDG_LOCK	Watchdog lock
0x1024	WDG_CNT_RD_LOW	Low 16 bit of watchdog counter value for read**(new added)**
0x1028	WDG_CNT_RD_HIGH	High 16 bit of watchdog counter value for read**(new added)**
0x102C	WDG_IRQVALUE_LOW	Low 16 bit of watchdog irq value**(new added)**
0x1030	WDG_IRQVALUE_HIGH	High 16 bit of watchdog irq value**(new added)**

5.13.5.2 Register description

5.13.5.2.1 WDG_LOAD_LOW

Description: Low 16 bit of watchdog load value

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1000			Low 16 bit of watchdog load value (Reset 0x1000_FFFF)										WDG_LOAD_LOW			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdg_load_low															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
wdg_load_low	[15:0]	RW	16'hFFFF	wdg_load_low: low 16 bit of watchdog timer load value. Wdg_load_high: high 16 bit of watchdog timer load value. wdg_load_low and wdg_load_high are used together. Software should write wdg_load_high firstly, and then write wdg_load_low, because writing wdg_load_low can trig loading both wdg_load_low and wdg_load_high to watchdog counter, and writing wdg_load_high cannot trig this event. So software must guarantee wdg_load_high is ready when writing wdg_load_low. In reset mode, software should load new value before timer decrease to 0. In interrupt mode, this value is counting start number. The default value is about 8 seconds.

5.13.5.2.2 **WDG_LOAD_HIGH**

Description: High 16 bit of watchdog load value

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1004	High 16 bit of watchdog load value (Reset 0x1000_0003)												WDG_LOAD_HIGH			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdg_load_high															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
wdg_load_high	[15:0]	RW	16'h0003	See wdg_load_low description

5.13.5.2.3 **WDG_CTRL (add wdg_new wdg_rst_en)**

Description: Watchdog control

0x1008	Watchdog control (Reset 0x1000_0000)															WDG_CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												wdg_rst_en	wdg_new	wdg_run	wdg_irq_en
Type	RO												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:4]	RO	28'h0	Reserved
wdg_rst_en	[3]	RW	1'h0	Watchdog reset enable bit 0: reset is disabled 1: reset is enabled In reset mode and combined mode, this bit should be 1
wdg_new	[2]	RW	1'h0	Watchdog version 0: watchdog use old behavior, this is for backward compatibility. 1: watchdog uses new

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Default Value	Description
				behavior, such as multiple loads without checking busy bit, only need to read once to get timer counter value.
wdg_run	[1]	RW	1'h0	Watchdog counter open: 0: counter stops. 1: counter runs.
wdg_irq_en	[0]	RW	1'h0	Watchdog interrupt enable bit 0: interrupt is disabled 1: interrupt is enabled In interrupt mode and combined mode, this bit should be 1

5.13.5.2.4 **WDG_INT_CLR**

Description: Watchdog interrupt clear

0x100C			Watchdog interrupt clear (Reset 0x1000_0000)										WDG_INT_CLR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												wdg_rst_clr	Reserved		wdg_int_clr
Type	RO												WO	RO		WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:4]	RO	28'h0	Reserved
wdg_rst_clr	[3]	WO	1'h0	Watchdog reset clear Write 1 to this bit to clear reset Read this bit always get 0.
	[2:1]	RO	2'h0	Reserved
wdg_int_clr	[0]	WO	1'h0	Watchdog interrupt clear Write 1 to this bit to clear interrupt Read this bit always get 0.

5.13.5.2.5 **WDG_INT_RAW**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Description: Watchdog interrupt raw status

0x1010	Watchdog interrupt raw status (Reset 0x1000_0000)															WDG_INT_RAW
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											wdg_ld_bus	wdg_rst_raw	Reserved		wdg_int_raw
Type	RO											RO	RO	RO		RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:5]	RO	27'h0	Reserved
wdg_ld_busy	[4]	RO	1'h0	Watchdog load busy status 0: Watchdog is ready for new loading 1: Last loading is not completed Software must not load new value when this bit is busy, that is, this bit should be checked before any new loading. This bit is set after a new loading, and lasts two or three RTC clock cycles, about 60us - 92us.
wdg_rst_raw	[3]	RO	1'h0	Watchdog reset raw status. Watch dog reset cannot clear this raw status, so it can be used to judge if or not system rebooting comes from watchdog reset. Write wdg_rst_clr can clear this raw status.
	[2:1]	RO	2'h0	Reserved
wdg_int_raw	[0]	RO	1'h0	Watchdog interrupt raw status. Watch dog reset cannot clear this raw status. Write wdg_int_clr can clear this raw status.

5.13.5.2.6 **WDG_INT_MASK**

Description: Watchdog interrupt mask status

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1014			Watchdog interrupt mask status (Reset 0x1000_0000)													WDG_INT_MASK
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															wdg_int_mask
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:1]	RO	31'h0	Reserved
wdg_int_mask	[0]	RO	1'h0	Watchdog interrupt masked status

5.13.5.2.7 **WDG_CNT_LOW**

Description: Low 16 bit of watchdog counter value

0x1018			Low 16 bit of watchdog counter value (Reset 0x1000_FFFF)													WDG_CNT_LOW
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdg_cnt_low															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
wdg_cnt_low	[15:0]	RO	16'hFFFF	wdg_cnt_low: Low 16 bit of watchdog timer counter value. wdg_cnt_high: High 16 bit of watchdog timer counter value. wdg_cnt_low and wdg_cnt_high are used together. This read-only register indicates current counter value.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Reset Value	Description
				It's not recommended to read this register in normal usage. Because the counter is in different clock domain with APB, software needs use double-reading method to read this value, like system timer.

5.13.5.2.8 **WDG_CNT_HIGH**

Description: High 16 bit of watchdog counter value

0x101C			High 16bit of watchdog counter value (Reset 0x1000_FFFF)											WDG_CNT_HIGH		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdg_cnt_high															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
wdg_cnt_high	[15:0]	RO	16'hFFFF	See wdg_cnt_low description.

5.13.5.2.9 **WDG_LOCK**

Description: Watchdog lock control

0x1020			Watchdog lock control (Reset 0x1000_0000)													WDG_LOCK
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdg_lock															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
wdg_lock	[15:0]	RW	16'h0	Watchdog lock control Write 16'hE551 to this register to unlock watchdog. Write other value to this register to lock watchdog If reading this register, bit-0 is lock status, and other bits are reserved. If watchdog is locked, all control registers cannot be written by software.

5.13.5.2.10 **WDG_CNT_RD_LOW**

Description: Low 16 bit of watchdog counter value for read

0x1024	**Low 16 bit of watchdog counter value for read(Reset 0x1000_FFFF)**														**WDG_CNT_RD_LOW**	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdg_cnt_rd_low															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
wdg_cnt_rd_low	[15:0]	RO	16'hFFFF	wdg_cnt_rd_low: Low 16 bit of watchdog timer counter value for read. wdg_cnt_rd_high: High 16 bit of watchdog timer counter value for read. wdg_cnt_rd_low and wdg_cnt_rd_high are used together. This read-only register indicates current counter value. Read once can get watchdog counter value. No need to

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Reset Value	Description
				double read this reg. Refer to timer's TIMER0_CNT_RD or TIMER1_CNT_RD

5.13.5.2.11 **WDG_CNT_RD_HIGH**

Description: High 16 bit of watchdog counter value for read

0x1028			**High 16bit of watchdog counter value for read (Reset 0x1000_FFFF)**										**WDG_CNT_RD_HIGH**			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdg_cnt_rd_high															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
wdg_cnt_rd_high	[15:0]	RO	16'hFFFF	Refer to wdg_cnt_rd_low

5.13.5.2.12 **WDG_IRQVALUE_LOW**

Description: Low 16 bit of watchdog irq value

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x102C			Low 16 bit of watchdog irq value (Reset 0x1000_0000)										WDG_IRQVALUE_LOW			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdg_irqvalue_low															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
wdg_irqvalue_low	[15:0]	RW	16'h0000	wdg_ irqvalue_low: Low 16 bit of watchdog irqvalue. wdg_ irqvalue_high: High 16 bit of watchdog irqvalue. wdg_ irqvalue_low and wdg_ irqvalue_high are used together. It's useful in interrupt mode and combined mode. When wdg_cnt equal watchdog irqvalue, an interrupt is generated. Default value of watchdog irqvalue is 32'h0003_0000, corresponds to 6 seconds, which means reset will occur after irq is 1 for 6 seconds.

5.13.5.2.13 **WDG_IRQVALUE_HIGH**

Description: High 16 bit of watchdog irq value

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1030			High 16 bit of watchdog irq value (Reset 0x1000_0003)										WDG_IRQVALUE_HIGH			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	wdg_irqvalue_high															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
wdg_irqvalue_high	[15:0]	RW	16'h0003	wdg_ irqvalue_low: Low 16 bit of watchdog irqvalue. wdg_ irqvalue_high: High 16 bit of watchdog irqvalue. wdg_ irqvalue_low and wdg_ irqvalue_high are used together, which means reset will occur after irq is 1 for 6 seconds. It's useful in interrupt mode and combined mode. When wdg_cnt equal watchdog irqvalue, an interrupt is generated. Default value of watchdog irqvalue is 32'h0003_0000, corresponds to 6 seconds.

5.13.6 Application notes

When software uses watchdog, it should set wdg_eb bit and wdg_rtc_eb bit in global control register, and also should guarantee arch_rtc_eb is set.

Before configuring watchdog, software should write 16'hE551 to wdg_lock to unlock watchdog.

Then Software configures all control registers – wdg_load_low, wdg_load_high, wdg_irqvalue_low, wdg_irqvalue_high, wdg_mode and wdg_new.

IMPORTANT: wdg_load_high should always be configured before writing wdg_load_low.

Then wdg_run is set to 1 to open counter.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reset mode is used as normal watchdog function. After enabled, watchdog timer can be loaded at any time, and software should guarantee the timer is reloaded before it decreases to 0.

Whenever watchdog timer gets to 0, system reset is issued. Then system reboots, and watchdog timer comes back to 32'hFFFF_FFFF, and all controlled registers and status also come back to reset value, except interrupt raw status. Interrupt raw status can be used to judge if or not system rebooting comes from watchdog reset.

For interrupt mode, watchdog timer runs as a periodic generic timer. If watchdog timer gets to 0, an interrupt is issued, and then the timer is reloaded automatically.

After receiving interrupt, software can check interrupt status by reading wdg_int_mask, and can clear interrupt by writing 1 to wdg_int_clr.

Interrupt mode is used as debug mode or as a generic periodic timer.

Combined mode is the combination of reset mode and interrupt mode. Interrupt will be generated first if software doesn't feed wdg. Then software should stop wdg so that wdg reset is not generated. If software cannot response to this interrupt, then wdg reset will be generated finally when wdg_cnt decease to 0 which reboots the entire system.

When software completes using watchdog, it should disable wdg_run firstly, then it disable wdg_rtc_eb and wdg_eb in global control registers.

It's IMPORTANT that only writing wdg_load_high cannot reload watchdog. Both wdg_load_low and wdg_load_high should be written if watchdog need reloaded. And software must write wdg_load_high firstly, then write wdg_load_low.

Another IMPORTANT thing is that there are 3-5 RTC clock cycles delay from setting wdg_load_low to counter setting success because of different clock domains, just as timer does.

It's not recommended to read counter value in normal usage, just as timer does.

5.13.7 Implementations

Logic in clk_rtc domain should be synthesized at least 26M, just as timer does.

5.13.8 Future improvements

- There are 3-5 RTC clock cycles delay from loading watchdog to counter setting success just as timer does.
- In current design, when PCLK is closed, wdg_cnt_rd_low and wdg_cnt_rd_high is not accurate, just as timer does.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.14 Charge Watchdog(for internal only)

5.14.1 Overview

SC6531 supports high constant-current charge which is completely controlled by software through PWM charge. A protect module is provided that could power down charge circuit in case the high current charge is out of control when software is abnormal

5.14.2 Features

- The protect module could be initialized by software through APB bus.
- When PWM charge mode start, the protect module automatically starts at the same time.
- The protect module is mainly implemented by a WDG which should be “feed” by software periodically in PWM charge mode.
- Power down signal will be active when WDG count to zero, interrupt is generated at the same time.
- Power down and interrupt signals are all level active which need software to clear respectively.

5.14.3 Signal description

Null

5.14.4 Funtion description

When the chip is in charge, it could be set in high current charge mode for shorting charge time. In this charge mode, the software triggers a switch signal to start or stop charge. When to start or stop is basis on software algorithm. However the consequent risk is coming. Once the software falls into abnormal state in this charge mode, chip could be damaged by high current without of software’s control.

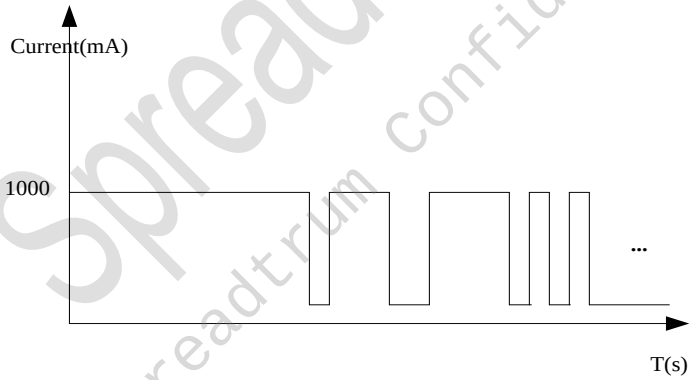


Figure 5-83 High current charge

In order to avoid this risk, a charge protect module which use a watch dog as its core is added to protect the high current charge. In high current charge mode, normal software should periodically “feed dog”. Once software falls into abnormal situation, the watch dog will power down charge circuit until software clears the power down signal.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

The protect module's control registers could be configured by APB bus as a APB slave. The generated charge power down signal for protect will be sent into RTC domain to OR the normal one for software control.

The main function of charge protect module is:

Generate power down signal to power down charge when the WDG time out;

Generate interrupt to MCU when the WDG time out;

5.14.5 Control registers

5.14.5.1 Memory map

ARM base address: 0x8200_1500

Offset Address	Name	Description
0x1000	WD_LOAD_LOW	Low 16 bit of Watchdog load
0x1004	WD_LOAD_HIGH	High16 bit of Watchdog load
0x1008		Reserved
0x100C	WD_ CLR	Watchdog interrupt and charge PD clear
0x1010	WD_RAW_STATUS	Watchdog raw interrupt and charge PD
0x1014	WD_MSK_STATUS	Watchdog masked interrupt and charge PD
0x1018	WD_CNT_LOW	Low 16 bit current value of the counter
0x101C	WD_CNT_HIGH	High16 bit of current value of the counter
0x1020	WD_LOCK	Watchdog lock

5.14.5.2 Register description

5.14.5.2.1 WD_LOAD_LOW

Description: Low 16 bit of Watchdog load

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1000	Low 16 bit of Watchdog load (reset 0xFFFF)												WD_LOAD_LOW			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WD_LOAD_LOW															
Type	R/W															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
WD_LOAD_LOW	[15:0]	R/W	16'hFFFF	Low 16 bit of watchdog Load (together with WD_LOAD_HIGH, default value equals 8 seconds). The unit of this load value is rtc_clk. First write WD_LOAD_HIGH and then write WD_LOAD_LOW and check WD_LD_BUSY, if it's 0, wdg have loaded the value completely. if it's 1, wdg is busy with loading.

5.14.5.2.2 **WD_LOAD_HIGH**

Description: High 16 bit of Watchdog load

0x1004	High 16 bit of Watchdog load (reset 0x1003)												WD_LOAD_HIGH			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WD_LOAD_HIGH															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Field Name	Bit	Type	Reset Value	Description
WD_LOAD_HIGH	[15:0]	R/W	16'h0003	High 16 bit of watchdog Load ((together with WD_LOAD_LOW, default value equals 8 seconds)). The unit of this load value is rtc_clk. First write WD_LOAD_HIGH and then write WD_LOAD_LOW and check WD_LD_BUSY, if it's 0, wdg have loaded the value completely. if it's 1, wdg is busy with loading.

5.14.5.2.3 **WD_CTRL**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Description: Watchdog control

0x1008	Watchdog control (reset 0x1000)															WD_CTRL
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															WD INT_ EN
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Field Name	Bit	Type	Reset Value	Description
Reserved	[15:1]	RO	15'h0000	Reserved
WD_INT_EN	[0]	R/W	1'h1	Watchdog interrupt enable, active high

5.14.5.2.4 **WD_CLR**

Description: Watchdog interrupt and charge PD clear

0x100C	Watchdog interrupt and PD clear (reset 0x1000)														WD_ CLR	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved														WD_	WD_
Type	RO														WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Reserved	[15:1]	RO	14'h0000	Reserved
WD_PD_CLR	[1]	WO	1'h0	Watchdog charge power down clear
WD_INT_CLR	[0]	WO	1'h0	Watchdog interrupt clear

5.14.5.2.5 **WD_RAW_STATUS**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Description: Watchdog interrupt and power down status

0x1010	Watchdog raw interrupt and PD(reset 0x1000)											WD_STATUS			
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											WD_LD_BUS	Reserved		WD_PD_RA	WD_INT_RA
Type	RO											RO	RO		RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Reserved	[15:5]	RO	11'h000	Reserved
WD_LD_BUSY	[4]	RO	1'h0	Watchdog load busy. When WDG_LD_BUSY is 1, wdg is busy with loading value. First write WD_LOAD_HIGH and then write WD_LOAD_LOW and check WD_LD_BUSY, if it's 0, wdg have loaded the value completely. if it's 1, wdg is busy with loading.
Reserved	[3:2]	RO	2'h0	Reserved
WD_PD_RAW	[1]	RO	1'h0	Watchdog raw charge power down
WD_INT_RAW	[0]	RO	1'h0	Watchdog raw interrupt

5.14.5.2.6 **WD_MSK_STATUS**

Description: Watchdog masked interrupt and power down

0x1014	Watchdog masked interrupt and PD(reset 0x1000)															WD_MSK_STATUS
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															WD_INT_MSK
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reserved	[15:1]	RO	15'h0000	Reserved
WD_INT_MSK	[0]	RO	1'h0	Watchdog masked interrupt by wdg_irq_en

5.14.5.2.7 **WD_CNT_LOW**

Description: Low 16 bit of current value of the counter

0x1018	Low 16 bit of current value of the counter (reset 0xFFFF)												WD_CNT_LOW			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WD_CNT_LOW															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
WD_CNT_LOW	[15:0]	RO	16'hFFFF	Low 16 bit of current value of the counter

5.14.5.2.8 **WD_CNT_HIGH**

Description: High 16 bit of current value of the counter

0x101C	High 16 bit of current value of the counter (reset 0xFFFF)												WD_CNT_HIGH			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WD_CNT_HIGH															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
WD_CNT_HIGH	[15:0]	RO	16'hFFFF	High 16 bit of current value of the counter

5.14.5.2.9 **WD_LOCK**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Description: Watchdog lock

0x1020	Watchdog lock (reset 0x1000)															WD_LOCK
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WD_LOCK															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
WD_LOCK	[15:0]	WO	16'h0000	Write for lock/unlock Watchdog Write 0xE551: unlock Write others: lock
WD_LOCK_ST	[0]	RO	1'h0	Read for lock status 0: unlocked 1: locked

5.14.6 Application notes

Step 1 : Before constant-current charge software initialize watch dog

Step 2 : Start charge and periodically feed the dog at the same time.

Step 3 : When charge process finish, software stop watch dog.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

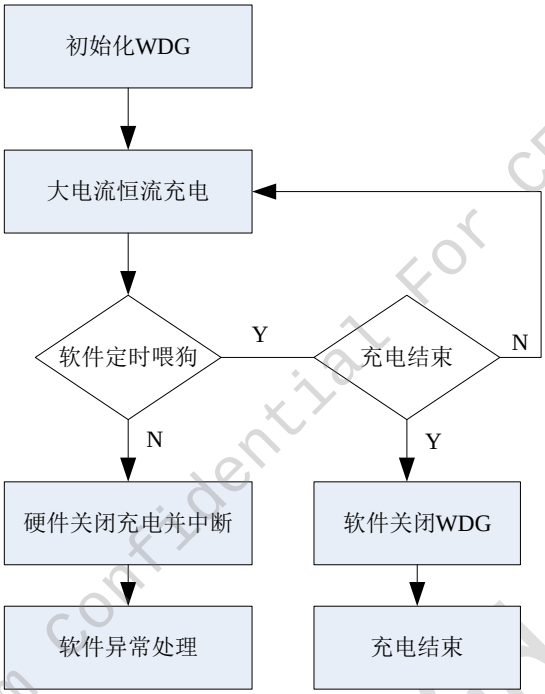


Figure 5-84 Software control flow

5.15 LZMA Decompress Accelerator (for internal only)

5.15.1 Overview

The LZMA decompress module is designed to decompress data with lzma compressed format.

Compressed data can be stored in FLASH or external RAM. And decompressed data will be transferred to internal RAM or external RAM. Decompress module supports buffered decompress. That means decompress operation can be done in internal RAM and the result be transferred to external RAM. Also it supports fetch segments of the decompressed data. Decompress module can output specific length of data to destination RAM.

LZMA compress algorism comprises two parts. One is range coding. The other is dictionary coding. So the decompress module is designed based on these two decoding parts. A basic diagram is shown in pic below .

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

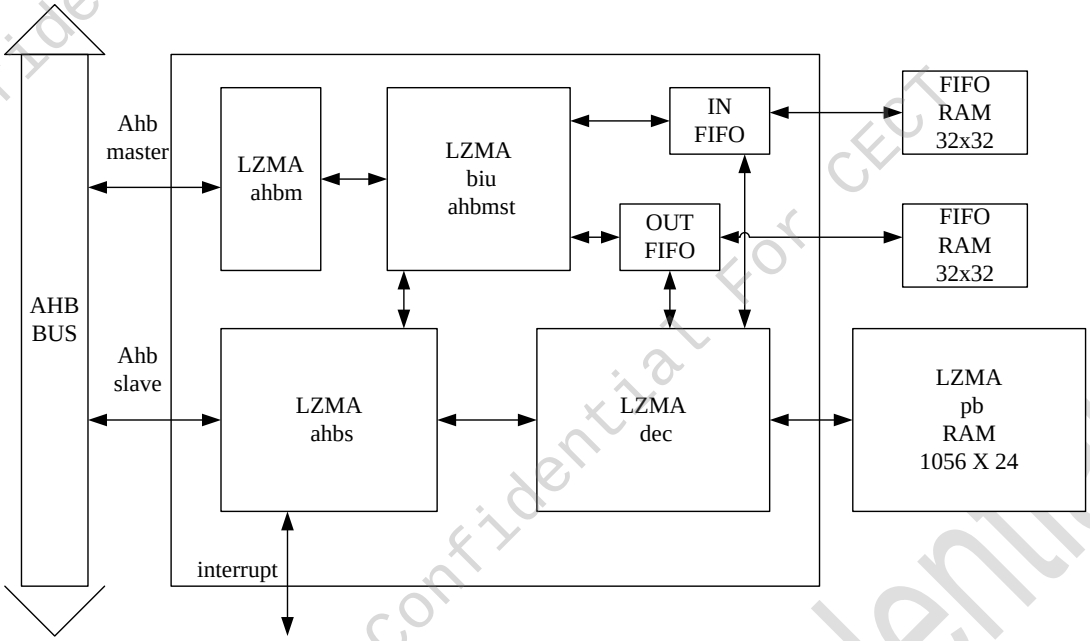


Figure 5-85 LZMA decompress module diagram.

LZMA ahbm comverts internal data transfer signal to AHB burst transfer signal. Biu ahbmst module controls dictionary decompress function , including “length ,distance” look up and write back function . It exchange data with LZMA dec module by using 2 cross clock domain data FIFO. LZMA dec module contains main decoding state machine. Its input is origin compressed data flow, and output is decompressed symbol (1byte data) and “length ,distance” information.

LZMA ahbs controls all the registers.

5.15.2 Features

- Support LZMA decompress algorithm(modified),
- AHB bus supported
- Support export segment of decompressed data.

5.15.3 Register Address Map

DSP base address: 0x20C0_0000

Offset Address	Name	Description
0x1000	LZMA_CTRL	LZMA control registers
0x1004	LZMA_CTRL_STS	lzma control status registers
0x1008	LZMA_INT	lzma interrupt register
0x100C	LZMA_SRC_SADDR	lzma source start address
0x1010	LZMA_DST_SADDR	lzma dest start address
0x1014	LZMA_SRC_LEN	lzma source length
0x1018	LZMA_DST_LEN	lzma dest length
0x101C	LZMA_BUFFER_SADDR	buffer start address
0x1020	LZMA_BUFFER_LEN	buffer length
0x1024	LZMA_BUFFER_START_LEN	buffer start length for transfer to dest address

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1028	LZMA_PROC_POS	proccessed postion
0x102C	LZMA_TRANS_LEN	total transfer length
0x1030	LZMA_UNZIP_SIZE	file size decoded from file header
0x1034	LZMA_STOP	Lzma stop reg
0x1038	LZMA_DEBUG_1	Debug reg 1
0x103C	LZMA_DEBUG_2	Debug reg 2
0x1040	LZMA_DEBUG_3	Debug reg 3
0x1044	LZMA_ENDIAN	Lzma endian control reg

5.15.3.1 LZMA_CTRL

0x1000			LZMA control registers (0x10000000)										LZMA_CTRL_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVED												BUFFER_FULL_DEC	BUFFER_EN	TRANSFER	START
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

including start, transfer state, buffer enable set and buffer full dec set

Field Name	Bit	Type	Reset Value	Description
RESERVED	[31:4]	RO	0x0	reserved
BUFFER_FULL_DEC	[3]	WO	0x0	only active when BUFFER_EN is set to 1. 0: decompression will finish when decomp size meet unzip size or BUFFER_START_LEN + DST_LENGTH. 1: decompression will finish when decomp size meet unzip size or BUFFER_LENGTH RWite set, RWite clear
BUFFER_EN	[2]	WO	0x0	0: won't begin data transfer 1: will begin transfer when decompression is over. If set to 0, BUFFER_SADDR, BUFFER_LENGTH, BUFFER_START_LENGTH won't be used. Controller use DST_SADDR and DST_LENGTH directly for decompression. If set to 1, Controller will decomp data to buffer and transfer data to DST_SADDR after decomp is finish. RWite set, RWite clear
TRANSFER	[1]	WO	0x0	status bit. Active only when BUFFER_EN is set. 0:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				Data transfer is not ongoing 1:Data transfer is ongoing. RWite 0 when data transfer is ongoing can stop operattion. Notice If BUFFER_EN is set, then both START and TRANSFER is cleared to 0 means operation is over. self set, self clear, transfer status
START	[0]	WO	0x0	Active bit status bit. Indicates that decompression occurs: 0: Decompression is not ongoing. 1: Decompression is ongoing. Self cleared when decompression is finished. RWite 1 to begin decompression, if BUFFER_EN is set to 0, then this bit 0 shows all decompression is over. If BUFFER_EN is set t o1, then both START and TRANSFER bit should be checked. RWite 0 when decompression is ongoing can stop the operation. RWite set, self clear, running status

5.15.3.2 LZMA_CTRL_STS

0x1000			LZMA control registers (0x10000000)										LZMA_CTRL_REG			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVED												BUFFER_FULL_DEC_STS	BUFFER_EN_STS	TRANSFER_STS	START_STS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

all interrupt status can be checked here.

Field Name	Bit	Type	Reset Value	Description
RESERVED	[31: 4]	RO	0x0	reserved
BUFFER_FULL_DEC_STS	[3]	RO	0x0	Staturs of BUFFER_FULL_DEC
BUFFER_EN_STS	[2]	RO	0x0	Status of BUFFER_EN
TRANSFER_STS	[1]	RO	0x0	Status of TRANSFER
START_STS	[0]	RO	0x0	Status of START

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.15.3.3 LZMA_INT

0x1008	lzma interrupt mask register (0x10000003)												LZMA_INT_MSK			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED			BUF_LEN_ERR_INT_RAW	DST_LEN_ERR_INT_RAW	DEC_ERR_INT_RAW	MST_ERR_INT_RAW	LZMA_FIN_RAW	RESERVED			BUF_LEN_ERR_INT_STS	DST_LEN_ERR_INT_STS	DEC_ERR_INT_STS	MST_ERR_INT_STS	LZMA_FIN_STS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVED			BUF_LEN_ERR_INT_CLR	DST_LEN_ERR_INT_CLR	DEC_ERR_INT_CLR	MST_ERR_INT_CLR	LZMA_FIN_CLR	RESERVED			BUF_LEN_ERR_INT_EN	DST_LEN_ERR_INT_EN	DEC_ERR_INT_EN	MST_ERR_INT_EN	LZMA_FIN_EN
Type	RO	RO	RO	RW	RW	RW	RW	RW	RO	RO		RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0

lzma interrupt mask

Field Name	Bit	Type	Reset Value	Description
RESERVED	[31:29]	RO	0x0	Reserved
BUF_LEN_ERR_INT_RAW	[28]	RO	0x0	0: buffer length set ok 1: buffer length set error Only active when BUFFER_EN set. Set when BUFFER_LEN < UNZIP_SIZE. It doesn't means true error . It only indicates the user should consider the BUFFER length carefully sel set ,RWite clear
DST_LEN_ERR_INT_RAW	[27	RO	0x0	0: dest length set ok 1: dest length set error Only active when BUFFER_EN not set . Set when DST_LENGTH < UNZIP_SIZE , It doesn't means true error . It only indicates the user should consider the dest length carefully sel set ,RWite clear
DEC_ERR_INT_RAW	[26]	RO	0x0	0: decompression no error 1: decompression error Set when decode error, compare distance with processed bytes. sel set ,RWite clear
MST_ERR_INT_RAW	[25]	RO	0x0	0: decompression no error 1:decompression error Set when decode processed bytes number differ for RWite out mem bytes number

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				sel set ,RWite clear
LZMA_FIN_RAW	[24]	RO	0x0	0: decompression not finish 1:decompression finish sel set ,RWite clear
RESERVED	[23:21]	RO	0x0	Reserved
BUF_LEN_ERR_INT_STS	[20]	RO	0x0	Masked int of BUF_LEN_ERR_INT 0: buffer length set ok 1: buffer length set error Only active when BUFFER_EN set. Set when BUFFER_LEN < UNZIP_SIZE. It doesn't means true error . It only indicates the user should consider the BUFFER length carefully sel set ,RWite clear
DST_LEN_ERR_INT_STS	[19	RO	0x0	Masked int of DST_LEN_ERR_INT 0: dest length set ok 1: dest length set error Only active when BUFFER_EN not set . Set when DST_LENGTH < UNZIP_SIZE , It doesn't means true error . It only indicates the user should consider the dest length carefully sel set ,RWite clear
DEC_ERR_INT_STS	[18]	RO	0x0	Masked int of DEC_ERR_INT 0: decompression no error 1: decompression error Set when decode error, compare distance with processed bytes. sel set ,RWite clear
MST_ERR_INT_STS	[17]	RO	0x0	Masked int of MST_ERR_INT 0: decompression no error 1:decompression error Set when decode processed bytes number differ for RWite out mem bytes number sel set ,RWite clear
LZMA_FIN_STS	[16]	RO	0x0	Masked int of LZMA_FIN 0: decompression not finish 1:decompression finish sel set ,RWite clear
RESERVED	[15:13]	RO	0x0	Reserved
BUF_LEN_ERR_INT_CLR	[12]	RW	0x0	Write 1 clear BUFFER_LEN_ERR_INT_RAW
DST_LEN_ERR_INT_CLR	[11	RW	0x0	Write 1 clear DST_LEN_ERR_INT_RAW
DEC_ERR_INT_CLR	[10]	RW	0x0	Write 1 clear DEC_ERR_INT_RAW
MST_ERR_INT_CLR	[9]	RW	0x0	Write 1 clear MST_ERR_INT_RAW
LZMA_FIN_CLR	[8]	RW	0x0	Write 1 clear LZMA_FIN_RAW
RESERVED	[7:5]	RO	0x0	Reserved
BUF_LEN_ERR_INT_EN	[4]	RW	0x0	Write 1 enable BUF_LEN_ERR_INT_STS
DST_LEN_ERR_INT_EN	[3]	RW	0x0	Write 1 enable DST_LEN_ERR_INT_STS
DEC_ERR_INT_EN	[2]	RW	0x0	Write 1 enable DEC_ERR_INT_STS
MST_ERR_INT_EN	[1]	RW	0x0	Write 1 enable MST_ERR_INT_STS

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

LZMA_FIN_EN	[0]	RW	0x0	Write 1 enable LZMA_FIN_STS

5.15.3.4 LZMA_SRC_SADDR

0x100C			lzma source start address (0x10000000)										LZMA_SRC_SADDR			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_SADDR															
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_SADDR															
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

lzma source start address

Field Name	Bit	Type	Reset Value	Description
SRC_SADDR	[31: 0]	RW	0x0	compressed data source address RWite set, RWite clear

5.15.3.5 LZMA_DST_SADDR

0x1010			lzma dest start address (0x10000000)										LZMA_DST_SADDR			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DST_SADDR															
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST_SADDR															
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

lzma dest start address

Field Name	Bit	Type	Reset Value	Description
DST_SADDR	[31: 0]	RW	0x0	decompressed data will RWite to this address finally RWite set, RWite clear

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.15.3.6 LZMA_SRC_LEN

0x1014			lzma source length (0x10000000)										LZMA_SRC_LEN			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_LENGTH															
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_LENGTH															
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

lzma source length

Field Name	Bit	Type	Reset Value	Description
SRC_LENGTH	[31: 0]	RW	0x0	compressed data length. RWite set, RWite clear

5.15.3.7 LZMA_DST_LEN

0x1018			lzma dest length (0x10000000)										LZMA_DST_LEN			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DST_LENGTH															
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST_LENGTH															
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

lzma dest length

Field Name	Bit	Type	Reset Value	Description
DST_LENGTH	[31: 0]	RW	0x0	if BUFFER_EN is 0, decompression will finish when decompressed data size meet DST_LENGTH. If BUFFER_EN is 1, controller will transfer data from buffer to dest saddr with size DST_LENGTH or file size (the smaller) RWite set, RWite clear

5.15.3.8 LZMA_BUFFER_SADDR

0x101C	buffer start address (0x10000000)	LZMA_BUFFER_SADDR

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUFFER_SADDR															
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUFFER_SADDR															
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

buffer start address

Field Name	Bit	Type	Reset Value	Description
BUFFER_SADDR	[31:0]	RW	0x0	Only active when BUFFER_EN is set to 1. controoler will decompress data to this address first, and then transfer to DST_SADDR RWite set, RWite clear

5.15.3.9 LZMA_BUFFER_LEN

0x1020		buffer length (0x10000000)											LZMA_BUFFER_LEN			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUFFER_LEN															
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUFFER_LEN															
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

buffer total length

Field Name	Bit	Type	Reset Value	Description
BUFFER_LEN	[31:0]	RW	0x0	Only active when BUFFER_EN is set to 1. Decompression size won't larger than BUFFER_LEN RWite set, RWite clear

5.15.3.10 LZMA_BUFFER_START_LEN

0x1024		buffer start length for transfer to dest address (0x10000000)										LZMA_BUFFER_START_LEN			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUFFER_START_LEN															

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUFFER_START_LEN															
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

buffer start length for transfer to dest address

Field Name	Bit	Type	Reset Value	Description
BUFFER_START_LEN	[31: 0]	RW	0x0	Only active when BUFFER_EN is set to 1. After dcompression is over, transfer will begin . Data will be transferred from BUFFER_START_LEN to DST_SADDR. Size is DST_LENGTH or file size (the smaller) RWite set, RWite clear

5.15.3.11 LZMA_PROC_POS

0x1028			proccessed postion (0x10000000)										LZMA_PROC_POS			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PROC_POS															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PROC_POS															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

decompressed total byte size

Field Name	Bit	Type	Reset Value	Description
PROC_POS	[31: 0]	RO	0x0	indicates how many bytes have been decompressed. self set, read only

5.15.3.12 LZMA_TRANS_LEN

0x102C			total transfer length (0x10000000)										LZMA_TRANS_LEN			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TRANS_LEN															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANS_LEN															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

indecates how many bytes have been transferred

Field Name	Bit	Type	Reset Value	Description
TRANS_LEN	[31:0]	RO	0x0	Only active when BUFFER_EN is set to 1 . Indicates how many bytes have been transferred from buffer to dest address. self set, read only

5.15.3.13 LZMA_UNZIP_SIZE

0x1030			file size decoded from file header (0x10000000)										LZMA_UNZIP_SIZE			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UNZIP_SIZE															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNZIP_SIZE															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

file size decoded from file header

Field Name	Bit	Type	Reset Value	Description
UNZIP_SIZE	[31:0]	RO	0x0	file size decoded from file header. Only available after decompression is begin. self set, read only

5.15.3.14 LZMA_STOP

0x1034			LZMA stop registers (0x10000000)										LZMA_STOP			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVED														TRANSFER	STAR
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	WO	WO	WO	WO

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

including start and transfer stop bit

Field Name	Bit	Type	Reset Value	Description
RESERVED	[31: 4]	RO	0x0	reserved
TRANSFER_STP	[1]	WO	0x0	Write 1 clear TRANSFER bit , transfer will stop, note: please clear both START_STOP and TRANSFER_STOP at the same time
START_STP	[0]	WO	0x0	Write 1 clear START bit , decompress will stop. note: please clear both START_STOP and TRANSFER_STOP at the same time

5.15.3.15 LZMA_DEBUG_1

0x1038			LZMA Debug registers (0x10000000)								LZMA_DEBUG_1					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED										MULT_STP	INFF_EMPTY	OUTFF_FULL	PB		DEC_ST
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEC_STS				LEN_DIST	BUF_CNT					WB	BUF_ST		BIU_STATE		
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

including start and transfer stop bit

Field Name	Bit	Type	Reset Value	Description
RESERVED	[31: 22]	RO	0x0	reserved
MULT_STP	[21]	RO	0x0	Debug only, multi stop sig
INFF_EMPTY	[20]	RO	0x0	Debug only, in fifo empty sig
OUFF_FULL	[19]	RO	0x0	Debug only, out fifo full sig
PB	[18:17]	RO	0x0	Debug only, PB parameter
DEC_STS	[16:12]	RO	0x0	Debug only, decompress fsm state
LEN_DIST	[11]	RO	0x0	Debug only, length, distance sig
BUF_CNT	[10:6]	RO	0x0	Debug only, master buffer count
WB	[5]	RO	0x0	Debug only, write back sig
BUF_ST	[4:3]	RO	0x0	Debug only, master buffer state
BIU_STATE	[2: 0]	RO	0x10	Debug only, master fsm state

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.15.3.16 LZMA_DEBUG_2

0x103C			LZMA debug registers (0x10000000)										LZMA_DEBUG_2			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REM_LEN															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REM_LEN															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

including start and transfer stop bit

Field Name	Bit	Type	Reset Value	Description
REM_LEN	[31:0]	RO	0x0	Debug only, remain length for last decompress

5.15.3.17 LZMA_DEBUG_3

0x1040			LZMA DEBUG registers (0x10000000)										LZMA_DEBUG_3			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PROCPOS															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PROCPOS															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

including start and transfer stop bit

Field Name	Bit	Type	Reset Value	Description
PROCPOS	[31:0]	RO	0x0	Debug only, processed position

5.15.3.18 LZMA_ENDIAN

0x1044			LZMA stop registers (0x10000000)										LZMA_ENDIAN			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVED												ENDIAN_R		ENDIAN_W	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	00		00	

including both read and write endian switch for master

Field Name	Bit	Type	Reset Value	Description
RESERVED	[31: 4]	RO	0x0	reserved
ENDIAN_R	[3:2]	WR	0x10	Endian switch for master read 00:data[31:0] 01:data[7:0], data[15:8], data[23:16], data[31:24] 10: data[15:0], data[31:16] 11: data[23:16], data[31:24], data[7:0], data[15:8]
ENDIAN_W	[1:0]	WR	0x10	Endian switch for master write: 00:data[31:0] 01:data[7:0], data[15:8], data[23:16], data[31:24] 10: data[15:0], data[31:16] 11: data[23:16], data[31:24], data[7:0], data[15:8]

5.15.4 Application Notes

Based on control registers, the decompress module has 3 operation methods:

1. BUFFER_EN set to 0 :

In this type , module won't use buffer ram at all. When started , the compressed data is read from SRC_SADDR, and decode directly to DST_SADDR. The decompress data length is the minimum of UNZIP_SIZE and DST_LENGTH.

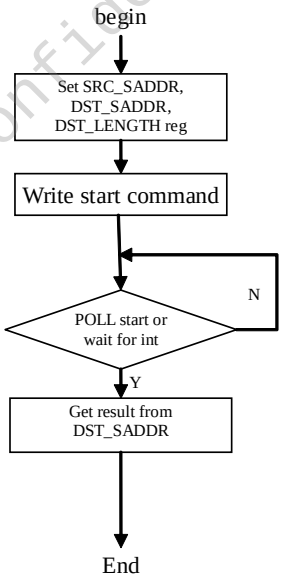


Figure 5-86 Program Flow

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Program Flow: 1. Write configure parameters to 0x0C,10,18.

2. Write 0x10 bit 0 to start computation.
3. Poll register 0x10 bit 0 to determine the computation status. Or just wait the interrupt .
4. Both poll or interrupt finish, should clear 0x04 reg.
5. Read the decompressed data from DST_SADDR. With data size DST_LENGTH.
6. Begin next computation.

2. BUFFER_EN set to 1, BUFFER_FULL_DEC set to 0 :

In this type , module will use buffer ram to decompress data, and then transfer specific length of data to dest address.. When started , the compressed data is read from SRC_SADDR, and decompressed to BUFFER_SADDR. Decompression will finish when decompressed data size meets BUFFER_START_LEN + DST_LENGTH or UNZIP_SIZE (minimum).

Important notice !!!!!!

1. If useful data is from the begging, the BUFFER_START_LEN should be set to 0x1000_0000, not buffer address.

2. Though not all the data will be decompressed , BUFFER_LENGTH should be bigger than BUFFER_START_LEN + DST_LENGTH!!!!!!!! It is recommended BUFFER_LENGTH set to UNZIP_SIZE.

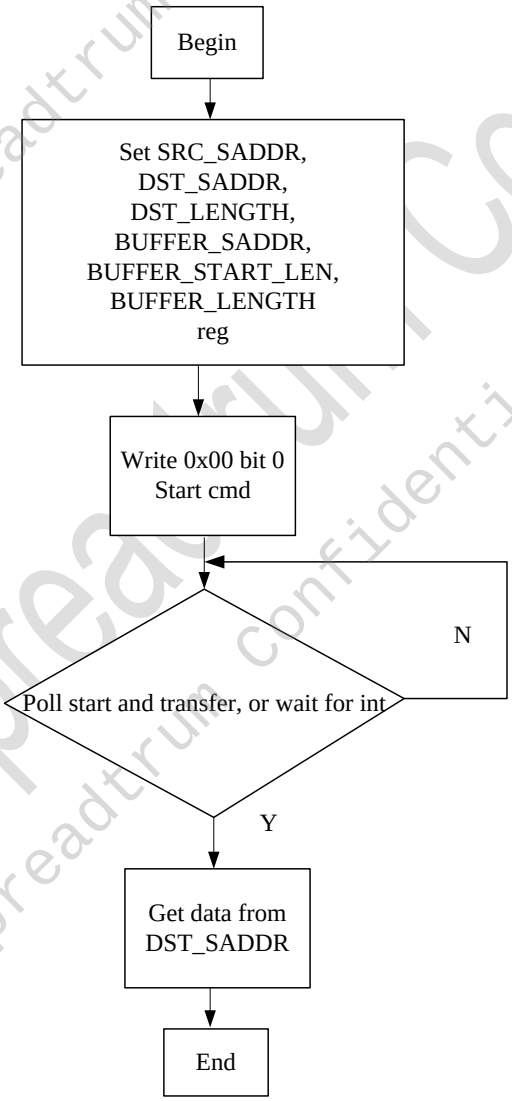


Figure 5-87 Program Flow

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Program Flow: 1. Write configure parameters to 0x0C,10,18.1C,20,24

2. Write 0x10 bit 0 to start computation.
3. Poll register 0x10 both bit 0 and bit 1 to determine the computation status. Or just wait the interrupt . Both START and TRANSFER bit cleared to 0 means finish.
4. Both poll or interrupt finish, should clear 0x04 int reg.
5. Read the decompressed data from DST_SADDR. With data size DST_LENGTH.
6. Begin next computation.

3. BUFFER_EN set to 1, BUFFER_FULL_DEC set to 1 :

In this type , module will use buffer ram to decompress data, and then transfer specific length of data to dest address.. When started , the compressed data is read from SRC_SADDR, and decompressed to BUFFER_SADDR. Decompression will finish when decompressed data size meets BUFFER_ LENGTH or UNZIP_SIZE (minimum).

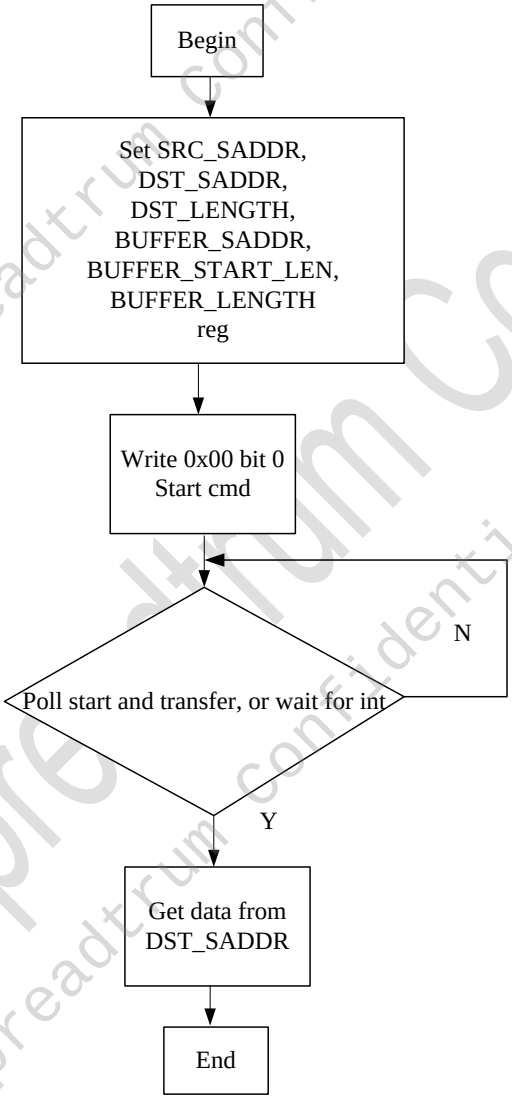


Figure 5-88 Program Flow

Program Flow: 1. Write configure parameters to 0x0C,10,18.1C,20,24

2. Write 0x10 bit 0 to start computation.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

3. Poll register 0x10 both bit 0 and bit 1 to determine the computation status. Or just wait the interrupt . Both START and TRANSFER bit cleared to 0 means finish.
4. Both poll or interrupt finish, should clear 0x04 int reg.
5. Read the decompressed data from DST_SADDR. With data size DST_LENGTH.
6. Begin next computation.

5.16 GEA(EPT) Accelerator (for internal only)

5.16.1 Overview

The GEA module is designed to encrypt and decrypt n blocks of data, under the control of a 64-bit key Kc, 32-bit initialization vector INPUT (also known as message key) and a DIRECTION bit.

Kc, INPUT, and DIRECTION are used to initialize the state of a keystream generator, which is then clocked to generate a sequence of keystream bits. These keystream bits are used to produce (encrypted) ciphertext from plaintext, or produce (decrypted) plaintext from ciphertext, shown in Fig. 1.

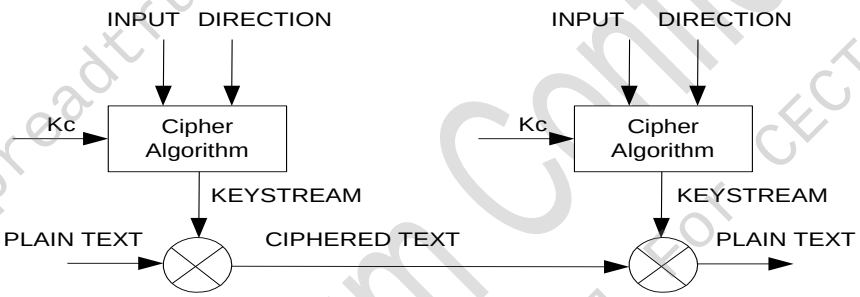


Figure 5-89 Basic GPRS Ciphering Environment

5.16.2 Features

- Support GEA I GEA II GEAIII ,GEAIVand KASUMI algorithm,
- A 4x32 regfile to buffer keystream
- Parameters of direction(1bit), KC(64bits), Input(32bits) and word length should be configurated
- Interrupt sent to ARM after keystream is generated
- APB bus supported

5.16.3 Control Registers

5.16.3.1 Memory map

ARM base address: 0x8D10_0000

Offset Address	Name	Description
0x1000	EPT_START_CMD	EPT control

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description
0x1004		Reserved
0x1008	COUNT	COUNT register
0x100C	FRESH	FRESH register
0x1010	KEY0	KEY0 register
0x1014	KEY1	KEY1 register
0x1018	KEY2	KEY2 register
0x101C	KEY3	KEY3 register
0x1020	POLL_REG	Polling register for EPT status
0x1024	DMA_REG	Dma mode and data switch
0x1028	KASUMI_OUT1	Kasumi /GEA3/4 output 1 register
0x102C	KASUMI_OUT2	Kasumi /GEA3/4 output 2 register
0x1030		Reserved
0x1034	GEA1/GEA2 OUT	GEA1/GEA2 output register

5.16.3.2 Register Descriptions

5.16.3.2.1 EPT_START_CMD

Description: EPT control

0x1000			EPT control(reset 0x0)										EPT_START_CMD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SOFT_RST	Reserved														
Type	R/W	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										START_TYPE	KM_TYPE		EPT_TYPE		
Type	RO										R/W	R/W		R/W		
Reset	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0

Note:

When anytime if SOFT_RST bit is set, EPT module will be soft reset;

When anytime if this register is updated with new written value, EPT module will start calculation again.

If SOFT_RESET bit is set or this register is updated when DMA transfer is not finished, since there is no mechanism for cancel DMA request, so DMA transfer might keep running in this case.

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
SOFT_RST	[31]	R/W	1'h0	Soft reset EPT module
	[30:6]	RO	14'h0	Reserved
START_TYPE	[5]	R/W	1'h0	Set start type when encrypted data length is bigger than memory size(512x32 bits) 0: First Start 1: Second Start
KM_TYPE	[4:3]	R/W	2'h0	KM type for KASUMI mode only: 2'h0:0x0 2'h1:x55555555555555555555555555555555 2'h2:0xaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaa 2'h3:0xffffffffffffffffffffffffffffffff
EPT_TYPE	[2:0]	R/W	3'h0	EPT Algorithm mode 3'h0: KASUMI 3'h3: GEA3 3'h4: GEA4 3'h5: GEA1 3'h6: GEA2 Others: Reserved

5.16.3.2.2 **COUNT**

Description: COUNT register for input parameter configuration

0x1008	**COUNT register(reset 0x0)**															**COUNT**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	COUNT															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	COUNT															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
COUNT	[31:0]	R/W	32'h0	Input parameter for each algorithm with different use: Kasumi: Input M[63:32] GEA1/2: [31:16] Reserved [15] Direction [14:0] Data length(unit is 16-bit) GEA3/4: Message[31:0]

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.16.3.2.3 **FRESH**

Description: FRESH register for input parameter configuration

0x100C			FRESH register(reset 0x0)													FRESH
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	FRESH															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FRESH															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
FRESH	[31:0]	R/W	32'h0	Input parameter for each algorithm with different use: Kasumi: Input M[31:0] GEA1/2: Message[31:0] GEA3/4: [31:1] Reserved [0] Direction

5.16.3.2.4 **KEY0**

Description: Key0 parameter , GEA1、GEA2、GEA3 key are all 64bit ,configured by Key0、Key1, GEA4, KASUMI only mode is 128bit key

0x1010			KEY0 register(reset 0x0)													KEY0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	KEY0															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KEY0															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
KEY0	[31:0]	R/W	32'h0	Input confidentially KEY [31:0] for all algorithm

5.16.3.2.5 **KEY1**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Description: Key1 parameter, GEA1、GEA2、GEA3 key are all 64bit ,configured by Key0、Key1, GEA4 ,KASUMI only mode is 128bit key

0x1014			KEY1 register(reset 0x0)													KEY1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	KEY1															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KEY1															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
KEY1	[31:0]	R/W	32'h0	Input confidentially KEY [63:32] for all algorithm

5.16.3.2.6 **KEY2**

Description: Key2 parameter, GEA1、GEA2、GEA3 key are all 64bit ,configured by Key0、Key1, GEA4 ,KASUMI only mode is 128bit key

0x1018			KEY2 register(reset 0x0)													KEY2
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	KEY2															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KEY2															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
KEY2	[31:0]	R/W	32'h0	Input confidentially KEY [95:64] for Kasumi

5.16.3.2.7 **KEY3**

Description: Key3 parameter, GEA1、GEA2、GEA3 key are all 64bit ,configured by Key0、Key1, GEA4, KASUMI only mode is 128bit key

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x101c			KEY3 register(reset 0x0)													KEY3
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	KEY3															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KEY3															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
KEY3	[31:0]	R/W	32'h0	Input confidentially KEY [127:96] for Kasumi

5.16.3.2.8 **POLL_REG**

Description: Polling register for EPT status

0x1020			Polling register for EPT status (reset 0x0)													POLL_REG
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved							GEA2_RUNNING	GEA1_RUNNING			GEA3/4_RUNNING	KASUMI_RUNNING			
Type	RO							RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved													GEA_DONE		EPT_DONE
Type	RO													R/W	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:25]	RO	7'h0	Reserved
GEA2_RUNNING	[24]	RO	1'h0	Indicating current status is GEA2 running, active high
GEA1_RUNNING	[23]	RO	1'h0	Indicating current status is GEA1 running, active high
	[22:21]	RO	1'b0	Reserved
GEA3_RUNNING	[20]	RO	1'h0	Indicating current status is GEA3/4 running, active high
KASUMI_RUNNING	[19]	RO	1'h0	Indicating current status is KASUMI mode running, active high

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[18:3]	RO	13'h0	Reserved
GEA_DONE	[2]	R/W	1'h0	Indicating GEA1/2 calculation is done, active high. SW is responsible for clear this bit after read out.
	[1]	RO	1'b0	Reserved
EPT_DONE	[0]	R/W	1'h0	Indicating Kasumi/GEA3/4 calculation is done, active high. SW is responsible for clear this bit after read out.

5.16.3.2.9 **DMA_REG**

Description: DMA mode control reg

0x1024	**DMA mode control register(reset 0x0)**															**DMA_REG**
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															DATA_SWITCH2
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DATA_SWITCH2		DMA_MODE	RUN_NUM										DATA_SWITCH		
Type			RW	RW										R/W		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:14]	RO	18'h0	Reserved
DATA_SWITCH2	[16:14]	RW	3'b0	For DMA mode, 3'b000: 0040: DMA_MEM[31:0] 0044:DMA_MEM[63:32] 0048: DMA_MEM[95:64] 004C: DMA_MEM[127:96] 3'b001: 0040: {[7:0],[15:8],[23:16],[31:24]} 0044: {[39:32],[47:40],[55:48],[63:56]} 0048 {[71:64]:[79:72]:[87:80],[95:88]} 004C:{[103:96],[111:104],[119:112],[127:120]} 3'b010: 0040: {[15:0],[31:16]} 0044: {[47:32],[63:48]} 0048 {[79:64]:[95:80]} 004C:{[111:96],[127:112]} 3'b011:0040: {[23:16],[31:24],[7:0],[15:8]} 0044: {[55:48],[63:56],[39:32],[47:40]} 0048: {[87:80],[95:88],[71:64],[79:72]} 004C: {[119:112],[127:120],[103:96],[111:104]}

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				3'b100: 0040: [63:32] 0044: [31:0] 0048: [127:96] 004C: [95:64] 3'b101: 0040: {[39:32],[47:40],[55:48],[63:56]} 0044: {[7:0],[15:8],[23:16],[31:24]} 0048 {[103:96],[111:104],[119:112],[127:120]} 004C:{[71:64]:[79:72]:[87:80],[95:88]} 3'b110: 0040: {[47:32],[63:48]} 0044: {[15:0],[31:16]} 0048: {[111:96],[127:112]} 004C: {[79:64]:[95:80]}
DMA_MODE	[13]	RW	1'h0	1:DMA mode enable 2:DMA mode disable
RUN_NUM	[12:3]	RW	10'h0	Indicating the run number of next dma transfer
DATA_SWITCH	[2:0]	RW	3'b0	For none DMA mode 3'b000: 0028: KASUMI_REG3_OUT[31:0] 002C: KASUMI_REG3_OUT[63:32] 3'b001: 0028: {[7:0],[15:8],[23:16],[31:24]} 002C:{[39:32],[47:40],[55:48],[63:56]} 3'b010: 0028: {[15:0],[31:16]} 002C:{[47:32],[[63:48]} 3'b100: 0028: {[63:32]} 002C:{[31:0]} 3'b101: 0028:{[39:32],[47:40],[55:48],[63:56]} 002C:{[7:0],[15:8],[23:16],[31:24]} 3'b110: 0028:{[47:32],[[63:48]} 002C: {[15:0],[31:16]}

5.16.3.2.10 **KASUMI_GEA3/4_OUT1**

Description: KASUMI /GEA3/4 output 1

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1028			KASUMI/GEA3/4 output 1(reset 0x0)										KASUMI_GEA3/4_OUT1			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	KASUMI_GEA3/4_OUT1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KASUMI_GEA3/4_OUT1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
KASUMI_GEA3/4_OUT1	[31:0]	RO	32'h0	Kasumi/GEA3/4 output [31:0]

5.16.3.2.11 **KASUMI_GEA3/4_OUT2**

Description: KASUMI/GEA3/4 output 2

0x102c			KASUMI/GEA3/4 output 2(reset 0x0)										KASUMI_GEA3/4_OUT2			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	KASUMI_GEA3/4_OUT2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KASUMI_GEA3/4_OUT2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
KASUMI_GEA2_OUT2	[31:0]	RO	32'h0	Kasumi /GEA3/4: output [63:32]

5.16.3.2.12 **GEA1/GEA2 Result**

Description: GEA1/GEA2 Result register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1034			GEA1/GEA2 output (reset 0x0)										GEA1_GEA2_OUT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	GEA1_GEA2_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GEA1_GEA2_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:0]	RO	0	GEA1/GEA2 output

5.16.3.2.13 **DMA_MEM1**

Description: DMA mode memory 1 [31:0]

0x1040			DMA_MEM1 (reset 0x0)										DMA_MEM1			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DMA_MEM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DMA_MEM1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
DMA_MEM1	[31:0]	RO	0	DMA memory [31:0]

5.16.3.2.14 **DMA_MEM2**

Description: DMA mode memory 2 [63:32]

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x1044			DMA_MEM2 (reset 0x0)													DMA_MEM2
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DMA_MEM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DMA_MEM2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
DMA_MEM2	[31:0]	RO	0	DMA memory [63:32]

5.16.3.2.15 **DMA_MEM3**

Description: DMA mode memory 3 [95:64]

0x1048			DMA_MEM3 (reset 0x0)													DMA_MEM3
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DMA_MEM3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DMA_MEM3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
DMA_MEM3	[31:0]	RO	0	DMA memory [95:64]

5.16.3.2.16 **DMA_MEM4**

Description: DMA mode memory 4 [127:96]

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x104C			DMA_MEM4 (reset 0x0)													DMA_MEM4
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DMA_MEM4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DMA_MEM4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
DMA_MEM4	[31:0]	RO	0	DMA memory [127:96]

5.16.4 Application Notes

The configuration interface between Link layer software and ASIC is through ARM 16-bit APB bus. GEA1,2 and GEA3/4,KASUMI share different algorithm core. Also they have different process cycle.However all algorithms have the same process flow. The parameter registers should be configured. Once the start command is issued, the result can be read from result register with EPT IRQ generated.

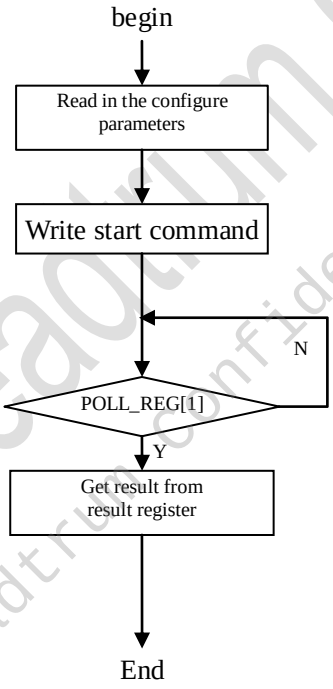


Figure 5-90 Program Flow

Program Flow: 1. Write configure parameters to 0x08,0C,10,14,18,1C.

2. Write 0x10 to start computation.
3. Poll register 0x20 to determine the computation status. Or just wait the interrupt EPT IRQ.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

4. When 0x20 bit 0 (GEA3/4/KASUMI) or bit 2(GEA1/2) turned to 1, it indicates that the computation finished
5. Read the keystream out from registers 0x28, 0x2C(GEA3/4/KASUMI), 0x34(GEA1/GEA2)
6. Clear register 0x20, bit 0(GEA3/4/KASUMI) or bit 2(GEA1/2) by write 1 to them.
7. Begin next computation.

5.17 GPIO

5.17.1 Overview

The GPIO module provides more then 100 GPIO pins of MCU. However, many of the pins are multiplexed with other functions and system design trade-off must be exercised on selecting them. All the GPIO pins can be programmed to be either input or output. When in input mode, they can be programmed to trigger interrupt to the MCU.

5.17.2 Features

- positive edge detect and interrupt generate
- negative edge detect and interrupt generate
- both edges detect and interrupt generate
- high level detect and interrupt generate
- low level detect and interrupt generate
- interrupt mask
- interrupt clear
- input data sample or mask
- output data or mask
- level interrupt generate at system power down
- level detect conditions changeable
- different interrupts happen
- edge detect conditions changeable

Spreadtrum Confidential
Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.17.3 Function Description

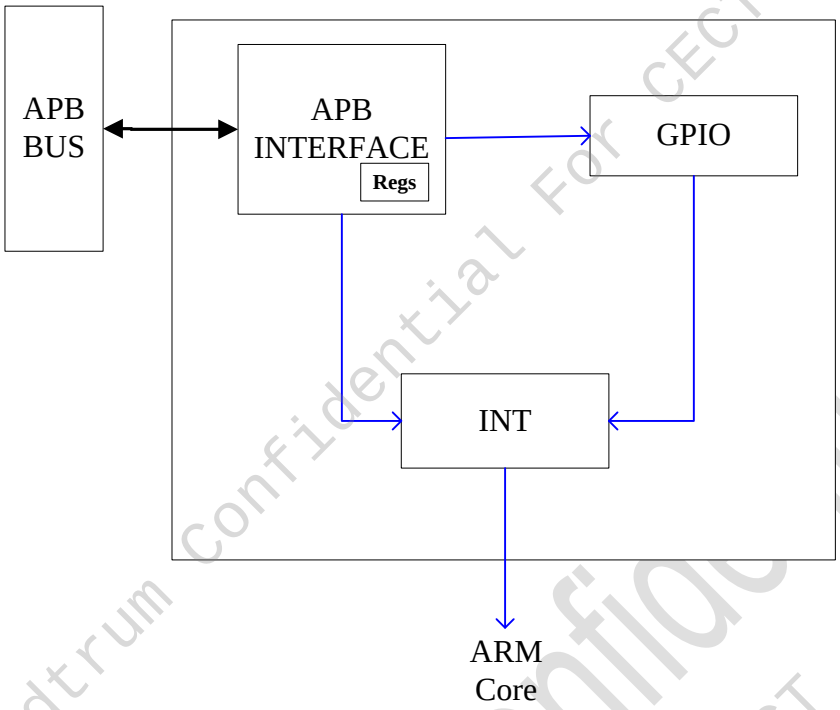


Figure 5-91 GPIO block diagram

As the above diagram shows, SW communicates with GPIO module by APB BUS. When the module has received active input signals, interrupts will be created to notify ARM core.

5.17.4 Control Registers

5.17.4.1 Memory map

Table 1 GPIO Control Register Address Map

ARM base address:
For GPIO0~GPIO127:
0x8A00_0000, 0x8A00_0080, 0x8A00_0100, 0x8A00_0180,
0x8A00_0200, 0x8A00_0280, 0x8A00_0300, 0x8A00_0380,

For GPIO128~GPIO131:
0x8200_1780, 0x8200_17C0

Offset Address	Name	Description
0x0000	GPIODATA	GPIO bits data
0x0004	GPIODMSK	GPIO bits data mask
0x0008	GPIODIR	GPIO bits data direction
0x000C	GPIOIS	GPIO bits interrupt sense
0x0010	GPIOIBE	GPIO bits both edges interrupt

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description
0x0014	GPIOIEV	GPIO bits interrupt event
0x0018	GPIOIE	GPIO bits interrupt enable
0x001C	GPIORIS	GPIO bits raw interrupt status
0x0020	GPIOMIS	GPIO bits masked interrupt status
0x0024	GPIOIC	GPIO bits interrupt clear
0x0028	GPIOINEN	GPIO input enable

5.17.4.2 Register Descriptions

5.17.4.2.1 GPIODATA

Description：GPIO bits data register

0x0000			(reset 0x0000_0000)													GPIOATA
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIODATA															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	R/W	16'h0	Reserved
GPIODATA	[15:0]	R/W	16'h0	GPIO bits data

5.17.4.2.2 GPIODMSK

Description：GPIO bits mask register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0004			(reset 0x0000_0000)													GPIODMSK
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIODMSK															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIODMSK	[15:0]	R/W	16'h0	GPIODATA register can be read/write if GPIO DMSK set "1"

5.17.4.2.3 **GPIODIR**

Description：GPIO bits direction register

0x0008			(reset 0x0000_0000)													GPIODIR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIODIR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

GPIODIR	[15:0]	R/W	16'h0	"1" configure gpio bits to be output "0" configure gpio bits to be input

5.17.4.2.4 **GPIOIS**

Description：GPIO bits interrupt sense register

0x000C			(reset 0x0000_FFFF)													GPIOIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIS															
Type	R/W															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOIS	[15:0]	R/W	16'hFFFF	"1" detect signals level "0" detect signals edge

5.17.4.2.5 **GPIOIBE**

Description：GPIO bits both edges interrupt register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0010			(reset 0x0000_0000)													GPIOIBE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIBE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOIBE	[15:0]	R/W	16'h0	"1" both edges trigger an interrupt, "0" interrupt generation event is controlled by GPIOIEV

5.17.4.2.6 **GPIOIEV**

Description： GPIO bits interrupt status register

0x0014			(reset 0x0000_FFFF)													GPIOIEV
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIEV															
Type	R/W															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[31:16]	RO	16'h0	Reserved
GPIOIEV	[15:0]	R/W	16'hFFFF	GPIO bits interrupt event register: "1" high levels trigger interrupts, "0" low levels trigger interrupts.

5.17.4.2.7 **GPIOIE**

Description： GPIO bits interrupt enable register

0x0018			**(reset 0x0000_0000)**													GPIOIE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	**Bit**	**Type**	**Reset Value**	**Description**
	[31:16]	RO	16'h0	Reserved
GPIOIE	[15:0]	R/W	16'h0	GPIO bits interrupt enable register: "1" corresponding bit interrupt is enabled. "0" corresponding bit interrupt isn't enabled

5.17.4.2.8 **GPIORIS**

Description： GPIO bits raw interrupt status register, and it reflects the status of interrupts trigger conditions detection on pins (prior to GPIOMIS)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x001C			(reset 0x0000_0000)													GPIORIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIORIS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIORIS	[15:0]	RO	16'h0	GPIO bits raw interrupt status register: "1" interrupt condition met "0" condition not met

5.17.4.2.9 **GPIOMIS**

Description： GPIO bits masked interrupt status register

0x0020			(reset 0x0000_0000)													GPIOMIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOMIS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
	[31:16]	RO	16'h0	Reserved
GPIOMIS	[15:0]	RO	16'h0	GPIO bits masked interrupt status register: "1" Interrupt active "0" interrupt not active

5.17.4.2.10 **GPIOIC**

Description： GPIO bits interrupt clear register

0x0024			(reset 0x0000_0000)													GPIOIC
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIC															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOIC	[15:0]	WO	16'h0	GPIO bits interrupt clear register: "1" clears detected interrupt. "0" has no effect.

5.17.4.2.11 **GPIOINEN**

Description： GPIO input enable register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0028			(reset 0x0000_FFFF)													GPIOINEN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOINEN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOINEN	[15:0]	RW	16'h0	GPIO input enable register: "1" input enable. "0" input disable.

5.17.5 Application Notes

5.17.5.1 Programming Notes

1) GPIOMIS is equal to GPIOIE & GPIORIS.

5.18 EIC

5.18.1 Overview

The EIC module includes four sub-modules: EIC_DBNC, EIC_LATCH, EIC_ASYNC and EIC_SYNC.

The EIC_DBNC sub-module provides up to 8 source input signal connection. A de-bounce mechanism is used to capture input signal's stable status and a single-trig mechanism is introduced into this sub-module to enhance the input event detect reliability. In addition, this sub-module's clock can be shut off automatically to reduce power dissipation. The de-bounce range is from 1 ms to 4 s with the step of 1 ms. The input signals shorter than 1 ms will be omitted at this sub-module.

THE EIC_LATCH sub-module is used to latch some special input signal and send interrupts to MCU core by channel 0, and it can provides up to 8 EIC_LATCH source input signal connection.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.18.2 Features

5.18.2.1 EIC_DBNC

- high level detect and interrupt generate(not bypass mode)
- low level detect and interrupt generate(not bypass mode)
- interrupt mask(not bypass mode)
- interrupt clear(not bypass mode)
- level interrupt generate at system power down with once active trig(not bypass mode)
- keep interrupt stable when no interrupt clear(not bypass mode)
- input data sample or mask(not bypass mode)
- de-bounce number configurable(not bypass mode)
- only once trig active(not bypass mode)
- trig level condition configurable(not bypass mode)
- high level detect and interrupt generate(bypass mode)
- low level detect and interrupt generate(bypass mode)
- interrupt mask(bypass mode)
- interrupt clear(bypass mode)
- input data sample or mask(bypass mode)
- level interrupt generate at system power down(bypass mode)
- force to open the clock of de-bounce

5.18.2.2 EIC_LATCH

- Special IRQ or FIQ interrupt on channel 0 is used to latch some input signal status and trigger IRQ or FIQ interrupt by level detecting (no edge detecting)
- Special IRQ or FIQ interrupt on channel 0 is multiplexed from 8 independent input sources
- Using Latch circuit to realize interrupt generation, INTMSK connected to the set port of Latch, and INTCLR connected to the clear port of Latch.
- Provide raw status for each of 8 input sources on special channel
- Provide polarity control bit for each of 8 input sources on special channel
- Provide only one clear bit to clear all latches on special channel
- Each input source can be enabled or disabled independently on special channel

5.18.2.3 EIC_ASYNC

- positive edge detect and interrupt generate
- negative edge detect and interrupt generate
- both edges detect and interrupt generate
- high level detect and interrupt generate
- low level detect and interrupt generate
- interrupt mask
- interrupt clear
- input data sample or mask
- level interrupt generate at system power down
- level detect conditions changeable
- edge detect conditions changeable

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.18.2.4 EIC_SYNC

- Input signal synced with clk_apb
- positive edge detect and interrupt generate
- negative edge detect and interrupt generate
- both edges detect and interrupt generate
- high level detect and interrupt generate
- low level detect and interrupt generate
- interrupt mask
- interrupt clear
- input data sample or mask
- level interrupt generate at system power down
- level detect conditions changeable
- edge detect conditions changeable

5.18.3 Funtion description

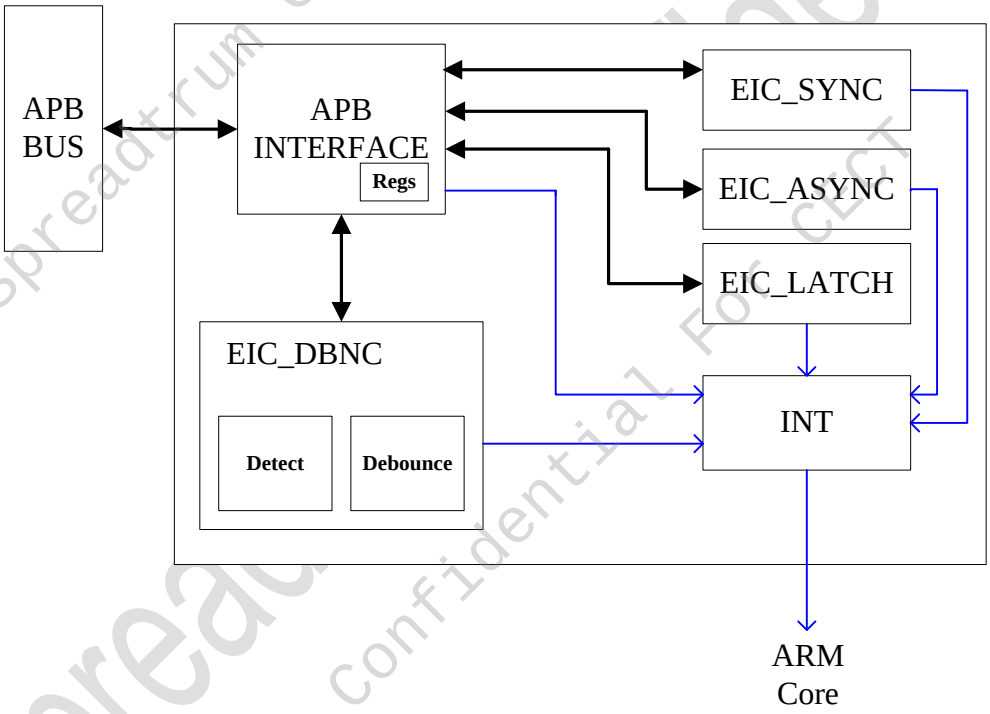


Figure 5-92 EIC block diagram

As the above diagram shows, SW communicates with EIC module by APB BUS. When the module has received active input signals, interrupts will be created to notify ARM core.

5.18.4 Control registers

5.18.4.1 Memory map

Table 2 EIC_DBNC Control Register Address Map

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

ARM base address: 0x8A00_1000 (EIC_DBNC) (EIC0-EIC15)
0x8200_1900 (EIC_DBNCA) (EIC16-EIC31)

Offset Address	Name	Description
0x0000	EIC_DBNC_DATA	EIC_DBNC bits data input
0x0004	EIC_DBNC_DMSK	EIC_DBNC bits data mask
0x0014	EIC_DBNC_IEV	EIC_DBNC bits interrupt event
0x0018	EIC_DBNC_IE	EIC_DBNC bits interrupt enable
0x001C	EIC_DBNC_RIS	EIC_DBNC bits raw interrupt status
0x0020	EIC_DBNC_MIS	EIC_DBNC bits masked interrupt status
0x0024	EIC_DBNC_IC	EIC_DBNC bits interrupt clear
0x0028	EIC_DBNC_TRIG	EIC_DBNC bits trig control
0x0040	EIC0_DBNC_CTRL	EIC0_DBNC control register
0x0044	EIC1_DBNC_CTRL	EIC1_DBNC control register
0x0048	EIC2_DBNC_CTRL	EIC2_DBNC control register
0x004C	EIC3_DBNC_CTRL	EIC3_DBNC control register
0x0050	EIC4_DBNC_CTRL	EIC4_DBNC control register
0x0054	EIC5_DBNC_CTRL	EIC5_DBNC control register
0x0058	EIC6_DBNC_CTRL	EIC6_DBNC control register
0x005C	EIC7_DBNC_CTRL	EIC7_DBNC control register

EIC0-1: come from external pad;
EIC2-15: reserved;
EIC16: from TP_XL;
EIC17: PBINT2;
EIC18: CHGR_INT;
EIC19: PBINT;
EIC20: HEAD_BUTTON;
EIC21: HEADMIC_DETECTION;
EIC22: CHGR_OVI;
EIC23-31: reserved;

Table 3 EIC_LATCH Control Register Address Map

ARM base address: 0x8A00_1080

Offset Address	Name	Description
0x0000	EIC_LATCH_INTEN	EIC_LATCH interrupt enable

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description
0x0004	EIC_LATCH_INTRAW	EIC_LATCH raw interrupt
0x0008	EIC_LATCH_INTMSK	EIC_LATCH interrupt mask
0x000C	EIC_LATCH_INTCLR	EIC_LATCH interrupt clear
0x0010	EIC_LATCH_INTPOL	EIC_LATCH interrupt polarity
0x0014	EIC_LATCH_INTMODE	EIC_LATCH interrupt mode

Table 4 EIC_ASYNC Control Register Address Map

ARM base address: 0x8A00_10A0

Offset Address	Name	Description
0x0000	EIC_ASYNC_INTEN	EIC_ASYNC interrupt enable
0x0004	EIC_ASYNC_INTRAW	EIC_ASYNC raw interrupt
0x0008	EIC_ASYNC_INTMSK	EIC_ASYNC interrupt mask
0x000C	EIC_ASYNC_INTCLR	EIC_ASYNC interrupt clear
0x0010	EIC_ASYNC_INTMODE	EIC_ASYNC interrupt edge or level mode setting
0x0014	EIC_ASYNC_INTBOTH	EIC_ASYNC interrupt both edge setting
0x0018	EIC_ASYNC_INTPOL	EIC_ASYNC interrupt polarity
0x001C	EIC_ASYNC_INTDATA	EIC_ASYNC input data

Table 5 EIC_SYNC Control Register Address Map

ARM base address: 0x8A00_10C0

Offset Address	Name	Description
0x0000	EIC_SYNC_INTEN	EIC_SYNC interrupt enable
0x0004	EIC_SYNC_INTRAW	EIC_SYNC raw interrupt
0x0008	EIC_SYNC_INTMSK	EIC_SYNC interrupt mask
0x000C	EIC_SYNC_INTCLR	EIC_SYNC interrupt clear
0x0010	EIC_SYNC_INTMODE	EIC_SYNC interrupt edge or level mode setting
0x0014	EIC_SYNC_INTBOTH	EIC_SYNC interrupt both edge setting
0x0018	EIC_SYNC_INTPOL	EIC_SYNC interrupt polarity
0x001C	EIC_SYNC_INTDATA	EIC_SYNC input data

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

5.18.4.2 Register description

5.18.4.2.1 EIC_DBNC_DATA

Description： EIC_DBNC bits data register, read only

0x0000			(reset 0x0000_0000)													EIC_DBNC_DATA
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_DATA							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_DBNC_DATA	[7:0]	RO	8'h0	EIC_DBNC bits data input

Note: EIC_DBNC_DATA synchronizes the original data inputs with 2 cycles of Rtcdiv5_clk, so SW need delay 2ms to get the exact value of original data inputs when Rtcdiv5_clk is enabled.

5.18.4.2.2 EIC_DBNC_DMSK

Description： EIC_DBNC bits data mask register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0004			(reset 0x0000_0000)													EIC_DBNC_DMSK
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_DMSK							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_DBNC_DMSK	[7:0]	R/W	8'h0	EIC_DBNC_DATA register can be read if EIC_DBNC_DMSK set "1"

5.18.4.2.3 **EIC_DBNC_IEV**

Description： EIC_DBNC bits interrupt status register

0x0014			(reset 0x0000_00FF)													EIC_DBNC_IEV
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_IEV							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

EIC_DBNC-IEV	[7:0]	R/W	8'hFF	EIC_DBNC bits interrupt status register: "1" high levels trigger interrupts, "0" low levels trigger interrupts.

5.18.4.2.4 **EIC_DBNC_IE**

Description： EIC_DBNC bits interrupt enable register

0x0018			(reset 0x0000_0000)										EIC_DBNC_IE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_IE							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_DBNC_IE	[7:0]	R/W	8'h0	EIC_DBNC bits interrupt enable register: "1" corresponding bit interrupt is enabled. "0" corresponding bit interrupt isn't enabled

5.18.4.2.5 **EIC_DBNC_RIS**

Description： EIC_DBNC bits raw interrupt status register, and it reflects the status of interrupts trigger conditions detection on pins (prior to EIC_DBNC_MIS)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x001C			(reset 0x0000_0000)													EIC_DBNC_RIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_RIS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_DBNC_RIS	[7:0]	RO	8'h0	EIC bits raw interrupt status register: "1" interrupt condition met "0" condition not met

5.18.4.2.6 **EIC_DBNC_MIS**

Description： EIC_DBNC bits masked interrupt status register

0x0020			(reset 0x0000_0000)													EIC_DBNC_MIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_MIS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: EIC_DBNC_MIS = EIC_DBNC_IE & EIC_DBNC_RIS

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_DBNC_MIS	[7:0]	RO	8'h0	EIC_DBNC bits masked interrupt status register: "1" Interrupt active "0" interrupt not active

5.18.4.2.7 **EIC_DBNC_IC**

Description： EIC_DBNC_ bits interrupt clear register

0x0024	(reset 0x0000_0000)												EIC_DBNC_IC			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_IC							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	WO	24'h0	Reserved
EIC_DBNC_IC	[7:0]	WO	8'h0	EIC_DBNC bits interrupt clear register: "1" clears detected interrupt. "0" has no effect.

5.18.4.2.8 **EIC_DBNC_TRIG**

Description： EIC_DBNC bits trig control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0028			(reset 0x0000_0000)													EIC_DBNC_TRIG
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_TRIG							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	WO	24'h0	Reserved
EIC_DBNC_TRIG	[7:0]	WO	8'h0	EIC_DBNC bits trig control register: "1": generate the trig_start pulse "0": no effect It must set EIC_DBNC_TRIG for using de-bounce function and getting active interrupt.

5.18.4.2.9 **EIC0_DBNC_CTRL**

Description： EIC0_DBNC control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0040			(reset 0x0000_4032)												EIC0_DBNC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

5.18.4.2.10 **EIC1_DBNC_CTRL**

Description： EIC1_DBNC control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0042			(reset 0x0000_4032)												EIC1_DBNC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

5.18.4.2.11 **EIC2_DBNC_CTRL**

Description： EIC2_DBNC control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0048			(reset 0x0000_4032)												EIC2_DBNC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

5.18.4.2.12 **EIC3_DBNC_CTRL**

Description： EIC3 control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x004C			(reset 0x0000_4032)												EIC3_DBNC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

5.18.4.2.13 **EIC4_DBNC_CTRL**

Description： EIC4_DBNC control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0050			(reset 0x0000_4032)												EIC4_DBNC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

5.18.4.2.14 **EIC5_DBNC_CTRL**

Description： EIC5_DBNC control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0054			(reset 0x0000_4032)												EIC5_DBNC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

5.18.4.2.15 **EIC6_DBNC_CTRL**

Description： EIC6_DBNC control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0058			(reset 0x0000_4032)												EIC6_DBNC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

5.18.4.2.16 **EIC7_DBNC_CTRL**

Description： EIC7 control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x005C			(reset 0x0000_4032)													EIC7_DBNC_CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

5.18.4.2.17 **EIC_LATCH_INTEN**

Description：EIC_LATCH interrupt enable register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0000			(reset 0x0000_0000)												EIC_LATCH_INTEN	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_LATCH_INTEN							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_LATCH_INTEN	[7:0]	RW	8'h0	EIC_LATCH interrupt enable register: "1": enable bit interrupt "0": disable bit interrupt

5.18.4.2.18 **EIC_LATCH_INTRAW**

Description：EIC_LATCH raw interrupt register

0x0004			(reset 0x0000_0000)												EIC_LATCH_INTRAW	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_LATCH_INTRAW							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[31:8]	RO	24'h0	Reserved
EIC_LATCH_INTRAW	[7:0]	RW	8'h0	EIC_LATCH raw interrupt status register: "1" interrupt condition met "0" condition not met

5.18.4.2.19 **EIC_LATCH_INTMSK**

Description：EIC_LATCH interrupt mask register

0x0008			**(reset 0x0000_0000)**										EIC_LATCH_INTMSK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_LATCH_INTMSK							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	**Bit**	**Type**	**Reset Value**	**Description**
	[31:8]	RO	24'h0	Reserved
EIC_LATCH_INTMSK	[7:0]	RO	8'h0	EIC_LATCH interrupt mask register "1" Interrupt active "0" interrupt not active

Note: EIC_LATCH_INTMSK = EIC_LATCH_INTEN & EIC_LATCH_INTRAW, and EIC_LATCH_INTMSK are connected to the set port of Latch

5.18.4.2.20 **EIC_LATCH_INTCLR**

Description：EIC_LATCH interrupt clear register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x000C			(reset 0x0000_0000)										EIC_LATCH_INTCLR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_LATCH_INTCLR							
Type	RO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_LATCH_INTCLR	[7:0]	WO	8'h0	EIC_LATCH interrupt clear register: "1" clears detected interrupt. "0" has no effect.

Note: EIC_LATCH_INTCLR are connected to the "clear" port of Latch, and it need disable the "set" port of Latch by changing EIC_LATCH_INTPOL to clear EIC_LATCH interrupt.

5.18.4.2.21 **EIC_LATCH_INTPOL**

Description：EIC_LATCH interrupt polarity register

0x0010			(reset 0x0000_0000)										EIC_LATCH_INTPOL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_LATCH_INTPOL							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_LATCH_INTPOL	[7:0]	RW	8'h0	EIC_LATCH polarity register: "0": high levels trigger interrupts, "1": low levels trigger interrupts.

5.18.4.2.22 **EIC_LATCH_INTMODE**

Description： EIC_LATCH interrupt mode register

0x0014			(reset 0x0000_0000)										EIC_LATCH_INTMODE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_LATCH_INTMODE							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_LATCH_INTMODE	[7:0]	RW	8'h0	EIC_LATCH interrupt mode register: "1": interrupt active without chip sleep "0": interrupt active with chip sleep

5.18.4.2.23 **EIC_ASYNC_INTIE**

Description： EIC_ASYNC bits interrupt enable register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0000			(reset 0x0000_0000)													EIC_ASYNC_INTIE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_INTIE							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_ASYNC_IE	[7:0]	R/W	8'h0	EIC_ASYNC bits interrupt enable register: "1" corresponding bit interrupt is enabled. "0" corresponding bit interrupt isn't enabled

5.18.4.2.24 **EIC_ASYNC_INTRAW**

Description：EIC_ASYNC raw interrupt register

0x0004			(reset 0x0000_0000)													EIC_ASYNC_INTRAW
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_INTRAW							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_ASYNC_INTRAW	[7:0]	RW	8'h0	EIC_ASYNC raw interrupt status register: "1" interrupt condition met "0" condition not met

5.18.4.2.25 **EIC_ASYNC_INTMSK**

Description：EIC_ASYNC interrupt mask register

0x0008			(reset 0x0000_0000)										EIC_ASYNC_INTMSK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_INTMSK							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_ASYNC_INTMSK	[7:0]	RO	8'h0	EIC_ASYNC interrupt mask register "1" Interrupt active "0" interrupt not active

5.18.4.2.26 **EIC_ASYNC_INTCLR**

Description：EIC_ASYNC interrupt clear register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x000C			(reset 0x0000_0000)										EIC_ASYNC_INTCLR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_INTCLR							
Type	RO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_ASYNC_INTCLR	[7:0]	WO	8'h0	EIC_ASYNC interrupt clear register: "1" clears detected interrupt. "0" has no effect.

5.18.4.2.27 **EIC_ASYNC_INTMODE**

Description：EIC_ASYNC bits interrupt mode register

0x0010			(reset 0x0000_FFFF)										EIC_ASYNC_INTMODE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_INTCLR							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
	[31:8]	RO	24'h0	Reserved
EIC_ASYNC_INTMODE	[7:0]	R/W	8'hFFFF	"1" detect signals level "0" detect signals edge

5.18.4.2.28 **EIC_ASYNC_INTBOTH**

Description：EIC_ASYNC bits both edges interrupt register

0x0014	(reset 0x0000_0000)												EIC_ASYNC_INTBOTH			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_INTBOTH							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	16'h0	Reserved
EIC_ASYNC_INTBOTH	[7:0]	R/W	16'h0	"1" both edges trigger an interrupt, "0" interrupt generation event is controlled by EIC_ASYNC_INTMODE

5.18.4.2.29 **EIC_ASYNC_INTPOL**

Description：EIC_ASYNC interrupt polarity register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0018			(reset 0x0000_0000)													EIC_ASYNC_INTPOL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_INTPOL							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_ASYNC_INTPOL	[7:0]	RW	8'h0	EIC_ASYNC polarity register: "1": high levels or pos-edge trigger interrupts, "0": low levels or neg-edge trigger interrupts.

5.18.4.2.30 **EIC_ASYNC_DATA**

Description： EIC_ASYNC bits data register, read only

0x001C			(reset 0x0000_0000)													EIC_ASYNC_DATA
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_DATA							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_ASYNC_DATA	[7:0]	RO	8'h0	EIC_ASYNC bits data input

5.18.4.2.31 **EIC_SYNC_INTIE**

Description： EIC_SYNC bits interrupt enable register

0x0000	(reset 0x0000_0000)														EIC_SYNC_INTIE	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_INTIE							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_SYNC_IE	[7:0]	R/W	8'h0	EIC_SYNC bits interrupt enable register: "1" corresponding bit interrupt is enabled. "0" corresponding bit interrupt isn't enabled

5.18.4.2.32 **EIC_SYNC_INTRAW**

Description：EIC_SYNC raw interrupt register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0004			(reset 0x0000_0000)										EIC_SYNC_INTRAW			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_INTRAW							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_SYNC_INTRAW	[7:0]	RW	8'h0	EIC_SYNC raw interrupt status register: "1" interrupt condition met "0" condition not met

5.18.4.2.33 **EIC_SYNC_INTMSK**

Description：EIC_SYNC interrupt mask register

0x0008			(reset 0x0000_0000)										EIC_SYNC_INTMSK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_INTMSK							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
	[31:8]	RO	24'h0	Reserved
EIC_SYNC_INTMSK	[7:0]	RO	8'h0	EIC_SYNC interrupt mask register "1" Interrupt active "0" interrupt not active

5.18.4.2.34 **EIC_SYNC_INTCLR**

Description：EIC_SYNC interrupt clear register

0x000C			(reset 0x0000_0000)											EIC_SYNC_INTCLR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_INTCLR							
Type	RO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_SYNC_INTCLR	[7:0]	WO	8'h0	EIC_SYNC interrupt clear register: "1" clears detected interrupt. "0" has no effect.

5.18.4.2.35 **EIC_SYNC_INTMODE**

Description：EIC_SYNC bits interrupt mode register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0010			(reset 0x0000_FFFF)												EIC_SYNC_INTMODE	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_INTCLR							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_SYNC_INTMODE	[7:0]	R/W	8'hFFFF	"1" detect signals level "0" detect signals edge

5.18.4.2.36 **EIC_SYNC_INTBOTH**

Description：EIC_SYNC bits both edges interrupt register

0x0014			(reset 0x0000_0000)												EIC_SYNC_INTBOTH	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_INTBOTH							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[31:8]	RO	16'h0	Reserved
EIC_SYNC_INTBOTH	[7:0]	R/W	16'h0	"1" both edges trigger an interrupt, "0" interrupt generation event is controlled by EIC_SYNC_INTMODE

5.18.4.2.37 **EIC_SYNC_INTPOL**

Description：EIC_SYNC interrupt polarity register

0x0018	(reset 0x0000_0000)												EIC_SYNC_INTPOL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_INTPOL							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_SYNC_INTPOL	[7:0]	RW	8'h0	EIC_SYNC polarity register: "1": high levels or pos-edge trigger interrupts, "0": low levels or neg-edge trigger interrupts.

5.18.4.2.38 **EIC_SYNC_DATA**

Description： EIC_SYNC bits data register, read only

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x001C			(reset 0x0000_0000)										EIC_SYNC_DATA			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_DATA							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_SYNC_DATA	[7:0]	RO	8'h0	EIC_SYNC bits data input

5.18.5 Application notes

5.18.5.1 Programming Model

For EIC_DBNC sub-module, software needs to adopt corresponding steps as follows:

1) When system resets, EIC_DBNC module is also under the reset status and cannot capture the EIC_DBNC input signals. At the process of system initialization, ARM needs to configure the EIC_DBNC input signal detecting conditions, such as '1'/'0' detection, read INT status registers and write EIC_DBNC_IC to clear the EIC_DBNC INTs. Then, if necessary, ARM sends a trig_start pulse to commence one EIC signal detection process. Before system enters deep-sleep mode or closes PCLK, it ought to assure that EIC_DBNC INT has been enabled and cleared and system has sent out active trig_start pulse.
2) After receiving the trig_start pulse, EIC_DBNC module starts the process of EIC_DBNC signal detection. If EIC captures one stable input signal, it will send an INT to ARM, shut off the clock of debounce circuit automatically and wait for next trig_start pulse.
3) When ARM receives the EIC_DBNC INT again, it enters INT process flow. And if EIC input condition changes, ARM needs to configure those detecting condition registers again. Then, if necessary, ARM sends a trig_start pulse again to commence a new EIC_DBNC signal detection process.
4) Step 1 to step 3 cycles.
5) For the debounce bypass mode, ARM can receive INT without the need of sending trig_start pulse.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

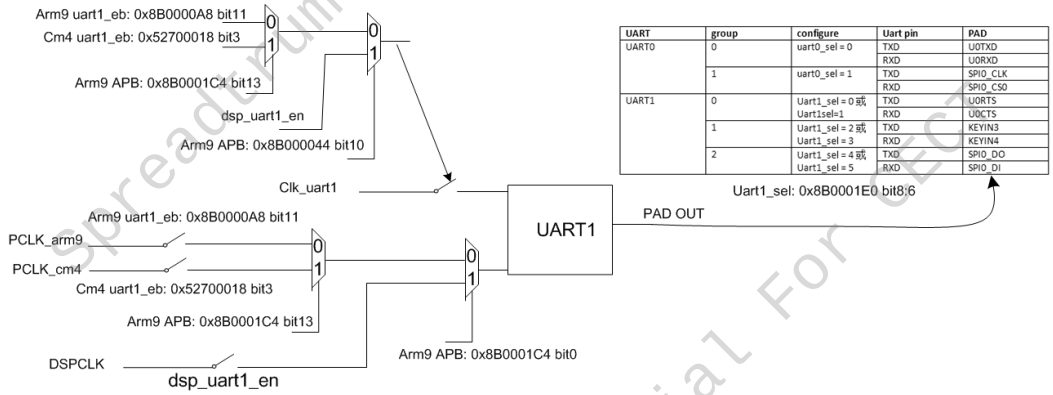
5.18.5.2 Programming Notes

2) The register, EIC_DBNC_IEV, is used to set the input signal constraints for INT trigger.
3) EIC_DBNC_INT comes from EIC_DBNC_MIS, which EIC_DBNC_MIS is equal to EIC_DBNC_IE & EIC_DBNC_RIS. So, if it needs to get some EIC_DBNC' INT, the EIC_DBNC_IE should be unmasked. And if ARM has received one EIC_DBNC INT, it maybe need to mask the corresponding bit of EIC_DBNC_IE to avoid to received the same INT, and set corresponding bits 1 to of EIC_DBNC_IC.
4) To quit EIC_DBNC FSM correctly, it needs 2 or 3 additional milliseconds. So it needs consider the additional time for exact debounce period.

5.19 ARM9/CM4/DSP share UART1 mechanism

5.19.1 arch

For cost down, ARM9/CM4/DSP share one log uart: uart1. The detail share mechanism is shown in next figure:



UART	group	configure	Uart pin	PAD
UART0	0	uart0_sel = 0	TXD	U0TXD
			RXD	U0RXD
	1	uart0_sel = 1	TXD	SPI0_CLK
			RXD	SPI0_CS0
UART1	0	Uart1_sel = 0 或 Uart1sel=1	TXD	U0RTS
			RXD	U0CTS
	1	Uart1_sel = 2 或 Uart1_sel = 3	TXD	KEYIN3
			RXD	KEYIN4
	2	Uart1_sel = 4 或 Uart1_sel = 5	TXD	SPI0_DO
			RXD	SPI0_DI

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6 Micro-Controller Unit Peripherals

6.1 USB

This section describes guidelines to interface the Universal Serial Bus (USB) controller of SC6531 to a USB client cable connector for attachment to a USB network. Included in this section is a description of how to configure SC6531 USB controller registers for connection to external USB host.

6.1.1 Overview

SC6531 includes a Universal Serial Bus (USB) device controller that complies with the Universal Serial Bus Specification Rev 1.1. The USB device controller is designed to provide a high performance of full speed (12 Mbps) function with DMA interface. The USB device controller allows bulk transfer with DMA, interrupt transfer and control transfer. Refer to the Universal Serial Bus Specification Rev 1.1 for a full description of the USB protocol and its operations.

The USB device controller includes 5 endpoints, one is control endpoint, and the others are data endpoints.

- Endpoint0 is the control endpoint. This endpoint will be done by hardware and the main function of this endpoint is for the host to configure the device.
- Endpoint1 is a configurable IN endpoint. It can be configured into bulk or interrupt IN endpoint.
- Endpoint2 is a configurable OUT endpoint. It can be configured into bulk or interrupt OUT endpoint.
- Endpoint3 is a configurable IN endpoint. It can be configured into bulk or interrupt IN endpoint.
- Endpoint4 is a configurable OUT endpoint. It can be configured into bulk or interrupt OUT endpoint.

6.1.2 Features

6.1.2.1 Five Endpoints with FIFO and DMA Interface

6.1.2.1.1 Endpoint0, a Control Endpoint

The configuration of USB device controller is done by this endpoint. The configuration includes: get_status, clear_feature, set_feature, set_address, get_descriptor, set_descriptor, get_configuration, set_configuration, get_interface, set_interface and synch_frame. And in these request the request set_descriptor can be enabled by ARM AHB and its default state is enable.

In these configurations we will get the data such as endpoint number current used, device address, endpoint1 type, endpoint2 type, endpoint3 type, endpoint4 type, max size of one packet, max size of one transfer and so on.

- This endpoint does not support bulk transfer.
- This endpoint does not support interrupt transfer.
- This endpoint does not support isochronous transfer.
- This endpoint provides an interrupt signal to USB controller.
- This endpoint provides some interrupts for debug or control.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

- This endpoint features a 128-byte FIFO for IN channel, a128-byte FIFO for OUT channel.
- This endpoint features two dedicate DMA channels, one is used by IN channel, and the other is used by OUT channel.

6.1.2.1.2 **Endpoint1, a Configurable IN Endpoint**

This endpoint can be configured into bulk or interrupt endpoint.

- As a bulk endpoint, it will receive data coming from host and then send the data to memory by the DMA channel.
- As an interrupt endpoint, it will receive data from host and then send the data to memory by the DMA channel.
- This endpoint does not support control transfer.
- This endpoint does not support isochronous transfer.
- This endpoint provides an interrupt signal to USB controller.
- This endpoint provides some interrupt sources for debug or control.
- This endpoint features a 64-byte FIFO.
- This endpoint features a dedicate DMA channel.

6.1.2.1.3 **Endpoint2, a Configurable OUT Endpoint**

This endpoint can be configured into bulk or interrupt endpoint.

- As a bulk endpoint, it will transfer data coming from memory by DMA channel to host.
- As an interrupt endpoint, it will transfer data coming from memory by DMA channel to host.
- This endpoint does not support isochronous transfer.
- This endpoint provides an interrupt signal to USB controller.
- This endpoint provides some interrupt sources for debug or control.
- This endpoint features a 64-byte FIFO.
- This endpoint features a dedicate DMA channel.

6.1.2.1.4 **Endpoint3, a Configurable IN Endpoint**

This endpoint can be configured into bulk or interrupt endpoint.

- As a bulk endpoint, it will receive data coming from host and then send the data to memory by the DMA channel.
- As an interrupt endpoint, it will receive data from host and then send the data to memory by the DMA channel.
- This endpoint does not support control transfer.
- This endpoint does not support isochronous transfer.
- This endpoint provides a interrupt signal to USB controller.
- This endpoint provides some interrupt sources for debug or control.
- This endpoint features a 64-byte FIFO.
- This endpoint features a dedicate DMA channel.

6.1.2.1.5 **Endpoint4, a Configurable OUT Endpoint**

This endpoint can be configured into bulk or interrupt endpoint.

- As a bulk endpoint, it will transfer data coming from memory by DMA channel to host.
- As an interrupt endpoint, it will transfer data coming from memory by DMA channel to host.
- This endpoint does not support isochronous transfer.
- This endpoint provides a interrupt signal to USB controller.
- This endpoint provides some interrupt sources for debug or control.
- This endpoint features a 64-byte FIFO.
- This endpoint features a dedicate DMA channel.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.1.2.2 Support Suspending and Resuming

The USB controller can check whether to get suspending and resuming signals and can check the use of suspending and resuming signal in the state machine.

6.1.2.3 Support Reset Signal Coming from Host

The reset signal coming from host is judged by SIE module and it will reset all sub modules except the registers on the ARM AHB bus. When device receives this reset signal the whole module will enter the default main state.

6.1.2.4 Support 6 DMA Channels

There are six DMA channels in the USB controller module. They are endpoint0 IN, endpoint0 OUT, endpoint1, endpoint2, endpoint3, and endpoint4 channel.

6.1.2.5 Support Interrupt Enable and State

Every endpoint provides a dedicate interrupt source to the USB controller, and the USB device controller provides a dedicate interrupt source to MCU Interrupt Controller. Please refer to 3.10.

Every endpoint provides many interrupt reasons for debugging or that can be used for flow control.

6.1.2.6 Read and Write of Memories

Every endpoint has a dedicate block of dual port RAM as FIFO.

Notes: These FIFOs only support 32-bit write and read.

6.1.2.7 Support Remote Wakeup

The USB controller supports remote wakeup from suspend state. The remote wakeup signal comes from device when the host is in suspend state.

6.1.2.8 Integrate USB Transceiver

SC6531 has integrated USB transceiver inside.

6.1.3 Signal description

SC6531 can be easily connected to the USB port of an external host by a USB cable.

SC6531 supports USB charge by USB cable.

SC6531 controls USB connection by enabling inside USB_LDO.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

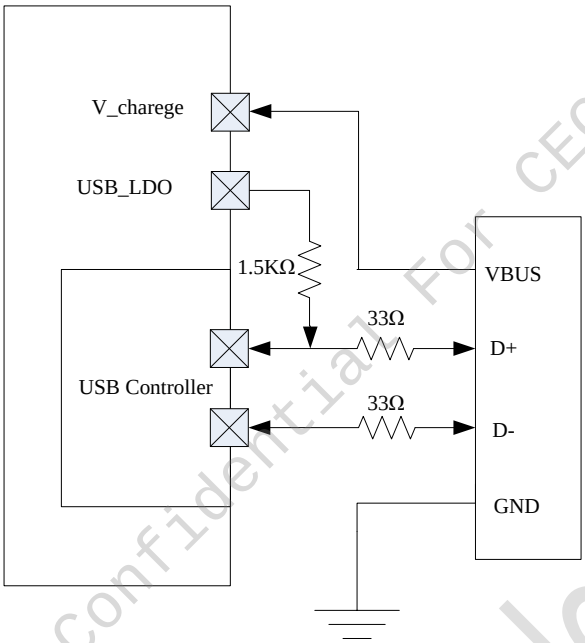


Figure 6-1 USB application diagram

6.1.4 Control registers

6.1.4.1 Memory map

Table 6-1 USB Contol Register Address Map

Address offset	Register name	Description
0x0000	USB_CTRL	USB device control
0x0004	USB_STS	USB device status
0x0008		Reserved
0x000C	ENDP_RST	Endpoint reset
0x0010	SIE_CTRL	SIE control
0x0014	INT_CTRL	Interrupt control
0x0018	INT_STS	Interrupt masked status of device
0x001C	INT_CLR	Interrupt clear of device
0x0020	INT_RAW_STS	Interrupt raw status of device
0x0024	FRM_NUM	Frame number
0x0028	TIMEOUT_LMT	Time out limit
0x002C-0x003F		Reserved.
0x0040	TR_SIZE_IN_ENDP0	Transfer size for endpoint 0 IN
0x0044	TR_SIZE_OUT_ENDP0	Transfer size for endpoint 0 OUT
0x0048	SEND_SIZE_ENDP0	Send transfer data size for endpoint 0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Address offset	Register name	Description
0x004C	RCV_SIZE_ENDP0	Receive transfer data size for endpoint 0
0x0050	RMT_SEND	Remote send
0x0054	CFG_VALUE	Configuration value
0x0058	IF_ALT	Interface alternate
0x005C	REQ_SETUP_LOW	Request setup low word
0x0060	REQ_SETUP_HIGH	Request setup high word
0x0064	ENDP0_CTRL	Endpoint 0 control
0x0068	INT_CTRL_ENDP0	Interrupt control for endpoint 0
0x006C	INT_ STS_ENDP0	Interrupt status for endpoint 0
0x0070	INT_CLR_ENDP0	Interrupt clear for endpoint 0
0x0074	INT_RAW_STS_ENDP0	Interrupt raw status for endpoint 0
0x0078	DMA_WAIT_IN_ENDP0	DMA endpoint 0 IN wait time
0x007C	DMA_WAIT_OUT_ENDP0	DMA endpoint 0 OUT wait time
0x0080-0x00BF	Reserved.	
0x00C0	ENDP1_CTRL	Endpoint 1 control
0x00C4	SND_DATA_ENDP1	Send transfer data for endpoint 1
0x00C8	TRANS_SIZE_ENDP1	Transfer size for endpoint 1
0x00CC	INT_CTRL_ENDP1	Interrupt control for endpoint 1
0x00D0	INT_STS_ENDP1	Interrupt status for endpoint 1
0x00D4	INT_CLR_ENDP1	Interrupt clear for endpoint 1
0x00D8	INT_RAW_STS_ENDP1	Interrupt raw status for endpoint 1
0x00DC	DMA_WAIT_ENDP1	DMA endpoint 1 wait time
0x00E0-0x00FF	Reserved.	
0x0100	ENDP2_CTRL	Endpoint 2 control
0x0104	RCV_DATA_ENDP2	Receive transfer data for endpoint 2
0x0108	TRANS_SIZE_ENDP2	Transfer size for endpoint 2
0x010C	INT_CTRL_ENDP2	Interrupt control for endpoint 2
0x0110	INT_STS_ENDP2	Interrupt status for endpoint 2
0x0114	INT_CLR_ENDP2	Interrupt clear for endpoint 2
0x0118	INT_RAW_STS_ENDP2	Interrupt raw status for endpoint 2
0x011C	DMA_WAIT_ENDP2	DMA endpoint 2 wait time
0x0120-0x013F	Reserved.	
0x0140	ENDP3_CTRL	Endpoint 3 control
0x0144	SND_DATA_ENDP3	Send transfer data for endpoint 3
0x0148	TRANS_SIZE_ENDP3	Transfer size for endpoint 3
0x014C	INT_CTRL_ENDP3	Interrupt control for endpoint 3

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Address offset	Register name	Description
0x0150	INT_STS_ENDP3	Interrupt status for endpoint 3
0x0154	INT_CLR_ENDP3	Interrupt clear for endpoint 3
0x0158	INT_RAW_STS_ENDP3	Interrupt raw status for endpoint 3
0x015C	DMA_WAIT_ENDP3	DMA endpoint 3 wait time
0x0160-0x017F	Reserved.	
0x0180	ENDP4_CTRL	Endpoint 4 control
0x0184	RCV_DATA_ENDP4	Receive transfer data for endpoint 4
0x0188	TRANS_SIZE_ENDP4	Transfer size for endpoint 4
0x018C	INT_CTRL_ENDP4	Interrupt control for endpoint 4
0x0190	INT_STS_ENDP4	Interrupt status for endpoint 4
0x0194	INT_CLR_ENDP4	Interrupt clear for endpoint 4
0x0198	INT_RAW_STS_ENDP4	Interrupt raw status for endpoint 4
0x019C	DMA_WAIT_ENDP4	DMA endpoint 4 wait time
0x01A0-0x7FFFF	Reserved.	
0x80000	FIFO_entry_endp0_in	-
0x80004	FIFO_entry_endp1	-
0x80008	FIFO_entry_endp3	-
0x8000C	FIFO_entry_endp_out	-
0x80010	FIFO_entry_endp2	-
0x80014	FIFO_entry_endp4	-

6.1.4.2 Register description

6.1.4.2.1 DEV_CTRL

Description: This register is used to enable or disable the USB module

0x0000 USB control

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved														SELF_PWR	USB_EN
Type	RO														R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Field Name	Bit	R/W	Default	Description
Reserved	[31:2]			

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SELF_PWR	[1]	RW	1'b1	Self powered 0: not self-powered device. Software should write 1 to this bit since our USB device is always self-powered. 1: this USB device is self-powered, no need for external power from bus
USB_EN	[0]	RW	1'b0	Device enable: 1: enable the device 0: disable the device

6.1.4.2.2 **USB_STS**

Description: This register is used to get current state of USB module

0x0004 USB device status

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved												REMOTE_WAKEUP_EN	ENDP		
Type	RO												RO	RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ENDP	Reserved					STATE_CURRENT			DEVICE_ADDRESS						
Type	RO	RO					RO			RO						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
DEVICE_ADDRESS	[6:0]	RO	7'b0	Device address coming from host by set_address request
STATE_CURRENT	[9:7]	RO	3'b0	Current state of device: 0: Default 1: Address 2: Configured 3: Suspend from Default 4: Suspend from Address 5: Suspend from Configured 6: reserved 7: reserved
	[14:10]	RO	5'b0	Reserved
ENDP	[18:15]	RO	4'b0	Endpoint number what is using
REMOTE_WAKEUP_EN	[19]	RO	1'b0	Current state of device Remote wakeup (feature set by HOST): 0:Disable 1:Enable
	[31:20]	RO	12'b0	Reserved

6.1.4.2.3 **ENDP_RST**

Description: This register is used to enable or disable the USB module

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x000C **Endpoint reset**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved				TOGGLE_RST4	TOGGLE_RST3	TOGGLE_RST2	TOGGLE_RST1	Reserved	TOGGLE_RST0	FIFO_RST4	FIFO_RST3	FIFO_RST2	FIFO_RST1	FIFO_RST0_OUT	FIFO_RST0_IN
Type	RO				WO	WO	WO	WO	RO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:12]	RO	20'b0	Reserved.
TOGGLE_RST4	[11]	WO	1'b0	Data toggle reset for endpoint 4
TOGGLE_RST3	[10]	WO	1'b0	Data toggle reset for endpoint 3
TOGGLE_RST2	[9]	WO	1'b0	Data toggle reset for endpoint 2
TOGGLE_RST1	[8]	WO	1'b0	Data toggle reset for endpoint 1
	[7]	RO	1'b0	Reserved
TOGGLE_RST0	[6]	WO	1'b0	Data toggle reset for endpoint 0
FIFO_RST4	[5]	WO	1'b0	FIFO reset for endpoint 4
FIFO_RST3	[4]	WO	1'b0	FIFO reset for endpoint 3
FIFO_RST2	[3]	WO	1'b0	FIFO reset for endpoint 2
FIFO_RST1	[2]	WO	1'b0	FIFO reset for endpoint 1
FIFO_RST0_OUT	[1]	WO	1'b0	FIFO reset for endpoint 0 OUT
FIFO_RST0_IN	[0]	WO	1'b0	FIFO reset for endpoint 0 IN

6.1.4.2.4 **SIE_CTRL**

Description: This register is used to configure SIE interface.

0x0010 **SIE control**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved														SIE_RX_EOP_TIME OUT	SIE_RX_SYNC_DETECT_MODE
Type	RO														R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:2]	RO	30'b0	Reserved.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SIE_RX_EOP_TIMEOUT	[1]	RW	1'b0	0: Disable 1: Enable SIE Rx EOP signal timeout
SIE_RX_SYNC_DETECT_MODE	[0]	RW	1'b0	SIE Rx detect sync mode 0: detect sync by 8 bits 1: detect sync by 5 bits

6.1.4.2.5 **INT_CTRL**

Description: This register is used to enable interrupt sources of the USB device

0x0014 Interrupt control

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved									STATE_CHANGE	PID_ERROR	UNSUP_PID	RST_FROM_HOST	RESUME	SUSPEND	SOF_PACKET
Type	RO									R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:7]	RO	25'b0	Reserved.
STATE_CHANGE	[6]	RW	1'b0	State of device changed
PID_ERROR	[5]	RW	1'b0	Received PID error
UNSUP_PID	[4]	RW	1'b0	Received unsupported PID
RST_FROM_HOST	[3]	RW	1'b0	Reset from host
RESUME	[2]	RW	1'b0	Detected a J to K state change when the device is in the suspend state
SUSPEND	[1]	RW	1'b0	Device into suspend state
SOF_PACKET	[0]	RW	1'b0	Start of frame packet

6.1.4.2.6 **INT_STS**

Description: This register is used to get interrupt status of the USB module, which could be masked by register int_ctrl

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0018 **Interrupt status**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved									STATE_CHANGE	PID_ERROR	UNSUP_PID	RST_FROM_HOST	RESUME	SUSPEND	SOF_PACKET
Type	RO									RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:7]	RO	25'b0	Reserved
STATE_CHANGE	[6]	RO	1'b0	0: No interrupt request 1: State of device changed interrupt is pending.
PID_ERROR	[5]	RO	1'b0	0: No interrupt request 1: PID error interrupt is pending.
UNSUP_PID	[4]	RO	1'b0	0: No interrupt request 1: Unsupported PID interrupt is pending.
RST_FROM_HOST	[3]	RO	1'b0	0: No interrupt request 1: Reset interrupt from host is pending.
RESUME	[2]	RO	1'b0	0: No interrupt request 1: A J to K state change interrupt when the device is in the 'suspend' state is pending.
SUSPEND	[1]	RO	1'b0	0: No interrupt request 1: Into suspend state interrupt is pending
SOF_PACKET	[0]	RO	1'b0	0: No interrupt request 1: SOF packet interrupt is pending.

6.1.4.2.7 **INT_CLR**

Description: This register is used to clear the interrupt status of USB module, both masked status and raw status

0x001C **Interrupt clear**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved									STATE_CHANGE	PID_ERROR	UNSUP_PID	RST_FROM_HOST	RESUME	SUSPEND	SOF_PACKET
Type	RO									R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[31:7]	WO	25'b0	Reserved
STATE_CHANGE	[6]	WO	1'b0	0: No effect. 1: Clear state of device changed interrupt
PID_ERROR	[5]	WO	1'b0	0: No effect. 1: Clear PID error interrupt
UNSUP_PID	[4]	WO	1'b0	0: No effect. 1: Clear unsupported PID interrupt
RST_FROM_HOST	[3]	WO	1'b0	0: No effect. 1: Clear reset signal interrupt
RESUME	[2]	WO	1'b0	0: No effect. 1: Clear a J to K state change interrupt
SUSPEND	[1]	WO	1'b0	0: No effect.. 1: Clear suspend state interrupt
SOF_PACKET	[0]	WO	1'b0	0: No effect. 1: Clear SOF packet interrupt

6.1.4.2.8 **INT_RAW_STS**

Description: This register is used to get the interrupt raw status of USB module

0x0020 Raw interrupt status

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved									STATE_CHANGE	PID_ERROR	UNSUP_PID	RST_FROM_HOST	RESUME	SUSPEND	SOF_PACKET
Type	RO									RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:7]	RO	25'b0	Reserved
STATE_CHANGE	[6]	RO	1'b0	0: No interrupt request 1: State of device changed interrupt is pending.
PID_ERROR	[5]	RO	1'b0	0: No interrupt request 1: PID error interrupt is pending.
UNSUP_PID	[4]	RO	1'b0	0: No interrupt request 1: Unsupported PID interrupt is pending.
RST_FROM_HOST	[3]	RO	1'b0	0: No interrupt request 1: Reset interrupt from host is pending.
RESUME	[2]	RO	1'b0	0: No interrupt request 1: A J to K state change interrupt when the device is in the 'suspend' state is pending.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SUSPEND	[1]	RO	1'b0	0: No interrupt request 1: Into suspend state interrupt is pending
SOF_PACKET	[0]	RO	1'b0	0: No interrupt request 1: SOF packet interrupt is pending.

6.1.4.2.9 **FRM_NUM**

Description: This register is used to get the number of frame received.

0x0024 **Frame number**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved					FRAME_NUMBER										
Type	RO					RO										
Reset	0	0	0	0	0											

Field Name	Bit	R/W	Default	Description
	[31:11]	RO	21'b0	Reserved
FRAME_NUMBER	[10:0]	RO	11'b0	Frame number as received from SOF packet

6.1.4.2.10 **TIMEOUT_LMT**

Description: This register is used to set the time out limited of inter packet.,The unit of time is 12MHz cycles

0x0028 **Timeout limit for inter packet**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								TIMEOUT_LIMIT							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:8]	RO	24'h0	Reserved
TIMEOUT_LIMIT	[7:0]	RW	8'h8	Time out limited of inter packet. Actual used value is 8'hb+Tmout_lmt

6.1.4.2.11 **TR_SIZE_IN_ENDP0**

Description: This register is used to set total size in endpoint0 next IN transfer.The unit of transfer size is byte.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0040 **Transfer size for endpoint 0 IN**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	
Name	Reserved															TR
Type																R/W
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSF_SIZE_IN_ENDP0															
Type	R/W															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:17]	RO	15'b0	Reserved
TRANSF_SIZE_IN_ENDP0	[16:0]	RW	17'h04000	Total size (byte number) in endpoint0 next IN transfer.

6.1.4.2.12 **TR_SIZE_OUT_ENDP0**

Description: This register is used to set total size in endpoint0 of the next OUT transfer.The unit of transfer size is byte.

0x0044 **Transfer size for endpoint 0 OUT**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															TR
Type																R/W
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSF_SIZE_OUT_ENDP0															
Type	R/W															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:17]	RO	15'b0	Reserved
TRANSF_SIZE_OUT_ENDP0	[16:0]	RW	17'h04000	Total size (byte number) in endpoint0 next OUT transfer.

6.1.4.2.13 **SEND_SIZE_ENDP0**

Description: This register is used to get the number of transfer data has been sent from the endpoint0.The unit of transfer data is byte.

0x0048 **Sent transfer data size for endpoint 0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															TR
Type																R/W
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENT_TRANSDATA0															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:17	RO	15'b0	Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SENT_TRANSDATA0	[16:0]	RO	17'h0	Sent the transfer data byte number of endpoint0

6.1.4.2.14 **RCV_SIZE_ENDP0**

Description: This register is used to get the number of transfer data has been received from the endpoint0.The unit of transfer data is byte.

0x004C **Receive transfer data size for endpoint 0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															TR
Type																R/W
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RCV_TRANSDATA0															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:17]	RO	15'b0	Reserved
RCV_TRANSDATA0	[16:0]	RO	17'h0	Received the transfer data byte number of endpoint0

6.1.4.2.15 **RMT_SEND**

Description: This register is used to send remote wakeup signal to HOST.

0x0050 **Remote send**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															RMT_SNED
Type	RO															WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:1]	RO	31'b0	Reserved
RMT_SNED	[0]	WO	1'b0	Remote wakeup sending action: 0: No effect. 1: Send remote wakeup signal to host

6.1.4.2.16 **CFG_VALUE**

Description: This register is used to get configuration value coming from HOST.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0054 **Configuration value**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								CFG_VALUE							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:8]	RO	24'b0	Reserved
CFG_VALUE	[7:0]	RO	8'b0	Configuration value coming from host

6.1.4.2.17 **IF_ALT**

Description: This register is used to get interface number coming from host by SETUP transaction.

0x0058 **Interface alternate**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								ALTERNATE_SETTING				INTERFACE_NUMBER			
Type	RO								R/W				RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:8]	RO	24'h0	Reserved
ALTERNATE_SETTING	[7:4]	RW	4'h0	Alternate interface setting from host or SW; (wValue)
INTERFACE_NUMBER	[3:0]	RO	4'h0	Interface number coming from host by SETUP transaction. (wIndex)

6.1.4.2.18 **REQ_SETUP_LOW**

Description: This register is used to get request setup low word data.

0x005C **Request setup low word**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WVALUE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BREQUEST								BMREQUESTTYPT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
WVALUE	[31:16]	RO	16'h0	Word-sized field that varies according to request

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

BREQUEST	[15:8]	RO	8'h0	Specific request
BMREQUESTTYPT	[7:0]	RO	8'h0	Characteristics of request: D7: Data transfer direction 0 = Host-to-device 1 = Device-to-host D6...5: Type 0 = Standard 1 = Class 2 = Vendor 3 = Reserved D4...0: Recipient 0 = Device 1 = Interface 2 = Endpoint 3 = Other 4...31 = Reserved

6.1.4.2.19 **REQ_SETUP_HIGH**

Description: This register is used to get request setup high word data.

0x0060 **Request setup high word**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WLENGTH															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	WINDEX															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
WLENGTH	[31:16]	RO	16'h0	Number of bytes to transfer if there is a Data stage
WINDEX	[15:0]	RO	16'h0	Word-sized field that varies according to request; typically used to pass an index or offset

6.1.4.2.20 **ENDP0_CTRL**

Description: This register is used to get the status of Endpoint0.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0064 **Endpoint 0 control**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved		STALL	BUFF_READY	DATA_READY	Reserved				MAX_PL_SZ						
Type	RO		R/W	R/W	R/W	RO				R/W						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_PL_SZ				SETUP_INT_INTERVENE	PACKET_NUMBER										
Type	R/W				R/W	RO										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:30]	RO	2'b0	Reserved
STALL	[29]	RW	1'b0	0: Stop sending STALL to host 1: USB device controller sends STALL handshake to host at DATA or STATUS stage Note: endpoint will sending STALL to host either SW set register or HOST set feature
BUFF_READY	[28]	RW Self-clear	1'b0	0: Invalid; 1: Buffer ready of endpoint0, MCU or DMA can send data to FIFO when this bit has been set.
DATA_READY	[27]	RW Self-clear	1'b0	0: Invalid; 1: Data ready of endpoint0,MCU or DMA sends data to FIFO then sets this bit to 1, USB device controller will send data from FIFO to host after this bit has been set to 1, then clear it after send action end.
	[26:23]	RO	4'b0	Reserved
MAX_PL_SZ	[22:12]	RW	11'h40	Maximum payload size(maxpacketsize) in byte
SETUP_INT_INTERVENE	[11]	RW	1'b0	0: only enable setup transaction interrupt when request should be intervened by ARM. 1: every setup transaction interrupt enable
PACKET_NUMBER	[10:0]	R only	11'h0	Show the bytes number in current data packet received from host

6.1.4.2.21 **INT_CTRL_ENDP0**

Description: This register is used to get the status of Endpoint0.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0068 Interrupt control for endpoint 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved		DATA_NOT_READY	BUF_NOT_READY	DMAOUT_TMOUT	DMAIN_TMOUT	TRANSFER_END	SETUP_TRANS_END	BUF_FULL	BUF_EMPTY	CRC16_ERROR	SETUP_TIMEOUT	OUT_TIMEOUT	IN_TIMEOUT	DATA_TOGGLE	TRANSACTION_END
Type	RO		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:14]	RO	18'b0	Reserved
DATA_NOT_READY	[13]	RW	1'b0	0: Disable this interrupt; 1: Enable endpoint0 not be ready to send data to host interrupt.
BUF_NOT_READY	[12]	RW	1'b0	0: Disable this interrupt; 1: Enable endpoint0 buffer not be ready to receive data interrupt.
DMAOUT_TMOUT	[11]	RW	1'b0	0: Disable this interrupt; 1: Endpoint0 OUT wait DMA ACK time out interrupt.
DMAIN_TMOUT	[10]	RW	1'b0	0: Disable this interrupt; 1: Enable endpoint0 IN wait DMA ACK time out interrupt.
TRANSFER_END	[9]	RW	1'b0	0: Disable this interrupt; 1: Enable transfer end interrupt of control endpoint0. When USB controller receives the token of status stage, this interrupt will be provided. USB controller will wait MCU to clear this interrupt for sending zero data to host.
SETUP_TRANS_END	[8]	RW	1'b0	0: Disable this interrupt; 1: Enable setup transaction end interrupt.
BUF_FULL	[7]	RW	1'b0	0: Disable this interrupt; 1: Enable buffer full interrupt. When received data from host and all data has been send to MCU, this interrupt will be provided .
BUF_EMPTY	[6]	RW	1'b0	0: Disable this interrupt; 1: Enable buffer empty interrupt, When received data from MCU and all data has been send to host, this interrupt will be provided .
CRC16_ERROR	[5]	RW	1'b0	0: Disable this interrupt; 1: Enable CRC16 error interrupt

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SETUP_TIMEOUT	[4]	RW	1'b0	0: Disable this interrupt; 1: Enable SETUP wait data packet timeout interrupt
OUT_TIMEOUT	[3]	RW	1'b0	0: Disable this interrupt; 1: Enable OUT wait data packet timeout interrupt
IN_TIMEOUT	[2]	RW	1'b0	0: Disable this interrupt; 1: Enable IN wait ack packet timeout
DATA_TOGGLE	[1]	RW	1'b0	0: Disable this interrupt; 1: Enable data toggle error interrupt
TRANSACTION_END	[0]	RW	1'b0	0: Disable this interrupt; 1: Enable transaction end interrupt;

6.1.4.2.22 **INT_ STS_ENDP0**

Description: This register is used to get the status of Endpoint0 interrupt, which could by masked by register int_ctrl.

0x006C **Interrupt status for endpoint 0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved		DATA_NOT_READY	BUF_NOT_READY	DMAOUT_TMOUT	DMAIN_TMOUT	TRANSFER_END	SETUP_TRANS_END	BUF_FULL	BUF_EMPTY	CRC16_ERROR	SETUP_TIMEOUT	OUT_TIMEOUT	IN_TIMEOUT	DATA_TOGGLE	TRANSACTION_END
Type	RO		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:14]	RO	18'b0	Reserved
DATA_NOT_READY	[13]	RO	1'b0	0: No interrupt request 1: Endpoint0 not be ready to send data to host interrupt is pending.
BUF_NOT_READY	[12]	RO	1'b0	0: No interrupt request 1: Enable endpoint0 buffer not be ready to receive data interrupt is pending.
DMAOUT_TMOUT	[11]	RO	1'b0	0: No interrupt request 1: Endpoint0 OUT wait DMA ACK time out interrupt is pending.
DMAIN_TMOUT	[10]	RO	1'b0	0: No interrupt request 1: Endpoint0 IN wait DMA ACK time out interrupt is pending

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

TRANSFER_END	[9]	RO	1'b0	0: No interrupt request 1: Transfer end interrupt of control endpoint0 is pending. When USB controller receives the token of status stage, this interrupt will be provided. USB controller will wait MCU to clear this interrupt for sending zero data to host.
SETUP_TRANS_END	[8]	RO	1'b0	0: No interrupt request 1: Setup transaction end interrupt is pending.
BUF_FULL	[7]	RO	1'b0	0: No interrupt request 1: Buffer full interrupt is pending. When received data from host and all data has been send to MCU,
BUF_EMPTY	[6]	RO	1'b0	0: No interrupt request 1: Buffer empty interrupt is pending, When received data from MCU and all data has been send to host
CRC16_ERROR	[5]	RO	1'b0	0: No interrupt request 1: CRC16 error interrupt is pending
SETUP_TIMEOUT	[4]	RO	1'b0	0: No interrupt request 1: SETUP wait data packet timeout interrupt is pending
OUT_TIMEOUT	[3]	RO	1'b0	0: No interrupt request 1: OUT wait data packet timeout interrupt is pending.
IN_TIMEOUT	[2]	RO	1'b0	0: No interrupt request 1: IN wait ack packet timeout interrupt is pending;
DATA_TOGGLE	[1]	RO	1'b0	0: No interrupt request 1: Data toggle error interrupt is pending
TRANSACTION_END	[0]	RO	1'b0	0: No interrupt request; 1: Transaction end interrupt is pending;

6.1.4.2.23 **INT_CLR_ENDP0**

Description: This register is used to clear the status of Endpoint0 interrupt, both masked status and raw status.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0070 Interrupt clear for endpoint 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved		DATA_NOT_READY	BUF_NOT_READY	DMAOUT_TMOUT	DMAIN_TMOUT	TRANSFER_END	SETUP_TRANS_END	BUF_FULL	BUF_EMPTY	CRC16_ERROR	SETUP_TIMEOUT	OUT_TIMEOUT	IN_TIMEOUT	DATA_TOGGLE	TRANSACTION_END
Type	RO		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:14]	RO	18'b0	Reserved
DATA_NOT_READY	[13]	WO	1'b0	0: No effect; 1: Clear endpoint0 not be ready to send data to host interrupt
BUF_NOT_READY	[12]	WO	1'b0	0: No effect; 1: Clear endpoint0 buffer not be ready to receive data interrupt
DMAOUT_TMOUT	[11]	WO	1'b0	0: No effect; 1: Clear Endpoint0 OUT wait DMA ACK time out interrupt
DMAIN_TMOUT	[10]	WO	1'b0	0: No effect; 1: Clear Endpoint0 IN wait DMA ACK time out interrupt
TRANSFER_END	[9]	WO	1'b0	0: No effect; 1: Clear transfer end interrupt of control endpoint0. MCU must clear this interrupt for sending zero data to host.
SETUP_TRANS_END	[8]	WO	1'b0	0: No effect; 1: Clear setup transaction end interrupt
BUF_FULL	[7]	WO	1'b0	0: No effect; 1: Clear buffer full interrupt,
BUF_EMPTY	[6]	WO	1'b0	0: No effect; 1: Clear buffer empty interrupt
CRC16_ERROR	[5]	WO	1'b0	0: No effect; 1: Clear CRC16 error interrupt
SETUP_TIMEOUT	[4]	WO	1'b0	0: No effect; 1: Clear SETUP wait data packet timeout interrupt
OUT_TIMEOUT	[3]	WO	1'b0	0: No effect; 1: Clear OUT wait data packet timeout interrupt.
IN_TIMEOUT	[2]	WO	1'b0	0: No effect; 1: Clear IN wait ack packet timeout interrupt

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

DATA_TOGGLE	[1]	WO	1'b0	0: No effect; 1: Clear data toggle error interrupt
TRANSACTION_END	[0]	WO	1'b0	0: No effect; 1: Clear transaction end interrupt;

6.1.4.2.24 **INT_RAW_STS_ENDP0**

Description: This register is used to get the raw status of Endpoint0 interrupt.

0x0074 Interrupt raw status for endpoint 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved		DATA_NOT_READY	BUF_NOT_READY	DMAOUT_TMOUT	DMAIN_TMOUT	TRANSFER_END	SETUP_TRANS_END	BUF_FULL	BUF_EMPTY	CRC16_ERROR	SETUP_TIMEOUT	OUT_TIMEOUT	IN_TIMEOUT	DATA_TOGGLE	TRANSACTION_END
Type	RO		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:14]	RO	18'b0	Reserved
DATA_NOT_READY	[13]	RO	1'b0	0: No interrupt request 1: Endpoint0 not be ready to send data to host interrupt is pending.
BUF_NOT_READY	[12]	RO	1'b0	0: No interrupt request 1: Enable endpoint0 buffer not be ready to receive data interrupt is pending.
DMAOUT_TMOUT	[11]	RO	1'b0	0: No interrupt request 1: Endpoint0 OUT wait DMA ACK time out interrupt is pending.
DMAIN_TMOUT	[10]	RO	1'b0	0: No interrupt request 1: Endpoint0 IN wait DMA ACK time out interrupt is pending
TRANSFER_END	[9]	RO	1'b0	0: No interrupt request 1: Transfer end interrupt of control endpoint0 is pending. When USB controller receives the token of status stage, this interrupt will be provided. USB controller will wait MCU to clear this interrupt for sending zero data to host.
SETUP_TRANS_END	[8]	RO	1'b0	0: No interrupt request 1: Setup transaction end interrupt is pending.
BUF_FULL	[7]	RO	1'b0	0: No interrupt request 1: Buffer full interrupt is pending. When received data from host and all data has been send to MCU,

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

BUF_EMPTY	[6]	RO	1'b0	0: No interrupt request 1: Buffer empty interrupt is pending, When received data from MCU and all data has been send to host
CRC16_ERROR	[5]	RO	1'b0	0: No interrupt request 1: CRC16 error interrupt is pending
SETUP_TIMEOUT	[4]	RO	1'b0	0: No interrupt request 1: SETUP wait data packet timeout interrupt is pending
OUT_TIMEOUT	[3]	RO	1'b0	0: No interrupt request 1: OUT wait data packet timeout interrupt is pending.
IN_TIMEOUT	[2]	RO	1'b0	0: No interrupt request 1: IN wait ack packet timeout interrupt is pending;
DATA_TOGGLE	[1]	RO	1'b0	0: No interrupt request 1: Data toggle error interrupt is pending
TRANSACTION_END	[0]	RO	1'b0	0: No interrupt request; 1: Transaction end interrupt is pending;

6.1.4.2.25 DMA_WAIT_IN_ENDP0

Description: This register is used to set the timeout limit of Endpoint0 IN DMA waiting dma_ack The unit of time is 12MHz clock cycle

0x0078 DMA endpoint 0 IN wait time

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA0IN_WAITTIME															
Type	R/W															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:16]	RO	16'h0	Reserved
DMA0IN_WAITTIME	[15:0]	RW	16'h0100	Endpoint0 IN DMA wait dma_ack timeout limit

6.1.4.2.26 DMA_WAIT_OUT_ENDP0

Description: This register is used to set the timeout limit of Endpoint0 OUT DMA waiting dma_ack. The unit of time is 12MHz clock cycle

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x007C **DMA endpoint 0 OUT wait time**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DMA0OUT_WAITTIME															
Type	R/W															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:16]	RO	16'h0	Reserved
DMA0OUT_WAITTIME	[15:0]	RW	16'h0100	Endpoint0 OUT DMA wait dma_ack timeout limit

6.1.4.2.27 **ENDP1/3_CTRL**

Description: This register is used to control the action of endpoint1 (3)

0x00C0 **Endpoint 1 control**

0x0140 **Endpoint 3 control**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved		STALL		DATA_READY		EP_EN	TRANS_TYPE		MAX_PL_SZ						
Type			R/W		R/W		R/W	R/W		R/W						
Reset			0		0	0	0	0	0	0	0	0	0	1	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MAX_PL_SZ				HALT_EN	PACKET_NUMBER										
Type	R/W				RO	RO										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:30]	RO	2'b0	Reserved
STALL	[29]	RW	1'b0	0: Stop sending STALL to host 1: USB device controller sends STALL handshake to host at DATA or STATUS stage Note: endpoint will sending STALL to host either SW set register or HOST set feature
	[28]	RO	1'b0	Reserved
DATA_READY	[27]	RW Self-clear	1'b0	Data ready of endpoint_in
	[26]	RO	1'b0	Reserved
EP_EN	[25]	RW	1'b0	Endpoint enable 1: Enable corresponding endpoint 0: Disable corresponding endpoint

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

TRANS_TYPE	[24:23]	RW	EP1: 00 EP3: 01	Endpoint transfer type: 00: Bulk 01: interrupt 10: reserved 11: reserved
MAX_PL_SZ	[22:12]	RW	11'h40	Maximum payload size(maxpacketsize) in byte
HALT_EN	[11]	RO	1'b0	Endpoint_INx halt enable signal coming from host.
PACKET_NUMBER	[10:0]	RO	11'h0	Show the bytes number in current data packet received from host

6.1.4.2.28 **SND_DATA_ENDP1/3**

Description: This register is used to get the number of sent transfer data of endpoint1 (3) .
The unit of time is byte.

0x00C4 **Send transfer data for endpoint 1**

0x0144 **Send transfer data for endpoint 3**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_TRANSDATA1/3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:17]	RO	15'b0	Reserved
SEND_TRANSDATA1/3	[16:0]	RO	17'b0	Sent the transfer data byte number of endpoint1(3)

6.1.4.2.29 **TRANS_SIZE_ENDP1/3**

Description: This register is used to set total size in endpoint_in of one transfer
The unit of time is byte.

0x00C8 **Transfer size for endpoint 1**

0x0148 **Transfer size for endpoint 3**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANS_SIZE_ENDP1/3															
Type	R/W															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[31:17]	RO	15'h0	Reserved
TRANS_SIZE_ENDP1/3	[16:0]	RW	17'h04000	Total size (byte number) in endpoint1 (3) of one transfer.

6.1.4.2.30 **INT_CTRL_ENDP1/3**

Description: This register is used to control the interrupt of endpoint1 (3).

0x00CC **Interrupt control for endpoint 1**

0x014C **Interrupt control for endpoint 3**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		DATA_NOT_READY	Reserved		DMA_TMOUT	TRANSFER_END	Reserved		BUF_EMPTY	Reserved			TIMEOUT	Reserved	TRANSACTION_END
Type	RO		R/W	RO		R/W	R/W	RO		R/W	RO			R/W	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:14]	RO	18'b0	Reserved
DATA_NOT_READY	[13]	RW	1'b0	0: Disable this interrupt 1: Enable endpoint1 (3) not ready data to send to host interrupt. This interrupt will be active when host request data by sending IN token while data_ready not set
	[12:11]	RO	2'b0	Reserved
DMA_TMOUT	[10]	RW	1'b0	0: Disable this interrupt. 1: Enable endpoint1 (3) wait DMA ACK time out interrupt. This interrupt will be active when USB controller doesn't receive a DMA_ACK in specified time.
TRANSFER_END	[9]	RW	1'b0	0: Disable this interrupt. 1: Enable transfer end interrupt of endpoint1 (3). This interrupt will be active when all transfer data have been sent to host.
	[8:7]	RO	2'b0	Reserved
BUF_EMPTY	[6]	RW	1'b0	0: Disable this interrupt. 1: Enable buffer empty interrupt. This interrupt will be active when receiving data from MCU and these data have been send to host.
	[5:3]	RO	3'b0	Reserved
TIMEOUT	[2]	RW	1'b0	0: Disable this interrupt 1: Enable inter_packet time out interrupt. This interrupt will be active when inter packet delay exceed 8'hb+Tmout_lmt

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[1]	RO	1'b0	Reserved
TRANSACTION_END	[0]	RW	1'b0	0: Disable this interrupt. 1: Enable transaction end interrupt. This interrupt will be active when a transaction is end.

6.1.4.2.31 **INT_STS_ENDP1/3**

Description: This register is used to get the status of corresponding interrupt of endpoint1 (3) , which could be masked by register int_ctrl.

0x00D0 Interrupt status for endpoint 1

0x0150 Interrupt status for endpoint 3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved		DATA_NOT_READY	Reserved		DMA_TMOUT	TRANSFER_END	Reserved		BUF_EMPTY	Reserved			TIMEOUT	Reserved	TRANSACTION_END
Type	RO		RO	RO		RO	RO	RO		RO	RO			RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:14]	RO	18'b0	Reserved
DATA_NOT_READY	[13]	RO	1'b0	0: No interrupt request 1: Enable endpoint1 (3) not ready data to send to host interrupt is pending.
	[12:11]	RO	2'b0	Reserved
DMA_TMOUT	[10]	RO	1'b0	0: No interrupt request. 1: Endpoint1 (3) wait DMA ACK time out interrupt is pending.
TRANSFER_END	[9]	RO	1'b0	0: No interrupt request. 1: Transfer end interrupt is pending
	[8:7]	RO	2'b0	Reserved
BUF_EMPTY	[6]	RO	1'b0	0: No interrupt request. 1: Buffer empty interrupt is pending
	[5:3]	RO	3'b0	Reserved
TIMEOUT	[2]	RO	1'b0	0: No interrupt request. 1: Inter_packet time out interrupt is pending.
	[1]	RO	1'b0	Reserved
TRANSACTION_END	[0]	RO	1'b0	0: No interrupt request. 1: Transaction end interrupt is pending.

6.1.4.2.32 **INT_CLR_ENDP1/3**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Description: This register is used to clear corresponding interrupt of endpoint1 (3), both masked status and raw status.

0x00D4 **Interrupt clear for endpoint 1**

0x0154 **Interrupt clear for endpoint 3**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved		DATA_NOT_READY	Reserved		DMA_TMOUT	TRANSFER_END	Reserved		BUF_EMPTY	Reserved			TIMEOUT	Reserved	TRANSACTION_END
Type	RO		R/W	RO		R/W	R/W	RO		R/W	RO			R/W	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:14]	RO	18'b0	Reserved
DATA_NOT_READY	[13]	WO	1'b0	0: No effect 1: Clear endpoint1 not ready data to send to host interrupt.
	[12:11]	RO	2'b0	Reserved
DMA_TMOUT	[10]	WO	1'b0	0: No effect 1: Clear DMA ACK timeout interrupt.
TRANSFER_END	[9]	WO	1'b0	0: No effect 1: Clear transfer end interrupt
	[8:7]	RO	2'b0	Reserved
BUF_EMPTY	[6]	WO	1'b0	0: No effect 1: Clear buffer empty interrupt
	[5:3]	RO	3'b0	Reserved
TIMEOUT	[2]	WO	1'b0	0: No effect 1: Clear inter_packet timeout interrupt.
	[1]	RO	1'b0	Reserved
TRANSACTION_END	[0]	WO	1'b0	0: No effect 1: Clear transaction end interrupt.

6.1.4.2.33 **INT_RAW_STS_ENDP1/3**

Description: This register is used to get the raw status of endpoint1 (3) interrupts.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x00D8 **Interrupt raw status for endpoint 1**

0x0158 **Interrupt raw status for endpoint 3**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved		DATA_NOT_READY	Reserved		DMA_TMOUT	TRANSFER_END	Reserved		BUF_EMPTY	Reserved			TIMEOUT	Reserved	TRANSACTION_END
Type	RO		RO	RO		RO	RO	RO		RO	RO			RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:14]	RO	18'b0	Reserved
DATA_NOT_READY	[13]	RO	1'b0	0: No interrupt request 1: Enable endpoint1 (3) not ready data to send to host interrupt is pending.
	[12:11]	RO	2'b0	Reserved
DMA_TMOUT	[10]	RO	1'b0	0: No interrupt request. 1: Endpoint1 (3) wait DMA ACK time out interrupt is pending.
TRANSFER_END	[9]	RO	1'b0	0: No interrupt request. 1: Transfer end interrupt is pending
	[8:7]	RO	2'b0	Reserved
BUF_EMPTY	[6]	RO	1'b0	0: No interrupt request. 1: Buffer empty interrupt is pending
	[5:3]	RO	3'b0	Reserved
TIMEOUT	[2]	RO	1'b0	0: No interrupt request. 1: Inter_packet time out interrupt is pending.
	[1]	RO	1'b0	Reserved
TRANSACTION_END	[0]	RO	1'b0	0: No interrupt request. 1: Transaction end interrupt is pending.

6.1.4.2.34 **DMA_WAIT_ENDP1/3**

Description: This register is used to set the timeout limit of endpoint1 (3) wait DMA_ACK
The unit of time is 12MHz clock cycle

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x00DC **DMA endpoint 1 wait time**

0x015C **DMA endpoint 3 wait time**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_WAITTIME															
Type	R/W															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:16]		16'h0	reserved
DMA_WAITTIME	[15:0]	RW	16'h0100	Endpoint1(3) channel wait DMA_ACK timeout limit

6.1.4.2.35 **ENDP2/4_CTRL**

Description: This register is used to control endpoint2 (4).

0x0100 **Endpoint 2 control**

0x0180 **Endpoint 4 control**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved		STALL	BUF_READY	Reserved		EP_EN	TRANS_TYPE		MAX_PL_SZ						
Type	RO		R/W	R/W	RO		R/W	R/W		R/W						
Reset			0	0		0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_PL_SZ				HALT_EN	PACKET_NUMBER										
Type	R/W				RO	RO										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:30]	RO	2'b0	reserved
STALL	[29]	RW	1'b0	0: Stop sending STALL to host 1: USB device controller sends STALL handshake to host at DATA or STATUS stage Note: endpoint will sending STALL to host either SW set register or HOST set feature
BUF_READY	[28]	RW Self-clear	1'b0	Buffer ready of endpoint2(4)
	[27:26]	RO	2'b0	Reserved
EP_EN	[25]	RW	1'b0	Endpoint enable 1: Enable this endpoint 0: Disable this endpoint

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

TRANS_TYPE	[24:23]	RW	EP2: 00 EP4: 01	Endpoint transfer type: 00: Bulk 01: interrupt 10: reserved 11: reserved
MAX_PL_SZ	[22:12]	RW	11'h0040	Maximum payload size(maxpacketsize) in byte
HALT_EN	[11]	RO	1'b0	Endpoint2 (4) halt enable signal coming from host.
PACKET_NUMBER	[10:0]	RO	11'b0	Show the bytes number in current data packet received from host

6.1.4.2.36 **RCV_DATA_ENDP2/4**

Description: This register is used to get the number of received the transfer data of endpoint2 (4). The unit of time is byte.

0x0104 **Receive transfer data for endpoint 2**

0x0184 **Receive transfer data for endpoint 4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RECEIVE_TRANSDATA2/4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:17]	RO	15'h0	Reserved
Received_Transdata2(4)	[16:0]	RO	17'h0	Received the transfer data byte number of endpoin2(4)

6.1.4.2.37 **TRANS_SIZE_ENDP2/4**

Description: This register is used to set total size in endpoint2 (4) of one transfer

The unit of time is byte.

0x0108 **Transfer size for endpoint 2**

0x0188 **Transfer size for endpoint 4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANS_SIZE_ENDP2/4															
Type	R/W															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:17]	RO	15'h0	Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Transf_size_endp2(4)	[16:0]	RW	17'h4000	Total size (byte number) in endpoint2 (4) OUT of one transfer.

6.1.4.2.38 **INT_CTRL_ENDP2/4**

Description: This register is used to control the interrupt of endpoint2 (4).

0x010C **Interrupt control for endpoint 2**

0x018C **Interrupt control for endpoint 4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			BUF_NOT_READY	DMA_TMOUT	Reserved	TRANSFER_END	Reserved	BUF_FULL	Reserved	CRC16_ERROR	Reserved	TIMEOUT	Reserved	DATA_TOGGLE	TRANSACTION_END
Type	RO			R/W	R/W	RO	R/W	RO	R/W	RO	R/W	RO	R/W	RO	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:13]	RO	19'b0	Reserved
BUF_NOT_READY	[12]	RW	1'b0	0: Disable this interrupt 1: Enable endpoint2 (4) buff not ready to receive data interrupt. This interrupt will be active when host sending data in OUT transaction while buffer_ready not set
DMA_TMOUT	[11]	RW	1'b0	0: Disable this interrupt. 1: Enable endpoint2 (4) wait DMA ACK time out interrupt. This interrupt will be active when USB controller didn't receive a DMA_ACK in specified time.
	[10]	RO	1'b0	Reserved
TRANSFER_END	[9]	RW	1'b0	0: Disable this interrupt. 1: Enable transfer end interrupt of endpoint2 (4). This interrupt will be active when all transfer data have been received from host.
	[8]	RO	1'b0	Reserved
BUF_FULL	[7]	RW	1'b0	0: Disable this interrupt. 1: Enable endpoint 2(4) buffer full interrupt. This interrupt will be active when endpoint2 buffer (FIFO) is full.
	[6]	RO	1'b0	Reserved
CRC16_ERROR	[5]	RW	1'b0	0: Disable this interrupt. 1: Enable CRC16 error interrupt. This interrupt will be active when CRC16 error happened in received data.
	[4]	RO	1'b0	Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

TIMEOUT	[3]	RW	1'b0	0: Disable this interrupt 1: Enable inter_packet time out interrupt. This interrupt will be active when inter packet delay exceed 8'hb+Tmout_lmt
	[2]	RO	1'b0	Reserved
DATA_TOGGLE	[1]	RW	1'b0	0: Disable this interrupt. 1: Enable data toggle error interrupt. This interrupt will be active when data toggle error happened in received data.
TRANSACTION_END	[0]	RW	1'b0	0: Disable this interrupt. 1: Enable transaction end interrupt. This interrupt will be active when a transaction is end.

6.1.4.2.39 **INT_STS_ENDP2/4**

Description: This register is used to get the status of corresponding interrupt of endpoint2 (4) , which could by masked by register int_ctrl.

0x0110 Interrupt status for endpoint 2

0x0190 Interrupt status for endpoint 4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved			BUF_NOT_READY	DMA_TMOUT		TRANSFER_END	Reserved	BUF_FULL		CRC16_ERROR	Reserved	TIMEOUT	Reserved	DATA_TOGGLE	TRANSACTION_END
Type	RO			RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:13]	RO	19'b0	Reserved
BUF_NOT_READY	[12]	RO	1'b0	0: No interrupt request. 1: Enable endpoint2 (4) buff not ready to receive data interrupt is pending.
DMA_TMOUT	[11]	RO	1'b0	0: No interrupt request. 1: Endpoint wait DMA ACK timeout interrupt is pending.
	[10]	RO	1'b0	Reserved
TRANSFER_END	[9]	RO	1'b0	0: No interrupt request. 1: Transfer end interrupt is pending
	[8]	RO	1'b0	Reserved
BUF_FULL	[7]	RO	1'b0	0: No interrupt request. 1: Buffer full interrupt is pending
	[6]	RO	1'b0	Reserved
CRC16_ERROR	[5]	RO	1'b0	0: No interrupt request. 1: CRC16 error interrupt is pending.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[4]	RO	1'b0	Reserved
TIMEOUT	[3]	RO	1'b0	0: No interrupt request. 1: Inter_packet time out interrupt is pending.
	[2]	RO	1'b0	Reserved
DATA_TOGGLE	[1]	RO	1'b0	0: No interrupt request. 1: Data toggle error interrupt is pending.
TRANSACTION_END	[0]	RO	1'b0	0: No interrupt request. 1: Transaction end interrupt is pending.

6.1.4.2.40 **INT_CLR_ENDP2/4**

Description: This register is used to clear corresponding interrupt of endpoint2 (4) , both masked status and raw status.

0x0114 Interrupt clear for endpoint 2

0x0194 Interrupt clear for endpoint 4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved			BUF_NOT_READY	DMA_TMOUT	Reserved	TRANSFER_END	Reserved	BUF_FULL	Reserved	CRC16_ERROR	Reserved	TIMEOUT	Reserved	DATA_TOGGLE	TRANSACTION_END
Type	RO			R/W	R/W	RO	R/W	RO	R/W	RO	R/W	RO	R/W	RO	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:13]	RO	19'b0	Reserved
BUF_NOT_READY	[12]	W	1'b0	0: No effect 1: Clear endpoint2 (4) buff not ready to receive data interrupt.
DMA_TMOUT	[11]	W	1'b0	0: No effect 1: Clear DMA ACK timeout interrupt.
	[10]	RO	1'b0	Reserved
TRANSFER_END	[9]	W	1'b0	0: No effect 1: Clear transfer end interrupt
	[8]	RO	1'b0	Reserved
BUF_FULL	[7]	W	1'b0	0: No effect 1: Clear buffer full interrupt
	[6]	RO	1'b0	Reserved
CRC16_ERROR	[5]	W	1'b0	0: No effect 1: Clear CRC16 error interrupt.
	[4]	RO	1'b0	Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

TIMEOUT	[3]	W	1'b0	0: No effect 1: Clear inter_packet timeout interrupt.
	[2]	RO	1'b0	Reserved
DATA_TOGGLE	[1]	W	1'b0	0: No effect 1: Clear data toggle interrupt.
TRANSACTION_END	[0]	W	1'b0	0: No effect 1: Clear transaction end interrupt.

6.1.4.2.41 **INT_RAW_STS_ENDP2/4**

Description: This register is used to get the raw status of endpoint2 interrupts.

0x0118 Interrupt raw status for endpoint 2

0x0198 Interrupt raw status for endpoint 4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			BUF_NOT_READY	DMA_TMOUT	Reserved	TRANSFER_END	Reserved	BUF_FULL	Reserved	CRC16_ERROR	Reserved	TIMEOUT	Reserved	DATA_TOGGLE	TRANSACTION_END
Type	RO			RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:13]	RO	19'b0	Reserved
BUF_NOT_READY	[12]	RO	1'b0	0: No interrupt request. 1: Enable endpoint2 (4) buff not ready to receive data interrupt is arousing.
DMA_TMOUT	[11]	RO	1'b0	0: No interrupt request. 1: Endpoint wait DMA ACK time out interrupt is arousing.
	[10]	RO	1'b0	Reserved
TRANSFER_END	[9]	RO	1'b0	0: No interrupt request. 1: Transfer end interrupt is arousing
	[8]	RO	1'b0	Reserved
BUF_FULL	[7]	RO	1'b0	0: No interrupt request. 1: Buffer full interrupt is arousing
	[6]	RO	1'b0	Reserved
CRC16_ERROR	[5]	RO	1'b0	0: No interrupt request. 1: CRC16 error interrupt is arousing.
	[4]	RO	1'b0	Reserved
TIMEOUT	[3]	RO	1'b0	0: No interrupt request. 1: Inter_packet time out interrupt is arousing.
	[2]	RO	1'b0	Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

DATA_TOGGLE	[1]	RO	1'b0	0: No interrupt request. 1: Data toggle error interrupt is arousing.
TRANSACTION_END	[0]	RO	1'b0	0: No interrupt request. 1: Transaction end interrupt is arousing.

6.1.4.2.42 **DMA_WAIT_ENDP2/4**

Description: This register is used to set the timeout limit of endpoint2 (4) DMA wait DMA_ACK
The unit of time is 12MHz clock cycle

0x011C **DMA endpoint 2 wait time**

0x019C **DMA endpoint 4 wait time**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_WAITTIME															
Type	R/W															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:16]	RO	16'h0	Reserved
DMA_WAITTIME	[15:0]	RW	16'h100	Endpoint2(4) DMA wait dma_ack timeout limit

6.1.4.2.43 **FIFO_ENTRY_IN_ENDP0/1/3**

Description: This register is entry of endpoint FIFO. The depth of this FIFO is 128 bytes. When the FIFO is almost-empty (only have MaxPayloadSize/2 bytes) it will send DMA request to DMA module

These FIFO only support 32 bits write and read

0x80000 **FIFO Entry in endpoint0**

0x80004 **FIFO Entry in endpoint1**

0x80008 **FIFO Entry in endpoint3**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_ENTRY_IN															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_ENTRY_IN															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
FIFO_ENTRY_IN	[31:0]	RW	32'h0	Entry of FIFO for endpoint0 IN (endp1,endp3)written by AHB

6.1.4.2.44 **FIFO_ENTRY_OUT_ENDP0/2/4**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Description: This register is entry of endpoint FIFO. The depth of this FIFO is 128 bytes. When the FIFO is almost-empty (only have MaxPayloadSize/2 bytes) it will send DMA request to DMA module

These FIFO only support 32 bits write and read

0x8000C **FIFO Entry out endpoint0**

0x80010 **FIFO Entry out endpoint2**

0x80014 **FIFO Entry out endpoint4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_ENTRY_OUT															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_ENTRY_OUT															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
FIFO_ENTRY_OUT	[31:0]	RW	32'h0	Entry of FIFO for endpoint0 IN (endp2,endp4) read by AHB

6.1.5 Application notes

- When software wants to reset one endpoint, it should first write EP_enable of the endpoint to 0 and then write 1 to this bit.
- After software write EP_ENABLE to 0, the endpoint will reset all its registers.
- Each time one Endpoint's data toggle reset to DATA 0, the software must write data toggle reset bit to 1 before set EP_DREADY or EP_BREADY to 1.
- Each time before enable an interrupt source, software must clear the interrupt.
- Under DMA data transfer mode, each time before setting Data Ready or Buffer Ready, SW must reset the correspond endpoint's FIFO; in ARM data transfer mode, SW must reset the FIFO before writing data or setting buffer ready.
- DMA burst size should be set to MaxPayloadSize/2 in terms of word, i.e., MaxPayloadSize/8 or [MaxPayloadSize/8] +1
- In DMA data transfer mode, SW should monitor DMA interrupt status to judge a transfer finished or not and disable corresponding DMA channel if transfer ends; while in ARM data transfer mode SW should use USB interrupts.
- For an IN transfer, if inter_packet timed out, the current transaction will be sent again when the next IN token comes. For an OUT transfer, if CRC16 error interrupt occurs, the current transaction should be received again.
- If a data toggle error occurs without CRC16 error, which means the HOST did not receive ACK of device, just ignore the received data.
- System power manager needs to judge the source of charge, since it can come from external adaptor or USB; when system received charge interrupt first, power manager needs to enable USB and check the interrupt of USB .If the setup interrupt of USB is valid, the charge source comes from USB. Otherwise, it comes from the adaptor. If the source comes from an external adaptor, power manager needs close USB module for saving power and prepares for next plugging in.
- All endpoints FIFO only support 32 bits write and read.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.2 UART and IrDA interface

6.2.1 Overview

UART is an asynchronous communication interface. The UART module includes a baud rate generator with software-programmable divider ratios for all common baud rates. Two 128-byte-deep FIFO buffers can minimize processor overhead. The module also includes a flexible interrupt with multiple maskable interrupt sources. Two hardware flow control lines are included (one for input, the other for output). This module also has a built-in IrDA controller and can be configured to connect to an IrDA transceiver. When being used as regular UART port, the IrDA controller is bypassed.

6.2.2 Features

- Full-duplex operation
- Hardware flow control support
- Software flow control support with configurable command and escape register
- 128-byte-deep FIFOs minimizes processor overhead at high data rates
- Wide selection of UART word lengths, including 5, 6, 7 and 8 bits
- Stop bit number can be 0, 1, 1.5 or 2 bits
- Support odd/even parity
- Auto detect for parity and framing error
- UART loop-back test mode
- Break character detection and generation
- support DMA operation
- Single interrupt line for multiple maskable interrupt source events
- Programmable interrupt trigger levels for FIFOs
- Baud rate generation based upon programmable divisors, operating from a flexible functional clock
- Includes a built-in IrDA controller

6.2.3 Signal description

Signal	I/O	Description	Reset
uart_txd	O	Serial data output. Since the uart_txd is active high, the pin is set to low on reset	1'h1
uart_rxd	I	Serial data in	1'hx
uart_ctsn	I	Clear to send Active-low modem status signal. This signal is asserted (logic'0') by the DCE device to inform the UART module that transmission may begin. RTS and CTS are commonly used as handshaking signals to moderate the flow of data into the receiving UART device. The value of this signal is indicated by the UART STS0 bit9 after logical inverse. When the input signal CTSN changes value, either from 0 to 1 or from 1 to 0, an interrupt will be generated to the MCU. If hardware flow control is enabled and the signal CTSN is high, the UART immediately stops data transmission on the TXD output pin after it completes the current data byte transmission. Reading bit 9 of the UART status register checks the condition of uart_cts (inverse).	1'hx
uart_rtsn	O	Request to send When active (low), the module is ready to receive data. This assertion might	1

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

		mean enabling the transmit circuits of DTE device, or setting up the channel direction in half-duplex applications. When hardware flow control is not set, programming the UART CTL0 bit 6 directly controls the output of RTSN. This pin is the inverse of UART CTL0 bit 6. If receive hardware flow control is set by writing “1” to UART CTL1 bit 7, RTSN will be controlled by the RX FIFO level and Receive_Hardware_Flow_Control threshold. The threshold can be configured by writing UART CTL1[5:0].In this case, RTSN remains high as long as the number of data in the RX FIFO is greater than the configured threshold value.	

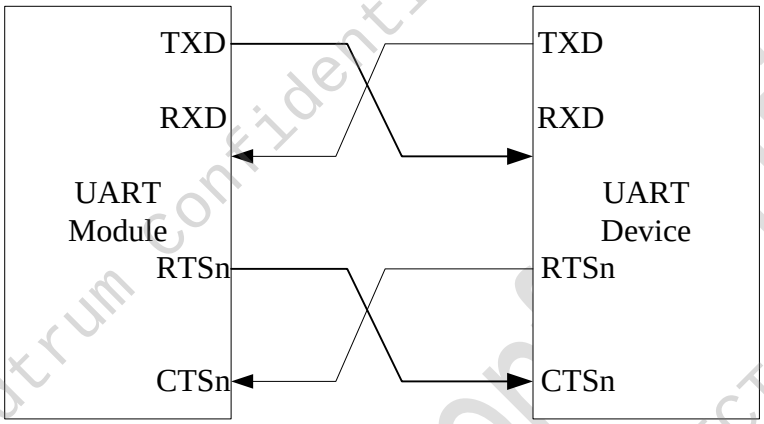


Figure 1 UART with flow control signal connection application

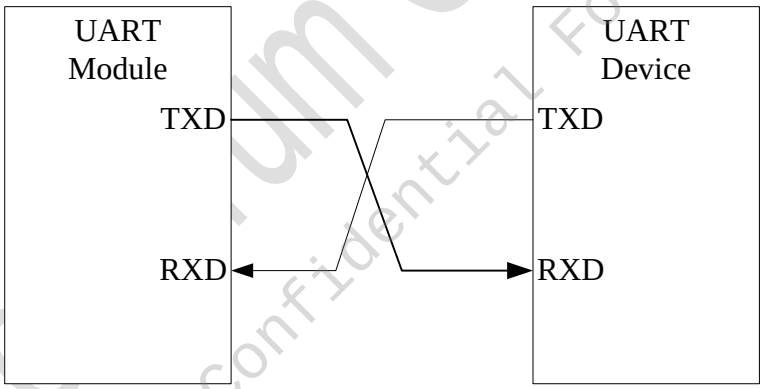


Figure 2 UART1/UART2 without flow control signal connection application

6.2.4 Funtion description

The UART and IRDA baud rate generator is based on the clk_uart, the divisor coefficient is controlled by register UART_CKD0. IRDA part clock period is the 1/16 of the UART part since the required timing of IRDA is 3/16 or 4/16 of bit width. The serial data rate can be changed by modify the clk_uart or the UART divisor coefficient.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

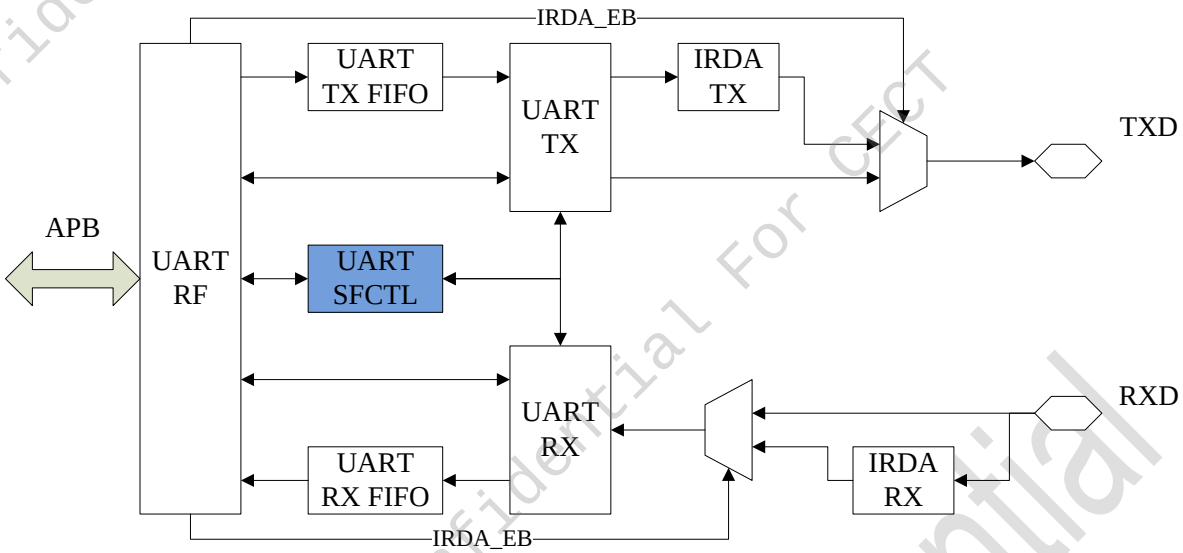


Figure3 Diagram of UART

Figure 3 is the architecture diagram of the UART module, as it depicted in the graphic, the UART module has seperated RX and TX channel to realize the duplex working mode. And the UART module also support to enable the IRDA transceiver mode.

6.2.4.1 UART Mode Description

UART module has an independent baud rate generator, which is used as a reference clock for data transmit and recovery. It also has a 128-byte-deep RX FIFO and a 128-byte-deep TX FIFO to decrease processor interrupt load during the data receiving and transmitting.

6.2.4.1.1 FIFO Management

FIFOs are accessed by reading/writing UART_RXD/UART_TXD register. The number of data in TX/RX FIFO can be observed by reading UART_STS1 [6:0]/UART_STS1 [14:8]. Rx_fifo_full and Tx_fifo_empty status can be obtained by reading UART_STS0 [1:0]. UART_CTL2 register controls the FIFO trigger level, which enables the DMA request and interrupt generation.

TX FIFO size is 128 bytes. It uses a FIFO pointer to monitor the number of data in the TX FIFO that has not yet been transmitted. The MCU can read the UART STS1 [14:8] to access the pointer. The UART also provides a TXF empty interrupt threshold that can be configured by writing UART CTL2 [14:8].

RX FIFO size is 128 bytes. It uses a pointer to monitor the number of data in the RX FIFO that have not yet been read by the MCU. The MCU can access the pointer by reading the UART STS1 [6:0]. The UART also provides a RX FIFO full interrupt threshold that can be configured by writing to UART CTL2 [6:0]. In FIFO interrupt mode with flow control, the programmer must also ensure that the Receive_Hardware_Flow_Control_Threshold (UART_CTL1 [6:0]) value is greater than or equal to the Receive_Int_WaterMark (UART_CTL2 [6:0]). Otherwise, FIFO operation stalls.

In FIFO interrupt mode, the processor is informed of the status of the receiver and transmitter by an interrupt signal. The rx_fifo_full interrupt is set when the number of RX FIFO data bytes is larger than the RX interrupt watermark value. It is auto cleared when the condition disappears. The tx_fifo_empty interrupt is set when the number of TX FIFO data bytes is less than the TX interrupt watermark value. It is auto cleared when the condition disappears. The two interrupt sources can be masked by writing “0” to UART_IEN register bit 0 and bit 1.The interrupt signal instructs the local hosts to write data to TX FIFO or read data from RX FIFO.

Note that in the cases of the UART flow control being enabled along with the interrupt capabilities, the user must ensure that the UART flow control FIFO threshold is greater than or equal to the receive FIFO watermark.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

The TX and RX FIFO may be accessed by DMA. Writing to control register UART_CTL1 bit 15 will enable DMA mode. In receive mode, a DMA request is generated as soon as the receive FIFO reached its threshold level defined in UART_CTL2 [6:0]. This request is deserted when the number of bytes is less than the threshold level. In transmit mode, a DMA request is automatically asserted when the transmit FIFO is almost empty.

In this mode, when RX FIFO is almost full (the number of RX FIFO data bytes is larger than the RX interrupt watermark value), it will send the receive request to DMA controller, and when TX FIFO is almost empty, it will send the transmit request to DMA controller.

6.2.4.1.2 Flow Control

The UART module support hardware and software flow control. The hardware flow control should use rtsn/ctsn signal to indicate the flow status. The software flow control use command which integrated in data stream in the txd/rxd signal to indicate the flow control status. The hardware flow control control has two mode, 1) auto flow control, 2) software configured hardware flow control. When the UART_SFCTL register bit1 is set to 1, the software flow control enabled, or if the UART_SFCTL[1] is 0 and if the UART_CTL1[8:7] is set to 2'b11 the auto hardware flow is enabled, or if the UART_CTL[8:7] is 2'b00, the rtsn is set by software, and the receive flow control is disabled.

6.2.4.1.3 Hardware Flow Control

The UART module supports both auto hardware flow control and software configured hardware flow control. When UART_CTL1 register bit 7 is set to "0", software will control the signal uart_rtsn by writing UART_CTL0 register bit 6; if "1", the signal uart_rtsn will be controlled by hardware itself, called auto-RTS.

Auto hardware flow control is composed of auto-CTS and auto-RTS. Auto-CTS and auto-RTS can be enabled/disabled independently by programming UART_CTL1 [8:7].

Auto-RTS data flow control originates in the receiver block. The receiver FIFO trigger levels used in auto-RTS are stored in the UART_CTL1 [6:0]. RTS is active if the RX FIFO level is below the HALT trigger level. When the receiver FIFO HALT trigger level is reached, uart_rtsn is deserted. The sending device (external UART device) may send an additional byte after the trigger level is reached because it may not recognize the desertion of RTSn until it has begun sending the additional byte. The assertion requests the sending device to resume transmission. In this case, uart_rtsn is an active-low signal.

With auto-CTS, uart_ctsn must be active before the module can transmit data. The transmitter circuitry checks uart_ctsn before sending the next data byte. When uart_ctsn is active, the transmitter sends the next byte. The auto-CTS function reduces interrupts to the host system. When auto-CTS flow control is enabled, the CTS state changes need not trigger host interrupts because the device automatically controls its own transmitter. Without auto-CTS, the transmitter sends any data present in the transmit FIFO and a receiver overrun error can result. In this case, uart_ctsn is an active-low signal.

6.2.4.1.4 Software Flow Control without CTSn and RTSn

The UART module support software flow control without use CTSn and RTSn signals. When the UART_SFCTL reigster **bit[1]** is set to 1, the software flow control is enabled.The user also can config the UART_SFCTL reigster **bit[0]** to select the mode of the software flow contorl function.

The process of the software flow control is showing as the figure 4.The reciver endpoint use the receive fifo index to judge whether to suspend the tranmision. When the receive fifo index is larger than the threshold, the receive endpoint will send XOFF command by uart_tx to the transmit endpoint, then the transmit will be suspend. When the receive fifo index is smaller than the threshold , the receive endpoint will send the XON command to transmitter to restart the transmission.Vice verse, when transmitting data, the uart_rx will receive the XOFF and XON command to suspend and restart

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

the transmission.So the UART module will realize the control flow without use CTSn and RTSn signals, it can reduce the usage of IO resource.

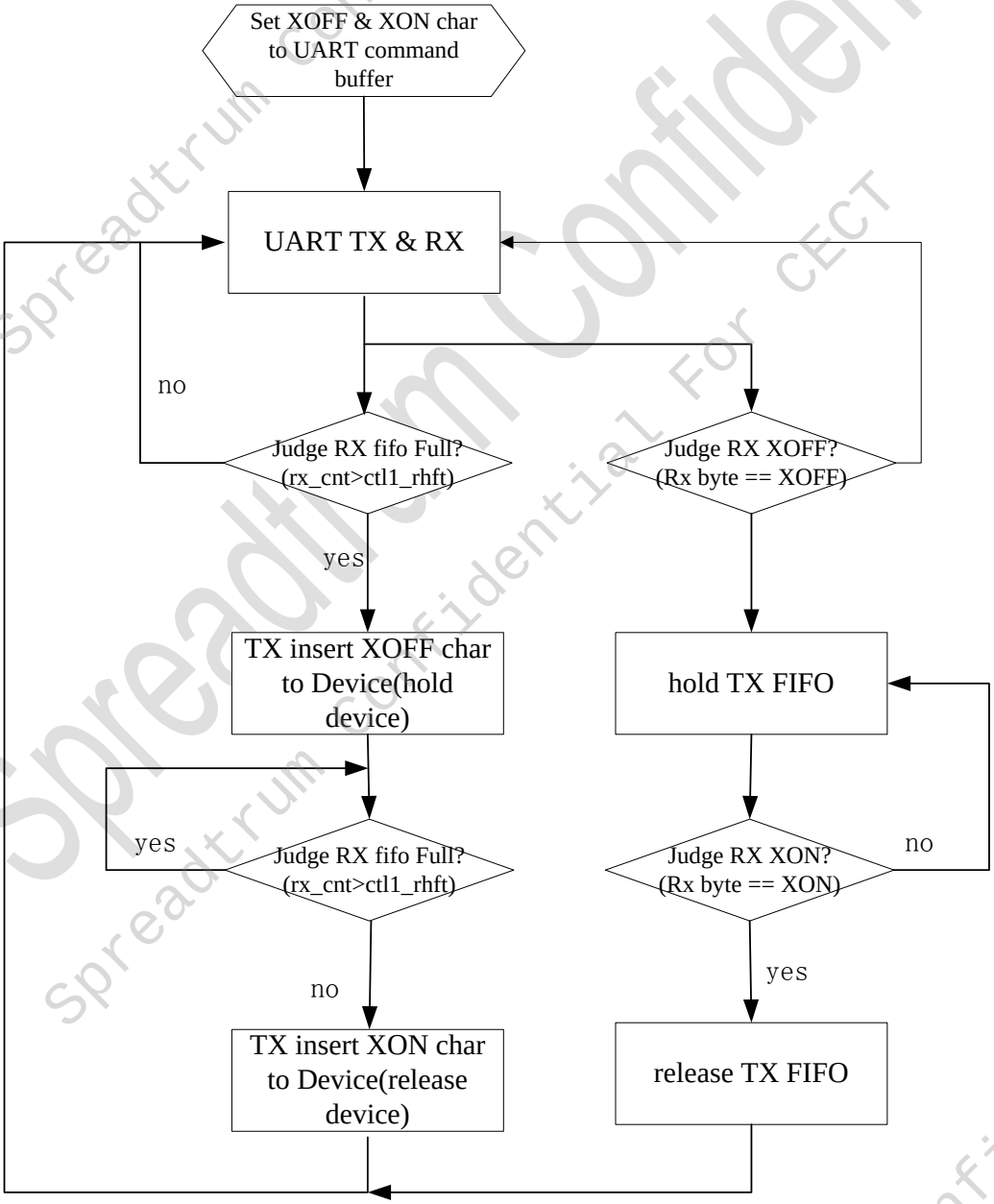
Since the software flow control will send command to represent the flow control status, there will be several data have the same value as the XCMD(XON/XOFF), in order to prevent transmission error, the data or the command should be escaped before transmitting or after the receiving. So it will use another command ESC to represent the data status.

The UART module support two mode for escaping. The fisrt mode is send XCMD as the normal data, and use ESC command and the inverted data to repesent the transfer data that has the same value of the XCMD and ESC.The second kind is send the data that has the same value of the XCMD as normal uart transmitting, and send XCMD with a ESC prefix.The format example are shown as follow:

Suppose using 0x11 to represent XON, 0x13 to represent XOFF, 0x77 to represent ESC,

When use mode 0 to transimit data 0x11 0x13 0x77, the data should be escape to 0x77 0xEE 0x77 0xEC 0x77 0x88. When transimit XON, it should be tranismit 0x11.

When use mode 1 to transimit data 0x11 0x13, the data can be tranimited without escape, when transimt XON, the transmit data should be 0x77 0x11, when transimit data 0x77, the data should be escaped to 0x77 0x77.



This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Figure 4 Software Flow Control Processing Flow

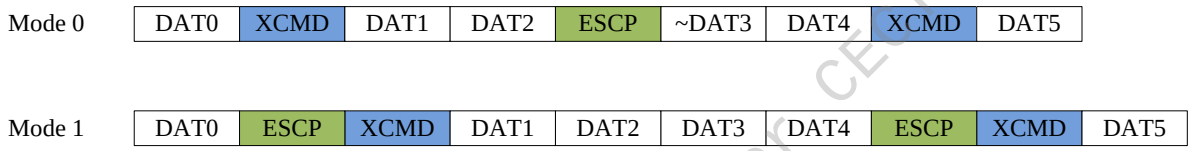


Figure 5 Software Flow Control Data Stream(Mode0/Mode1)

6.2.4.1.5 Interrupt sources

The UART also provides a TXF empty interrupt threshold that can be configured by writing UART CTL2 [14:8]. A tx_fifo_empty interrupt will be generated when the number of TX FIFO data bytes is less than the TX interrupt watermark value. It is auto cleared when the condition disappears.

UART also provides a RX FIFO full interrupt threshold that can be configured by writing to UART CTL2 [6:0]. An rx_fifo_full interrupt will be generated when the number of RX FIFO data bytes is larger than the RX interrupt watermark value. The interrupt will be auto cleared when the condition disappears.

An rx_tout interrupt will be generated if the UART has not received data from the input line in a period of time. This period depends on the baudrate and the value of CTL1 [13:9]. If the value of CTL1 [13:9] is '0',the interrupt will never be generated. The interrupt can be cleared by writing "1" to UART_ICLR bit 13.

When having received data, UART generate parity error/framing error if error condition occurs. Also, when having received FIFO overrun, an error interrupt will be generated. Writing to corresponding interrupt clear bit will clear these interrupts.

All interrupt sources in UART module can be disabled and masked by writing to the corresponding registers.

When TX FIFO is empty and TX is idle, setting send break bit forces the TX data output to low.

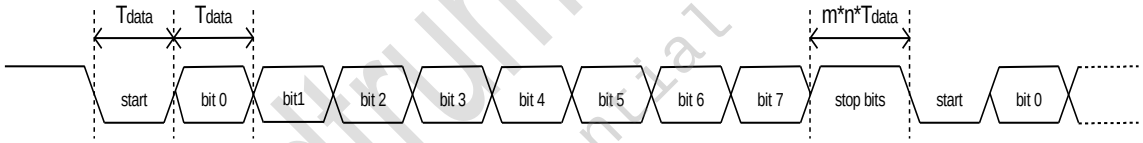


Figure 6 UART timing parameter

6.2.4.1 IRDA Mode Description

The IrDA can be used to communicate with other IrDA compatible device. IrDA mode is selected by writing "1" to UART CTL0 [15]. The default value of this bit is "0".

IrDA mode is achieved by adding IrDA transmit block and IrDA receive block into UART module. The IrDA transmit block changes the UART transmit serial bits to the IrDA timing, and then sends to TXD port. On the other side, the receive module detects the IrDA timing from the RXD port and changes back to UART bit stream to let the UART receive block to finish the data receiving.

Figure below shows the transmit IrDA timing. The polarity could be changed by UART CTL0 bit 9, and the pulse of a bit may be 3 or 4 high cycle controlled by the UART CTL0 bit 13. In the no polarity invert working mode, when sending "1", the output remains "0". And when sending "0", output follows the IrDA timing as demonstrated in the figure. On the receive data path, the polarity could be change by UART_CTL0 bit 10. The transmission and receive operation could be controlled by the UART CTL0 bit 11 and bit 12.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

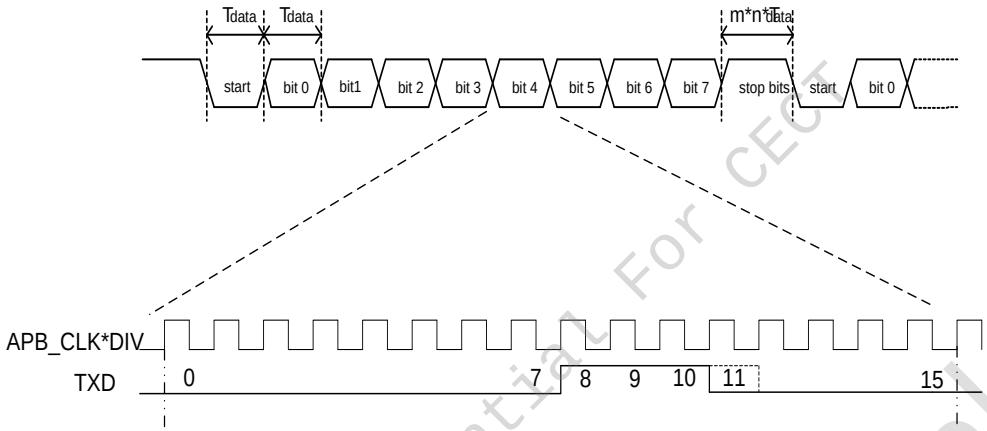


Figure 7 IrDA transmit timing

6.2.4.2 Uart interface timing

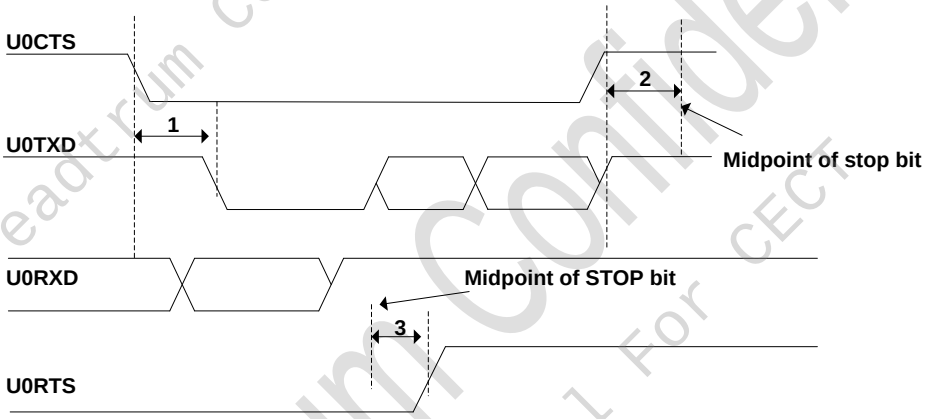


Figure 8 Uart Bus Timing (Default)

TABLE 1 Bus Timing – Parameter Values (Default)

Ref NO.	Characteristics	Min.	Typical	Max.	Unit
1	Delay time,uart_cts_n low to uart_txd valid	-	-	1.5	Bit periods
2	Setup time,uart_cts_n high before midpoint of stop bit	-	-	-	Bit periods
3	Delay time,midpoint of stop bit to uart_rts_n high	-	-	0.5	Bit periods

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

For T2 timing, If T2 >= 0.5 bit time (U0CTS high active before the stop bit), next TX data will not send; else, the next TX data will send out, and the data after the next one will not send.

6.2.5 Control registers

6.2.5.1 Memory map

Offset Address	Name	Description
0x0000	UART_TXD	Write data to this address initiates a character transmission through TX FIFO
0x0004	UART_RXD	Read from this address retrieve data from RX FIFO
0x0008	UART_STS0	UART working status
0x000C	UART_STS1	The fifo idex of TXF and RXF
0x0010	UART_IEN	UART interrupt enable register
0x0014	UART_ICLR	UART interrupt clear register
0x0018	UART_CTRL0	UART control register
0x001C	UART_CTRL1	UART control register
0x0020	UART_CTRL2	UART control register
0x0024	UART_CKD0	Divisor is the configed data in CKD
0x002C	UART_STS2	UART interrupt mask status
0x0030	UART_DSPWAIT	Control register
0x0034	UART_SFCTL	Software flow control function config register
0x0038	UART_XCMD	XCMD(XON/XOFF) command config register
0x003C	UART_ESCAPE	ESCAPE command config register

6.2.5.2 Register description

6.2.5.2.1 UART_TXD

Description：Write data to this address initiates a character transmission through TX FIFO.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0000			UART TX register(0x0000_0000)													UART_TXD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								UART_TXD							
Type	RO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
UART_TXD	[7:0]	WO	8'h0	Write data to this address initiates a character transmission through TX FIFO

6.2.5.2.2 **UART_RXD**

Description： the entry of RX Data FIFO, read RX fifo from this address

0x0004			UART RX register(0x0000_0000)													UART_RXD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								UART_RXD							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
UART_RXD	[7:0]	RO	8'h0	FIFO operation register Reading this register retrieves the next data byte from the Rx FIFO.

6.2.5.2.3 **UART_STS0**

Description： UART status register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0008			Register description (0x0000_9802)													UART_STS0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TRANS_OVER	RXF_REALFULL	TIME_OUT_RAW_STS	RXF_REALEMPTY	RXD	RTS	CTS	DSR	BRK_DTCT_RAW_STS	CTS_CHG_RAW_STS	DSR_CHG_RAW_STS	RXF_OVERRUN_RAW_STS	FRAME_ERR_RAW_STS	PARITY_ERR_RAW_STS	TXF_EMPTY_RAW_STS	RXF_FULL_RAW_STS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0

Field Name	Bit	R/W	Reset Value	Description
TRANS_OVER	[15]	RO	1'h1	Data transfer is really over
RXF_REALFULL	[14]	RO	1'h0	RX FIFO is real full(not relates to register RXF_FULL_THLD)
TIME_OUT_RAW_STS	[13]	RO	1'h0	RAW timeout interrupt , this bit is set when receive time is out.
RXF_REALEMPTY	[12]	RO	1'h1	1: rxf real empty 0: rxf not real empty
RXD	[11]	RO	1'h1	Receive data
RTS	[10]	RO	1'h0	(~rtsn)Request to send, if cnt_rxf< RCV_HW_FLOW_THLD, RTS=1, else RTS=0. if reset RTS=0.
CTS	[9]	RO	1'h0	(~ctsn)Clear to send.
DSR	[8]	RO	1'h0	(~dsrn)Data set ready(no used)
BRK_DTCT_RAW_STS	[7]	RO	1'h0	Raw break detect interrupt
CTS_CHG_RAW_STS	[6]	RO	1'h0	Raw CTS change interrupt
DSR_CHG_RAW_STS	[5]	RO	1'h0	Raw DSR change interrupt
RXF_OVERRUN_RAW_STS	[4]	RO	1'h0	Raw RX FIFO overrun interrupt
FRAME_ERR_RAW_STS	[3]	RO	1'h0	Raw frame error interrupt
PARITY_ERR_RAW_STS	[2]	RO	1'h0	Raw parity error interrupt
TXF_EMPTY_RAW_STS	[1]	RO	1'h1	Raw TX FIFO empty interrupt

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

RXF_FULL_RAW_STS	[0]	RO	1'h0	Raw RX FIFO full interrupt

6.2.5.2.4 **UART_STS1**

Description： data number in the TXF and RXF

0x000C		Register description (0x0000_0000)													UART_STS1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	TXF_CNT							Reserved	RXF_CNT						
Type	RO	RO							RO	RO						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_CNT	[14:8]	RO	7'h0	The number reserved in TX FIFO. The register will increase when writing data to the TX FIFO, while decrease when reading data from TX FIFO
Reserved	[7]	RO	1'h0	
RXF_CNT	[6:0]	RO	7'h0	The number reserved in RX FIFO. The register will increase when writing data to the RX FIFO, while decrease when reading data from RX FIFO

6.2.5.2.5 **UART_IEN**

Description：UART interrupt enable register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0010			Interrupt enable (0x0000_0000)													UART_IEN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		TIME_OUT_INT_EN	Reserved					BRK_DTCT_INT_EN	CTS_CHG_INT_EN	DSR_CHG_INT_EN	RXF_OVERRUN_INT_EN	FRAME_ERR_INT_EN	PARITY_ERR_INT_EN	TXF_EMPTY_INT_EN	RXF_FULL_INT_EN
Type	RO		R/W	RO					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TIME_OUT_INT_EN	[13]	R/W	1'h0	Time out interrupt enable
Reserved	[12:8]	RO	5'h0	
BRK_DTCT_INT_EN	[7]	R/W	1'h0	Break detect interrupt enable
CTS_CHG_INT_EN	[6]	R/W	1'h0	CTS change interrupt enable
DSR_CHG_INT_EN	[5]	R/W	1'h0	DSR change interrupt enable
RXF_OVERRUN_INT_EN	[4]	R/W	1'h0	RX FIFO overrun interrupt enable
FRAME_ERR_INT_EN	[3]	R/W	1'h0	Frame error interrupt enable
PARITY_ERR_INT_EN	[2]	R/W	1'h0	Parity error interrupt enable
TXF_EMPTY_INT_EN	[1]	R/W	1'h0	TX FIFO empty interrupt enable
RXF_FULL_INT_EN	[0]	R/W	1'h0	RX FIFO full interrupt enable

6.2.5.2.6 UART_ICLR

Description：UART interrupt clear register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0014			Interrupt clear (0x0000_0000)													UART_ICLR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		TIME_OUT_INT_CLR	Reserved					BRK_DTCT_INT_CLR	CTS_CHG_INT_CLR	DSR_CHG_INT_CLR	RXF_OVERRUN_INT_CLR	FRAME_ERR_INT_CLR	PARITY_ERR_INT_CLR	Reserved	
Type	RO		WO	RO					WO	WO	WO	WO	WO	WO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TIME_OUT_INT_CLR	[13]	WO	1'h0	Write "1" Clear time out interrupt
Reserved	[12:8]	RO	5'h0	
BRK_DTCT_INT_CLR	[7]	WO	1'h0	Write "1" Clear break_detect interrupt
CTS_CHG_INT_CLR	[6]	WO	1'h0	Write "1" Clear cts_change interrupt
DSR_CHG_INT_CLR	[5]	WO	1'h0	Write "1" Clear dsr_change interrupt
RXF_OVERRUN_INT_CLR	[4]	WO	1'h0	Write "1" Clear rxf_overrun interrupt
FRAME_ERR_INT_CLR	[3]	WO	1'h0	Write "1" Clear frame_error interrupt
PARITY_ERR_INT_CLR	[2]	WO	1'h0	Write "1" Clear parity_error interrupt
Reserved	[1:0]	RO	2'h0	

6.2.5.2.7 **UART_CTRL0**

Description : UART control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0018			Control register (0x0000_0000)													UART_CTRL0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MODE_SEL	Reserved	IR_WCTL	IR_DPLX	IR_TX_EN	IR_RX_IV	IR_TX_IV	DTR_REG	SEND_BRK_EN	RTS_REG	STOP_BIT_NUM		BYTE_LEN		PARITY_EN	ODD_PARITY
Type	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W		R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Field Name	Bit	R/W	Reset Value	Description
MODE_SEL	[15]	R/W	1'h0	"0" : UART "1" : IrDA
Reserved	[14]	RO	1'h0	
IR_WCTL	[13]	R/W	1'h0	set "1", increase pulse width for one clock.
IR_DPLX	[12]	R/W	1'h0	IRDA TX/RX enable
IR_TX_EN	[11]	R/W	1'h0	IRDA TX enable
IR_RX_IV	[10]	R/W	1'h0	IRDA RX polarity inverse
IR_TX_IV	[9]	R/W	1'h0	IRDA TX polarity inverse
DTR_REG	[8]	R/W	1'h0	This bit controls the dtrn output
SEND_BRK_EN	[7]	R/W	1'h0	When TX FIFO is empty and TX is idle, setting this bit forces the TX data output low. Need to be cleared by MCU.
RTS_REG	[6]	R/W	1'h0	When UART_SFCTL[1] is 0 and UART_CTL1[7] is 0, the rtsn signal is controlled by RTS_REG bit 0: rtsn is high 1: rtsn is low
STOP_BIT_NUM	[5:4]	R/W	2'h3	0: unused, 1: 1stop bit, 2: 1.5 stop bits, 3: 2 stop bits.
BYTE_LEN	[3:2]	R/W	2'h3	data byte length. 0: 5 bits, 1: 6 bits, 2: 7 bits, 3: 8 bits.
PARITY_EN	[1]	R/W	1'h0	0: parity disabled 1: parity enabled
ODD_PARITY	[0]	R/W	1'h0	0: even parity 1: odd parity

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.2.5.2.8 **UART_CTRL1**

Description：UART control register

0x001C			Control register (0x0000_0000)													UART_CTRL1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DMA_EN	LOOP_BACK	RX_TOUT_THLD					TX_HW_FLOW_EN	RCV_HW_FLOW_EN	RCV_HW_FLOW_THLD						
Type	R/W	R/W	R/W					R/W	R/W	R/W						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
DMA_EN	[15]	R/W	1'h0	"1" enable DMA access UART FIFOs
LOOP_BACK	[14]	R/W	1'h0	Self test mode, TX input to RX
RX_TOUT_THLD	[13:9]	R/W	5'h0	Receive timeout threshold Receive time cycle num = RX_TOUT_THLD * UART_CKD * 8
TX_HW_FLOW_EN	[8]	R/W	1'h0	Transmit_Hardware_Flow_Control_Enable "1" enable transmit hardware flow control "0" disable
RCV_HW_FLOW_EN	[7]	R/W	1'h0	Receive_Hardware_Flow_Control_Enable "1" enable receive hardware flow control "0" disable
RCV_HW_FLOW_THLD	[6:0]	R/W	6'h0	Receive_Hardware_Flow_Control_Threshold When RCV_HW_FLOW_EN is enabled, if the number of unread bytes in the RX FIFO is greater than the receive hardware flow control threshold value, the RTSN is set to high to stop the remote TX.

6.2.5.2.9 **UART_CTRL2**

Description：UART TX FIFO empty and RX FIFO full watermark register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0020			Control register (0x0000_0008)													UART_CTRL2
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	TXF_EMPTY_THLD							Reserved	RXF_FULL_THLD						
Type	RO	R/W							RO	R/W						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_EMPTY_THLD	[14:8]	R/W	5'h0	TX FIFO data empty threshold
Reserved	[7]	RO	1'h0	
RXF_FULL_THLD	[6:0]	R/W	5'h8	RX FIFO data full threshold

6.2.5.2.10 **UART_CKD0**

Description : This register is used to configure baud rate

0x0024			Divisor register (0x0000_054A)													SCFG0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	UART_CKD0															
Type	R/W															
Reset	0	0	0	0	0	1	0	1	0	1	0	0	1	0	1	0

Field Name	Bit	R/W	Reset Value	Description
UART_CKD0	[15:0]	R/W	16'h54A	Clock divisor bit 0 to 15

6.2.5.2.11 **UART_STS2**

Description : UART interrupt mask status

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x002C			INT mask status (0x0000_0000)										UART_STS2			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		TIME_OUT_MASK_STS	Reserved					BRK_DTCT_MASK_STS	CTS_CHG_MASK_STS	DSR_CHG_MASK_STS	RXF_OVERRUN_MASK_STS	FRAME_ERR_MASK_STS	PARITY_ERR_MASK_STS	TXF_EMPTY_MASK_STS	RXF_FULL_MASK_STS
Type	RO		RO	RO					RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TIME_OUT_MASK_STS	[13]	RO	1'h0	Time out interrupt mask status
Reserved	[12:8]	RO	5'h0	
BRK_DTCT_MASK_STS	[7]	RO	1'h0	Break detect interrupt mask status
CTS_CHG_MASK_STS	[6]	RO	1'h0	CTS change interrupt mask status
DSR_CHG_MASK_STS	[5]	RO	1'h0	DSR change interrupt mask status
RXF_OVERRUN_MASK_STS	[4]	RO	1'h0	RX FIFO overrun interrupt mask status
FRAME_ERR_MASK_STS	[3]	RO	1'h0	Frame error interrupt mask status
PARITY_ERR_MASK_STS	[2]	RO	1'h0	Parity error interrupt mask status
TXF_EMPTY_MASK_STS	[1]	RO	1'h0	TX FIFO empty interrupt enable
RXF_FULL_MASK_STS	[0]	RO	1'h0	RX FIFO full interrupt mask status

6.2.5.2.12 **UART_DSPWAIT**

Description：UART control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0030			Control register (0x0000_0001)												UART_DSPWAIT	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										TX_DMA_MOD_SEL	RX_DMA_MOD_SEL	UART_DSPWAIT			
Type	RO										R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Field Name	Bit	R/W	Reset Value	Description
TX_DMA_MOD_SEL	[5]	R/W	1'h0	0: tx_dma_req keep 1 until receiving the rx_dma_ack 1: tx_dma_req is "1" when rx_full is "1",else "0"
RX_DMA_MOD_SEL	[4]	R/W	1'h0	0: rx_dma_req keep 1 until receiving the rx_dma_ack 1: rx_dma_req is "1" when rx_full is "1",else "0"
UART_DSPWAIT	[3:0]	R/W	4'h1	This register is used for DSP control

6.2.5.2.13 **UART_SFCTL**

Desciption : UART software flow control function configuration register

0x0034			UART SFCTL register(0x0000_0000)												UART_SFCTL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														SW_FCTL_EN	SW_FCTL_MODE
Type	RO														R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
SW_FCTL_EN	[1]	R/W	1'h0	"0" : Disable software flow control "1" : Enable software flow

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				control
SW_FCTL_MODE	[0]	R/W	1'h0	"0" software flow control mode 0 "1" software flow control mode 1

6.2.5.2.14 **UART_XCMD**

Desciption : UART XCMD command configuration register

0x0038			UART XCMD register(0x0000_1113)												UART_XCMD	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	UART_XON								UART_XOFF							
Type	R/W								R/W							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	1

Field Name	Bit	R/W	Reset Value	Description
UART_XON	[15:8]	R/W	8'h11	The XON command configuration value
UART_XOFF	[7:0]	R/W	8'h13	The XOFF command configuration value

6.2.5.2.15 **UART_ESCAPE**

Desciption : UART ESCAPE command configuration register

0x003C			UART ESCAPE register(0x0000_0077)												UART_ESCAPE	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								UART_ESCAPE							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1

Field Name	Bit	R/W	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

UART_ESCAPE	[7:0]	R/W	8'h13	The ESCAPE command configuration value

6.2.6 Application notes

Including RAM input and output formats, special requirement, software control flow, description, etc.

Working in UART mode with hardware flow control (full duplex)

1. The initiator writes to the setup register (global register)
2. The initiator writes the UART_CTL0 register bit 15 to "0" to enable UART mode.
3. The initiator configures UART_CKD0 registers to generate the suitable baud rate. For example, if clk_uart is 26 MHz, UART_CKD0 is set to 0xe1, then the UART baud rate is 115 k.
4. The initiator configures UART_CTL0 to generate the suitable data format, such as parity enable and parity style, byte length, and stop bit number
5. Set UART_CTL0 register bit 7 to "1" to enable receive hardware flow control
6. The initiator configures UART_CTL1 register bit [5:0] to suitable value
7. Set UART_CTL0 register bit 8 to "1" to enable transmit hardware flow control
8. The initiator configures UART_CTL2 to generate receive watermark and transmit watermark
9. The initiator writes UART_CTL1 register to configure receive timeout value
10. Enable related interrupts by writing UART_STS2 register
11. Writing data to UART_TXD

Once the TX FIFO is not empty:

12. data in TX FIFO will appear on TX line in sequence
13. If data number in the TX FIFO is less than the data empty threshold value, a txf_empty interrupt will be generated. After receiving this interrupt, MCU should clear the interrupt and write more data into the TX FIFO
14. If data number in the RX FIFO is more than the data full threshold value. An rxf_full interrupt will be generated. After receiving this interrupt, MCU should clear the interrupt and read data from RX FIFO
15. If receiving RX_TOUT interrupt, read all data in the RX FIFO

When the transmission is completed:

16. If RX FIFO is not empty, read all data in the RX FIFO when receiving RX_TOUT interrupt
17. Disable all interrupts, disable uart_en in global register

When use the software flow control without ctsn and rtsn signal

18. The XON/XOFF/ESCAPE register should be configed before the enable of software flow control and mode selection
19. The software flow control enable bit should be configured before starting a software flow control transation

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

20. The frame length **must** be configured as 8 bit, when enable software flow control function
21. The flow control fifo deep threshold(uart_ctl1[6:0]) should be **bigger or equal** than rx_fifo full threshold(uart_ctl2[6:0])

6.3 SPI interface

SC6531 includes two spi: spi0 & spi1.

6.3.1 Overview

SPI is a serial synchronous communication interface. SPI block enables the device to interface with SPI peripherals (i.e. A/D converters, display drivers, EEPROMs etcs.) It consists of a serial shift register with serial data input, serial data output and serial shift clock. The shift clock can be selected from either an interval source or an external source. Operating the SPI with the internal clock source is called the Master mode of operation. Similarly, operating the SPI with an external shift clock is called the Slave mode of operation. SPI module support MICROWIRE/PLUS mode, sync mode , s8 mode and 3-wire mode. Only in MICROWIRE/PLUS mode, master and slave both be supported. This document defines function and configuration of SPI block.

6.3.2 Features

- Compliant with the SPI standard
- Support MICRO/PLUS mode, SYNC mode, S8 mode and 3-wire mode
- Serial clock with programmable frequency , polarity
- Wide selection of SPI word lengths ranging from 1 to 32 bits
- Two 32-word-deep FIFOs minimizes processor overhead at high data rates
- Master / slave
- data transmit or receive with MSB first or LSB first
- Transmit only/ receive only / transmit and receive mode
- For only receive mode , the length of words ready to receive form the slave can be programmed
- The intervals of two SPI frames can be programmed
- Supports DMA
- interrupts for FIFO events and transfer events
- The polarity and position of the sync can be configured
- As slave transmit phase adjustable
- TX/RX FIFO address can be reset
- Support csn input in slave mode
- Little endian default
- Supports higher speed data transfer mode for slave
- Supports 3-wire 9bits and 4-wire 8bits SPI mode for LCD interface

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.3.3 Signal description

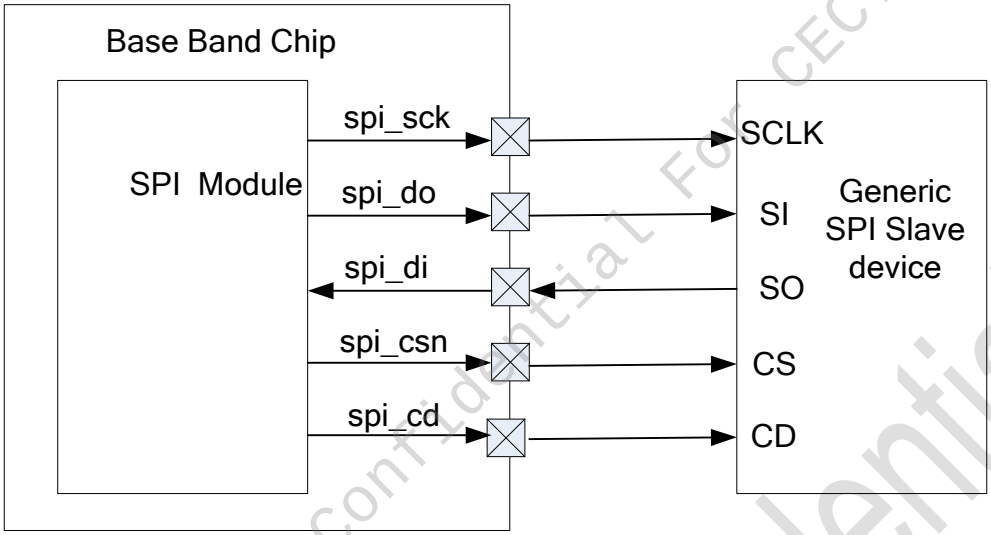


Figure 6.3-1 SPI in Master Mode(FULL-Duplex)

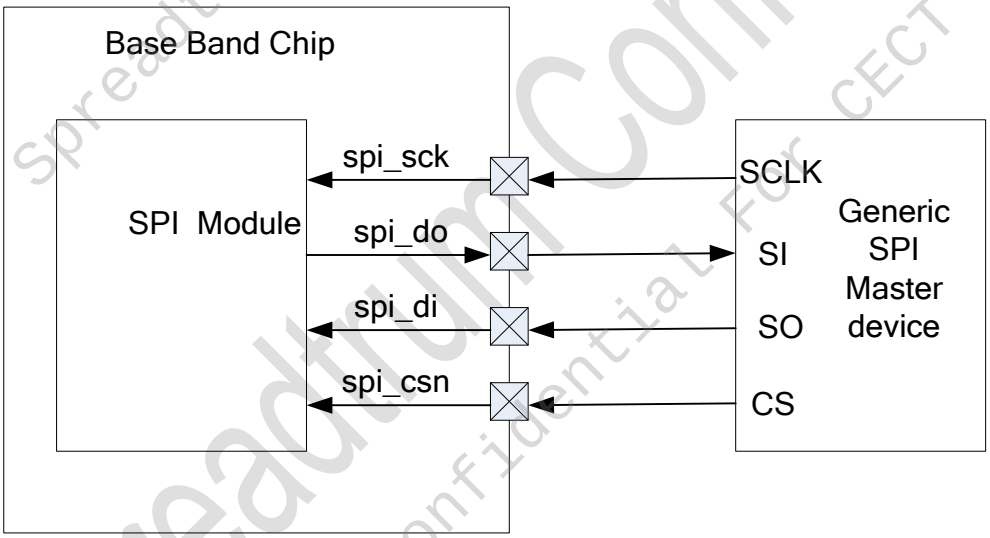


Figure 6.3-2 SPI in Slave Mode(FULL-Duplex)

6.3.4 Funtion description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

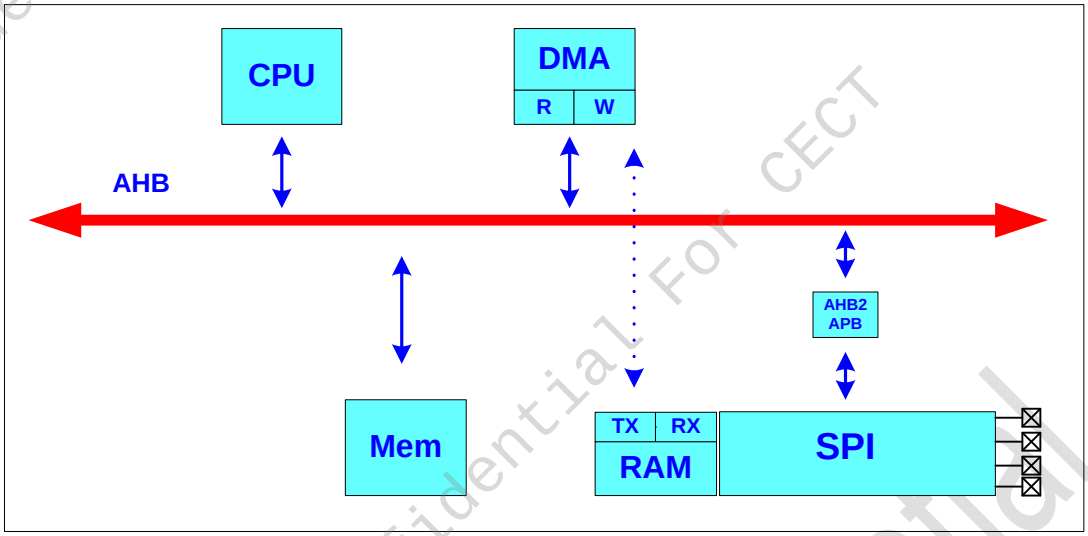


Figure 6.3-3 The Overview of SPI block

The SPI block worked as an interface to drive periphery device such as LCD. This block is controlled by CPU through AHB bus to transmission data in memory to the periphery device. Some times in order to save the resource of CPU, it will be handle by DMA(Direct Memory Access). It load data by a APB bus, and store the RX/TX data in a 2-port RAM.

SPI master mode supports communication with up to two independent SPI devices. SPI initiates a data transfer on the data lines (spi_do and spi_di) and generate clock (sck) and control signals (spi_csn).

Write data to this Spi_txd register initiates a character transmission through TX FIFO, the pointer txf_wr_address will increase. All data ready to send must be written into the TX FIFO first, then occurs in transmit line.

Data sampled from receive line is placed in RX FIFO first. When the data number in the RX FIFO is more than the receive data full threshold value, an rxf_full interrupt is generated. MCU will read data from RX FIFO as soon as receiving the interrupt.

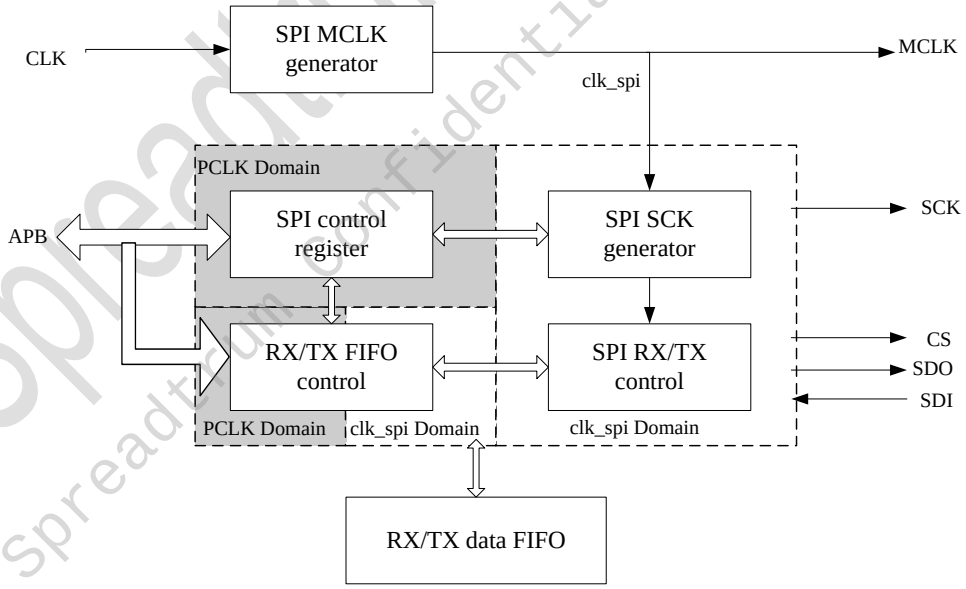


Figure 1.1-4 Diagram of SPI Master

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

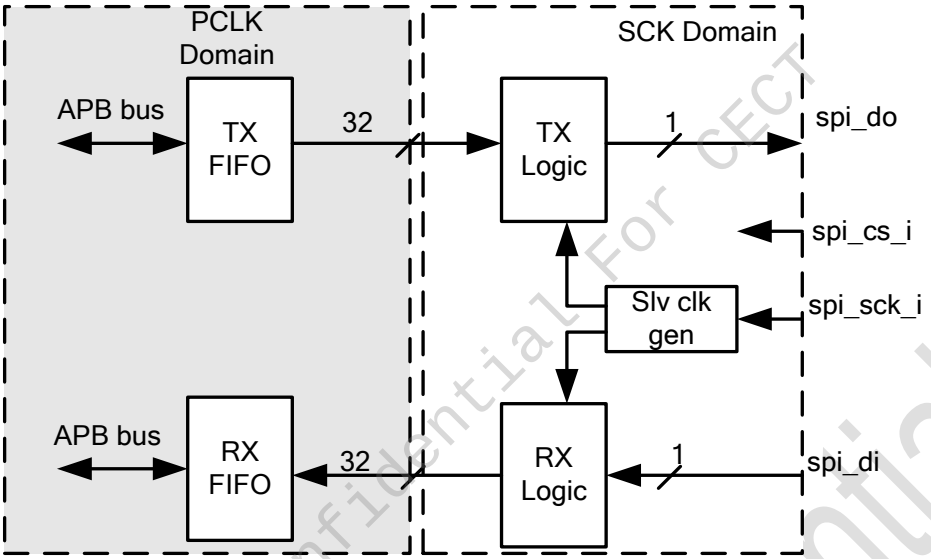


Figure 1.1-5 Diagram of SPI Slave

6.3.4.1 MICROWIRE/PLUS work mode

MICROWIRE/PLUS is an enhancement of the MICROWIRE™ synchronous serial communications scheme, originally implemented by National Semiconductor's COP400 family microcontrollers. It has three wires, SI (serial input), SO (serial output), and SK (serial clock). The input data one the SI is shifted high order first into the chip; the output data is shifted out high order first from the Most Significant Bit (MSB) on SO. The SK clock is generated internally for the master mode. One burst has 8 data bits. The input data is captured on the rising edge of SK. Following is the timing diagram.

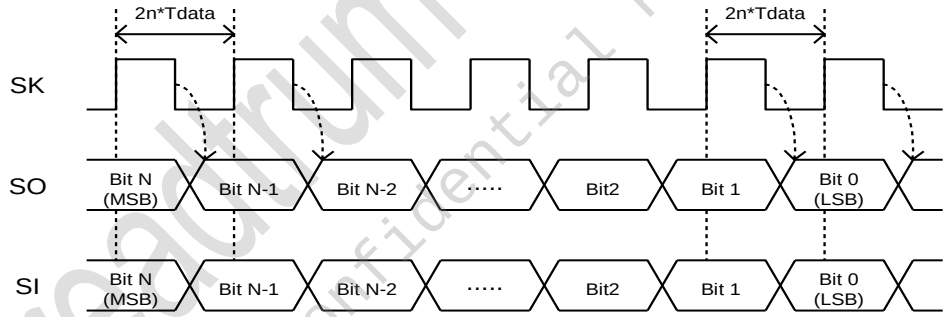
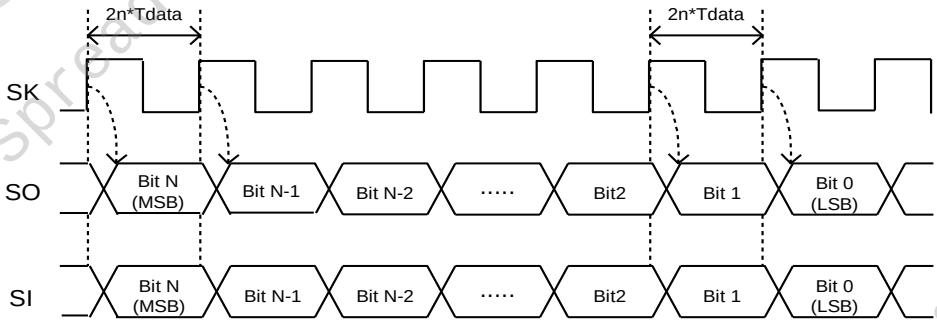


Figure 2 MICROWIRE/PLUS Timing (CPOL=0, CPHA=0)



This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Figure 3 Alternated Phase SK Clock Timing (CPOL=0, CPHA=1)

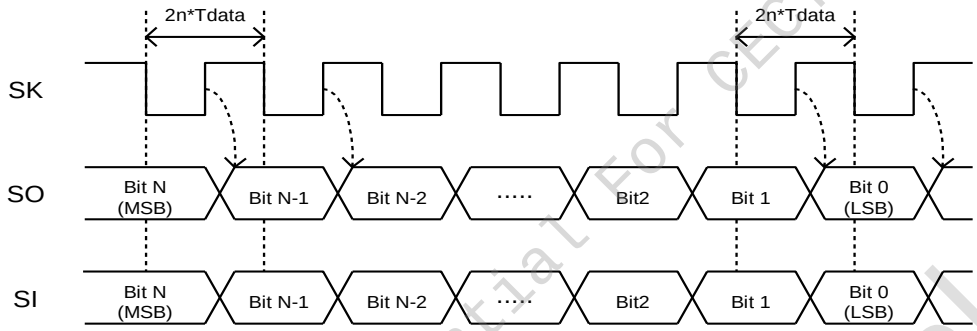


Figure 4 MICROWIRE/PLUS Timing (CPOL=1, CPHA=0)

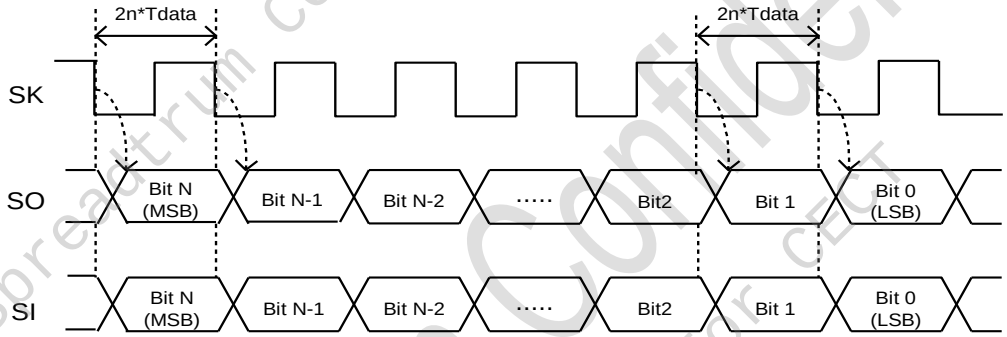


Figure 5 MICROWIRE/PLUS Timing (CPOL=1, CPHA=1)

In the normal mode data is shifted in on the rising edge of the SCK clock and data is shifted out on the falling edge of the SCK clock. It is also allow an additional Alternate SCK Phase Operation. In the alternate SCK phase operation, data is shifted in on the falling edge of the SCK clock and data is shifted out on the rising edge of the SCK clock.

To configure SPI for this mode, just enable SPI clock in global control register, program spi_ctl0 control register, enable RX data shift in at SCK rising edge(spi_ctl0[0] = 1), and enable TX data shift out at SCK falling edge(spi_ctl0[1] = 0), set transmit data bit number to 8 . Also program spi_clkd according to MCLK and SCK clock rate. Leaving other control register with default value. When put data into TX FIFO, the SPI will send and receive an N bit data at the same time.

The clock phase and TX/RX data timing is programmable to meet other requirements. For example, for:

N = 8, CS0, CPOL=0, CPHA =0 timing as Figure2, set spi_ctl0 = 0x0e22

N = 8, CS0, CPOL=0, CPHA =1 timing as Figure3, set spi_ctl0 = 0x0e21

N = 8, CS0, CPOL=1, CPHA =0 timing as Figure4, set spi_ctl0 = 0x2e22

N = 8, CS0, CPOL=1, CPHA =1 timing as Figure5, set spi_ctl0 = 0x2e21

CPOL=0 means SCK idle phase is low, maps to spi_ctl0[13] = 0;

CPOL=1 means SCK idle phase is high, maps to spi_ctl0[13]=1;

CPHA decides SPI working in normal mode or in the alternate SK phase operation.

CPHA maps to ctl0_reg[1:0],

“10” (CPHA=0) means output data at negedge of clk while receiving data at posedge of clk

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

"01"(CPHA=1)means output data at posedge of clk while receiving data at negedge of clk

"00" and "11" are not available in this mode

6.3.4.2 Synchronous SPI

Besides SCK, SDI, SDO, Synchronous SPI provides the fourth pin as a synchronous signal. It generates single bit width pulse on one of the TX/RX bit position. On slave side, it tells when to latch the received byte and prepare the next data for transmit.

If enable sync mode by setting spi_ctl0 register bit14, the sync pulse will appear on the last bit. If program spi_ctl1 register bit 4~0 to N, the sync pulse will locates on top of bit N. The SYNC bit can be program output to one of the 4 chip select pins by setting spi_ctl1[11:8].

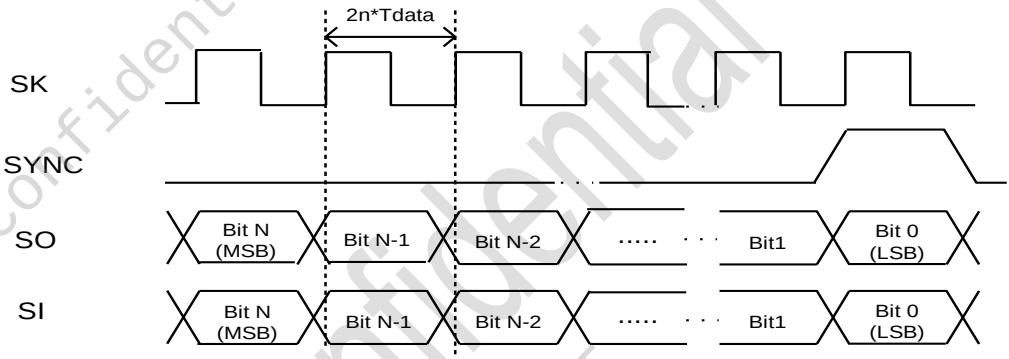


Figure 6 Alternated Phase SK Clock Timing (CPOL=0, CPHA=1)

6.3.4.3 4-wire Serial Interface(s8)

SC8800G SPI supports 4-wire serial interface, which required by LCD driver like ULTRACHIP UC1607. Only write operations are supported in this mode. Pin CS is used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. On each write cycle, 8 bits of data, MSB first, are transmitted on falling SCK edges. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data. Pin CD is examined when SCK is pulled low for the LSB(D0) of each burst. The maximum SCK frequency required is 5MHZ.

To enable SPI working in this mode, all settings are same as program MICROWIRE except to enable TX data shifting out at SCK rising edge. Also need to set spi_ctl1 control register bit7, enable s8 mode, and assign the CD signal output from one of the four CS pins by programming bit11~8. Please pay attention to not mapping CD to the same CS pin used for LCD chip select. For example using CS0 as chip select, using cs1 as CD, we should program spi_ctl0 register bit11~8 "1100" and programming spi_ctl1 register bit11~8 "0010".

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

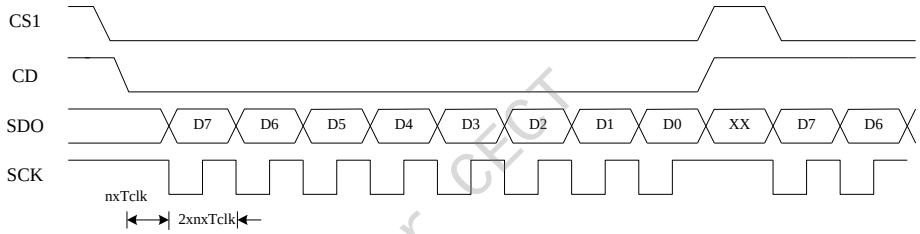


Figure 7 4-wire Serial Interface (s8) Timing

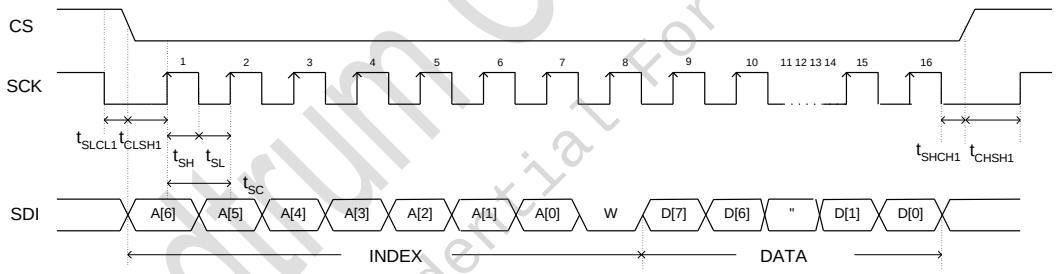
(1) SW write 9 bits data to TX FIFO while ctl0_reg[6:2]] program to 8. Bit 8 is used to control CD signal, and bit[7:0] will be used to transmit to slave.

(2) SW Set SPI_CD_BIT, this bit will be connected to SPI_CD pin, will be used to transmit to slave

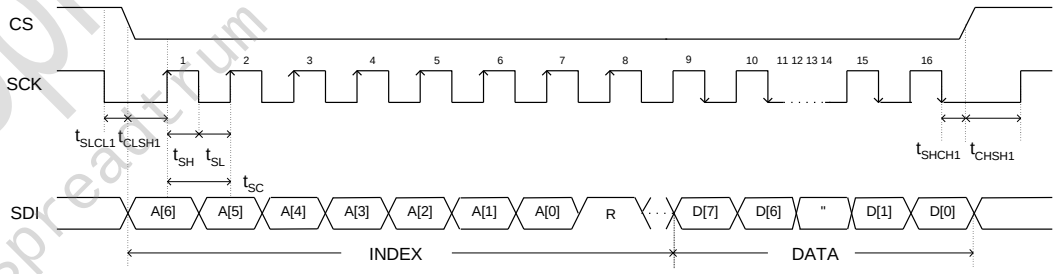
6.3.4.4 3-wire Serial interface

The 3-wire serial interface is required by Sound Generator Chips like OKIML2860. SDO works as an in/out pin because data has to be read/write through the same pin. SCK is the serial clock, output data from SDO change at clock falling edge, input data is sampled at falling edge. See Figure 8. There is also an alternate SCK phase operation, data output at clock rising edge and input data is sampled at rising edge. See Figure 12. One burst has 16 bits. 7 address bits sent first. Bit8 is command bit. “1” means writing 8 bits data to the slave. “0” means reading 8 bits data from the slave, the read data address in slave is the 7 bits address sent in the same burst.

Data Write Timing 1



Data Read Timing 1



This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Figure 8 3-wire Serial InterfaceTiming 1

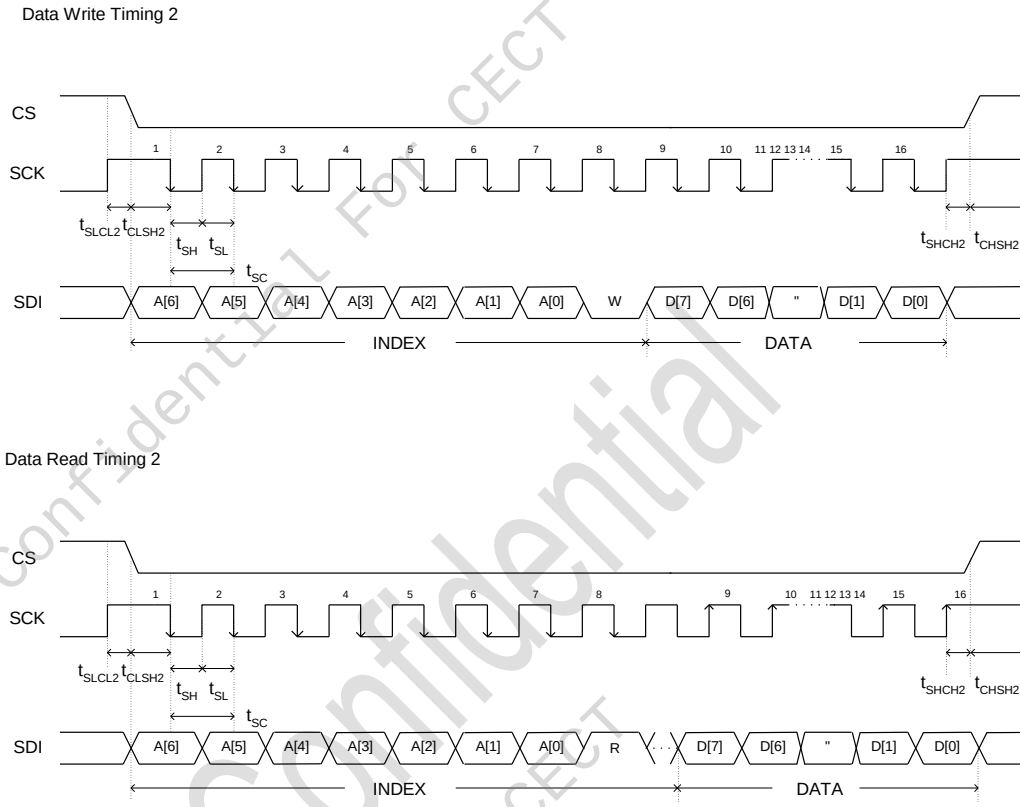


Figure 9 3-wire Serial InterfaceTiming 2

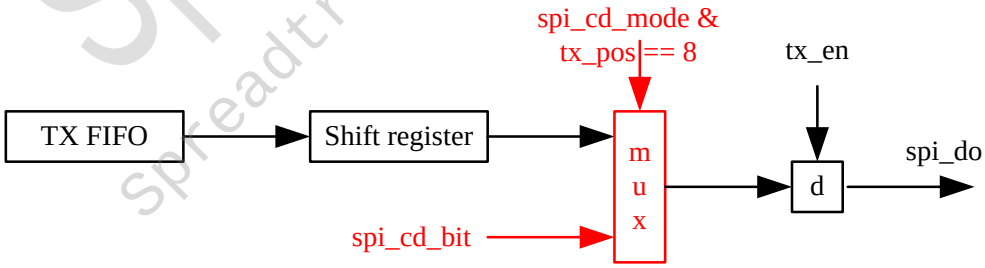
To program SPI in this mode, set spi_ctl0 control register to 0x0e43 ,means 16bits sent in one burst, TX at clock falling edge, RX sample at clock falling edge, CS maps to cs0. Set spi_ctl1 to 0x3028 , means to enable 3-wire mode, command bit is bit8. Set spi_ctl2 to 0x07 , the read data starts from bit7. Then put 16 bits data into TX FIFO, and receive 8 bit data from RX FIFO.

If set spi_ctl1 bit6 to “1”, signal CS will change to low before half cycle of the first edge of SCK, and go high after half cycle of the last edge of SCK .

To program alternate SCK phase timing as Figure 9, set spi_ctl0 bit13 to “1”, other setting are same as timing 1.

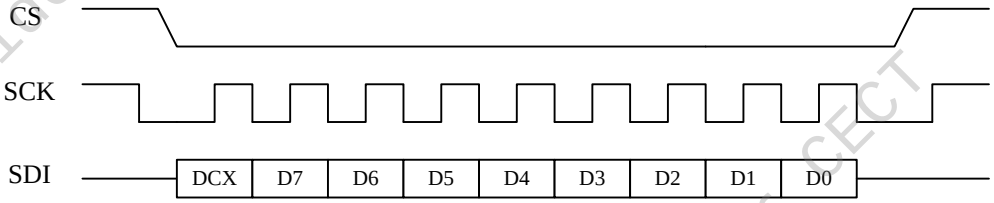
New feature:

When set spi_mode=1 / 2 , cd bit will be send out with data together ,and be put to bit 8 position.



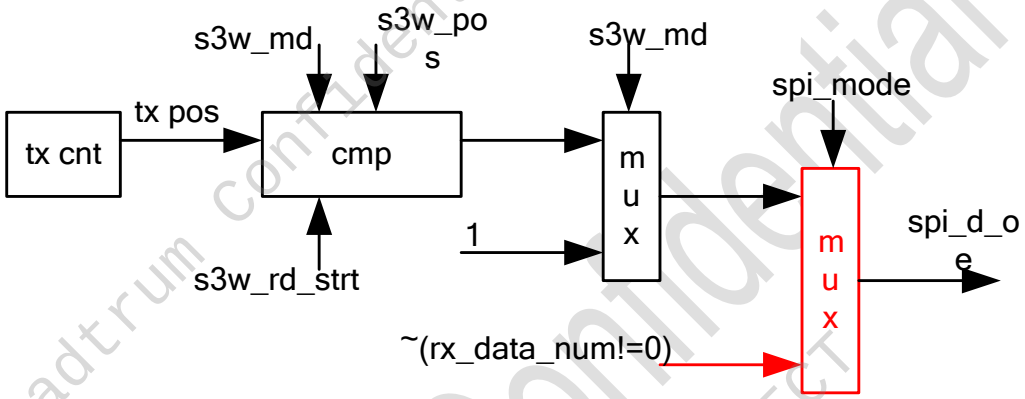
Support cd bit be transmitted with data together. Set SPI_CD_BIT, put it to bit 8 position when transmit out from tx shift register.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.



When set spi_mode = 1 / 3 , spi_d_oe is controlled by is_rx_only bit, when set is_rx_only bit, spi_d_oe is 0, and spi_d_ie is 1.

Logic description:



6.3.4.5 2-data-line Interface

GC9304 SPI supports 4-wire serial interface. And it has 4 wires, which are CS, SCK, SDA and RS.

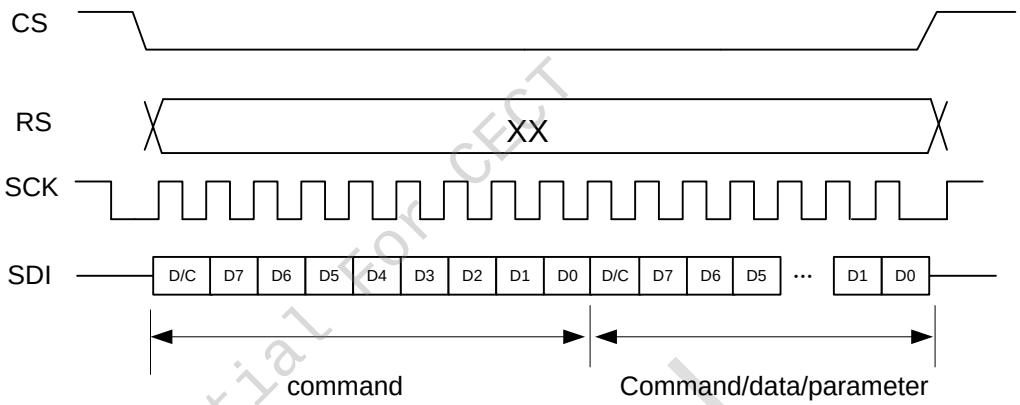
(1) Write cycle sequence:

The write mode of the interfaces means that the host writes commands or data to GC9304C. The 3-lines serial data packet contains a data/command select bit(D/CX) and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command byte. Otherwise, the transmission byte is command register as parameter.

Any instruction in transmission is the MSB is transmitted first.

Host processor drives the CS to low and starts by setting the D/CX bit on SDA. The bit is read by slave on the first rising edge of SCK. On the next falling edge of SCK, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCK, the next bit (D6) is set on SDA.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.



2-data-line interfaces of writing data Timing

The length of the transaction of a write register/command may be larger than 32 bit, and the maximum length of the transaction of the former design is 32 bit. So the transaction must be divided into 2 parts if the transaction length is larger than 32-bit. The first part is used to write the command, and the second part is used to write the command contents or data/parameter.

(2) Read cycle sequence:
The read register is used in 3-wire mode. The read mode is used to the host reads register's parameter from GC9304C. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. GC9304C latches the SDA (input data) at the rising edge of SCK. And then shifts SDA (output data) at the falling edges of SCK. After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCK of the last bit. The Read mode has three bytes of transmitted command data (8/24/32-bit) according to the command code.

When the master read the registers from the slave, it works in the 3-wire mode. The SDA pad is bi-director. And the RS is no used. But in the former design, the maximum length of a transaction is 32-bit. So the read transaction will be divided into 2 parts which is liked the write transaction. The first part is used to write the command, and second part is used to read the data and parameter. And when the first part is end, the SDA pad will became into a input pad.

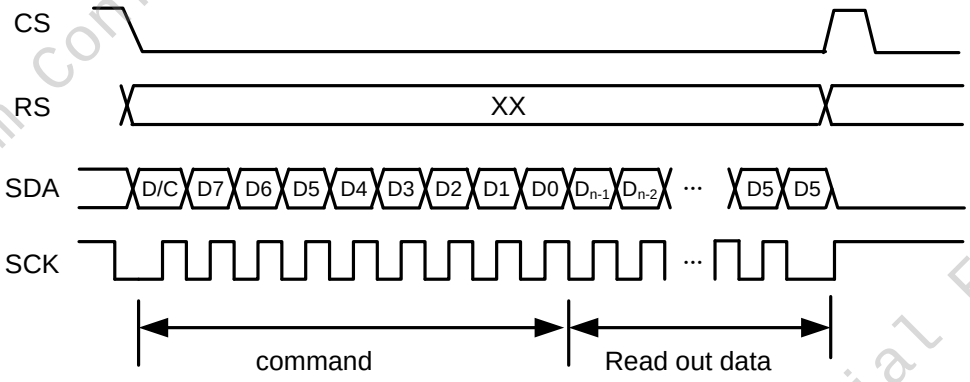


Figure 10 2-data-line interfaces of reading data Timing

In order to support this case, the design must be added 2 registers to control it. The first register is used to make the hardware work in this mode. And the second register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

is used to switch the pad direction of the SDA when the command is send in the end. If the transaction is writing, the SDA keep the status as output when the command is finished (9-bit later). And then the SPI master must changed its length register (CHNL_LEN). And the master gets the data from FIFO to send data to the slave.
If the transaction is reading, the SDA pad must be change into input status when the command is finished (9-bit later). And then the SPI master must changed its length register (CHNL_LEN) and works in only-receiver mode. And the master gets the data/parameter from the slave.
During the write/read transaction, the CSn must be kept in the low status.

(3) Write date:

Only frame pixel data write transitions are sent in this mode.

The CS enables and disables the serial interface. SCK is the serial data clock. SDA and RS are serial data lines.

Serial data must be output to SDA in the sequence A0, D15 to D8 and RS in the sequence A0, D7 to D0. The master sent the data at the falling edges of SCK. And the GC9304C reads the data at the rising edge of SCK signal. The first bit of the serial date A0 is data/command flag. It must be set to “1”, D15 to D0 bits are display RAM data.

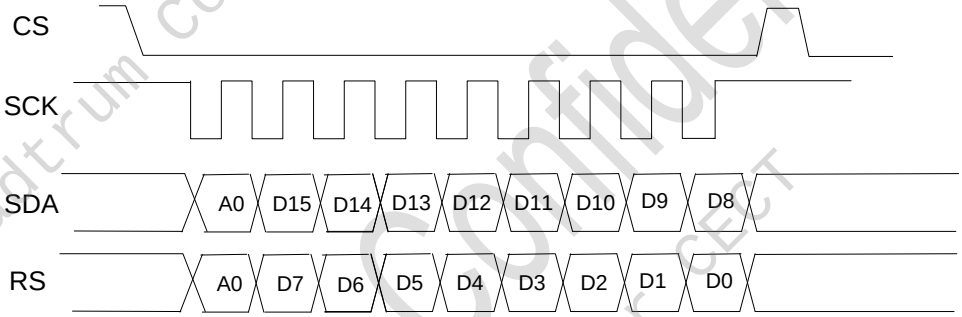


Figure 11 2-data-line interfaces of writing pixel data Timing

6.3.4.5.1 **RGB565 1pixel/transition**

The following Figure is showed that the master transmits a pixel data. It is include 5-bit R, 6-bit G and 5-bit B which follows the A0.

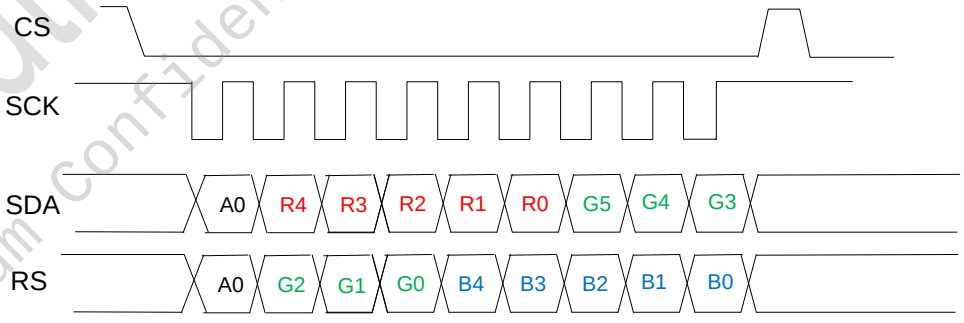


Figure 12 RGB565 1 pixel/transition

1.1.4.5.2 RGB666 1pixel/transition

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

The following Figure is showed that the master transmits a pixel data. It is include 6-bit R, 6-bit G and 6-bit B which follows the A0.

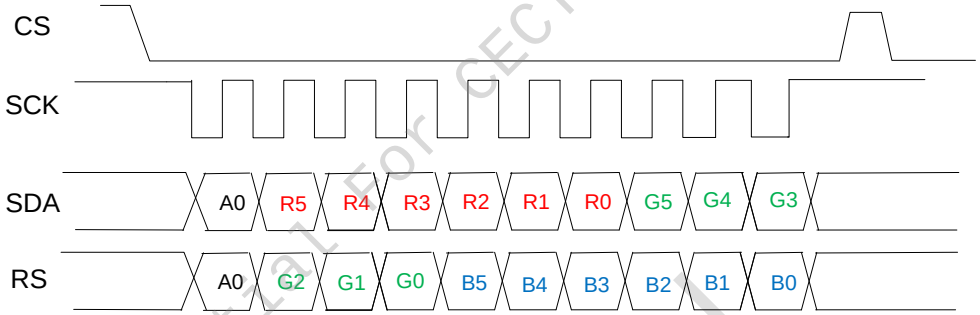


Figure 13 RGB666 1 pixel/transition

1.1.4.5.3 RGB888 1pixel/transition

The following Figure is showed that the master transmits a pixel data. It is include 8-bit R, 8-bit G and 8-bit B which follows the A0.

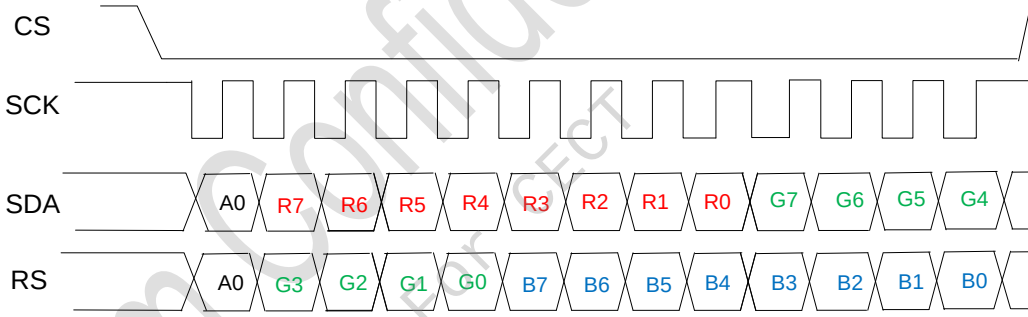


Figure 14 RGB888 1 pixel/transition

1.1.4.5.4 RGB data align before the SPI

The data which is written into the SPI TX FIFO is aligned in the below format:

1 pixel mode:

RGB888	[31:24]	[23:16]	[15:8]	[7:0]
	XX	R0	G0	B0
	XX	R1	G1	B1

RGB666	[31:24]	[23:22]	[21:16]	[15:14]	[13:8]	[7:6]	[5:0]
	XX	--	R0	--	G0	--	B0
	XX	--	R1	--	G1	--	B1

RGB565	[31:27]	[26:21]	[20:16]	[15:11]	[10:5]	[4:0]
	R0	G0	B0	R1	G1	B1
	R2	G2	B2	R3	G3	B3

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

2/3 pixel mode:

RGB888	[31:24]	[23:16]	[15:8]	[7:0]
	R1	B0	G0	R0
	G2	R2	B1	G1
	B3	G3	R3	B2

RGB666	[31:30]	[29:24]	[23:22]	[21:16]	[15:14]	[13:8]	[7:6]	[5:0]
	--	R1	--	B0	--	G0	--	R0
	--	G2	--	R2	--	B1	--	G1
	--	B3	--	G3	--	R3	--	B2

1.1.4.5.5 The design changed for 2-data-line mode in write data

When the SPI write data to the slave, there are 2 line data to transfer the data. And the maximum length is in RGB888 mode. The length is 26. And the TX FIFO is 32-bit, so we can fill the TX FIFO into two parts, the lower parts is used to stored the SDA data, and the higher parts is used to stored the RS data. When the SPI read the data from TX FIFO, and shift the read data to data lines in 2-bit once time.

The pad spi_di is the output at the same time, so we should add the spi_di_oe and spi_di_ie to control the pad (spi_di_o). And the A0 is added by HW automatically, so the spi mode should like the 3-wire 9-bit mode. The following code is showed the logic of spi_di_p.

i) Add a new signal spi_di_p for spi_di pad output

ii) Add a new signal spi_di_oe for control spi_di pad output enable

iii) Add a new signal spi_di_ie for control spi_di pad input enable

So the write data to the TX FIFO must be aligned again to following the formats which are showed from Figure 12 to Figure 14. In RGB565 mode, the APB bus will write 32-bit once time, it means there are 2 pixels are written into the FIFO. And the FIFO will shift the pixel data just in one pixel once time. So in RGB565 mode, the write FIFO should be divided into 2 parts. The first time is used to write the higher bits and the second time is used to write the lower bit.

1) RGB888

In this mode, the APB bus write 32bit into the FIFO and write data's sequence is showed as the below table:

No.	[31:24]	[23:16]	[15:8]	[7:0]
APB wdata	XX	R	G	B

So the APB bus write data should be aligned as the following format:

No.	[31:28]	[27:24]	[23:16]	[15:12]	[11:4]	[3:0]
TXFIFO wdata	XX	[11:8]	[7:0]	XX	[23:16]	[15:12]

2) RGB666

In this mode, the APB bus write 32bit into the FIFO and write data's sequence is showed as the below table:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

No.	[31:24]	[23:22]	[21:16]	[15:14]	[13:8]	[7:6]	[5:0]
APB wdata	XX	--	R0	--	G0	--	B0

So the APB bus write data should be aligned as the following format:

No.	[31:25]	[24:22]	[21:16]	[15:9]	[8:3]	[2:0]
TXFIFO wdata	XX	[10:8]	[5:0]	XX	[21:16]	[13:11]

3) RGB565

In this mode, the APB bus write 32bit into the FIFO and write data's sequence is showed as the below table:

No.	[31:27]	[26:21]	[20:16]	[15:11]	[10:5]	[4:0]
APB wdata	R0	G0	B0	R1	G1	B1

So the APB bus write data should be aligned as the following format:

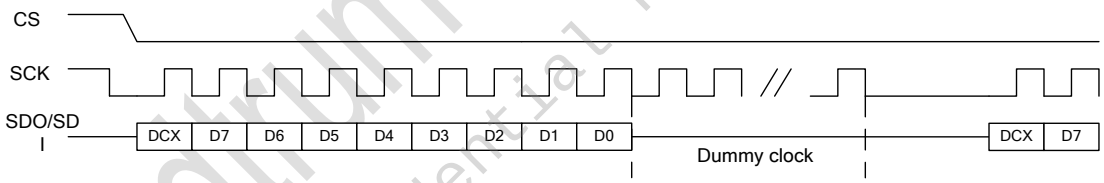
No.	[31:24]	[23:21]	[20:16]	[15:8]	[7:3]	[2:0]
TXFIFO wdata0	XX	[23:21]	[20:16]	XX	[31:27]	[26:24]
TXFIFO wdata1	XX	[7:5]	[4:0]	XX	[15:11]	[10:8]

In this mode, if the APB writes one time into SPI, and the SPI TX FIFO must be written two times.

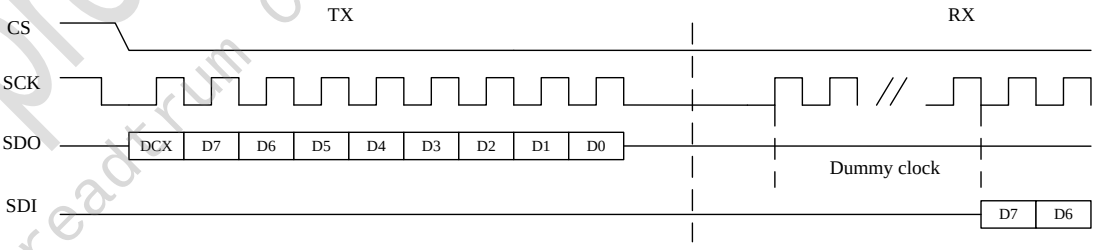
6.3.4.6 Dummy control

SPI controller supports write and read configurable dummy clocks.

For TX mode, dummy clock number is controlled by SPI_TX_DUMY_LEN, which set dummy clock number when write LCD。



For Rx mode, dummy clock number is controlled by SPI_RX_DUMY_LEN, which set dummy clock number when read LCD.

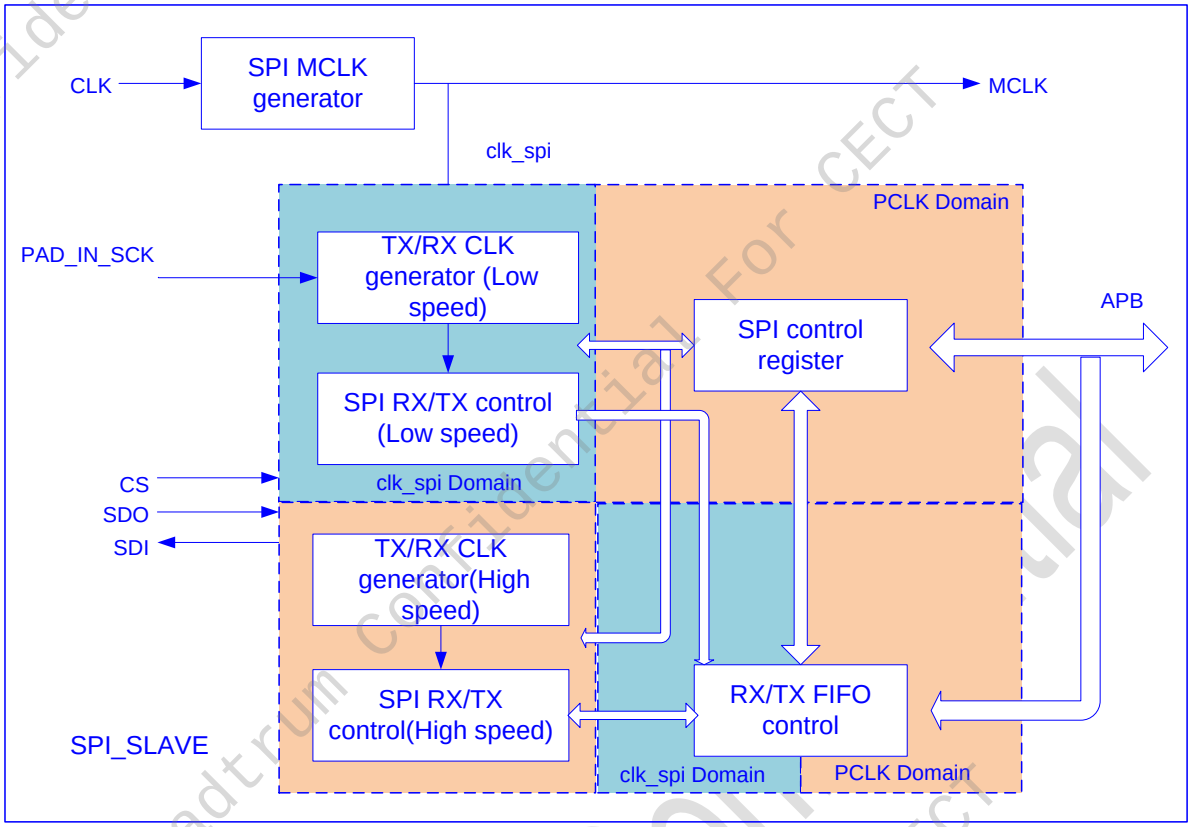


6.3.4.7 SPI Slave Design

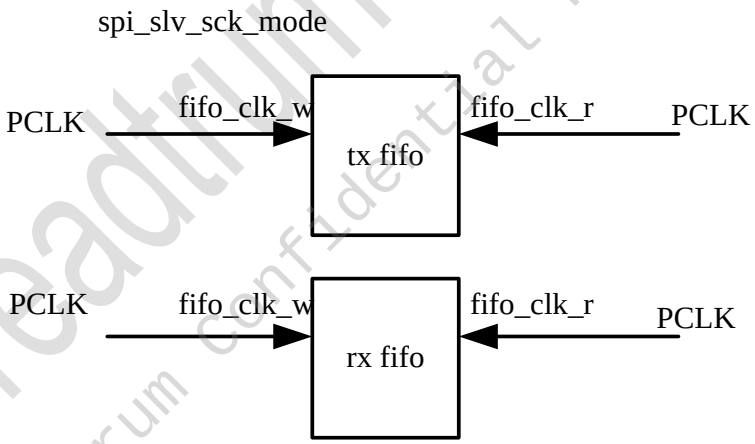
6.3.4.7.1 SPI Slave Architecture

The SPI slave can work in normal mode or high speed mode, they work in different clock domain and configure by register file block

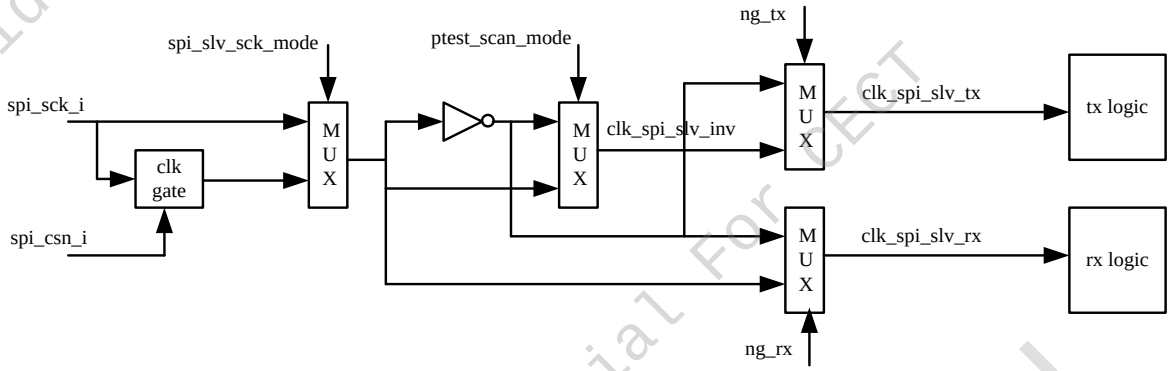
This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.



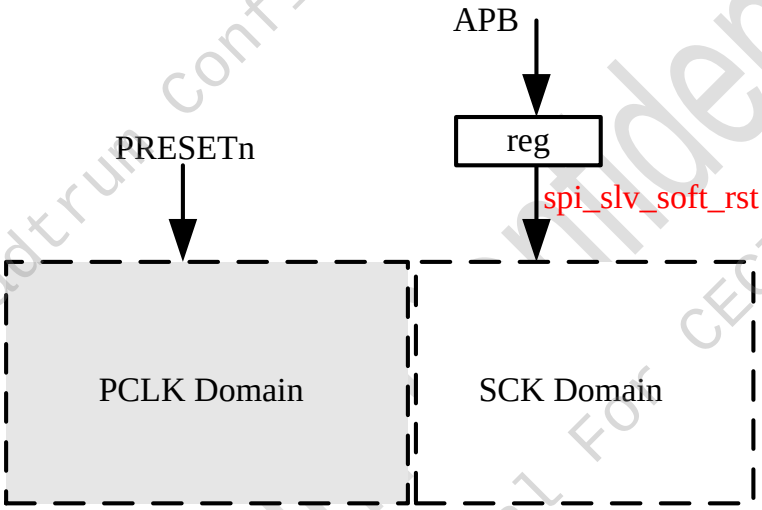
6.3.4.7.2 **SPI Slave Clock**



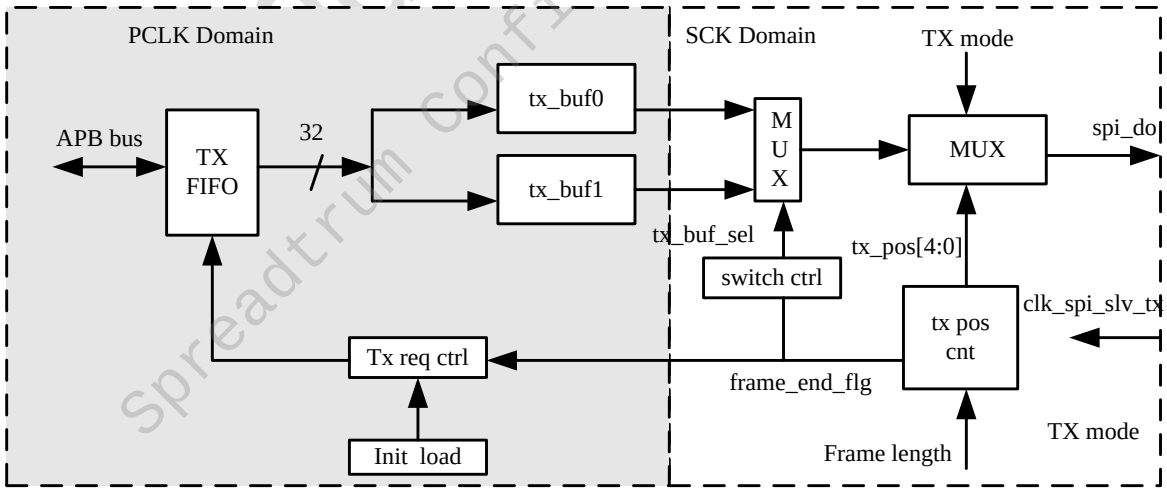
This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.



6.3.4.7.3 SPI Slave Reset



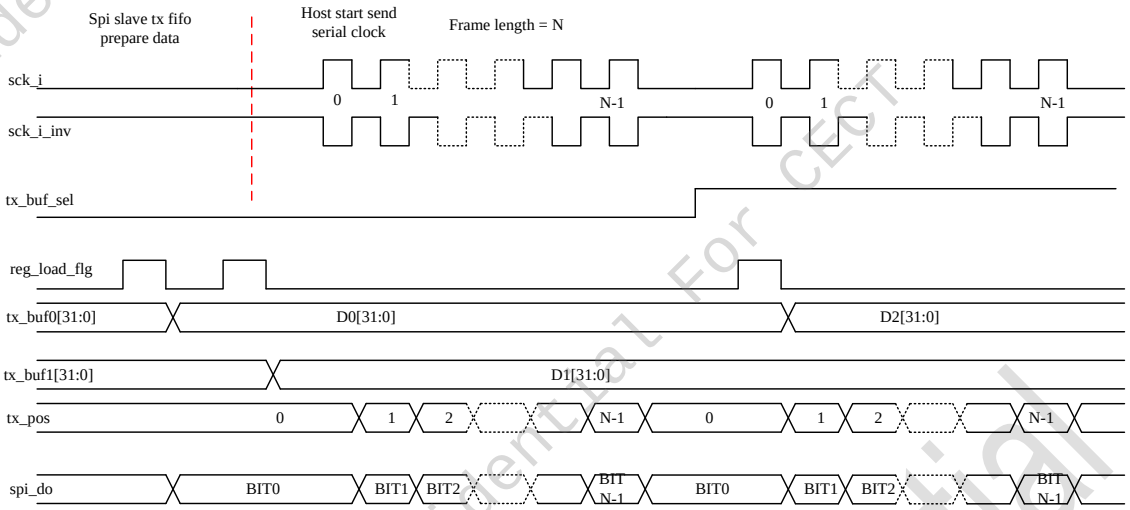
6.3.4.7.4 SPI Slave TX



TX logic structure

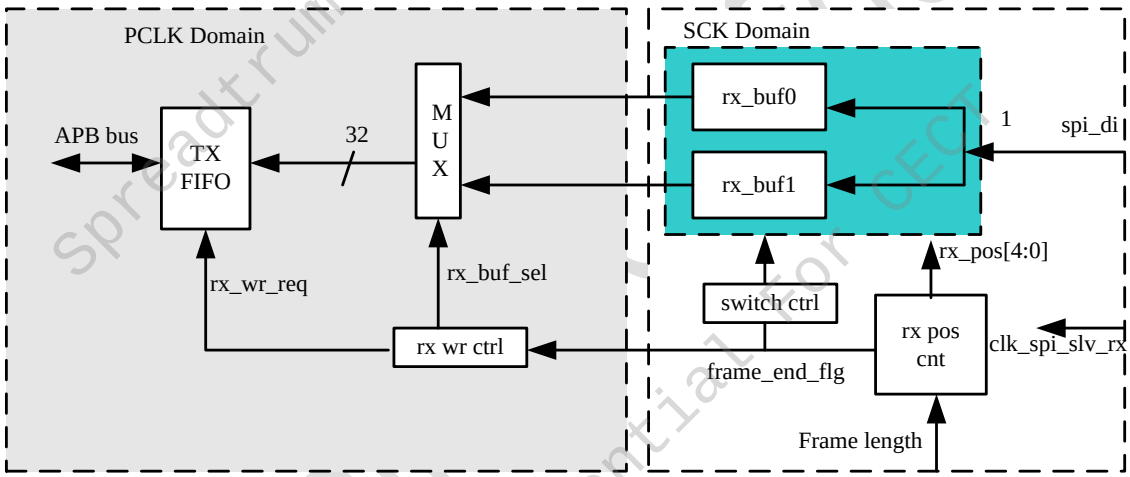
- After TX FIFO ready data, load TX FIFO data to tx_buf0 and tx_buf1
- Waiting master send serial clock to slave

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.



TX timing chart

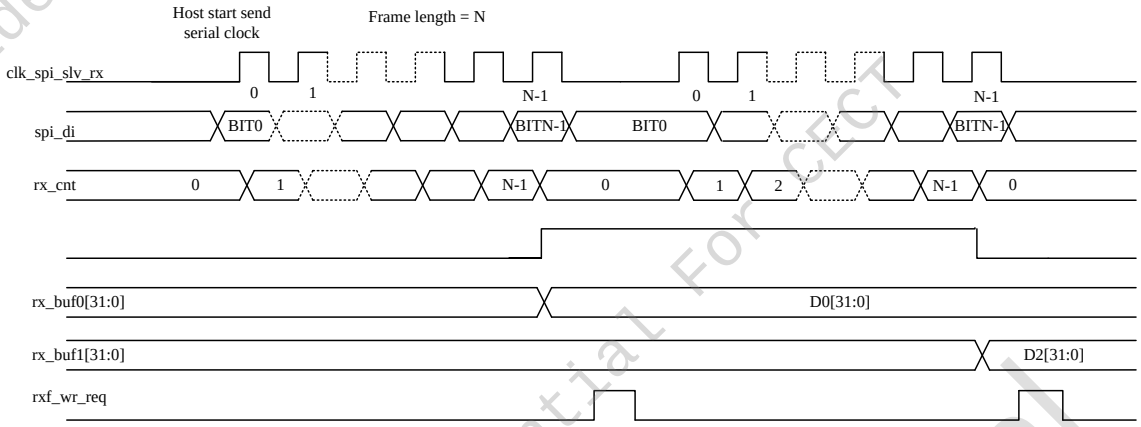
6.3.4.7.5 **SPI Slave RX**



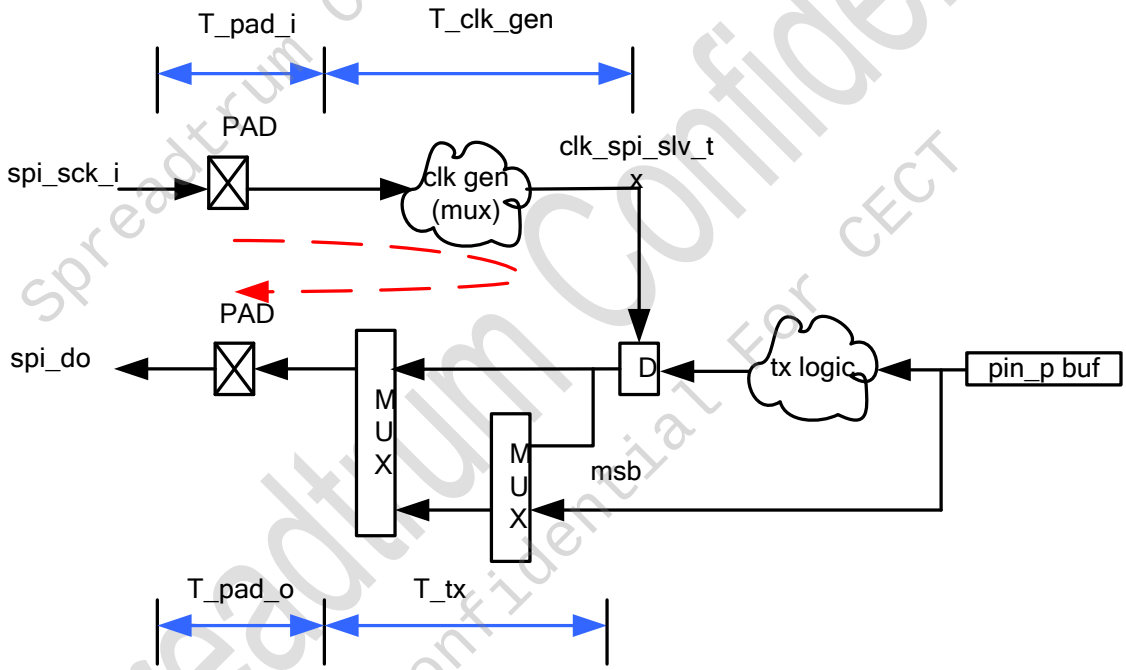
RX Logic structure

- According to SPI interface timing mode requirements , clock generator generates clk_spi_slv_rx
- Rx pos counter count clk_spi_slv_rx, generating rx_buf_sel signal during the last clock per frame. If rx_buf_sel=0, sample the serial data input to rx_buf0, otherwise sample to rx_buf1.
- Synchronize the rx_buf_sel signal to PCLK domain, get the edge , and generate rx_wr_req. fetch data from rx_buf0, write to FIFO during the rising edge , and rx_buf1 during the falling edge.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

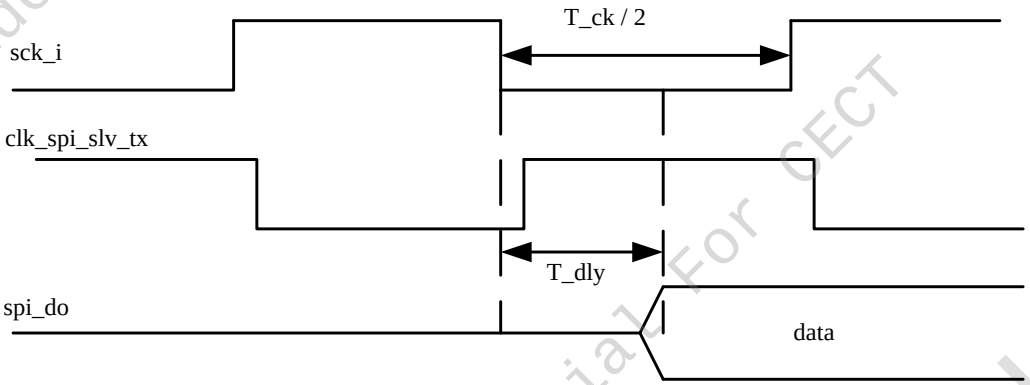


6.3.4.7.6 SPI Slave Timing



When TX transmission mode, loop timing delay from sck in to spi_do is : T_dly = T_pad_i + T_clk_gen + T_tx + T_pad_o. according to SPI timing requirement, send data during rising edge of SCK, and sample data during falling edge of SCK. Otherwise, send data during falling edge of SCK, and sampling data during rising edge of SCK, so, timing should satisfied T_ck /2 – T_dly > T_setup.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.



6.3.5 Control registers

6.3.5.1 Memory map

ARM base address: 0x8e00_2000

Offset Address	Name	Description (detail of abbreviation of this control register)
0x0000	SPI_TXD	Write data to this address initiates a character transmission through tx FIFO Read this address retrieve data from rx fifo
0x0004	SPI_CLKD	Clock divider bit 0 to 15. Divider is (n+1)*2
0x0008	SPI_CTL0	SPI control register
0x000C	SPI_CTL1	SPI control register
0x0010	SPI_CTL2	SPI control register
0x0014	SPI_CTL3	SPI control register
0x0018	SPI_CTL4	SPI control register
0x001C	SPI_CTL5	SPI control register
0x0020	SPI_INT_EN	SPI interrupt enable register
0x0024	SPI_INT_CLR	SPI interrupt clear register
0x0028	SPI_INT_RAW_STS	SPI interrupt raw status
0x002C	SPI_INT_MASK_STS	SPI interrupt mask status
0x0030	SPI_STS1	SPI status register
0x0034	SPI_STS2	SPI status register
0x0038	DSP_WAIT	Used for DSP control
0x003C	SPI_STS3	SPI status register
0x0040	SPI_CTL6	SPI control register
0x0044	SPI_STS4	SPI status register
0x0048	SPI_FIFO_RST	SPI RX/TX FIFO reset bit
0x004C	SPI_CTL7	SPI control register
0x0050	SPI_STS5	SPI status register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description (detail of abbreviation of this control register)
0x0054	SPI_CTL8	SPI tx data control for LCD
0x0058	SPI_CTL9	Spi tx data control for LCD
0x005C	SPI_CTL10	Spi rx data control for LCD
0x0060	SPI_CTL11	Spi rx data control for LCD
0x0064	SPI_CTL12	Spi rx /tx soft request
0x0068	SPI_STS6	tx_data_cnt[15:0]
0x006C	SPI_STS7	{tx_dummy_cnt[5:0], 6'd0,tx_data_cnt[19:16]}
0x0070	SPI_STS8	rx_data_cnt[15:0]
0x0074	SPI_STS9	{rx_dummy_cnt[5:0], 6'd0,rx_data_cnt[19:16]}

6.3.5.2 Register description

6.3.5.3 SPI_TXD

Description：Transmit word or Receive word

0x0000			RTX register (Reset 0x0000_0000)										SPI_TXD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	SPI_TXD															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SPI_TXD															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
SPI_TXD	[31:0]	W/O	32'h0	Write data to this address initiates a character transmission through TX FIFO Read from this address retrieve data from RX FIFO

6.3.5.4 SPI_CLKD

Description：Clock divisor bit 0 to 15

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0004			Clock divisor (Reset 0x0000_0003)													SPI_CLKD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SPI_CLKD															
Type	SPI_CLKD															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Field Name	Bit	Type	Reset Value	Description
SPI_CLKD	[15:0]	R/W	16'h3	Specify the clock ratio between spi_sck and clk_spi. If clk_spi runs at 48 MHz, and spi_sck runs at 12MHz, SPI_CLKD should be 1, spi_sck = clk_spi/2(n+1).

Note:

When work in the slave mode, the frequency of spi_sck depends on the SPI master, so the register SPI_CLKD is not used .

6.3.5.5 SPI_CTL0

Description：This register is used to configuration of the SPI interface

0x0008			Configure register (Reset 0x0000_0F02)													SPI_CTL0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SYNC_POL	SYNC_MD	SCK_REV	Reserved	SPI_CSN_PRE				LSB	CHNL_LEN					NG_TX	NG_RX
Type	R/W	R/W	R/W	RO	R/W				R/W	R/W					R/W	R/W
Reset	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	0

Field Name	Bit	R/W	Reset Value	Description
SYNC_POL	[15]	R/W	1'h0	Sync_polarity, positive or negative pulse for SPI or 3-wire mode ,read command polarity
SYNC_MD	[14]	R/W	1'h0	"1" : sync mode
SCK_REV	[13]	R/W	1'h0	"1" : spi_sck reverse

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reserved	[12]	RO	1'h0	
SPI_CSN_PRE	[11:8]	R/W	4'hf	4 bit chip select. There are totally 4 chip selects for SPI "1110": cs0 is valid "1101": cs1 is valid ……
LSB	[7]	R/W	1'h0	In default, The input data is shifted high order first into the chip; the output data is shifted out high order first from the Most Significant Bit (MSB) on SO. When this bit is set, the data will be shift out or in from the LSB
CHNL_LEN	[6:2]	R/W	1'h0	Transmit data bit number. "0" : 32 bits per word "1" : 1 bits per word … "31": 31 bits per word
NG_TX	[1]	R/W	1'h1	"1" enable TX data shift out at clock neg-edge
NG_RX	[0]	R/W	1'h0	"1" enable RX data shift in at clock neg-edge

6.3.5.6 SPI_CTL1

Description：This register is used to configuration of the SPI interface

0x000C			Configure register (Reset 0x0000_3000)												SPI_CTL1	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		RTX_MD		SYN_CSN_SEL				S8_MD	CS_H_MD	S3W_MD	S3W_POS				
Type	RO		R/W		R/W				R/W	R/W	R/W	R/W				
Reset	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:14]	RO	2'h0	
RTX_MD	[13:12]	R/W	2'h3	"00" : idle mode "01" : receive mode "10" : transmit mode "11" : transmit and receive

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SYN_CSN_SEL	[11:8]	R/W	4'h0	S8 CD or SYNC signal maps to csn number "0x0001" selects csn0 as cd signal "0x0010" selects csn1 as cd signal …
S8_MD	[7]	R/W	1'h0	"1" : enable S8 mode
CS_H_MD	[6]	R/W	1'h0	3-wire Melody timing 1, csn high mode enable
S3W_MD	[5]	R/W	1'h0	"1" : enable 3-wire mode
S3W_POS	[4:0]	R/W	5'h0	3-wire mode, w/r control position or the sync pulse position(the pulse will locates on top of bit N)

6.3.5.7 SPI_CTL2

Description：This register is used to configuration of the SPI interface

0x0010	Configure register (Reset 0x0000_0000)														SPI_CTL2	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						TX_DMA_SEL	RX_DMA_SEL	RX_ONLY_HLD	DMA_EN	IS_SLVD	S3W_RD_STRT				
Type	RO						R/W	R/W	R/W	R/W	R/W	R/W				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:11]	RO	6'h0	
DMA_REQ_SEL_SEL	[10]	RW	1'b0	0:DMA TX and RX REQ independent 1:DMA TX REQ are depended on RX REQ status
TX_DMA_SEL	[9]	R/W	1'h0	0: tx_dma_req keep 1 until receiving the tx_dma_ack 1: tx_dma_req is "1" when tx_empty is "1",else "0"
RX_DMA_SEL	[8]	R/W	1'h0	0: rx_dma_req keep 1 until receiving the rx_dma_ack 1: rx_dma_req is "1" when

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				rx_full is “1”,else “0”
RX_ONLY_HLD	[7]	R/W	1’h0	“0” : working on only receive mode, when rxf_realfull is high, SPI will be held until rxf_realfull is low “1” : no holding
DMA_EN	[6]	R/W	1’h0	“1” enable DMA mode
IS_SLVD	[5]	R/W	1’h0	“0” : master “1” : slave, only support microplus mode
S3W_RD_STRT	[4:0]	R/W	5’h0	Read data start bit, used for 3 wire mode and 3 wire 9bit RW mode. The 3 wire 9bit RW mode reuse this config registers, it indicated read data start position.

6.3.5.8 SPI_CTL3

Description：SPI RX FIFO FULL/EMPTY watermark

0x0014	RXF watermark (Reset 0x0000_1010)														SPI_CTL3	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			RXF_EMPTY_THLD					Reserved			RXF_FULL_THLD				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
RXF_EMPTY_THLD	[12:8]	R/W	5’h10	Receive FIFO data empty threshold. Relative with rx_fifo_empty interrupt
Reserved	[7:5]	RO	3’h0	
RXF_FULL_THLD	[4:0]	R/W	5’h10	Receive FIFO data full threshold. Relative with rx_fifo_full interrupt

6.3.5.9 SPI_CTL4

Description：This register is used to configuration of the SPI interface

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0018			Configure register (Reset 0x0000_0000)													SPI_CTL4
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RX_ONLY_DO	IS_FST	PHS_DLY		SYNC_CLKMASK	SYNC_HALF	IS_RX_ONLY	BLOCK_NUM								
Type	R/W	R/W	R/W		R/W	R/W	R/W	R/W								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
RX_ONLY_DO	[15]	R/W	1'h0	working in only receive mode, "0" : SPI send all 0 to slave "1" : SPI send all 1 to slave
IS_FST	[14]	R/W	1'h0	"0" : normal mode "1" : fast mode Only used for slave mode
PHS_DLY	[13:12]	R/W	2'h0	Phase delay. Relate to fast mode. When in normal mode, this bit is not used . Only used for slave mode
SYNC_CLKMASK	[11]	R/W	1'h0	"1" Mask out the first clock pulse in SPI mode
SYNC_HALF	[10]	R/W	1'h0	Sync_half, sync width is half spi_sck cycle
IS_RX_ONLY	[9]	R/W	1'h0	"1":receive data only. The bit should be written at last. Only used for master mode
BLOCK_NUM	[8:0]	R/W	9'h0	Number of data words ready to receive in "receive only" mode. Only used for master mode.

6.3.5.10 SPI_CTL5

Description：This register is used to configuration of the SPI interface

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x001C			Configure register(Reset 0x0000_0000)													SPI_CTL5
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ITVL_NUM															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
ITVL_NUM	[15:0]	R/W	16'h0	For master, transmit data interval, programmable n from 0 to 65535, delay is (n*4+3) clock cycle. For slave, max receive data interval. If the slave has not sampled the edge of spi_clk in the interval(n*4+3), slave will stop the receive process and send timout interrupt

6.3.5.11 SPI_INT_EN

Description：SPI interrupt enable register

0x0020			Interrupt enable (Reset 0x0000_0000)													SPI_INT_EN
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						RX_END_INT_EN	TX_END_INT_EN	TXF_EMPTY_INT_EN	RXF_FULL_INT_EN	TIME_OUT_INT_EN	RX_OVF_INT_EN	Reserved	TXF_FULL_INT_EN	RXF_EMPTY_INT_EN	Reserved
Type	RO						R/W	R/W	R/W	R/W	R/W	R/W	RO	R/W	R/W	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

RX_END_INT_EN	[9]	R/W	1'h0	Rx end interrupt enable
TX_END_INT_EN	[8]	R/W	1'h0	Tx end interrupt enable
TXF_EMPTY_INT_EN	[7]	R/W	1'h0	txf_empty interrupt enable
RXF_FULL_INT_EN	[6]	R/W	1'h0	Rxf_full interrupt enable
TIME_OUT_INT_EN	[5]	R/W	1'h0	Slave mode timeout interrupt enable
RX_OVF_INT_EN	[4]	R/W	1'h0	Rx_overrun_reg interrupt enable
Reserved	[3]	RO	1'h0	
TXF_FULL_INT_EN	[2]	R/W	1'h0	Tx_fifo_full interrupt enable
RXF_EMPTY_INT_EN	[1]	R/W	1'h0	Rx_fifo_empty interrupt enable
Reserved	[0]	RO	1'h0	

6.3.5.12 SPI_INT_CLR

Description：SPI interrupt clear register

0x0024			Interrupt clear (Reset 0x0000_0000)													SPI_INT_CLR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						RX_END_INT_CLR	TX_END_INT_CLR	Reserved		TIME_OUT_INT_CLR	RX_OVF_INT_CLR	Reserved	TXF_FULL_INT_CLR	RXF_EMPTY_INT_CLR	Reserved
Type	RO						WO	WO			WO	WO	RO	WO	WO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
RX_END_INT__CLR	[9]	WO	1h0	Rx data end interrupt clear
TX_END_INT_CLR	[8]	WO	1h0	Tx data end interrupt clear
TIME_OUT_INT_CLR	[5]	WO	1'h0	Write "1" clear slave mode timeout interrupt
RX_OVF_INT_CLR	[4]	WO	1'h0	Write "1" clear Rx_overrun_reg interrupt
TXF_EMPTY_INT_CLR	[3]	WO	1'h0	Write "1" clear Tx_fifo_empty interrupt

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

TXF_FULL_INT_CLR	[2]	WO	1'h0	Write "1" clear Tx_fifo_full interrupt
RXF_EMPTY_INT_CLR	[1]	WO	1'h0	Write "1" clear Rx_fifo_empty interrupt
RXF_FULL_INT_CLR	[0]	WO	1'h0	Write "1" clear Rx_fifo_full interrupt

6.3.5.13 SPI_INT_RAW

Description：SPI interrupt raw status

0x0028	Raw status (Reset 0x0000_008A)													SPI_INT_RAW_STS		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						RX_END_IRQ	TX_END_IRQ	TXF_EMPTY_RAW_STS	RXF_FULL_RAW_STS	TIME_OUT_RAW_STS	RX_OVF_RAW_STS	TX_FIFO_EMPTY_W	TXF_FULL_RAW_STS	RXF_EMPTY_RAW_STS	RX_FIFO_FULL_R
Type	RO						RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0

Field Name	Bit	R/W	Reset Value	Description
RX_END_IRQ	[9]	RO	1`h0	Raw rx data end interrupt, this bit is set when spi controller received RX_DATA_LEN data from slave.
TX_END_IRQ	[8]	RO	1`h0	Raw tx data end interrupt,this bit is set when spi controller send TX_DATA_LEN data.
TXF_EMPTY_RAW_STS	[7]	RO	1'h1	Raw txf_empty interrupt, This bit is set when the number of tx fifo data byte is less than the tx empty watermark value. Auto cleared when the condition disappears.
RXF_FULL_RAW_STS	[6]	RO	1'h0	Raw rxf_full interrupt.This bit is set when the number of rx fifo data byte is larger than the rx full watermark value. Auto cleared when the condition disappears.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

TIME_OUT_RAW_STS	[5]	RO	1'h0	Raw slave mode time out interrupt
RX_OVF_RAW_STS	[4]	RO	1'h0	Raw Rx_overrun_reg interrupt
TX_FIFO_EMPTY_W	[3]	RO	1'h1	Txf_empty_w(for debug)
TXF_FULL_RAW_STS	[2]	RO	1'h0	Raw Tx_fifo_full interrupt
RXF_EMPTY_RAW_STS	[1]	RO	1'h1	Raw rx_fifo_empty interrupt
RX_FIFO_FULL_R	[0]	RO	1'h0	Rxf_full_r(for debug)

6.3.5.14 SPI_INT_MASK_STS

Description：IIS interrupt raw status

0x002C			Mask status (Reset 0x0000_0000)										SPI_INT_MASK_STS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						RX_END_IRQ_MASK_STS	TX_END_IRQ_MASK_STS	TXF_EMPTY_MASK_STS	RXF_FULL_MASK_STS	TIME_OUT_MASK_STS	RX_OVF_MASK_STS	Reserved	TXF_FULL_MASK_STS	RXF_EMPTY_MASK_STS	Reserved
Type	RO						RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
RX_END_IRQ_MASK_STS	[9]	RO	1`h0	Raw rx data end interrupt, this bit is set when spi controller received RX_DATA_LEN data from slave.
TX_END_IRQ_MASK_STS	[8]	RO	1`h0	Raw tx data end interrupt,this bit is set when spi controller send TX_DATA_LEN data.
TXF_EMPTY_MASK_STS	[7]	RO	1'h1	Txf_empty interrupt mask status.
RXF_FULL_MASK_STS	[6]	RO	1'h0	Rxf_full interrupt mask status.
TIME_OUT_MASK_STS	[5]	RO	1'h0	Slave mode time out

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				interrupt mask status
RX_OVF_MASK_STS	[4]	RO	1'h0	Rx_overrun_reg interrupt mask status
Reserved	[3]	RO	1'h0	
TXF_FULL_MASK_STS	[2]	RO	1'h0	Tx_fifo_full interrupt mask status
RXF_EMPTY_MASK_STS	[1]	RO	1'h1	Rx_fifo_empty interrupt mask status
Reserved	[0]	RO	1'h0	

6.3.5.15 SPI_STS1

Description：SPI RX FIFO write address and read address

0x0030			RXF address (Reset 0x0000_0000)													SPI_STS1
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			RXF_WADDR					Reserved			RXF_RADDR				
Type	RO			RO					RO			RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
RXF_WADDR	[12:8]	RO	5'h0	RX FIFO write address
Reserved	[7:5]	RO	3'h0	
RXF_RADDR	[4:0]	RO	5'h0	RX FIFO read address

6.3.5.16 SPI_STS2

Description：SPI status register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0034			Register description (Reset 0x0000_12AA)													SPI_STS2
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
SPI_CS	[12]	RO	1'h1	Spi_cs(for debug)
SPI_SCK	[11]	RO	1'h0	Spi_sck(for debug)
SPI_TXD	[10]	RO	1'h0	Spi_txd(for debug)
SPI_RXD	[9]	RO	1'h1	Spi_rxd(for debug)
BUSY	[8]	RO	1'h0	"1" transmit process "0" idle state
TXF_REAL_EMPTY	[7]	RO	1'h1	TX FIFO has no data
TXF_REAL_FULL	[6]	RO	1'h0	TX FIFO is real full. (not relates to TX full threshold)
RXF_REAL_EMPTY	[5]	RO	1'h1	RX FIFO has no data
RXF_REAL_FULL	[4]	RO	1'h0	RX FIFO is real full. (not relates to TX full threshold)
TXF_EMPTY	[3]	RO	1'h1	This bit is set when the number of TX FIFO data byte is less than the TX empty interrupt watermark value. Auto cleared when the condition disappears.
TXF_FULL	[2]	RO	1'h0	This bit is set when the number of TX FIFO data byte is larger than the TX full interrupt watermark value. Auto cleared when the condition disappears.
RXF_EMPTY	[1]	RO	1'h1	This bit is set when the number of RX FIFO data byte is less than the RX empty interrupt watermark value. Auto cleared when the condition disappears.
RXF_FULL	[0]	RO	1'h0	This bit is set when the number of RX FIFO data byte is larger than the RX full interrupt watermark value. Auto cleared when the

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				condition disappears.

6.3.5.17 SPI_DSPWAIT

Description：This register is used for DSP control

0x0038			Register description (Reset 0x0000_0001)												SPI_DSPWAIT	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												IIS_DSPWAIT			
Type	RO												R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Field Name	Bit	R/W	Reset Value	Description
SPI_TX_SWT	[7:6]	R/W	2'h0	Write data switch. 2'b0: WDATA=PDATA; 2'b1: WDATA={PDATA[7:0], PDATA[15:8], PDATA[23:16], PDATA[31:24]}; 2'b2: WDATA={PDATA[15:0],PDATA[31:16]};
SPI_RX_SWT	[5:4]	R/W	2'h0	Read data switch. 2'b0: RDATA=PDATA; 2'b1: RDATA={PDATA[7:0], PDATA[15:8], PDATA[23:16], PDATA[31:24]}; 2'b2: RDATA={PDATA[15:0],PDATA[31:16]};
SPI_DSPWAIT	[3:0]	R/W	4'h1	This register is used for DSP control

6.3.5.18 SPI_STS3

Description：This register is used to observe the status

0x003C			Register description (Reset 0x0000_0000)												SPI_STS3	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							RX_CNT								
Type	RO							RO								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Reset Value	Description
RX_CNT	[8:0]	RO	9'h0	working in only receive mode as master

6.3.5.19 SPI_CTL6

Description：This register is used to configuration of the SPI interface

0x0040	Register description (Reset 0x0000_1010)														SPI_CTL6	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			TXF_EMPTY_THLD					Reserved			TXF_FULL_THLD				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_EMPTY_THLD	[12:8]	R/W	5'h10	TX FIFO data empty threshold. Relative with rx_fifo_empty interrupt
Reserved	[7:5]	RO	3'h0	
TXF_FULL_THLD	[4:0]	R/W	5'h10	TX FIFO data full threshold. Relative with rx_fifo_full interrupt

6.3.5.20 SPI_STS4

Description：SPI status register

0x0044	Register description (Reset 0x0000_0000)														SPI_STS4	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			TXF_WADDR					Reserved			TXF_RADDR				
Type	RO			RO					RO			RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

TXF_WADDR	[12:8]	RO	5'h0	TX FIFO write address
Reserved	[7:5]	RO	3'h0	
TXF_RADDR	[4:0]	RO	5'h0	TX FIFO read address

6.3.5.21 SPI_FIFO_RST

Description：Used to reset TX/RX FIFO

0x0048	Register description (Reset 0x0000_0000)													SPI_FIFO_RST		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															SPI_FIFO_RST
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
SPI_FIFO_RST	[0]	R/W	1'h0	"1" : reset all FIFOs. FIFO address will changed to 0

6.3.5.22 SPI_CTL7

Description：This register is used to configuration of the SPI interface

0x004C	Register description (Reset 0x0000_0000)															SPI_CTL7
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DATA_LINE2_EN	RGB565_EN	RGB666_EN	RGB888_EN	SPI_SLV_SEL	SPI_SLV_EN	DATA_IN_MODE	SPI_RX_HLD_EN	SPI_TX_HLD_EN	TX_CMD_SET	SPI_MODE		CSN_I_SEL			CSN_IE_CTL
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W			R/W
Reset	0	0	0	0	0	0	0	0	0	0	0		0	0		0

Field Name	Bit	R/W	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
DATA_LINE2_EN	[15]	R/W	0	1: two data line function enable 0: two data line function disable
RGB565_EN	[14]	R/W	0	1: enable RGB565 data format 0: disable RGB565 data format
RGB666_EN	[13]	R/W	0	1: enable RGB666 data format 0: disable RGB666 data format
RGB888_EN	[12]	R/W	0	1: enable RGB888 data format 0: disable RGB888 data format
SPI_SLV_SEL	[11]	R/W	0	1: SPI slave in Low speed mode 0: SPI slave in High speed mode
SPI_SLV_EN	[10]	R/W	0	Used when SPI slave in High speed mode. 1: enable spi slave rtx 0: disable spi slave rtx
DATA_IN_MODE	[9]	R/W	1'd0	Use for 3 wire 9bit RW mode and 4 wire 8bit RW mode (SPI_MODE=5 or SPI_MODE=6). 0: Data in and data out of SPI share one IO (SDA). 1: Data in and data out of SPI use separated IO (SDI, SDO).
SPI_RX_HLD_EN	[8]	R/W	1'd0	1: enable ahb2apb bridge read hold when rx fifo empty 0: disable ahb2apb bridge read hold
SPI_TX_HLD_EN	[7]	R/W	1'd0	1: enable ahb2apb bridge write hold when tx fifo full 0: disable ahb2apb bridge write hold
TX_CMD_SET	[6]	R/W	1'd0	1: select fmark as the dma request 0: select software dma request
SPI_MODE	[5:3]	R/W	3'd0	Used for master only 0: SPI_MODE disable 1: 3 wire 9 bit, cd bit, SDI/SDO share one IO 2: 3 wire 9 bit, cd bit, SDI, SDO 3: 4 wire 8 bit, cd pin, SDI/SDO share one IO 4: 4 wire 8 bit, cd pin, SDI, SDO 5: 3 wire 9bit RW mode, 9 bit command and 8 bit read data, cd bit is enable. Design for LCD driver (GC9304C). 6: 4 wire 8bit RW mode, 8bit command and 8 bit read data. Use CD PAD indicates command or data. Design for LCD driver

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				(GC9304C).
CSN_I_SEL	[2:1]	R/W	2'h0	CSN select control: 0: CSN 0 1: CSN 1 2: CSN 2 3: CSN 3
CSN_IE_CTL	[0]	R/W	1'h0	CSN IE output set(only slave) 0: not support csn input 1: support csn intput

6.3.5.23 SPI_STS5

Description：Used to observe csn error

0x0050			Register description (Reset 0x0000_0000)													SPI_STS5
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															CSN_IN_ERR_SYNC2
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
CSN_IN_ERR_SYNC2	[0]	RO	1'h0	1: indicates csn occurring a exception

6.3.5.24 SPI_CTL8

Description：This register is used to configuration of the SPI interface

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0054			Register description (Reset 0x0000_0000)											SPI_CTL8		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SPI_CD_BIT	SPI_CD_BIT2	CD_DATA2_SEL				SPI_TX_DUMY_LEN						SPI_TX_DATA_LEN_H			
Type	R/W	R/W	R/W				R/W						R/W			
Reset	0	0	0				0						0			

	Bit	R/W	Reset Value	Description
SPI_CD_BIT	[15]	R/W	1'h0	Spi tx cd bit: 0: indicates command 1: indicates data
SPI_CD_BIT2	[14]	R/W	1'h0	Use for 4 wire 8bit RW mode. Determine CD PAD high or low in read data phase.
CD_DATA2_SEL	[13]	R/W	1'h0	Second data line of two data line function select bit: 0: DI PAD as second data line 1: CD PAD as second data line
RGB_PIX_MODE	[12]	R/W	1'h0	Two data line RGB data format mode: 0: 1pixel mode 1: 2/3 pixel mode
Reserved	[11:10]			
SPI_TX_DUMY_LEN	[9:4]	R/W	6'h0	Spi tx dummy clock length
SPI_TX_DATA_LEN_H	[3:0]	R/W	4'h0	Indicates tx data length from tx fifo, High 4 bits of spi tx data length

6.3.5.25 SPI_CTL9

Description：This register is used to configuration of the SPI interface

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0058			Register description (Reset 0x0000_0000)													SPI_CTL9
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_TX_DATA_LEN_L															
Type	R/W															
Reset	0															

Field Name	Bit	R/W	Reset Value	Description
SPI_TX_DATA_LEN_L	[15:0]	R/W	16'h0	Indicates: spi tx data length from tx fifo, Low 16bit of tx data length

6.3.5.26 SPI_CTL10

Description：This register is used to configuration of the SPI interface

0x005C			Register description (Reset 0x0000_0000)													SPI_CTL10
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved						SPI_RX_DUMY_LEN						SPI_TX_DATA_LEN_H			
Type	RO						R/W						R/W			
Reset	0						0						0			

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:10]			
SPI_RX_DUMY_LEN	[9:4]	R/W	6'h0	Spi rx dummy clock length
SPI_RX_DATA_LEN_H	[3:0]	R/W	4'h0	Indicates receives data length from slave, high 4 bits of spi rx data length

6.3.5.27 SPI_CTL11

Description：This register is used to configuration of the SPI interface

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0060	Register description (Reset 0x0000_0000)												SPI_CTL11			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SPI_RX_DATA_LEN_L															
Type	R/W															
Reset	0															

Field Name	Bit	R/W	Reset Value	Description
SPI_RX_DATA_LEN_L	[15:0]	R/W	16'h0	Indicates: spi receives data length from slave, Low 16bit of rx data length

6.3.5.28 SPI_CTL12

Description：This register is used to configuration of the SPI interface

0x0064	Register description (Reset 0x0000_0000)												SPI_CTL12			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name															SW_RX_REQ	SW_RX_REQ
Type	R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:2]	R/W	16'h0	
SW_TX_REQ	[1]	WO	1'h0	Software TX data request, for write LCD
SW_RX_REQ	[0]	WO	1'h0	Software RX data request, for read LCD

6.3.5.29 SPI_STS6

Description：Used to observe tx data counter

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0068			Register description (Reset 0x0000_0000)													SPI_STS6
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TX_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TX_DATA_CNT	[15:0]	RO	16'h0	Tx data cnt

6.3.5.30 SPI_STS7

Description：Used to observe tx data counter

0x006C			Register description (Reset 0x0000_0000)													SPI_STS7
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TX_DUMMY_CNT						RO	RO	RO	RO	RO	RO	TX_DATA_CNT			
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TX_DATA_CNT	[3:0]	RO	5'h0	tx data counter
TX_DUMMY_CNT	[15:10]	RO	5'h0	tx dummy counter

6.3.5.31 SPI_STS8

Description：Used to observe rx data counter

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0070			Register description (Reset 0x0000_0000)													SPI_STS8
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RX_DATA_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
RX_DATA_CNT	[15:0]	RO	16'h0	Rx data cnt

6.3.5.32 SPI_STS9

Description：Used to observe rx data counter

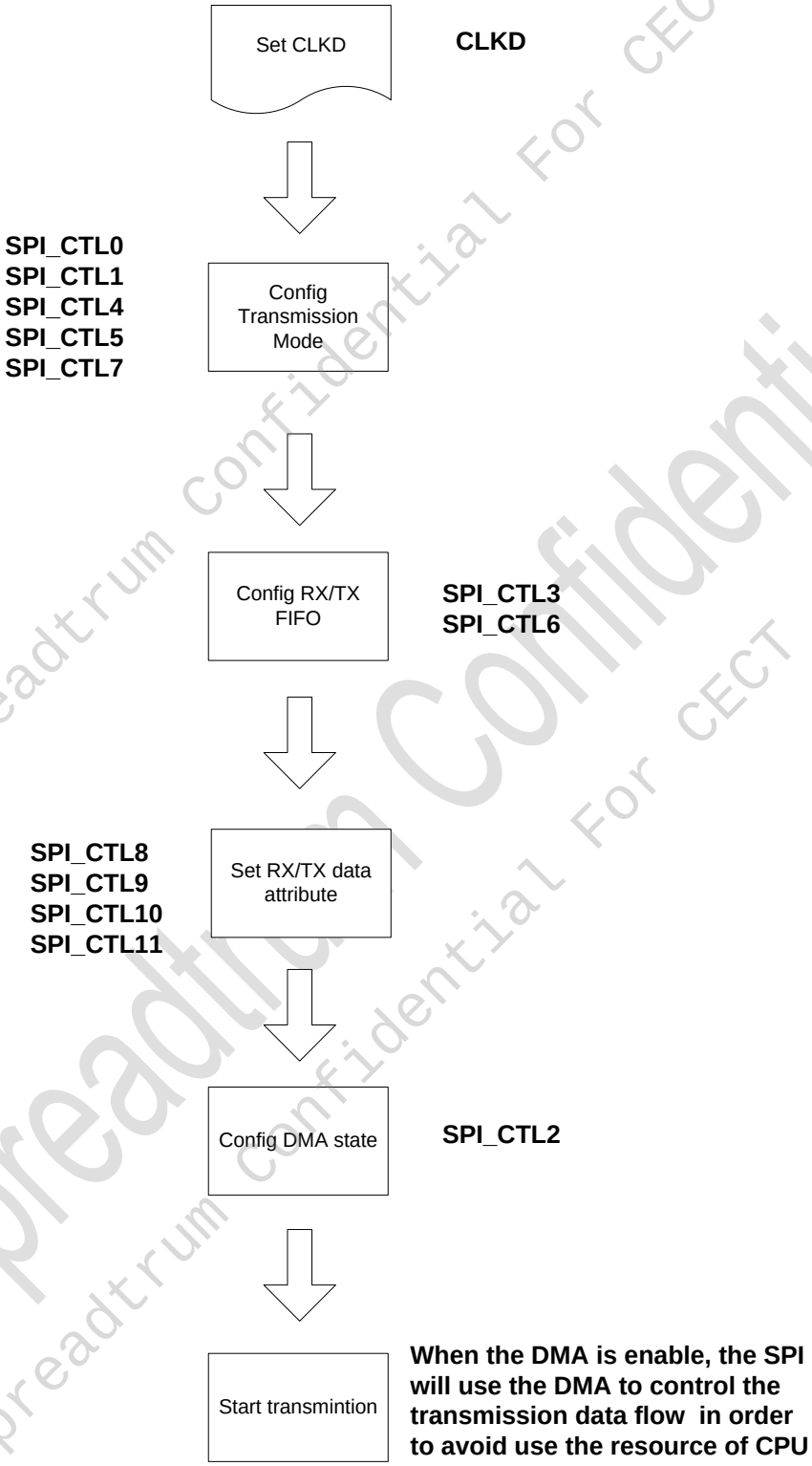
0x0074			Register description (Reset 0x0000_0000)													SPI_STS9
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TX_DUMMY_CNT						RO	RO	RO	RO	RO	RO	TX_DATA_CNT			
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
RX_DATA_CNT	[3:0]	RO	5'h0	rx data counter
RX_DUMMY_CNT	[15:10]	RO		rx dummy counter

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.3.6 Application notes

6.3.6.1 Programming Model



When control the SPI transmission, the control register must be set in correct mode. Here list some example of control register configuration method, for more detail information, please reference the chapter 1.1.5.

6.3.6.1.1 MICRO/PLUS mode program examples

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

1. **MICRO/PLUS mode**, master, 32 bits per-channel, MCLK 48M, SCK 24M, CS0 is valid, RX at negedge, TX at posedge, SCK idle phase being low, Program control register:

```
Spi_clkd = 0x0001;
Spi_ctl0  = 0x0e01;
Spi_ctl1  = 0x3100;
Spi_ctl2  = 0x0000;
Spi_ctl3  = 0x1d1a;
Spi_ctl4  = 0x0000;
Spi_ctl5  = 0x0000;
Spi_ctl6  = 0x1303;
Spi_ctl7  = 0x0000;
Spi_ctl8  = 0x0000;
Spi_ctl9  = 0x0019;
Spi_ctl10  = 0x0000;
Spi_ctl11  = 0x0019;
```

2. 16 bits per-channel, master, MCLK 80M, SCK 10M, only receive mode, ready to receive 0x1f words from slave, CS1 is valid, RX at falling edge, TX at rising edge, SCK idle phase being low,Program control register:

```
Spi_clkd = 0x0003;
Spi_ctl0   = 0x0d41;
Spi_ctl1   = 0x1000;
Spi_ctl2   = 0x0000;
Spi_ctl3   = 0x1010;
Spi_ctl4   = 0x021f;
Spi_ctl5   = 0x0000;
Spi_ctl6   = 0x1010
Spi_ctl7   = 0x0000
Spi_ctl8   = 0x0000
Spi_ctl9   = 0x0011
Spi_ctl10   = 0x0000
Spi_ctl11   = 0x0011
```

3. 8 bits per-channel, master, MCLK 48M, SCK 24M, CS2 is valid, RX at falling edge, TX at rising edge, SCK idle phase being high, LSB, dma_en, Program control register:

```
Spi_clkd = 0x0000;
Spi_ctl0  = 0x27a2;
Spi_ctl1  = 0x3000;
Spi_ctl2  = 0x0040;        //bit[6], enable dma
Spi_ctl3  = 0x1010;
Spi_ctl4  = 0x0000;
Spi_ctl5  = 0x0000;
Spi_ctl6  = 0x1010
Spi_ctl7  = 0x0000;
```


This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Spi_ctl8 = 0x0000
Spi_ctl9 = 0x0011
Spi_ctl10 = 0x0000
Spi_ctl11 = 0x0011

4. MICRO/PLUS mode, master, 32 bits per-channel, MCLK 80M, SCK 20M, CS0 is valid, RX at rising edge, TX at negedge, SCK idle phase being low, transmit only, Program control register:

```
Spi_clkd = 0x0001;
Spi_ctl0  = 0x0e02;
Spi_ctl1  = 0x2000;  // transmit only
Spi_ctl2  = 0x0000;
Spi_ctl3  = 0x1010;
Spi_ctl4  = 0x0000;
Spi_ctl5  = 0x0000;
Spi_ctl6  = 0x1010
Spi_ctl7  = 0x0000;
Spi_ctl8   = 0x0000
Spi_ctl9   = 0x0011
Spi_ctl10   = 0x0000
Spi_ctl11   = 0x0011
```

5. MICRO/PLUS mode, **slave**, 32 bits per-channel, RX at rising edge, TX at negedge, SCK idle phase being low, Program control register :

```
Spi_clkd  //no use when SPI working as slave , half SCK must have at least 4
            system(MCLK) clock cycle.
Spi_ctl0  = 0x0f02;
Spi_ctl1  = 0x3000;
Spi_ctl2  = 0x0020;
Spi_ctl3  = 0x1010;
Spi_ctl4  = 0x0000;
Spi_ctl5  = 0x0080;
Spi_ctl6  = 0x1010
```

6. MICRO/PLUS mode, slave, 8 bits per-channel, RX at falling edge, TX at rising edge, SCK idle phase being low, TX only/ RX only, Program control register:

```
Spi_ctl0  = 0x0e21;
Spi_ctl1  = 0x2000(TX only);  / spi_ctl1 = 0x1000(RX only)
Spi_ctl2  = 0x0020;
Spi_ctl3  = 0x1010;
Spi_ctl4  = 0x0000;
Spi_ctl5  = 0x0090;
Spi_ctl6  = 0x1010
```

6.3.6.1.2 SYNC mode program examples

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Only work in master mode.

Relative register: spi_ctl0[15:14], spi_ctl1[4:0], spi_ctl1[11:8],

1. SYNC mode, master, 32 bits per-channel, MCLK 48M, SCK 12M, RX at rising edge, TX at falling edge, CS0 is valid , and signal sync maps to cs2, Program control register:

   Spi_clkd = 0x0001;

   Spi_ctl0 = 0x4a02; //bit[14] enable sync mode, bit[15] = 0 means positive pulse

   Spi_ctl1 = 0x3400;// sync pulse position will locate on top of bit0, sync maps to cs2

   Spi_ctl2 = 0x0000;

   Spi_ctl3 = 0x1010;

   Spi_ctl4 = 0x0000;

   Spi_ctl5 = 0x0000;

   Spi_ctl6 = 0x1010

   Spi_ctl7 = 0x0000;

   Spi_ctl8 = 0x0000

   Spi_ctl9 = 0x0011

   Spi_ctl10 = 0x0000

   Spi_ctl11 = 0x0011

6.3.6.1.3 4-WIRE(S8) mode program examples

only work in master mode and only operation write being supported, TX at falling edge

relative register: spi_ctl1[7], spi_ctl1[11:8].

1. S8 mode, 8 bits per-channel, TX at falling edge, CS0 is valid and signal CD maps to cs1, program control register:

   Spi_ctl0 = 0x2e21;

   Spi_ctl1: 0x3280;

   Spi_ctl2 = 0x0000;

   Spi_ctl3 = 0x1010;

   Spi_ctl4 = 0x0000;

   Spi_ctl5 = 0x0000;

   Spi_ctl6 = 0x1010

   Spi_ctl7 = 0x0000;

   Spi_ctl8 = 0x0000

   Spi_ctl9 = 0x0011

   Spi_ctl10 = 0x0000

   Spi_ctl11 = 0x0011

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.3.6.1.4 3-WIRE mode program examples

Only work in master mode.

Relative register: spi_ctl0[15], spi_ctl1[4:0], spi_ctl1[5], spi_ctl1[6], spi_ctl2[4:0]

1. timing1(TX RX at falling edge), 16 bits per-channel, CS0 is valid, read command polarity is high, w/r control position is 8, read data start bit is 7, program control register:

   spi_ctl0 = 0x0e43;

   spi_ctl1 = 0x3068;

   spi_ctl2 = 0x0007;

2. timing2(TX RX at rising edge), 16 bits per-channel, CS0 is valid, read command polarity is low, w/r control position is 8, read data start bit is 7, program control register:

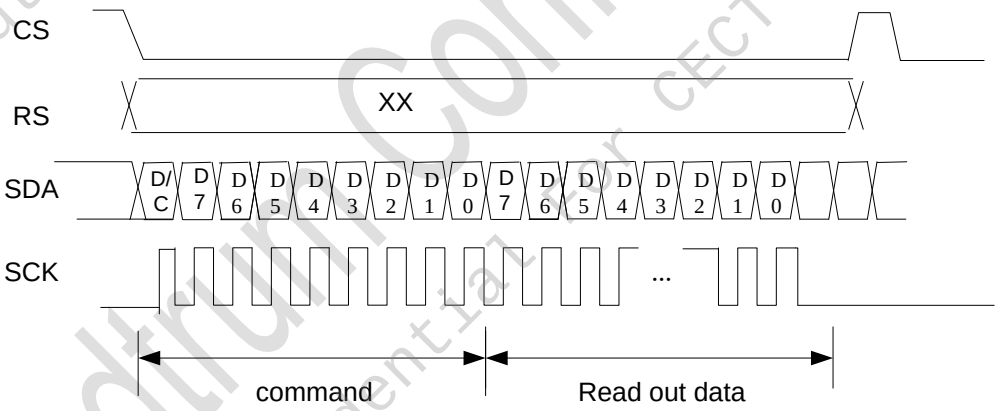
   spi_ctl0 = 0xae43;

   spi_ctl1 = 0x3068;

   spi_ctl2 = 0x0007;

6.3.6.2 GC9304C LCD driver Programming Model

6.3.6.2.1 8 bit read program examples



Only work in master mode, TX at falling edge and received at rising edge. Use 9bit 3 wire RW mode. 1 command bit, 8 bits output data and 8 bit input data per-channel, no dummy cycle.

Spi_ctl0 = 0x2e41

Spi_ctl1= 0x3100

Spi_ctl2 = 0x0000

Spi_ctl3 = 0x1010

Spi_ctl4 = 0x0000

Spi_ctl5 = 0x0000

Spi_ctl6 = 0x1010

Spi_ctl7 = 0x0028 3 wire 9bit RW mode

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Spi_ctl8 = 0x0000

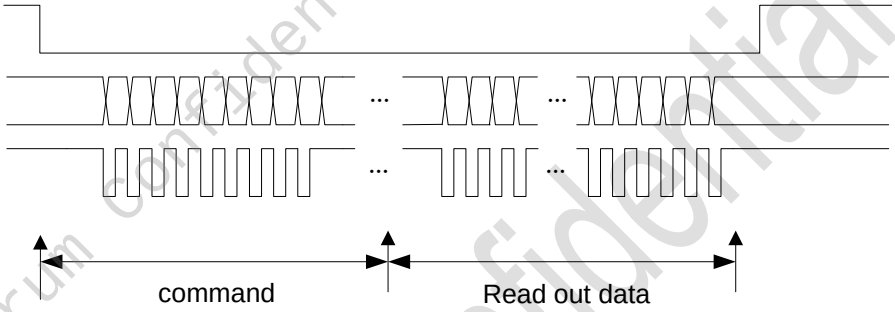
Spi_ctl9 = 0x0011

Spi_ctl10 = 0x0000

Spi_ctl11 = 0x0011

Spi_ctl12 = 0x0002

6.3.6.2.2 **24/32 bit read program examples**



Only work in master mode, TX at falling edge and received at rising edge. Use 9bit 3 wire mode and 4 wire 8bit mode. The read transfer divided into 2 transactions. The first one send 1 command bit and 8 bits output command data, the second transaction received 24/32 bit read data use 4 wire 8bit mode.



1. 3 wire 9 bit mode transmit command

Spi_ctl0 = 0x2e21

Spi_ctl1 = 0x2100

Spi_ctl2 = 0x0007

Spi_ctl3 = 0x1010

Spi_ctl4 = 0x0000

Spi_ctl5 = 0x0000

Spi_ctl6 = 0x1010

Spi_ctl7 = 0x0008 3 wire 9 bit mode

Spi_ctl8 = 0x0010 TX dummy length=1

Spi_ctl9 = 0x0001

Spi_ctl10 = 0x0000

Spi_ctl11 = 0x0001

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Spi_ctl12 = 0x0002

2. Read data in 4 wire 8bit mode

Spi_ctl0 = 0x2e01 32bit data

Spi_ctl1 = 0x1100

Spi_ctl2 = 0x0007

Spi_ctl3 = 0x1010

Spi_ctl4 = 0x0000

Spi_ctl5 = 0x0000

Spi_ctl6 = 0x1010

Spi_ctl7 = 0x0018 4 wire 8 bit mode

Spi_ctl8 = 0x0000

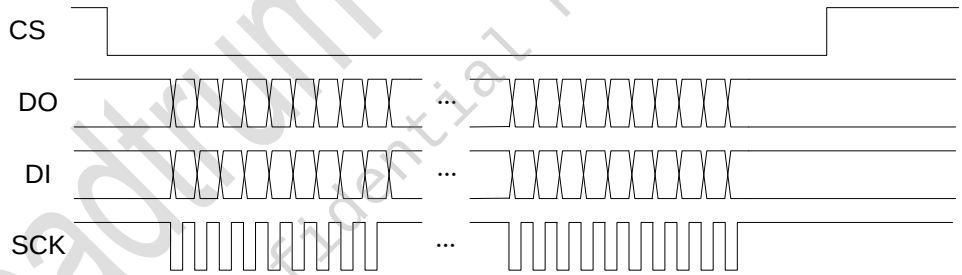
Spi_ctl9 = 0x0001

Spi_ctl10 = 0x0000

Spi_ctl11 = 0x0001

Spi_ctl12 = 0x0001

6.3.6.2.3 Two data line mode program examples



Only work in master mode, TX at falling edge and received at rising edge. Use 9bit 3 wire mode send RGB data. In this mode, DI pin is second data line.

1. 3 wire 9 bit mode transmit RGB data (RGB565)

Spi_ctl0 = 0x2e21

Spi_ctl1 = 0x2100

Spi_ctl2 = 0x0007

Spi_ctl3 = 0x1010

Spi_ctl4 = 0x0000

Spi_ctl5 = 0x0000

Spi_ctl6 = 0x1010

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Spi_ctl7 = 0xc008 3 wire 9 bit mode, enable two data line, data format RGB565

Spi_ctl8 = 0x0000

Spi_ctl9 = 0x0001

Spi_ctl10 = 0x0000

Spi_ctl11 = 0x0001

Spi_ctl12 = 0x0002

6.3.6.3 Programming Notes

1. only receive mode

   as master: set spi_ctl4[9] = 1 and set spi_ctl1[13:12] = “01” and program spi_ctl4[8:0] to N, means enable rx only mode , and ready to receive N words from slave.

   as slave: set spi_ctl1[13:12] = “01” , the received number depending on master the posedge of is_rx_only(spi_ctl4[9] = 1) will trigger the process, so SW should write to “0” first, then write to “1” to this bit.

2. fast mode

   used for slave mode. In slave mode, half SCK must have at least 4 system clock cycle.

   When SCK < 14X MCLK, recommend to use fast mode.

   8X : is_fst(spi_ctl4[14]) =1, phs_dly([spi_ctl4[13:12]] = 1

   10X : is_fst=1, phs_dly = 2

   12X : IS_fst=1, phs_dly = 3

3. In salve mode, spi_ctl5[15:0]* Tclk_spi should not be such smaller than Tspi_sck, so as not to make SPI stop transfer.

4. DMA enable
   a) DMA should be configured first
   b) Program SPI control register except spi_ctl2[6]
   c) Write spi_ctl2[6] at last

5. When change SPI control register configuration , SW should ensure:
   a) tx_fifo is real empty at first
   b) then, rx_fifo is real empty
   c) change SPI control register

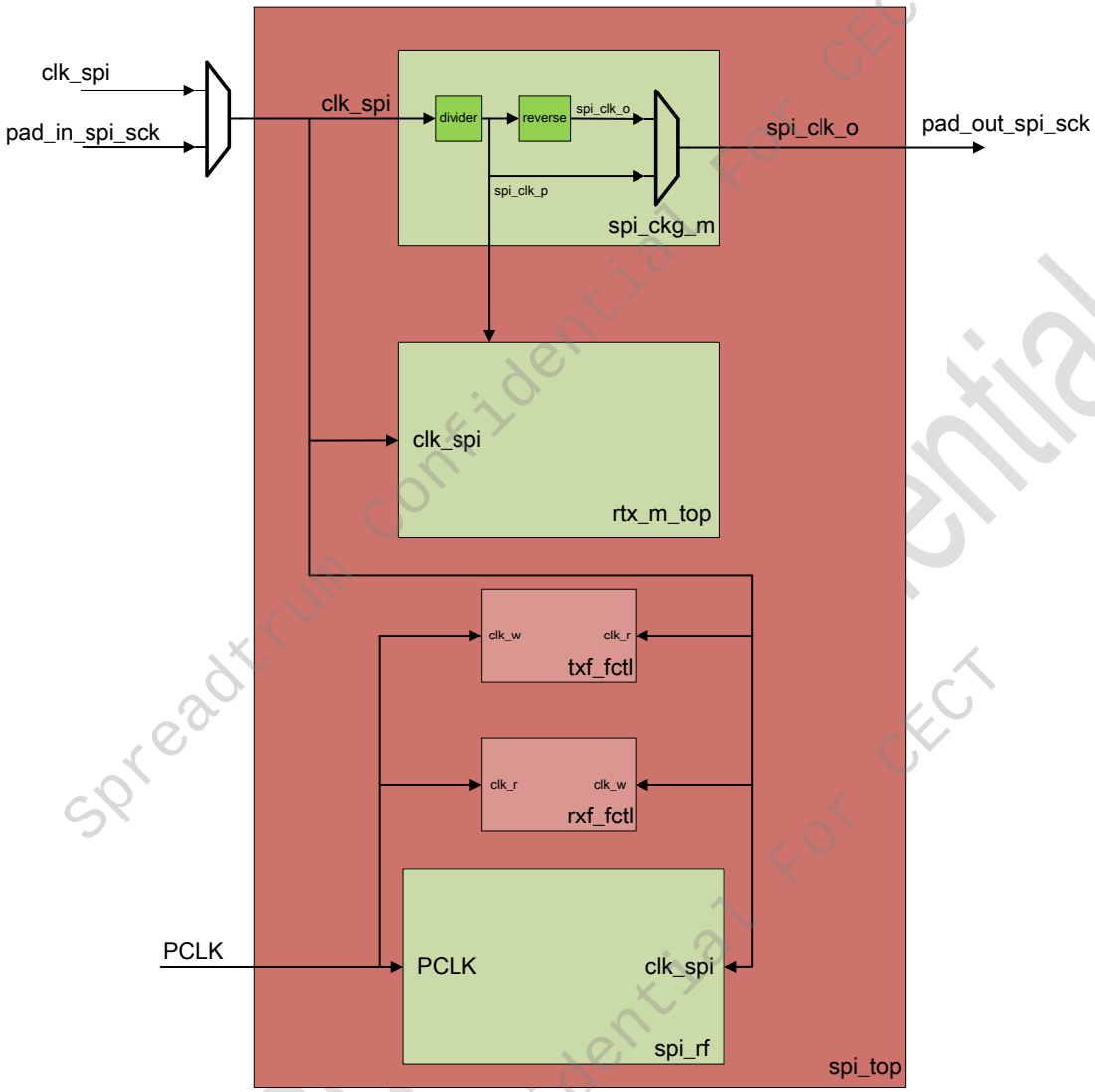
6.3.7 New feature

- Support csn input in slave mode.
- Add csn_ie_ctl register to control csn input ie when slave
- Add csn_i_sel[1:0] register to select csn when slave

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

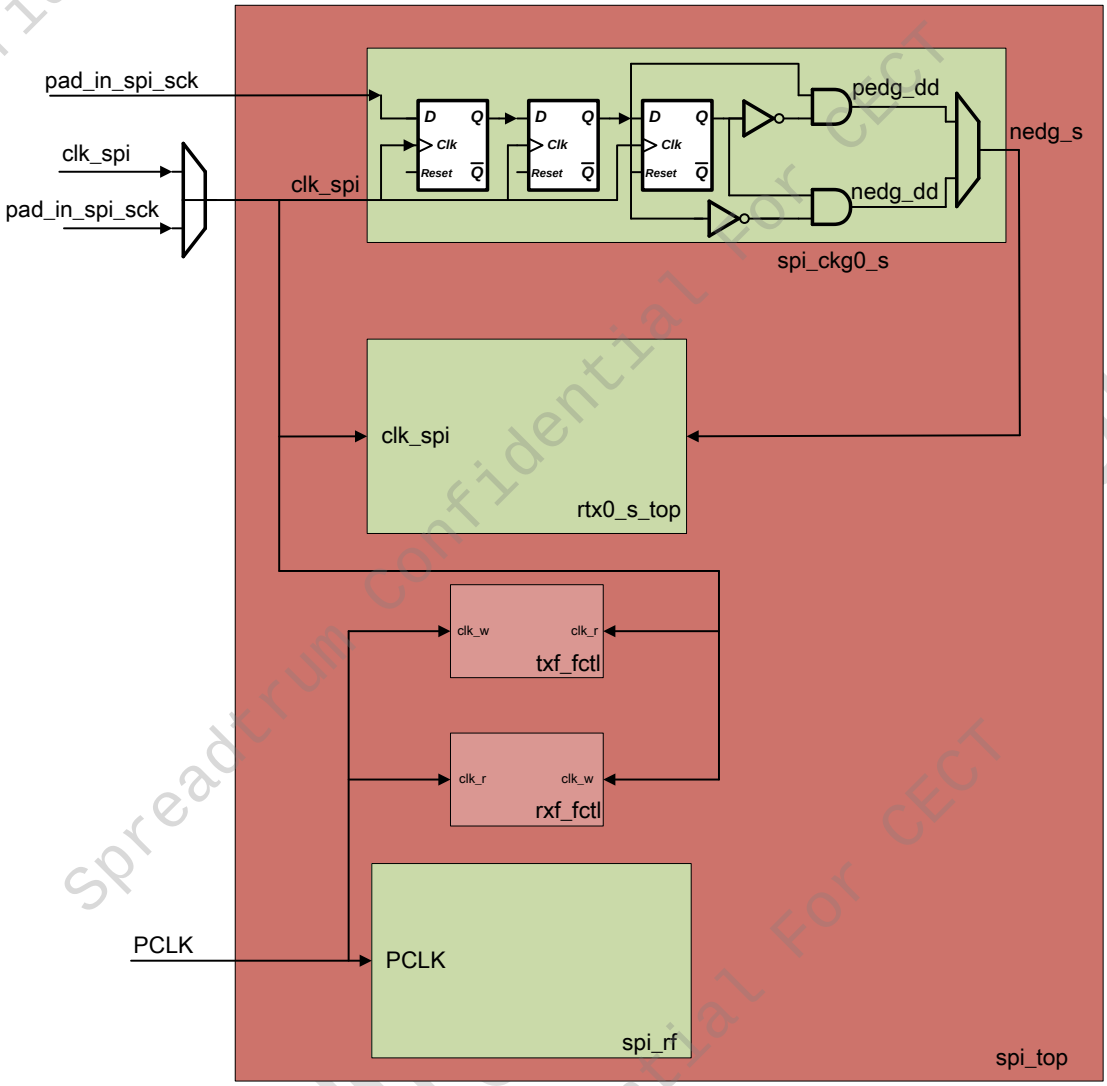
6.3.8 Clock Path

6.3.8.1 Master mode



This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

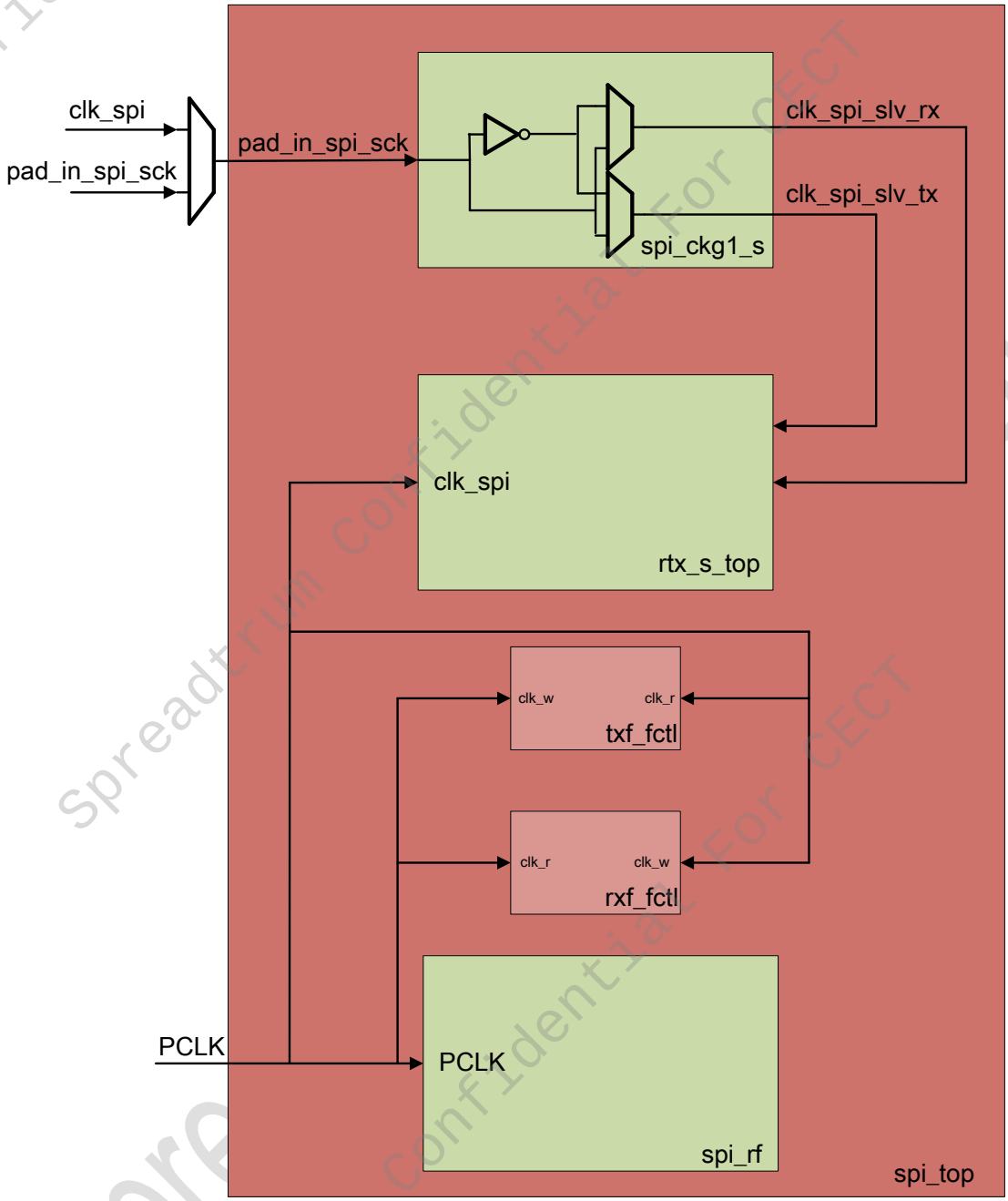
6.3.8.2 Slave low speed mode



Spreadtrum Confidential For CECT

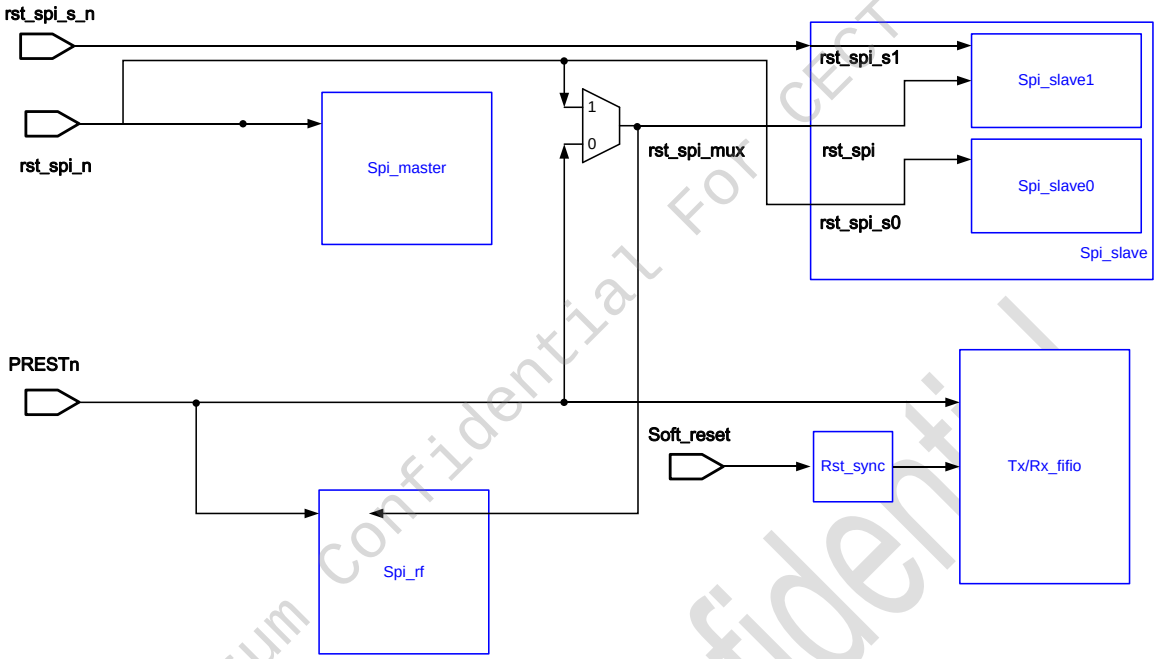
This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.3.8.3 Slave high speed mode



This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.3.9 Reset



Signal Name	Direction	Description	Connection Information
rst_spi_n	Input	SPI core reset signal, low active.	Core logic reset, SYNC with clk_spi clock domain.
rst_spi_s_n	Input	SPI TX RX logic reset for slave HS mode.	Because of clk_spi may no active clock in HS slave mode, so it connected to PCLK domain reset signal.
PRESETn	Input	APB bus reset.	Connected to system bus reset for APB.

6.4 IIS and PCM interface

6.4.1 Overview

IIS is a common digital audio interface specification. Base Band Chip IIS Interface can be used to implement a CODEC interface with external digital audio system working as host or slave. The IIS interface supports both IIS and PCM data format. The interface can transmit and receive data simultaneously as well as transmit or receive data alternatively at a time. This document defines function and configuration of IIS block.

IIS module can be controlled both by ARM or DSP.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.4.2 Features

- Compliant with the IIS/PCM standard
- Support IIS, MSB-Justified and DSP data bus interface working on IIS mode
- Support Long Frame, Short Frame and Multi-cycle Frame working on PCM mode
- Serial clock with programmable frequency
- Two 32-word-deep FIFOs minimizes processor overhead at high data rates
- LRCK polarity can be configured
- Wide selection of IIS data lengths 8,16,32bits
- Master / slave
- MSB / LSB
- Transmit only/ receive only / transmit and receive mode
- 2 DMA requests
- Single interrupt line for multiple interrupt source events
- IIS and PCM master mode: support integer clock divider
- IIS master mode: support fraction clock divider – both variable and fixed serial clock mode
- PCM master mode: support fraction clock divider – only variable serial clock mode
- Support 32bit width of APB 2.0 configuration.

6.4.3 Signal description

c

Figure 6-6 IIS connection as master

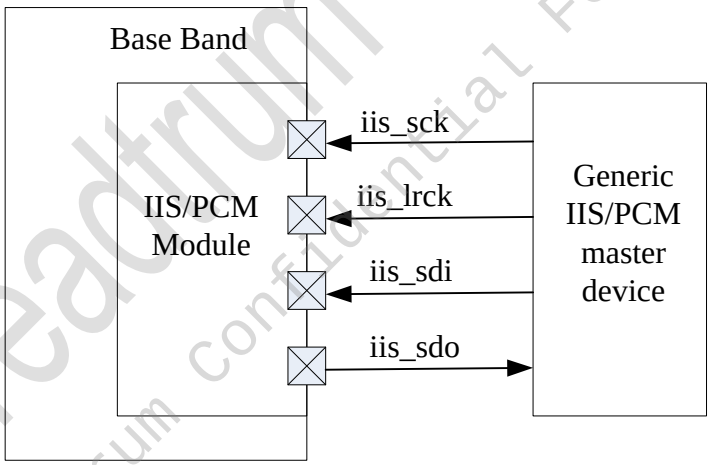


Figure 6-7 IIS connection as slave

6.4.4 Funtion description

6.4.4.1 IIS interface

IIS module consists of RX/TX controller, ARM APB interface control register, clock generator and FIFO control. ARM programs IIS register, enable IIS mode, starts RX/TX data transfer. Output data is written to TX FIFO and received data is stored in RX FIFO. Each FIFO is 32-bit width plus 32-address length.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

MCLK generator generates main clock for IIS block. This clock also output as master clock during hand shaking. In slave mode, external clock source can be input, working as the IIS main clock. Clock divider value and control signal for MCLK come from global control register.

The IIS SCLK generator divides main clock according to a 16-bit clock divider register, which defines half SCLK clock width. It can be programmed from 0 to 32767.

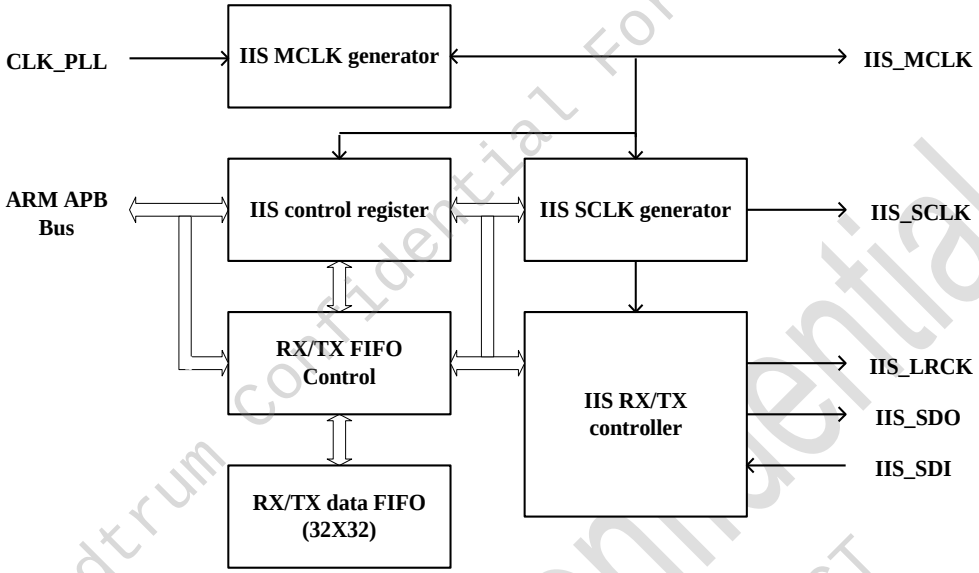


Figure 6-8 IIS module diagram

IIS interface has 4 pins, IIS_SCK is serial clock output, IIS_SDI is serial data input, IIS_SDO is serial data output. IIS_LRCK is left/right channel select. The device generating IIS_LRCK and IIS_SCK is the master. IIS_LRCK and IIS_SCK are output pins if working as master. They are input pins if working as slave.

Serial data is transmitted in two's complement format with the MSB first. Serial data can be sent at rising or falling edge of SCK, at receiver, it must be latched at rising edge. When system word length is greater than the transmitter word length, the word is truncated (least significant data bits are set to '0') for data transmission. If the receiver is sent more bits than its word length, the bits after the LSB are ignored. On the other hand, if the receiver is sent fewer bits than its word length, the missing bits are set to zero internally.

Three bus formats are available in this module. Following Figures illustrate the relationship between the SCK, LRCK and serial data I/O for different interface protocols. The polarity of LRCK is programmable. The bits per-channel is programmable up to 32bit.

IIS mode is where the MSB is available on the 2nd rising edge of SCLK following a LRCK transition.

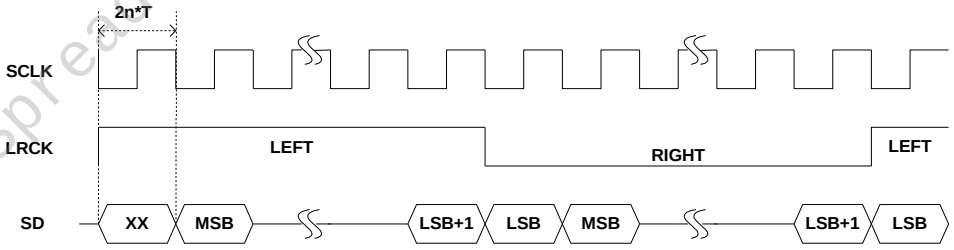


Figure 6-9 IIS-compatible format

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

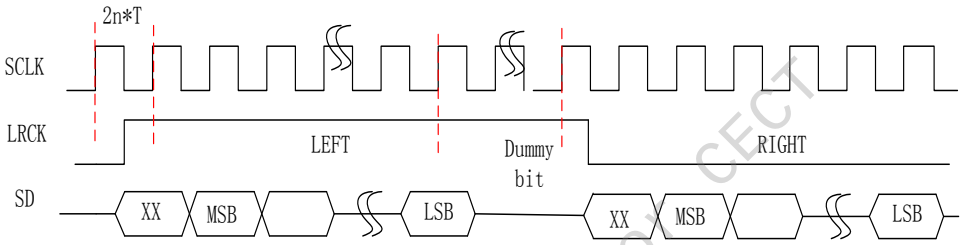


Figure 6-10 IIS-compatible format with dummy bit

MSB-justified mode is where the MSB is available on the first rising edge of SCK following a LRCK transition.

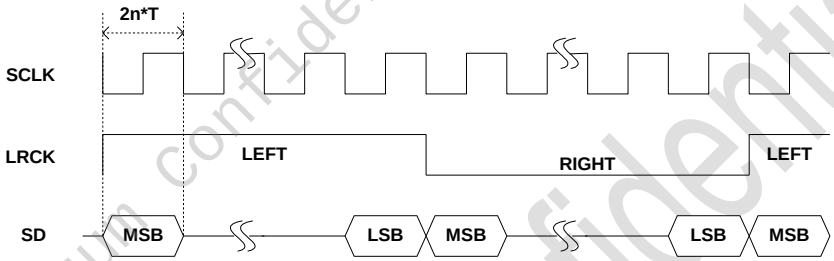


Figure 6-11 MSB-justified format

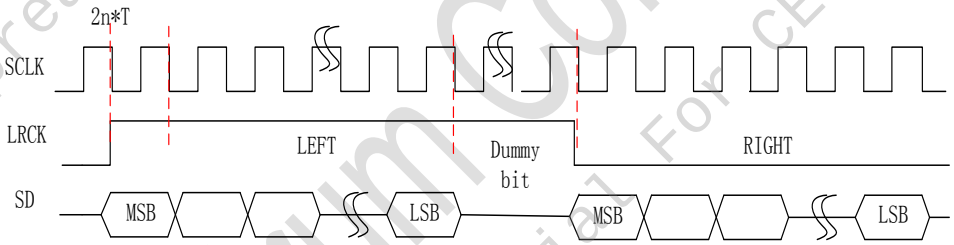


Figure 6-12 MSB-justified format with dummy bit

DSP mode is where the left channel MSB is available on either the 1st or 2nd rising edge of BCLK following a LRCK transition high. Right channel data immediately follows left channel data.

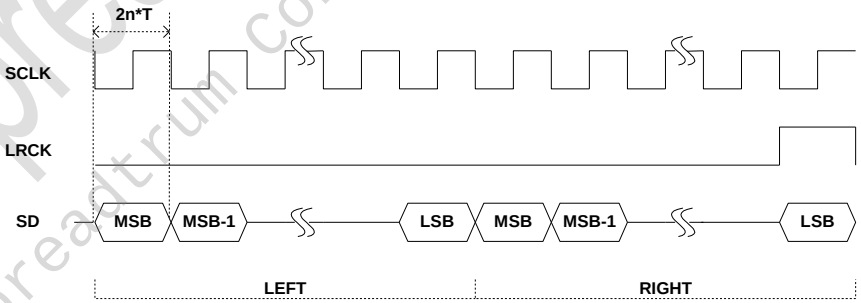


Figure 6-13 Synchronized format

Note:

T: 1/(system clock frequency)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

n: register programmable integer, n-1 = 1, …., 32767

Table 2 IIS data format memory map

IIS_CTL bit1~0	Bits / channel	Data arrangement
00	8bit	Data on bit 31~24
01	16bit	Data on bit 31~15
1x	32bit	Data on bit 31~0

6.4.4.2 PCM interface

PCM interface is a direct voice interface connects to standard CODEC. The implementation is compliant with the MP-PCM requirements for voice transfer (8 kHz PCM_SYNC and 8 or 16 bits data). The four signals of the PCM interface are:

– PCM_CLK: PCM clock

– PCM_SYNC: PCM 8KHz synchronization signal

– PCM_OUT: PCM output data

– PCM_IN: PCM input data

These four pins is able to share IIS interface follow this mapping:

PCM_CLK share with IIS_SCK,

PCM_IN share with IIS_SDI,

PCM_OUT share with IIS_SDO,

PCM_SYNC share with IIS_LRCK.

The data can be linear PCM (13-16 bit), μ-Law (8 bit) or A-Law (8bit). The interface can work as either Master or Slave.

Programming IIS_CTL 0 register bit 15 to 1 configures the PCM mode.

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When Base Band Chip is configured as PCM Master, generating PCM_SYNC and PCM_CLK, 8 bits in one frame, then PCM_SYNC is 7-bit long. When Base Band chip is configured as PCM Slave, PCM_SYNC may be from one consecutive falling edges of PCM_CLK to not big or equal than PCM data length (as figure shows, PCM_SYNC is 2~7.5 bits) long.

Programming IIS_CTL0 register bit8 to zero configures the Long Frame Sync mode.

PCM_IN is captured on the falling edge of PCM_CLK and PCM_OUT transmits on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge. The control bit is IIS_CTL2 bit10, if high, OE changes to low at falling edge of the last bit.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

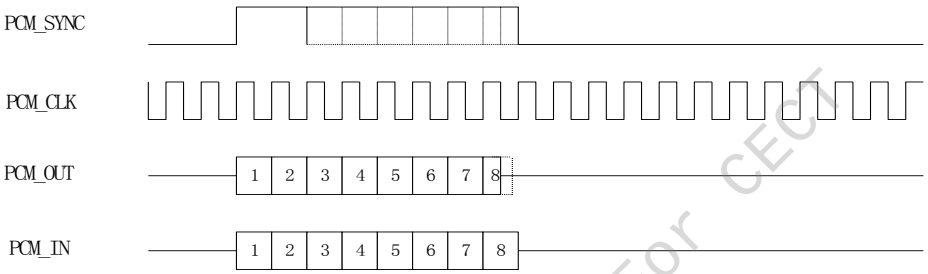


Figure 6-14 Long frame sync (Shown with 8-bit sample)

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

As with Long Frame Sync, Base Band Chip samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

Programming IIS_CTL0 register bit8 to high configures the Short Frame Sync mode.

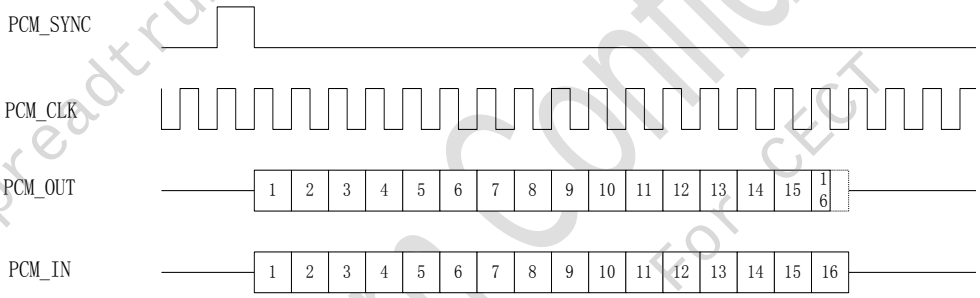


Figure 6-15 Short frame sync (Shown with 16-bit sample)

More than one channel connection over the PCM interface is supported using multiple slots. Up to three channel connections can be carried over any of the first three slots.

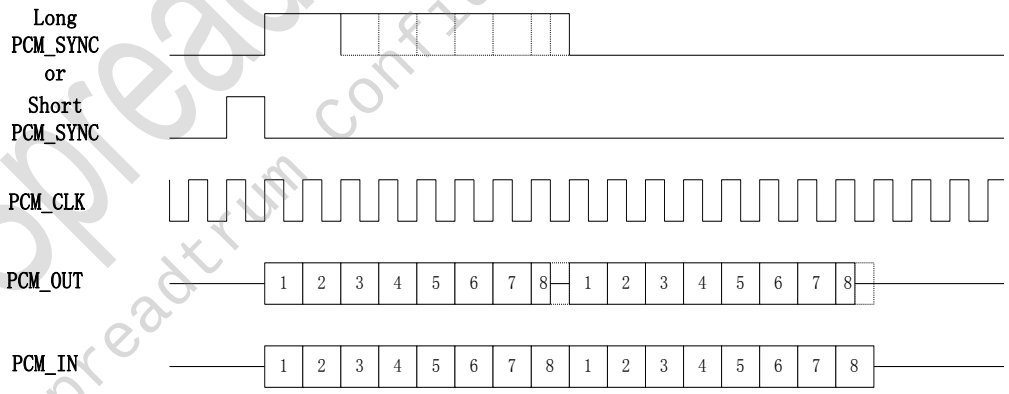


Figure 6-16 Multi-slot operation with two slots and 8-bit compounded samples

Three slots can be configured in one PCM frame; IIS_CTL2 register bit 2~0 define which channel is occupied. Each bit configures one of the three channels. If bit0 is high, then slot0 is carrying data. If channel 0 and 2 is active, this register is 0x5.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

PCM data format in TX/RX buffer is different between master and slave mode. If burst size is 16 or 8bit, in slave mode, data for slot 0 and slot 1 are packed into one word, which locates in lower address; data for slot2 locates in higher address; slot0 and slot2 fill higher bits (bit31~24). In master mode, only slot0 takes lower address and locates on lower bits (bit15~8); slot1, slot2 packed in higher address, and slot2 takes lower bits while slot1 in higher bits. Following table shows PCM data format for master and slave mode.

Table 3 PCM data format for master mode

IIS_CTL bit1~0	Bits / channel	Data arrangement
00	8bit	Data for channel 0 on bit 15~8, in lower address. Data for channel 1 on bit 31~24, Data for channel 2 on bit 15~8, on higher address.
01	16bit	Data for channel 0 on bit 15~0, in lower address. Data for channel 1 on bit 31~16, Data for channel 2 on bit 15~0, on higher address
1x	32bit	Data for channel 0 store in low address, data for channel 1, 2 store in high address.

Table 4 PCM data format for slave mode

IIS_CTL bit1~0	Bits / channel	Data arrangement
00	8bit	Data for channel 0 on bit 31~24, Data for channel 1 on bit 15~8, in lower address. Data for channel 2 on bit 31~24, on higher address.
01	16bit	Data for channel 0 on bit 31~16, Data for channel 1 on bit 15~0, in lower address. Data for channel 2 on bit 31~16, on higher address
1x	32bit	Data for channel 0 store in low address, data for channel 1, 2 store in high address.

Table 5 PCM multiple slot and PCM cycle configuration suggestion

pcm_slot[0]	pcm_slot[1]	pcm_slot[2]	pcm_cycle
0	0	1	<=2
0	1	0	>=1
0	1	1	>=1
1	0	0	>=2
1	0	1	>=2
1	1	0	>=2
1	1	1	>=2

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Table 6 Exceptions for PCM multiple slot configuration

Bit width	pcm_slot[0]	pcm_slot[1]	pcm_slot[2]	pcm_cycle	sample rate	clk_iis
32	1	-	1	2	8 or 44.1 or 48k	26/80MHz
16,8				4		

Note:

- In PCM fraction divide mode, clk_iis frequency should be 20 times bigger than bit clock
- For EDA simulation, pcm_slot[2:0]=101, bit_width=8 or 16,pcm_cycle>=2 is ok, but software test meet some problem when sample rate > 1KHz. So we suggest software engineer setting pcm_cycle =4 in application. It`s ok for both software and EDA simulation.

Spreadtrum Confidential
Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.4.4.3 IIS clock path

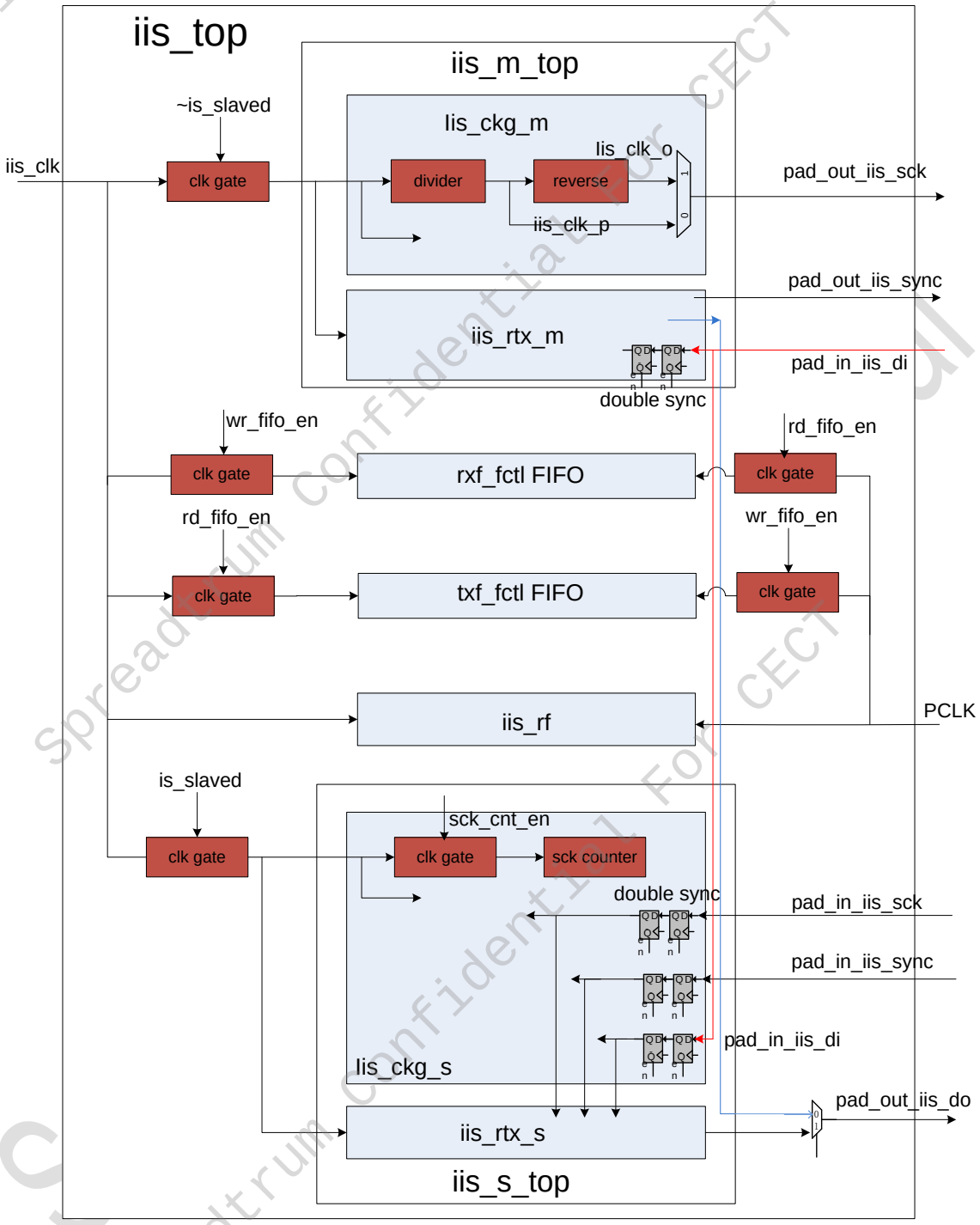


Figure 6-17 IIS clock path

Note：

a. Module clock: iis_clk, PCLK.
b. IO pad: iis_sck, iis_sync, iis_di, iis_do.
c. IIS IP can be configured as master mode or slave mode. The configure signal is iis_slaved

If iis_salved= 1, iis works as slave. iis_m_top will not work.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

If iis_salved = 0,iis works as master. Iis_s_top will not work.

d. “divider” block function: iis_clk_p = iis_clk/M. where M is a clock divider factor.
e. “reverse” block function: iis_clk_o = ~ iis_clk_p.
f. “sck counter” block function: count iis_sck period. Count unit is iis_clk.
g. “double sync” block is used to resolve crossing clock domain signal.

6.4.4.4 Pad IO timing

In default mode, iis output signals, like iis_do, iis_sync(for master) signal, are sent at the posedge of iis_sck. And input signals like iis_di, iis_sync(for slave), are sampled at the negedge of iis_sck.

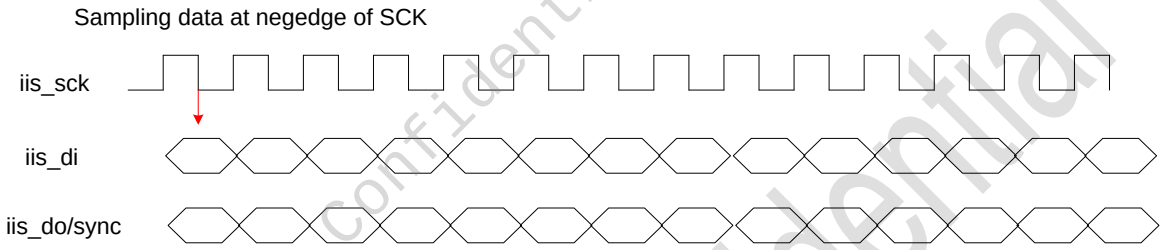


Figure 6-18 Sampling data at negedge of IIS_SCK

We can also set output signal sent edge as negedge and sampling edge as posedge, like the following.

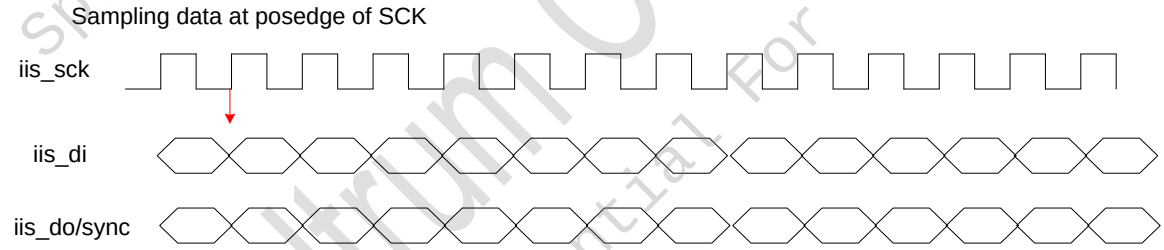


Figure 6-19 Sampling data at posedge of IIS_SCK

The implementation of sampling edge is as following.

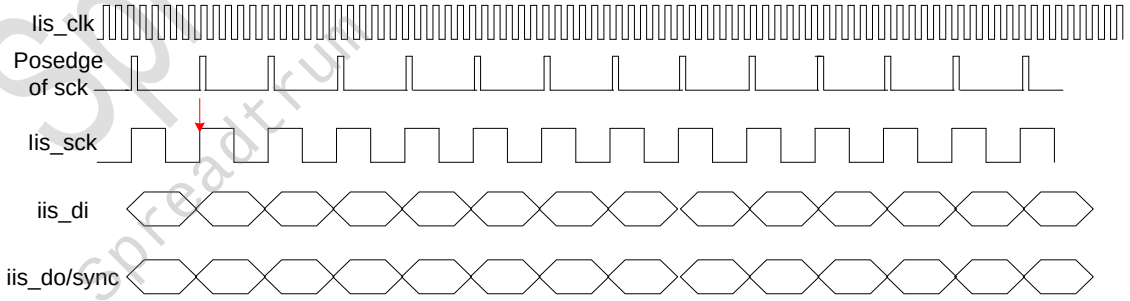


Figure 6-20 implementation of sampling data at negedge of IIS_SCK

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

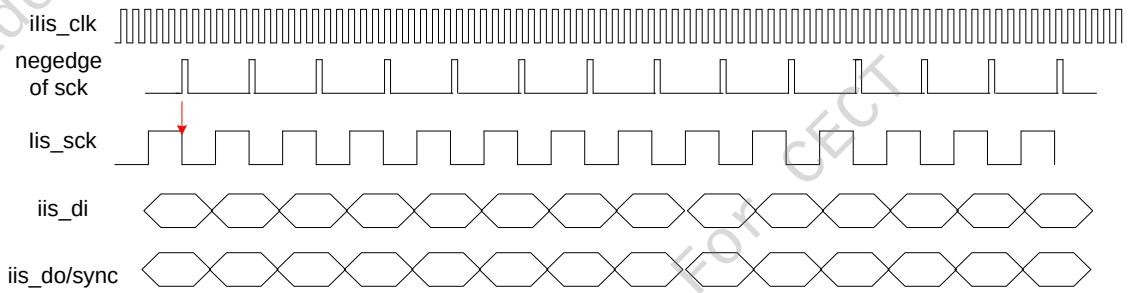


Figure 6-21 implementation of sampling data at posedge of IIS_SCK

6.4.4.5 Setup time and hold time

If we assume that max input delay is 10ns and min input delay is 0ns for iis_di to iis_sck. max output delay is 10ns and min output delay is 5ns for iis_do/iis_lrck to iis_sck. The clock period time is 50ns for iis_sck.

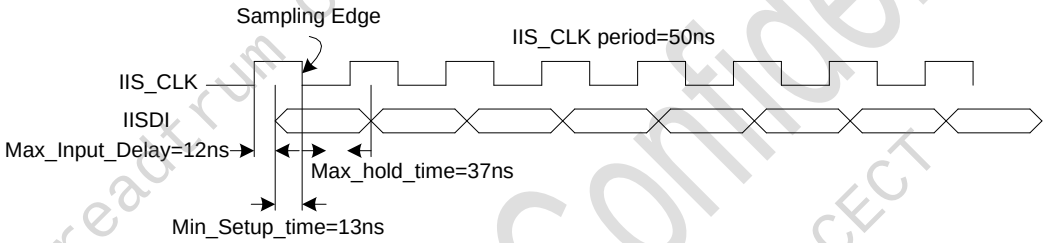


Figure 6-22 implementation of sampling data at posedge of IIS_SCK

Then for iis_di, the setup time range is 13ns<setup_time<25ns,and the hold time range is 25ns<hold_time<37ns. For iis_do/iis_lrck, the setup time range is 13ns<setup_time<25ns,and the hold time range is 25ns<hold_time<37ns

6.4.5 Control registers

6.4.5.1 Memory map

Base address: IIS_BASE_ADDRESS

Offset Address	Name	Description
0x0000	IIS_TXD	Write data to this address initiates a character transmission through TX FIFO Read from this address retrieve data from RX FIFO
0x0004	IIS_CLKD	Integer clock divider
0x0008	IIS_CTRL0	Control register
0x000C	IIS_CTRL1	Control register
0x0010	IIS_CTRL2	Control register
0x0014	IIS_CTRL3	RX FIFO watermark

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description
0x0018	IIS_INT_IEN	IIS interrupt enable register
0x001C	IIS_INT_CLR	IIS interrupt clear register
0x0020	IIS_INT_RAW	IIS interrupt raw status
0x0024	IIS_INT_STS	IIS interrupt mask status
0x0028	IIS_STS1	RX FIFO address
0x002C	IIS_STS2	IIS internal status
0x0030	IIS_STS3	IIS internal status
0x0034	IIS_DSPWAIT	Control register
0x0038	IIS_CTRL4	TX FIFO watermark
0x003C	IIS_STS4	TX FIFO address
0x0040	IIS_CTRL5	Control register
0x0044	Reserved	Reserved
0x0048	Reserved	Reserved
0x004C	Reserved	Reserved
0x0050	IIS_CLKML	Fraction clock divider: M[15:0]
0x0054	IIS_CLKMH	Fraction clock divider: M[21:16]
0x0058	IIS_CLKNL	Fraction clock divider: N[15:0]
0x005C	IIS_CLKNH	Fraction clock divider: N[21:16]

6.4.5.2 Register description

6.4.5.2.1 IIS_TXD

Description： Write data to this address initiates a character transmission through TX FIFO; Read from this address retrieve data from RX FIFO.

0x0000	IIS RTX register(0x0000_0000)												IIS_TXD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	IIS_TXD															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	IIS_TXD															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
IIS_TXD	[31:0]	R/W	32'h0	Write data to this address initiates a character transmission through TX FIFO Read from this address retrieve data from RX FIFO

6.4.5.2.2 **IIS_CLKD**

Description：Integer clock divider

0x0004			Integer clock divider (Reset 0x0000_0003)													IIS_CLKD
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	IIS_CLKD															
Type	IIS_CLKD															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Field Name	Bit	Type	Reset Value	Description
IIS_CLKD	[15:0]	R/W	16'h3	Specify the clock ratio between iis_sck and clk_iis. IIS_CLKD = (clk_iis / (2 * iis_sck)) - 1 And iis_sck = sample rate * channel number * channel length For example, if clk_iis runs at 76.8MHz, and IIS module is configured as 48K sample rate, 2 channel and 16-bit channel length, iis_sck should be 48K * 2 * 16 = 1.536MHz, IIS_CLKD should be (76.8M / (2 * 1.536M)) - 1 = 24 Note: When work in the slave mode, the frequency of iis_sck depends on the IIS master, so the register IIS_CLKD is not used.

6.4.5.2.3 **IIS_CTL0**

Description：IIS control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0008	Control register (Reset 0x0000_00C1)															IIS_CTL0
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PCM_EB	DMA_EN	Reserved		SCK_REV	IS_LRCK_PH	IS_SYNC_MD	IS_IISC_SHRTF	RTX_MD		BPCHN		IS_SLVD	LSB	NG_TX	NG_RX
Type	R/W	R/W	RO		R/W	R/W	R/W	R/W	R/W		R/W		R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1

Field Name	Bit	R/W	Reset Value	Description
PCM_EB	[15]	R/W	1'h0	"1" : PCM mode "0" : IIS mode
DMA_EN	[14]	R/W	1'h0	"1" : enable DMA
Reserved	[13:12]	R/W	2'h0	
SCK_REV	[11]	R/W	1'h0	SCK inverse enable
IS_LRCK_PH	[10]	R/W	1'h0	Active level of left / right channel "0" : low for left "1" : high for left
IS_SYNC_MD	[9]	R/W	1'h0	Output LRCK or SYNC for IIS mode "0" : LRCK "1" : SYNC
IS_IISC_SHRTF	[8]	R/W	1'h0	"0" : MSB justified in IIS mode Long frame in PCM mode "1" : iis-compatible format in IIS mode Short frame in PCM mode
RTX_MD	[7:6]	R/W	2'h3	"00" : idle mode "01" : receive mode "10" : transmit mode "11" : transmit and receive
BPCHN	[5:4]	R/W	2'h0	Serial bit per channel "00" : 8 bits "01": 16 bits "1x": 32 bits
IS_SLVD	[3]	R/W	1'h0	"0": IIS/PCM work as master "1": IIS/PCM work as slave
LSB	[2]	R/W	1'h0	"1": enable transmit data from LSB

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

NG_TX	[1]	R/W	1'h0	"1" enable TX data shift out at clock neg-edge
NG_RX	[0]	R/W	1'h1	"1" enable RX data shift in at clock neg-edge

6.4.5.2.4 **IIS_CTL1**

Description：IIS configure register

0x000C			Control reigster (Reset 0x0000_0000)											IIS_CTL1		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	IS_RXIOSTP	IS_TXIOSTP	IS_FSCNT_EB	IS_NUM_CNT	ITVL_NUM											
Type	R/W	R/W	R/W	R/W	R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
IS_RXIOSTP	[15]	R/W	1'h0	Receive IO stop enable "1" : enalbe
IS_TXIOSTP	[14]	R/W	1'h0	Transmit IO stop enable "1" : enable
IS_FSCNT_EB	[13]	R/W	1'h0	Clock counter enable, for debug "1": enable
IS_NUM_CNT	[12]	R/W	1'h0	Count clock for one "0" : lrck cycle "1" : sclk cycle
ITVL_NUM	[11:0]	R/W	12'h0	Used for timeout decision for slave mode If the slave has not sampled the edge of iis_sck in the interval (n*4+3)*Tclk_iis, slave will stop the receive process and send timeout interrupt

6.4.5.2.5 **IIS_CTL2**

Description：IIS control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0010	Control register (Reset 0x0000_0021)														IIS_CTL2	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SYNC_POS					PCM_OE_EN	PCM_CYC							PCM_SLOT		
Type	R/W					R/W	R/W							R/W		
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

Field Name	Bit	R/W	Reset Value	Description
SYNC_POS	[15:11]	R/W	5'h0	SYNC position when working in DSP format: 0: MSB is available on the 2nd rising edge of SCK Channel length-1: MSB is available on the 1ST rising edge of SCK
PCM_OE_EN	[10]	R/W	1'h0	"1" : Enable data oe change to low at falling edge of last bit
PCM_CYC	[9:3]	R/W	7'h4	Pcm_cycle, used for multi_slot PCM
PCM_SLOT	[2:0]	R/W	3'h1	Pcm_slot, used for multi_slot PCM "001": slot 0 is used "010": slot 1 is used "100": slot 2 is used "011": slot 0 and slot 1 are in use …

6.4.5.2.6 **IIS_CTL3**

Description : IIS RX FIFO FULL/EMPTY watermark value

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0014			RXF watermark (Reset 0x0000_0808)												IIS_CTL3	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			RXF_EMPTY_THLD					Reserved			RXF_FULL_THLD				
Type	RO								RO							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Field Name	Bit	R/W	Reset Value	Description
RXF_EMPTY_THLD	[12:8]	R/W	5'h8	Receive data full threshold
Reserved	[7:5]	R/W	3'h0	
RXF_FULL_THLD	[4:0]	R/W	5'h8	Receive data empty threshold

6.4.5.2.7 **IIS_INT_EN**

Description : IIS interrupt enable register

0x0018			Interrupt enable (Reset 0x0000_0000)												IIS_INT_EN	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								TXF_EMPTY_INT_EN	RXF_FULL_INT_EN	TIME_OUT_INT_EN	RX_OVF_INT_EN	Reserved	TXF_FULL_INT_EN	RXF_EMPTY_INT_EN	Reserved
Type	RO								R/W	R/W	R/W	R/W	RO	R/W	R/W	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_EMPTY_INT_EN	[7]	R/W	1'h0	Tx_fifo_empty interrupt enable
RXF_FULL_INT_EN	[6]	R/W	1'h0	Rx_fifo_full interrupt enable
TIME_OUT_INT_EN	[5]	R/W	1'h0	Slave mode timeout interrupt enable
RX_OVF_INT_EN	[4]	R/W	1'h0	Rx_overrun_reg interrupt enable

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reserved	[3]	R/W	1'h0	
TXF_FUL_INT_EN	[2]	R/W	1'h0	Tx_fifo_full interrupt enable
RXF_EMPTY_INT_EN	[1]	R/W	1'h0	Rx_fifo_empty interrupt enable
Reserved	[0]	R/W	1'h0	

6.4.5.2.8 **IIS_INT_CLR**

Description：IIS interrupt clear register

0x001C			Interrupt clear (Reset 0x0000_0000)										IIS_INT_CLR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										TIME_OUT_INT_CLR	RX_OVF_INT_CLR	Reserved	TXF_FULL_INT_CLR	RXF_EMPTY_INT_CLR	Reserved
Type	RO										WO	WO	RO	WO	WO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TIME_OUT_INT_CLR	[5]	WO	1'h0	Write "1" clear slave mode timeout interrupt
RX_OVF_INT_CLR	[4]	WO	1'h0	Write "1" clear Rx_overrun_reg interrupt
Reserved	[3]	RO	1'h0	
TXF_FULL_INT_CLR	[2]	WO	1'h0	Write "1" clear Tx_fifo_full interrupt
RXF_EMPTY_INT_CLR	[1]	WO	1'h0	Write "1" clear Rx_fifo_empty interrupt
Reserved	[0]	RO	1'h0	

6.4.5.2.9 **IIS_INT_RAW_STS**

Description：IIS interrupt raw status

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0020			Raw status (Reset 0x0000_008A)										IIS_INT_RAW_STS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								TXF_EMPTY_RAW_STS	RXF_FULL_RAW_STS	TIME_OUT_RAW_STS	RX_OVF_RAW_STS	TX_FIFO_EMPTY_W	TXF_FULL_RAW_STS	RXF_EMPTY_RAW_STS	RX_FIFO_FULL_R
Type	RO								RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0

Field Name	Bit	R/W	Reset Value	Description
TXF_EMPTY_RAW_STS	[7]	RO	1'h1	Raw txf_empty interrupt, This bit is set when the number of tx fifo data byte is less than the tx empty watermark value. Auto cleared when the condition disappears.
RXF_FULL_RAW_STS	[6]	RO	1'h0	Raw rxf_full interrupt.This bit is set when the number of rx fifo data byte is larger than the rx full watermark value. Auto cleared when the condition disappears.
TIME_OUT_RAW_STS	[5]	RO	1'h0	Raw slave mode time out interrupt
RX_OVF_RAW_STS	[4]	RO	1'h0	Raw Rx_overrun_reg interrupt
TX_FIFO_EMPTY_W	[3]	RO	1'h1	Txf_empty_w(for debug)
TXF_FULL_RAW_STS	[2]	RO	1'h0	Raw Tx_fifo_full interrupt
RXF_EMPTY_RAW_STS	[1]	RO	1'h1	Raw rx_fifo_empty interrupt
RX_FIFO_FULL_R	[0]	RO	1'h0	Rxf_full_r(for debug)

6.4.5.2.10 **IIS_INT_MASK_STS**

Description：IIS interrupt mask status

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0024			Mask status (Reset 0x0000_0000)										IIS_INT_MASK_STS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	Reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								TXF_EMPTY_MASK_STS	RXF_FULL_MASK_STS	TIME_OUT_MASK_STS	RX_OVF_MASK_STS	Reserved	TXF_FULL_MASK_STS	RXF_EMPTY_MASK_STS	Reserved
Type	RO								RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_EMPTY_MASK_STS	[7]	RO	1'h0	Txf_empty interrupt mask status.
RXF_FULL_MASK_STS	[6]	RO	1'h0	Rxf_full interrupt mask status.
TIME_OUT_MASK_STS	[5]	RO	1'h0	Slave mode time out interrupt mask status
RX_OVF_MASK_STS	[4]	RO	1'h0	Rx_overrun_reg interrupt mask status
Reserved	[3]	RO	1'h0	
TX_FIFO_FULL_MASK_STS	[2]	RO	1'h0	Tx_fifo_full interrupt mask status
RX_FIFO_EMPTY_MASK_STS	[1]	RO	1'h0	Rx_fifo_empty interrupt mask status
Reserved	[0]	RO	1'h0	

6.4.5.2.11 **IIS_STS1**

Description：IIS RX FIFO write address and read address

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0028			RXF address (Reset 0x0000_0000)												IIS_STS1	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			RXF_WR_ADDR					Reserved			RXF_RD_ADDR				
Type	RO			RO					RO			RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
RXF_WR_ADDR	[12:8]	RO	5'h0	RX FIFO write address
Reserved	[7:5]	RO	3'h0	
RXF_RD_ADDR	[4:0]	RO	5'h0	RX FIFO read address

6.4.5.2.12 **IIS_STS2**

Description : IIS status register

0x002C			Status register (Reset 0x0000_10AA)												IIS_STS2	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			IIS_LRCK	IIS_CLK	IIS_DO	IIS_DI	BUSY	TXF_REALEMPTY	TXF_REALFULL	RXF_REALEMPTY	RXF_REALFULL	TXF_EMPTY	TXF_FULL	RXF_EMPTY	RXF_FULL
Type	RO			RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	1	0	0	0	0	1	0	1	0	1	0	1	0

Field Name	Bit	R/W	Reset Value	Description
IIS_LRCK	[12]	RO	1'h1	IIS_LRCK, for debug
IIS_SCK	[11]	RO	1'h0	IIS_SCK, for debug
IIS_DO	[10]	RO	1'h0	IIS_DO, for debug
IIS_DI	[9]	RO	1'hX	IIS_DI, for debug
BUSY	[8]	RO	1'h0	BUSY, for debug
TXF_REALEMPTY	[7]	RO	1'h1	TX FIFO is real empty. TX FIFO has no data

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

TXF_REALFULL	[6]	RO	1'h0	TX FIFO is real full.(not relates to register TXF_FULL_THLD)
RXF_REALEMPTY	[5]	RO	1'h1	RX FIFO is real empty. RX FIFO has no data
RXF_REALFULL	[4]	RO	1'h0	RX FIFO is real full.(not relates to register RXF_FULL_THLD)
TXF_EMPTY	[3]	RO	1'h1	This bit is set when the number of TX FIFO data byte is less than the TX empty watermark value. Auto cleared when the condition disappears.
TXF_FULL	[2]	RO	1'h0	This bit is set when the number of TX FIFO data byte is larger than the TX full watermark value. Auto cleared when the condition disappears.
RXF_EMPTY	[1]	RO	1'h1	This bit is set when the number of RX FIFO data byte is less than the RX empty interrupt watermark value. Auto cleared when the condition disappears.
RXF_FULL	[0]	RO	1'h0	This bit is set when the number of RX FIFO data byte is larger than the RX full watermark value. Auto cleared when the condition disappears.

6.4.5.2.13 **IIS_STS3**

Description：IIS status register

0x0030			Status register(Reset 0x0000_0000)										IIS_STS3			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LRCKCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
LRCKCNT	[15:0]	RO	16'h0	Number of clk_iis cycle per SCK cycle or LRCK cycle , depends on ctl1[12].

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.4.5.2.14 **IIS_DSPWAIT**

Description：This register is used for DSP control

0x0034			Control register(Reset 0x0000_0001)										IIS_DSPWAIT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved					IIS_BUS_MODE	TX_DATA_SWT		RX_DATA_SWT		TX_DMA_SEL	RX_DMA_SEL	IIS_DSPWAIT			
Type	RO					R/W	R/W		R/W		R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Field Name	Bit	R/W	Reset Value	Description
IIS_BUS_MODE	[10]	R/W	1'h0	0: iis use 32bit APB bus, 1: iis use 16bit APB bus
TX_DATA_SWT	[9:8]	R/W	2'h0	TX FIFO write data endian for : 0: = wdata[31:0] (APB wdata) 1: ={wdata[7:0], wdata[15:8], wdata[23:16], wdata[31:24]} (APB wdata) 2: = {wdata[15:0],wdata[31:16]} (ABP wdata)
RX_DATA_SWT	[7:6]	R/W	2'h0	RX FIFO read data endian for APB rdata : 0: = rdata[31:0] (FIFO read data) 1: =rdata[7:0], rdata[15:8], rdata[23:16], rdata[31:24]} 2: = {rdata[15:0],rdata[31:16]}
TX_DMA_SEL	[5]	R/W	1'h0	TX DMA request type select: 0: request auto clear or by ack feed back from DMA 1: request clear only by ack feed back from DMA
RX_DMA_SEL	[4]	R/W	1'h0	RX DMA request type select: 0: request auto clear or by ack feed back from DMA 1: request clear only by ack feed back from DMA

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

IIS_DSPWAIT	[3:0]	R/W	4'h1	This register is used for DSP control

6.4.5.2.15 **IIS_CTL4**

Description：IIS TX FIFO full/empty watermark register

0x0038			TXF watermark (Reset 0x0000_0808)												IIS_CTL4	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			TXF_EMPTY_THLD					Reserved			TXF_FULL_THLD				
Type	RO			R/W					RO			R/W				
Reset	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_EMPTY_THLD	[12:8]	R/W	5'h8	TX FIFO data empty threshold
Reserved	[7:5]	R/W	3'h0	
TXF_FULL_THLD	[4:0]	R/W	5'h8	TX FIFO data full threshold

6.4.5.2.16 **IIS_STS4**

Description：IIS TXF FIFO write address and read address

0x003C			TXF address (Reset 0x0000_0000)												IIS_STS4	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			TXF_WR_ADDR					Reserved			TXF_RD_ADDR				
Type	RO			RO					RO			RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
TXF_WR_ADDR	[12:8]	RO	5'h0	TX FIFO write address

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reserved	[7:5]	RO	3'h0	
TXF_RD_ADDR	[4:0]	RO	5'h0	TX FIFO read address

6.4.5.2.17 **IIS_CTL5**

Description：IIS slave dummy bit mode control register

0x0040			TXF watermark (Reset 0x0000_0000)										IIS_CTL4			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								IIS_DUMMY_DEBUG	IIS_CLK_DVDR_CLR	IIS_CLK_DVDR_MD1	IIS_CLK_DVDR_MD0	IIS_SCK_AON	Reserved for debug	IIS_SCK_DUMMY_MODE1	IIS_SCK_DUMMY_MODE0
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
Reserved	[31:8]	RO	24'h0	
IIS_DUMMY_DEBUG	[7]	R/W	1'h0	1: when IIS_CTL5[5]=1 and IIS_CTL0[5]=1. 0: others. Note: iis working on fraction mode1 and channel width = 32bit, IIS_DUMMY_DEBUG is set to 1.
IIS_CLK_DVDR_CLR	[6]	R/W	1'h0	Only used for debug.
IIS_CLK_DVDR_MD1	[5]	R/W	1'h0	For only IIS master mode, this bit is used to select output serial clock mode. 0: iis_sck is integrally divided from clk_iis. Refer to IIS_CLKD for detailed. 1: iis_sck is fractionally divided from clk_iis. iis_sck = 1/2 * clk_iis / (IIS_CLKD + 1) iis_sck * (IIS_CLKM / IIS_CLKN) = target sample rate * channel number * channel length Note1: the frequency of iis_sck is fixed. But the actual sample rate is variable, and only average is target sample rate. Note2: if IIS_CLK_DVDR_MD1 is 1, IIS_CLK_DVDR_MD0 must be 0.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				Note3: IIS_CLKM must be not more than IIS_CLKN. Note4: Compared with MD0, the advantage of MD1 is that iis_sck is fixed, but the disadvantage is that the jitter of sample rate is higher. MD0 is preferred normally except system needs fixed iis_sck.
IIS_CLK_DVDR_MD0	[4]	R/W	1'h0	For IIS/PCM master mode, this bit is used to select output serial clock mode. 0: iis_sck is integrally divided from clk_iis. Refer to IIS_CLKD for detailed. 1: iis_sck is fractionally divided from clk_iis. target iis_sck = 1/2 * clk_iis * (IIS_CLKM / IIS_CLKN) target iis_sck = sample rate * channel number * channel length Note1: the actual frequency of iis_sck is variable, and only average is target frequency. Because of this variability, the iis_lrck frequency is also variable, and only average is target sample rate. Note2: if IIS_CLK_DVDR_MD0 is 1, IIS_CLK_DVDR_MD1 must be 0. Note3: IIS_CLKM must be not more than IIS_CLKN.
IIS_SCK_AON	[3]	R/W	1'h0	iis_sck always-on enable bit in master mode. 0: serial clock is issued only during RX/TX 1: serial clock is always-on
Reserved for debug	[2]	R/W	1'h0	Reserved for debug
IIS_SCK_DUMMY_MODE0	[1]	R/W	1'h0	Dummy mode for IIS compatible mode
IIS_SCK_DUMMY_MODE0	[0]	R/W	1'h0	Dummy mode for IIS justified mode

6.4.5.2.18 **IIS_CLKML**

Description : Fraction clock divider: M[15:0]

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0050			Fraction clock divider: M[15:0] (Reset 0x0000_0000)										IIS_CLKML			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	IIS_CLKML															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
IIS_CLKML	[15:0]	R/W	16'h0	Specify the low 16 bits of fraction clock divider M (M[15:0])

6.4.5.2.19 **IIS_CLKMH**

Description：Fraction clock divider: M[21:16]

0x0054			Fraction clock divider: M[21:16] (Reset 0x0000_0000)										IIS_CLKMH			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										IIS_CLKMH					
Type	RO										R/W					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
IIS_CLKMH	[5:0]	R/W	6'h0	Specify the high 6 bits of fraction clock divider M (M[21:16])

6.4.5.2.20 **IIS_CLKNL**

Description：Fraction clock divider: N[15:0]

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0058			Fraction clock divider: N[15:0] (Reset 0x0000_0000)										IIS_CLKNL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	IIS_CLKNL															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
IIS_CLKNL	[15:0]	R/W	16'h0	Specify the low 16 bits of fraction clock divider N (N[15:0])

6.4.5.2.21 **IIS_CLKNH**

Description：Fraction clock divider: N[21:16]

0x005C			Fraction clock divider: N[21:16] (Reset 0x0000_0000)										IIS_CLKNH			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										IIS_CLKNH					
Type	RO										R/W					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
IIS_CLKNH	[5:0]	R/W	6'h0	Specify the high 6 bits of fraction clock divider N (N[21:16])

6.4.6 Application notes

6.4.6.1 IIS Program examples

1. Justified format, master, 16 bits per-channel, LRCK low for left, Program control register:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

iis_clkd = 32’0000_000a

iis_ctl0 = 32’h0000_08d1

iis_ctl1 = 32’h0000_0f11

iis_ctl2 = 32’h0000_0000

2. IIS format, master , 8 bits per-channel, LRCK high for left,Program control register:

iis_clkd = 32’0000_000a

iis_ctl0 = 32’h0000_0dc1

iis_ctl1 = 32’h0000_0f11

iis_ctl2 = 32’h0000_0000

3. DSP (sync) format, master, 16 bits per-channel, MSB is available on the 1st rising edge, Program control register

iis_clkd = 32’0000_000a

iis_ctl0 = 32’h0000_0ad1

iis_ctl1 = 32’h0000_0f11

iis_ctl2 = 32’h0000_0000

4. DSP format, master, 16 bits per-channel, MSB is available on the 1st rising edge , Program control register:

iis_clkd = 32’0000_000a

iis_ctl0 = 32’h0000_0ed1

iis_ctl1 = 32’h0000_3f11

iis_ctl2 = 32’h0000_7800

5. Justified mode, slave, 8 bits per-channel, enable clock counter, Program control register:

iis_ctl0 = 32’h0000_08c9

iis_ctl1 = 32’h0000_3f22

iis_ctl2 = 32’h0000_0000

6.4.6.2 PCM program examples

Setting IIS_CTL0 register bit[15] to “1” enables IIS module working in PCM mode.

1. Long Frame format, master, 8 bits per-channel, RX at falling edge, TX at rising edge, Program control register:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

iis_clkd = 32’0000_000a

iis_ctl0 = 32’h0000_80c1

iis_ctl1 = 32’h0000_0f11

iis_ctl2 = 32’h0000_0001

2. Short Frame format, master, 8 bits per-channel,

iis_clkd = 32’0000_000a

iis_ctl0 = 32’h0000_81c1

iis_ctl1 = 32’h0000_0f11

iis_ctl2 = 32’h0000_0001

3. Multi-cycle format, master, 8 bits per-channel, pcm_oe=1,pcm_cyc=1, slot0 is occupied

iis_clkd = 32’0000_000a

iis_ctl0 = 32’h0000_80c1

iis_ctl1 = 32’h0000_0f11

iis_ctl2 = 32’h0000_0409

4. Muti-cycle format, master, 8 bits per-channel, pcm_cyc=2, slot0 and slot1 are occupied

iis_clkd = 32’0000_000a

iis_ctl0 = 32’h0000_80c1

iis_ctl1 = 32’h0000_0f11

iis_ctl2 = 32’h0000_0013

5. Long frame format, slave, 16 bits per-channel, enable clock count,

iis_ctl0 = 32’h0000_80c9

iis_ctl1 = 32’h0000_3f11

iis_ctl2 = 32’h0000_0001

6. Short frame format , slave, 16 bits per-channel, enable clock count,

iis_ctl0 = 32’h0000_81cd

iis_ctl1 = 32’h0000_3a1

iis_ctl2 = 32’h0000_0001

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.4.6.3 Clock dividing modes

In master mode, the IIS serial clock iis_sck is sent from the IIS module, and this clock is divided from clk_iis. IIS module provides three modes for clock dividing.

1. Integer clock dividing mode

- Both IIS and PCM master support this mode.
- This mode can be used only if iis_sck is integrally divided from clk_iis.
- Mode enable: IIS_CLK_DVDR_MD0 = 0 and IIS_CLK_DVDR_MD1 = 0
- Only IIS_CLKD is used for dividing; IIS_CLKM and IIS_CLKN are DON'T CARE.
- IIS_CLKD = (clk_iis / (2 * iis_sck)) - 1; iis_sck = sample rate * channel number * channel length
- For example, if clk_iis runs at 153.6MHz, and IIS module is configured as 48K sample rate, 2 channel and 16-bit channel length, iis_sck should be 48K * 2 * 16 = 1.536MHz, IIS_CLKD should be (153.6M / (2 * 1.536M)) - 1 = 49

2. Fraction clock dividing mode0

- Both IIS and PCM master support this mode.
- In this mode, the actual frequency of iis_sck is variable, and only average is target frequency. Because of this variability, the iis_lrck frequency is also variable, and only average is target sample rate.
- Mode enable: IIS_CLK_DVDR_MD0 = 1 and IIS_CLK_DVDR_MD1 = 0
- IIS_CLKM and CLKN are used for dividing; but IIS_CLKD is DON'T CARE.
- IIS_CLKM / IIS_CLKN = 2 * (target iis_sck) / clk_iis; (target iis_sck) = sample rate * channel number * channel length
- IIS_CLKM = 2 * sample rate (Hz) * channel number * channel length / 100
- IIS_CLKN = clk_iis (Hz) / 100
- For example, if clk_iis runs at 153.6MHz, and IIS module is configured as 44.1K sample rate, 2 channel and 16-bit channel length, IIS_CLKM = 2 * 44100 * 2 * 16 / 100 = 28224, IIS_CLKN = 153600000 / 100 = 1536000.

3. Fraction clock dividing mode1

- Only IIS master supports this mode.
- In this mode, the frequency of iis_sck is fixed. But the actual sample rate is variable, and only average is target sample rate.
- Compared with MD0, the advantage of MD1 is that iis_sck is fixed, but the disadvantage is that the jitter of sample rate is higher.
- Mode enable: IIS_CLK_DVDR_MD0 = 0 and IIS_CLK_DVDR_MD1 = 1
- IIS_CLKM, CLKN and CLKD are used for dividing.
- IIS_CLKD = (clk_iis / (2 * iis_sck)) – 1
- IIS_CLKM / IIS_CLKN = (target sample rate) * channel number * channel length / iis_sck; IIS_CLKM must be not more than IIS_CLKN.
- IIS_CLKM = 2 * (IIS_CLKD + 1) * (target sample rate) * channel number * channel length / 100
- IIS_CLKN = clk_iis / 100
- The iis_sck (or IIS_CLKD) should be decided by software. iis_sck must be not lower than ((target sample rate) * channel number * channel length). And iis_sck should be not too high for timing issue. Usually iis_sck is a little bit higher than ((target sample rate) * channel number * channel length).
- For example, if clk_iis runs at 153.6MHz, and IIS module is configured as 44.1K sample rate, 2 channel and 16-bit channel length. Firstly, we choose iis_sck as 153.6M / (2 * (44 + 1)) = 1.706667MHz because ((target sample rate) * channel number * channel length) = 1.4112MHz and 1.706667MHz is a little bit higher than 1.4112MHz. IIS_CLKD = 44, IIS_CLKM = 2 * (44 + 1) * 44100 * 2 * 16 / 100 = 1270080, IIS_CLKN = 153600000 / 100 = 1536000.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

4. Some guidelines for clock dividing modes

- Integer clock dividing mode is preferred if possible, because this mode has fixed serial clock frequency and fixed sample rate.
- If iis_sck cannot be integrally divided from clk_iis, we choose fraction clock dividing modes. If system needs fixed serial clock frequency, mode1 is chosen. Otherwise mode0 is preferred for small sample rate jitter.
- IIS master supports both mode0 and mode1, and PCM master supports only mode0.
- The frequency options of clk_iis depend on different chips. But 153.6MHz is always preferred because this frequency can be divided integrally to support 48K, 24K, 12K, 32K, 16K and 8K sample rate.

5. Fraction clock divide mode1 configure

Table 7 IIS configure for fraction clock divide

MD0, MSB-justified	**Master**	**Slave**
IIS_CTL[5]	0	x(don't care)
IIS_CTL[4]	1	x(don't care)
IIS_CTL[1]	x(don't care)	x(don't care)
IIS_CTL[0]	x(don't care)	x(don't care)
MD0, compatible	**Master**	**Slave**
IIS_CTL[5]	0	x(don't care)
IIS_CTL[4]	1	x(don't care)
IIS_CTL[1]	x(don't care)	x(don't care)
IIS_CTL[0]	x(don't care)	x(don't care)
MD1, MSB-justified	**Master**	**Slave**
IIS_CTL[5]	1	x(don't care)
IIS_CTL[4]	0	x(don't care)
IIS_CTL[1]	x(don't care)	0
IIS_CTL[0]	x(don't care)	1
MD1, compatible	**Master**	**Slave**
IIS_CTL[5]	1	x(don't care)
IIS_CTL[4]	0	x(don't care)
IIS_CTL[1]	x(don't care)	1
IIS_CTL[0]	x(don't care)	0

Table 8 iis_clk confiugure suggestion

iis mode	rate	width	clk_iis
compatible	192k	32	153.6M(Suggest)
compatible	192k	32	128M(Suggest)
compatible	192k	32	80M(Not Suggested)
compatible	192k	32	26M(Not Suggested)
compatible	192k	16	153.6M(Suggest)
compatible	192k	16	128M(Suggest)
compatible	192k	16	80M(Suggest)
compatible	192k	16	26M(Not Suggested)
compatible	192k	8	153.6M

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

compatible	192k	8	128M
compatible	192k	8	80M
compatible	192k	8	26M
compatible	44.1k	32	153.6M
compatible	44.1k	32	128M
compatible	44.1k	32	80M
compatible	44.1k	32	26M
compatible	44.1k	16	153.6M
compatible	44.1k	16	128M
compatible	44.1k	16	80M
compatible	44.1k	16	26M
compatible	44.1k	8	153.6M
compatible	44.1k	8	128M
compatible	44.1k	8	80M
compatible	44.1k	8	26M
Justified	192k	32	153.6M(Suggest)
Justified	192k	32	128M(Suggest)
Justified	192k	32	80M(Not Suggested)
Justified	192k	32	26M(Not Suggested)
Justified	192k	16	153.6M(Suggest)
Justified	192k	16	128M(Suggest)
Justified	192k	16	80M(Suggest)
Justified	192k	16	26M(Not Suggested)
Justified	192k	8	153.6M
Justified	192k	8	128M
Justified	192k	8	80M
Justified	192k	8	26M
Justified	44.1k	32	153.6M
Justified	44.1k	32	128M
Justified	44.1k	32	80M
Justified	44.1k	32	26M
Justified	44.1k	16	153.6M
Justified	44.1k	16	128M
Justified	44.1k	16	80M
Justified	44.1k	16	26M

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Justified	44.1k	8	153.6M
Justified	44.1k	8	128M
Justified	44.1k	8	80M
Justified	44.1k	8	26M

Note :

- In IIS fraction clock divide mode1, clk_iis frequency should be higher when bit clock is fast.

6.4.6.4 Working mode examples

1. DMA mode,PCM,Slave,16bit

iis_clkd = 32'0000_000a

iis_ctl0 = 32'h0000_c3d9

iis_ctl1 = 32'h0000_0f11

iis_ctl2 = 32'h0000_0001

iis_ctl3 = 32'h0000_0f0f (threshold is half volume of buffer)

iis_int_en=32'h0000_0036

2. Interrupt mode,PCM,slave,16bit

iis_clkd = 32'0000_000a

iis_ctl0 = 32'h0000_83d9

iis_ctl1 = 32'h0000_0f11

iis_ctl2 = 32'h0000_0001

iis_ctl3 = 32'h0000_0f0f (threshold is half volume of buffer)

iis_int_en=32'h0000_00f6

note : iis is same configuration as pcm mode.

6.4.6.5 Debug tips

- To ensure that it is working well, the first step is to test iis_sck, iis_lrck , iis_di, iis_do using scope or by observing state of IIS_STS2.
- In the iis mode, iis_lrck changes periodically, and high/low duty ratio is 50%.In the pcm mode, iis_lrck is a periodical pulse.
- If iis_sck , iis_lrck, iis_di, iis_do is nomal, then you can operate IIS_TXD. Transmitting a word by writing data to IIS_TXD in one side(e.g transmitter). Observe the result by reading data from IIS_TXD in another side(e.g receiver).
- iis working on fraction mode1 and channel width = 32bit, IIS_DUMMY_DEBUG is set to be 1. And in other cases, IIS_DUMMY_DEBUG should set to be 0. IIS_DUMMY_DEBUG bit is added from r5p0 v091 and later versions. It mainly solve bugs when transmitting width is 32

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

bit, sample rate is 192k. In this case, slave will write receiving data to FIFO twice and send msb bit too early in versions older than r5p0 v091.

6.5 I2C interface

6.5.1 Overview

I2C: Inter-Integrated Circuit

2 wire serial system is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices.

The interface defines 3 transmission speeds:

- Standard mode: 100 Kbps
- Fast mode: 400 Kbps
- High-speed mode: 3.5 Mbps

6.5.2 Features

I2C features list

- Software programmable clock frequency
- Software programmable acknowledge bit
- Interrupt driven data-transfers
- Start/Stop/Repeated Start/Acknowledge generation
- Supports Clock Stretching/Wait state generation
- Single Master Operation
- 8 word buffer mode support
- normal ,fast and High-speed modes are supported in this design
- Software programmable duty ratio of clock frequency are supported in this design

6.5.3 Signal description

The 2 wire serial interface uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. Both lines must be pulled-up to VCC by external resistors. The tri-state buffers for the SCL and SDA lines have to be added at a higher hierarchical level.

Connections should be made according to the following figure:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

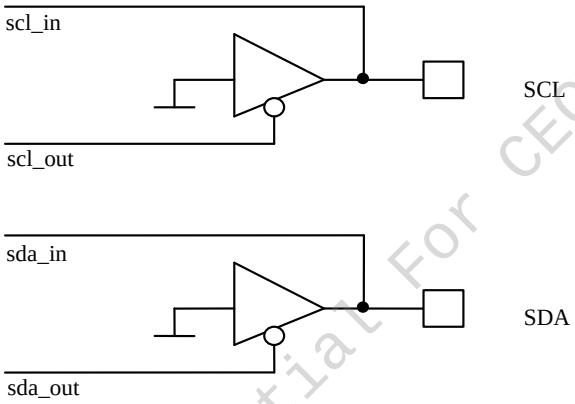


Figure 6.5-1 I2C PAD connection

6.5.4 Funtion description

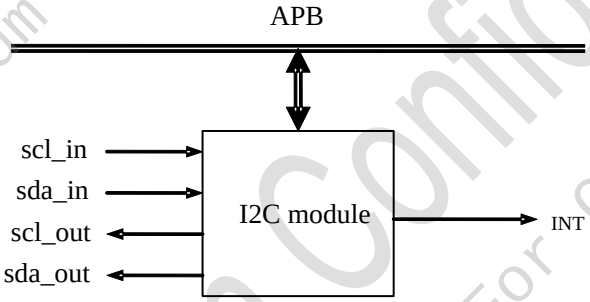


Figure 6.5-2 I2C system diagram

6.5.4.1 System Configuration

The 2 wire serial system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. The logic AND function is exercised on both lines with external pull-up resistors.

The 2 wire serial controller implemented here is a single master device; therefore it starts generating a clock as soon as it is enabled. The user should program this register to the desired value before starting any transfers.

Data is transmitted synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. There is an acknowledge bit following each transferred byte. Each bit is sampled during the high period of SCL; therefore the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP command).

6.5.4.2 Wire Serial Protocol

Normally, a standard communication consists of four parts:

- START signal generation
- Slave address transfer
- Data transfer
- STOP signal generation

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

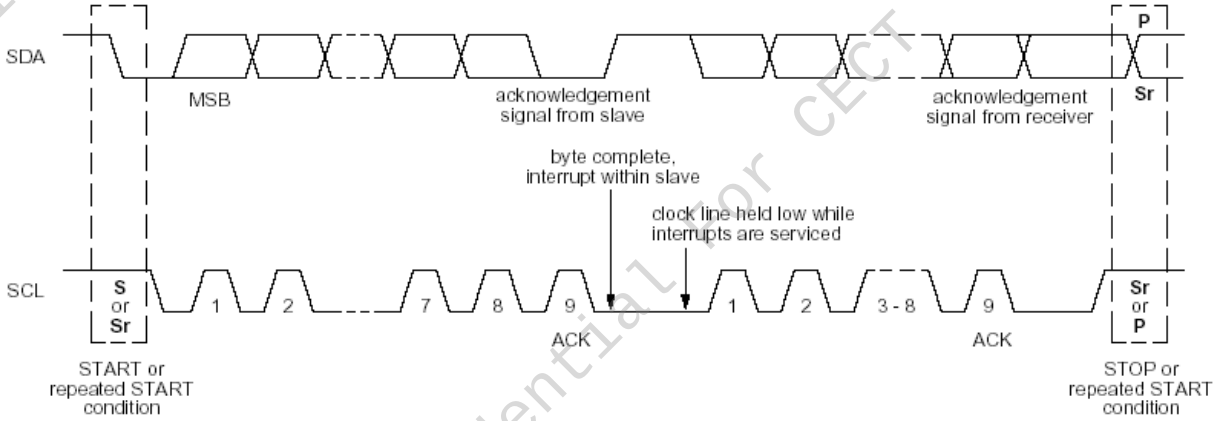


Figure 6.5-3 Data transfer on the I2C-bus

1. START signal

When the bus is free/idle, that is no master device is engaging the bus (both SCL and SDA lines are high), a master can initiate a transfer by sending a START signal. A START signal is defined as a high-to-low transition of SDA while SCL is high. The START signal denotes the beginning of a new data transfer.

A repeated START is a START signal without first generating a STOP signal. The master uses this method to communicate with another slave or the same slave in a different transfer direction (e.g. writing to device to reading from device) without releasing the bus.

The controller generates a START signal when the start bit in the 2ws_command Register is set and the read or write bits are set. Depending on the current status of the SCL line a START or Repeated START is generated.

2. Slave Address Transfer

The first byte of data transferred by the master immediately after the START signal is the slave address. This is a seven-bit calling address followed by a RW bit. The RW bit signals the slave data transfer direction. No two slaves in the system can have the same address. Only the slave with an address that matches the one transmitted by the master will respond by returning an acknowledge bit by pulling the SDA low at the 9th SCL clock cycle.

The controller treats a Slave Address Transfer as any other write action. Store the slave device's address in the 2ws_command register and set the write bit. The controller will then transfer the slave address on the bus.

3. Data Transfer

Once successful slave addressing is achieved, the data transfer can proceed on a byte-by-byte basis in the direction specified by the RW bit sent by the master. Each transferred byte is followed by an acknowledge bit on the 9th SCL clock cycle. If the slave signals a No Acknowledge (NACK), the master can generate a STOP signal to abort the data transfer or generate a repeated START signal and start a new transfer cycle.

If the master, as the receiving device, does not acknowledge the slave, the slave releases the SDA line for the master to generate a STOP or repeated START signal.

For writing data to a slave, store the data to transmit in the 2ws_command register and set the write bit. For reading data from a slave, set the read bit. When the transfer is done, an interrupt is generated to MCU. The 2ws_command bit 8 to bit 15 contains valid data. The user may issue a new write or read command at this time.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

3. STOP signal

The master can terminate the communication by generating a STOP signal. A STOP signal is defined as a low-to-high transition of SDA while SCL is at logical ‘1’.

6.5.4.3 Arbitration Procedure

Since the 2 wire serial controller supports single master configurations only, no Arbitration logic is added to the controller. Only clock synchronization is supported since slave devices can use this mechanism for clock stretching.

1. Clock Synchronization

Since the logical AND function is performed on the signals, a high to low transition on SCL or SDA affect all devices connected to the bus. The SCL clock signal can be synchronized between multiple masters using this feature. Each device starts counting its SCL low period when the current master drives SCL low. Once a device’s clock has gone low, it holds the SCL line low until the clock high state is reached.

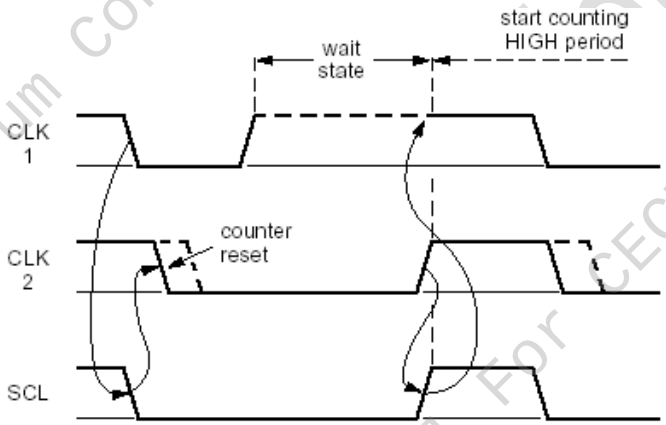


Figure 6.5-4 Clock synchronization during the arbitration procedure

2. Clock Stretching

Slave devices can use the clock synchronization mechanism to slow down the transfer bit rate. After the master has driven SCL low the slave can drive SCL low for the required period and then release it. If the slave’s SCL low period is greater than the master’s SCL low period, the resulting SCL bus signal low period is stretched, thus inserting wait-states.

6.5.4.4 Timing Prameters

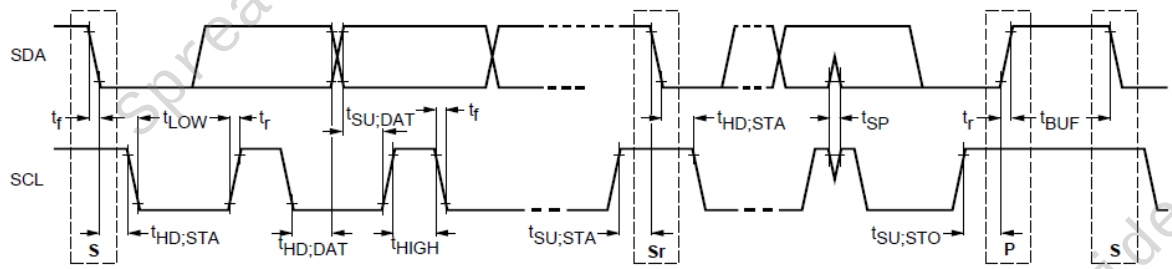


Figure 6.5-5 I2C timing diagram

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Parameter	Description	Standard mode		Fast mode	
		Min	Max	Min	Max
fSCL	SCL clock frequency	0 kHz	100 kHz	0 kHz	400 kHz
tHD;STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0 us	-	0.6 us	-
tLOW	LOW period of the SCL clock	4.7 us	-	1.3 us	-
tHIGH	HIGH period of the SCL clock	4.0 us	-	0.6 us	-
tSU;STA	Set-up time for a repeated START condition	4.7 us	-	0.6 us	-
tHD;DAT	Data hold time	0 us	3.45 us	0	0.9 us
tSU;DAT	Data set-up time	250 ns	-	100 ns	-
tr	Rise time of both SDA and SCL signals	-	1000 ns	20 + 0.1Cb	300 ns
tf	Fall time of both SDA and SCL signals	-	300 ns	20 + 0.1Cb	300 ns
tSU;STO	Set-up time for STOP condition	4.0 us	-	0.6 us	-
tBUF	Bus free time between a STOP and START condition	4.7 us	-	1.3 us	-
Cb	Capacitive load for each bus line	-	400 pF	-	400 pF

6.5.5 Control registers

6.5.5.1 Memory map

Offset Address	Name	Description
0x0000	2WS_CONTROL	2 wire serial system control register
0x0004	2WS_COMMAND	2 wire serial system command register
0x0008	2WS_DIVIDOR0	2 wire serial system dividor register0
0x000C	2WS_DIVIDOR1	2 wire serial system dividor register1
0x0010	2WS_RST	2 wire serial system reset register
0x0014	2WS_CMD_BUF	2 wire serial system command buffer register
0x0018	2WS_CMD_BUF_CTRL	2 wire serial system command buffer control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description
0x001c	2WS_STA_STO_DVD	2 wire serial system tHD sta/ tSU sto divdor register

6.5.5.2 Register description

6.5.5.2.1 2WS_CONTROL

Description : 2 wire serial system control register

0x0000			2ws system control register (Reset 0x0700_0062)										2WS_CONTROL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	I2c revsion															
Type	RO															
Reset	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	I2c_cmd_opt	i2c_dvd_opt	i2c_high_opt	i2c_trim_opt	i2c_out_opt	ws_noack_int_clr	2ws_noack_int_status	2ws_noack_int_en	2ws_sda_line	2ws_scl_line	2ws_en	2ws_ie	2ws_busy	2ws_ack	2ws_int
Type	RO	R/W	R/W	R/W	R/W	R/W	WO	RO	R/W	RO	RO	R/W	R/W	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
I2c_revsion	[31:15]	RO	16'h700	I2c version : r7p0
	[15]	RO	1'h0	Reserved
I2c_cmd_opt	[14]	R/W	1'h0	Command mod bug modify option: 1:no fix ,0:fix
I2c_dvd_opt	[13]	R/W	1'b0	SCL frequency calculation modifies option. 1: (freq_i2c/4*freq_scl)-0.5 = prescale ---r6p0 0: (freq_i2c/4*freq_scl)- 2 = prescale ---r3p0 - Dividor= prescale -1 (no duty ratio) - Dividor + low_dividor = prescale -2 (duty ration)
i2c_hight_opt	[12]	R/W	1'b0	Asynchronous bug modify option. 1:fix 0: no fix.
i2c_trim_opt	[11]	R/W	1'b0	Clock duty ratio modify option 1: enable :adjust the clock duty ratio 0: fix.
i2c_out_opt	[10]	R/W	1'b0	Output Modify Option. 0: enable , 1 : no enable.
2ws_noack_int_clr	[9]	WO	1'b0	2ws no ack response interrupt clear bit

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

2ws_noack_int_status	[8]	RO	1'b0	2ws no ack response interrupt status
2ws_noack_int_en	[7]	R/W	1'b0	2ws no ack response interrupt enable
2ws_sda_line	[6]	RO	1'b1	SDA line signal level
2ws_scl_line	[5]	RO	1'b1	SCL line signal level
2ws_en	[4]	R/W	1'b0	2ws module enable
2ws_ie	[3]	R/W	1'b0	2ws interrupt enable
2ws_busy	[2]	RO	1'b0	2ws data line value
2ws_ack	[1]	RO	1'b1	2ws received acknowledge value
2ws_int	[0]	RO	1'b0	2ws interrupt

6.5.5.2.2 **2WS_COMMAND**

Description： 2 wire serial system command register

0x0004	**2ws system command register (Reset 0x0000_0040)**												**2WS_ COMMAND**			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	2ws_data								2ws_busy	2ws_ack	cmd_start	cmd_stop	cmd_read	cmd_write	tx_ack	int_ack
Type	R/W								RO	RO	R/W	R/W	R/W	R/W	R/W	WO
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Field Name	**Bit**	**Type**	**Reset Value**	**Description**
	[31:16]	RO	16'h0	Reserved
2ws_data	[15:8]	R/W	8'h0	2ws data received or data need to be transmitted
2ws_busy	[7]	RO	1'b0	2ws busy in exec commands, same with 2WS_CONTROL bit 2
2ws_ack	[6]	RO	1'b1	2ws received acknowledge value, same with 2WS_CONTROL bit 1
cmd_start	[5]	R/W	1'b0	2ws start command
cmd_stop	[4]	R/W	1'b0	2ws stop command
cmd_read	[3]	R/W	1'b0	2ws read command
cmd_write	[2]	R/W	1'b0	2ws write command
tx_ack	[1]	R/W	1'b0	2ws transmit acknowledge that need to be send
int_ack	[0]	WO	1'b0	2ws interrupt clear bit

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.5.5.2.3 **2WS_DIVIDOR0**

Description： 2 wire serial system dividor register0

0x0008			2 wire serial system dividor register0 (Reset 0x0040_0040)											2WS_DIVIDOR0		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	2ws_low_dividor0															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	2ws_dividor0															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
2ws_low_dividor0	[31:16]	R/W	16’h40	2ws clock low phase dividor [15:0], default is 0x40
2ws_dividor0	[15:0]	R/W	16’h40	2ws clock dividor [15:0], default is 0x40

6.5.5.2.4 **2WS_DIVIDOR1**

Description： 2 wire serial system dividor register1

0x000C			2 wire serial system dividor register1 (Reset 0x0000_0000)											2WS_DIVIDOR1		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved						2ws_low_dividor1									
Type	RO						R/W									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						2ws_dividor1									
Type	RO						R/W									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:26]	RO	6’h0	Reserved
2ws_low_dividor1	[25:16]	R/W	10’h0	2ws clock low phase dividor [25:16], default is 0x0
	[15:10]	RO	6’h0	Reserved
2ws_dividor1	[9:0]	R/W	10’h0	2ws clock dividor [25:16], default is 0x0

Note:

Change the value of prescale register only when the w2s_control[4] bit is cleared and no need clock duty ratio modify .Due to the structure of the I2C interface, the controller uses “4*SCL” clock internally.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Example: PCLK = 26MHz, desired SCL = 100khz,

prescale = 26MHz/(4*100khz) – 3 = 62 (dec) = 3e (hex)

Reset value : 0x40

6.5.5.2.5 **2WS_RST**

Description： 2 wire serial system reset register

0x0010			2ws system reset register (Reset 0x0000_0000)													2WS_RST
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															2ws_rst
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:1]	RO	31’h0	Reserved
2ws_rst	[0]	R/W	1’b0	Write with bit 0 set to1 1 will reset the 2ws module, it will reset 2WS_CMD_BUF and 2WS_COMMAND registers, and flush command buffer.

6.5.5.2.6 **2WS_CMD_BUF**

Description： 2ws system command buffer register

0x0014			2ws system command buffer register (Reset 0x0000_0000)													2WS_CMD_BUF
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	2ws_cmd_buf															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	31’h0	Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

2ws_cmd_buf	[15:0]	R/W	16'h0	Write command to this register will save the command to the command buffer. Read from this register after the commands are all finished will return the results of the corresponding commands. The format of the command and the return result is the same as i2c_command register.

6.5.5.2.7 **2WS_CMD_BUF_CTRL**

Description： 2 wire serial system command buffer control register

0x0018			2ws command buffer control register (Reset 0x0000_0000)										2WS_CMD_BUF_CTRL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	2ws_ cmdbuf_rptr				2ws_ cmdbuf_wptr				2ws_st_cmdbuf			Reserved		2ws_endian_switch	2ws_cmd_exec	2ws_cmdbuf_en
Type	RO				RO				RO			RO		R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:13]	RO	19'h0	Reserved
2ws_ cmdbuf_rptr	[15:12]	R/W	3'h0	2ws command buffer read pointer
2ws_ cmdbuf_wptr	[11:8]	R/W	3'h0	2ws command buffer write pointer
2ws_st_cmdbuf	[7:5]	R/W	3'h0	The state of 2ws command buffer state machine.
	[4:3]	RO	2'h0	Reserved
2ws_endian_switch	[2]	R/W	1'b0	
2ws_cmd_exec	[1]	R/W	1'b0	Start to exec the command in the command buffer
2ws_cmdbuf_en	[0]	R/W	1'b0	Enable the command buffer mode

6.5.5.2.8 **2WS_STA_STO_DVD**

Description： 2 wire serial system tHD:STA/ tSU STO dividor register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x001C			2 wire serial system sta/sto dvd register (Reset 0x0000_0069)										2WS_STA_STO_DVD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved						2ws_sta_sto_dvd									
Type	RO						R/W									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	2ws_sta_sto_dvd															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1

Field Name	Bit	Type	Reset Value	Description
	[31:26]	RO	6'h0	Reserved
2ws_sta_sto_dvd	[25:0]	R/W	26'h0	2ws clock tHD:STA/ tSU STO phase counter num, default is 0x69

Note:

Change the value of prescale register only when the w2s_control[4] bit is cleared and no need clock duty ratio modify .This register only valid when the w2s_control[11] bit is set to 1.

Reset value :26x4 = 0x68 <0x69

6.5.6 Application notes

List all data formats. Detail the programming flow for the module. For different speed mode, please pay attention to w2s_dividor0 and w2s_dividor1 registers according to frequency of PCLK. For fast mode and high speed mode, command buffer mode is recommended.

- Standard mode; a single master operation; a master-transmitter addressing a slave receiver with a 7-bit address; single common mode

```
w2s_rst              = 0x0000;          //
w2s_dividor0   = 0x0040;          //
w2s_dividor1   = 0x0000;          //
w2s_control          = 0x0018;          // 2ws_en = 1; 2ws_ie = 1
w2s_command= 0x9C25;          // 1001110    0   0010 0101
                                   // ADDRESS  W    S    W lack
w2s_command= 0xFE05;          // 11111110   0000 0101
                                   //  DATA
w2s_command= 0xFE15;          // 11111110   0001 0101
                                   // DATA          P
```

- Fast mode; a single master operation; combined format; 7-bit address; common buffer mode: a burst of 16 commands is written to the buffer

```
w2s_rst              = 0x0000;          //
w2s_dividor0   = 0x0040;          //
```


This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

```
w2s_dividor1    = 0x0000;           //
w2s_control           = 0x0098;           // noack_int_en=1; 2ws_en=1; 2ws_ie=1
w2s_cmd_buf_ctrl      = 0x0001;           // 2ws_cmdbuf_en=1

w2s_cmd_buf  = 0x9C25;              // write to command buffer, WR command
w2s_cmd_buf  = 0x2005;              // write to command buffer, WR command
w2s_cmd_buf  = 0x9D15;              // write to command buffer, WR command
w2s_cmd_buf  = 0x001B;              // write to command buffer, RD command
w2s_cmd_buf  = 0x9C25;              // write to command buffer, WR command
w2s_cmd_buf  = 0x2005;              // write to command buffer, WR command
w2s_cmd_buf  = 0x9D15;              // write to command buffer, WR command
w2s_cmd_buf  = 0x001B;              // write to command buffer, RD command
w2s_cmd_buf  = 0x9C25;              // write to command buffer, WR command
w2s_cmd_buf  = 0x2005;              // write to command buffer, WR command
w2s_cmd_buf  = 0x9D15;              // write to command buffer, WR command
w2s_cmd_buf  = 0x001B;              // write to command buffer, RD command
w2s_cmd_buf  = 0x9C25;              // write to command buffer, WR command
w2s_cmd_buf  = 0x2005;              // write to command buffer, WR command
w2s_cmd_buf  = 0x9D15;              // write to command buffer, WR command
w2s_cmd_buf  = 0x001B;              // write to command buffer, RD command

w2s_cmd_buf_ctrl      = 0x0003;           // 2ws_cmdbuf_en=1; 2ws_cmdbuf_exec=1
```

Get interrupt when all commands in command buffer are complete

```
w2s_cmd_buf  = 0x9C00;              // read from command buffer, WR command
w2s_cmd_buf  = 0x2000;              // read from command buffer, WR command
w2s_cmd_buf  = 0x9D00;              // read from command buffer, WR command
w2s_cmd_buf  = 0xXX1B;              // read from command buffer, RD command
w2s_cmd_buf  = 0x9C00;              // read from command buffer, WR command
w2s_cmd_buf  = 0x2000;              // read from command buffer, WR command
w2s_cmd_buf  = 0x9D00;              // read from command buffer, WR command
w2s_cmd_buf  = 0x001B;              // read from command buffer, RD command
w2s_cmd_buf  = 0x9C00;              // read from command buffer, WR command
w2s_cmd_buf  = 0x2000;              // read from command buffer, WR command
w2s_cmd_buf  = 0x9D00;              // read from command buffer, WR command
w2s_cmd_buf  = 0xXX1B;              // read from command buffer, RD command
w2s_cmd_buf  = 0x9C00;              // read from command buffer, WR command
w2s_cmd_buf  = 0x2000;              // read from command buffer, WR command
w2s_cmd_buf  = 0x9D00;              // read from command buffer, WR command
w2s_cmd_buf  = 0xXX1B;              // read from command buffer, RD command
```


This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

If all commands in command buffer are write commands, no need to read command buffer

```
w2s_cmd_buf  = 0x2005;              // write to command buffer, WR command
w2s_cmd_buf  = 0x9D15;              // write to command buffer, WR command
w2s_cmd_buf  = 0x001B;              // write to command buffer, RD command
w2s_cmd_buf_ctrl      = 0x0003;             // 2ws_cmdbuf_en=1; 2ws_cmdbuf_exec=1

w2s_cmd_buf  = 0x2000;              // read from command buffer, WR command
w2s_cmd_buf  = 0x9D00;              // read from command buffer, WR command
          w2s_cmd_buf      = 0xXX1B;          // read from command buffer, RD command
```

6.6 Keypad interface

6.6.1 Overview

Here Keypad means “keypad controller” which is one APB device in ARM system. The keypad controller scans the external “key matrix” whose maximum size is 8 rows x 8 columns. It scans the “key matrix” row by row and checks the keys of the row one by one. There are at most four keys “pressed”. “released” status can be detected in the same time, which is the so called “multi-key detection”. On the other hand, one pressed key can generate multi interrupts periodically to software and this mode is named the “long key” mode.

For the reason that the external “key matrix” is pure mechanical, if the geometric shape constituted by any three “pressed keys” is a “right-angled triangle “, the keypad controller will detect another “inductive pressed” key. For example, if key 1 (x1, y1), key 2 (x2, y2), key 3 (x1, y2) are pressed then the key 4 (x2, y1) will also be detected as the “pressed” key. The keypad controller will check the geometric shape constituted by the three “pressed keys” and if above condition is detected one “error” status will be reported to software, which should discard current error multi-keys combination.

Finally, low power of the keypad controller is very important. If the controller finds that none key is pressed in the specific time, the clock of most logic inside the controller will be disabled to save power and controller goes into the sleep mode. In the sleep mode controller will be sensitive to any change of the “key matrix”. In other words, any key’s press or release will wakes up the controller to scan the “key matrix”.

6.6.2 Features

- Support maximum 8 row x 8 column key matrix and size is programmable
- Support at most four keys detection under “multi-key” mode
- Support “long key” or “single key” mode for any pressed key
- Support “right-angled triangle” geometric shape detection for the pressed keys
- Support sleep mode to save power
- Support programmable “de-bounce” time for key’s press and release
- Support programmable I/O polarity
- Support programmable scan speed
- Support detecting GPIO connection with one row multi columns

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.6.3 Signal description

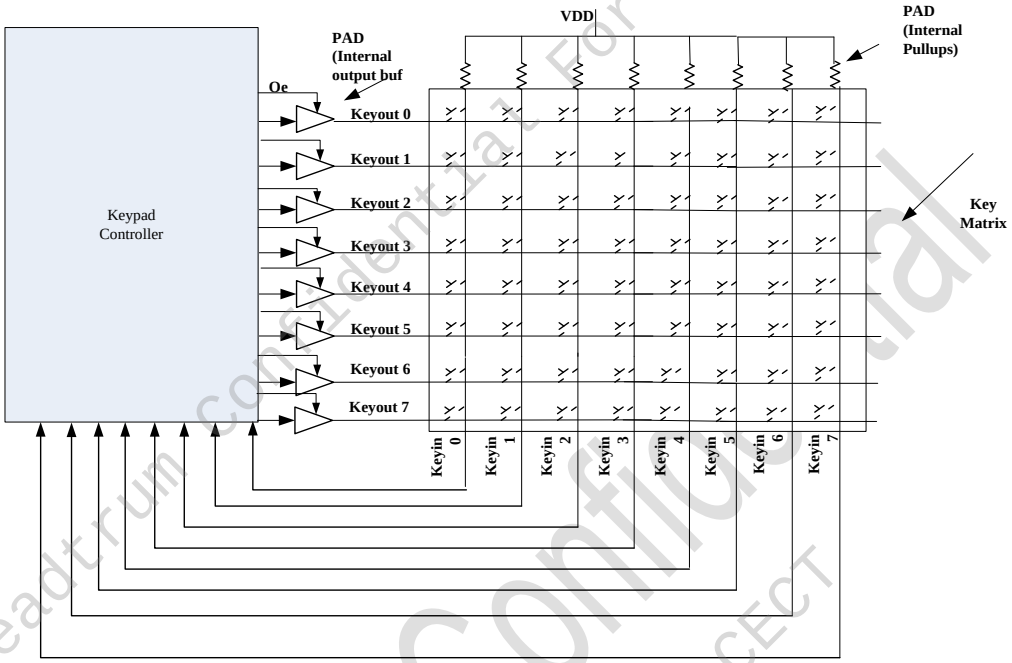


Figure 6.6-1 Keypad connection with external key matrix

The above diagram shows how to interface the keypad controller and the key matrix with pad internal pull-up resistance when the key matrix is 8 rows x 8 columns. For key matrix, the input is keyout 0 ~ keyout 7 and the output is the keyin 0 ~ keyin 7. Every keyout signal can be enabled or disabled. The keyout signal will be forced to be “low level” when it is enabled and only one keyout should be enabled at any time during scanning.

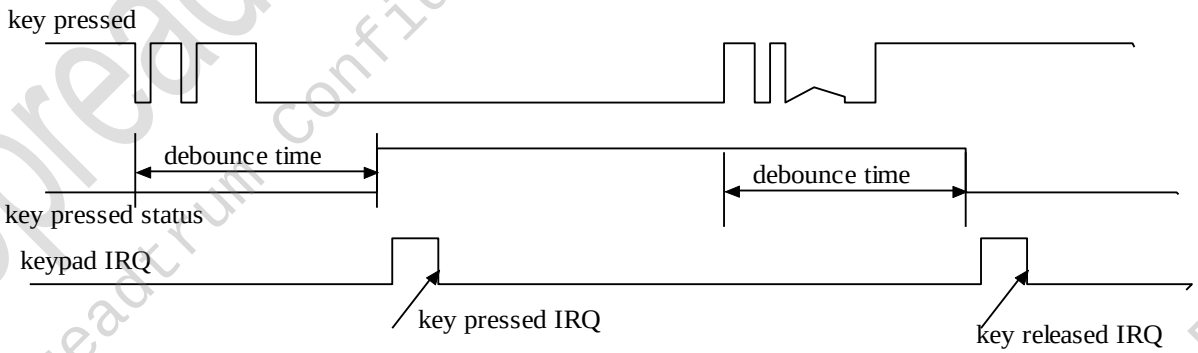


Figure 6.6-2 Single-key mode

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

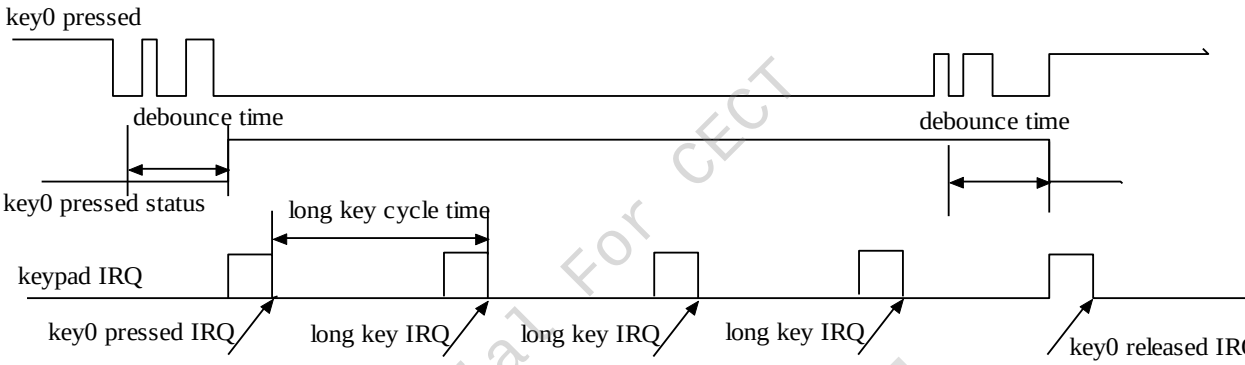


Figure 6.6-3 Long-key mode

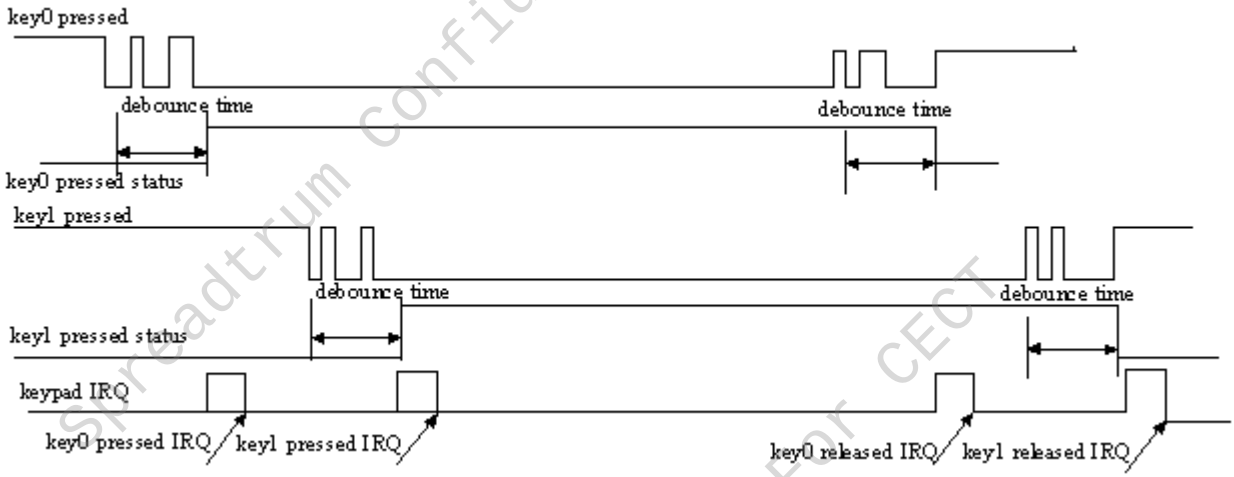


Figure 6.6-4 Multi-key mode

In order to reduce chip PAD, GPIO only uses one switch to connect Keyin0 and GND. Comparing with Figure1.1-1, row scan output signal Keyout is not used. If r3p0 version KPD works in GPIO connection showing as following. r3p0 version KPD will detect two keys pressed, but there is only one key is pressed actually. If we press two keys, it shows four keys was pressed.

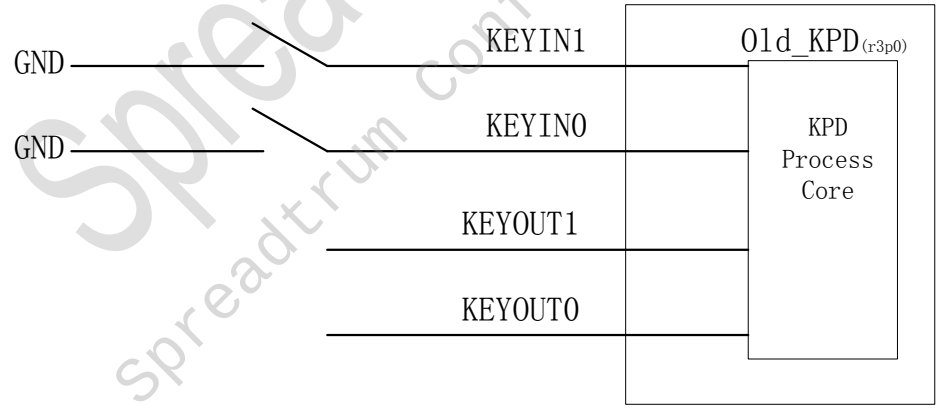


Figure 6.6-5 GPIO connection with old KPD (r3p0)

In order to support detecting one row multi columns GPIO connection, we increase eight MUXs in KPD IP(each column increases one MUX), shown as Figure1.1-6. This makes each column Keyin signal is effective only when row scan Keyout signal is

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

effective, so that the new version KPD can support one row multi columns GPIO connection.

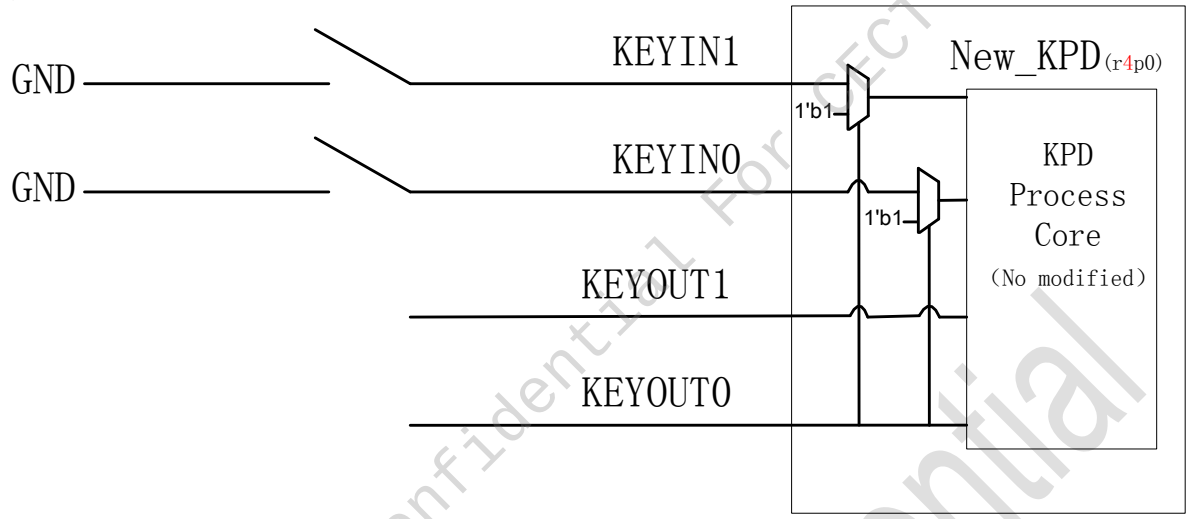


Figure 6.6-6 r4p0 KPD modification strategy

6.6.4 Funtion description

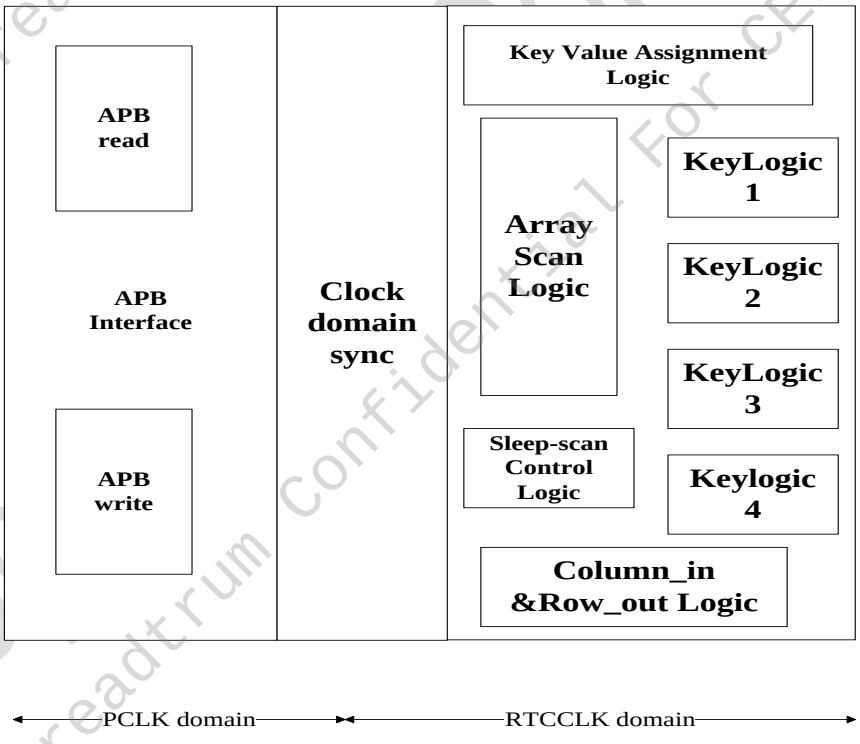


Figure 6.6-7 Keypad controller diagram

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.6.5 Control registers

6.6.5.1 Memory map

Offset Address	Name	Description
0x0000	KPD_CTRL	Keypad global control register
0x0004	KPD_INT_EN	Keypad INT enable register
0x0008	KPD_INT_RAW_STATUS	Keypad INT raw status register
0x000C	KPD_INT_MASK_STATUS	Keypad INT status register
0x0010	KPD_INT_CLR	Keypad INT clear register
0x0014		Reserved
0x0018	KPD_POLARITY	Keypad I/O polarity control register
0x001C	KPD_DEBOUNCE_CNT	Keypad de-bouncing time configuration register
0x0020	KPD_LONG_KEY_CNT	Keypad long-key time configuration register
0x0024	KPD_SLEEP_CNT	Keypad sleep wait time configuration register
0x0028	KPD_CLK_DIVIDE_CNT	Keypad scan clock division coefficient register
0x002C	KPD_ KEY_STATUS	Keypad key status register
0x0030	KPD_SLEEP_STATUS	Keypad sleep status register
0x0034	KPD_DEBUG_STATUS1	Keypad debug status register1
0x0038	KPD_DEBUG_STATUS2	Keypad debug status register2

6.6.5.2 Register description

6.6.5.2.1 KPD_CTRL

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0000			Keypad global control													KPD_CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reerved								KPD_ROW7_EN	KPD_ROW6_EN	KPD_ROW5_EN	KPD_ROW4_EN	KPD_ROW3_EN	KPD_ROW2_EN	KPD_ROW1_EN	KPD_ROW0_EN
Type	RO								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KPD_COL7_EN	KPD_COL6_EN	KPD_COL5_EN	KPD_COL4_EN	KPD_COL3_EN	KPD_COL2_EN	KPD_COL1_EN	KPD_COL0_EN	Reerved					KPD_LONG_KEY_EN	KPD_SLEEP_EN	KPD_EN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO					R/W	R/W	R/W
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:25]	RO	9'b0	Reserved
KPD_ROW7_EN	[23]	R/W	1'b0	Enable bit for row 7
KPD_ ROW6_EN	[22]	R/W	1'b0	Enable bit for row 6
KPD_ ROW5_EN	[21]	R/W	1'b0	Enable bit for row 5
KPD_ ROW4_EN	[20]	R/W	1'b0	Enable bit for row 4
KPD_ ROW3_EN	[19]	R/W	1'b0	Enable bit for row 3
KPD_ ROW2_EN	[18]	R/W	1'b0	Enable bit for row 2
KPD_ ROW1_EN	[17]	R/W	1'b1	Enable bit for row 1
KPD_ ROW0_EN	[16]	R/W	1'b1	Enable bit for row 0
KPD_COL7_EN	[15]	R/W	1'b0	Enable bit for column 7
KPD_COL6_EN	[14]	R/W	1'b0	Enable bit for column 6
KPD_COL5_EN	[13]	R/W	1'b0	Enable bit for column 5
KPD_COL4_EN	[12]	R/W	1'b0	Enable bit for column 4
KPD_COL3_EN	[11]	R/W	1'b0	Enable bit for column 3
KPD_COL2_EN	[10]	R/W	1'b0	Enable bit for column 2
KPD_COL1_EN	[9]	R/W	1'b1	Enable bit for column 1
KPD_COL0_EN	[8]	R/W	1'b1	Enable bit for column 0
	[7:3]	R	5'b0	Reserved
KPD_LONG_KEY_EN	[2]	R/W	1'b0	When set to 1, keypad can enter long key mode if a key is pressed for a long time
KPD_SLEEP_EN	[1]	R/W	1'b0	When set to 1, the keypad can enter sleep mode if there is no key press for a certain time. The scan will stop until there has a press pulse.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

KPD_EN	[0]	R/W	1'b0	Keypad global enable signal. Set to1 will make whole keypad work by generate the clk_en signal to do scan and other process. Notice: port signal kpd_eb directly generates RTCLK clock gating.

6.6.5.2.2 **KPD_INT_EN**

0x0004	Keypad interrupt enable												KPD_INT_EN			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					KPD4_LONG_KEY_INT_EN	KPD3_LONG_KEY_INT_EN	KPD2_LONG_KEY_INT_EN	KPD1_LONG_KEY_INT_EN	KPD4_RELEA_INT_EN	KPD3_RELEA_INT_EN	KPD2_RELEA_INT_EN	KPD1_RELEA_INT_EN	KPD4_PRESS_INT_EN	KPD3_PRESS_INT_EN	KPD2_PRESS_INT_EN	KPD1_PRESS_INT_EN
Type	RO				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:12]	RO	0	Reserved
KPD4_LONG_KEY_INT_EN	[11]	R/W	0	Keypad long-key interrupt enable for No.4
KPD3_LONG_KEY_INT_EN	[10]	R/W	0	Keypad long-key interrupt enable for No.3
KPD2_LONG_KEY_INT_EN	[9]	R/W	0	Keypad long-key interrupt enable for No.2
KPD1_LONG_KEY_INT_EN	[8]	R/W	0	Keypad long-key interrupt enable for No.1
KPD4_RELEA_INT_EN	[7]	R/W	0	Keypad release interrupt enable for No.4
KPD3_RELEA_INT_EN	[6]	R/W	0	Keypad release interrupt enable for No.3

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

KPD2_RELEA_INT_EN	[5]	R/W	0	Keypad release interrupt enable for No.2
KPD1_RELEA_INT_EN	[4]	R/W	0	Keypad release interrupt enable for No.1
KPD4_PRESS_INT_EN	[3]	R/W	0	Keypad press interrupt enable for No.4
KPD3_PRESS_INT_EN	[2]	R/W	0	Keypad press interrupt enable for No.3
KPD2_PRESS_INT_EN	[1]	R/W	0	Keypad press interrupt enable for No.2
KPD1_PRESS_INT_EN	[0]	R/W	0	Keypad press interrupt enable for No.1

6.6.5.2.3 **KPD_INT_RAW_STATUS**

0x0008	Keypad interrupt raw status												KPD_INT_RAW_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					KPD4_LONG_KEY_INT	KPD3_LONG_KEY_INT	KPD2_LONG_KEY_INT	KPD1_LONG_KEY_INT	KPD4_RELEA_INT	KPD3_RELEA_INT	KPD2_RELEA_INT	KPD1_RELEA_INT	KPD4_PRESS_IN	KPD3_PRESS_INT	KPD2_PRESS_INT	KPD1_PRESS_INT
Type	RO				RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

~~Field Name~~	Bit	R/W	Reset Value	Description
	[31:12]	RO	0	Reserved
KPD4_LONG_KEY_INT	[11]	RO	0	Keypad long-key interrupt for No.4
KPD3_LONG_KEY_INT	[10]	RO	0	Keypad long-key interrupt for No.3

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

KPD2_LONG_KEY_INT	[9]	RO	0	Keypad long-key interrupt for No.2
KPD1_LONG_KEY_INT	[8]	RO	0	Keypad long-key interrupt for No.1
KPD4_RELEA_INT	[7]	RO	0	Keypad release interrupt for No.4
KPD3_RELEA_INT	[6]	RO	0	Keypad release interrupt for No.3
KPD2_RELEA_INT	[5]	RO	0	Keypad release interrupt for No.2
KPD1_RELEA_INT_EN	[4]	RO	0	Keypad release interrupt for No.1
KPD4_PRESS_INT	[3]	RO	0	Keypad press interrupt for No.4
KPD3_PRESS_INT	[2]	RO	0	Keypad press interrupt for No.3
KPD2_PRESS_INT	[1]	RO	0	Keypad press interrupt for No.2
KPD1_PRESS_INT	[0]	RO	0	Keypad press interrupt for No.1

6.6.5.2.4 **KPD_INT_MASK_STATUS**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x000C			Keypad interrupt mask										KPD_INT_MASK_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					KPD4_MASK_LONG_KEY_INT	KPD3_MASK_LONG_KEY_INT	KPD2_MASK_LONG_KEY_INT	KPD1_MASK_LONG_KEY_INT	KPD4_MASK_RELEA_INT	KPD3_MASK_RELEA_INT	KPD2_MASK_RELEA_INT	KPD1_MASK_RELEA_INT	KPD4_MASK_PRESS_IN	KPD3_MASK_PRESS_INT	KPD2_MASK_PRESS_INT	KPD1_MASK_PRESS_INT
Type	RO				RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:12]	RO	0	Reserved
KPD4_MASK_LONG_KEY_INT	[11]	RO	0	No.4 keypad long-key interrupt masked by long-key interrupt enable.
KPD3_MASK_LONG_KEY_INT	[10]	RO	0	No.3 keypad long-key interrupt masked by long-key interrupt enable.
KPD2_MASK_LONG_KEY_INT	[9]	RO	0	No.2 keypad long-key interrupt masked by long-key interrupt enable.
KPD1_MASK_LONG_KEY_INT	[8]	RO	0	No.1 keypad long-key interrupt masked by long-key interrupt enable.
KPD4_MASK_RELEA_INT	[7]	RO	0	No.4 keypad release interrupt masked by release interrupt enable.
KPD3_MASK_RELEA_INT	[6]	RO	0	No.3 keypad release interrupt masked by release interrupt enable.
KPD2_MASK_RELEA_INT	[5]	RO	0	No.2 keypad release interrupt masked by release interrupt enable.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

KPD1_MASK_RELEA_INT_EN	[4]	RO	0	No.1 keypad release interrupt masked by release interrupt enable.
KPD4_MASK_PRESS_INT	[3]	RO	0	No.4 keypad press interrupt masked by press interrupt enable.
KPD3_MASK_PRESS_INT	[2]	RO	0	No.3 keypad press interrupt masked by press interrupt enable.
KPD2_MASK_PRESS_INT	[1]	RO	0	No.2 keypad press interrupt masked by press interrupt enable.
KPD1_MASK_PRESS_INT	[0]	RO	0	No.1 keypad press interrupt masked by press interrupt enable.

6.6.5.2.5 **KPD_INT_CLR**

0x0010	Keypad interrupt clear												KPD_INT_CLR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name					KPD4_LONG_KEY_INT_CLR	KPD3_LONG_KEY_INT_CLR	KPD2_LONG_KEY_INT_CLR	KPD1_LONG_KEY_INT_CLR	KPD4_RELEA_INT_CLR	KPD3_RELEA_INT_CLR	KPD2_RELEA_INT_CLR	KPD1_RELEA_INT_CLR	KPD4_PRESS_INT_CLR	KPD3_PRESS_INT_CLR	KPD2_PRESS_INT_CLR	KPD1_PRESS_INT_CLR
Type	RO				WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:12]	RO	0	Reserved
KPD4_LONG_KEY_INT_CLR	[11]	WO	0	Write 1 to this bit will clear the No.4 key long-key interrupt raw status.
KPD3_LONG_KEY_INT_CLR	[10]	WO	0	Write 1 to this bit will clear the No.3 key long-key interrupt raw

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				status.
KPD2_LONG_ KEY_INT_CLR	[9]	WO	0	Write 1 to this bit will clear the No.2 key long-key interrupt raw status.
KPD1_LONG_ KEY_INT_CLR	[8]	WO	0	Write 1 to this bit will clear the No.1 key long-key interrupt raw status.
KPD4_RELEA_ INT_CLR	[7]	WO	0	Write 1 to this bit will clear the No.4 key release interrupt raw status.
KPD3_RELEA_ INT_CLR	[6]	WO	0	Write 1 to this bit will clear the No.3 key release interrupt raw status.
KPD2_RELEA_ INT_CLR	[5]	WO	0	Write 1 to this bit will clear the No.2 key release interrupt raw status.
KPD1_RELEA_ INT_CLR	[4]	WO	0	Write 1 to this bit will clear the No.1 key release interrupt raw status.
KPD4_PRESS_ INT_CLR	[3]	WO	0	Write 1 to this bit will clear the No.4 key press interrupt raw status.
KPD3_PRESS_ INT_CLR	[2]	WO	0	Write 1 to this bit will clear the No.3 key press interrupt raw status.
KPD2_PRESS_ INT_CLR	[1]	WO	0	Write 1 to this bit will clear the No.2 key press interrupt raw status.
KPD1_PRESS_ INT_CLR	[0]	WO	0	Write 1 to this bit will clear the No.1 key press interrupt raw status.

6.6.5.2.6 **KPD_POLARITY**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0018			Kpd row column polarity												KPD_POLARITY	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KPD_COLUMN_POLARITY								KPD_ROW_POLARITY							
Type																
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	0	Reserved
KPD_COLUMN_ POLARITY	[15:8]	R/W	8'hFF	Column input xor with this value to generate the internal column input. This register is used to control the column input polarity.
KPD_ROW_ POLARITY	[7:0]	R/W	8'hFF	Internal row output xor with this value to generate row output. This register is used to control the row output polarity.

6.6.5.2.7 **KPD_DEBOUNCE_CNT**

0x001C			Kpd press and release de-bounce time control register										KPD_DEBOUNCE_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KPD_DEBOUNCE_CNT															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	0	Reserved
KPD_DEBOUNCE_CNT	[15:0]	R/W	16'h0080	Counter for de-bounce time It is the function of scan array size and clock divider

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				number. Default value: 165ms when clk_divider is 0 and 42 keys are enable(7*6 array) The calculation method is: y(ms)= (x +1) * array_size /(32.768/(clk_div_num +1))

6.6.5.2.8 **KPD_LONG_KEY_CNT**

0x0020			Kpd long key time control register										KPD_LONG_KEY_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KPD_LONG_KEY_CNT															
Type	R/W															
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:16]	RO	0	Reserved
KPD_LONG_KEY_CNT	[15:0]	R/W	16'h0400	Counter for long key time It is the function of scan array size and clock divider number. Default value: 1.34s when clk_divider is 0 and 42 keys are enable(7*6 array) The calculation method is: y(ms)= (x +1) * array_size /(32.768/(clk_div_num +1))

6.6.5.2.9 **KPD_SLEEP_CNT**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0024			Counter for enter sleep mode enable(from no key press)										KPD_SLEEP_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved									KPD_SLEEP_CNT						
Type	RO									R/W						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KPD_SLEEP_CNT															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:23]	RO	0	Reserved
KPD_SLEEP_CNT	[22:0]	R/W	23'h080000	Counter for enter sleep mode enable(from no key press) It is not the function of scan number and clock divider number. Default value:16.384s Y(ms)=(x+1)/32.768

6.6.5.2.10 **KPD_CLK_DIVIDE_CNT**

0x0028			Kpd scan clock divider coefficients configuration register										KPD_CLK_DIVIDE_CNT			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								KPD_CLK_DIVIDE_CNT							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	**Bit**	**R/W**	**Reset Value**	**Description**
	[31:8]	RO	0	Reserved
KPD_CLK_DIVIDE_CNT	[7:0]	R/W	0	Clk_divider[7:0], divide RTCLK (32.768 kHz) used for keypad. Can slow down keypad's work speed.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				The RTCLK will be divided (cnt + 1) times

6.6.5.2.11 **KPD_KEY_STATUS**

0x002C				Keypad keys status register.								KPD_KEY_STATUS			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	KPD4_KEY_STS	KPD4_ROW_CNT			Reserved	KPD4_COL_CNT			KPD3_KEY_STS	KPD3_ROW_CNT			Reserved	KPD3_COL_CNT		
Type	RO	RO			RO	RO			RO	RO			RO	RO		
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KPD2_KEY_STS	KPD2_ROW_CNT			Reserved	KPD2_COL_CNT			KPD1_KEY_STS	KPD1_ROW_CNT			KPD_FOUR_KEY_CROSS	KPD1_COL_CNT		
Type	RO	RO			RO	RO			RO	RO			RO	RO		
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1

Field Name	Bit	R/W	Reset Value	Description
KPD4_KEY_STS	[31]	RO	0	No.4 key is pressed status
KPD4_ROW_CNT	[30:28]	RO	3'b111	No.4 key row coordinate
	[27]	RO		Reserved
KPD4_COL_CNT	[26:24]	RO	3'b111	No.4 key column coordinate
KPD3_KEY_STS	[23]	RO	0	No.3 key is pressed status.
KPD3_ROW_CNT	[22:20]	RO	3'b111	No.3 key row coordinate
	[19]	RO	0	Reserved
KPD3_COL_CNT	[18:16]	RO	3'b111	No.3 key column coordinate
KPD2_KEY_STS	[15]	RO	0	No.2 key is pressed status.
KPD2_ROW_CNT	[14:12]	RO	3'b111	No.2 key row coordinate
	[11]	RO	0	Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

KPD2_COL_CNT	[10:8]	RO	3'b111	No.2 key column coordinate
KPD1_KEY_STS	[7]	RO	0	No.1 key is pressed status.
KPD1_ROW_CNT	[6:4]	RO	3'b111	No.1 key row coordinate
KPD_FOUR_KEY_CROSS	[3]	RO	0	Set to 1 indicates that when 4 keys are all pressed, these keys can be constructed into right-angled coordinate
KPD1_COL_CNT	[2:0]	RO	3'b111	No.1 key column coordinate

6.6.5.2.12 **KPD_SLEEP_STATUS**

0x0030			Keypad sleep status register										**KPD_SLEEP_STATUS**			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															KPD_SLEEP_STS
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

~~Field Name~~	**Bit**	**R/W**	**Reset Value**	**Description**
	[31:1]	RO	0	Reserved
KPD_SLEEP_STS	[0]	RO	0	Set to 1 shows keypad is in sleep state, 0 shows in common scan state

6.6.5.2.13 **KPD_DEBUG_STATUS1**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0034			Kpd debug status1 register										KPD_DEBUG_STATUS1			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved					KPD_ROW_CNT			Reserved	KPD_COL_CNT			Reserved			KPD_KEY_VALUE
Type	RO					RO			RO	RO			RO			RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
	[31:11]	RO	0	Reserved
KPD_ROW_CNT	[10:8]	RO	3'd0	Current scanning key's column coordinate
	[7]	RO	0	Reserved
KPD_COL_CNT	[6:4]	RO	3'd0	Current scanning key's row coordinate
	[3:1]	RO	0	Reserved
KPD_KEY_VALUE	[0]	RO	0	Keypad scanning flag, active high.

6.6.5.2.14 **KPD_DEBUG_STATUS2**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0038			Keypad debug status2 register										KPD_DEBUG_STATUS2			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name				KPD_KEY4_STATE								KPD_KEY3_STATE				
Type				RO								RO				
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				KPD_KEY2_STATE								KPD_KEY1_STATE				
Type				RO								RO				
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Field Name	Bit	R/W	Reset Value	Description
	[31:29]	RO	0	Reserved
KPD_KEY4_STATE	[28:24]	RO	5'b00001	Key_state_4 FSM's state The same as above
	[23:21]	RO	0	Reserved
KPD_KEY3_STATE	[20:16]	RO	5'b00001	Key_state_3 FSM's state The same as above
	[15:13]	RO	0	Reserved
KPD_KEY2_STATE	[12:8]	RO	5'b00001	Key_state_2 FSM's state The same as above
	[7:5]	RO	0	Reserved
KPD_KEY1_STATE	[4:0]	RO	5'b00001	Key_state_1 FSM's state 00001: release state 00010: press de-bounce state 00100: press state 01000: release de-bounce state 10000: release busy state

6.6.6 Application notes

Be careful, r4p0 KPD only supports detecting one row multi columns GPIO connection. Configure 0x0000(KPD_CTRL)register's bit23~17 to "0"(only row0 is enable). Multi rows multi columns GPIO is not supported in r4p0 KPD.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.6.7 Clock enable

There are two clock inputs for keypad controller: clk_rtc and APB PCLK. Before enable keypad controller to work these two clocks should be enabled. Please refer to the 0x402e_0000 register (GEN0 in APB global register)

[1]	RTC_KPD_EB	Clock rtc enable for keypad 0: Clock rtc will be off for keypad use. 1: Clock rtc will be on for keypad use.
[8]	KPD_EB	Keypad access enable 0: The peripheral clock (PCLK) of keypad controller will be off so its control registers cannot be accessed by MCU. 1: MCU can read or write keypad control registers.

6.6.1 KPD configuration

Please assure the right “keypad matrix size”, “row in/out polarity”, “key de-bounce time”, and “int enables”.

Also set the keypad controller works under the “sleep mode” by enable the “KPD_CTRL” register bit[1] can save power.

6.7 VBC Interface

6.7.1 Overview

The VBC module is designed as a digital interface, for software control and data handling with Audio Codec. Digital high-pass IIR filters, digital gain, side tone module and loop path are also implemented in VBC for special applications.

6.7.2 Features

- Both ARM and DSP can control Voice Band independently, so both APB bus and DSP Z bus are included in VBC module. They are able to access the same VB control registers
- Support two ADC channels: ADC0 and ADC1(one is reserved)
- Support two DAC channels: DAC0 and DAC1
- Two slave IIS/PCM serial interface for ADC/DAC data
- 2 320x16 SRAM are used as ADC ping-pong buffer, in which address 0~159 is for ADC0, and address 160~319 is for ADC1
- 2 320x16 SRAM are used as DAC0, DAC1 ping-pong buffer, in which address 0~159 is for DAC0, and address 160~319 is for DAC1
- Max buffer size of 4 channels supported is 160
- Support DMA access in ARM control mode
- DAC serial 6th-order IIR filter sections are designed for application such as high-pass filter and EQ
- DAC auto-level control(ALC) is supported
- DAC digital gain is supported
- DAC output limit is supported
- DAC notch tone and notch filter is supported
- DAC output can be selected as 16 bits or 24 bits
- ADC digital gain is supported
- Side tone is supported
- ADC input signal can be sent to DAC through side tone
- DAC output signal can be loop to ADC

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

- External IIS serial data can be selected as ADC input
- ADC interrupt to software if one ADC buffer is full
- DAC interrupt to software if one DAC buffer is empty

6.7.3 Signal Description

6.7.4 Function Description

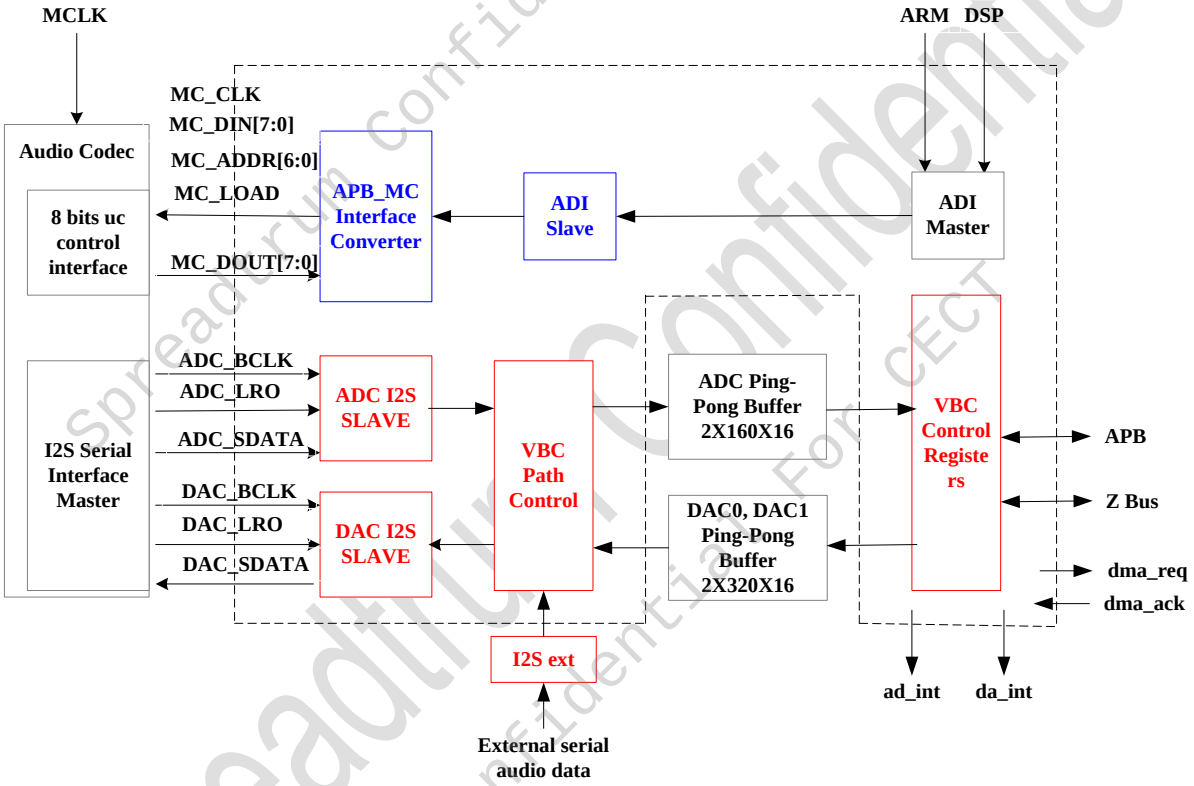


Figure 1 Voice Band Digital Interface

In the figure, the red parts belong to VBC module, and the blue part, which converts APB bus to uC bus.

Audio Codec digital interface includes clocks, serial audio interface and control interface. MCLK are generated from clock managing block in the top level of the chip. IIS/PCM serial interface transfer audio data between Codec and 160-word data ping-pong buffer. APB-MC interface converter, together with the ADI interface, work as a data bridge between APB/Z-bus and 8-bit uC interface.

Both ARM and DSP can control Voice Band independently. They are able to access the same VB control register, and control the data interrupt frequency. Through ARM and DSP register, four Voice paths ADC0,ADC1, DAC0, DAC1 can be shut down at different time, VB register access clock can

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

also be shut down. Interrupt will be sent to ARM/DSP after the data in the ping-pong buffer is full for ADC channel, or empty for DAC channel.

In ARM global register 0x8B00_0044, a 1-bit control register “arm_vb_acc” is used to select ARM or DSP control voice band. Default value is 0, allowing DSP controlling.

If ARM controlling is selected, a DMA hardware channel is provided for ADC and DAC respectively. Instead of interrupt, DMA request will be sent to DMA after the data in the ping-pong buffer is full for ADC channel, or empty for DAC channel.

6.7.4.1 Path Control and Function Module

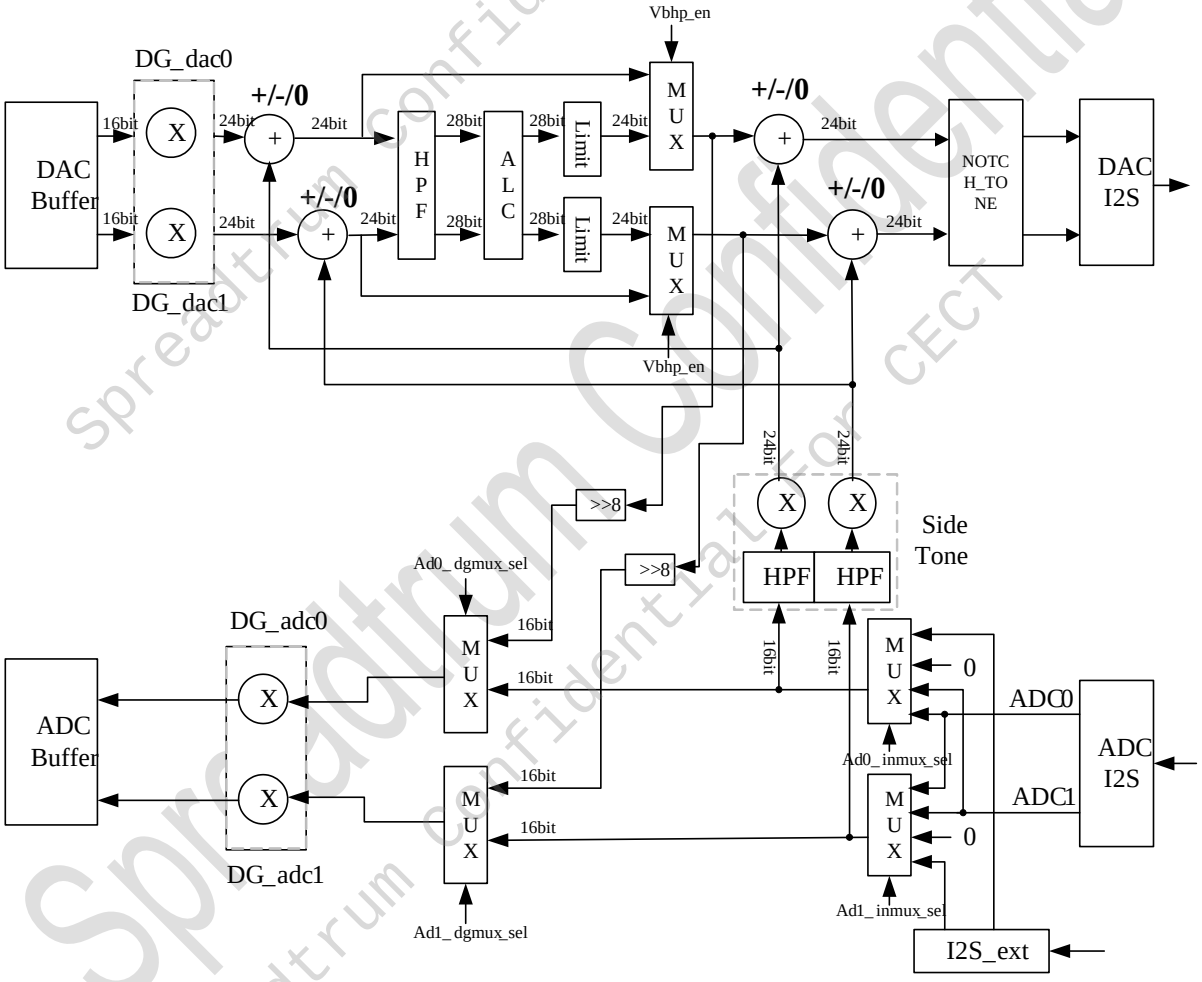


Figure 2 VBC Path Control

The above figure describes all VBC data flow paths. Except the direct DAC and ADC paths, several loop paths are added for different application.

- ADC loop to DAC

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Side tone module is implemented between ADC and DAC path, and through the side tone module, ADC data can loop to DAC, either to the input of DAC HPF, or output of DAC channel, added or subtracted by the DAC data.

- DAC loop to ADC

  The output of DAC can also loop to ADC path, after right shifting 8 bits and into the ADC digital gain module

The input data of each ADC channel can be selected between the two input channel, and also an external-chip input is also designed, which is useful when external audio signal is needed to be processed.

A digital gain is implemented for each DAC and ADC channel, and the gain coefficient DG[6:0] is parsed as follows..

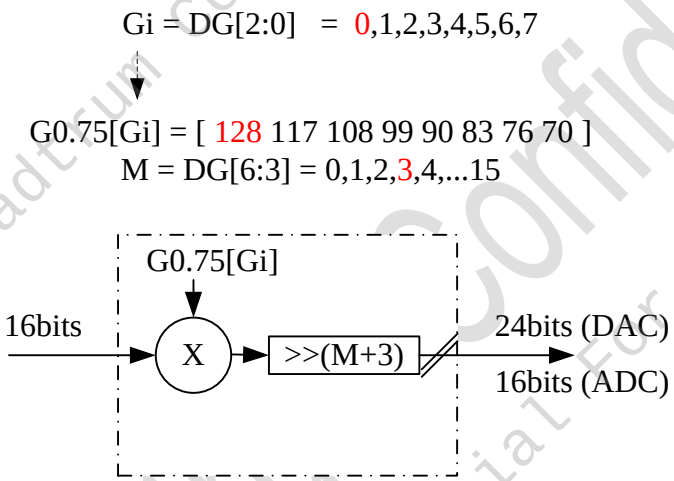


Figure 3 VBC Digital Gain

The 6th-order IIR high-pass filter is showed in the following figure. The filter is grouped into 3 parts. Each part is a 2nd-order IIR, and implemented in one module, named vbhp_s01.v, vbhp_s23.v and vbhp_45.v. In each 2nd-order IIR, DAC0 and DAC1 share the hardware, so after a valid-in signal, the DAC0 data are processed first, and then the DAC1 data are processed. After DAC1 data processing finishes, the valid-out signal is generated.

All the data during IIR processing are 34bits. The input 16bits data are left shifted 16bits and extended 2 bits to be 34bits, and the output data are 28bits for ALC module processing.

As for the ALC module, please refer to the document “SC850X VBC_ALC Design Specification”.

The 8bits hp_limit control register is for the output limit logic. The output signal also can be limited to an expected value, and the value is hp_limit[7:0]<<16+16’hFFFF.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Note 1: The input 16bit data of the 6-band IIR are left shifted 16bits and then extended to be 34bits, but the output 34bits data from the 6-band IIR are first right shifted 6 bits to be 28bits, pass through ALC, clipped to 24bits, and then right shifted 8 bits after the limiter to be 16bits.

Note2: Since the input data is 16bits left shifted, and the output data are 6+8=14bit right shifted, if the digital gain and the 6-band IIR are both configured to be bypass-state, the output of DAC is 4-times amplified.

Note3: If the 6-band IIR is enabled, the following configuration of the 43 HPCOEF registers is corresponding to the bypass-state of the 6-band IIR

HPCOEF0: ‘h1000 HPCOEF1: ‘h4000 HPCOEF2: ’h4000
HPCOEF3: ’h0000 HPCOEF4: ’h0000 HPCOEF5: ’h0000 HPCOEF6: ’h0000

HPCOEF7: ’h1000 HPCOEF8: ’h4000 HPCOEF9: ’h4000
HPCOEF10: ’h0000 HPCOEF11: ’h0000 HPCOEF12: ’h0000 HPCOEF13: ’h0000

HPCOEF14: ’h1000 HPCOEF15: ’h4000 HPCOEF16: ’h4000
HPCOEF17: ’h0000 HPCOEF18: ’h0000 HPCOEF19: ’h0000 HPCOEF20: ’h0000

HPCOEF21: ’h1000 HPCOEF22: ’h4000 HPCOEF23: ’h4000
HPCOEF24: ’h0000 HPCOEF25: ’h0000 HPCOEF26: ’h0000 HPCOEF27: ’h0000

HPCOEF28: ’h1000 HPCOEF29: ’h4000 HPCOEF30: ’h4000
HPCOEF31: ’h0000 HPCOEF32: ’h0000 HPCOEF33: ’h0000 HPCOEF34: ’h0000

HPCOEF35: ’h1000 HPCOEF36: ’h4000 HPCOEF37: ’h4000
HPCOEF38: ’h0000 HPCOEF39: ’h0000 HPCOEF40: ’h0000 HPCOEF41: ’h0000

HPCOEF42: ’h1000

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

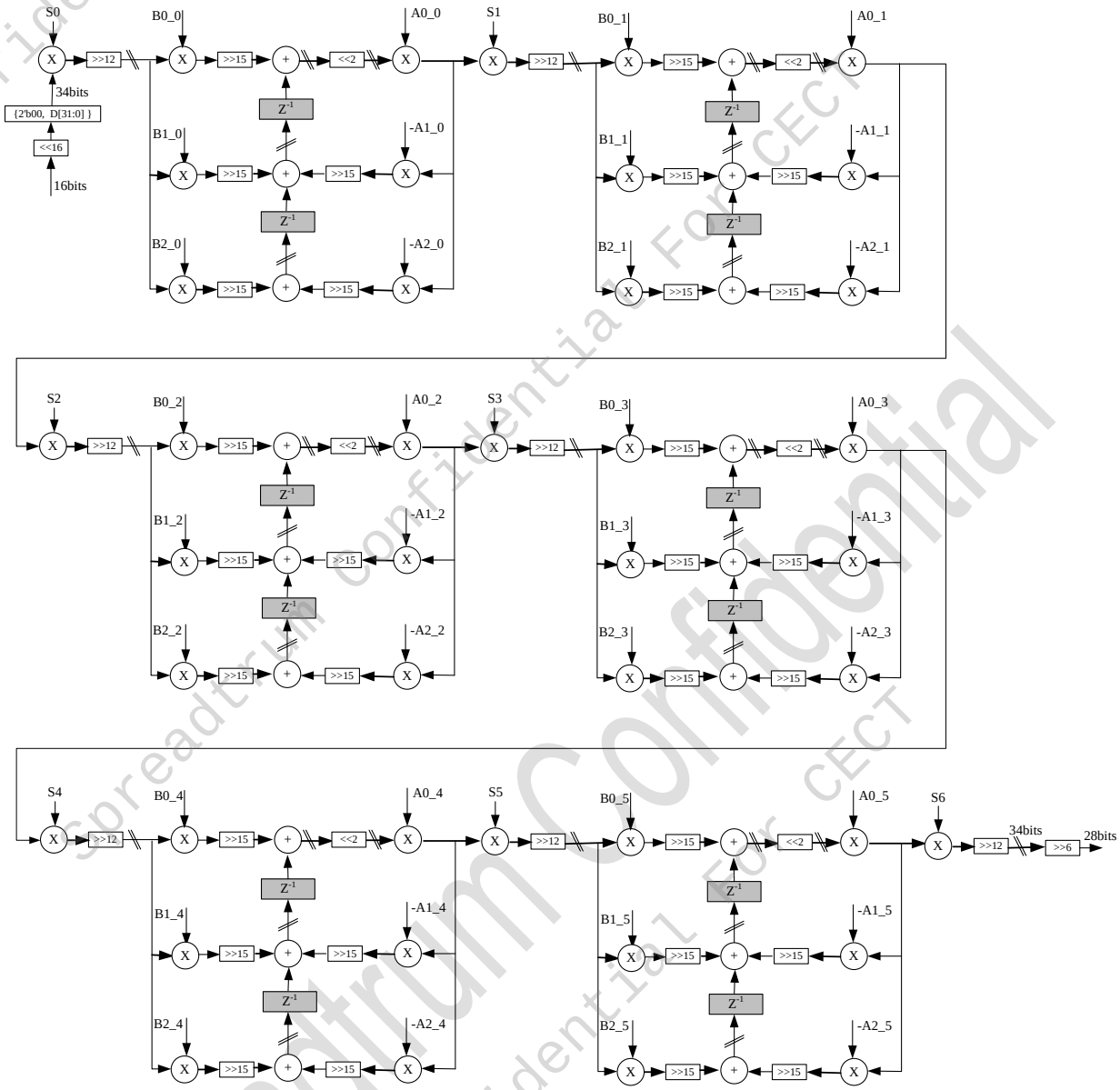


Figure 4 VBC 6-order DAC IIR filter

The side tone module includes a high-pass filter and a digital gain. The coefficient N[3:0] of the high-pass filter should be configured by software. The digital gain of side tone is the same with the DAC and ADC channel digital gain.

Notch Tone

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

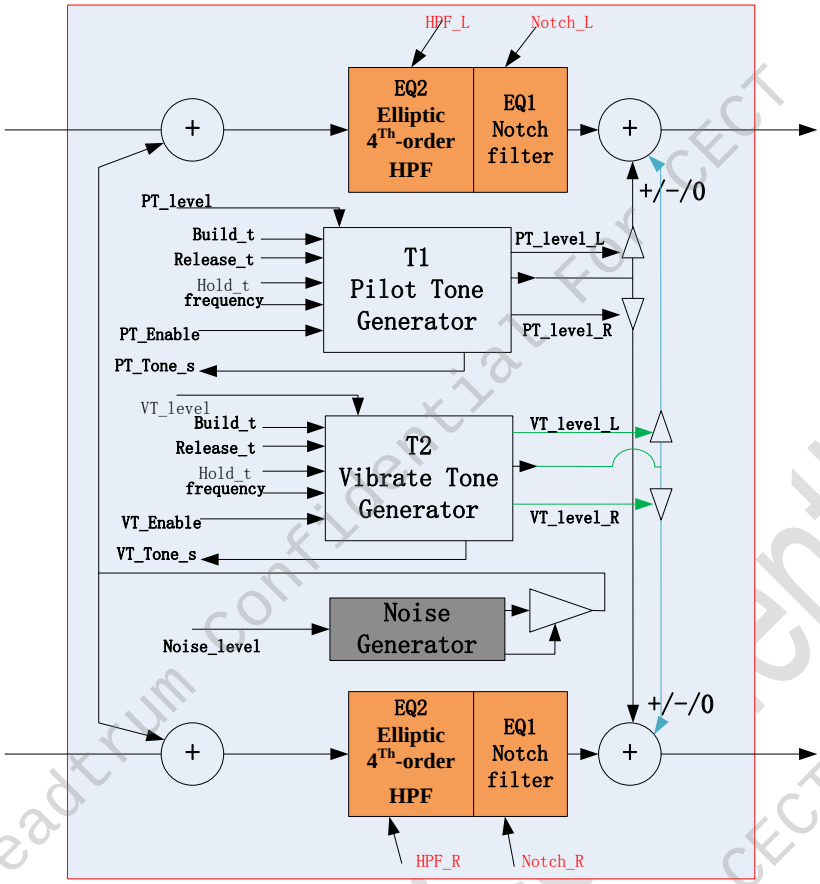
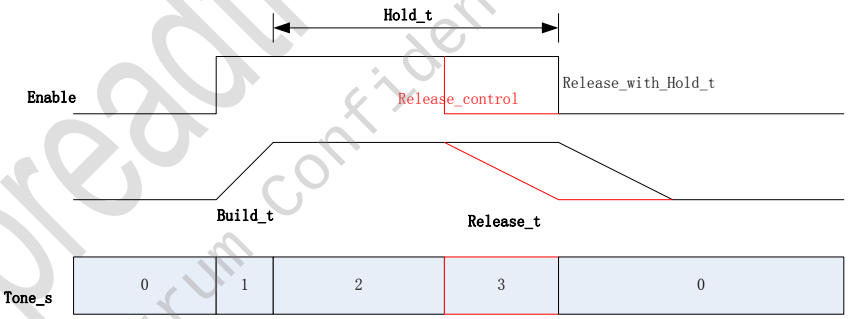


Figure 5 Notch Tone

Pilot tone : used for voice coil temperature measurement
Vibrate tone: used for 3-in-1 speaker.



This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

$$h(z) = (1 - 1>>(N+1)) \frac{1 - Z^{-1}}{1 - (1-1>>N) Z^{-1}}$$

Gi = DG[2:0] = 0,1,2,3,4,5,6,7

G0.75[Gi] = [128 117 108 99 90 83 76 70]

M = DG[6:3] = 0,1,2,3,4,...15

N = HPF[3:0] = 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15

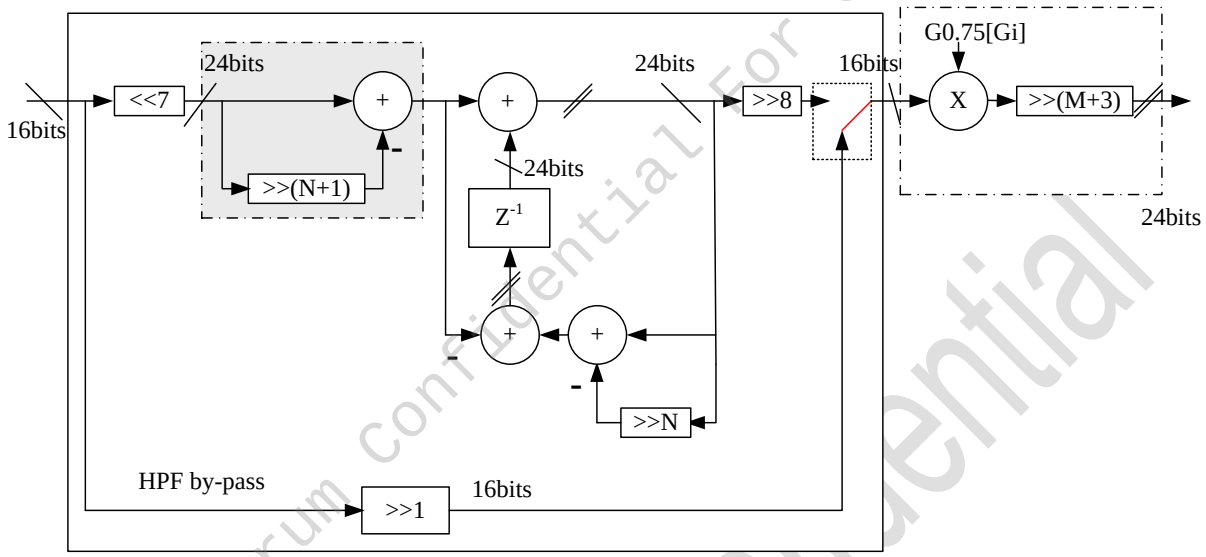


Figure 6 VBC Side Tone

6.7.4.2 Clock Domain

Clock for ADC/DAC I2S slave interface and data buffer can be shut down independently. Totally four clocks input to voice band interface:

- ADC_BCLK for ADC I2S Slave block, ADC digital gain and ADC data buffer. Control signal: vb_ad0on and vb_ad1on. If ARM controlling voice band, the two control bits are located in global control register 0x8B00_0044 bit[5:4]. If DSP controlling voice band, the two control bits are located in STC(system timing and controls) control register 0x0064_0294 bit[6:5].
- DAC_BCLK for DAC I2S Slave block, DAC digital gain, DAC high pass filter and DAC data buffer. Control signal: vb_da0on and vb_da1on. If ARM controlling voice band, the two control bits are located in global control register 0x8B00_044 bit[4:3]. If DSP controlling voice band, the two control bits are located in STC(system timing and controls) control register FORCE_PD bit[8:7] .
- APB clock or Z bus clock for ADC,DAC data buffer, selected by arm_vb_acc, global control register 0x8B00_0044 bit[7] .
- .CLK_12M for Audio Codec main clock.

6.7.4.3 I2S Slave Interface

The I2S slave interface receives serial ADC data under the control of ADC_BCLK and ADC_LRO, which are generated by audio codec I2S master interface, and sends serial DAC data under the control of DAC_BCLK and DAC_LRO, which are also generated by audio codec I2S master interface.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.7.4.4 Audio Codec control Interface

For the control registers located in audio codec, ARM or DSP access them through an 8-bit parallel µC interface. The 8-bit parallel µC interfaces are synchronized to MC_CLK. The other control signals, MC_ADDR, MC_LOAD and MC_DIN, are supposed to be generated on MC_CLK rising edge.

To read registers in the audio codec, ARM/DSP sends a read operation through the ADI interface, and the APB-MC bridge generates MC_ADDR, to the Audio Codec, then the Audio Codec outputs MC_DOUT data after a Tread delay. MC_DOUT can be sampled by the APB-MC bridge just after the Tread delay time (sure on the next rising edge of MC_CLK). MC_DOUT will be sent to ARM/DSP through the ADI interface after word length expanded to 16 bits.

To write registers in the audio codec, ARM/DSP sends a write operation through the ADI interface, and the APB-MC bridge generates MC_ADDR, MC_LOAD and the input data MC_DIN on the MC_CLK rising edge. MC_DIN is sampled by the Codec on the next MC_CLK rising edge.

The following two figures show the read and write timing of the 8-bit parallel µC interfaces.

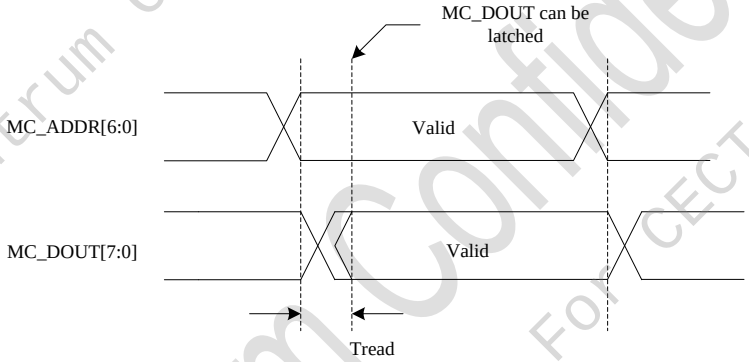


Figure 7 Parallel µC Interface Register Read Timing

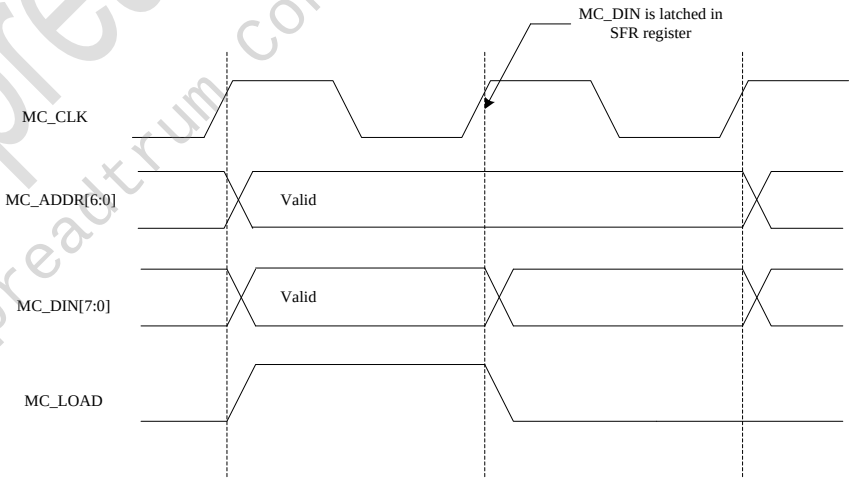


Figure 11-1

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Figure 8 Parallel µC Interface Register Write Timing

6.7.4.5 Digital Audio Data Buffer

Two 160x16 bit SRAM work as ping-pong buffers for each channel. The 4 160x16 SRAM for DAC0 and DAC1 ping-pong buffers are combined to 2 320 x 16 SRAM. The address 0 ~ 159 in each SRAM is DAC0 ping-pong buffer, and the address 160~319 in each SRAM is DAC1 ping-pong buffer. It's the same for ADC0 and ADC1 ping-pong buffer.

Received voice data are read out from ADC0 and ADC1 data buffer by software, and data for transmit are sent to DAC0, DAC1 data buffer also by software. Buffer size is programmable from 1 to 160 words. ADC interrupt(shared by ADC0 and ADC1) will be generated when ADC data buffer is full (written by hardware), and DAC interrupt (shared by DAC0 and DAC1) will be generated when DAC data buffer is empty (read by hardware). Voice interrupt frequency can be calculated from the buffer size. For example: when playing voice at 8 kHz sampling rate, buffer size is 160 words, the interval between two interrupt is: 125 us x 160 = 20 ms.

If DAC and ADC buffer sizes are the same, after voice band is enabled, the buffer size is not changed, two interrupts should be synchronized (within one voice sample duration), either one can be used as buffer full/empty interrupt.

Address counter for each path will be reset to zero after interrupt is generated or at VBENABLE register (0xBB06 bit 15) changing from low to high.

6.7.5 Control Registers

6.7.5.1 Memory map

DSP side base address: 0x0063_0000

DSP controls the Voice Band Controller (VBC) by default.

ARM side base address: 0x8200_3000/0x1063_0000

From the ARM side, please set 0x8B00_0044 bit[7] = 1'b1, to enable ARM access to VB

Note:

ARM can access Voice Band Codec module either through **APB space**, at base address 32'h8200_3000 or through **AHB space** (from ARM matrix to DSP matrix), at base address 32'h1063_0000.

For all Voice Band Codec registers through AHB space, please use half-word access; byte, word, or double-word accessing is forbidden. If access through APB space, only word access is permitted.

Table 7-6 Voice Band control registers

Offset Address	Name	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description
0x0000(0x0000)	VBDA0	Voice band DAC0 data buffer
0x0004(0x0002)	VBDA1	Voice band DAC1 data buffer
0x0008(0x0004)	VBAD0	Voice band ADC0 data buffer
0x000C(0x0006)	VBAD1	Voice band ADC1 data buffer
0x0010(0x0008)	VBBUFFSIZE	Voice band buffer size
0x0014(0x000A)	VBADBUFFDTA	Voice band AD buffer control
0x0018(0x000C)	VBDABUFFDTA	Voice band DA buffer control
0x001C(0x000E)	VBADCNT	Voice band AD buffer counter
0x0020(0x0010)	VBDACNT	Voice band DA buffer counter
0x0024(0x0012)	VBSHARECTRL	VBC register address share control
0x0028 ~0x0030 (0x0014~0x0018)		Reserved
0x0034 (0x001A)	VBINTTYPE	Voice band interrupt type
0x0038 (0x001C)	VBDATASWT	VBC data format of APB bus
0x003C(0x001E)	VBIISSEL	VBC iis control registers
0x0040(0x0020)	DAPATHCTL	DAC path control
0x0044(0x0022)	DADGCTL	DAC digital gain control
0x0048(0x0024)	DAHPCTL	DAC 6-band IIR high-pass filter control
0x004C(0x0026)	DAALCCTL0	DAC ALC coefficient: hold
0x0050(0x0028)	DAALCCTL1	DAC ALC coefficient: rise
0x0054(0x002A)	DAALCCTL2	DAC ALC coefficient: fall
0x0058(0x002C)	DAALCCTL3	DAC ALC coefficient: limit
0x005C(0x002E)	DAALCCTL4	DAC ALC coefficient: threshold
0x0060(0x0030)	DAALCCTL5	DAC ALC coefficient: ratio
0x0064(0x0032)	DAALCCTL6	DAC ALC coefficient: cg_var
0x0068(0x0034)	DAALCCTL7	DAC ALC coefficient: release_rate
0x006C(0x0036)	DAALCCTL8	DAC ALC coefficient: attack_rate
0x0070(0x0038)	DAALCCTL9	DAC ALC coefficient: release_rate_ex
0x0074(0x003A)	DAALCCTL10	DAC ALC coefficient: attack_rate_ex
0x0078(0x003C)	STCTL0	Side tone control of channel 0
0x007C(0x003E)	STCTL1	Side tone control of channel 1
0x0080(0x0040)	ADPATHCTL	ADC path control
0x0084(0x0042)	ADDGCTL	ADC digital gain control
0x0088(0x0044)	DANCHCTL	DAC notch tone control registers

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description
0x008C(0x0046)	DANCH_PTSINMW	high 16bit of DAC notch tone pt sin
0x0090(0x0048)	DANCH_PTSINLW	low 16bit of DAC notch tone pt sin
0x0094(0x004A)	DANCH_PTCOSMW	high 16bit of DAC notch tone pt cos
0x0098(0x004C)	DANCH_PTCOSLW	low 16bit of DAC notch tone pt cos
0x009C(0x004E)	DANCH_PTGL	DAC notch tone pt left channel gain
0x00A0(0x0050)	DANCH_PTGR	DAC notch tone pt right channel gain
0x00A4(0x0052)	DANCH_PTGD	DAC notch tone pt gain down
0x00A8(0x0054)	DANCH_PTGU	DAC notch tone pt gain up
0x00AC(0x0056)	DANCH_PTH	DAC notch tone pt hold t
0x00B0(0x0058)	DANCH_VTSINMW	high 16bit of DAC notch tone vt sin
0x00B4(0x005A)	DANCH_VTSINLW	low 16bit of DAC notch tone vt sin
0x00B8(0x005C)	DANCH_VTCOSMW	high 16bit of DAC notch tone vt cos
0x00BC(0x005E)	DANCH_VTCOSLW	low 16bit of DAC notch tone vt cos
0x00C0(0x0060)	DANCH_VTGL	DAC notch tone vt left channel gain
0x00C4(0x0062)	DANCH_VTGR	DAC notch tone vt right channel gain
0x00C8(0x0064)	DANCH_VTGD	DAC notch tone vt gain down
0x00CC(0x0066)	DANCH_VTGU	DAC notch tone vt gain up
0x00D0(0x0068)	DANCH_VTH	DAC notch tone vt hold t
0x00D4(0x006A)	DANCH_STS	DAC notch tone status
0x00D8 ~ 0x00FC (0x006C ~ 0x007E)		rf_vbc_addr_share: 0: Reserved 1: notch eq4 coef address
0x0100 (0x0080)	HPCOEF0	DAC 6 band IIR High-pass filter coefficients s0
0x0104 (0x0082)	HPCOEF1	DAC 6 band IIR High-pass filter coefficients b0_0
0x0108 (0x0084)	HPCOEF2	DAC 6 band IIR High-pass filter coefficients a0_0
0x010C (0x0086)	HPCOEF3	DAC 6 band IIR High-pass filter coefficients b1_0
0x0110 (0x0088)	HPCOEF4	DAC 6 band IIR High-pass filter coefficients a1_0
0x0114 (0x008A)	HPCOEF5	DAC 6 band IIR High-pass filter coefficients b2_0
0x0118 (0x008C)	HPCOEF6	DAC 6 band IIR High-pass filter coefficients a2_0
0x011C (0x008E)	HPCOEF7	DAC 6 band IIR High-pass filter coefficients s1

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description
0x0120 (0x0090)	HPCOEF8	DAC 6 band IIR High-pass filter coefficients b0_1
0x0124 (0x0092)	HPCOEF9	DAC 6 band IIR High-pass filter coefficients a0_1
0x0128 (0x0094)	HPCOEF10	DAC 6 band IIR High-pass filter coefficients b1_1
0x012C (0x0096)	HPCOEF11	DAC 6 band IIR High-pass filter coefficients a1_1
0x0130 (0x0098)	HPCOEF12	DAC 6 band IIR High-pass filter coefficients b2_1
0x0134 (0x009A)	HPCOEF13	DAC 6 band IIR High-pass filter coefficients a2_1
0x0138 (0x009C)	HPCOEF14	DAC 6 band IIR High-pass filter coefficients s2
0x013C (0x009E)	HPCOEF15	DAC 6 band IIR High-pass filter coefficients b0_2
0x0140 (0x00A0)	HPCOEF16	DAC 6 band IIR High-pass filter coefficients a0_2
0x0144 (0x00A2)	HPCOEF17	DAC 6 band IIR High-pass filter coefficients b1_2
0x0148 (0x00A4)	HPCOEF18	DAC 6 band IIR High-pass filter coefficients a1_2
0x014C (0x00A6)	HPCOEF19	DAC 6 band IIR High-pass filter coefficients b2_2
0x0150 (0x00A8)	HPCOEF20	DAC 6 band IIR High-pass filter coefficients a2_2
0x0154 (0x00AA)	HPCOEF21	DAC 6 band IIR High-pass filter coefficients s3
0x0158 (0x00AC)	HPCOEF22	DAC 6 band IIR High-pass filter coefficients b0_3
0x015C (0x00AE)	HPCOEF23	DAC 6 band IIR High-pass filter coefficients a0_3
0x0160 (0x00B0)	HPCOEF24	DAC 6 band IIR High-pass filter coefficients b1_3
0x0164 (0x00B2)	HPCOEF25	DAC 6 band IIR High-pass filter coefficients a1_3
0x0168 (0x00B4)	HPCOEF26	DAC 6 band IIR High-pass filter coefficients b2_3
0x016C (0x00B6)	HPCOEF27	DAC 6 band IIR High-pass filter coefficients a2_3
0x0170 (0x00B8)	HPCOEF28	DAC 6 band IIR High-pass filter coefficients s4
0x0174 (0x00BA)	HPCOEF29	DAC 6 band IIR High-pass filter

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description
		coefficients b0_4
0x0178 (0x00BC)	HPCOEF30	DAC 6 band IIR High-pass filter coefficients a0_4
0x017C (0x00BE)	HPCOEF31	DAC 6 band IIR High-pass filter coefficients b1_4
0x0180 (0x00C0)	HPCOEF32	DAC 6 band IIR High-pass filter coefficients a1_4
0x0184 (0x00C2)	HPCOEF33	DAC 6 band IIR High-pass filter coefficients b2_4
0x0188 (0x00C4)	HPCOEF34	DAC 6 band IIR High-pass filter coefficients a2_4
0x018C (0x00C6)	HPCOEF35	DAC 6 band IIR High-pass filter coefficients s5
0x0190 (0x00C8)	HPCOEF36	DAC 6 band IIR High-pass filter coefficients b0_5
0x0194 (0x00CA)	HPCOEF37	DAC 6 band IIR High-pass filter coefficients a0_5
0x0198 (0x00CC)	HPCOEF38	DAC 6 band IIR High-pass filter coefficients b1_5
0x019C(0x00CE)	HPCOEF39	DAC 6 band IIR High-pass filter coefficients a1_5
0x01A0 (0x00D0)	HPCOEF40	DAC 6 band IIR High-pass filter coefficients b2_5
0x01A4 (0x00D2)	HPCOEF41	DAC 6 band IIR High-pass filter coefficients a2_5
0x01A8 (0x00D4)	HPCOEF42	DAC 6 band IIR High-pass filter coefficients s6
0x0040(0x0020)	DAC_NCH_COEF0	Left channel low 16bit Elliptic4_HPF_s1_gain_L(shared)
0x0044(0x0022)	DAC_NCH_COEF0	Left channel high 8bit Elliptic4_HPF_s1_gain_L(shared)
0x0048(0x0024)	DAC_NCH_COEF1	Left channel low 16bit Elliptic4_HPF_s1_b_L(1) (shared)
0x004C(0x0026)	DAC_NCH_COEF1	Left channel high 8bit Elliptic4_HPF_s1_b_L(1) (shared)
0x0050(0x0028)	DAC_NCH_COEF2	Left channel low 16bit Elliptic4_HPF_s1_b_L (2) (shared)
0x0054(0x002A)	DAC_NCH_COEF2	Left channel high 8bit Elliptic4_HPF_s1_b_L (2) (shared)
0x0058(0x002C)	DAC_NCH_COEF3	Left channel low 16bit Elliptic4_HPF_s1_b_L (3) (shared)
0x005C(0x002E)	DAC_NCH_COEF3	Left channel high 8bit

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description
		Elliptic4_HPF_s1_b_L (3) (shared)
0x0060(0x0030)	DAC_NCH_COEF4	Left channel low 16bit Elliptic4_HPF_s1_b_L (2) (shared)
0x0064(0x0032)	DAC_NCH_COEF4	Left channel high 8bit Elliptic4_HPF_s1_b_L (2) (shared)
0x0068(0x0034)	DAC_NCH_COEF5	Left channel low 16bit Elliptic4_HPF_s1_b_L (3) (shared)
0x006C(0x0036)	DAC_NCH_COEF5	Left channel high 8bit Elliptic4_HPF_s1_b_L (3) (shared)
0x0070(0x0038)	DAC_NCH_COEF6	Right channel low 16bit Elliptic4_HPF_s1_gain_R(shared)
0x0074(0x003A)	DAC_NCH_COEF6	Right channel high 8bit Elliptic4_HPF_s1_gain_R(shared)
0x0078(0x003C)	DAC_NCH_COEF7	Right channel low 16bit Elliptic4_HPF_s1_b_R(1) (shared)
0x007C(0x003E)	DAC_NCH_COEF7	Right channel high 8bit Elliptic4_HPF_s1_b_R(1) (shared)
0x0080(0x0040)	DAC_NCH_COEF8	Right channel low 16bit Elliptic4_HPF_s1_b_R (2) (shared)
0x0084(0x0042)	DAC_NCH_COEF8	Right channel high 8bit Elliptic4_HPF_s1_b_R (2) (shared)
0x0088(0x0044)	DAC_NCH_COEF9	Right channel low 16bit Elliptic4_HPF_s1_b_R (3) (shared)
0x008C(0x0046)	DAC_NCH_COEF9	Right channel high 8bit Elliptic4_HPF_s1_b_R (3) (shared)
0x0090(0x0048)	DAC_NCH_COEF10	Right channel low 16bit Elliptic4_HPF_s1_b_R (2) (shared)
0x0094(0x004A)	DAC_NCH_COEF10	Right channel high 8bit Elliptic4_HPF_s1_b_R (2) (shared)
0x0098(0x004C)	DAC_NCH_COEF11	Right channel low 16bit Elliptic4_HPF_s1_b_R (3) (shared)
0x009C(0x004E)	DAC_NCH_COEF11	Right channel high 8bit Elliptic4_HPF_s1_b_R (3) (shared)
0x00A0(0x0050)	DAC_NCH_COEF12	Left channel low 16bit Elliptic4_HPF_s2_gain_L(shared)
0x00A4(0x0052)	DAC_NCH_COEF12	Left channel high 8bit Elliptic4_HPF_s2_gain_L(shared)
0x00A8(0x0054)	DAC_NCH_COEF13	Left channel low 16bit Elliptic4_HPF_s2_b_L(1) (shared)
0x00AC(0x0056)	DAC_NCH_COEF13	Left channel high 8bit Elliptic4_HPF_s2_b_L(1) (shared)
0x00B0(0x0058)	DAC_NCH_COEF14	Left channel low 16bit Elliptic4_HPF_s2_b_L (2) (shared)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description
0x00B4(0x005A)	DAC_NCH_COEF14	Left channel high 8bit Elliptic4_HPF_s2_b_L (2) (shared)
0x00B8(0x005C)	DAC_NCH_COEF15	Left channel low 16bit Elliptic4_HPF_s2_b_L (3) (shared)
0x00BC(0x005E)	DAC_NCH_COEF15	Left channel high 8bit Elliptic4_HPF_s2_b_L (3) (shared)
0x00C0(0x0060)	DAC_NCH_COEF16	Left channel low 16bit Elliptic4_HPF_s2_b_L (2) (shared)
0x00C4(0x0062)	DAC_NCH_COEF16	Left channel high 8bit Elliptic4_HPF_s2_b_L (2) (shared)
0x00C8(0x0064)	DAC_NCH_COEF17	Left channel low 16bit Elliptic4_HPF_s2_b_L (3) (shared)
0x00CC(0x0066)	DAC_NCH_COEF17	Left channel high 8bit Elliptic4_HPF_s2_b_L (3) (shared)
0x00D0(0x0068)	DAC_NCH_COEF18	Right channel low 16bit Elliptic4_HPF_s2_gain_R(shared)
0x00D4(0x006A)	DAC_NCH_COEF18	Right channel high 8bit Elliptic4_HPF_s2_gain_R(shared)
0x00D8(0x006C)	DAC_NCH_COEF19	Right channel low 16bit Elliptic4_HPF_s2_b_R(1) (shared)
0x00DC(0x006E)	DAC_NCH_COEF19	Right channel high 8bit Elliptic4_HPF_s2_b_R(1) (shared)
0x00E0(0x0070)	DAC_NCH_COEF20	Right channel low 16bit Elliptic4_HPF_s2_b_R (2) (shared)
0x00E4(0x0072)	DAC_NCH_COEF20	Right channel high 8bit Elliptic4_HPF_s2_b_R (2) (shared)
0x00E8(0x0074)	DAC_NCH_COEF21	Right channel low 16bit Elliptic4_HPF_s2_b_R (3) (shared)
0x00EC(0x0076)	DAC_NCH_COEF21	Right channel high 8bit Elliptic4_HPF_s2_b_R (3) (shared)
0x00F0(0x0078)	DAC_NCH_COEF22	Right channel low 16bit Elliptic4_HPF_s2_b_R (2) (shared)
0x00F4(0x007A)	DAC_NCH_COEF22	Right channel high 8bit Elliptic4_HPF_s2_b_R (2) (shared)
0x00F8(0x007C)	DAC_NCH_COEF23	Right channel low 16bit Elliptic4_HPF_s2_b_R (3) (shared)
0x00FC(0x007E)	DAC_NCH_COEF23	Right channel high 8bit Elliptic4_HPF_s2_b_R (3) (shared)
0x0100 (0x0080)	DAC_NCH_COEF24	Left channel low 16bit Elliptic4_HPF_s3_gain_L(shared)
0x0104 (0x0082)	DAC_NCH_COEF24	Left channel high 8bit Elliptic4_HPF_s3_gain_L(shared)
0x0108 (0x0084)	DAC_NCH_COEF25	Left channel low 16bit

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description
		Elliptic4_HPF_s3_b_L(1) (shared)
0x010C (0x0086)	DAC_NCH_COEF25	Left channel high 8bit Elliptic4_HPF_s3_b_L(1) (shared)
0x0110 (0x0088)	DAC_NCH_COEF26	Left channel low 16bit Elliptic4_HPF_s3_b_L (2) (shared)
0x0114 (0x008A)	DAC_NCH_COEF26	Left channel high 8bit Elliptic4_HPF_s3_b_L (2) (shared)
0x0118 (0x008C)	DAC_NCH_COEF27	Left channel low 16bit Elliptic4_HPF_s3_b_L (3) (shared)
0x011C (0x008E)	DAC_NCH_COEF27	Left channel high 8bit Elliptic4_HPF_s3_b_L (3) (shared)
0x0120 (0x0090)	DAC_NCH_COEF28	Left channel low 16bit Elliptic4_HPF_s3_b_L (2) (shared)
0x0124 (0x0092)	DAC_NCH_COEF28	Left channel high 8bit Elliptic4_HPF_s3_b_L (2) (shared)
0x0128 (0x0094)	DAC_NCH_COEF29	Left channel low 16bit Elliptic4_HPF_s3_b_L (3) (shared)
0x012C (0x0096)	DAC_NCH_COEF29	Left channel high 8bit Elliptic4_HPF_s3_b_L (3) (shared)
0x0130 (0x0098)	DAC_NCH_COEF30	Right channel low 16bit Elliptic4_HPF_s3_gain_R(shared)
0x0134 (0x009A)	DAC_NCH_COEF30	Right channel high 8bit Elliptic4_HPF_s3_gain_R(shared)
0x0138 (0x009C)	DAC_NCH_COEF31	Right channel low 16bit Elliptic4_HPF_s3_b_R(1) (shared)
0x013C (0x009E)	DAC_NCH_COEF31	Right channel high 8bit Elliptic4_HPF_s3_b_R(1) (shared)
0x0140 (0x00A0)	DAC_NCH_COEF32	Right channel low 16bit Elliptic4_HPF_s3_b_R (2) (shared)
0x0144 (0x00A2)	DAC_NCH_COEF32	Right channel high 8bit Elliptic4_HPF_s3_b_R (2) (shared)
0x0148 (0x00A4)	DAC_NCH_COEF33	Right channel low 16bit Elliptic4_HPF_s3_b_R (3) (shared)
0x014C (0x00A6)	DAC_NCH_COEF33	Right channel high 8bit Elliptic4_HPF_s3_b_R (3) (shared)
0x0150 (0x00A8)	DAC_NCH_COEF34	Right channel low 16bit Elliptic4_HPF_s3_b_R (2) (shared)
0x0154 (0x00AA)	DAC_NCH_COEF34	Right channel high 8bit Elliptic4_HPF_s3_b_R (2) (shared)
0x0158 (0x00AC)	DAC_NCH_COEF35	Right channel low 16bit Elliptic4_HPF_s3_b_R (3) (shared)
0x015C(0x00AE)	DAC_NCH_COEF35	Right channel high 8bit Elliptic4_HPF_s3_b_R (3) (shared)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.7.5.2 Register Descriptions

6.7.5.2.1 VBDA0

Description：

0x0000 (0x0000) Voice band DAC0 data (reset 0x0000_0000) VBDA0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBDA0															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBDA0	[15:0]	R/W	16'h0	Voice band DAC0 channel data from ARM/DSP. ARM/DSP writes every word of DAC0 data to this control register, and VBC moves the 16bits data to corresponding address of DAC0 buffer one by one

6.7.5.2.2 VBDA1

Description：

0x0004 (0x0002) Voice band DAC1 data (reset 0x0000_0000) VBDA1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBDA1															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

VBDA1	[15:0]	R/W	16'h0	Voice band DAC1 channel data from ARM/DSP. ARM/DSP writes every word of DAC1 data to this control register, and VBC moves the 16bits data to corresponding address of DAC1 buffer one by one

6.7.5.2.3 **VBAD0**

Description :

0x0008 (0x0004) Voice band ADC0 data (reset 0x0000_0000) VBAD0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VBAD0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBAD0	[15:0]	RO	16'h0	ADC0 channel data from Audio CODEC to ARM/DSP. VBC moves every word from ADC0 buffer one by one to this register, and ARM/DSP read the ADC0 data from this register

6.7.5.2.4 **VBAD1**

Description :

0x000C (0x0006) Voice band ADC1 data (reset 0x0000_0000) VBAD1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VBAD1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
VBAD1	[15:0]	RO	16'h0	Reserved for voice band another ADC channel input data. 0x0000 will be output if software reads this control register

6.7.5.2.5 **VBBUFFSIZE**

Description :

0x0010 (0x0008) Voice band buffer size(reset 0x0000_0000) VBBUFFSIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VBDABUFFSIZE								VBADBUFFSIZE							
Type	R/W								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBDABUFFSIZE	[15:8]	R/W	8'h0	Voice band DAC0 and DAC1 channel data buffer size, equals to real buffer size minus 1. max 159. 0~159 maps to real buffer size 1~160
VBADBUFFSIZE	[7:0]	R/W	8'h0	Voice band ADC channel data buffer size, equals to real buffer size minus 1. max 159. 0~159 maps to real buffer size 1~160

6.7.5.2.6 **VBADBUFFDTA**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0014 (0x000A) Voice band buffer and I2S control(reset 0x0000_1000) VBADBUFFDTA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBIIS_LRCK	VBPCM_MODE	VBIIS_DLOOP	VBISAD_DSEL	VBLSB_EB	VBISDACK_INV	VBISADCK_INV	ADBUFF_Δ								
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBIIS_LRCK	[15]	R/W	1'h0	Active level of 0/1 channel for both ADC and DAC channel "0": High for channel 0, low for channel 1 "1": Low for channel 0, high for channel 1
VBPCM_MODE	[14]	R/W	1'h0	I2S interface format for both ADC and DAC channel 0: I2S compatible format 1: PCM compatible format Note: I2S mode is recommended to be compatible with audio CODEC I2S master
VBIIS_DLOOP	[13]	R/W	1'h0	Loop IIS three Tx signals(DA) to IIS 3 Rx signals(AD). 0: normal mode 1: loop mode
VBISAD_DSEL	[12]	R/W	1'h1	Reserved, No use
VBLSB_EB	[11]	R/W	1'h0	I2S serial data transfer order for both ADC and DAC channel 0: MSB first 1: LSB first Note: must always be programmed to '0'
VBISDACK_INV	[10]	R/W	1'h0	VBC interface reverses DAC I2S BCLK from audio CODEC as its I2S BCLK to send serial data 0: normal mode 1: inverse mode
VBISADCK_INV	[9]	R/W	1'h0	VBC interface reverses ADC I2S BCLK from audio CODEC as its I2S BCLK to receive serial data 0: normal mode 1: inverse mode
ADBUFF_Δ	[8:0]	R/W	9'h0	Voice band ADC channel data buffer size change, 2's compliment number added to VBADBUFFSIZE, control AD data buffer change for next block.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.7.5.2.7 **VBDABUFFDTA**

Description :

0x0018 (0x000C) Voice band buffer and mode control(reset 0x0000_0000) VBDABUFFDTA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBENABLE	VBDA1DMA_EN	VBDA0DMA_EN	VBAD1DMA_EN	VBAD0DMA_EN	RAMSW_EN	RAMSW_NUMB	DABUFF_Δ								
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBENABLE	[15]	R/W	1'h0	Enable this bit then VBC interface starts working and software can receive voice band interrupt. Better set this bit after all other register bits are programmed. 0: disable 1: enable
VBDA1DMA_EN	[14]	R/W	1'h0	DMA write DAC1 data buffer enable, set this bit to enable DAC1 DMA mode 0: disable 1: enable
VBDA0DMA_EN	[13]	R/W	1'h0	DMA write DAC0 data buffer enable, set this bit to enable DAC0 DMA mode 0: disable 1: enable
VBAD1DMA_EN	[12]	R/W	1'h0	Reserved for DMA reading ADC1 data buffer enable 0: disable 1: enable Note: No use since there is only one ADC channel
VBAD0DMA_EN	[11]	R/W	1'h0	DMA read ADC0 data buffer enable, set this bit to enable ADC0 DMA mode 0: disable 1: enable
RAMSW_EN	[10]	R/W	1'h0	Software access ping-pong buffer enable when VBENABE bit low(before VBC interface start working), for both ADC and DAC channel(reading ADC data buffer and writing DAC0, DAC1 data

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				buffer) 0: disable 1: enable
RAMSW_NUMB	[9]	R/W	1'h0	Software accessing ping-pong buffer indication, for both ADC and DAC channel(reading ADC data buffer and writing DAC0, DAC1 data buffer) 0: software access data buffer 0 1: software access data buffer 1
DABUFF_Δ	[8:0]	R/W	9'h0	Voice band DAC channel data buffer size change, 2's compliment number added to VBDABUFFSIZE, control DA data buffer change for next block.

6.7.5.2.8 **VBADCNT**

Description :

0x001C (0x000E) Voice band ADC buffer counter(reset 0x0000_0000) VBADCNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBAD1CNT								VBAD0CNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBAD1CNT	[15:8]	RO	8'h0	Reserved for ADC1 data buffer address counter.
VBAD0CNT	[7:0]	RO	8'h0	ADC0 data buffer address counter (address of VBC interface writing input data from audio CODEC to ADC0 ping-pong buffer)

6.7.5.2.9 **VBDACNT**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0020 (0x0010) Voice band DAC buffer counter(reset 0x0000_0000) VBDACNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VBDA1CNT								VBDA0CNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
VBDA1CNT	[15:8]	RO	8'h0	DAC1 data buffer address counter (address of VBC interface reading output data from DAC1 ping-pong buffer to audio CODEC)
VBDA0CNT	[7:0]	RO	8'h0	DAC0 data buffer address counter (address of VBC interface reading output data from DAC0 ping-pong buffer to audio CODEC)

6.7.5.2.10 **VBSHARECTRL**

Description :

0x0024 (0x0012) VBC address shared control (reset 0x0000_0000) VBSHARECTRL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															rf_vbc_addr_share
Type	RO															R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:2]	RO	14'h0	Reserved
rf_vbc_addr_share	[0]	R/W	1'h0	VBC address share register: 1'b0: address 0x40(0x20)~0xD4(0x6A) used for registers configure, and 0x100(0x80) ~ 0x15C(0xAE) used for eq6 coef.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				1’b1: 0x40(0x20)~0x15C(0xAE) used for notch eq4 coef.

6.7.5.2.11 **VBINTTYPE**

Description :

0x0034 (0x001A) Voice Band interrupt type(reset 0x0000_0000) VBINTTYPE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved												Da_int_type		Ad_int_type	
Type	RO												R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:4]	RO	12’h0	Reserved
Da_int_type	[3:2]	R/W	1’h0	DAC interrupt type, 2’h0: wide pulse, and the width is 12 DAC IIS bit clock cycles 2’h1: one apb/z-bus clock cycle pulse 2’h2,2’h3: interrupt that need to clear by software
Ad_int_type	[1:0]	R/W	1’h0	ADC interrupt type, 2’h0: wide pulse, and the width is 12 DAC IIS bit clock cycles 2’h1: one apb/z-bus clock cycle pulse 2’h2,2’h3: interrupt that need to clear by software

6.7.5.2.12 **VBDATASWT**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0038 (0x001C) data format control(reset 0x0000_0000) VBDATASWT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved														rf_vb_buf_out_swt	rf_vb_buf_in_swt
Type	RO														R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:2]	RO	14'h0	Reserved
rf_vb_buf_out_swt	[1]	R/W	1'h0	ADC data format control 1'b0: low 16bit of APB data is valid 1'b1: high 16bit of APB data is valid
rf_vb_buf_in_swt	[0]	R/W	1'h0	DAC data format control 1'b0: low 16bit of APB data is valid 1'b1: high 16bit of APB data is valid

6.7.5.2.13 **VBIISSEL**

Description :

0x003C (0x001E) VBC iis select(reset 0x0000_0000) VBIISSEL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved						rf_vb_iis_da_lr_md	rf_vb_iis_ad_lr_md	rf_vb_iis_da_pcm_md	rf_vb_iis_ad_pcm_md	rf_vb_iis_da_lsb	rf_vb_iis_ad_lsb	rf_vb_iis_da_sel		rf_vb_iis_ad_sel	
Type	RO						R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[15:10]	RO	6'h0	Reserved
rf_vb_iis_da_lr_md	[9]	R/W	1'h0	Active level of 0/1 channel for DAC "0": High for channel 0, low for channel 1 "1": Low for channel 0, high for channel 1
rf_vb_iis_ad_lr_md	[8]	R/W	1'h0	Active level of 0/1 channel for ADC "0": High for channel 0, low for channel 1 "1": Low for channel 0, high for channel 1
rf_vb_iis_da_pcm_md	[7]	R/W	1'h0	DAC I2S interface format 0: I2S compatible format 1: PCM compatible format Note: I2S mode is recommended to be compatible with audio CODEC I2S master
rf_vb_iis_ad_pcm_md	[6]	R/W	1'h0	ADC I2S interface format 0: I2S compatible format 1: PCM compatible format Note: I2S mode is recommended to be compatible with audio CODEC I2S master
rf_vb_iis_da_lsb	[5]	R/W	1'h0	DAC IIS bit endianess select: 1'b0: msb 1'b1: lsb
rf_vb_iis_ad_lsb	[4]	R/W	1'h0	ADC IIS bit endianess select: 1'b0: msb 1'b1: lsb
rf_vb_iis_da_sel	[3:2]	R/W	2'h0	DAC IIS select, 2'h0: iis0 2'h1: iis1 2'h2: iis2 2'h3: iis3
rf_vb_iis_ad_sel	[1:0]	R/W	2'h0	ADC IIS select, 2'h0: iis0 2'h1: iis1 2'h2: iis2 2'h3: iis3

6.7.5.2.14 **DAPATHCTL**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0040 (0x0020) Voice band DAC path control (reset 0x0000_0000) DAPATHCTL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								Da1_addst_sel		Da0_addst_sel		Da1_addfm_sel		Da0_addfm_sel	
Type	RO								R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:8]	RO	8'h0	Reserved
Da1_addst_sel	[7:6]	R/W	2'h0	2'b00: DAC1 data from ALC directly sent to DAC I2S 2'b01: DAC1 data from ALC added with side tone data, then sent to DAC I2S 2'b10: DAC1 data from ALC subtracted from side tone output data, then sent to DAC I2S 60.96cmb11: Reserved
Da0_addst_sel	[5:4]	R/W	2'h0	2'b00: DAC0 data from ALC directly sent to DAC I2S 2'b01: DAC0 data from ALC added with side tone data, then sent to DAC I2S 2'b10: DAC0 data from ALC subtracted from side tone output data, then sent to DAC I2S 2'b11: Reserved
Da1_addfm_sel	[3:2]	R/W	2'h0	2'b00: DAC1 buffer data directly sent to DAC HPF 2'b01: DAC1 buffer data added with side tone data, then sent to DAC HPF 2'b10: DAC1 buffer data subtracted from side tone output data, then sent to DAC HPF 2'b11: Reserved
Da0_addfm_sel	[1:0]	R/W	2'h0	2'b00: DAC0 buffer data directly sent to DAC HPF 2'b01: DAC0 buffer data added with side tone output data, then sent to DAC HPF 2'b10: DAC0 buffer data subtracted from side tone output data, then sent to DAC HPF 2'b11: Reserved

6.7.5.2.15 **DADGCTL**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0044 (0x0022) Voice band DAC digital gain control (reset 0x0000_1818) DADGCTL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Dadg_en_1	Dadg_dg_1							Dadg_en_0	Dadg_dg_0						
Type	R/W	R/W							R/W	R/W						
Reset	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dadg_en_1	[15]	R/W	1'h0	DAC1 digital gain enable
Dadg_dg_1	[14:8]	R/W	7'h18	DAC1 digital gain coefficient 7'h18: 0db larger than 7'h18 : amplify the input signal, and the step is 0.75db smaller than 7'h18 : reduce the input signal, and the step is 0.75db
Dadg_en_0	[7]	R/W	1'h0	DAC0 digital gain enable
Dadg_dg_0	[6:0]	R/W	7'h18	DAC0 digital gain coefficient 7'h18: 0db larger than 7'h18 : amplify the input signal, and the step is 0.75db smaller than 7'h18 : reduce the input signal, and the step is 0.75db

6.7.5.2.16 **DAHPCTL**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0048 (0x0024) **Voice band DAC High pass filter control (reset 0x0000_007F)** **DAHPCTL**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved				Dac_alc_en	Vbhp_en	Hp_reg_clr	Wid_sel	R_limit							
Type	RO				R/W	R/W	R/W	R/W	R/W							
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[15:12]	RO	4'h0	Reserved
Dac_alc_en	[11]	R/W	1'h0	1'b0: ALC bypass 1'b1: ALC enable(if vbhp_en=1)
Vbhp_en	[10]	R/W	1'h0	1'b0: 6-band IIR and ALC bypass 1'b1: 6-band IIR and ALC enable
Hp_reg_clr	[9]	R/W	1'h0	Clear all HPF IIR registers, Please write 1'b1 and later write 1'b0 to finish the register clear process
Wid_sel	[8]	R/W	1'h0	1'b0: 16bits output 1'b1: 24bits output
R_limit	[7:0]	R/W	8'h7F	DAC output signal limit, the actual limit value on the 24bits output signal is: r_limit[7:0]<<16+16'hFFFF

6.7.5.2.17 **DAALCCTL0**

Description :

0x004C (0x0026) **Voice band DAC ALC coefficient : hold (reset 0x0000_0000)** **DAALCCTL0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_hld															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
Dac_alc_hld	[15:0]	R/W	16'h0	DAC ALC coefficient: hold

6.7.5.2.18 **DAALCCTL1**

Description :

0x0050 (0x0028) Voice band DAC ALC coefficient : rise (reset 0x0000_0000) DAALCCTL1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_rise															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_rise	[15:0]	R/W	16'h0	DAC ALC coefficient: rise

6.7.5.2.19 **DAALCCTL2**

Description :

0x0054 (0x002A) Voice band DAC ALC coefficient : fall (reset 0x0000_0000) DAALCCTL2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_fall															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
Dac_alc_fall	[15:0]	R/W	16'h0	DAC ALC coefficient: fall

6.7.5.2.20 **DAALCCTL3**

Description :

0x0058 (0x002C) Voice band DAC ALC coefficient : limit (reset 0x0000_0000) DAALCCTL3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_lmt															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_lmt	[15:0]	R/W	16'h0	DAC ALC coefficient: limit

6.7.5.2.21 **DAALCCTL4**

Description :

0x005C (0x002E) Voice band DAC ALC coefficient : threshold (reset 0x0000_0000) DAALCCTL4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_thd															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
Dac_alc_thd	[15:0]	R/W	16'h0	DAC ALC coefficient: threshold

6.7.5.2.22 **DAALCCTL5**

Description :

0x0060 (0x0030) Voice band DAC ALC coefficient : ratio (reset 0x0000_0000) DAALCCTL5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_ratio															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_ratio	[15:0]	R/W	16'h0	DAC ALC coefficient: ratio

6.7.5.2.23 **DAALCCTL6**

Description :

0x0064 (0x0032) Voice band DAC ALC coefficient : cg_var (reset 0x0000_0000) DAALCCTL6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_cg_var															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
Dac_alc_cg_var	[15:0]	R/W	16'h0	DAC ALC coefficient: cg_var

6.7.5.2.24 **DAALCCTL7**

Description :

0x0068 (0x0034) **Voice band DAC ALC coefficient : release rate(reset 0x0000_0000)** **DAALCCTL7**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_rls_rate															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_rls_rate	[15:0]	R/W	16'h0	DAC ALC coefficient: release rate

6.7.5.2.25 **DAALCCTL8**

Description :

0x006C (0x0036) **Voice band DAC ALC coefficient : attack rate(reset 0x0000_0000)** **DAALCCTL8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_atk_rate															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Dac_alc_atk_rate	[15:0]	R/W	16'h0	DAC ALC coefficient: attack rate

6.7.5.2.26 **DAALCCTL9**

Description :

0x0070 (0x0038) **Voice band DAC ALC coefficient : release_rate_ex(reset 0x0000_0000)** **DAALCCTL9**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_rls_rate_ex															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Dac_alc_rls_rate_ex	[15:0]	R/W	16'h0	DAC ALC coefficient: release_rate_ex

6.7.5.2.27 **DAALCCTL10**

Description :

0x0074 (0x003A) **Voice band DAC ALC coefficient : attack_rate_ex(reset 0x0000_0000)** **DAALCCTL10**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Dac_alc_atk_rate_ex															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
Dac_alc_atk_rate_ex	[15:0]	R/W	16'h0	DAC ALC coefficient: attack_rate_ex

6.7.5.2.28 **STCTL0**

Description：

0x0078 (0x003C) **Voice band Side Tone control of channel0(reset 0x0000_0183)** **STCTL0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved			Vbst_en_0	Vbst_hpf_en_0	Vbst_hpf_dg_0							Vbst_hpf_n_0			
Type	RO			R/W	R/W	R/W							R/W			
Reset	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1

Field Name	Bit	Type	Reset Value	Description
	[15:13]	RO	3'h0	Reserved
Vbst_en_0	[12]	R/W	1'h0	0: Side tone of channel 0 disable 1: Side tone of channel 0 enable
Vbst_hpf_en_0	[11]	R/W	1'h0	0: Side tone HPF of channel 0 disable 1: Side tone HPF of channel 0 enable
Vbst_hpf_dg_0	[10:4]	R/W	7'h18	Side tone gain coefficient of channel 0 7'h18: 0db larger than 7'h18 : amplify the input signal, and the step is 0.75db smaller than 7'h18 : reduce the input signal, and the step is 0.75db
Vbst_hpf_n_0	[3:0]	R/W	4'h3	Side tone high-pass filter coefficient of channel0. If the high-pass filter is enabled, 4'h3 is the typical configuration, and 4'h0 is reserved.

6.7.5.2.29 **STCTL1**

Description：

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x007C (0x003E) **Voice band Side Tone control of channel1(reset 0x0000_0183)** **STCTL1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved			Vbst_en_1	Vbst_hpf_en_1	Vbst_hpf_dg_1							Vbst_hpf_n_1			
Type	RO			R/W	R/W	R/W							R/W			
Reset	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1

Field Name	Bit	Type	Reset Value	Description
	[15:13]	RO	3'h0	Reserved
Vbst_en_1	[12]	R/W	1'h0	0: Side tone of channel 1 disable 1: Side tone of channel 1 enable
Vbst_hpf_en_1	[11]	R/W	1'h0	0: Side tone HPF of channel 1 disable 1: Side tone HPF of channel 1 enable
Vbst_hpf_dg_1	[10:4]	R/W	7'h18	Side tone gain coefficient of channel 1 7'h18: 0db larger than 7'h18 : amplify the input signal, and the step is 0.75db smaller than 7'h18 : reduce the input signal, and the step is 0.75db
Vbst_hpf_n_1	[3:0]	R/W	4'h3	Side tone high-pass filter coefficient of channel1. If the high-pass filter is enabled, 4'h3 is the typical configuration, and 4'h0 is reserved.

6.7.5.2.30 **ADPATHCTL**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0080 (0x0040) Voice band ADC path control(reset 0x0000_0000) ADPATHCTL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved										Ad1_dgmux_sel	Ad0_dgmux_sel	Ad1_inmux_sel		Ad0_inmux_sel	
Type	RO										R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:6]	RO	3'h0	Reserved
Ad1_dgmux_sel	[5]	R/W	1'h0	1'b0: ADC data as input of ADC1 DG 1'b1: DAC ALC output data as input of ADC1 DG
Ad0_dgmux_sel	[4]	R/W	1'h0	1'b0: ADC data as input of ADC0 DG 1'b1: DAC ALC output data as input of ADC0 DG
Ad1_inmux_sel	[3:2]	R/W	2'h0	2'b00: I2S ADC1 data as input of ADC1 path 2'b01: I2S ADC0 data as input of ADC1 path 2'b10: Digital TV I2S ADC1 data as input of ADC1 path 2'b11: All zero as input of ADC1 path
Ad0_inmux_sel	[1:0]	R/W	2'h0	2'b00: I2S ADC0 data as input of ADC0 path 2'b01: I2S ADC1 data as input of ADC1 path 2'b10: Digital TV I2S ADC0 data as input of ADC0 path 2'b11: All zero as input of ADC0 path

6.7.5.2.31 **ADDGCTL**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0084 (0x0042) Voice band ADC digital gain control (reset 0x0000_1818) ADDGCTL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Addg_en_1	Addg_dg_1							Addg_en_0	Addg_dg_0						
Type	R/W	R/W							R/W	R/W						
Reset	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0

Field Name	Bit	Type	Reset Value	Description
Addg_en_1	[15]	R/W	1'h0	ADC1 digital gain enable
Addg_dg_1	[14:8]	R/W	7'h18	ADC1 digital gain coefficient 7'h18: 0db larger than 7'h18 : amplify the input signal, and the step is 0.75db smaller than 7'h18 : reduce the input signal, and the step is 0.75db
Addg_en_0	[7]	R/W	1'h0	ADC0 digital gain enable
Addg_dg_0	[6:0]	R/W	7'h18	ADC0 digital gain coefficient 7'h18: 0db larger than 7'h18 : amplify the input signal, and the step is 0.75db smaller than 7'h18 : reduce the input signal, and the step is 0.75db

6.7.5.2.32 **DANCHCTL**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0088 (0x0044) VBC DAC notch tone control (reset 0x0000_0000) DANCHCTL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved			notch_tone_clr	notch_eq4_clr	vt_tone_on	vt_tone_en	pt_tone_on	pt_tone_en	notch_eq4_group2_r_en	notch_eq4_group2_l_en	notch_eq4_group1_r_en	notch_eq4_group1_l_en	notch_eq4_group0_r_en	notch_eq4_group0_l_en	notch_eq4_en
Type	RO			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:13]	RO	3'h0	Reserved
notch_tone_clr	[12]	RW	1'h0	DAC notch tone clear
notch_eq4_clr	[11]	RW	1'h0	DAC notch eq4 clear
vt_tone_on	[10]	RW	1'h0	DAC notch tone vt tone on
vt_tone_en	[9]	RW	1'h0	DAC notch tone vt tone enable
pt_tone_on	[8]	RW	1'h0	DAC notch tone pt tone on
pt_tone_en	[7]	RW	1'h0	DAC notch tone pt tone enable
notch_eq4_group2_r_en	[6]	RW	1'h0	DAC notch eq4 band2 right channel enable
notch_eq4_group2_l_en	[5]	RW	1'h0	DAC notch eq4 band2 left channel enable
notch_eq4_group1_r_en	[4]	RW	1'h0	DAC notch eq4 band1 right channel enable
notch_eq4_group1_l_en	[3]	RW	1'h0	DAC notch eq4 band1 left channel enable
notch_eq4_group0_r_en	[2]	RW	1'h0	DAC notch eq4 band0 right channel enable
notch_eq4_group0_l_en	[1]	RW	1'h0	DAC notch eq4 band0 left channel enable
notch_eq4_en	[0]	RW	1'h0	DAC notch eq4 enable

6.7.5.2.33 **DANCH_PTSINMW**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x008C (0x0046) DAC notch pt tone sin high 16bit(reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pt_tone_sin_mw															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
pt_tone_sin_mw	[15:0]	R/W	16'h0	DAC notch pt tone sin high 16bit

6.7.5.2.34 **DANCH_PTSINLW**

Description :

0x0090 (0x0048) DAC notch pt tone sin low 16bit (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pt_tone_sin_lw															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
pt_tone_sin_lw	[15:0]	R/W	16'h0	DAC notch pt tone sin low 16bit

6.7.5.2.35 **DANCH_PTCOSMW**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0094 (0x004A) DAC notch pt tone cos high 16bit (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	pt_tone_cos_mw															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
pt_tone_cos_mw	[15:0]	R/W	16'h0	DAC notch pt tone cos high 16bit

6.7.5.2.36 **DANCH_PTCOSLW**

Description :

0x0098 (0x004C) DAC notch pt tone cos low 16bit (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	pt_tone_cos_lw															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
pt_tone_cos_lw	[15:0]	R/W	16'h0	DAC notch pt tone cos low 16bit

6.7.5.2.37 **DANCH_PTGL**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x009C (0x004E) DAC notch pt tone left channel gain (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pt_tone_gain_l															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
pt_tone_gain_l	[15:0]	R/W	16'h0	DAC notch pt tone left channel gain

6.7.5.2.38 **DANCH_PTGR**

Description :

0x00A0 (0x0050) DAC notch pt tone right channel gain (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pt_tone_gain_r															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
pt_tone_gain_r	[15:0]	R/W	16'h0	DAC notch pt tone right channel gain

6.7.5.2.39 **DANCH_PTGD**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x00A4(0x0052) DAC notch pt tone gain down (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pt_tone_gain_down															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
pt_tone_gain_down	[15:0]	R/W	16'h0	DAC notch pt tone gain down

6.7.5.2.40 **DANCH_PTGU**

Description :

0x00A8 (0x0054) DAC notch pt tone gain up (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pt_tone_gain_up															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
pt_tone_gain_up	[15:0]	R/W	16'h0	DAC notch pt tone gain up

6.7.5.2.41 **DANCH_PTH**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x00AC (0x0056) DAC notch pt tone hold t (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	pt_tone_hold_t															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
pt_tone_hold_t	[15:0]	R/W	16'h0	DAC notch pt tone hold t

6.7.5.2.42 **DANCH_VTSINMW**

Description :

0x00B0(0x0058) DAC notch vt tone sin high 16bit(reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	vt_tone_sin_mw															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
vt_tone_sin_mw	[15:0]	R/W	16'h0	DAC notch vt tone sin high 16bit

6.7.5.2.43 **DANCH_VTSINLW**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x00B4 (0x005A) DAC notch vt tone sin low 16bit (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vt_tone_sin_lw															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
vt_tone_sin_lw	[15:0]	R/W	16'h0	DAC notch vt tone sin low 16bit

6.7.5.2.44 **DANCH_VTCOSMW**

Description :

0x00B8 (0x005C) DAC notch vt tone cos high 16bit (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vt_tone_cos_mw															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
vt_tone_cos_mw	[15:0]	R/W	16'h0	DAC notch vt tone cos high 16bit

6.7.5.2.45 **DANCH_VTCOSLW**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x00BC(0x005E) DAC notch vt tone cos low 16bit (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vt_tone_cos_lw															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
vt_tone_cos_lw	[15:0]	R/W	16'h0	DAC notch vt tone cos low 16bit

6.7.5.2.46 **DANCH_VTGL**

Description :

0x00C0 (0x0060) DAC notch vt tone left channel gain (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vt_tone_gain_l															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
vt_tone_gain_l	[15:0]	R/W	16'h0	DAC notch vt tone left channel gain

6.7.5.2.47 **DANCH_VTGR**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x00C4 (0x0062) DAC notch vt tone right channel gain (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vt_tone_gain_r															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
vt_tone_gain_r	[15:0]	R/W	16'h0	DAC notch vt tone right channel gain

6.7.5.2.48 **DANCH_VTGD**

Description :

0x00C8 (0x0064) DAC notch vt tone gain down (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vt_tone_gain_down															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
vt_tone_gain_down	[15:0]	R/W	16'h0	DAC notch vt tone gain down

6.7.5.2.49 **DANCH_VTGU**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x00CC (0x0066) DAC notch vt tone gain up (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	vt_tone_gain_up															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
vt_tone_gain_up	[15:0]	R/W	16'h0	DAC notch vt tone gain up

6.7.5.2.50 **DANCH_VTH**

Description :

0x00D0 (0x068) DAC notch vt tone hold t (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	vt_tone_hold_t															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
vt_tone_hold_t	[15:0]	R/W	16'h0	DAC notch vt tone hold t

6.7.5.2.51 **DANCH_STS**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x00D4 (0x06A) DAC notch tone status (reset 0x0000_0000)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved										vt_tone_on_hardware	pt_tone_on_hardware	nch_vt_sts		nch_pt_sts	
Type	RO										RO	RO	RO		RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[15:6	RO	10'h0	Reserved
vt_tone_on_hardware	[5]	RO	1'h0	vt tone hardware on status
pt_tone_on_hardware	[4]	RO	1'h0	pt tone hardware on status
nch_vt_sts	[3:2]	RO	2'h0	notch tone vt fsm state status
nch_pt_sts	[1:0]	RO	2'h0	notch tone pt fsm state status

6.7.5.2.52 **HPCOEF0**

Description :

0x00100 (0x0080) DAC 6 band IIR HPF coefficient s0(reset 0x0000_0000) HPCOEF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef0															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef0	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient s0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.7.5.2.53 **HPCOEF1**

Description :

0x00104 (0x0082) DAC 6 band IIR HPF coefficient b0_0(reset 0x0000_0000) HPCOEF1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef1															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef1	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b0_0

6.7.5.2.54 **HPCOEF2**

Description :

0x00108 (0x0084) DAC 6 band IIR HPF coefficient a0_0(reset 0x0000_0000) HPCOEF2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef2															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
Hpcoef2	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a0_0

6.7.5.2.55 **HPCOEF3**

Description：

0x0010C (0x0086) DAC 6 band IIR HPF coefficient b1_0(reset 0x0000_0000) HPCOEF3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef3															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef3	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b1_0

6.7.5.2.56 **HPCOEF4**

Description：

0x00110 (0x0088) DAC 6 band IIR HPF coefficient a1_0(reset 0x0000_0000) HPCOEF4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef4															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
Hpcoef4	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a1_0

6.7.5.2.57 **HPCOEF5**

Description：

0x00114 (0x008A) DAC 6 band IIR HPF coefficient b2_0(reset 0x0000_0000) HPCOEF5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef5															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef5	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b2_0

6.7.5.2.58 **HPCOEF6**

Description：

0x00118 (0x008C) DAC 6 band IIR HPF coefficient a2_0(reset 0x0000_0000) HPCOEF6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef6															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
Hpcoef6	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a2_0

6.7.5.2.59 **HPCOEF7**

Description：

0x0011C (0x008E) DAC 6 band IIR HPF coefficient s1(reset 0x0000_0000) HPCOEF7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef7															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef7	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient s1

6.7.5.2.60 **HPCOEF8**

Description：

0x00120 (0x0090) DAC 6 band IIR HPF coefficient b0_1(reset 0x0000_0000) HPCOEF8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef8															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
Hpcoef8	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b0_1

6.7.5.2.61 **HPCOEF9**

Description :

0x00124 (0x0092) DAC 6 band IIR HPF coefficient a0_1(reset 0x0000_0000) HPCOEF9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef9															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef9	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a0_1

6.7.5.2.62 **HPCOEF10**

Description :

0x00128 (0x0094) DAC 6 band IIR HPF coefficient b1_1(reset 0x0000_0000) HPCOEF10

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef10															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
Hpcoef10	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b1_1

6.7.5.2.63 **HPCOEF11**

Description：

0x0012C (0x0096) DAC 6 band IIR HPF coefficient a1_1(reset 0x0000_0000) HPCOEF11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef11															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef11	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a1_1

6.7.5.2.64 **HPCOEF12**

Description：

0x00130 (0x0098) DAC 6 band IIR HPF coefficient b2_1(reset 0x0000_0000) HPCOEF12

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef12															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
Hpcoef12	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b2_1

6.7.5.2.65 **HPCOEF13**

Description：

0x00134 (0x009A) DAC 6 band IIR HPF coefficient a2_1(reset 0x0000_0000) HPCOEF13

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef13															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef13	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a2_1

6.7.5.2.66 **HPCOEF14**

Description：

0x00138 (0x009C) DAC 6 band IIR HPF coefficient s2(reset 0x0000_0000) HPCOEF14

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef14															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
Hpcoef14	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient s2

6.7.5.2.67 **HPCOEF15**

Description：

0x0013C (0x009E) DAC 6 band IIR HPF coefficient b0_2(reset 0x0000_0000) HPCOEF15

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef15															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef15	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b0_2

6.7.5.2.68 **HPCOEF16**

Description：

0x00140 (0x00A0) DAC 6 band IIR HPF coefficient a0_2(reset 0x0000_0000) HPCOEF16

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef16															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Hpcoef16	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a0_2

6.7.5.2.69 **HPCOEF17**

Description：

0x00144 (0x00A2) DAC 6 band IIR HPF coefficient b1_2(reset 0x0000_0000) HPCOEF17

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef17															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef17	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b1_2

6.7.5.2.70 **HPCOEF18**

Description：

0x00148 (0x00A4) DAC 6 band IIR HPF coefficient a1_2(reset 0x0000_0000) HPCOEF18

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef18															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef18	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a1_2

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.7.5.2.71 **HPCOEF19**

Description :

0x0014C (0x00A6) DAC 6 band IIR HPF coefficient b2_2(reset 0x0000_0000) HPCOEF19

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef19															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef19	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b2_2

6.7.5.2.72 **HPCOEF20**

Description :

0x00150 (0x00A8) DAC 6 band IIR HPF coefficient a2_2(reset 0x0000_0000) HPCOEF20

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef20															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef20	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a2_2

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.7.5.2.73 **HPCOEF21**

Description：

0x00154 (0x00AA) DAC 6 band IIR HPF coefficient s3(reset 0x0000_0000) HPCOEF21

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef21															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef21	[15:0]	R/W	16’h0	DAC 6 band IIR HPF coefficient s3

6.7.5.2.74 **HPCOEF22**

Description：

0x00158 (0x00AC) DAC 6 band IIR HPF coefficient b0_3(reset 0x0000_0000) HPCOEF22

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef22															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef22	[15:0]	R/W	16’h0	DAC 6 band IIR HPF coefficient b0_3

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.7.5.2.75 **HPCOEF23**

Description：

0x0015C (0x00AE) DAC 6 band IIR HPF coefficient a0_3(reset 0x0000_0000) HPCOEF23

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Hpcoef23															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef23	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a0_3

6.7.5.2.76 **HPCOEF24**

Description：

0x00160 (0x00B0) DAC 6 band IIR HPF coefficient b1_3(reset 0x0000_0000) HPCOEF24

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Hpcoef24															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef24	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b1_3

6.7.5.2.77 **HPCOEF25**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Description :

0x00164 (0x00B2) DAC 6 band IIR HPF coefficient a1_3(reset 0x0000_0000) HPCOEF25

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef25															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef25	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a1_3

6.7.5.2.78 **HPCOEF26**

Description :

0x00168 (0x00B4) DAC 6 band IIR HPF coefficient b2_3(reset 0x0000_0000) HPCOEF26

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef26															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef26	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b2_3

6.7.5.2.79 **HPCOEF27**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0016C (0x00B6) DAC 6 band IIR HPF coefficient a2_3(reset 0x0000_0000) HPCOEF27

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef27															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef27	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a2_3

6.7.5.2.80 **HPCOEF28**

Description :

0x00170 (0x00B8) DAC 6 band IIR HPF coefficient s4(reset 0x0000_0000) HPCOEF28

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef28															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef28	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient s4

6.7.5.2.81 **HPCOEF29**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x00174 (0x00BA) DAC 6 band IIR HPF coefficient b0_4(reset 0x0000_0000) HPCOEF29

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef29															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef29	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b0_4

6.7.5.2.82 **HPCOEF30**

Description :

0x00178 (0x00BC) DAC 6 band IIR HPF coefficient a0_4(reset 0x0000_0000) HPCOEF30

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef30															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef30	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a0_4

6.7.5.2.83 **HPCOEF31**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0017C (0x00BE) DAC 6 band IIR HPF coefficient b1_4(reset 0x0000_0000) HPCOEF31

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef31															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef31	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b1_4

6.7.5.2.84 **HPCOEF32**

Description :

0x00180 (0x00C0) DAC 6 band IIR HPF coefficient a1_4(reset 0x0000_0000) HPCOEF32

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef32															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef32	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a1_4

6.7.5.2.85 **HPCOEF33**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x00184 (0x00C2) DAC 6 band IIR HPF coefficient b2_4(reset 0x0000_0000) HPCOEF33

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef33															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef33	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b2_4

6.7.5.2.86 **HPCOEF34**

Description :

0x00188 (0x00C4) DAC 6 band IIR HPF coefficient a2_4(reset 0x0000_0000) HPCOEF34

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef34															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef34	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a2_4

6.7.5.2.87 **HPCOEF35**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0018C (0x00C6) DAC 6 band IIR HPF coefficient s5(reset 0x0000_0000) HPCOEF35

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef35															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef35	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient s5

6.7.5.2.88 **HPCOEF36**

Description :

0x00190 (0x00C8) DAC 6 band IIR HPF coefficient b0_5(reset 0x0000_0000) HPCOEF36

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef36															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef36	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b0_5

6.7.5.2.89 **HPCOEF37**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x00194 (0x00CA) DAC 6 band IIR HPF coefficient a0_5(reset 0x0000_0000) HPCOEF37

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef37															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef37	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a0_5

6.7.5.2.90 **HPCOEF38**

Description :

0x00198 (0x00CC) DAC 6 band IIR HPF coefficient b1_5(reset 0x0000_0000) HPCOEF38

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef38															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef38	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b1_5

6.7.5.2.91 **HPCOEF39**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0019C (0x00CE) DAC 6 band IIR HPF coefficient a1_5(reset 0x0000_0000) HPCOEF39

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef39															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef39	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a1_5

6.7.5.2.92 **HPCOEF40**

Description :

0x001A0 (0x00D0) DAC 6 band IIR HPF coefficient b2_5(reset 0x0000_0000) HPCOEF40

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef40															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef40	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient b2_5

6.7.5.2.93 **HPCOEF41**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x001A4 (0x00D2) DAC 6 band IIR HPF coefficient a2_5(reset 0x0000_0000) HPCOEF41

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef41															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef41	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient a2_5

6.7.5.2.94 **HPCOEF42**

Description :

0x001A8 (0x00D4) DAC 6 band IIR HPF coefficient s6(reset 0x0000_0000) HPCOEF42

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Hpcoef42															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
Hpcoef42	[15:0]	R/W	16'h0	DAC 6 band IIR HPF coefficient s6

6.7.5.2.95 **VBFIFOLVL**

Description :

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x01C0 (0x00E0) VBC inner FIFO level control(reset 0x0000_4444) VBFIFOLVL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved	vb_fifo_ae_lvl_w			Reserve	vb_fifo_ae_lvl_r			Reserve	vb_fifo_af_lvl_w			Reserve	vb_fifo_af_lvl_r		
Type	RO	R/W			RO	R/W			RO	R/W			RO	R/W		
Reset	0	3'h4			0	3'h4			0	3'h4			0	3'h4		

Field Name	Bit	Type	Reset Value	Description
	[15]	RO	6'h0	Reserved
vb_fifo_ae_lvl_w	[14:12]	R/W	3'h4	VBC FIFO almost empty threshold
	[11]	RO	1'h0	Reserved
vb_fifo_ae_lvl_r	[10:8]	R/W	3'h4	VBC FIFO almost empty threshold
	[7]	RO	1'h0	Reserved
vb_fifo_af_lvl_w	[6:4]	R/W	3'h4	VBC FIFO almost full threshold
	[3]	RO	1'h0	Reserved
vb_fifo_af_lvl_r	[2:0]	R/W	3'h4	VBC FIFO almost full threshold

6.7.5.2.96 **VBIRQEN**

Description :

0x01C4 (0x00E2) VBC interrupt enable(reset 0x0000_0000) VBIRQEN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved														da_irq_en	ad_irq_en
Type	RO														R/W	R/W
Reset	0														0	0

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[15:2]	RO	14'h0	Reserved
da_irq_en	[1]	R/W	1'h0	DAC interrupt enable
ad_irq_en	[0]	R/W	1'h0	ADC interrupt enable

6.7.5.2.97 **VBIRQCLR**

Description :

0x01C8 (0x00E4) VBC interrupt interrupt(reset 0x0000_0000) VBIRQCLR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved														da_irq_clr	ad_irq_clr
Type	RO														WC	WC
Reset	0														0	0

Field Name	Bit	Type	Reset Value	Description
	[15:2]	RO	14'h0	Reserved
da_irq_clr	[1]	WC	1'h0	DAC interrupt clear
ad_irq_clr	[0]	WC	1'h0	ADC interrupt clear

6.8 GPIO

6.8.1 Overview

The GPIO module provides more then 100 GPIO pins of MCU. However, many of the pins are multiplexed with other functions and system design trade-off must be exercised on selecting them. All the GPIO pins can be programmed to be either input or output. When in input mode, they can be programmed to trigger interrupt to the MCU.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.8.2 Features

- positive edge detect and interrupt generate
- negative edge detect and interrupt generate
- both edges detect and interrupt generate
- high level detect and interrupt generate
- low level detect and interrupt generate
- interrupt mask
- interrupt clear
- input data sample or mask
- output data or mask
- level interrupt generate at system power down
- level detect conditions changeable
- different interrupts happen
- edge detect conditions changeable

6.8.3 Funtion description

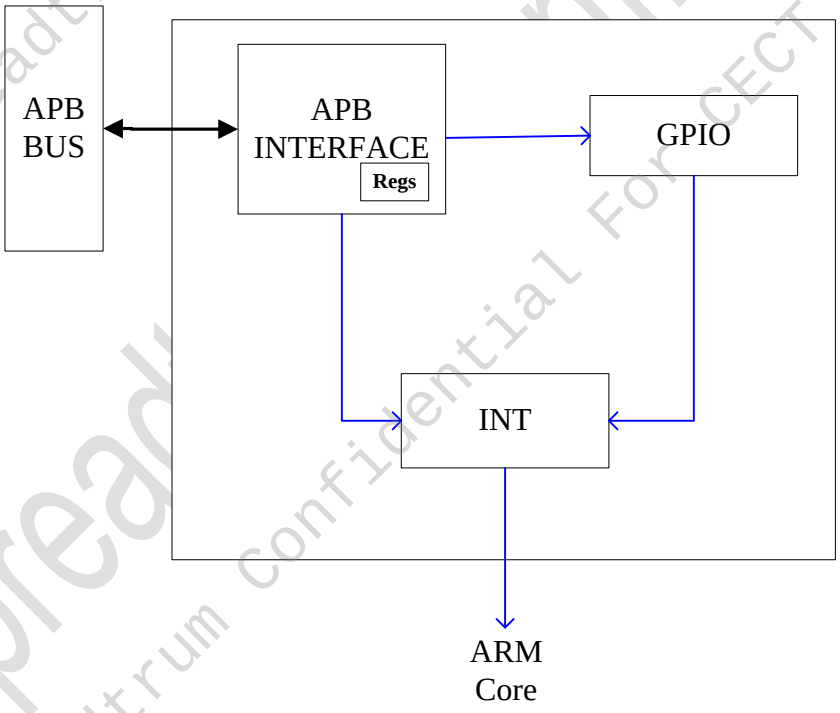


Figure 6-8 GPIO block diagram

As the above diagram shows, SW communicates with GPIO module by APB BUS. When the module has received active input signals, interrupts will be created to notify ARM core.

6.8.4 Control registers

6.8.4.1 Memory map

Table 6 GPIO Control Register Address Map

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

ARM base address:
For GPIO0~GPIO127:
0x8A00_0000, 0x8A00_0080, 0x8A00_0100, 0x8A00_0180,
0x8A00_0200, 0x8A00_0280, 0x8A00_0300, 0x8A00_0380,

For GPIO128~GPIO131:
0x8200_1780, 0x8200_17C0

Offset Address	Name	Description
0x0000	GPIODATA	GPIO bits data
0x0004	GPIODMSK	GPIO bits data mask
0x0008	GPIODIR	GPIO bits data direction
0x000C	GPIOIS	GPIO bits interrupt sense
0x0010	GPIOIBE	GPIO bits both edges interrupt
0x0014	GPIOIEV	GPIO bits interrupt event
0x0018	GPIOIE	GPIO bits interrupt enable
0x001C	GPIORIS	GPIO bits raw interrupt status
0x0020	GPIOMIS	GPIO bits masked interrupt status
0x0024	GPIOIC	GPIO bits interrupt clear
0x0028	GPIOINEN	GPIO input enable

6.8.4.2 Register description

6.8.4.3 GPIODATA

Description：GPIO bits data register

0x0000			(reset 0x0000_0000)										GPIOATA			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIODATA															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
	[31:16]	R/W	16'h0	Reserved
GPIODATA	[15:0]	R/W	16'h0	GPIO bits data

6.8.4.4 GPIODMSK

Description：GPIO bits mask register

0x0004	(reset 0x0000_0000)												GPIODMSK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIODMSK															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIODMSK	[15:0]	R/W	16'h0	GPIODATA register can be read/write if GPIO DMSK set "1"

6.8.4.5 GPIODIR

Description：GPIO bits direction register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0008			(reset 0x0000_0000)													GPIODIR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIODIR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIODIR	[15:0]	R/W	16'h0	"1" configure gpio bits to be output "0" configure gpio bits to be input

6.8.4.6 GPIOIS

Description：GPIO bits interrupt sense register

0x000C			(reset 0x0000_FFFF)													GPIOIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIS															
Type	R/W															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

GPIOIS	[15:0]	R/W	16'hFFFF	"1" detect signals level "0" detect signals edge

6.8.4.7 GPIOIBE

Description：GPIO bits both edges interrupt register

0x0010			(reset 0x0000_0000)													GPIOIBE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIBE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOIBE	[15:0]	R/W	16'h0	"1" both edges trigger an interrupt, "0" interrupt generation event is controlled by GPIOIEV

6.8.4.8 GPIOIEV

Description： GPIO bits interrupt status register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0014			(reset 0x0000_FFFF)													GPIOIEV
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIEV															
Type	R/W															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOIEV	[15:0]	R/W	16'hFFFF	GPIO bits interrupt event register: "1" high levels trigger interrupts, "0" low levels trigger interrupts.

6.8.4.9 GPIOIE

Description： GPIO bits interrupt enable register

0x0018			(reset 0x0000_0000)													GPIOIE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIE															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[31:16]	RO	16'h0	Reserved
GPIOIE	[15:0]	R/W	16'h0	GPIO bits interrupt enable register: "1" corresponding bit interrupt is enabled. "0" corresponding bit interrupt isn't enabled

6.8.4.10 GPIORIS

Description： GPIO bits raw interrupt status register, and it reflects the status of interrupts trigger conditions detection on pins (prior to GPIOMIS)

0x001C			(reset 0x0000_0000)													GPIORIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIORIS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIORIS	[15:0]	RO	16'h0	GPIO bits raw interrupt status register: "1" interrupt condition met "0" condition not met

6.8.4.11 GPIOMIS

Description： GPIO bits masked interrupt status register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0020			(reset 0x0000_0000)													GPIOMIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOMIS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOMIS	[15:0]	RO	16'h0	GPIO bits masked interrupt status register: "1" Interrupt active "0" interrupt not active

6.8.4.12 GPIOIC

Description： GPIO bits interrupt clear register

0x0024			(reset 0x0000_0000)													GPIOIC
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOIC															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[31:16]	RO	16'h0	Reserved
GPIOIC	[15:0]	WO	16'h0	GPIO bits interrupt clear register: "1" clears detected interrupt. "0" has no effect.

6.8.4.13 GPIOINEN

Description： GPIO input enable register

0x0028	(reset 0x0000_FFFF)												GPIOINEN			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GPIOINEN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:16]	RO	16'h0	Reserved
GPIOINEN	[15:0]	RW	16'h0	GPIO input enable register: "1" input enable. "0" input disable.

6.8.5 Application notes

5) GPIOMIS is equal to GPIOIE & GPIORIS.

6.9 EIC

6.9.1 Overview

The EIC module includes four sub-modules: EIC_DBNC, EIC_LATCH, EIC_ASYNC and EIC_SYNC.

The EIC_DBNC sub-module provides up to 8 source input signal connection. A de-bounce mechanism is used to capture input signal's stable status and a single-trig mechanism is introduced into this sub-module to enhance the input event detect reliability. In addition,

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

this sub-module's clock can be shut off automatically to reduce power dissipation. The de-bounce range is from 1 ms to 4 s with the step of 1 ms. The input signals shorter than 1 ms will be omitted at this sub-module.

THE EIC_LATCH sub-module is used to latch some special input signal and send interrupts to MCU core by channel 0, and it can provides up to 8 EIC_LATCH source input signal connection.

6.9.2 Features

6.9.2.1 EIC_DBNC

- high level detect and interrupt generate(not bypass mode)
- low level detect and interrupt generate(not bypass mode)
- interrupt mask(not bypass mode)
- interrupt clear(not bypass mode)
- level interrupt generate at system power down with once active trig(not bypass mode)
- keep interrupt stable when no interrupt clear(not bypass mode)
- input data sample or mask(not bypass mode)
- de-bounce number configurable(not bypass mode)
- only once trig active(not bypass mode)
- trig level condition configurable(not bypass mode)
- high level detect and interrupt generate(bypass mode)
- low level detect and interrupt generate(bypass mode)
- interrupt mask(bypass mode)
- interrupt clear(bypass mode)
- input data sample or mask(bypass mode)
- level interrupt generate at system power down(bypass mode)
- force to open the clock of de-bounce

6.9.2.2 EIC_LATCH

- Special IRQ or FIQ interrupt on channel 0 is used to latch some input signal status and trigger IRQ or FIQ interrupt by level detecting (no edge detecting)
- Special IRQ or FIQ interrupt on channel 0 is multiplexed from 8 independent input sources
- Using Latch circuit to realize interrupt generation, INTMSK connected to the set port of Latch, and INTCLR connected to the clear port of Latch.
- Provide raw status for each of 8 input sources on special channel
- Provide polarity control bit for each of 8 input sources on special channel
- Provide only one clear bit to clear all latches on special channel
- Each input source can be enabled or disabled independently on special channel

6.9.2.3 EIC_ASYNC

- positive edge detect and interrupt generate
- negative edge detect and interrupt generate
- both edges detect and interrupt generate
- high level detect and interrupt generate
- low level detect and interrupt generate
- interrupt mask
- interrupt clear
- input data sample or mask

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

- level interrupt generate at system power down
- level detect conditions changeable
- edge detect conditions changeable

6.9.2.4 EIC_SYNC

- Input signal synced with clk_apb
- positive edge detect and interrupt generate
- negative edge detect and interrupt generate
- both edges detect and interrupt generate
- high level detect and interrupt generate
- low level detect and interrupt generate
- interrupt mask
- interrupt clear
- input data sample or mask
- level interrupt generate at system power down
- level detect conditions changeable
- edge detect conditions changeable

6.9.3 Funtion description

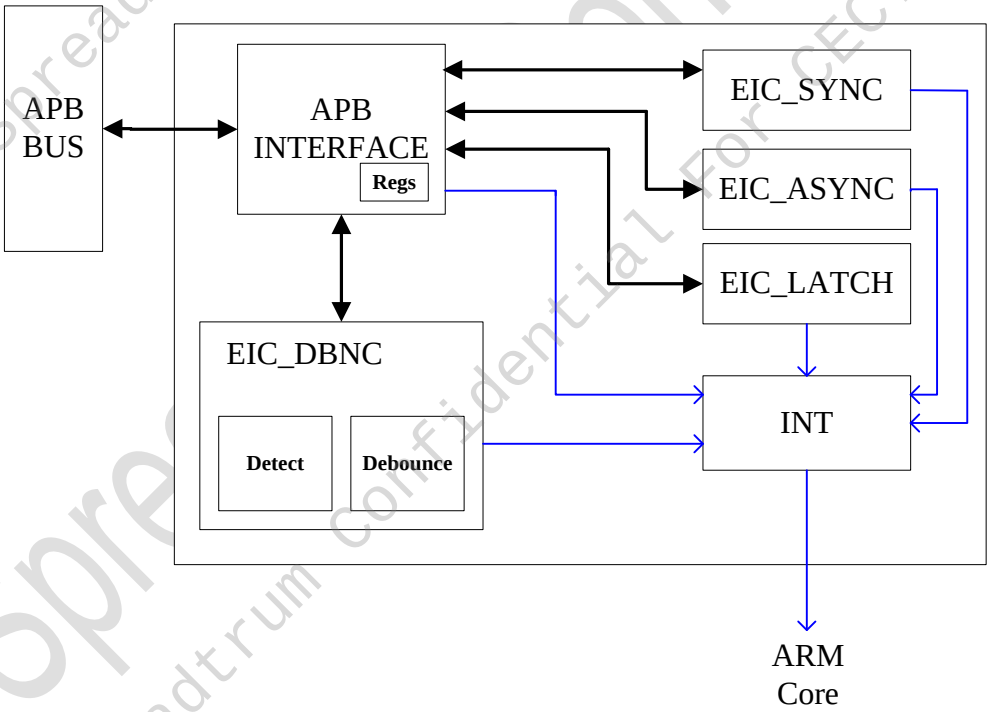


Figure 6-9 EIC block diagram

As the above diagram shows, SW communicates with EIC module by APB BUS. When the module has received active input signals, interrupts will be created to notify ARM core.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.9.4 Control registers

6.9.4.1 Memory map

Table 7 EIC_DBNC Control Register Address Map

ARM base address: 0x8A00_1000 (EIC_DBNC) (EIC0-EIC15)
0x8200_1900 (EIC_DBNCA) (EIC16-EIC31)

Offset Address	Name	Description
0x0000	EIC_DBNC_DATA	EIC_DBNC bits data input
0x0004	EIC_DBNC_DMSK	EIC_DBNC bits data mask
0x0014	EIC_DBNC_IEV	EIC_DBNC bits interrupt event
0x0018	EIC_DBNC_IE	EIC_DBNC bits interrupt enable
0x001C	EIC_DBNC_RIS	EIC_DBNC bits raw interrupt status
0x0020	EIC_DBNC_MIS	EIC_DBNC bits masked interrupt status
0x0024	EIC_DBNC_IC	EIC_DBNC bits interrupt clear
0x0028	EIC_DBNC_TRIG	EIC_DBNC bits trig control
0x0040	EIC0_DBNC_CTRL	EIC0_DBNC control register
0x0044	EIC1_DBNC_CTRL	EIC1_DBNC control register
0x0048	EIC2_DBNC_CTRL	EIC2_DBNC control register
0x004C	EIC3_DBNC_CTRL	EIC3_DBNC control register
0x0050	EIC4_DBNC_CTRL	EIC4_DBNC control register
0x0054	EIC5_DBNC_CTRL	EIC5_DBNC control register
0x0058	EIC6_DBNC_CTRL	EIC6_DBNC control register
0x005C	EIC7_DBNC_CTRL	EIC7_DBNC control register

EIC0-1: come from external pad;
EIC2-15: reserved;
EIC16: from TP_XL;
EIC17: PBINT2;
EIC18: CHGR_INT;
EIC19: PBINT;
EIC20: HEAD_BUTTON;
EIC21: HEADMIC_DETECTION;
EIC22: CHGR_OVI;
EIC23-31: reserved;

Table 8 EIC_LATCH Control Register Address Map

ARM base address: 0x8A00_1080

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description
0x0000	EIC_LATCH_INTEN	EIC_LATCH interrupt enable
0x0004	EIC_LATCH_INTRAW	EIC_LATCH raw interrupt
0x0008	EIC_LATCH_INTMSK	EIC_LATCH interrupt mask
0x000C	EIC_LATCH_INTCLR	EIC_LATCH interrupt clear
0x0010	EIC_LATCH_INTPOL	EIC_LATCH interrupt polarity
0x0014	EIC_LATCH_INTMODE	EIC_LATCH interrupt mode

Table 9 EIC_ASYNC Control Register Address Map

ARM base address: 0x8A00_10A0

Offset Address	Name	Description
0x0000	EIC_ASYNC_INTEN	EIC_ASYNC interrupt enable
0x0004	EIC_ASYNC_INTRAW	EIC_ASYNC raw interrupt
0x0008	EIC_ASYNC_INTMSK	EIC_ASYNC interrupt mask
0x000C	EIC_ASYNC_INTCLR	EIC_ASYNC interrupt clear
0x0010	EIC_ASYNC_INTMODE	EIC_ASYNC interrupt edge or level mode setting
0x0014	EIC_ASYNC_INTBOTH	EIC_ASYNC interrupt both edge setting
0x0018	EIC_ASYNC_INTPOL	EIC_ASYNC interrupt polarity
0x001C	EIC_ASYNC_INTDATA	EIC_ASYNC input data

Table 10 EIC_SYNC Control Register Address Map

ARM base address: 0x8A00_10C0

Offset Address	Name	Description
0x0000	EIC_SYNC_INTEN	EIC_SYNC interrupt enable
0x0004	EIC_SYNC_INTRAW	EIC_SYNC raw interrupt
0x0008	EIC_SYNC_INTMSK	EIC_SYNC interrupt mask
0x000C	EIC_SYNC_INTCLR	EIC_SYNC interrupt clear
0x0010	EIC_SYNC_INTMODE	EIC_SYNC interrupt edge or level mode setting
0x0014	EIC_SYNC_INTBOTH	EIC_SYNC interrupt both edge setting
0x0018	EIC_SYNC_INTPOL	EIC_SYNC interrupt polarity
0x001C	EIC_SYNC_INTDATA	EIC_SYNC input data

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

6.9.4.2 Register description

6.9.4.2.1 EIC_DBNC_DATA

Description： EIC_DBNC bits data register, read only

0x0000			(reset 0x0000_0000)													EIC_DBNC_DATA
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_DATA							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_DBNC_DATA	[7:0]	RO	8'h0	EIC_DBNC bits data input

Note: EIC_DBNC_DATA synchronizes the original data inputs with 2 cycles of Rtcdiv5_clk, so SW need delay 2ms to get the exact value of original data inputs when Rtcdiv5_clk is enabled.

6.9.4.2.2 EIC_DBNC_DMSK

Description： EIC_DBNC bits data mask register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0004			(reset 0x0000_0000)													EIC_DBNC_DMSK
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_DMSK							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_DBNC_DMSK	[7:0]	R/W	8'h0	EIC_DBNC_DATA register can be read if EIC_DBNC_DMSK set "1"

6.9.4.2.3 **EIC_DBNC_IEV**

Description： EIC_DBNC bits interrupt status register

0x0014			(reset 0x0000_00FF)													EIC_DBNC_IEV
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_IEV							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

EIC_DBNC-IEV	[7:0]	R/W	8'hFF	EIC_DBNC bits interrupt status register: "1" high levels trigger interrupts, "0" low levels trigger interrupts.

6.9.4.2.4 **EIC_DBNC_IE**

Description： EIC_DBNC bits interrupt enable register

0x0018			(reset 0x0000_0000)										EIC_DBNC_IE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_IE							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_DBNC_IE	[7:0]	R/W	8'h0	EIC_DBNC bits interrupt enable register: "1" corresponding bit interrupt is enabled. "0" corresponding bit interrupt isn't enabled

6.9.4.2.5 **EIC_DBNC_RIS**

Description： EIC_DBNC bits raw interrupt status register, and it reflects the status of interrupts trigger conditions detection on pins (prior to EIC_DBNC_MIS)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x001C			(reset 0x0000_0000)													EIC_DBNC_RIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_RIS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_DBNC_RIS	[7:0]	RO	8'h0	EIC bits raw interrupt status register: "1" interrupt condition met "0" condition not met

6.9.4.2.6 **EIC_DBNC_MIS**

Description： EIC_DBNC bits masked interrupt status register

0x0020			(reset 0x0000_0000)													EIC_DBNC_MIS
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_MIS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: EIC_DBNC_MIS = EIC_DBNC_IE & EIC_DBNC_RIS

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_DBNC_MIS	[7:0]	RO	8'h0	EIC_DBNC bits masked interrupt status register: "1" Interrupt active "0" interrupt not active

6.9.4.2.7 **EIC_DBNC_IC**

Description： EIC_DBNC_ bits interrupt clear register

0x0024			(reset 0x0000_0000)													EIC_DBNC_IC
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_IC							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	WO	24'h0	Reserved
EIC_DBNC_IC	[7:0]	WO	8'h0	EIC_DBNC bits interrupt clear register: "1" clears detected interrupt. "0" has no effect.

6.9.4.2.8 **EIC_DBNC_TRIG**

Description： EIC_DBNC bits trig control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0028			(reset 0x0000_0000)													EIC_DBNC_TRIG
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_DBNC_TRIG							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	WO	24'h0	Reserved
EIC_DBNC_TRIG	[7:0]	WO	8'h0	EIC_DBNC bits trig control register: "1": generate the trig_start pulse "0": no effect It must set EIC_DBNC_TRIG for using de-bounce function and getting active interrupt.

6.9.4.2.9 **EIC0_DBNC_CTRL**

Description： EIC0_DBNC control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0040			(reset 0x0000_4032)												EIC0_DBNC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.10 **EIC1_DBNC_CTRL**

Description： EIC1_DBNC control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0042			(reset 0x0000_4032)												EIC1_DBNC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.11 **EIC2_DBNC_CTRL**

Description： EIC2_DBNC control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0048			(reset 0x0000_4032)												EIC2_DBNC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.12 **EIC3_DBNC_CTRL**

Description： EIC3 control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x004C			(reset 0x0000_4032)												EIC3_DBNC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.13 **EIC4_DBNC_CTRL**

Description： EIC4_DBNC control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0050			(reset 0x0000_4032)												EIC4_DBNC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.14 **EIC5_DBNC_CTRL**

Description： EIC5_DBNC control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0054			(reset 0x0000_4032)												EIC5_DBNC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.15 **EIC6_DBNC_CTRL**

Description： EIC6_DBNC control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0058			(reset 0x0000_4032)												EIC6_DBNC_CTRL	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.16 **EIC7_DBNC_CTRL**

Description： EIC7 control register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x005C			(reset 0x0000_4032)													EIC7_DBNC_CTRL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FORCE_CLK_DBNC	DBNC_EN	Reserved		DBNC_CNT											
Type	R/W	R/W	RO		R/W											
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Field Name	Bit	Type	Reset Value	Description
/	[31:16]	RO	16'd0	Reserved
FORCE_CLK_DBNC	[15]	R/W	1'h0	1: clock of dbnc forced open; 0: no effect
DBNC_EN	[14]	R/W	1'h1	de-bounce mechanism enable or disable: 1 enable,0 disable(bypass)
/	[13:12]	RO	2'd0	Reserved
DBNC_CNT	[11:0]	R/W	12'h032	de-bounce counter period value setting, the unit is millisecond

6.9.4.2.17 **EIC_LATCH_INTEN**

Description：EIC_LATCH interrupt enable register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0000			(reset 0x0000_0000)											EIC_LATCH_INTEN			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_LATCH_INTEN							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_LATCH_INTEN	[7:0]	RW	8'h0	EIC_LATCH interrupt enable register: "1": enable bit interrupt "0": disable bit interrupt

6.9.4.2.18 **EIC_LATCH_INTRAW**

Description：EIC_LATCH raw interrupt register

0x0004			(reset 0x0000_0000)											EIC_LATCH_INTRAW		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_LATCH_INTRAW							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[31:8]	RO	24'h0	Reserved
EIC_LATCH_INTRAW	[7:0]	RW	8'h0	EIC_LATCH raw interrupt status register: "1" interrupt condition met "0" condition not met

6.9.4.2.19 **EIC_LATCH_INTMSK**

Description：EIC_LATCH interrupt mask register

0x0008			(reset 0x0000_0000)												EIC_LATCH_INTMSK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_LATCH_INTMSK							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_LATCH_INTMSK	[7:0]	RO	8'h0	EIC_LATCH interrupt mask register "1" Interrupt active "0" interrupt not active

Note: EIC_LATCH_INTMSK = EIC_LATCH_INTEN & EIC_LATCH_INTRAW, and EIC_LATCH_INTMSK are connected to the set port of Latch

6.9.4.2.20 **EIC_LATCH_INTCLR**

Description：EIC_LATCH interrupt clear register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x000C			(reset 0x0000_0000)										EIC_LATCH_INTCLR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_LATCH_INTCLR							
Type	RO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_LATCH_INTCLR	[7:0]	WO	8'h0	EIC_LATCH interrupt clear register: "1" clears detected interrupt. "0" has no effect.

Note: EIC_LATCH_INTCLR are connected to the "clear" port of Latch, and it need disable the "set" port of Latch by changing EIC_LATCH_INTPOL to clear EIC_LATCH interrupt.

6.9.4.2.21 **EIC_LATCH_INTPOL**

Description：EIC_LATCH interrupt polarity register

0x0010			(reset 0x0000_0000)										EIC_LATCH_INTPOL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_LATCH_INTPOL							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_LATCH_INTPOL	[7:0]	RW	8'h0	EIC_LATCH polarity register: "0": high levels trigger interrupts, "1": low levels trigger interrupts.

6.9.4.2.22 **EIC_LATCH_INTMODE**

Description： EIC_LATCH interrupt mode register

0x0014			(reset 0x0000_0000)										EIC_LATCH_INTMODE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_LATCH_INTMODE							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_LATCH_INTMODE	[7:0]	RW	8'h0	EIC_LATCH interrupt mode register: "1": interrupt active without chip sleep "0": interrupt active with chip sleep

6.9.4.2.23 **EIC_ASYNC_INTIE**

Description： EIC_ASYNC bits interrupt enable register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0000			(reset 0x0000_0000)													EIC_ASYNC_INTIE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_INTIE							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_ASYNC_IE	[7:0]	R/W	8'h0	EIC_ASYNC bits interrupt enable register: "1" corresponding bit interrupt is enabled. "0" corresponding bit interrupt isn't enabled

6.9.4.2.24 **EIC_ASYNC_INTRAW**

Description：EIC_ASYNC raw interrupt register

0x0004			(reset 0x0000_0000)													EIC_ASYNC_INTRAW
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_INTRAW							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_ASYNC_INTRAW	[7:0]	RW	8'h0	EIC_ASYNC raw interrupt status register: "1" interrupt condition met "0" condition not met

6.9.4.2.25 **EIC_ASYNC_INTMSK**

Description：EIC_ASYNC interrupt mask register

0x0008	(reset 0x0000_0000)												EIC_ASYNC_INTMSK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_INTMSK							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_ASYNC_INTMSK	[7:0]	RO	8'h0	EIC_ASYNC interrupt mask register "1" Interrupt active "0" interrupt not active

6.9.4.2.26 **EIC_ASYNC_INTCLR**

Description：EIC_ASYNC interrupt clear register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x000C			(reset 0x0000_0000)										EIC_ASYNC_INTCLR			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_INTCLR							
Type	RO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_ASYNC_INTCLR	[7:0]	WO	8'h0	EIC_ASYNC interrupt clear register: "1" clears detected interrupt. "0" has no effect.

6.9.4.2.27 **EIC_ASYNC_INTMODE**

Description：EIC_ASYNC bits interrupt mode register

0x0010			(reset 0x0000_FFFF)										EIC_ASYNC_INTMODE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_INTCLR							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
	[31:8]	RO	24'h0	Reserved
EIC_ASYNC_INTMODE	[7:0]	R/W	8'hFFFF	"1" detect signals level "0" detect signals edge

6.9.4.2.28 **EIC_ASYNC_INTBOTH**

Description：EIC_ASYNC bits both edges interrupt register

0x0014	(reset 0x0000_0000)												EIC_ASYNC_INTBOTH			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_INTBOTH							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	16'h0	Reserved
EIC_ASYNC_INTBOTH	[7:0]	R/W	16'h0	"1" both edges trigger an interrupt, "0" interrupt generation event is controlled by EIC_ASYNC_INTMODE

6.9.4.2.29 **EIC_ASYNC_INTPOL**

Description：EIC_ASYNC interrupt polarity register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0018			(reset 0x0000_0000)													EIC_ASYNC_INTPOL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_INTPOL							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_ASYNC_INTPOL	[7:0]	RW	8'h0	EIC_ASYNC polarity register: "1": high levels or pos-edge trigger interrupts, "0": low levels or neg-edge trigger interrupts.

6.9.4.2.30 **EIC_ASYNC_DATA**

Description： EIC_ASYNC bits data register, read only

0x001C			(reset 0x0000_0000)													EIC_ASYNC_DATA
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_ASYNC_DATA							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_ASYNC_DATA	[7:0]	RO	8'h0	EIC_ASYNC bits data input

6.9.4.2.31 **EIC_SYNC_INTIE**

Description： EIC_SYNC bits interrupt enable register

0x0000	(reset 0x0000_0000)														EIC_SYNC_INTIE	
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_INTIE							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_SYNC_IE	[7:0]	R/W	8'h0	EIC_SYNC bits interrupt enable register: "1" corresponding bit interrupt is enabled. "0" corresponding bit interrupt isn't enabled

6.9.4.2.32 **EIC_SYNC_INTRAW**

Description：EIC_SYNC raw interrupt register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0004			(reset 0x0000_0000)										EIC_SYNC_INTRAW			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_INTRAW							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_SYNC_INTRAW	[7:0]	RW	8'h0	EIC_SYNC raw interrupt status register: "1" interrupt condition met "0" condition not met

6.9.4.2.33 **EIC_SYNC_INTMSK**

Description：EIC_SYNC interrupt mask register

0x0008			(reset 0x0000_0000)										EIC_SYNC_INTMSK			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_INTMSK							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
	[31:8]	RO	24'h0	Reserved
EIC_SYNC_INTMSK	[7:0]	RO	8'h0	EIC_SYNC interrupt mask register "1" Interrupt active "0" interrupt not active

6.9.4.2.34 **EIC_SYNC_INTCLR**

Description：EIC_SYNC interrupt clear register

0x000C			(reset 0x0000_0000)													EIC_SYNC_INTCLR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_INTCLR							
Type	RO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_SYNC_INTCLR	[7:0]	WO	8'h0	EIC_SYNC interrupt clear register: "1" clears detected interrupt. "0" has no effect.

6.9.4.2.35 **EIC_SYNC_INTMODE**

Description：EIC_SYNC bits interrupt mode register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0010			(reset 0x0000_FFFF)											EIC_SYNC_INTMODE		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_INTCLR							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_SYNC_INTMODE	[7:0]	R/W	8'hFFFF	"1" detect signals level "0" detect signals edge

6.9.4.2.36 **EIC_SYNC_INTBOTH**

Description：EIC_SYNC bits both edges interrupt register

0x0014			(reset 0x0000_0000)											EIC_SYNC_INTBOTH		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_INTBOTH							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	[31:8]	RO	16'h0	Reserved
EIC_SYNC_INTBOTH	[7:0]	R/W	16'h0	"1" both edges trigger an interrupt, "0" interrupt generation event is controlled by EIC_SYNC_INTMODE

6.9.4.2.37 **EIC_SYNC_INTPOL**

Description：EIC_SYNC interrupt polarity register

0x0018	**(reset 0x0000_0000)**												EIC_SYNC_INTPOL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_INTPOL							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	**Bit**	**Type**	**Reset Value**	**Description**
	[31:8]	RO	24'h0	Reserved
EIC_SYNC_INTPOL	[7:0]	RW	8'h0	EIC_SYNC polarity register: "1": high levels or pos-edge trigger interrupts, "0": low levels or neg-edge trigger interrupts.

6.9.4.2.38 **EIC_SYNC_DATA**

Description： EIC_SYNC bits data register, read only

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x001C			(reset 0x0000_0000)													EIC_SYNC_DATA
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								EIC_SYNC_DATA							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	Type	Reset Value	Description
	[31:8]	RO	24'h0	Reserved
EIC_SYNC_DATA	[7:0]	RO	8'h0	EIC_SYNC bits data input

6.9.5 Application notes

6.9.5.1 Programming Model

For EIC_DBNC sub-module, software needs to adopt corresponding steps as follows:

6) When system resets, EIC_DBNC module is also under the reset status and cannot capture the EIC_DBNC input signals. At the process of system initialization, ARM needs to configure the EIC_DBNC input signal detecting conditions, such as '1'/'0' detection, read INT status registers and write EIC_DBNC_IC to clear the EIC_DBNC INTs. Then, if necessary, ARM sends a trig_start pulse to commence one EIC signal detection process. Before system enters deep-sleep mode or closes PCLK, it ought to assure that EIC_DBNC INT has been enabled and cleared and system has sent out active trig_start pulse.
7) After receiving the trig_start pulse, EIC_DBNC module starts the process of EIC_DBNC signal detection. If EIC captures one stable input signal, it will send an INT to ARM, shut off the clock of debounce circuit automatically and wait for next trig_start pulse.
8) When ARM receives the EIC_DBNC INT again, it enters INT process flow. And if EIC input condition changes, ARM needs to configure those detecting condition registers again. Then, if necessary, ARM sends a trig_start pulse again to commence a new EIC_DBNC signal detection process.
9) Step 1 to step 3 cycles.
10) For the debounce bypass mode, ARM can receive INT without the need of sending trig_start pulse.

6.9.5.2 Programming Notes

6) The register, EIC_DBNC_IEV, is used to set the input signal constraints for INT trigger.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

7) EIC_DBNC_INT comes from EIC_DBNC_MIS, which EIC_DBNC_MIS is equal to EIC_DBNC_IE & EIC_DBNC_RIS. So, if it needs to get some EIC_DBNC' INT, the EIC_DBNC_IE should be unmasked. And if ARM has received one EIC_DBNC INT, it maybe need to mask the corresponding bit of EIC_DBNC_IE to avoid to received the same INT, and set corresponding bits 1 to of EIC_DBNC_IC.
8) To quit EIC_DBNC FSM correctly, it needs 2 or 3 additional milliseconds. So it needs consider the additional time for exact debounce period.

6.10 SDIO Controller

6.10.1 Overview

The SD/SDIO/MMC4/CE-ATA Host Controller handles SD/SDIO/MMC4/CE-ATA protocol at transmission level, packing data, adding cyclic redundancy check (CRC), start/end bit, and checking for transaction format correctness. SD mode wide bus width is also supported. The controller conforms to SD Host Controller Standard Specification Draft Version 1.0.

The SD/SDIO/MMC4/CE-ATA Host Controller provides programmed I/O method and DMA data transfer method. In programmed I/O method, the ARM processor transfers data using the Buffer Data Port Register. Host controller's support for DMA can be determined by checking the DMA support in the *Capabilities* register. DMA allows a peripheral to read or write memory without the intervention from the CPU. The *System Address* register points to the first data address, and data is then accessed sequentially from that address.

CE-ATA

- Optimized HDD Interface for handhelds that build on proven technologies
- Added enhancements to MMC to deliver an optimized HDD interface
- After Power-UP or Reset, the device places the signature in its registers
- Host Software reads the signature to determine if the device is CE-ATA compliant
- Utilize the same MMC command sequences for initialization and new commands (CMD60 & CMD61) defined by CE-ATA for efficient HDD command execution

6.10.2 Features

- Meet SD Host Controller Standard Specification Draft version 2.0
- Meet SDIO card specification version 2.0.
- Meet SD Memory Card Security Specification version 2.0
- Meet MMC Specification version 3.31 and 4.0
- Meet AHB-Lite Specification
- Support both DMA and non-DMA mode of operation
- Support MMC Plus and MMC Mobile
- Card Detection (insertion/removal)
- Password protection of cards

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

- Host clock rate variable between 0 and 48 MHz
- Support 1 bit and 4 bit SD modes
- Support Multi Media Card Interrupt mode
- Allow card to interrupt host in 1 bit, and 4 bit SD modes
- Up to 10M bytes per second read and write rates using 4 parallel data lines (SD 4-bit mode)
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity
- Error Correction Code (ECC) support for MMC4.0 cards
- Designed to work with I/O cards, Read-only cards and Read/Write cards
- Support Read wait control, Suspend/Resume operations
- Support FIFO Overrun and Underrun conditions by stopping SD clock
- Conform to AMBA specification AHB 2.0

6.10.3 SDIO Control Registers

6.10.3.1 Memory Map

Table 6-9 SD/SDIO/MMC4/CE-ATA control registers

Offset Address	Name	Description
0x0000	SYS_ADDR	System address
0x0004	BLK_SIZE	Block size and count
0x0008	ARG	Argument
0x000C	TR_MODE	Transfer mode and command
0x0010	RESP0	Response 0, 1
0x0014	RESP2	Response 2, 3
0x0018	RESP4	Response 4, 5
0x001C	RESP6	Response 6, 7
0x0020	BUF_PRT	Buffer data port
0x0024	PRES_STATE	Present state
0x0028	SD_CTRL1	SD control 1
0x002C	SD_CTRL2	SD control 2
0x0030	INT_ST	Normal and error interrupt status
0x0034	INT_ST_EN	Interrupt status enable
0x0038	INT_SIG_EN	Interrupt signal enable
0x003C	CMD12_ST	Auto CMD12 error status
0x0040	CAP1	Capabilities 1
0x0044	CAP2	Capabilities 2 (reserved)
0x0048	MAX_CUR_CAP1	Maximum current capabilities 1
0x004C	MAX_CUR_CAP2	Maximum current capabilities 2 (reserved)
…	…	…
0x00FC	SLT_INT_ST	Slot interrupt status and version number

Note:

The SD host controller registers given above are for Slot 1. The same set of registers is used for Slot 2.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Address range for Slot 1: 0x0000 ~ 0x00FF

Address range for Slot 2: 0x0100 ~ 0x01FF

The following abbreviations are used in the tables.

RO: Read-only register

ROC: Read-only status. These bits are initialized to zero at reset. Write to this bit is ignored.

R/W: Read-write registers

RW1C: Read-only status, write 1 to clear status: register bits indicate status when read, a set bit indicating a event may be cleared by writing 1, Writing 0 has no effect.

RWAC: Read-write, automatic clear registers: writing 1 to such a bit starts an operation, and this bit will automatically clear to 0 after the operation is done. Writing 0 to such a bit has no effect.

HWinit: Hardware initialized: registers are frozen, bits are read-only after initialization, and writing to these bits are ignored.

Rsvd: Reserved. Reading these bits gets zero, and writing to these bits are ignored.

6.10.3.2 Register Descriptions

6.10.3.2.1 SYS_ADDR

0x0000	System Address															SYS_ADDR
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	DMA_SYS_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DMA_SYS_ADDR															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
DMA_SYS_ADDR	[31:0]	RO	18'h0	DMA system address.

Note: This register contains the system memory address for a DMA transfer. When the Host Controller (HC) stops a DMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during a transfer return an invalid value. The Host Driver (HD) shall initialize this register before starting a DMA transaction. After DMA has stopped, the next system address of the next contiguous data position can be read from this register. The DMA transfer waits at every boundary specified by the **Host DMA Buffer Size** in the Block Size register. The Host Controller generates DMA **Interrupt** to request to update this register. The HD set the next system address of the next data position to this register. When most upper byte of this register (0x0003) is written, the HC restarts the DMA transfer. When restarting DMA by the resume command or by setting **Continue Request** in the Block Gap Control register, the HC shall start at the next contiguous address stored here in the System Address register

6.10.3.2.2 BLK_SIZE

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0004 **Block size and count** **BLK_SIZE**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BLK_CNT															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TR_BLK_SIZE	HST_DMA_BUF_SIZE			TR_BLK_SIZE											
Type	R/W	R/W			R/W											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
BLK_CNT	[31:16]	RW	16'h0	Block count. This register is enabled when **Block Count Enable** in the Transfer Mode register is set to 1 and is valid only for multiple block transfers. The HC decrements the block count after each block transfer and stops when the count reaches zero. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored. When saving transfer context as a result of Suspend command, the number of blocks yet to be transferred can be determined by reading this register. When restoring transfer context prior to issuing a Resume command, the HD shall restore the previously saved block count.0x0000: stop count0x0001: 1 block0x0002: 2 blocks…0xFFFF: 65535 blocks
TR_BLK_SIZE	[15]	RW	1'b0	Transfer block size bit [12]. This bit is added to support 4 kb data block transfer.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

HST_DMA_BUF_SIZE	[14:12]	RW	3'b0	Host DMA buffer size. To perform long DMA transfer, System Address register shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at every boundary specified by these fields and the HC generates the **DMA Interrupt** to request the HD to update the System Address register. These bits shall be used when the **DMA Support** in the Capabilities register is set to 1 and this function is active when the **DMA Enable** in the Transfer Mode register is set to 1. 000: 4 KB (detect A11 carry out) 001: 8 KB (detect A11 carry out) 010: 16 KB (detect A11 carry out) 011: 32 KB (detect A11 carry out) 100: 64 KB (detect A11 carry out) 101: 128 KB (detect A11 carry out) 110: 256 KB (detect A11 carry out) 111: no limit, HC will not generate the DMA interrupt
TR_BLK_SIZE	[11:0]	RW	12'b0	Transfer block size. This register specifies the block size for block data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored. 0x0000: no data transfer 0x0001: 1 byte 0x0002: 2 bytes … 0x0200: 512 bytes

6.10.3.2.3 **ARG**

0x0008 **Argument** **ARG**

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	CMD_ARG															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CMD_ARG															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Default	Description
CMD_ARG	[31:0]	RW	16'h0	Commend argument. The SD Command Argument is specified as bits [39:8] of Command Format.

6.10.3.2.4 **TR_MODE**

0x000C **Transfer mode and command** **TR_MODE**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved		CMD_INDEX						CMD_TYPE		DATA_PRE_SEL	CMD_IND_CHK_EN	CMD_CRC_CHK_EN	Reserved	RESP_TYPE_SEL	
Type			R/W						R/W		R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved									CMD_COMP_ATA	MULT_BLK_SEL	DATA_DIR_SEL		AUTO_CMD12_EN	BLK_CNT_EN	DMA_EN
Type										R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:30]	RO	2'b0	Reserved
CMD_INDEX	[29:24]	RW	6'b0	Command index, set to the command number (CMD0-63, ACMD0-63)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

CMD_TYPE	[23:22]	RW	2'b0	Commend type. There are three types of special commands, Suspend, Resume and Abort. These bits shall bet set to 00b for all other commands. 00: Normal 01: Suspend 10: Resume 11: Abort **Suspend** If the Suspend command succeeds, the HC shall assume the SD Bus has been released and that it is possible to issue the next command which uses the DAT line. The HC shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The Interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the HC shall maintain its current state, and the HD shall restart the transfer by setting **Continue Request** in the Block Gap Control Register. **Resume** The HD re-starts the data transfer by restoring the registers in the range of 0x0000 ~ 0x000D. The HC shall check for busy before starting write transfers. **Abort** If this command is set when executing a read transfer, the HC shall stop read to the buffer. If this command is set when executing a write transfer, the HC shall stop driving the DAT line. After issuing the Abort command, the HD should issue a software reset.
DATA_PRE_SEL	[21]	RW	1'b0	Data present select 0: no data present 1: data present This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: 1. Commands using only CMD line (e.g., CMD52) 2. Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b, e.g., CMD38) 3. Resume Command

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

CMD_IND_CHK_EN	[20]	RW	1'b0	Command index check enable 0: disable 1: enable If this bit is set to 1, the HC shall check the index field in the Response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked.
CMD_CRC_CHK_EN	[19]	RW	1'b0	Command CRC check enable 0: disable 1: enable If this bit is set to 1, the HC shall check the CRC field in the Response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked.
	[18]	RO	1'b0	Reserved
RESP_TYPE_SEL	[17:16]	RW	2'b0	Response type select 00: no response 01: response length 136 10: response length 48 11: response length 48, check Busy after response
	[15:7]	RO	8'b0	Reserved
CMD_COMP_ATA	[6]	RW	1'b0	Command completion signal enable for CE-ATA device 0: device will not send command completion signal 1: device will send command completion signal
MULT_BLK_SEL	[5]	RW	1'b0	Multiple/single block select 0: single block 1: multiple blocks
DATA_DIR_SEL	[4]	RW	1'b0	Data transfer direction select 0: write (Host to Card) 1: read (Card to Host)
	[3]	RO	1'b0	Reserved
AUTO_CMD12_EN	[2]	RW	1'b0	Auto CMD12 enable 0: disable 1: enable Multiple block transfers for memory require CMD12 to stop the transaction. When this bit is set to 1, the HC shall issue CMD12 automatically when last block transfer is completed. The HD shall not set this bit to issue commands that do not require CMD12 to stop data transfer.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

BLK_CNT_EN	[1]	RW	1'b0	Block count enable 0: disable 1: enable This bit is used to enable the Block count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer.
DMA_EN	[0]	RW	1'b0	DMA enable 0: disable 1: enable DMA can be enabled only if **DMA Support** bit in the Capabilities register is set. If this bit is set to 1, a DMA operation shall begin when the HD writes to the upper byte of Command register (0x000F).

6.10.3.2.5 **RESP0**

0x0010 **Response 0 and 1** **RESP0**

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	RESPONSE [31:16]															
Type	ROC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RESPONSE [15:0]															
Type	ROC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	**Bit**	**R/W**	**Default**	**Description**
RESP0	[31:0]	RW	32'h0	

6.10.3.2.6 **RESP2**

0x0014 **Response 2 and 3** **RESP2**

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	RESPONSE [63:48]															
Type	ROC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RESPONSE [47:32]															
Type	ROC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Default	Description
RESP2	[31:0]	RW	32'h0	

6.10.3.2.7 **RESP4**

0x0018 **Response 4 and 5** **RESP4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESPONSE [95:80]															
Type	ROC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESPONSE [79:64]															
Type	ROC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
RESP4	[31:0]	RW	32'h0	

6.10.3.2.8 **RESP6**

0x001C **Response 6 and 7** **RESP6**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESPONSE [127:112]															
Type	ROC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESPONSE [111:96]															
Type	ROC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
RESP4	[31:0]	RW	32'h0	

6.10.3.2.9 **BUF_PRT**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0020 **Buffer data port** **BUF_PRT**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF_DATA															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_DATA															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
BUF_DATA	[31:0]	RW	32'h0	The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

6.10.3.2.10 **PRES_STATE**

0x0024 **Present state** **PRES_STATE**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved			DAT7_4_SIG_LVL				CMD_SIG_LVL	DAT3_0_SIG_LVL				W_PRO_LVL	CRD_DET_LVL	CRD_STATE_STABLE	CRD_INSERTED
Type				RO				RO	RO				RO	RO	RO	RO
Reset	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved				BUF_READ_EN	BUF_WR_EN	READ_ACTIVE	WRITE_ACTIVE	Reserved					DAT_LINE_ACTIVE	CMD_INH_DAT	CMD_INH_CMD
Type					ROC	ROC	ROC	ROC						ROC	ROC	ROC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:25]	RW		Reserved
CMD_SIG_LVL	[24]			CMD line signal level. This status is used to check **CMD** line level to recover from errors, and for debugging.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				DAT [3:0] line signal level. This status is used to check **DAT** line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT [0]. [23]: for DAT[3] [22]: for DAT[2] [21]: for DAT[1] [20]: for DAT[0]
DAT3_0_SIG_LVL	[23:20]			
	[19:12]			Reserved
BUF_READ_EN	[11]			Buffer read enable. This status is used for non-DMA read transfers. This read only flag indicates that valid data exists in the Host side buffer. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when all the block data is ready in the buffer and the **Buffer Read Ready** Interrupt is generated. 0: read disable 1: read enable
BUF_WR_EN	[10]			Buffer write enable. This status is used for non-DMA write transfers. This write only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer. A change of this bit from 0 to 1 occurs when top of block data can be written to the buffer and the **Buffer Write Ready** Interrupt is generated. 0: write disable 1: write enable
READ_ACTIVE	[9]			Read transfer active. This status is used for detecting completion of a read transfer. This bit is set to 1 for either of the following conditions: 1. After the end bit of the read command 2. When writing a 1 to continue Request in the Block Gap Control register to restart a read transfer This bit is cleared to 0 for either of the following conditions: 1. When the last data block as specified by block length is transferred to the system. 2. When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop at Block Gap Request set to 1. A transfer complete interrupt is generated when this bit changes to 0. 0: no valid data 1: transferring data

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

WRITE_ACITVE	[8]			Write transfer active. This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the HC. This bit is set in either of the following cases: 1. After the end bit of the write com mand 2. When writing a 1 to Continue Request in the Block Gap Control register to restart a write transfer This bit is cleared in either of the following cases: 1. After getting the CRC status of the last data block as specified by the t ransfer count (Single or Multiple) 2. After getting a CRC status of any block where data transmission is about to be stopped by a Stop at Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as a result of the Stop at Block Gap Request being set. This status is useful for the HD in determining when to issue commands during write busy. 0: no valid data 1: transferring data
	[7:3]			Reserved
DAT_LINE_ACTIVE	[2]			DAT line active. This bit indicates whether one of the **DAT** line on SD bus is in use. 0: DAT line inactive 1: DAT line active
				Command inhibit (DAT). This status bit is generated if either the **DAT Line Active** or the **Read Transfer Active** is 1. If this bit is 0, it indicates the HC can issue the next SD command. Commands with busy signal belong to **Command Inhibit (DAT)** (e.g., R1b, R5b type). Changing from 1 to 0 generates a **Transfer Complete** interrupt in the Normal Interrupt status register.Note: The SD Host Driver can save registers in the range of 0x0000 ~ 0x000D for a suspend transaction after this bit has changed from 1 to 0. 0: can issue command that uses the DAT line 1: cannot issue command that uses the DAT line
CMD_INH_DAT	[1]			

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

CMD_INH_CMD	[0]			Command inhibit (CMD). If this bit is 0, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after the Command register (0x000F) is written. This bit is cleared when the command response is received. Even if the Command Inhibit (DAT) is set to 1, Commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a Command complete interrupt in the Normal Interrupt Status register. If the HC cannot issue the command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1 and the Command Complete is not set. Status issuing Auto CMD12 is not read from this bit.

6.10.3.2.11 **SD_CTRL1**

0x0028 **SD control 1 (host, power, block gap, wakeup)** **SD_CTRL1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved					WK_EN_CRD_REM	WK_EN_CRD_INS	WK_EN_CRD_INT	Reserved				INT_AT_BLK_GAP	RD_WAIT_CTRL	CONT_REQUEST	STP_AT_BLK_GAP_REQ
Type						R/W	R/W	R/W					R/W	R/W	RWAC	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				SD_BUS_V_SEL			SD_BUS_PWR	Reserved		SD8B_MODE	Reserved		HI_SPD_EN	SD4B_MODE	LED_ON
Type					R/W			R/W			R/W			R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:27]			Reserved
WK_EN_CRD_REM	[26]			Wakeup event enable on SD card removal. This bit enables wakeup event via **Card Removal** assertion in the Normal Interrupt Status register. **FN_WUS** (Wakeup Support) in CIS does not affect this bit. 0: disable 1: enable

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

WK_EN_CRD_INS	[25]			Wakeup event enable on SD card insertion. This bit enables wakeup event via **Card Insertion** assertion in the Normal Interrupt Status register. **FN_WUS** (Wakeup Support) in CIS does not affect this bit. 0: disable 1: enable
WK_EN_CRD_INT	[24]			Wakeup event enable on SD card interrupt. This bit enables wakeup event via **Card Interrupt** assertion in the Normal Interrupt Status register. This bit can be set to 1 if FN_WUS (Wakeup Support) in CIS is set to 1. 0: disable 1: enable
	[23:20]			Reserved
INT_AT_BLK_GAP	[19]			Interrupt at block gap. This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card.
RD_WAIT_CTRL	[18]			Read wait control. The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise, the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1 or DAT line conflict may occur. If this bit is set to 0, Suspend/Resume cannot be supported. 0: disable read wait control 1: enable read wait control

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

CONT_REQUEST	[17]			Continue request. This bit is used to restart a transaction that was stopped using the Stop at Block Gap Request. To cancel stop at the block gap, set Stop at Block Gap Request to 0 and set this bit to restart the transfer. The HC automatically clears this bit in either of the following cases: 1. In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts 2. In the case of a write transaction, the Write transfer active changes from 0 to 1 as the write transaction restarts Therefore it is not necessary for Host driver to set this bit to 0. If Stop at Block Gap Request is set to 1, any write to this bit is ignored. 0: ignored 1: restart
STP_AT_BLK_GAP_REQ	[16]			Stop at block gap request. This bit is used to stop executing a transaction at the next block gap for both DMA and non-DMA transfers. Until the transfer complete is set to 1, indicating a transfer completion, the HD shall leave this bit set to 1. Clearing both the Stop at Block Gap Request and Continue Request shall not cause the transaction to restart. Read Wait is used to stop the read transaction at the block gap. The HC shall honor Stop at Block Gap Request for write transfers, but for read transfers it requires that the SD card support Read Wait. Therefore the HD shall not set this bit during read transfers unless the SD card supports Read Wait and has set Read Wait Control to 1. In case of write transfers in which the HD writes data to the Buffer Data Port register, the HD shall set this bit after all block data is written. If this bit is set to 1, the HD shall not write data to Buffer data port register. This bit affects Read Transfer Active, Write Transfer Active, DAT line active and Command Inhibit (DAT) in the Present State register. 0: transfer 1: stop
	[15:12]			Reserved
SD_BUS_V_SEL	[11:9]			SD bus voltage select. By setting these bits, the HD selects the voltage level for the SD card. Before setting this register, the HD shall check the **voltage support** bits in the Capabilities register. If an unsupported voltage is selected, the Host System shall not supply SD bus voltage. 000, 101: 1.80 V (typical) 001, 010, 011: 2.65 V (typical) 100: 2.80 V (typical) 110, 111: 3.00 V (typical)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				SD bus power. Before setting this bit, the SD host driver shall set SD Bus Voltage Select. If the HC detects the No Card State, this bit shall be cleared. 0: power off 1: power on
SD_BUS_PWR	[8]			
	[7:3]			Reserved
HI_SPD_EN	[2]			High speed enable. This bit is optional. Before setting this bit, the HD shall check the **High Speed Support** in the Capabilities register. If this bit is set to 0 (default), the HC outputs **CMD** line and **DAT** line at the falling edge of the SD clock (up to 25 MHz). If this bit is set to 1, the HC outputs **CMD** line and **DAT** line at the rising edge of the SD clock (up to 50 MHz). 0: normal speed mode 1: high speed mode
SD4B_MODE	[1]			Data transfer width, SD1 or SD4. This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. 0: 1-bit mode 1: 4-bit mode
	[0]			Reserved

6.10.3.2.12 **SD_CTRL2**

0x002C **SD control 2 (clock, timeout, software reset)** **SD_CTRL2**

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved					SW_RST_DAT	SW_RST_CMD	SW_RST_ALL	Reserved				DATA_TIMEOUT_CNT			
Type						RWAC	RWAC	RWAC					R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SDCLK_FRQ_SEL								Reserved					SDCLK_EN	INT_CLK_STABLE	INT_CLK_EN
Type	R/W													R/W	ROC	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	**Bit**	**R/W**	**Default**	**Description**
	[31:27]			Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SW_RST_DAT	[26]			Software reset for DAT line. Only part of data circuit is reset. DMA circuit is also reset. The following registers and bits are cleared by this bit: • Buffer Data Port Register: ▪ Buffer is cleared and initialized. • Present State register: ▪ Buffer Read Enable ▪ Buffer Write Enable ▪ Read Transfer Active ▪ Write Transfer Active ▪ DAT Line Active ▪ Command Inhibit (DAT) • Block Gap Control register: ▪ Continue Request ▪ Stop At Block Gap Request • Normal Interrupt Status register ▪ Buffer Read Ready ▪ Buffer Write Ready ▪ Block Gap Event Transfer Complete 0: work 1: reset
SW_RST_CMD	[25]			Software reset for CMD line. Only part of command circuit is reset. The following registers and bits are cleared by this bit: • Present State register ▪ Command Inhibit (CMD) • Normal Interrupt Status register ▪ Command Complete 0: work 1: reset
SW_RST_ALL	[24]			Software reset for all. This reset affects the entire HC except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0. During its initialization, the HD shall set this bit to 1 to reset the HC. The HC shall reset this bit to 0 when Capabilities registers are valid and the HD can read them. Additional use of **Software Reset for All** may not affect the value of the Capabilities registers. If this bit is set to 1, the SD card shall reset itself and must be reinitialized by the HD. 0: work 1: reset
	[23:20]			Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

DATA_TIMEOUT_CNT	[19:16]			Data timeout counter value. This value determines the interval by which DAT line timeouts are detected. Refer to the **Data Timeout Error** in the Error Interrupt Status register for information on factors that dictate timeout generation. Timeout clock frequency will be generated by dividing the base clock TMCLK by this value. When setting this register, prevent inadvertent timeout events by clearing the **Data Timeout Error Status Enable** (in the Error Interrupt Status Enable register). 0000: TMCLK * 2^(13) 0001: TMCLK * 2^(14) … 1110: TMCLK * 2^(27) 1111: reserved
SDCLK_FRQ_SEL	[15:8]			SD clock frequency select. This register is used to select the frequency of the **SDCLK** pin. The frequency is not programmed directly; rather this register holds the divisor of the **Base Clock Frequency for SD clock** in the Capabilities register. Only the following settings are allowed. 0x00: base clock (10~63 MHz) 0x01: base clock divided by 2 0x02: base clock divided by 4 0x04: base clock divided by 8 0x08: base clock divided by 16 0x10: base clock divided by 32 0x20: base clock divided by 64 0x40: base clock divided by 128 0x80: base clock divided by 256 Setting 0x00 specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor, but multiple bits should not be set. The two default divider values can be calculated by the frequency that is defined by the **Base Clock Frequency for SD Clock** in the Capabilities register. 1. 25 MHz divider value 2. 400 kHz divider value The frequency of the SDCLK is set by the following formula: Clock Frequency = (Base clock) / divisor Thus choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency.
	[7:3]			Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SDCLK_EN	[2]			SD clock enable. The HC shall stop **SDCLK** when writing this bit to 0. **SDCLK Frequency Select** can be changed when this bit is 0. Then, the HC shall maintain the same clock frequency until **SDCLK** is stopped (stop at **SDCLK** = 0). If the HC detects the No Card state, this bit shall be cleared. 0: disable 1: enable
INT_CLK_STABLE	[1]			Internal clock stable. This bit is set to 1 when SD clock is stable after writing to **Internal Clock Enable** in this register to 1. The SD Host Driver shall wait to set **SD Clock Enable** until this bit is 1.Note: This is useful when using PLL for a clock oscillator that requires setup time. 0: not ready 1: ready
INT_CLK_EN	[0]			Internal clock enable. This bit is set to 0 when the HD is not using the HC or the HC awaits a wakeup event. The HC should stop its internal clock to go to the very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1. When clock oscillation is stable, the HC shall set **Internal Clock Stable** in this register to 1. This bit shall not affect card detection. 0: stop 1: oscillate

6.10.3.2.13 **INT_ST**

0x0030 **Normal and error interrupt status** **INT_ST**

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	VNDR_ERR_ST			TRGT_RESP_ERR	Reserved			AUTO_CMD12_ERR	CUR_LMT_ERR	DATA_END_BIT_ERR	DATA_CRC_ERR	DATA_TIMEOUT_ER R	CMD_IND_ERR	CMD_END_BIT_ERR	CMD_CRC_ERR	CMD_TIMEOUT_ER R
Type	RW1C			RW1C				RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ERR_INT	Reserved						CARD_INT	CARD_REMOVAL	CARD_INSERTION	BUF_READ_RDY	BUF_WRITE_RDY	DMA_INT	BLK_GAP_EVNT	TR_COMPLETE	CMD_COMPLETE
Type	ROC							ROC	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	**Bit**	**R/W**	**Default**	**Description**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

VNDR_ERR_ST	[31:29]			Vender specified error status. Additional status bits can be defined in this register by the vendor.
TRGT_RESP_ERR	[28]			Target response error status. This occurs when detecting error in m_hresp. 0: no error 1: error
	[27:25]			Reserved
AUTO_CMD12_ERR	[24]			Auto CMD12 error. This occurs when detecting that one of the bits in Auto CMD12 Error Status register has changed from 0 to 1. This bit is set to 1 also when Auto CMD12 is not executed due to the previous command error. 0: no error 1: error
CUR_LMT_ERR	[23]			Current limit error. By setting the **SD Bus Power** bit in the Power Control Register, the HC is requested to supply power for the SD Bus. If the HC supports the Current Limit Function, it can be protected from an illegal card by stopping power supply to the card in which case this bit indicates a failure status. Reading 1 means the HC is not supplying power to SD card due to some failure. Reading 0 means that the HC is supplying power and no error has occurred. This bit shall always set to be 0, if the HC does not support this function. 0: no error 1: power failure
DATA_END_BIT_ERR	[22]			Data end bit error. This occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status. 0: no error 1: error
DATA_CRC_ERR	[21]			Data CRC error. This occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than “010”. 0: no error 1: error
DATA_TIMEOUT_ERR	[20]			Data timeout error. This occurs when detecting one of the following timeout conditions. 1. Busy Timeout for R1b, R5b type 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout 0: no error 1: timeout

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

CMD_IND_ERR	[19]			Command index error. This occurs if a Command Index error occurs in the Command Response. 0: no error 1: error
CMD_END_BIT_ERR	[18]			Command end bit error. This occurs when detecting that the end bit of a command response is 0. 0: no error 1: end bit error generated
CMD_CRC_ERROR	[17]			Command CRC error. Command CRC Error is generated in two cases. 1. If a response is returned and the Command Timeout Error is set to 0, this bit is set to 1 when detecting a CRC error in the command response 2. The HC detects a CMD line conflict by monitoring the CMD line when a command is issued. If the HC drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SDCLK edge, then the HC shall abort the command (stop driving CMD line) and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict. 0: no error 1: CRC error generated
CMD_TIMEOUT_ERR	[16]			Command timeout error. This occurs only if the no response is returned within 64 **SDCLK** cycles from the end bit of the command. If the HC detects a **CMD** line conflict, in which case **Command CRC Error** shall also be set. This bit shall be set without waiting for 64 **SDCLK** cycles because the command will be aborted by the HC. 0: no error 1: timeout
ERR_INT	[15]			Error interrupt. If any of the bits in the Error Interrupt Status Register is set, then this bit is set. Therefore, the HD can test for an error by checking this bit first. 0: no error 1: error
	[14:9]			Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

CARD_INT	[8]			Card interrupt. Writing this bit to 1 does not clear this bit. It is cleared by resetting the SD card interrupt factor. In 1-bit mode, the HC shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the card and the interrupt to the Host system. When this status has been set and the HD needs to start this interrupt service, Card Interrupt Status Enable in the Normal Interrupt Status register shall be set to 0 in order to clear the card interrupt statuses latched in the HC and stop driving the Host System. After completion of the card interrupt service (the reset factor in the SD card and the interrupt signal may not be asserted), set Card Interrupt Status Enable to 1 and start sampling the interrupt signal again. 0: no card interrupt 1: card interrupt generated
	[7:6]			Reserved
BUF_READ_RDY	[5]			Buffer read ready. This status is set if the Buffer Read Enable changes from 0 to 1. 0: not ready to read buffer 1: ready to read buffer
BUF_WRITE_RDY	[4]			Buffer write ready. This status is set if the Buffer Write Enable changes from 0 to 1. 0: not ready to write buffer 1: ready to write buffer
DMA_INT	[3]			DMA interrupt. This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size register. 0: no DMA interrupt 1: DMA interrupt generated
BLK_GAP_EVENT	[2]			Block gap event. If the Stop at Block Gap Request in the Block Gap Control Register is set, this bit is set. Read Transaction: This bit is set at the falling edge of the DAT Line Active Status (when the transaction is stopped at SD Bus timing. The Read Wait must be supported in order to use this function). Write Transaction: This bit is set at the falling edge of Write Transfer Active Status (after getting CRC status at SD Bus timing). 0: no block gap event 1: transaction stopped at block gap

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

TR_COMPLETE	[1]			Transfer complete. This bit is set when a read/write transaction is completed. Read Transaction: This bit is set at the falling edge of Read Transfer Active Status. There are two cases in which the Interrupt is generated. The first is when a data transfer is completed as specified by data length (after the last data has been read to the Host System). The second is when data has stopped at the block gap and completed the data transfer by setting the Stop at Block Gap Request in the Block Gap Control register (after valid data has been read to the Host System). Write Transaction: This bit is set at the falling edge of the DAT Line Active Status. There are two cases in which the Interrupt is generated. The first is when the last data is written to the card as specified by data length and Busy signal is released. The second is when data transfers are stopped at the block gap by setting Stop at Block Gap Request in the Block Gap Control register and data transfers completed (after valid data is written to the SD card and the busy signal is released). Note: Transfer Complete has higher priority than Data Timeout Error. If both bits are set to 1, the data transfer can be considered complete. 0: no data transfer complete 1: data transfer complete
CMD_COMPLETE	[0]			Command complete. This bit is set when getting the end bit of the command response (except auto CMD12). Note: Command Timeout Error has higher priority than Command Complete. If both are set to 1, it can be considered that the response was not received correctly. 0: no command complete 1: command complete

6.10.3.2.14 **INT_ST_EN**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0034 **Normal and error interrupt status enable** **INT_ST_EN**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VNDR_ERR_ST_EN			TRGT_RESP_ERR_EN	Reserved			AUTO_CMD12_ERR_EN	CUR_LMT_ERR_EN	DATA_END_BIT_ERR_EN	DATA_CRC_ERR_EN	DATA_TIMEOUT_ERR_EN	CMD_IND_ERR_EN	CMD_END_BIT_ERR_EN	CMD_CRC_ERR_EN	CMD_TIMEOUT_ERR_EN
Type	R/W			R/W				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Fixed to 0	Reserved						CARD_INT_EN	CARD_REMOVAL_EN	CARD_INSERTION_EN	BUF_READ_RDY_EN	BUF_WRITE_RDY_EN	DMA_INT_EN	BLK_GAP_EVNT_EN	TR_COMPLETE_EN	CMD_COMPLETE_EN
Type	RO							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
VNDR_ERR_ST_EN	[31:29]			Vender specified error status enable 0: masked 1: enabled
TRGT_RESP_ERR_EN	[28]			Target response error status enable 0: masked 1: enabled
	[27:25]			Reserved
AUTO_CMD12_ERR_EN	[24]			Auto CMD12 error status enable 0: masked 1: enabled
CUR_LMT_ERR_EN	[23]			Current limit error status enable 0: masked 1: enabled
DATA_END_BIT_ERR_EN	[22]			Data end bit error status enable 0: masked 1: enabled
DATA_CRC_ERR_EN	[21]			Data CRC error status enable 0: masked 1: enabled
DATA_TIMEOUT_ERR_EN	[20]			Data timeout error status enable 0: masked 1: enabled
CMD_IND_ERR_EN	[19]			Command index error status enable 0: masked 1: enabled

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

CMD_END_BIT_ERR_EN	[18]			Command end bit error status enable 0: masked 1: enabled
CMD_CRC_ERROR_EN	[17]			Command CRC error status enable 0: masked 1: enabled
CMD_TIMEOUT_ERR_EN	[16]			Command timeout error status enable 0: masked 1: enabled
Fixed at 0	[15]			The HC shall control error Interrupts using the Error Interrupt Status Enable register.
	[14:9]			Reserved
CARD_INT_EN	[8]			Card interrupt status enable. If this bit is set to 0, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1. The HD should clear the Card Interrupt Status Enable before servicing the Card Interrupt and should set this bit again after all Interrupt requests from the card are cleared to prevent inadvertent Interrupts. 0: masked 1: enabled
	[7:6]			Reserved
BUF_READ_RDY_EN	[5]			Buffer read ready status enable 0: masked 1: enabled
BUF_WRITE_RDY_EN	[4]			Buffer write ready status enable 0: masked 1: enabled
DMA_INT_EN	[3]			DMA interrupt status enable 0: masked 1: enabled
BLK_GAP_EVENT_EN	[2]			Block gap event status enable 0: masked 1: enabled
TR_COMPLETE_EN	[1]			Transfer complete status enable 0: masked 1: enabled
CMD_COMPLETE_EN	[0]			Command complete status enable 0: masked 1: enabled

6.10.3.2.15 **INT_SIG_EN**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0038 **Normal and error interrupt signal enable** **INT_SIG_EN**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VNDR_ERR_ST_EN			TRGT_RESP_ERR_EN	Reserved			AUTO_CMD12_ERR_EN	CUR_LMT_ERR_EN	DATA_END_BIT_ERR_EN	DATA_CRC_ERR_EN	DATA_TIMEOUT_ERR_EN	CMD_IND_ERR_EN	CMD_END_BIT_ERR_EN	CMD_CRC_ERR_EN	CMD_TIMEOUT_ERR_EN
Type	R/W			R/W				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Fixed to 0	Reserved						CARD_INT_EN	CARD_REMOVAL_EN	CARD_INSERTION_EN	BUF_READ_RDY_EN	BUF_WRITE_RDY_EN	DMA_INT_EN	BLK_GAP_EVNT_EN	TR_COMPLETE_EN	CMD_COMPLETE_EN
Type	RO							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
VNDR_ERR_ST_EN	[31:29]			Vender specified error signal enable 0: masked 1: enabled
TRGT_RESP_ERR_EN	[28]			Target response error signal enable 0: masked 1: enabled
	[27:25]			Reserved
AUTO_CMD12_ERR_EN	[24]			Auto CMD12 error signal enable 0: masked 1: enabled
CUR_LMT_ERR_EN	[23]			Current limit error signal enable 0: masked 1: enabled
DATA_END_BIT_ERR_EN	[22]			Data end bit error signal enable 0: masked 1: enabled
DATA_CRC_ERR_EN	[21]			Data CRC error signal enable 0: masked 1: enabled
DATA_TIMEOUT_ERR_EN	[20]			Data timeout error signal enable 0: masked 1: enabled
CMD_IND_ERR_EN	[19]			Command index error signal enable 0: masked 1: enabled

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

CMD_END_BIT_ERR_EN	[18]			Command end bit error signal enable 0: masked 1: enabled
CMD_CRC_ERROR_EN	[17]			Command CRC error signal enable 0: masked 1: enabled
CMD_TIMEOUT_ERR_EN	[16]			Command timeout error signal enable 0: masked 1: enabled
Fixed at 0	[15]			The HD shall control error Interrupts using the Error Interrupt Signal Enable register.
	[14:9]			Reserved
CARD_INT_EN	[8]			Card interrupt signal enable 0: masked 1: enabled
	[7:6]			Reserved
BUF_READ_RDY_EN	[5]			Buffer read ready signal enable 0: masked 1: enabled
BUF_WRITE_RDY_EN	[4]			Buffer write ready signal enable 0: masked 1: enabled
DMA_INT_EN	[3]			DMA interrupt signal enable 0: masked 1: enabled
BLK_GAP_EVENT_EN	[2]			Block gap event signal enable 0: masked 1: enabled
TR_COMPLETE_EN	[1]			Transfer complete signal enable 0: masked 1: enabled
CMD_COMPLETE_EN	[0]			Command complete signal enable 0: masked 1: enabled

6.10.3.2.16 **CMD12_ST**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x003C **Auto CMD12 error status** **CMD12_ST**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								CMD_NOT_ERR	Reserved		IND_ERR	END_BIT_ERR	CRC_ERR	TIMEOUT_ERR	
Type									ROC			ROC	ROC	ROC	ROC	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:8]			Reserved
CMD_NOT_ERR	[7]			Command not issued error. Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 error ([4:1]) in this register. 0: no error 1: not issued
	[6:5]			Reserved
IND_ERR	[4]			Auto CMD12 index error. This occurs if the Command Index error occurs in response to a command. 0: no error 1: error
END_BIT_ERR	[3]			Auto CMD12 end bit error. This occurs when detecting that the end bit of command response is 0. 0: no error 1: end bit error generated
CRC_ERR	[2]			Auto CMD12 CRC error. This occurs when detecting a CRC error in the command response. 0: no error 1: CRC error generated
TIMEOUT_ERR	[1]			Auto CMD12 timeout error. This occurs if the no response is returned within 64 **SDCLK** cycles from the end bit of the command. If this bit is set to 1, the other error status bits ([4:2]) are meaningless. 0: no error 1: timeout
	[0]			Reserved

6.10.3.2.17 **CAP1**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0040 **Capabilities 1** **CAP1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved					V18	V30	V33	SUSP_RES	DMA	HIGH_SPEED	Reserved			MAX_BLK_SIZE	
Type						HWinit	HWinit	HWinit	HWinit	HWinit	HWinit				HWinit	HWinit
Reset	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		BASE_CLK_FRQ						TIMEOUT_CLK_UNIT	Reserved	TIMEOUT_CLK_FRQ					
Type			HWinit						HWinit		HWinit					
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:27]			Reserved
V18	[26]			Voltage support 1.8 V. 0: 1.8 V not supported 1: 1.8 V supported
V30	[25]			Voltage support 3.0 V. 0: 3.0 V not supported 1: 3.0 V supported
V33	[24]			Voltage support 3.3 V. 0: 3.3 V not supported 1: 3.3 V supported
SUSP_RES	[23]			Suspend/resume support. This bit indicates whether the HC supports Suspend/Resume function. If this bit is 0, the Suspend and Resume mechanism is not supported and the HD shall not issue either Suspend/Resume command. 0: not supported 1: supported
DMA	[22]			DMA support. This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly. 0: DMA not supported 1: DMA supported
HIGH_SPEED	[21]			High speed support. This bit indicates whether the HC and the Host System support High Speed mode and they can supply SD Clock frequency from 25 MHz to 50 MHz. 0: high speed not supported 1: high speed supported
	[20:18]			Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

MAX_BLK_SIZE	[17:16]			This value indicates the maximum block size that the HD can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. 00: 512 bytes 01: 1024 bytes 10: 2048 bytes 11: 4096 bytes
	[15:14]			Reserved
BASE_CLK_FRQ	[13:8]			This value indicates the base (maximum) clock frequency for the SD clock. The unit is MHz. If the real frequency is 16.5 MHz, a larger value shall be set, i.e., 010001b (17 MHz) because the HD uses this value to calculate the clock divider value and it shall not exceed the upper limit of the SD clock frequency. The supported range is 10 to 63 MHz. If these bits are all 0, the Host System has to get information via another method. 0: get information via another method (Registry Entry) 1: 1 MHz 2: 2 MHz … 63: 63 MHz
TIMEOUT_CLK_UNIT	[7]			This bit shows the unit of base clock frequency used to detect Data Timeout Error. 0: kHz 1: MHz
	[6]			Reserved
TIMEOUT_CLK_FRQ	[5:0]			This bit shows the base clock frequency used to detect Data Timeout Error. 0: get information via another method 1: 1 MHz 2: 2 MHz … 63: 63 MHz

6.10.3.2.18 **CAP2**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0044 **Capabilities 2 (reserved)** **CAP2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																
Type																
Reset																

Field Name	Bit	R/W	Default	Description
	[31:0]			Reserved.

6.10.3.2.19 **MAX_CUR_CAP1**

0x0048 **Maximum current capabilities 1** **MAX_CUR_CAP1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved								MAX_CUR_V18							
Type									HWinit							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MAX_CUR_V30								MAX_CUR_V33							
Type	HWinit								HWinit							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
	[31:24]			Reserved
MAX_CUR_V18	[23:16]			Maximum current for 1.8 V. 0: get information via another method
MAX_CUR_V30	[15:8]			Maximum current for 3.0 V. 0: get information via another method
MAX_CUR_V33	[7:0]			Maximum current for 3.3 V. 0: get information via another method

6.10.3.2.20 **MAX_CUR_CAP2**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x004C **Maximum current capabilities 2 (reserved)** **MAX_CUR_CAP2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name																
Type																
Reset																

Field Name	Bit	R/W	Default	Description
	[31:0]			Reserved.

6.10.3.2.21 **SLT_INT_ST**

0x00FC **Slot interrupt status and version number** **SLT_INT_ST**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VNDR_VER_NO								SPEC_VER_NO							
Type	HWinit								HWinit							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								SLT_INT							
Type									ROC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default	Description
VNDR_VER_NO	[31:24]			This status is reserved for the vendor version number. The HD should not use this status.
SPEC_VER_NO	[23:16]			This status indicates the Host Controller Spec Version. The upper and lower 4 bits indicate the version. 0: SD Host Specification version 1.0 Others: reserved
	[15:8]			Reserved
SLT_INT	[7:0]			These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot. A maximum of 8 slots can be defined. If one interrupt signal is associated with multiple slots, the HD can know which interrupt is generated by reading these status bits. By a power-on reset or by Software Reset for All, the Interrupt signal shall be deasserted and this status shall read 0. [0]: slot 1 [1]: slot 2

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

7 BlueTooth

7.1 BT_TOP

7.1.1 Overview

BT_TOP is the blue tooth sub system which has one independent ARM Cortex-M4.

7.1.2 Features

- Independent ARM CortexM4 core
- 4+4 KB (8+4/8+8)code/data cache memory for ARM CM4
- 32KB+4KB+4KB IRAM shared between ARM CortexM4 and ARM9, total 40K Bytes
- Bypassable Async AHB bridge to support this sub system can work under same or different clock which clk_ahb in ARM9 side.
- 1KB dual port share memory to support the high speed data exchange between the CortexM4 and AMR9 system
- UART0 is dedicated for Blue tooth data/information exchange between Cortex M4 and ARM9 system
- UART1 is the peripheral device mainly for Blue tooth log output.
- CortexM4 boots from iram or external-memory with remap signal control.

7.1.3 Signal Description

The signals directly connect to IO PAD are as the follows:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

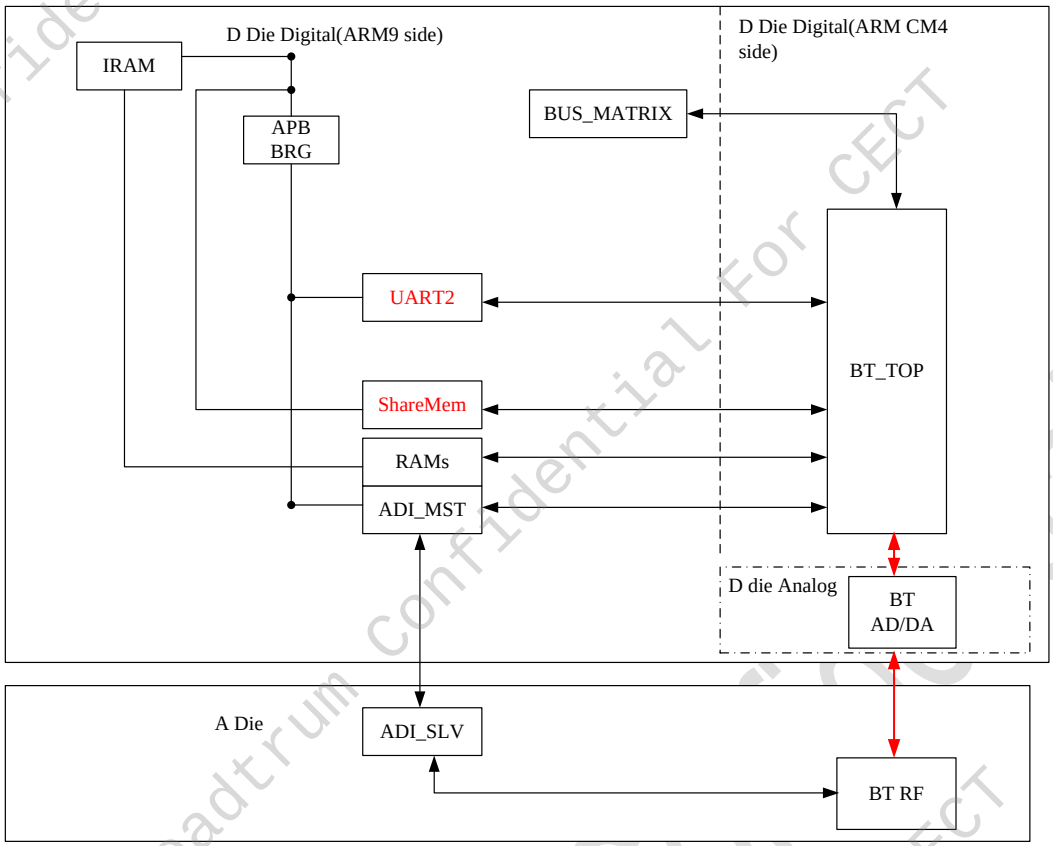


Figure 7.1-1 BT_TOP connection

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

7.1.4 Function Description

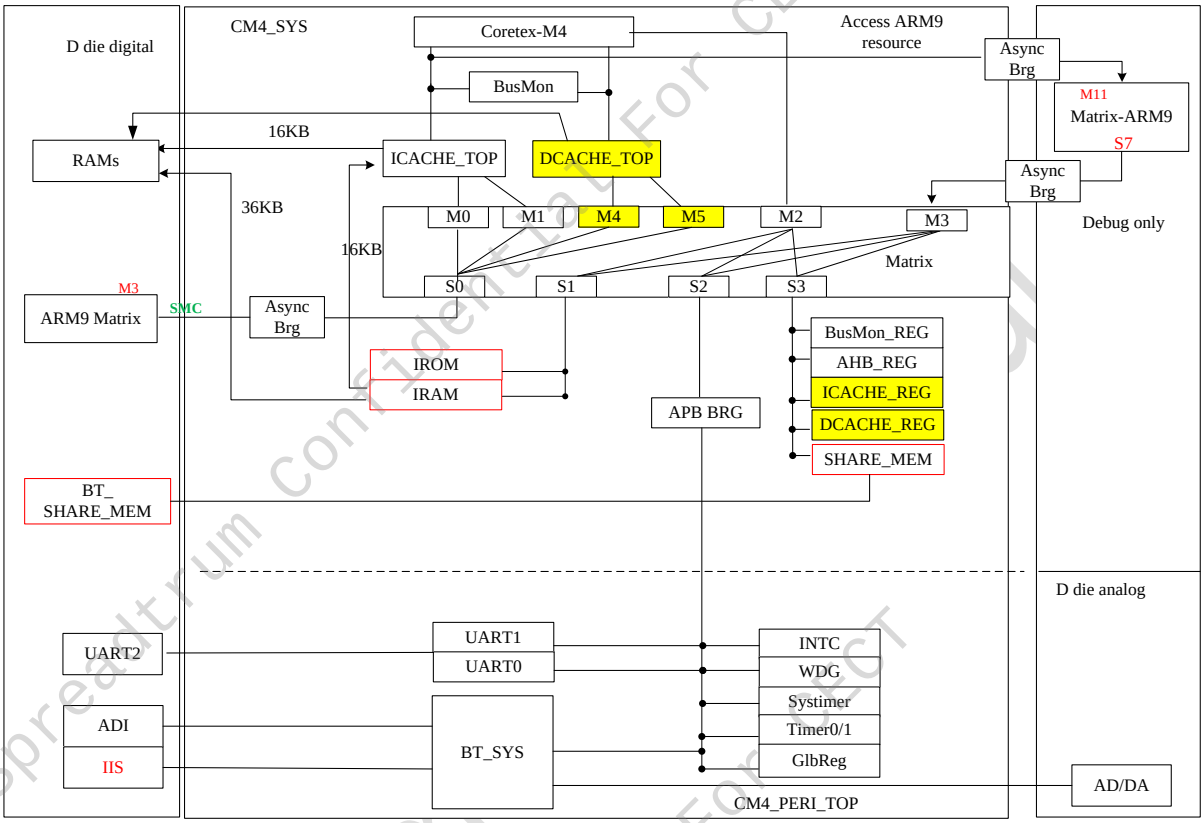


Figure 7.1-2 BT_TOP system diagram

Table 7.1-1 Module Signal Interface

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

7.1.5 Memory Map

7.1.5.1 BT MCU AHB Memory map

Address Range	Sector	Description
0x0000_0000 – 0x0FFF_FFFF	On-chip RAM space	ARM7_boot_sel = 1: 0x0000_0000 – 0x0000_57FF: 22k bytes, shared with ARM9; ARM9 control by default; 0x0000_5800 – 0x0000_58FF: 256 byte, shared with Dcache tag mem0 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_5900 – 0x0000_59FF: 256 byte, shared with Dcache tag mem1 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_5a00 – 0x0000_5aFF: 256 byte, shared with Dcache tag mem2 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_5b00 – 0x0000_5bFF: 256 byte, shared with Dcache tag mem3 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_5c00 – 0x0000_6bFF: 4K byte, shared with Dcache data mem & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_6c00 – 0x0000_6cFF: 256 byte, shared with Icache tag mem0 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_6d00 – 0x0000_6dFF: 256 byte, shared with Icache tag mem1 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_6e00 – 0x0000_6eFF: 256 byte, shared with Icache tag mem2 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

		0x0000_6f00 – 0x0000_6fFF: 256 byte, shared with Icache tag mem3 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_7000 – 0x0000_8000: 4K byte, shared with Icache data mem & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_8000 – 0x0000_9000: 4k byte, shared with ARM9; ARM9 control by default; If cache enable, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x0000_9000 – 0x0000_a000: 4k byte, shared with ARM9. ARM9 control by default; If cache enable, this 4k byte couldn't be accessed by ARM7 or ARM9. ARM7_boot_sel = 0: external memory space 0x0000_0000~0x0FFF_FFFF
0x1000_0000 – 0x1EFF_FFFF	External memory space	ARM7_boot_sel = 1: external memory space 0x1000_0000~0x1FFF_FFFF ARM7_boot_sel = 0: 0x1000_0000 – 0x1000_57FF: 22k bytes, shared with ARM9; ARM9 control by default; 0x1000_5800 – 0x1000_58FF: 256 byte, shared with Dcache tag mem0 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_5900 – 0x1000_59FF: 256 byte, shared with Dcache tag mem1 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_5a00 – 0x1000_5aFF: 256 byte, shared with Dcache tag mem2 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_5b00 – 0x1000_5bFF: 256 byte, shared with Dcache tag mem3 & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_5c00 – 0x1000_6bFF:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

		4K byte, shared with Dcache data mem & arm9 ARM9 control by default; If cache enable and select 8k Dcache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_6c00 – 0x1000_6cFF: 256 byte, shared with Icache tag mem0 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_6d00 – 0x1000_6dFF: 256 byte, shared with Icache tag mem1 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_6e00 – 0x1000_6eFF: 256 byte, shared with Icache tag mem2 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_6f00 – 0x1000_6fFF: 256 byte, shared with Icache tag mem3 & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_7000 – 0x1000_8000: 4K byte, shared with Icache data mem & arm9 ARM9 control by default; If cache enable and select 8k Icache size, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_8000 – 0x1000_9000: 4k byte, shared with ARM9; ARM9 control by default; If cache enable, this 4k byte couldn't be accessed by ARM7 or ARM9. 0x1000_9000 – 0x1000_a000: 4k byte, shared with ARM9. ARM9 control by default; If cache enable, this 4k byte couldn't be accessed by ARM7 or ARM9.
0x1F00_0000 – 0x1FFF_FFFF	On-chip ROM space	On-chip ROM space: 0x1F00_0000 – 0x1F00_7FFF(32KB)
0x5000_0000 – 0x500F_FFFF	Share memory	Share memory with ARM9, 1K bytes
0x5010_0000 – 0x501F_FFFF		Reserved
0x5020_0000 – 0x503F_FFFF		Reserved
0x5040_0000 – 0x5040_0FFF	Bus monitor0 space	
0x5040_1000 –		Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x5040_1FFF		
0x5040_2000 – 0x504F_FFFF		Reserved
0x5050_0000 – 0x505F_FFFF	General AHB control registers	
0x5060_0000 – 0x506F_FFFF	Cache registers	
0x5200_0000 – 0x52FF_FFFF	Peripherals space(BT Sys, uart0/1,INTC,APB Reg, Timer,EIC)	
0x5300_0000 – 0x53FF_FFFF:		Only can be accessed by ARM9
Others	The same as ARM9 memory map	

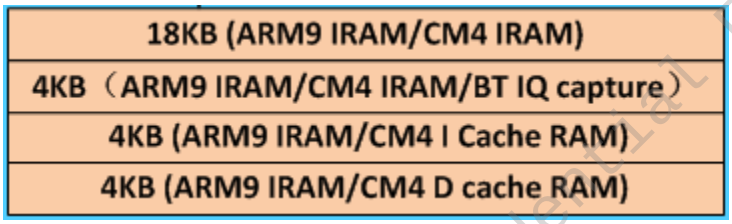
7.1.5.2 BT MCU APB Memory Map

Address Range	Sector	Description
0x5200_0000 – 0x5200_FFFF	Interrupt controller	
0x5210_0000 – 0x5210_0FFF	General-purpose timers	
0x5210_1000 – 0x5210_1FFF	Backup General-purpose timers	
0x5210_3000 – 0x5210_3FFF	System timers	
0x5220_0000 – 0x5220_FFFF	ARM7 accesses ADI Master	
0x5230_0000 – 0x5230_FFFF	UART0	
0x5240_0000 – 0x5240_FFFF	UART1	Reserved
0x5250_0000 – 0x525F_FFFF	BT_TOP	Blue tooth sub system
0x5260_0000 – 0x5260_FFFF	EIC	
0x5270_0000 – 0x5270_FFFF	Global control registers	
0x5280_0000 – 0x528F_FFFF		Reserved
0x5290_0000 – 0x529F_FFFF	Watch dog	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x52A0_0000 – 0x52FF_FFFF		Reserved

7.1.5.3 CortexCM4 shared irams with ARM9 diagram



1 All BT shared iram can be controlled by ARM CortexCM4 or ARM9；

2 ARM9 can access all CM4 iram when cache disable；

3 ARM9 uses the total 18+4+4+4 KB switch ram in default;

4 When ARM9 give up the control of switch ram, CM4 can access them. When cache disabled, 18+4+4+4KB switch ram can be used. When 4KB I cache & 4KB D cache used, 18+4KB switch ram can be used by CM4.

5 When BT IQ capture uses 4KB switch ram, CM4 can only use 18KB (cache enabled).

6 priority: CM4 cache enable > ARM9>BT IQ capture>CM4

7.1.5.4 Register Descriptions

7.1.5.4.1 AHB_REG

Refrer to *shsvn03/svn/CHIP/interface/SC6531/autoreg/CM4_AHB_reg.xls* excel

7.1.5.4.2 GLB_REG

Refrer to *shsvn03/svn/CHIP/interface/SC6531/autoreg/CM4_GLB_reg.xls* excel

7.1.6 Boot

7.1.6.1 Boot from shared iram

SYSTEM keeps ARM CortexM4 at reset status when ARM9 boots;

ARMM4_boot_sel is ‘1’ at default.

ARM9 loads ARM CortexM4 boot code in share irams with CortexM4, and share irams controlled by ARM9 at default.

ARM9 enables CortexM4 clock and releases the control of shares irams and the reset of CortexM4, then CortexM4 begins boots.

7.1.6.2 Boot from EMC or SFC

SYSTEM keeps CortexM4 at reset status when ARM9 boots;

ARMM4_boot_sel is ‘1’ at default.

ARM9 loads CortexM4 boot code in EMC or SFC with address offset and space remap control.

ARM9 sets the ARM4_boot_sel is ‘0’, enables CortexM4 clock and releases the reset of CortexM4, then CortexM4 boots.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

7.1.7 Core Low Power

7.1.7.1 Enter Sleep

CM4 core can jump into sleep by one of thress ways:

- Wait for interrupt
- Wait for event
- Sleep-on-exit

The wait for interrupt instruction,WFI,cause immediate entry to sleep mode unless the wake-up condition is true. When cm4 core excute a WFI instruction it stops excuting instructions and enters sleep mode.

The wait for event instruction,WFE,cause entry to sleep mode depending on the value of a one-bit event register. When the processor excutes a WFE instruction, it check the value of the event register:

Value	meaning
0	Cm4 core stops excuting instructions and enter sleep mode
1	Cm4 core clears the register to 0 and continue excuting instructions without enter sleep mode

If the event register is 1, this indicate that the cm4 core must not enter sleep mode on execution of a WFE instruction.Typically,this is because an external event signal is asserted or a processor in the system has excuted an SEV instruction(In SC6531,arm9 will not excute SEV instruction). Software cannot access this register directly.

If the SLEEPONEXIT bit of the SCR is set to 1,when the processor completes the execution of all exception handlers it return to Thread mdoe and immediately enter sleep mode.Use this mechanism in applications that only require the cm4 to run when an exception occurs.

7.1.7.2 Wakeup from sleep

Normally, the core wake up only when it detects an exception with sufficient priority to cause exception entry.When cm4 core entry sleep by wfe instruction,it have two more ways to wakeup.In NemeG, we only use exception to wake up core. Refer to cm4 core user guider for details.

System Control register

Addr:0xE000_ED10

31 ... 5	4	3	2	1	0
	sevonpend	reserved	sleepdeep	sleeponexit	reserved

Bit[2] control core use sleep or deep sleep as its low power mode, 0 mean sleep ,otherwise mean

deepsleep.

7.1.7.3 Wakeup from deepsleep

When core wakeup from deepsleep, it follow power-up flow, PMU can wakeup cm4 subsys.

7.1.8 Interrupt Source Assignment

BT system have two interruption source controller. One is core inside(Nested Vector Interrption Controller , nvic),the other is intc_top controller. Cm4 core can configure nvic registers to control these interruptions;also, software can configure intc_top register to control these interruptions. And, IRQ/FIQ comes from INTC_TOP,if not masked,each intc_top source can generate irq/fiq.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

The Table3-13 shows the detailed channel assignment for both IRQ and FIQ.It have 32 interrupt channel. The Figure3 show structure of interruption source.

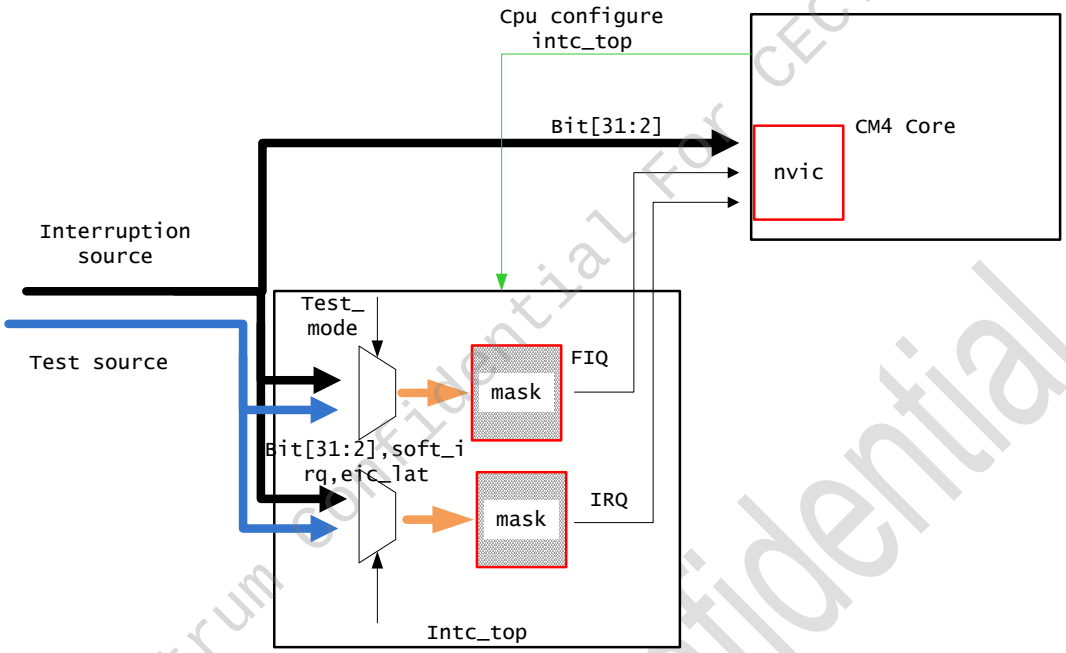


Figure 3 interruption source structure

Table 7-2 Interrupt Source Map

Channel Number	CORE SOURCE	INTC_TOP SOURCE
0	IRQ	1'b0
1	FIQ	1'b1
2	bt_masked_tim_intr[0]	bt_masked_tim_intr[0]
3	1'b0	1'b0
4	tmr0_irq	tmr0_irq or tmrb0_irq
5	tmr1_irq	tmr1_irq or tmrb1_irq
6	tmr2_irq	tmr2_irq or tmrb2_irq
7	syst_irq	syst_irq
8	arm9_to_cm4_irq1 | arm9_to_cm4_irq1_set	arm9_to_cm4_irq1 | arm9_to_cm4_irq1_set
9	arm9_to_cm4_irq0 | arm9_to_cm4_irq0_set	arm9_to_cm4_irq0 | arm9_to_cm4_irq0_set
10	bt_masked_tim_intr[1]	bt_masked_tim_intr[1]
11	dcache_irq	dcache_irq
12	ARM9 global register interruption: arm9_irq or arm9_irq_pls	ARM9 global register interruption: arm9_irq or arm9_irq_pls
13	bus monitor0	bus monitor0

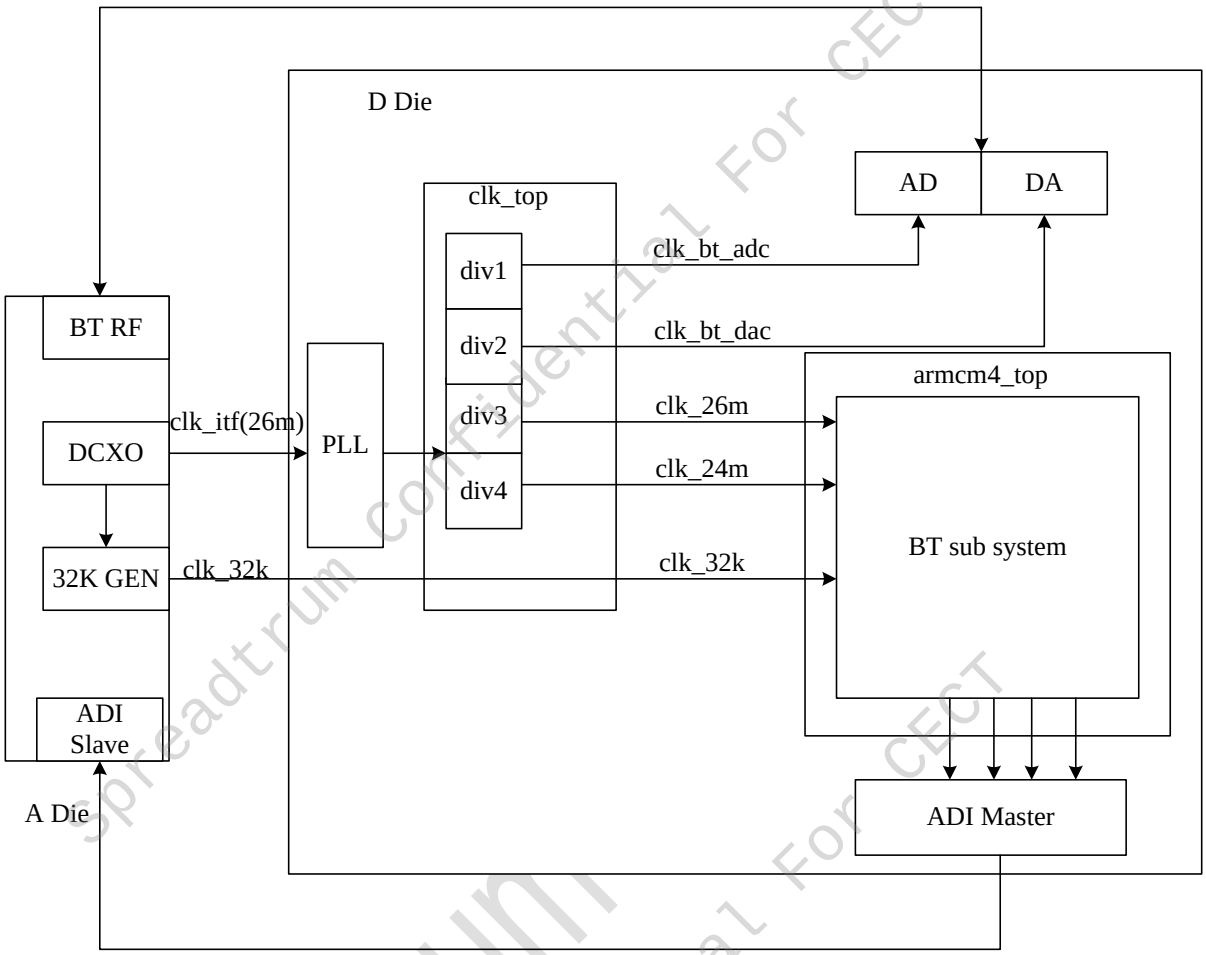
This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

14	uart1_irq	uart1_irq
15	wdg_irq	wdg_irq
16	icache irq	icache irq
17	eic async/sync/dbnc irq	eic async/sync/dbnc irq
18	combinational ARM9 all irqs/fiq	combinational ARM9 all irqs/frqs
19	rf_master_int	rf_master_int
20	bt_modem_intr	bt_modem_intr
21	bt_masked_page_timeout_intr	bt_masked_page_timeout_intr
22	bt_masked_sync_det_intr	bt_masked_sync_det_intr
23	bt_masked_pkd_rx_hdr	bt_masked_pkd_rx_hdr
24	bt_masked_tim_intr[2]	bt_masked_tim_intr[2]
25	bt_masked_pkd_intr	bt_masked_pkd_intr
26	bt_masked_pka_intr	bt_masked_pka_intr
27	bt_masked_aux_tmr_intr	bt_masked_aux_tmr_intr
28	gpio_irq	gpio_irq
29	1'b0	1'b0
30	1'b0	1'b0
31	bt_masked_tim_intr[3]	bt_masked_tim_intr[3]

7.2 Pending Issues

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

7.2.1 Clock



Note:

1. the clk_32k is the standard 32.768k
2. Clk_26m/clk_24m/clk_bt_dac/clk_bt_adc share the same PLL source for clock jitter consideration
3. BT sub system has it's local clock generator

7.2.2 Reset

1. Power reset and software reset
2. BT sub system has it's local reset generator

7.2.3 AD/DA Interface

The DAC has the dedicated calibration logic, which is inside the ARMCM4_TOP.

1. There is one analog switcher shared by AD/DA to support the bi-directional analog I/Q transferring.
2. BT sub-system should provide the direction control signal for AD/DA analog switcher.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

7.2.4 DCXO Calibration

1. GSM DSP should provide one flag to indicate that the DCXO is calibrated by GSM DSP.
2. If GSM DSP is not working, BT should do the DCXO calibration itself.

7.2.5 ADI Master

1. The max time delay for one ADI request is 16us (ADI clock is 79MHz)
2. All the BT RF control information is transferred by this interface.
3. The ADI Master must guarantee the transmission order.
4. Another SW ADI request channel should be added.

7.2.6 Low Power

ARCortexM4 BT SW should enable the “master sleep enable” to ARM9 system to make the whole chip can goes into “deep sleep” state

During chip deep sleep state, ARMCortexM4 system is powered and just clock gating.

ARMCortexM4 wakes up the ARM9 by interrupt.

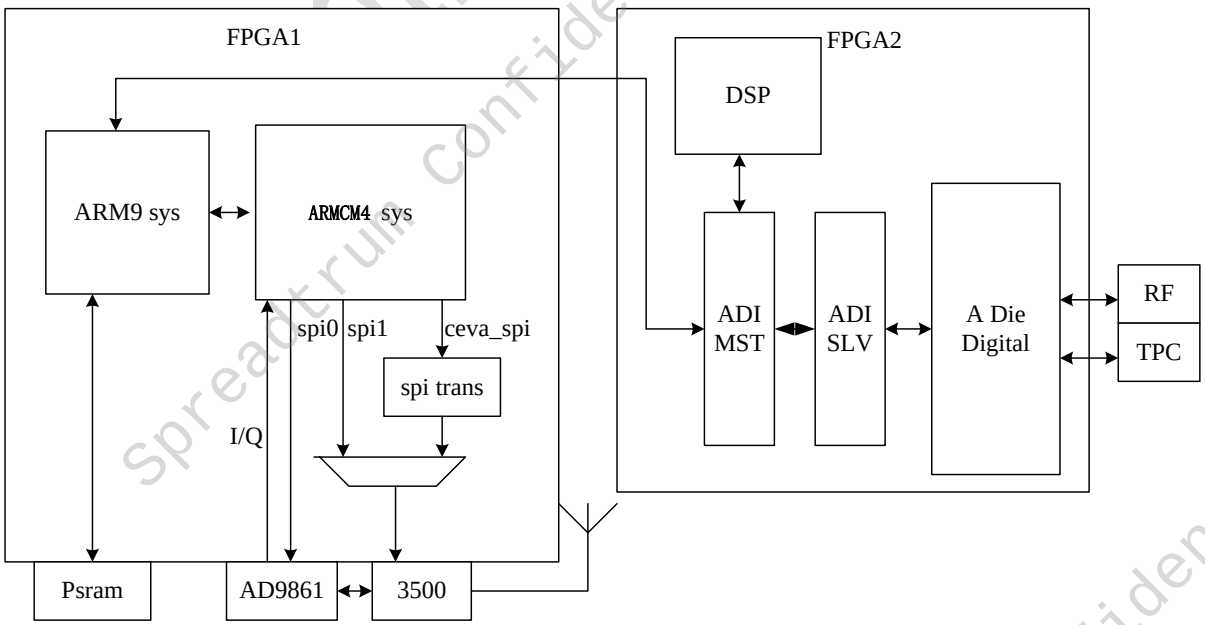
1. When the BT system is sleep, the PLL can be power down, Or the PLL should always be power on to generate the 26M/24M clock even chip is in deep sleep state.
2. When the BT system is sleep, only 32k clock is active.
3. Some RAM/ROM maybe should be shut down to save power during BT system is sleep.

7.2.7 BT Debug Mode

The whole chip (ARM9/CortexM4) system is in active mode, some internal signals are tied to the external PADs for monitor/control purpose.

1. Maybe PADs limited.

7.2.8 FPGA Test



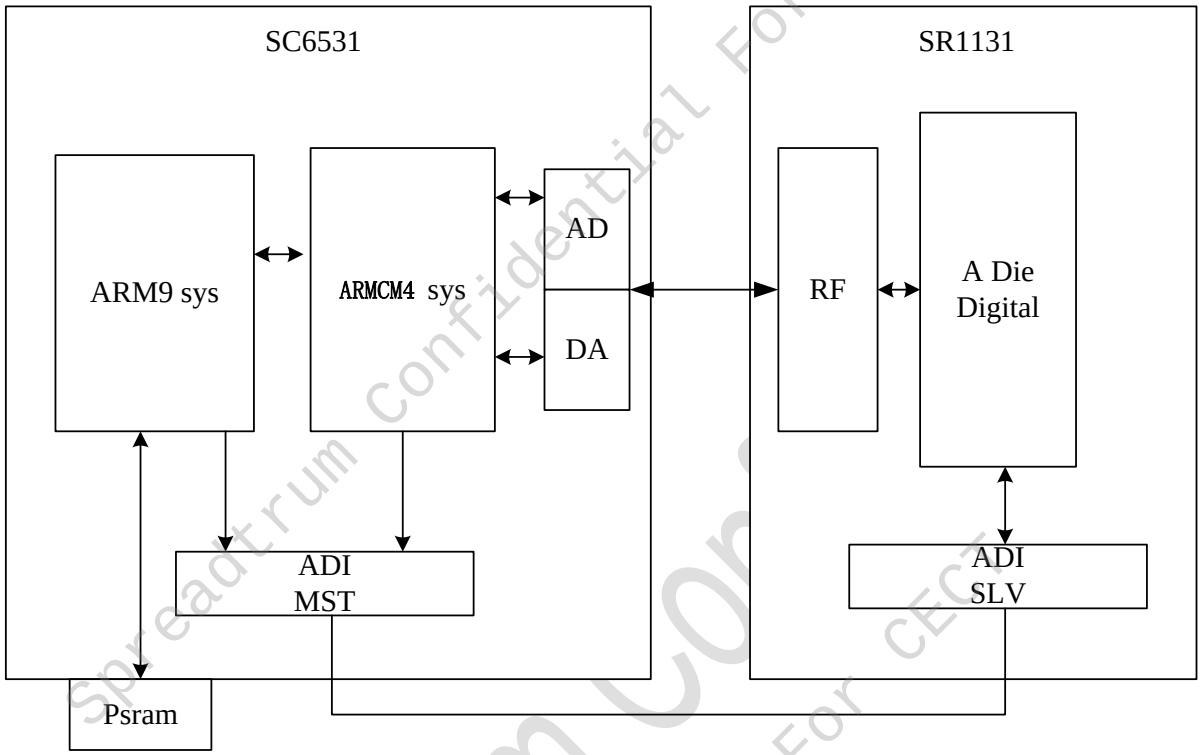
This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

1. FPGA can't touch all the real RF control, EDA simulation should guarantee these data path.

The purpose of FPGA test is just to debug the co-operation of ARMCortexM4 /ARM9.

7.2.9 EDA Simulation

The EDA simulation should touch the fully data path.



7.3 General Purpose Timer

7.3.1 Overview

The module includes three general-purpose asynchronous timers.

7.3.2 Features

- 32-bit decreasing counter
- Support one-time mode and period mode
- Support configurable counting value
- Can be used as wakeup source during deep sleep
- Support single read : no need to double read when reading counter value
- Support multiple load : no need to check busy bit before load tmr
- Support read counter value immediately after loading tmr: once tmr is loaded, the counter value is updated immediately

7.3.3 Signal Description

Null

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

7.3.4 Function Description

tmrfull_top provides three general-purpose timers. Timer 0/1/2's frequency is independent; generally it is 32.768KHz RTC clock, or other clock such as 26MHz. The frequency determines its frequency, if it's 32.768KHz, the precision is 30.5us. If is 26MHz, the precision is 38.461ns. These three timers can be controlled independently.

7.3.4.1 Each asynchronous Timers

Each timer has a 32-bit decreasing counter. This kind of timer provides two operating modes: one-time mode and period mode.

If the timer is configured in one-time mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued. This interrupt is hold until software clears it by writing corresponding clear bit. The counter also stays at 0 until software load it again.

If the timer is configured in period mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued. Then counter goes back to setting value again, and continues to decrease from setting value. The interrupt will hold until software clears it by writing corresponding clear bit.

If trigging clock is RTC clock, these two timers can be used to wake up system during deep sleep.

For RTC clock triggered timer, since the frequency of clk_rtc is much slower than that of PCLK, there are three issues in the r1p0 version of timer, the solution also list here:

Double read to read counter value: in r1p0, counter value belongs to clk_rtc domain, but it connect to PCLK directly, so when read the counter value, metastable state may occur, and the read result is wrong. In r1p0, double read is utilized to solve the problem. It read the counter value for two times(double read), if the two result is same, no metastable state is occurred, if they are different, metastable may be occurred so software should discard the read result and double read again until the results is same. So we can see that double read solve the problem of metastable at the cost of increasing software complexity.

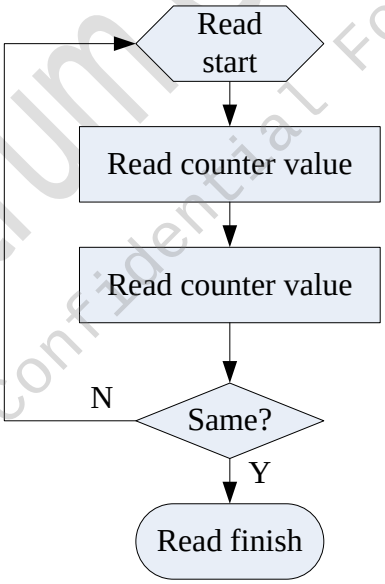


Figure 7-4 Double read flow

Solution to double read: In r2p0, a 32bit counter named tmr_cnt_shdw is used to solve this problem. It is in PCLK domain and once the tmr_cnt_value (clk_rtc) changes; it will also follow the change. Just as its name, it is the shadow of tmr_cnt_value which reflect the tmr_cnt_value accurately. Since it is in PCLK, metastable state can be avoided. In the case of deep sleep. PCLK is closed, tmr_cnt_shdw also stop following. Once PCLK is open, it quickly updates its value in 3 PCLK cycle. Figure 5-73 is the diagram of this solution, Figure 5-74 is the waveform of the updating process. Figure 5-75 illustrates the updating process when PCLK is closed.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

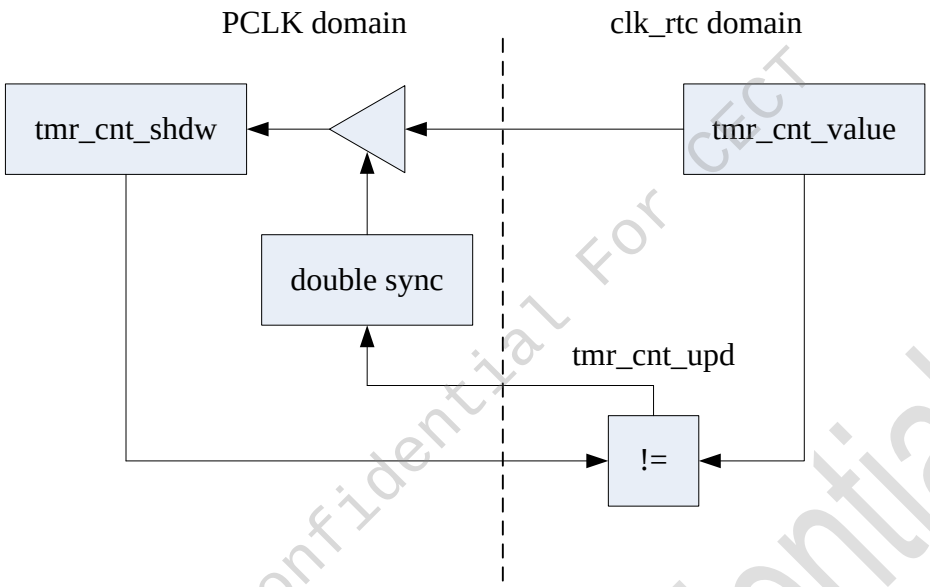
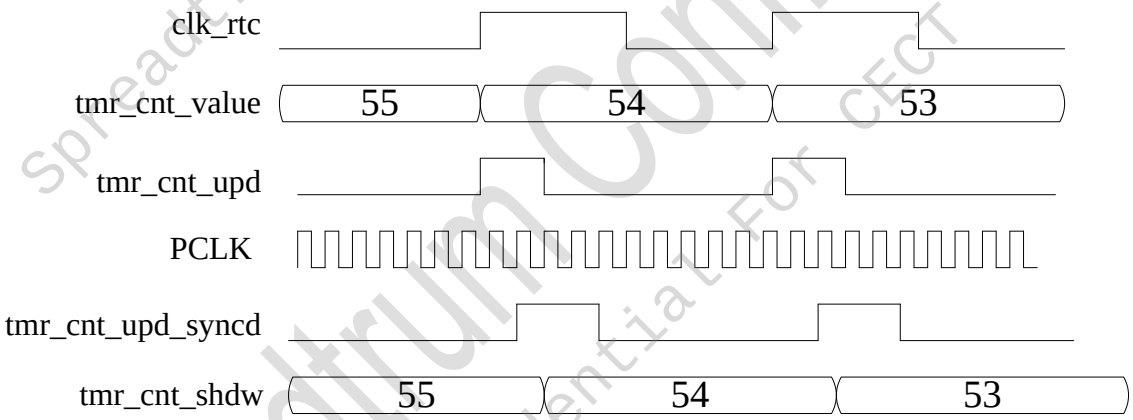


Figure 7-5 Principle of tmr_cnt_shdw



Requirement:
tmr_cnt_value should be stable before the first load(**Synthesis at 26M**)

Figure 7-6 waveform of tmr_cnt_shdw (PCLK open)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

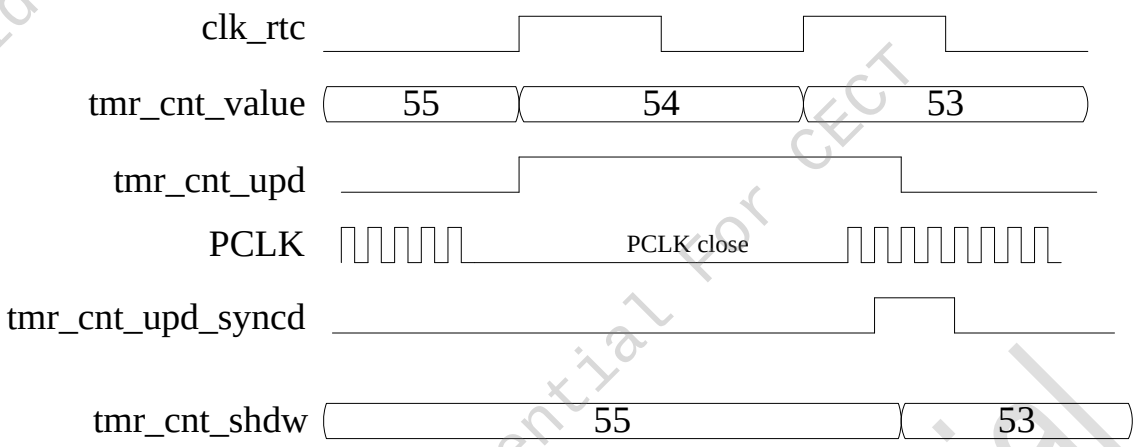


Figure 7-7 waveform of tmr_cnt_shdw (PCLK close)

Check busy bit before any load: in r1p0, one bit signal tmr_ld_reg is used to record the load operation. When there is a load, tmr_ld_reg will toggle (0->1 or 1->0) which indicate a new load is taken place. However, tmr_ld_reg should hold this value until the load value is successfully loaded into counter which belongs to clk_rtc. If not, tmr_ld_reg will toggle back to original status which forms a narrow pulse that cannot be sampled by clk_rtc. That is to say, clk_rtc will not know a new load is happen. To avoid this problem, a busy bit named tmr_ld_busy is provided to indicate that timer is now busy with loading; further loading should not happen in this period. So this method confines the software by not allowing loading when tmr_ld_busy is 1. Figure 5-76 demonstrates that when tmr_ld_busy is 1, no load is permitted.

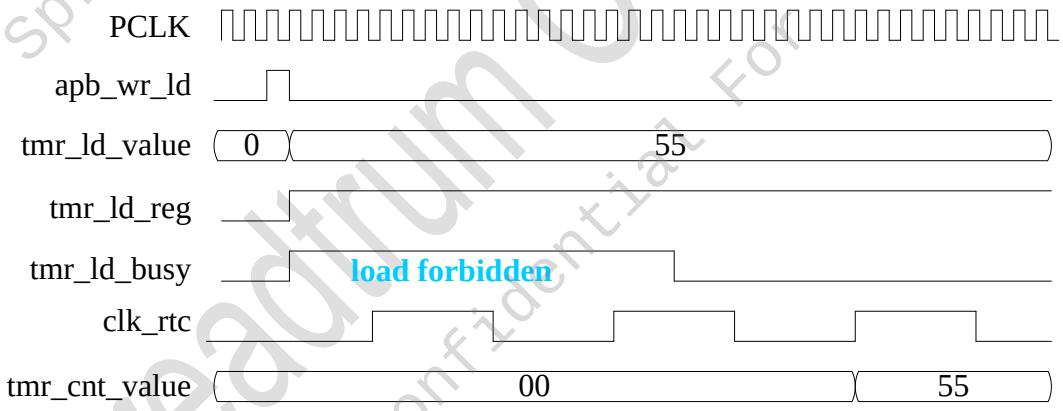


Figure 7-8 Check busy bit

Solution to check busy bit: In r1p0, 1-bit signal tmr_ld_reg is used to record the load status, if multiple load occurs in a short time, it may miss the status. Therefore, a 8-bit signal tmr_ld_idx in PCLK domain is used here to solve the problem. Whenever software write the tmr_ld_value, tmr_ld_idx increase 1 to indicate that a new load is taken place. In clk_rtc domain, there is also 8-bit signal named tmr_ld_idx_shdw_rtc, which is the shadow of tmr_ld_idx in clk_rtc domain. When a new load happen, tmr_ld_idx and tmr_ld_idx_shdw are different, then tmr_ld_idx_shdw and tmr_cnt_value will update at the same time. Figure 5-77 is the circuit diagram, Figure 5-78 is the waveform of single load, from which we can see that maximum delay between tmr_ld_value and tmr_cnt_value is 5 clk_rtc delays. Figure 5-77 is the waveform of multiple loads, notice that we no longer check tmr_ld_busy, instead, we have multiple loads in a short time and the last load value (77) is loaded.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

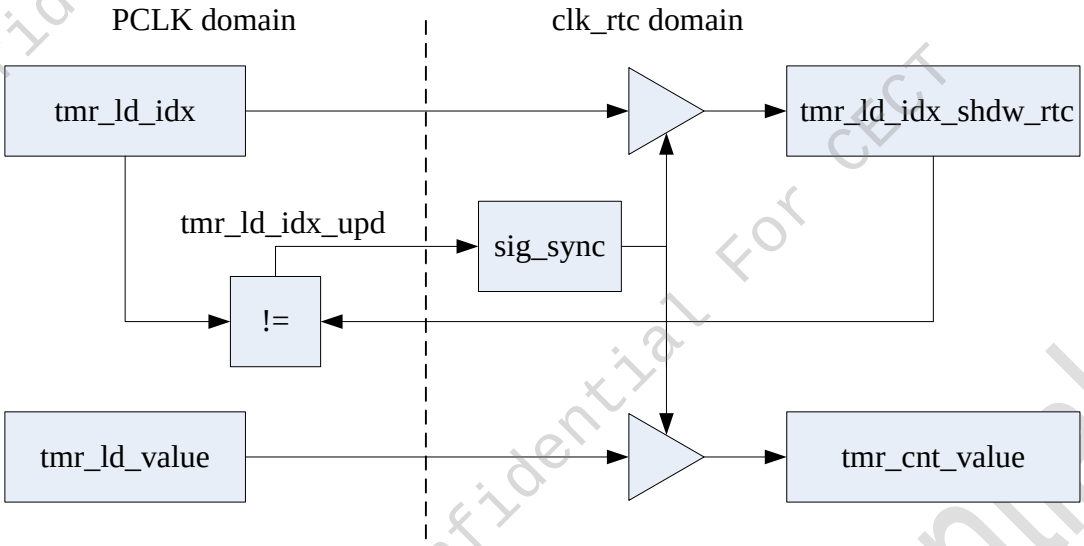
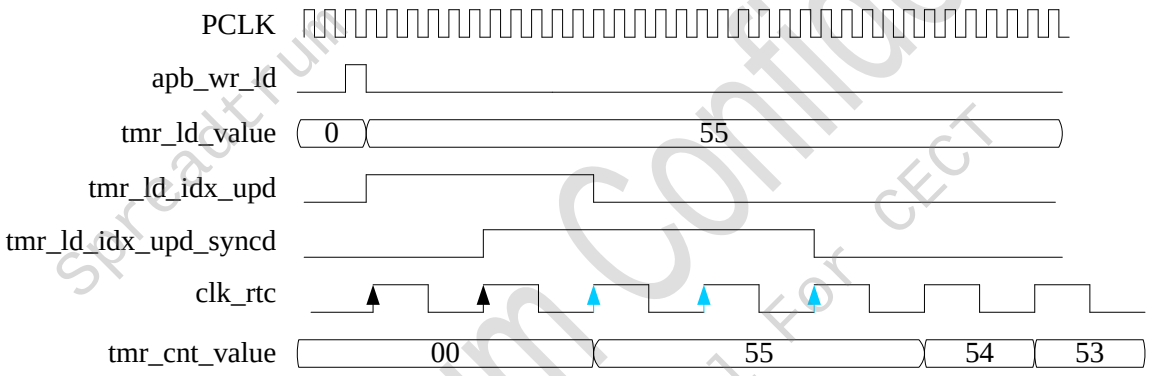
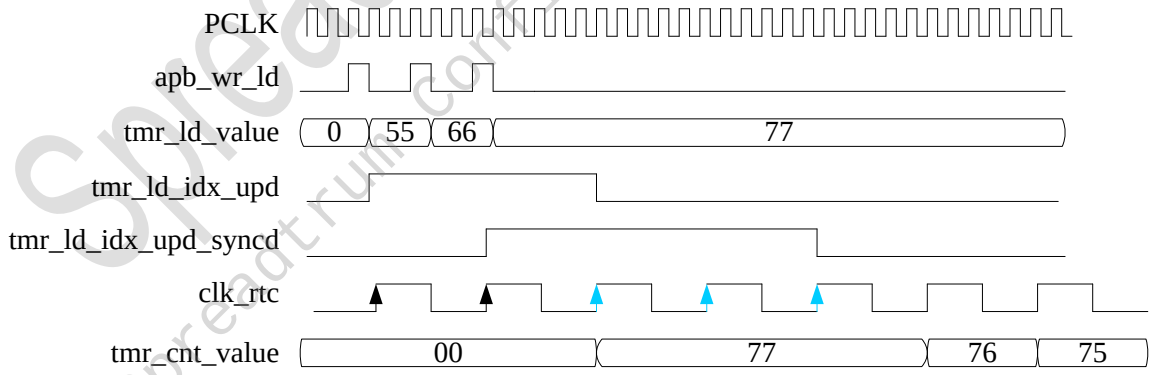


Figure 7-9 Solution of multiple load



Maximum delay is 5 clk_rtc

Figure 7-10 Single load



Last load value(77) is loaded into tmr_cnt_value

Figure 7-11 multiple load

Waiting before read counter value: In software, write and then read is commonly used to check whether a register is written correctly. However, when this method is used in timer, more attention

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

should be paid. Because the load need 3 clk_rtc to finish, read value before that is illegal. Furthermore, there is no signal to indicate load is finish. Software has to count 3 clk_rtc by itself or wait 1 clk_rtc after tmr_ld_busy change to 0.

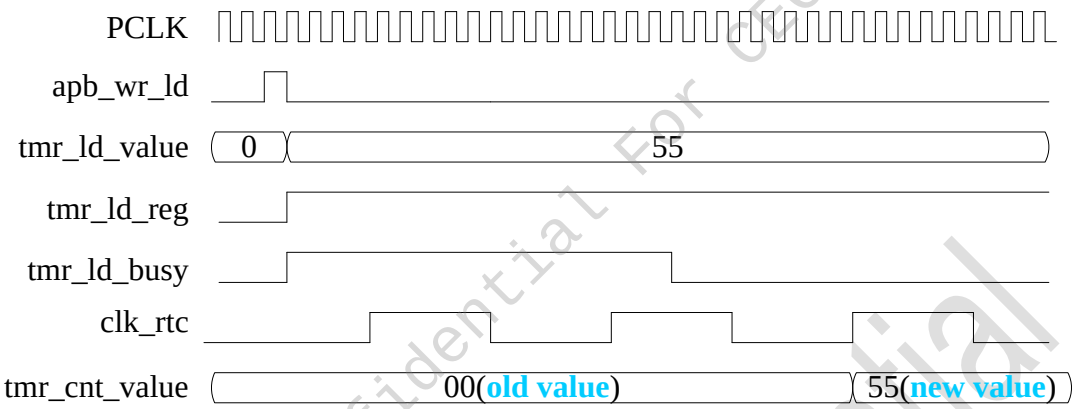


Figure 7-12 Wait 3 cycle to get new value

Solution to Waiting: The solution is based on the knowledge that before load is done, we can use tmr_ld_value for read, and after load is done we can use tmr_cnt_shdw. To determine when the load is done, we sync tmr_ld_idx_shdw_rtc back to PCLK domain, and the synced signal is tmr_ld_idx_shdw_pclk. If tmr_ld_idx_shdw_pclk is equal to tmr_ld_idx, current load is done (tmr_loading = 0). This method works in the case of PCLK closed or auto-gated. After PCLK is open again, tmr_ld_idx_shdw_pclk can quickly sample the tmr_ld_idx_shdw_rtc and tmr_loading is updated. This only needs three PCLK. Usually software read happens after that period of time, so the read result is accurate. In Figure 5-82, the signal synchronization circuit using shadow mechanism circuit is not showed for simplicity.

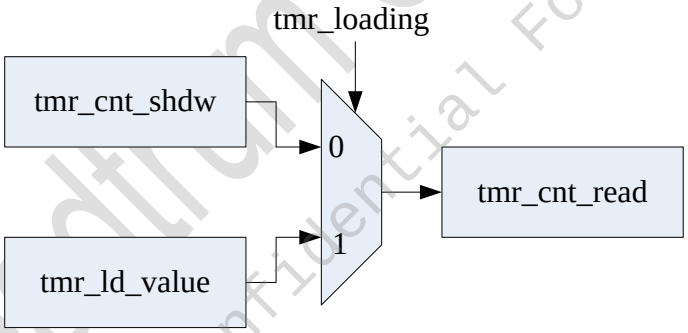


Figure 7-13 Solution to wait certain time

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

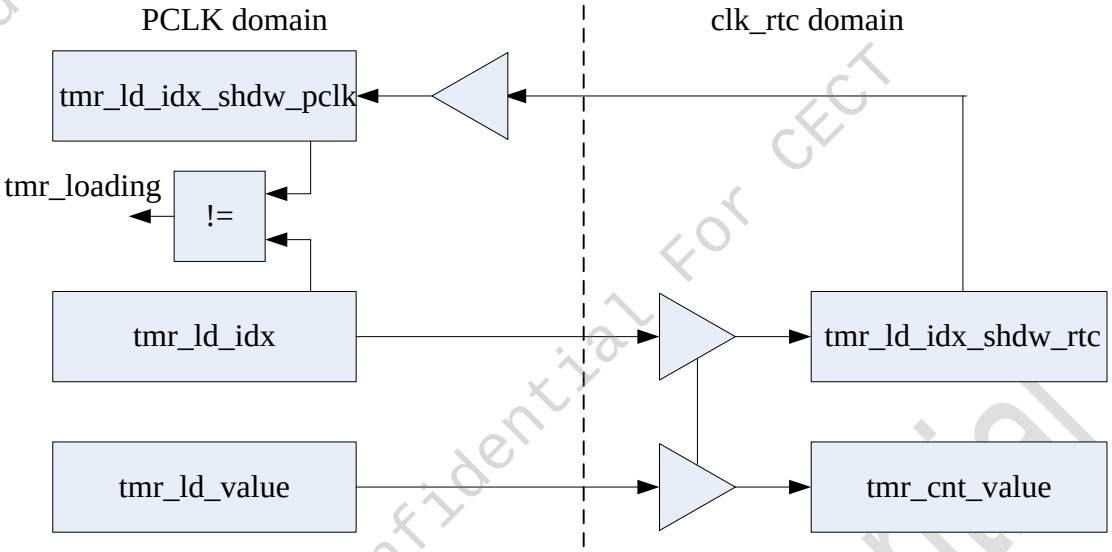


Figure 7-14 Waveform of tmr_loading

7.3.5 Control Registers

7.3.5.1 Memory map

Timer0:

Offset Address	Name	Description
0x0000	TIMER0_LOAD	Timer0 load value
0x0004	TIMER0_VALUE	Timer0 counter value
0x0008	TIMER0_CTL	Timer0 control registers**(add tmr_new)**
0x000C	TIMER0_INT	Timer0 interrupt
0x0010	TIMER0_CNT_RD	Timer0 counter value for read**(new added)**

Timer1:

Offset Address	Name	Description
0x0020	TIMER1_LOAD	Timer1 load value
0x0024	TIMER1_VALUE	Timer1 counter value
0x0028	TIMER1_CTL	Timer1 control registers
0x002C	TIMER1_INT	Timer1 interrupt
0x0030	TIMER1_CNT_RD	Timer1 counter value for read

Timer2:

Offset Address	Name	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Offset Address	Name	Description
0x0040	TIMER2_LOAD	Timer2 load value
0x0044	TIMER2_VALUE	Timer2 counter value
0x0048	TIMER2_CTL	Timer2 control registers
0x004C	TIMER2_INT	Timer2 interrupt
0x0050	TIMER2_CNT_RD	Timer2 counter value for read

7.3.5.2 Register Descriptions

7.3.5.2.1 TIMER0_LOAD

Description: Timer0 load value

0x0000			Timer0 load value (Reset 0x0000_0000)										TIMER0_LOAD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer0_load															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer0_load															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer0_load	[31:0]	RW	32'h0	Timer0 load value Write to this register will reload the timer with the new value. In one-time mode, this value is the first counting start number. In periodic mode, this value is each counting start number.

7.3.5.2.2 TIMER0_VALUE

Description: Timer0 counter value

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0004			Timer0 counter value (Reset 0x0000_0000)										TIMER0_VALUE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer0_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer0_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer0_value	[31:0]	RO	32'h0	Timer0 counter value This read-only register indicates current counter value. It's not recommended to read this register in normal usage. Because the counter is in different clock domain with APB, software needs use double-reading method to read this value, like system timer.

7.3.5.2.3 TIMER0_CTL (add tmr_new)

Description: Timer0 control registers

0x0008			Timer0 control register (Reset 0x0000_0000)										TIMER0_CTL			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							Timer0_new	timer0_run	timer0_mode	Reserved					
Type	RO							RW	RW	RW	RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:9]	RO	23'h0	Reserved
timer0_new	[8]	RW	1'h0	Timer0 version 0: timer use old behavior, this is

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Default Value	Description
				for backward compatibility. 1: timer uses new behavior, such as multiple loads without checking busy bit, only need to read once to get timer counter value. When timer0_new=1, software must not check checking busy bit. Busy bit cannot be used when timer0_new=1.
timer0_run	[7]	RW	1'h0	Timer0 open bit 0: timer stops 1: timer runs
timer0_mode	[6]	RW	1'h0	Timer0 mode select 0: one-time mode 1: period mode
	[5:0]	RO	6'h0	Reserved

7.3.5.2.4 **TIMER0_INT**

Description: Timer0 interrupt

0x000C			Timer0 interrupt (Reset 0x0000_0000)													TIMER0_INT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											timer0_ld_busy	timer0_int_clr	timer0_int_mask_sts	timer0_int_raw_sts	timer0_int_en
Type	RO											RO	WO	RO	RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:5]	RO	27'h0	Reserved
timer0_ld_busy	[4]	RO	1'h0	Timer0 load busy status 0: Timer is ready for new loading 1: Last loading is not completed Software must not load new value when this bit is busy, that is, this bit should be checked

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Default Value	Description
				before any new loading. This bit is set after a new loading, and lasts two or three RTC clock cycles, about 60us - 92us.
timer0_int_clr	[3]	WO	1'h0	Timer0 Interrupt clear Write 1 to this bit to clear interrupt
timer0_int_mask_sts	[2]	RO	1'h0	Timer0 interrupt masked status
timer0_int_raw_sts	[1]	RO	1'h0	Timer0 interrupt raw status
timer0_int_en	[0]	RW	1'h0	Timer0 interrupt enable

7.3.5.2.5 **TIMER0_CNT_RD**

Description: Timer0 counter value for read

0x0010			Timer0 counter value for read(Reset 0x0000_0000)										TIMER0_CNT_RD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer0_cnt_rd															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer0_ cnt_rd															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer0_cnt_rd	[31:0]	RO	32'h0	Timer0 counter value for read. Only valid when tmr_new = 1. If tmr_new = 0, don't read this register. This read-only register indicates current counter value. The advantage of this register is software can read the counter value immediately after load, without waiting for the load done. Also, software just needs to read once instead of double read.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

7.3.5.2.6 **TIMER1_LOA**

Description: Timer1 load value

0x0020			Timer1 load value (Reset 0x0000_0000)										TIMER1_LOAD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer1_load															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer1_load															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer1_load	[31:0]	RW	32'h0	Timer1 load value Write to this register will reload the timer with the new value. In one-time mode, this value is the first counting start number. In period mode, this value is each counting start number.

7.3.5.2.7 **TIMER1_VALUE**

Description: Timer1 counter value

0x0024			Timer1 counter value (Reset 0x0000_0000)										TIMER1_VALUE			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer1_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer1_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer1_value	[31:0]	RO	32'h0	Timer1 counter value This read-only register indicates current counter value. It's not recommended to read

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Reset Value	Description
				this register in normal usage. Because the counter is in different clock domain with APB, software needs use double-reading method to read this value, like system timer.

7.3.5.2.8 **TIMER1_CTL**

Description: Timer1 control registers

0x0028	Timer1 control register (Reset 0x0000_0000)													TIMER1_CTL		
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							Timer1_new	Timer1_run	Timer1_mode	Reserved					
Type	RO							RW	RW	RW	RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:9]	RO	23'h0	Reserved
Timer1_new	[8]	RW	1'h0	Timer1 version 0: timer use old behavior, this is for backward compatibility. 1: timer uses new behavior, such as multiple loads without checking busy bit, only need to read once to get timer counter value. When timer1_new=1, software must not check checking busy bit. Busy bit cannot be used when timer1_new=1.
timer1_run	[7]	RW	1'h0	Timer1 open bit 0: timer stops 1: timer runs
timer1_mode	[6]	RW	1'h0	Timer1 mode select 0: one-time mode 1: period mode
	[5:0]	RO	6'h0	Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

7.3.5.2.9 **TIMER1_INT**

Description: Timer1 interrupt

0x002C			Timer1 interrupt (Reset 0x0000_0000)													TIMER1_INT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											timer1_ld_busy	timer1_int_clr	timer1_int_mask_sts	timer1_int_raw_sts	timer1_int_en
Type	RO											RO	WO	RO	RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:5]	RO	27'h0	Reserved
timer1_ld_busy	[4]	RO	1'h0	Timer1 load busy status 0: Timer is ready for new loading 1: Last loading is not completed Software must not load new value when this bit is busy, that is, this bit should be checked before any new loading. This bit is set after a new loading, and lasts two or three RTC clock cycles, about 60us - 92us.
timer1_int_clr	[3]	WO	1'h0	Timer1 Interrupt clear Write 1 to this bit to clear interrupt
timer1_int_mask_sts	[2]	RO	1'h0	Timer1 interrupt masked status
timer1_int_raw_sts	[1]	RO	1'h0	Timer1 interrupt raw status
timer1_int_en	[0]	RW	1'h0	Timer1 interrupt enable

7.3.5.2.10 **TIMER1_CNT_RD**

Description: Timer1 counter value for read

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0030			Timer1 counter value for read(Reset 0x0000_0000)										TIMER1_CNT_RD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer1_cnt_rd															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	timer1_ cnt_rd															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer1_cnt_rd	[31:0]	RO	32'h0	Same as timer0_cnt_rd

7.3.5.2.11 **TIMER2_LOAD**

Description: Timer2 load value

0x0040			Timer2 load value (Reset 0x0000_0000)										TIMER2_LOAD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Timer2_load															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Timer2_load															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
Timer2_load	[31:0]	RW	32'h0	Timer2 load value Write to this register will reload the timer with the new value. In one-time mode, this value is the first counting start number. In period mode, this value is each counting start number.

7.3.5.2.12 **TIMER2_VALUE**

Description: Timer2 counter value

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0044			Timer2 counter value (Reset 0x0000_0000)													TIMER2_VALUE
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	timer2_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Timer2_value															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
timer2_value	[31:0]	RO	32'h0	Timer2 counter value This read-only register indicates current counter value. It's not recommended to read this register in normal usage. Because the counter is in different clock domain with APB, software needs use double-reading method to read this value, like system timer.

7.3.5.2.13 **TIMER2_CTL**

Description: Timer2 control registers

0x0048			Timer2 control register (Reset 0x0000_0000)													TIMER2_CTL
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							Timer2_new	Timer2_run	Timer2_mode	Reserved					
Type	RO							RW	RW	RW	RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:9]	RO	23'h0	Reserved
Timer2_new	[8]	RW	1'h0	Timer2 version 0: timer use old behavior, this is

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Default Value	Description
				for backward compatibility. 1: timer uses new behavior, such as multiple loads without checking busy bit, only need to read once to get timer counter value. When timer2_new=1, software must not check checking busy bit. Busy bit cannot be used when timer2_new=1.
Timer2_run	[7]	RW	1'h0	Timer2 open bit 0: timer stops 1: timer runs
Timer2_mode	[6]	RW	1'h0	Timer2 mode select 0: one-time mode 1: period mode
	[5:0]	RO	6'h0	Reserved

7.3.5.2.14 **TIMER2_INT**

Description: Timer2 interrupt

0x004C			Timer2 interrupt (Reset 0x0000_0000)													TIMER2_INT
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											timer2_ld_busy	timer2_int_clr	timer2_int_mask_sts	timer2_int_raw_sts	timer2_int_en
Type	RO											RO	WO	RO	RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Default Value	Description
	[31:5]	RO	27'h0	Reserved
Timer2_ld_busy	[4]	RO	1'h0	Timer2 load busy status 0: Timer is ready for new loading 1: Last loading is not completed Software must not load new value when this bit is busy, that is, this bit should be checked before any new loading.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Default Value	Description
				This bit is set after a new loading, and lasts two or three counting clock cycles.
Timer2_int_clr	[3]	WO	1'h0	Timer2 Interrupt clear Write 2 to this bit to clear interrupt
Timer2_int_mask_sts	[2]	RO	1'h0	Timer2 interrupt masked status
Timer2_int_raw_sts	[1]	RO	1'h0	Timer2 interrupt raw status
Timer2_int_en	[0]	RW	1'h0	Timer2 interrupt enable

7.3.5.2.15 **TIMER2_CNT_RD**

Description: Timer2 counter value for read

0x0050	Timer2 counter value for read(Reset 0x0000_0000)												TIMER2_CNT_RD			
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Timer2_cnt_rd															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Timer2_ cnt_rd															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
Timer2_cnt_rd	[31:0]	RO	32'h0	Same as timer0_cnt_rd

7.3.6 Application Notes

7.3.6.1 RTC Clock Trigged Timers

When software uses RTC clock trigged timer, it should set tmr_eb bit and tmr_rtc_eb bit in global control register.

Before opening timer0_run or timer1_run, software should configure all control registers – timer0_load or timer1_load, timer0_mode or timer1_mode, timer0_int_en or timer1_int_en, timer0_new or timer1_new.

Then timer0_run or timer1_run is set to 1 to open corresponding timer.

After receiving interrupt issued by a timer, software can check interrupt status by reading timer0_int_mask_sts or timer1_int_mask_sts, and can clear interrupt by writing 1 to timer0_int_clr or timer1_int_clr.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

When software completes using RTC clock trigged timer, it should disable timer0_run or timer1_run firstly, then it disable tmr_rtc_eb and tmr_eb in global control registers.

It's IMPORTANT that there are 3~5 RTC clock cycles delay from setting timer0_load or timer1_load to counter setting success(refer to Figure 5-78), that is, if N is configured in timer0_load or timer1_load, real counting number is N+3 or N+4 or N+5.

When timer0_new or timer1_new = 0, software must check timer0_ld_busy or timer1_ld_busy before loading.

When timer0_new or timer1_new =1, software need not check timer0_ld_busy or timer1_ld_busy. Loading is permitted at any time. Furthermore, software Must not check timer0_ld_busy or timer1_ld_busy.Since timer0_ld_busy or timer1_ld_busy cannot be used when timer0_new or timer1_new =1.timer0_ld_busy or timer1_ld_busy may stay at 1 all the time.

If the timer is configured in one-time mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued. The counter stays at 0 until software load it again.

If the timer is configured in period mode, counter decreases from setting value to 0. When counter gets to 0, an interrupt is issued, and counter is reloaded by setting value, and then counter continues to decrease from setting value.

7.3.7 Implementations

Logic in clk_rtc domain should be synthesized at least 26M.

In Figure 5-73, when tmr_cnt_value change, it will be sampled to tmr_cnt_shdw after 3 PCLK. So tmr_cnt_value must be stable before that. For safety, we require that all logic in clk_rtc domain should be synthesized at 26M.

7.3.8 Features

7.3.9 Signal description

7.3.10 Funtion description

7.3.11 Control registers

7.3.11.1 Memory map

7.3.11.2 Register description

7.3.12 Application notes

7.3.13 Implementations

7.3.14 Future improvements

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

8 FM System

8.1 Overview

Figure 1-1 illustrates the digital system of FM Receiver. It consists of major subsystems of: decimation stages, filters, downconverter with Cordic, FM demodulation, pilot extraction and subcarrier recovery, MPX demodulation, stereo-decode matrix, de-emphasis, DC-offset, RSSI, AGC, frequency offset, pilot detect, SEEK/TUNE, adaptive configuration, and ¼ msec timer.

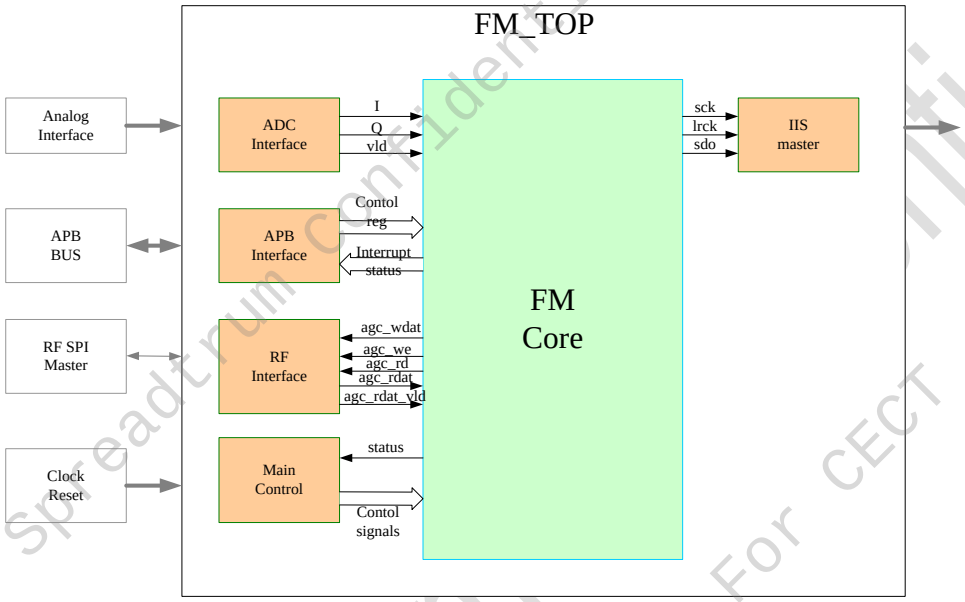


Figure 1-8 FM Architecture Diagram

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

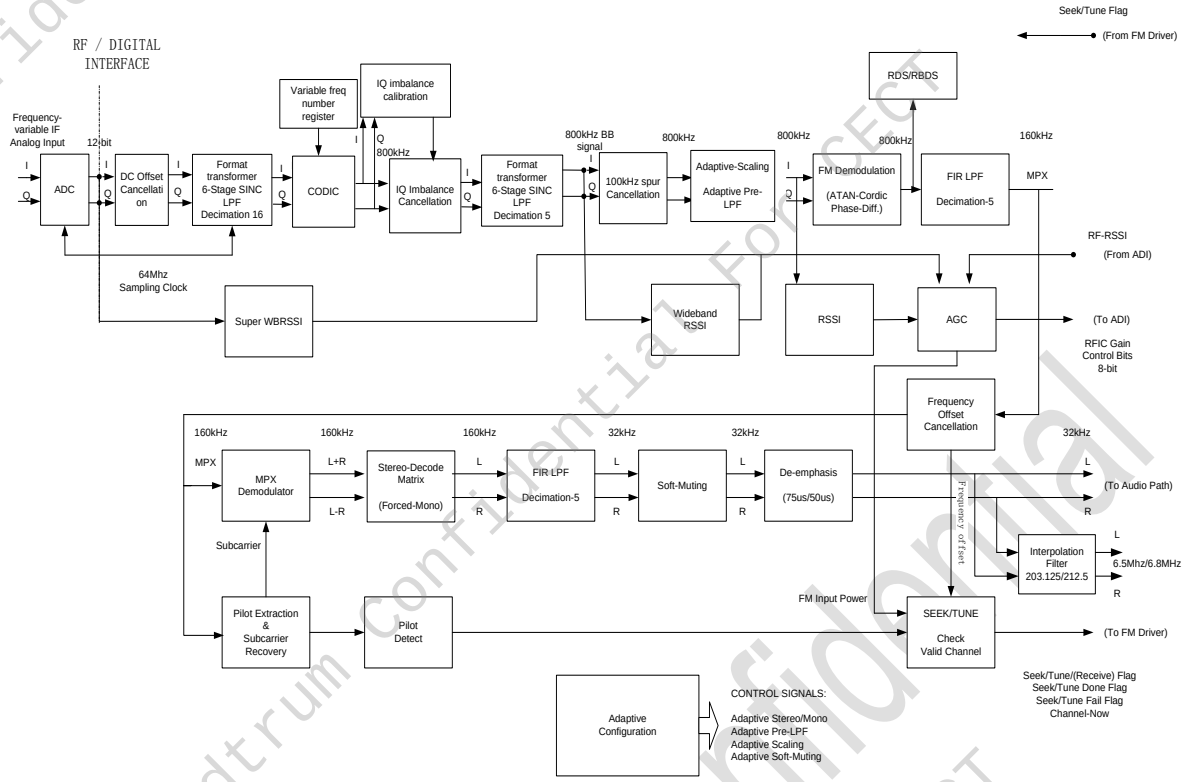


Figure 8-2 FM Data Path Diagram

Super WBRSSI

Super wbrssi calculates the power of ADC data before all the filters, downconverters and dc removal. And so super wbrssi control the gain in agc methods will perform high efficiency on keeping the ADC saturating.

Two 6-stage SINC LPF (CIC filter)

In this block, ADC data is converted from 64M sample rate to 4M sample rate after the first 6-stage SINC LPF and sample rate will be converted to 800k after the second 6-stage SINC LPF.

Cordic

The function of this module is to rotate the adc data from IF to near zero frequency. It works at 4M sample rate between the first and second 6-state SINC filter. It supports configurable IF, such as +/-100k, +/-200k, +/-128k .et.

IQ Imbalance Calibration

This module could be calibrate the imbalance in I and Q data path to improve the performance of FM. It works at 4M sample rate between the first and second 6-state SINC filter.

DC Offset Cancel

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

The function of this module is to removal the DC offset generated by RF circuit. DC offset cancel is independent with dcoc calibration and configurable to enable and disable. Removal DC is not only for cleaning the adc data, but also be prepared for the IQ calibration later.

Spur Removal

The function of spur removal is to inhibit the spur occurred when FM receive channel with 100k spur. The spur could influence FM on two aspects, one is leading FM seek the false channel if the channel do not exist, and the other making the SINAD worse more than 20dB when the channel do exist.

As a result of that the spur could be exactly moved to DC after Digital down converter (DDC), the method of inhibiting the spur is same with dc offset cancel module.

FIR LPF for Channel Selection

This linear-phase LPF provides major role of channel selection in the analog/digital input signal path prior to FM demodulation.

FM Demodulation

This FM demodulation is first to use the ATAN () function to get phase information from the current I/Q sample and then to use the phase difference from the previous sample to estimate frequency information. The un-filtered MPX signal is derived from the estimated frequency, without the knowledge of Peak Frequency Deviation of either 75 kHz in US or 22.5 kHz in Europe. The ATAN () function is actually implemented using a simple

FIR LPF of FM Demodulated Signal and Decimation

The FIR LPF filters the FM demodulated signal to provide the MPX signal and also provides the anti-aliasing lowpass filtering for the following decimation. The decimation by 5 next reduces the sampling of MPX to 160 kHz.

Extraction of Pilot in the MPX Signal

A narrow-band 19 kHz BPF provides filtering on 19 kHz Pilot. The extracted Pilot should have a good enough CNR for the next Subcarrier recovery.

The 38 kHz Subcarrier Recovery

The extracted Pilot is first squared, and the squared signal is then normalized using local samples. A narrow-band 38 kHz BPF filters the normalized squared-signal to obtain the 38 kHz Subcarrier for the following demodulation of the MPX signal to obtain the L-R signal.

The MPX Signal Demodulation

This block includes two functions, L-R Demodulation and L+R Demodulation. In L-R Demodulation, a wide-band BPF is first used to filter the MPX signal to get the modulated L-R signal portion centered at 38 kHz. The filtered signal is then multiplied with the 38 kHz Subcarrier to get the baseband L-R signal, along with other spectral components. In the L+R Demodulation block, the input signal is properly delayed as the baseband L+R signal, along with other spectral components.

Stereo-Decode Matrix, with Forced-Mono Operation

The Matrix inputs the baseband L+R and L-R signals and produces the L and R stereo audio signals. When Forced-Mono is ON, the matrix only takes in the L+R signal and outputs the Mono signal in both L and R channels, that is, L=R.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

FIR LPF of Stereo Signals

This FIR LPF filters the L and R signals, as the continuation of the previous Stereo-Decode operation. It also provides anti-aliasing lowpass filtering for a final decimation. This decimation by 5 brings the sampling of the L and R signals down to 32 kHz, as the audio output sampling.

De-emphasis

The de-emphasis LPF is conducted on the 32 kHz L and R signals. Configuration of the de-emphasis is 75us in US and 50us in Europe.

RSSI

The RSSI block works at 800 kHz and takes both the I signal and the Q signal from the channel-selection LPF after the quadrature downconverter. It takes relatively long time average on the input signal for the power estimate and converts it into a dB value of RSSI, for the purpose of AGC gain control and FM input power estimate.

AGC

The AGC block, running at 800 kHz, offers two functions: generating the AGC gain-table index for FM RF/Analog section and estimating FM input signal power. It compares the input RSSI value to a high boundary and a low boundary. The comparison results in an increment or a decrement from the current gain-table index or a no change on the gain.

Frequency Offset Measure and Cancellation

Frequency Offset Measure and Cancellation, at 160 kHz, uses SINC LPF to offer very lowpass filtering while keeps a lower complexity filter implementation. The need of very lowpass filtering is for a high performance requirement on Stereo-Audio SNR. The block estimates the frequency offset from the decimated, demodulated signal and thus cancels the frequency offset from the signal.

Pilot Detect

The Pilot Detect block, at 160 kHz, takes as input the two extracted pilot signals from Pilot Extraction and measures the amplitude averages. It then compares the first average to a programmable threshold and checks the difference between them. Finally, it makes a preliminary decision to decode this signal input in either Stereo-Audio or Mono-Audio mode or to handle the signal as noise, generating indicator Ind_StereoMonoNoise_byPilot.

SEEK/TUNE Check Valid-Channel

The inputs of this SEEK/TUNE Check Valid-Channel block are Ind_StereoMonoNoise_byPilot, frequency offset and FM input signal power. The block makes a (final) decision on a valid channel, during SEEK/TUNE operation, by comparing frequency offset and FM input signal power to programmable thresholds and checking the status of Ind_StereoMonoNoise_byPilot.

Adaptive Configuration

The Adaptive Configuration block takes several meaningful inputs from the other blocks. It adaptively adjusts a subset of configurable parameters which control operation modes of some of the blocks in order to provide robustness of this FM receiver in any dynamically changing radio environment.

Table 8-1 PIN Description

Name	Width	I/O	Description
PCLK	1	Input	APB clock

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

PRESTN	1	Input	APB reset, low active
64m_clk	1	Input	FM main clock, 64MHz
64m_rst_n	1	Input	FM reset, low active
PSEL	1	Input	APB select
PENABLE	1	Input	APB enable
PADDR	32	Input	APB address
PWDATA	32	Input	APB write data
PRDATA	32	Output	APB read data
fm_int	1	Output	FM interrupt
adc_idata	12	Input	I data from adc
adc_qdata	12	input	Q data from adc
i2s_sck	1	Output	I2S output clock
i2s_lrck	1	Output	I2S left/right channel select
i2s_do	1	Output	I2S serial data out
o_rfctl_aces_req	1	Output	SPI interface signals which be used for RF control.
o_rfctl_do	32	Output	
i_rfctl_rdy	1	Input	
i_rfctl_din	16	Input	

8.2 FM Key Function description

8.2.1 SEEK/Tune function description

Seek and tune control flow is shown on figure 1-3.

State Config_RF_Frequency is to configure the frequency of a channel. The state costs 8 clock periods.

State Config_RF_Gain is to configure the initial gain value of RF. The state costs 8 clock periods.

State Wait_RF_Data_stable is to wait for PLL and calibration, the state costs a configurable clock periods which is in the range of 0~224-1, that is 0~645ms;On one hand If the delay of this state is configured too small, FM will receive the unstable data and on the other hand the delay is configured too large, seek and tune one channel will cost too much time. As a result, 216-1(2.5ms) is proposed.

State Receive_Mode is to receive the stable ADC data. In the course of this state, FM will calculate the Power, frequency offset, pilot state and many other useful information of the locked channel. At the end of the state, FM will judge the channel is valid or not according to the calculated information. The state costs 1273999 clock periods which is about 48.9ms.

State channel_vld_chk_done is to set the status of seek/tune, to generate the interrupt when seek/tune is finish and to calculate the next channel frequency to seek when seek is not finish. The state costs only 1 clock period.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

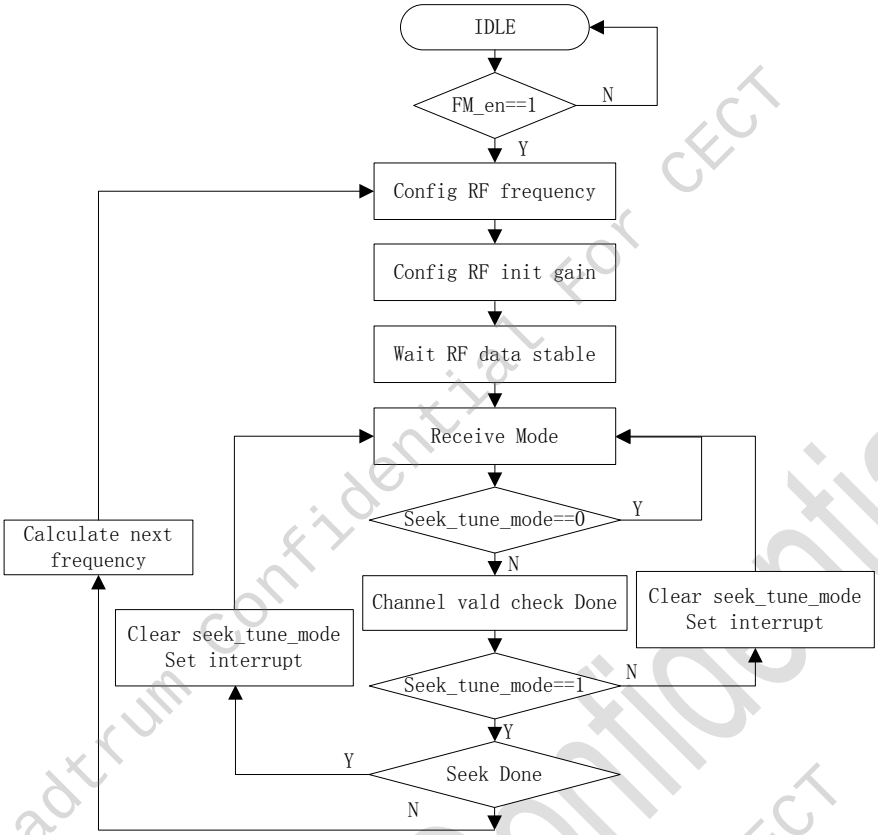


Figure 8-3 Seek/Tune Control Flow

8.2.2 RF control

FM realizes the control of RF through SPI. There are 4 signals between FM and SPI which are responsible for the communication: o_rfctl_aces_req, o_rfctl_do, i_rfctl_din and i_rfctl_rdy. Table 1-2 shows the function of these signals.

Table 8-2 Function of RF control Signals

Singal Name	Direction	Width	Function
o_rfctl_aces_req	O	1	1 means that FM wants to read from or write to RF.
o_rfctl_do	O	32	[31] bit: 0 means write; 1 means read. [30:16] corresponds to the address of registers in RF [15:0] the data write to RF when write mode and 0 when read mode
i_rfctl_din	I	16	Data read from RF.
i_rfctl_rdy	I	1	1 means that data read from RF is ready.

Take FM read data from address 7'h1f of RF for example. Figure 1.1.12-4 shows the sketch map.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

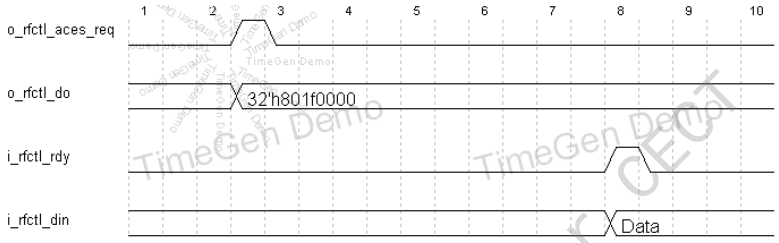


Figure 8-4 RF read sketch map

8.2.3 Calibration Description

Baseband of FM needs to do 5 kinds of calibration to improve the performance. As follows,

Shortant calibration, is to calibrate the different cap value for different channel frequency, so that to get good performance when fm works in shortant mode.

RC calibration, is to calibrate the rc parameter to get a good performance.

DCOC calibration, is to reduce the dc offset.

IQ imblance calibration is to depress the imbalance of I and Q data path.

AFC/AAC calibration is done in rf module, and the bb only need to send a start signal when change channels.

8.2.4 Ramp Softmute Method

Ramp softmute is a new added method to make sound ramp up and ramp down. There are 3 modes for controlling Ramp Softmute. Manual mode, RSSI mode and SNR mode. In Manual mode, users could configure the ramp step from 1 to 512 (only 2^n is valid), and could configure the end point of the raising or falling of the sound. In RSSI/SNR mode, the sound will ramp up or ramp down according to the calculated RSSI/SNR, When RSSI/SNR higher than the configurable threshold, Sound will hold or ramp up, otherwise, the sound will ramp down.

8.3 FM Register Address Map

Base address: 0x400B0000, 0x400B1000, 0x400B2000

Table 8-3 FM Register Address

Offset Addr	Name	Description
0x0000	FM_CTRL	FM Control Register
0x0004	FM_EN	FM Enable Control Register
0x0008	RF_INIT_GAIN	RF Initial Gain register
0x000C	CHAN	Channel selection frequency
0x0010	AGC_TBL_CLK	AGC DB Table clock control
0x0014	SEEK_LOOP	Seek loop configure register
0x0018	FMCTL_STI	Seek/Tune mode indicator register.
0x001C	BAND_LMT	Frequency band limit for seek.
0x0020	BAND_SPACE	Channel spacing.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0024	RFCTRL	RF control registers address
0x0028	ADCBITMAP	RF control registers address
0x0030	INT_EN	Interrupt Enable Register
0x0034	INT_CLR	Interrupt Clear Register
0x0038	INT_STS	Interrupt Status
0x003C	ADC_INFCTRL	ADC interface control
0x0040	SEEK_CH_TH	Seek Channel valid Threshold
0x0044	AGC_TBL_RFRSSI0	AGC table RFRSSI control register0
0x0048	AGC_TBL_RFRSSI1	AGC table RFRSSI control register1
0x004C	AGC_TBL_WBRSSI	WB RSSI measure control
0x0050	AGC_IDX_TH	AGC table Index Threshold
0x0054	AGC_RSSI_TH	AGC RSSI Threshold
0x0058	SEEK_ADPS	Seek Adaptive Scaling pre-demodulation
0x005C	STER_PWR	FM Stereo Power Threshold
0x0060	AGC_CTRL	AGC Control Register
0x0064	AGC_ITV_TH	AGC Interval Threshold
0x0068	AGC_ADPS0	AGC Adaptive Scaling pre-demodulation
0x006C	AGC_ADPS1	AGC Adaptive Scaling pre-demodulation
0x0070	PDP_TH	Pilot Detect Power Threshold
0x0074	PDP_DEV	Pilot Detect Power Deviation
0x0078	ADP_ST_CONF	Adaptive Stereo Configuration Register
0x007C	ADP_LPF_CONF	Adaptive LPF Configuration Register
0x0080	DEPHA_SCAL	De-emphasis scaling factor
0x0084	HW_MUTE	Hardware mute control
0x0088	SW_MUTE	Software mute control
0x008C	UPD_CTRL	Update counter control registers
0x0090	AUD_BLD0	Audio blend control register 0
0x0094	AUD_BLD1	Audio blend control register 1
0x0098	AGC_HYS	AGC Hysteresis control register
0x009C	MONO_PWR	FM Mono Power Threshold
0x00A0	RF_CFG_DLY	RF Configure Delay
0x00A4	AGC_TBL_STS	AGC Table Status
0x00A8	ADP_BIT_SFT	Pre-demodulation Adaptive Bit Shift
0x00AC	SEEK_CNT	Current Seek channel Counter
0x00B0	RSSI_STS	RSSI Status Register
0x00B8	CHAN_FREQ_STS	Current channel frequency
0x00BC	FREQ_OFF_STS	Frequency offset status
0x00C0	INPWR_STS	Input power status
0x00C4	RF_RSSI_STS	RF RSSI status
0x00C8	NO_LPF_STS	NO LPF status
0x00CC	SMUTE_STS	Software mute status
0x00D0	MISC_STS	Wideband RSSI status and some interface signals status
0x00D4	PILOT_STS	Pilot status
0x00D8	IQ_CALI_K1_ADDR	Pilot status
0x00DC	IQ_CALI_K2_ADDR	Pilot status
0x00E0	CALI_STS_ADDR	Pilot status
0x0100	SPUR_FREQ0	Spur position configuration
0x0104	SPUR_FREQ1	Spur position configuration
0x0108	IIS_CONFIG1	IIS config1 register
0x010C	IIS_CONFIG2	IIS config2 register
0x0110	IIS_CONFIG3	IIS config3 register
0x0114	IIS_CONFIG4	IIS config4 register
0x0118	CIC16_CONFIG1	CIC16_CONFIG1
0x011C	CIC16_CONFIG2	CIC16_CONFIG2

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0120	CIC16_FREQUENCY	CIC16_CONFIG1
0x0124	REG_CTRL1	FM control register 1
0x0128	AMP_ADJ	AMP_ADJ
0x012C	IQ_CALI	IQ_CALI
0x0130	SINE_GEN_ADDR	SINE_GEN_ADDR
0x0134	CALI_CTRL	CALI_CTRL
0x013C	RF_CTRL1	RF_CTRL1
0x0140	RF_CTRL2	RF_CTRL2
0x0144	RF_CTRL3	RF_CTRL3
0x0148	SOFTMUTE0	SOFTMUTE0
0x014C	SOFTMUTE1	SOFTMUTE1
0x0150	SOFTMUTE2	SOFTMUTE2
0x0154	SOFTMUTE3	SOFTMUTE3
0x0158	SOFTMUTE4	SOFTMUTE4
0x015C	SOFTMUTE5	SOFTMUTE5
0x0160	DB_COMP	DB_COMP

8.3.1 FM_CTRL

0x00000000			FM Control Register (0x02080110)									FM_CTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	dump_mod				reserved		FOC_MOD		reserved	FREEZE_ENB	MISC_SRST	ADC_LPF_NO1	SEEK_UP	STER_S_WAP	reserved	RXM
Type	RW				RO		RW		RO	RW	RW	RW	RW	RW	RO	RW
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved		SPRM_MODE		reserved			STE2MONO_MODE	reserved		DEM		reserved		NO_LPF	
Type	RO		RW		RO			RW	RO		RW		RO		RW	
Reset	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

FM Control Register

Field Name	Bit	Type	Reset Value	Description
dump_mod	[31:28]	RW	0x0	Data dump source select. 0: 0 1-A: FM b-f: FM_RDS
reserved	[27:26]	RO	0x0	Reserved
FOC_MOD	[25:24]	RW	0x2	0: Choose the first level of SINC filter as frequency offset;

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				1: Choose the second level of SINC filter as frequency offset; 2: Choose the second level of SINC filter as frequency offset;
reserved	[23]	RO	0x0	Reserved
FREEZE_ENB	[22]	RW	0x0	1. Freeze the statue of FM channel; 0: Not freeze the statue of FM channel;
MISC_SRST	[21]	RW	0x0	1.soft reset MISC logic 0:no soft reset misc logic
ADC_LPF_NO1	[20]	RW	0x0	1.new 90k filter 0:old 90k filter
SEEK_UP	[19]	RW	0x1	Seek loop up or down. 1: seek up 0: seek down
STER_SWAP	[18]	RW	0x0	Stereo channel swap. 0: no swap 1: left/right channel swap
reserved	[17]	RO	0x0	Reserved
RXM	[16]	RW	0x0	Stereo or Mono RX mode. 0: stereo mode 1: mono mode
reserved	[15:14]	RO	0x0	Reserved
SPRM_MODE	[13:12]	RW	0x0	Spur removal working mode: 0: disable 1:hardware automatic enable spur removal function 2:reserved 3:force enable
reserved	[11: 9]	RO	0x0	Reserved
STE2MONO_MODE	[8]	RW	0x1	0:force mono mode 1:disable automatic select mono/stereo mode
reserved	[7: 6]	RO	0x0	Reserved
DEM	[5: 4]	RW	0x1	De-emphasis type. 0: No de-emphasis 1: 75us for US 2: 50us for EU
reserved	[3: 2]	RO	0x0	Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

NO_LPF	[1: 0]	RW	0x0	ADC decimation LPF control

8.3.2 FM_EN

0x00000004			FM Enable Control Register (0x0003806E)									FM_EN				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	GLBEN	reserved													audio_dcrm_enb	IIS
Type	RW	RO													RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	AUD_PP	reserved		AUD_BLD	SW_MUTE	HW_MUTE	ADP_LPF	reserved	PLT_DECT	FOC	FOM	AGC_ADPS	AGC	RSSI	DCC	SEEK_ADPS
Type	RW	RO		RW	RW	RW	RW	RO	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0

FM Enable and Software Reset Control Register

Field Name	Bit	Type	Reset Value	Description
GLBEN	[31]	RW	0x0	FM Global Enable bit.
reserved	[30:18]	RO	0x0	reserved
audio_dcrm_enb	[17]	RW	0x1	audio_dcrm_enb
IIS	[16]	RW	0x1	IIS enable
AUD_PP	[15]	RW	0x1	Audio post process enable
reserved	[14:13]	RO	0x0	Reserved
AUD_BLD	[12]	RW	0x0	Audio blend enable
SW_MUTE	[11]	RW	0x0	Software mute enable
HW_MUTE	[10]	RW	0x0	Hardware mute enable.
ADP_LPF	[9]	RW	0x0	Adaptive configuration ADC decimation LPF enable
reserved	[8]	RO	0x0	Reserved
PLT_DECT	[7]	RW	0x0	Pilot Detect enable
FOC	[6]	RW	0x1	Frequency Offset Cancel enable
FOM	[5]	RW	0x1	Frequency Offset Measure enable
AGC_ADPS	[4]	RW	0x0	AGC Adaptive scaling pre-demodulation enable
AGC	[3]	RW	0x1	AGC enable
RSSI	[2]	RW	0x1	RSSI enable
DCC	[1]	RW	0x1	DC Offset Cancel enable
SEEK_ADPS	[0]	RW	0x0	Seek Adaptive scaling pre-demodulation enable

8.3.3 RF_INIT_GAIN

0x00000008			RF Initial Gain register (0x00000000)									RF_INIT_GAIN				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VAL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RF Initial Gain register

Field Name	Bit	Type	Reset Value	Description
reserved	[31:16]	RO	0x0	Reserved
VAL	[15: 0]	RW	0x0	RF initial gain value.

8.3.4 CHAN

0x0000000C			Channel selection frequency (0x0640036C)									CHAN				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved			CHAN_IF									reserved			FREQ
Type	RO			RW									RO			RW
Reset	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FREQ															
Type	RW															
Reset	0	0	0	0	0	0	1	1	0	1	1	0	1	1	0	0

Channel selection frequency.

Field Name	Bit	Type	Reset Value	Description
reserved	[31:29]	RO	0x0	Reserved
CHAN_IF	[28:20]	RW	0x64	CHAN_IF
reserved	[19:17]	RO	0x0	reserved
FREQ	[16: 0]	RW	0x36C	Channel selection frequency which is used for SEEK, Tune or directly play

8.3.5 AGC_TBL_CLK

0x00000010			AGC DB Table clock control (0x00000000)									AGC_TBL_CLK				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	reserved															SEL
Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AGC DB Table clock control

Field Name	Bit	Type	Reset Value	Description
reserved	[31: 1]	RO	0x0	Reserved
SEL	[0]	RW	0x0	Clock select. 0: Slect FM 26M clock for AGC table 1: Select APB clock for AGC table

8.3.6 SEEK_LOOP

0x00000014			Seek loop config register (0x00000064)									SEEK_LOOP				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						VAL									
Type	RO						RW									
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Seek loop config register

Field Name	Bit	Type	Reset Value	Description
reserved	[31:10]	RO	0x0	Reserved
VAL	[9: 0]	RW	0x64	Seek loop config value. Seek_loop=(band_lmt_high-band_lmt_low)/band_space when the seek mode is set.

8.3.7 FMCTL_STI

0x00000018			Seek/Tune mode indicator register. (0x00000000)									FMCTL_STI				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved															

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved														VAL	
Type	RO														RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Seek/Tune mode indicator register.

0: NORMAL

1: SEEK

2: TUNE

Field Name	Bit	Type	Reset Value	Description
reserved	[31: 2]	RO	0x0	Reserved
VAL	[1: 0]	RW	0x0	Seek/Tune indicator configure value. 0: NORMAL 1: SEEK 2: TUNE

8.3.8 BAND_LMT

0x0000001C			Frequency band limit for seek. (0x0000FDE8)									BAND_LMT				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															LOW
Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LOW															
Type	RW															
Reset	1	1	1	1	1	1	0	1	1	1	1	0	1	0	0	0

Frequency band limit for seek.

Frequency=val*10kHz

Field Name	Bit	Type	Reset Value	Description
reserved	[31:17]	RO	0x0	High band limit for seek
LOW	[16: 0]	RW	0xFDE	Low band limit for seek

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			8	

8.3.9 BAND_SPACE

0x00000020			Channel spacing. (0x6401A5E0)									BAND_SPACE				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	BAND_SPACE_VAL								reserved							BAND_LMT_HIGH
Type	RW								RO							RW
Reset	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BAND_LMT_HIGH															
Type	RW															
Reset	1	0	1	0	0	1	0	1	1	1	1	0	0	0	0	0

Channel spacing.

Space=val*10kHz

Field Name	Bit	Type	Reset Value	Description
BAND_SPACE_VAL	[31:24]	RW	0x64	BAND_SPACE_VAL
reserved	[23:17]	RO	0x0	Reserved
BAND_LMT_HIGH	[16: 0]	RW	0x1A5E0	Channel spacing config value

8.3.10 RFCTRL

0x00000024			RF control registers address (0x00040002)									RFCTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved	GAIN														
Type	RO	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved	BAND1														
Type	RO	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

RF control registers address

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
reserved	[31]	RO	0x0	Reserved
GAIN	[30:16]	RW	0x4	Gain control register address of RF
reserved	[15]	RO	0x0	Reserved
BAND1	[14: 0]	RW	0x2	frequency control register address of RF

8.3.11 ADCBITMAP

0x00000028			RF control registers address (0x7FFF7FFF)									ADCBITMAP				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved	LNA_STS														
Type	RO	RW														
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved	TIA_DCOC														
Type	RO	RW														
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

RF control registers address

Field Name	Bit	Type	Reset Value	Description
reserved	[31]	RO	0x0	Reserved
LNA_STS	[30:16]	RW	0x7FFF	LNA overload status register address of RF
reserved	[15]	RO	0x0	Reserved
TIA_DCOC	[14: 0]	RW	0x7FFF	Tia dcoc register address of RF

8.3.12 INT_EN

0x00000030			Interrupt Enable Register (0x00000000)									INT_EN				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved												RDS_BUF_GEN_INT_EN	RDS_BUF_UDF_INT_EN	RDS_BUF_OVF_INT_EN	STC
Type	RO												RO	RO	RO	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Interrupt Enable Register. Set 1 to enable the irq bit.

Field Name	Bit	Type	Reset Value	Description
reserved	[31: 4]	RO	0x0	Reserved
RDS_BUF_GEN_INT_EN	[3]	RO	0x0	RDS_BUF_GEN_INT_EN
RDS_BUF_UDF_INT_EN	[2]	RO	0x0	RDS_BUF_UDF_INT_EN
RDS_BUF_OVF_INT_EN	[1]	RO	0x0	RDS_BUF_OVF_INT_EN
STC	[0]	RW	0x0	Seek/Tune Complete Interrupt enable bit.

8.3.13 INT_CLR

0x00000034			Interrupt Clear Register (0x00000000)									INT_CLR				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved												RDS_BUF_GEN_INT_CLR	RDS_BUF_UDF_INT_CLR	RDS_BUF_OVF_INT_CLR	STC
Type	RO												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Interrupt Clear Register. Set 1 to clear the irq bit.

Field Name	Bit	Type	Reset Value	Description
reserved	[31: 4]	RO	0x0	Reserved
RDS_BUF_GEN_INT_CLR	[3]	RW	0x0	RDS_BUF_GEN_INT_CLR
RDS_BUF_UDF_INT_CLR	[2]	RW	0x0	RDS_BUF_UDF_INT_CLR
RDS_BUF_OVF_INT_CLR	[1]	RW	0x0	RDS_BUF_OVF_INT_CLR
STC	[0]	RW	0x0	Seek/Tune Complete Interrupt clear bit.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

8.3.14 INT_STS

0x00000038			Interrupt Status (0x00000000)									INT_STS				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved												RDS_BUF_GEN_INT_STS	RDS_BUF_UDF_INT_STS	RDS_BUF_OVF_INT_STS	STC
Type	RO												RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Interrupt Status

Field Name	Bit	Type	Reset Value	Description
reserved	[31: 4]	RO	0x0	Reserved
RDS_BUF_GEN_INT_STS	[3]	RO	0x0	RDS_BUF_GEN_INT_STS
RDS_BUF_UDF_INT_STS	[2]	RO	0x0	RDS_BUF_UDF_INT_STS
RDS_BUF_OVF_INT_STS	[1]	RO	0x0	RDS_BUF_OVF_INT_STS
STC	[0]	RO	0x0	Seek/Tune Complete Interrupt status.

8.3.15 ADC_INFCTRL

0x0000003C			ADC interface cotrol (0x00007FFF)									ADC_INFCTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved													adcif_control		
Type	RO													RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved	PGA_DCOC														
Type	RO	RW														
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

ADC interface cotrol

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

reserved	[31:19]	RO	0x0	Reserved
adcif_control	[18:16]	RW	0x0	[0]adcif soft reset [1]exchange I and q [2]convert the complent of adc data
reserved	[15]	RO	0x0	Reserved
PGA_DCOC	[14: 0]	RW	0x7FFF	pga dcoc register address of RF

8.3.16 SEEK_CH_TH

0x00000040			Seek Channel valid Threshold (0x000001F4)									SEEK_CH_TH				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VAL															
Type	RW															
Reset	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0

Seek Channel valid Threshold

Field Name	Bit	Type	Reset Value	Description
reserved	[31:16]	RO	0x0	Reserved
VAL	[15: 0]	RW	0x1F4	Seek channel valid threshold

8.3.17 AGC_TBL_RFRSSI0

0x00000044			AGC table RFRSSI control register0 (0x00200800)									AGC_TBL_RFRSSI0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved						UPD_CNT									
Type	RO						RW									
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved		HYST						reserved						MODE	
Type	RO		RW						RO						RW	
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

AGC table RFRSSI control register0

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

reserved	[31:26]	RO	0x0	Reserved
UPD_CNT	[25:16]	RW	0x20	AGC table RF RSSI update counter
reserved	[15:14]	RO	0x0	Reserved
HYST	[13: 8]	RW	0x8	AGC table RF RSSI hysteresis
reserved	[7: 2]	RO	0x0	Reserved
MODE	[1: 0]	RW	0x0	AGC table RF RSSI mode

8.3.18 AGC_TBL_RFRSSI1

0x00000048			AGC table RFRSSI control register1 (0x1F050BB8)									AGC_TBL_RFRSSI1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved	AVG_LEN							reserved					AVG_SH		
Type	RO	RW							RO					RW		
Reset	0	0	0	1	1	1	1	1	0	0	0	0	0	1	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TH															
Type	RW															
Reset	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0

AGC table RFRSSI control register1

Field Name	Bit	Type	Reset Value	Description
reserved	[31]	RO	0x0	Reserved
AVG_LEN	[30:24]	RW	0x1F	RFRSSI average length
reserved	[23:19]	RO	0x0	Reserved
AVG_SH	[18:16]	RW	0x5	RFRSSI average acc shift bits
TH	[15: 0]	RW	0xBB8	AGC table RF RSSI threshold

8.3.19 AGC_TBL_WBRSSI

0x0000004C			WB RSSI measure control (0x000A0C10)									AGC_TBL_WBRSSI				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved								TH							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved		HYST						reserved			WBRSSI_SHWAY	WBRSSI_SH		MODE	
Type	RO		RW						RO			RW	RW		RW	
Reset	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

WB RSSI measure control

Field Name	Bit	Type	Reset Value	Description
reserved	[31:24]	RO	0x0	Reserved
TH	[23:16]	RW	0xA	AGC table WBRSSI Threshold
reserved	[15:14]	RO	0x0	Reserved
HYST	[13: 8]	RW	0xC	AGC table WBRSSI hysteresis
reserved	[7: 5]	RO	0x0	Reserved
WBRSSI_SHWAY	[4]	RW	0x1	WNRSSI scaling method
WBRSSI_SH	[3: 2]	RW	0x0	WBRSSI scaling shift bits
MODE	[1: 0]	RW	0x0	AGC table WBRSSI mode [0]: mode [1]: mode2

8.3.20 AGC_IDX_TH

0x00000050			AGC table Index Threshold (0x00040302)									AGC_IDX_TH				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved											MAX				
Type	RO											RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved			MID					reserved			MIN				
Type	RO			RW					RO			RW				
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0

AGC table Index Threshold

Field Name	Bit	Type	Reset Value	Description
reserved	[31:21]	RO	0x0	Reserved
MAX	[20:16]	RW	0x4	Seek AGC index High Limit
reserved	[15:13]	RO	0x0	Reserved
MID	[12: 8]	RW	0x3	Seek AGC index Middle value
reserved	[7: 5]	RO	0x0	Reserved
MIN	[4: 0]	RW	0x2	Seek AGC index Low Limit

8.3.21 AGC_RSSI_TH

0x00000054			AGC RSSI Threshold (0x000A0028)									AGC_RSSI_TH				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved								MAX							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								MIN							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0

AGC RSSI Threshold

Field Name	Bit	Type	Reset Value	Description
reserved	[31:24]	RO	0x0	Reserved
MAX	[23:16]	RW	0xA	Seek AGC RSSI High Limit
reserved	[15: 8]	RO	0x0	Reserved
MIN	[7: 0]	RW	0x28	Seek AGC RSSI Low Limit

8.3.22 SEEK_ADPS

0x00000058			Seek Adaptive Scaling pre-demodulation (0x04280000)									SEEK_ADPS				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved				SFT				LBND							
Type	RO				RW				RW							
Reset	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Seek Adaptive Scaling pre-demodulation

Field Name	Bit	Type	Reset Value	Description
reserved	[31:28]	RO	0x0	Reserved
SFT	[27:24]	RW	0x4	Seek adaptive scaling pre-demodulation bit Shift
LBND	[23:16]	RW	0x28	Seek adaptive scaling pre-demodulation Low-Boundary
reserved	[15: 0]	RO	0x0	Reserved

8.3.23 STER_PWR

0x0000005C			FM Stereo Power Threshold (0x00000053)									STER_PWR				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	reserved							TH								
Type	RO							RW								
Reset	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1

FM Stereo Power Threshold

Field Name	Bit	Type	Reset Value	Description
reserved	[31: 9]	RO	0x0	Reserved
TH	[8: 0]	RW	0x53	FM Stereo Power Threshold

8.3.24 AGC_CTRL

0x00000060	AGC Control Register (0x09000120)											AGC_CTRL				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved			TAB_SIZE					SW_GAIN							
Type	RO			RW					RW							
Reset	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				GAIN_STEP				reserved		MTHD		reserved			
Type	RO				RW				RO		RW		RO			
Reset	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0

AGC Control Register

Field Name	Bit	Type	Reset Value	Description
reserved	[31:29]	RO	0x0	Reserved
TAB_SIZE	[28:24]	RW	0x9	AGC table size
SW_GAIN	[23:16]	RW	0x0	Software manual configure gain value when AGC is disabled.
reserved	[15:12]	RO	0x0	Reserved
GAIN_STEP	[11: 8]	RW	0x1	AGC Gain Step
reserved	[7: 6]	RO	0x0	Reserved
MTHD	[5: 4]	RW	0x2	AGC calculate method
reserved	[3: 0]	RO	0x0	Reserved

8.3.25 AGC_ITV_TH

0x00000064	AGC Interval Threshold (0x00020012)											AGC_ITV_TH				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved								MAX							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	reserved								MIN							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

AGC Interval Threshold

Field Name	Bit	Type	Reset Value	Description
reserved	[31:24]	RO	0x0	Reserved
MAX	[23:16]	RW	0x2	AGC Interval Threshold MAX value
reserved	[15: 8]	RO	0x0	Reserved
MIN	[7: 0]	RW	0x12	AGC Interval Threshold MIN value

8.3.26 AGC_ADPS0

0x00000068			AGC Adaptive Scaling pre-demodulation (0x03090008)									AGC_ADPS0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	HBND								LBND							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved												SFT_LMT			
Type	RO												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

AGC Adaptive Scaling pre-demodulation control register0

Field Name	Bit	Type	Reset Value	Description
HBND	[31:24]	RW	0x3	Pre-demodulation High Boundary
LBND	[23:16]	RW	0x9	Pre-demodulation Low Boundary
reserved	[15: 4]	RO	0x0	Reserved
SFT_LMT	[3: 0]	RW	0x8	Pre-demodulation Bit Shift Limit

8.3.27 AGC_ADPS1

0x0000006C			AGC Adaptive Scaling pre-demodulation (0x02080003)									AGC_ADPS1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	HLEV								LLEV							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved														MTHD	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Type	RO														RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

AGC Adaptive Scaling pre-demodulation control register1

Field Name	Bit	Type	Reset Value	Description
HLEV	[31:24]	RW	0x2	Pre-demodulation High Level for method not equal 0
LLEV	[23:16]	RW	0x8	Pre-demodulation Low Boundary for method not equal 0
reserved	[15: 2]	RO	0x0	Reserved
MTHD	[1: 0]	RW	0x3	Pre-demodulation adaptive scaling method

8.3.28 PDP_TH

0x00000070			Pilot Detect PowerThreshold (0x00000190)									PDP_TH				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			VAL												
Type	RO			RW												
Reset	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Pilot Detect PowerThreshold

Field Name	Bit	Type	Reset Value	Description
reserved	[31:13]	RO	0x0	Reserved
VAL	[12: 0]	RW	0x190	Pilot Detect Power Threshold

8.3.29 PDP_DEV

0x00000074			Pilot Detect Power Deviation (0x00000078)									PDP_DEV				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			VAL												
Type	RO			RW												
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Pilot Detect Power Deviation

Field Name	Bit	Type	Reset Value	Description
reserved	[31:13]	RO	0x0	Reserved
VAL	[12: 0]	RW	0x78	Pilot Detect Power Deviation

8.3.30 ADP_ST_CONF

0x00000078			Adaptive Stereo Configuration Register (0x0005001E)									ADP_ST_CONF				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved		MODE		reserved			HYS								
Type	RO		RW		RO			RW								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved							TH								
Type	RO							RW								
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0

Adaptive Stereo Configuration Register

Field Name	Bit	Type	Reset Value	Description
reserved	[31:30]	RO	0x0	Reserved
MODE	[29:28]	RW	0x0	Adaptive stereo configuration mode
reserved	[27:25]	RO	0x0	Reserved
HYS	[24:16]	RW	0x5	Stereo Hysteresis Adaptive Configuration
reserved	[15: 9]	RO	0x0	Reserved
TH	[8: 0]	RW	0x1E	Stereo Threshold Adaptive Configuration

8.3.31 ADP_LPF_CONF

0x0000007C			Adaptive LPF Configuration Register (0x00000001)									ADP_LPF_CONF				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved													VAL		
Type	RO													RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Adaptive LPF Configuration Register

Field Name	Bit	Type	Reset Value	Description
reserved	[31: 3]	RO	0x0	Reserved
VAL	[2: 0]	RW	0x1	Adaptive LPF Configuration

8.3.32 DEPHA_SCAL

0x00000080			De-emphasis scaling factor (0x00000006)									DEPHA_SCAL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved													VAL		
Type	RO													RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

De-emphasis scaling factor

Field Name	Bit	Type	Reset Value	Description
reserved	[31: 3]	RO	0x0	Reserved
VAL	[2: 0]	RW	0x6	De-emphasis scaling factor value.

8.3.33 HW_MUTE

0x00000084			Hardware mute control (0x0A070100)									HW_MUTE				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved				audio_dcrm_nbits				reserved			VOLUME_CONTROL				
Type	RO				RW				RO			RW				
Reset	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved						BASSBOOST_MODE		reserved		HIGHCUT_MODE		reserved			MND
Type	RO						RW		RO		RW		RO			RW
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Hardware mute control

Field Name	Bit	Type	Reset Value	Description
reserved	[31:28]	RO	0x0	Reserved

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

audio_dcrm_nbits	[27:24]	RW	0xA	audio_dcrm_nbits
reserved	[23:21]	RO	0x0	Reserved
VOLUME_CONTROL	[20:16]	RW	0x7	To control the volume ,5'hf highest volume
reserved	[15:10]	RO	0x0	Reserved
BASSBOOST_MODE	[9: 8]	RW	0x1	The mode of bassboost
reserved	[7: 6]	RO	0x0	Reserved
HIGHCUT_MODE	[5: 4]	RW	0x0	The mode of highcut
reserved	[3: 1]	RO	0x0	Reserved
MND	[0]	RW	0x0	Mandatory to use hardware mute function

8.3.34 SW_MUTE

0x00000088			Software mute control (0x0064006E)									SW_MUTE				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved							HBND								
Type	RO							RW								
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved							LBND								
Type	RO							RW								
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0

Software mute control

Field Name	Bit	Type	Reset Value	Description
reserved	[31:25]	RO	0x0	Reserved
HBND	[24:16]	RW	0x64	Software mute high boundary
reserved	[15: 9]	RO	0x0	Reserved
LBND	[8: 0]	RW	0x6E	Software mute low boundary

8.3.35 UPD_CTRL

0x0000008C			Update counter control registers (0x0A211000)									UPD_CTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved				STDIF_DLY				AGC_VS_RSSI				SEEK_AGC_DLY			
Type	RO				RW				RW				RW			
Reset	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	AGC_ADPS				PREDEM_DLY				SOFT_MUTE				ADP_ST			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Update counter control register

Field Name	Bit	Type	Reset Value	Description
reserved	[31:28]	RO	0x0	Reserved
STDIF_DLY	[27:24]	RW	0xA	Stereo Dif Delay
AGC_VS_RSSI	[23:20]	RW	0x2	AGC Update Counter vs RSSI
SEEK_AGC_DLY	[19:16]	RW	0x1	SEEK AGC delay
AGC_ADPS	[15:12]	RW	0x1	AGC adaptive scaling pre-demodulation update time
PREDEM_DLY	[11: 8]	RW	0x0	AGC adaptive scaling pre-demodulation delay
SOFT_MUTE	[7: 4]	RW	0x0	Softmute update counter
ADP_ST	[3: 0]	RW	0x0	Adaptive stereo configure update counter

8.3.36 AUD_BLD0

0x00000090	Audio blend control register 0 (0x0053005F)											AUD_BLD0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved							HBND								
Type	RO							RW								
Reset	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved							LBND								
Type	RO							RW								
Reset	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1

Audio blend control register 0

Field Name	Bit	Type	Reset Value	Description
reserved	[31:25]	RO	0x0	Reserved
HBND	[24:16]	RW	0x53	Audio blend high boundary
reserved	[15: 9]	RO	0x0	Reserved
LBND	[8: 0]	RW	0x5F	Audio blend low boundary

8.3.37 AUD_BLD1

0x00000094	Audio blend control register 1 (0x0057005B)											AUD_BLD1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	MODE	reserved						LEV2								
Type	RW	RO						RW								
Reset	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	1

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							LEV1								
Type	RO							RW								
Reset	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	1

Audio blend control register 1

Field Name	Bit	Type	Reset Value	Description
MODE	[31]	RW	0x0	Audio blend mode
reserved	[30:25]	RO	0x0	Reserved
LEV2	[24:16]	RW	0x57	Audio blend level 2
reserved	[15: 9]	RO	0x0	Reserved
LEV1	[8: 0]	RW	0x5B	Audio blend level 1

8.3.38 AGC_HYS

0x00000098	AGC Hysteresis control register (0x00000202)											AGC_HYS				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			THRESH					reserved			STEP				
Type	RO			RW					RO			RW				
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

AGC Hysteresis control register

Field Name	Bit	Type	Reset Value	Description
reserved	[31:13]	RO	0x0	Reserved
THRESH	[12: 8]	RW	0x2	AGC hysteresis thresh
reserved	[7: 5]	RO	0x0	Reserved
STEP	[4: 0]	RW	0x2	AGC hysteresis step

8.3.39 MONO_PWR

0x0000009C	FM Mono Power Threshold (0x019C0197)											MONO_PWR				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	reserved							TH2								
Type	RO							RW								
Reset	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							TH1								
Type	RO							RW								
Reset	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1	1

FM Mono Power Threshold

Field Name	Bit	Type	Reset Value	Description
reserved	[31:25]	RO	0x0	Reserved
TH2	[24:16]	RW	0x19C	FM Mono Power Threshold2
reserved	[15: 9]	RO	0x0	Reserved
TH1	[8: 0]	RW	0x197	FM Mono Power Threshold1

8.3.40 RF_CFG_DLY

0x000000A0			RF Config Delay (0x00000000)									RF_CFG_DLY				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved				LAN_STS_LOC				VAL							
Type	RO				RW				RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VAL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RF Configure Delay

Field Name	Bit	Type	Reset Value	Description
reserved	[31:28]	RO	0x0	Reserved
LAN_STS_LOC	[27:24]	RW	0x0	This registers is location of LNA_OVERLOAD in 16bit returned read data from RF
VAL	[23: 0]	RW	0x0	RF Configure Delay

8.3.41 AGC_TBL_STS

0x000000A4	AGC Table Status (0x00000000)	AGC_TBL_STS

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							SEL	reserved			IDX				
Type	RO							RO	RO			RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AGC Table Status

Field Name	Bit	Type	Reset Value	Description
reserved	[31: 9]	RO	0x0	Reserved
SEL	[8]	RO	0x0	AGC Table Select Status
reserved	[7: 5]	RO	0x0	reserved
IDX	[4: 0]	RO	0x0	AGC Table Index Status

8.3.42 ADP_BIT_SFT

0x000000A8			Pre-demodulation Adaptive Bit Shift (0x00000000)									ADP_BIT_SFT				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												VAL			
Type	RO												RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Pre-demodulation Adaptive Bit Shift

Field Name	Bit	Type	Reset Value	Description
reserved	[31: 4]	RO	0x0	Reserved
VAL	[3: 0]	RO	0x0	Pre-demodulation Adaptive Bit Shift

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

8.3.43 SEEK_CNT

0x000000AC			Current Seek channel Counter (0x00000000)									SEEK_CNT				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved						VAL									
Type	RO						RO									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Current Seek channel Counter

Field Name	Bit	Type	Reset Value	Description
reserved	[31:10]	RO	0x0	Reserved
VAL	[9: 0]	RO	0x0	Current Seek channel Counter

8.3.44 RSSI_STS

0x000000B0			RSSI Status Register (0x00000000)									RSSI_STS				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved												PILOT_DET		ST	SF
Type	RO												RO		RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved								RSSI							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSSI Status Register

Field Name	Bit	Type	Reset Value	Description
reserved	[31:20]	RO	0x0	Reserved
PILOT_DET	[19:18]	RO	0x0	Pilot detection status
ST	[17]	RO	0x0	Stereo Indicator. 1: Mono 0: Stereo

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SF	[16]	RO	0x0	Seek Fail Status. 0: Seek successful 1: Seek failure
reserved	[15: 8]	RO	0x0	Reserved
RSSI	[7: 0]	RO	0x0	Received Signal Strength Indicator

8.3.45 CHAN_FREQ_STS

0x000000B8			Current channel frequency (0x00000000)									CHAN_FREQ_STS				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															VAL
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Current channel frequency

Field Name	Bit	Type	Reset Value	Description
reserved	[31:17]	RO	0x0	Reserved
VAL	[16: 0]	RO	0x0	Current channel frequency status

8.3.46 FREQ_OFF_STS

0x000000BC			Frequency offset status (0x00000000)									FREQ_OFF_STS				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Frequency offset status

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
reserved	[31:16]	RO	0x0	Reserved
VAL	[15: 0]	RO	0x0	Frequency offset status

8.3.47 INPWR_STS

0x000000C0			Input power status (0x00000000)									INPWR_STS				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved							VAL								
Type	RO							RO								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Input power status

Field Name	Bit	Type	Reset Value	Description
reserved	[31: 9]	RO	0x0	Reserved
VAL	[8: 0]	RO	0x0	Input power status

8.3.48 RF_RSSI_STS

0x000000C4			RF RSSI status (0x00000000)									RF_RSSI_STS				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RF RSSI status

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

reserved	[31:16]	RO	0x0	Reserved
VAL	[15: 0]	RO	0x0	RF RSSI status value

8.3.49 NO_LPF_STS

0x000000C8			NO LPF status (0x00000000)									NO_LPF_STS				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved														VAL	
Type	RO														RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NO LPF status

Field Name	Bit	Type	Reset Value	Description
reserved	[31: 2]	RO	0x0	Reserved
VAL	[1: 0]	RO	0x0	NO LPF status value

8.3.50 SMUTE_STS

0x000000CC			Software mute status (0x00000000)									SMUTE_STS				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															k_upd
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved							ADCIF_AFIFO_OVF	reserved							VAL
Type	RO							RO	RO							RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Software mute status

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
reserved	[31:17]	RO	0x0	Reserved
k_upd	[16]	RO	0x0	k_upd
reserved	[15: 9]	RO	0x0	reserved
ADCIF_AFIFO_OVF	[8]	RO	0x0	1 means the afifo inf adc interface overflow
reserved	[7: 1]	RO	0x0	Reserved
VAL	[0]	RO	0x0	Software mute status value

8.3.51 MISC_STS

0x000000D0			WideBand RSSI status and some interface signals status (0x00000000)									MISC_STS				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved			MISC_STS					reserved					INF_STS		
Type	RO			RO					RO					RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved								VAL							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WideBand RSSI status and some interface signals status

Field Name	Bit	Type	Reset Value	Description
reserved	[31:29]	RO	0x0	Reserved
MISC_STS	[28:24]	RO	0x0	FM MISC Logic Signals, [1:0] : RF control State [2] : FIFO empty [3] : RF control ready [4] : RF control request
reserved	[23:19]	RO	0x0	Reserved
INF_STS	[18:16]	RO	0x0	FM interface Signals, [1] : FM working status, 0: idle 1:busy [2] : iis lrck [3] : iis serial data
reserved	[15: 8]	RO	0x0	Reserved
VAL	[7: 0]	RO	0x0	Wideband RSSI status value

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

8.3.52 PILOT_STS

0x000000D4			Pilot status (0x00000000)									PILOT_STS				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved			PILOT_PWR30												
Type	RO			RO												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved			PILOT_PWR31												
Type	RO			RO												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Pilot status

Field Name	Bit	Type	Reset Value	Description
reserved	[31:29]	RO	0x0	Reserved
PILOT_PWR30	[28:16]	RO	0x0	Wideband power of pilot
reserved	[15:13]	RO	0x0	Reserved
PILOT_PWR31	[12: 0]	RO	0x0	narrow band power of pilot

8.3.53 IQ_CALI_K1_ADDR

0x000000D8			Pilot status (0x00000000)									IQ_CALI_K1_ADDR				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	qklo															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	iklo															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Pilot status

Field Name	Bit	Type	Reset Value	Description
qklo	[31:16]	RO	0x0	qklo
iklo	[15: 0]	RO	0x0	iklo

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

8.3.54 IQ_CALI_K2_ADDR

0x000000DC			Pilot status (0x00000000)									IQ_CALI_K2_ADDR				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	qk2o															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ik2o															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Pilot status

Field Name	Bit	Type	Reset Value	Description
qk2o	[31:16]	RO	0x0	qk2o
ik2o	[15: 0]	RO	0x0	ik2o

8.3.55 CALI_STS_ADDR

0x000000E0			Pilot status (0x00000000)									CALI_STS_ADDR				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved			rssi_cal_done	reserved			dcoc_cal_done	dc_est_q							
Type	RO			RO	RO			RO	RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	dc_est_q				dc_est_i											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Pilot status

Field Name	Bit	Type	Reset Value	Description
reserved	[31:29]	RO	0x0	reserved
rssi_cal_done	[28]	RO	0x0	rssi_cal_done
reserved	[27:25]	RO	0x0	reserved
dcoc_cal_done	[24]	RO	0x0	dcoc_cal_done
dc_est_q	[23:12]	RO	0x0	dc_est_q
dc_est_i	[11: 0]	RO	0x0	dc_est_i

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

8.3.56 SPUR_FREQ0

0x00000100			Spur position configuration (0x00000000)									SPUR_FREQ0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	supr_freq1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	supr_freq0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Spur position configuration

Field Name	Bit	Type	Reset Value	Description
supr_freq1	[31:16]	RW	0x0	Reserved
supr_freq0	[15: 0]	RW	0x0	RF frequency where has a spur signal

8.3.57 SPUR_FREQ1

0x00000104			Spur position configuration (0x00000000)									SPUR_FREQ1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	supr_freq3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	supr_freq2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Spur position configuration

Field Name	Bit	Type	Reset Value	Description
supr_freq3	[31:16]	RW	0x0	Reserved
supr_freq2	[15: 0]	RW	0x0	RF frequency where has a spur signal

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

8.3.58 IIS_CONFIG1

0x00000108			IIS config1 register (0x003C07D0)									IIS_CONFIG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved							iis_config_div								
Type	RO							RW								
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved			iis_config_ratio												
Type	RO			RW												
Reset	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0

IIS config1 register

Field Name	Bit	Type	Reset Value	Description
reserved	[31:25]	RO	0x0	Reserved
iis_config_div	[24:16]	RW	0x3C	iis configure divider
reserved	[15:13]	RO	0x0	Reserved
iis_config_ratio	[12: 0]	RW	0x7D0	iis configure ratio

8.3.59 IIS_CONFIG2

0x0000010C			IIS config2 register (0x03C40004)									IIS_CONFIG2				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved			iis_config_sck_end												
Type	RO			RW												
Reset	0	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved			iis_config_sck_start												
Type	RO			RW												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

IIS config2 register

Field Name	Bit	Type	Reset Value	Description
reserved	[31:29]	RO	0x0	Reserved
iis_config_sck_end	[28:16]	RW	0x3C4	sck configure end
reserved	[15:13]	RO	0x0	Reserved
iis_config_sck_start	[12: 0]	RW	0x4	sck configure start

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

8.3.60 IIS_CONFIG3

0x00000110			IIS config3 register (0x00000000)									IIS_CONFIG3				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved							iis_config_ws_swap	reserved							iis_config_ws_rev
Type	RO							RW	RO							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved							iis_config_rev	reserved						iis_config_mod	
Type	RO							RW	RO						RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IIS config3 register

Field Name	Bit	Type	Reset Value	Description
reserved	[31:25]	RO	0x0	Reserved
iis_config_ws_swap	[24]	RW	0x0	iis configure ws swap
reserved	[23:17]	RO	0x0	Reserved
iis_config_ws_rev	[16]	RW	0x0	iis configure ws reverse
reserved	[15: 9]	RO	0x0	Reserved
iis_config_rev	[8]	RW	0x0	iis configure reverse
reserved	[7: 2]	RO	0x0	Reserved
iis_config_mod	[1: 0]	RW	0x0	iis configure mode

8.3.61 IIS_CONFIG4

0x00000114			IIS config4 register (0x00100004)									IIS_CONFIG4				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved									iis_config_bits_out_width						
Type	RO									RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved			iis_config_delay												
Type	RO			RW												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

IIS config4 register

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Reset Value	Description
reserved	[31:23]	RO	0x0	Reserved
iis_config_bits_out_width	[22:16]	RW	0x10	iis_config_bits_out_width
reserved	[15:13]	RO	0x0	Reserved
iis_config_delay	[12: 0]	RW	0x4	iis_config_delay

8.3.62 CIC16_CONFIG1

0x00000118			CIC16_CONFIG1 (0x0334E7FB)									CIC16_CONFIG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	COEF0_CIC16															
Type	RW															
Reset	0	0	0	0	0	0	1	1	0	0	1	1	0	1	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	COEF1_CIC16															
Type	RW															
Reset	1	1	1	0	0	1	1	1	1	1	1	1	1	0	1	1

CIC16_CONFIG1

Field Name	Bit	Type	Reset Value	Description
COEF0_CIC16	[31:16]	RW	0x334	coef0 of cic16
COEF1_CIC16	[15: 0]	RW	0xE7FB	coef1 of cic16

8.3.63 CIC16_CONFIG2

0x0000011C			CIC16_CONFIG2 (0x0003318D)									CIC16_CONFIG2				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved														COMP_EN_CIC5	COMP_EN_CIC16
Type	RO														RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	COEF2_CIC16															
Type	RW															
Reset	0	0	1	1	0	0	0	1	1	0	0	0	1	1	0	1

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

CIC16_CONFIG2

Field Name	Bit	Type	Reset Value	Description
reserved	[31:18]	RO	0x0	Reserved
COMP_EN_CIC5	[17]	RW	0x1	1 to enable the compensation filter of cic5
COMP_EN_CIC16	[16]	RW	0x1	1 to enable the compensation filter of cic16
COEF2_CIC16	[15: 0]	RW	0x318D	coef2 of cic16

8.3.64 CIC16_FREQUENCY

0x00000120			CIC16_CONFIG1 (0x00033333)									CIC16_FREQUENCY				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved									FREQUENCY						
Type	RO									RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FREQUENCY															
Type	RW															
Reset	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

CIC16_CONFIG1

Field Name	Bit	Type	Reset Value	Description
reserved	[31:23]	RO	0x0	Reserved
FREQUENCY	[22: 0]	RW	0x33333	the control frequency of cic16

8.3.65 REG_CTRL1

0x00000124			FM control register 1 (0x002DB5A0)									REG_CTRL1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved										sum_dly					
Type	RO										RW					
Reset	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	dif_nodelay	cordic_bp	super_sel	spur_dcrm_nbits				dcrm_nbits				db_comp_super_wbrssi				
Type	RW	RW	RW	RW				RW				RW				
Reset	1	0	1	1	0	1	0	1	1	0	1	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

FM control register 1

Field Name	Bit	Type	Reset Value	Description
reserved	[31:22]	RO	0x0	Reserved
sum_dly	[21:16]	RW	0x2D	means the delay of sum of L and R
dif_nodelay	[15]	RW	0x1	1 means the differ of L and R has no delay
cordic_bp	[14]	RW	0x0	bypass the cordic between cic16 and cic5
super_sel	[13]	RW	0x1	select the super wbrssi for AGC
spur_dcrm_nbits	[12: 9]	RW	0xA	spur removal control shift bits
dcrm_nbits	[8: 5]	RW	0xD	dc removal control shift bits
db_comp_super_wbrssi	[4: 0]	RW	0x0	compensate the super wbrssi in db unit

8.3.66 AMP_ADJ

0x00000128			audio_codec_control (0x00000554)									AMP_ADJ				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															subcar_neg_enb
Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved				amp_adj											
Type	RO				RW											
Reset	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0

audio_codec_control register

Field Name	Bit	Type	Reset Value	Description
reserved	[31:17]	RO	0x0	Reserved
subcar_neg_enb	[16]	RW	0x0	the enable of using the negative of subcar
reserved	[15:12]	RO	0x0	Reserved
amp_adj	[11: 0]	RW	0x554	the amplitude control of L-R

8.3.67 IQ_CALI

0x0000012C	audio_codec_control (0x00000000)	IQ_CALI

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	cal_enb	imb_cancell_enb	d_factor													
Type	RW	RW	RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	d_factor	c_factor														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

audio_codec_control register

Field Name	Bit	Type	Reset Value	Description
cal_enb	[31]	RW	0x0	cal_enb
imb_cancell_enb	[30]	RW	0x0	imb_cancell_enb
d_factor	[29:15]	RW	0x0	d_factor
c_factor	[14: 0]	RW	0x0	c_factor

8.3.68 SINE_GEN_ADDR

0x00000130			audio_codec_control (0x00000000)									SINE_GEN_ADDR				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved														sin_form_con	
Type	RO														RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sin_freq_con								reserved	sin_shift_con			reserved			sin_gen_enb
Type	RW								RO	RW			RO			RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

audio_codec_control register

Field Name	Bit	Type	Reset Value	Description
reserved	[31:18]	RO	0x0	reserved
sin_form_con	[17:16]	RW	0x0	sin_form_con
sin_freq_con	[15: 8]	RW	0x0	sin_freq_con

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

reserved	[7]	RO	0x0	reserved
sin_shift_con	[6: 4]	RW	0x0	sin_shift_con
reserved	[3: 1]	RO	0x0	reserved
sin_gen_enb	[0]	RW	0x0	sin_gen_enb

8.3.69 CALI_CTRL

0x00000134			audio_codec_control (0x00000000)									CALI_CTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved											short_ant_enb	dc0c_shift_bit			
Type	RO											RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved							dcoc_cal_enb	reserved		rc_cali_mod	rc_cali_enb	reserved			calibation_enb
Type	RO							RW	RO		RW	RW	RO			RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

audio_codec_control register

Field Name	Bit	Type	Reset Value	Description
reserved	[31:21]	RO	0x0	reserved
short_ant_enb	[20]	RW	0x0	short_ant_enb
dc0c_shift_bit	[19:16]	RW	0x0	dc0c_shift_bit
reserved	[15: 9]	RO	0x0	reserved
dcoc_cal_enb	[8]	RW	0x0	dcoc_cal_enb
reserved	[7: 6]	RO	0x0	reserved
rc_cali_mod	[5]	RW	0x0	rc_cali_mod
rc_cali_enb	[4]	RW	0x0	rc_cali_enb
reserved	[3: 1]	RO	0x0	reserved
calibation_enb	[0]	RW	0x0	calibation_enb

8.3.70 RF_CTRL1

0x0000013C			audio_codec_control (0x7FFF7FFF)									RF_CTRL1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved	rfctrl_band3_addr														
Type	RO	RW														
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserv	rfctrl_band2_addr														

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	ed															
Type	RO	RW														
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

audio_codec_control register

Field Name	Bit	Type	Reset Value	Description
reserved	[31]	RO	0x0	reserved
rfctrl_band3_addr	[30:16]	RW	0x7FFF	rfctrl_band3_addr
reserved	[15]	RO	0x0	reserved
rfctrl_band2_addr	[14: 0]	RW	0x7FFF	rfctrl_band2_addr

8.3.71 RF_CTRL2

0x00000140			**audio_codec_control (0x7FFF7FFF)**									**RF_CTRL2**				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved	rfctrl_calib_addr														
Type	RO	RW														
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved	rfctrl_band4_addr														
Type	RO	RW														
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

audio_codec_control register

Field Name	Bit	Type	Reset Value	Description
reserved	[31]	RO	0x0	reserved
rfctrl_calib_addr	[30:16]	RW	0x7FFF	rfctrl_calib_addr
reserved	[15]	RO	0x0	reserved
rfctrl_band4_addr	[14: 0]	RW	0x7FFF	rfctrl_band4_addr

8.3.72 RF_CTRL3

0x00000144			**audio_codec_control (0x00007FFF)**									**RF_CTRL3**				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	short_ant_comp															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rfctrl_shortant_addr														
Type	RO	RW														
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

audio_codec_control register

Field Name	Bit	Type	Reset Value	Description
short_ant_comp	[31:16]	RW	0x0	short_ant_comp
reserved	[15]	RO	0x0	reserved
rfctrl_shortant_addr	[14: 0]	RW	0x7FFF	rfctrl_shortant_addr

8.3.73 SOFTMUTE0

0x00000148				audio_codec_control (0x00000040)							SOFTMUTE0				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				status_soft_mute0		smute_lr_mux		smute_abs_alpha				smute_lr_mode		smute_mode	smute_en
Type	RO				RO		RW		RW				RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

audio_codec_control register

Field Name	Bit	Type	Reset Value	Description
reserved	[31:12]	RO	0x0	Reserved
status_soft_mute0	[11:10]	RO	0x0	status_soft_mute0
smute_lr_mux	[9: 8]	RW	0x0	smute_lr_mux
smute_abs_alpha	[7: 4]	RW	0x4	smute_abs_alpha
smute_lr_mode	[3: 2]	RW	0x0	smute_lr_mode
smute_mode	[1]	RW	0x0	smute_mode
smute_en	[0]	RW	0x0	smute_en

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

8.3.74 SOFTMUTE1

0x0000014C			audio_codec_control (0x00320064)									SOFTMUTE1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	smute_abs_lbound_l															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	smute_abs_hbound_l															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

audio_codec_control register

Field Name	Bit	Type	Reset Value	Description
smute_abs_lbound_l	[31:16]	RW	0x32	smute_abs_lbound_l
smute_abs_hbound_l	[15: 0]	RW	0x64	smute_abs_hbound_l

8.3.75 SOFTMUTE2

0x00000150			audio_codec_control (0x00320064)									SOFTMUTE2				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	smute_abs_lbound_r															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	smute_abs_hbound_r															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

audio_codec_control register

Field Name	Bit	Type	Reset Value	Description
smute_abs_lbound_r	[31:16]	RW	0x32	smute_abs_lbound_r
smute_abs_hbound_r	[15: 0]	RW	0x64	smute_abs_hbound_r

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

8.3.76 SOFTMUTE3

0x00000154			audio_codec_control (0x71807180)									SOFTMUTE3				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	smute_ramp_incr_step					smute_ramp_incr_bit										
Type	RW					RW										
Reset	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	smute_ramp_decr_step					smute_ramp_decr_bit										
Type	RW					RW										
Reset	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0

audio_codec_control register

Field Name	Bit	Type	Reset Value	Description
smute_ramp_incr_step	[31:27]	RW	0xE	smute_ramp_incr_step
smute_ramp_incr_bit	[26:16]	RW	0x180	smute_ramp_incr_bit
smute_ramp_decr_step	[15:11]	RW	0xE	smute_ramp_decr_step
smute_ramp_decr_bit	[10: 0]	RW	0x180	smute_ramp_decr_bit

8.3.77 SOFTMUTE4

0x00000158			audio_codec_control (0x40001000)									SOFTMUTE4				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	smute_ramp_decr_init															
Type	RW															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	smute_ramp_decr_min															
Type	RW															
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

audio_codec_control register

Field Name	Bit	Type	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

smute_ramp_decr_init	[31:16]	RW	0x4000	smute_ramp_decr_init
smute_ramp_decr_min	[15: 0]	RW	0x1000	smute_ramp_decr_min

8.3.78 SOFTMUTE5

0x0000015C			audio_codec_control (0x10004000)									SOFTMUTE5				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	smute_ramp_incr_init															
Type	RW															
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	smute_ramp_incr_max															
Type	RW															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

audio_codec_control register

Field Name	Bit	Type	Reset Value	Description
smute_ramp_incr_init	[31:16]	RW	0x1000	smute_ramp_incr_init
smute_ramp_incr_max	[15: 0]	RW	0x4000	smute_ramp_incr_max

8.3.79 DB_COMP

0x00000160			audio_codec_control (0x00000A04)									DB_COMP				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	db_comp_rssi								db_comp_wbrssi							
Type	RW								RW							
Reset	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0

audio_codec_control register

Field Name	Bit	Type	Reset	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

			Value	
reserved	[31:16]	RO	0x0	reserved
db_comp_rssi	[15: 8]	RW	0xA	db_comp_rssi
db_comp_wbrssi	[7: 0]	RW	0x4	db_comp_wbrssi

8.4 Application Note

A. FM Seek Flow:

1. Using SPI port, configure RF registers.
2. Configure FM registers.
3. Set FMCTL_STI to 1(seek mode).
4. Set GBLEN to 1, enable FM, then FM hardware will begin to search FM station.
5. When find a valid FM station, FM interrupt will be sent out.
6. If you want to seek next FM station, firstly, set GBLEN to 0, this operation will force FM's FSM to IDEL state, and then, repeat step3, step4.

B. FM Tune Flow:

1. Using SPI port, configure RF registers.
2. Configure FM registers.
3. Set FMCTL_STI to 2(tune mode).
4. Set CHAN to frequency which you want to receive.
5. Set GBLEN to 1, enable FM, then FM hardware will begin to search FM station.
6. When tune done, FM interrupt will be sent out.
7. If you want to tune other FM station, firstly, set GBLEN to 0 and then, repeat step3,step4 and step5.

C. Close FM

At anytime, setting GBLEN to 0 will close FM.

D. FM RDS

1. Init RDS.

FM_RDS_REG5[0]=1; // enable tracking loop

FM_RDS_REG5[1]=1; // enable phase tracking loop

FM_RDS_REG5[9]=1; // enable frequency tracking loop

FM_RDS_REG0[1:0]=3; // enable RDS

2. Check RDS status

Polling the status of RDS at the address of FM_RDS_REG7.

If the rds_exist_flag (**bit[4]**) is 1 and rds_peak_pos (**bit[3:0]**) is stable, then it means that RDS is found. Or you should continue to repeat polling this register status normally.

3. Read the RDS BUF status or wait the RDS interrupt

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Polling buf_save (**FM_RDS_REG9[21:17]**) to check whether there is enough data as required number. If yes, then read out the required number size of data from FM_RDS_BUF. If use the way of waiting for the interrupt, then check **bit[3]** of INT_STS. If fm interrupt is happened and also bit[3] is 1 , then read out conf_buf_int_size **(FM_RDS_REG11[23:20])** of data from FM_RDS_BUF.

4. Synchronization and Decode

After the driver layer receive the data from RDS_BUF, then driver layer need to decode the 32bits stream into 26 bits block firstly. Secondly, check the 26bits information word is whether one of the block A/B/C/C'/D. If none, then slide one bit and check until three continue blocks are found. Finally, do correction and decode.

Spreadtrum Confidential
Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

9 JTAG Debug

9.1 Overview

The JTAG interface on SC6531 is two wires SWD which is developed by arm used to reduce the pad cost. The SWD is connected with DAP module in chip. And DAP connects with CM4 core/ ARM9 core and AHB matrix in arm9 side. The architecture of the Debug system is shown in figure 1.

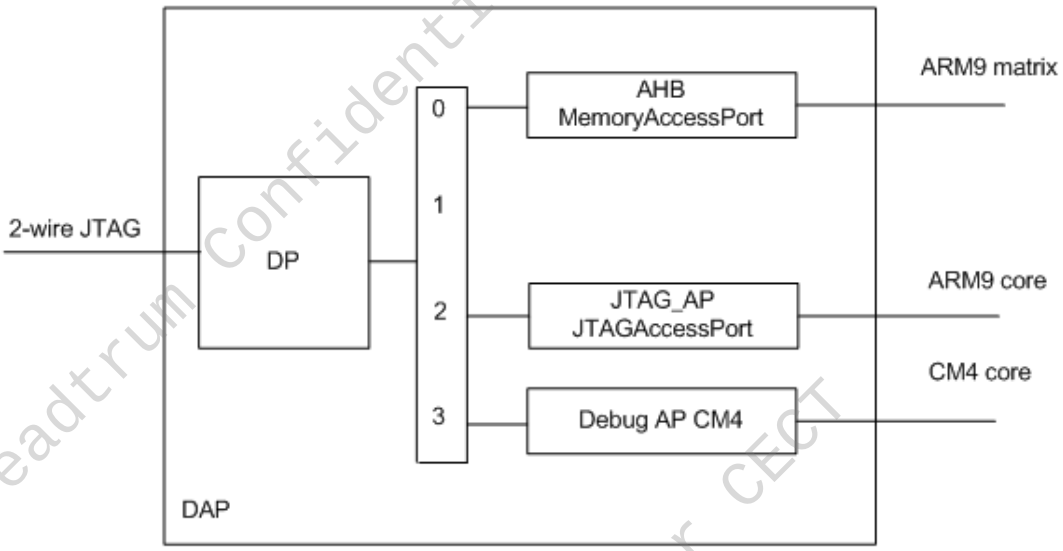


Figure 1 JTAG arch

9.2 Signal Descriptions

9.2.1 Pin Definitions

Table 9-1 JTAG Pin Definitions

Pin Name	Direction	Description
MTCK	Input	Test clock, clock input for the TAP controller and instruction and test data registers.
MTMS	Inout	Data pin

9.3 Operations

For more information about 2 wire JTAG interface, please refer to arm doc IHI0031C_debug_interface_as.pdf.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

10 Boot

10.1 Overview

SC65631MCU Support SPI Nor boot mode,func_dma boot mode and two download code modes.

1> boot modes: SPI Nor boot/func_dma boot;

2> download code modes: UART download and USB download;

SC6531 according the strappin and keypad state to judge entering boot mode or download mode.

The following describes condition to enter the different mode.

Table 15-1 boot and download mode condition

Mode name	Condition
SPI Nor boot	1) usb_dload_en strappin is high; 2) keyin0-keyout0 hasn't been pressed;
USB download	Usb_dload_en strappin is low or keyin0-keyout0 has been pressed;
UART download	1) usb_dload_en strappin is high; 2) keyin0-keyout0 hasn't been pressed; 3) UART connect to PC; 4) The software of Dloader is running
Func DMA boot	Used for production test

10.2 Boot Sequence

Romcode use max 3 step to jump to different mode.

First step: In this step, Romcode will judge if now the system is at the func_dma mode, if at func_dma mode (PTEST strappin is valid), func_dma will copy a segment code to IRAM to do remap and jump to 0 address.

Second step: in this step, romcode will identify if secure boot mode is enable. If not, romcode will enter download mode and check if the system is at USB download mode or UART download mode, or is no need to download.

1) First, romcode will check if secure boot mode. If secure boot mode is enable, romcode will boot directly. then the romcode enter USB download mode, else romcode enter to the UART download identify mode;

2) If secure boot mode is disable, romcode will enter download mode and check if the system is at USB download mode, if at USB download mode, then the romcode enter USB download mode, else romcode enter to the UART download identify mode;

3) In UART download identify mode , romcode will check if received more than 3 0x7e characters from PC, if received 3 0x7e, romcode will begin to UART download mode, else romcode will go to step 3.

Third step: In this step, romcode will begin to enter SPI Nor boot mode.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

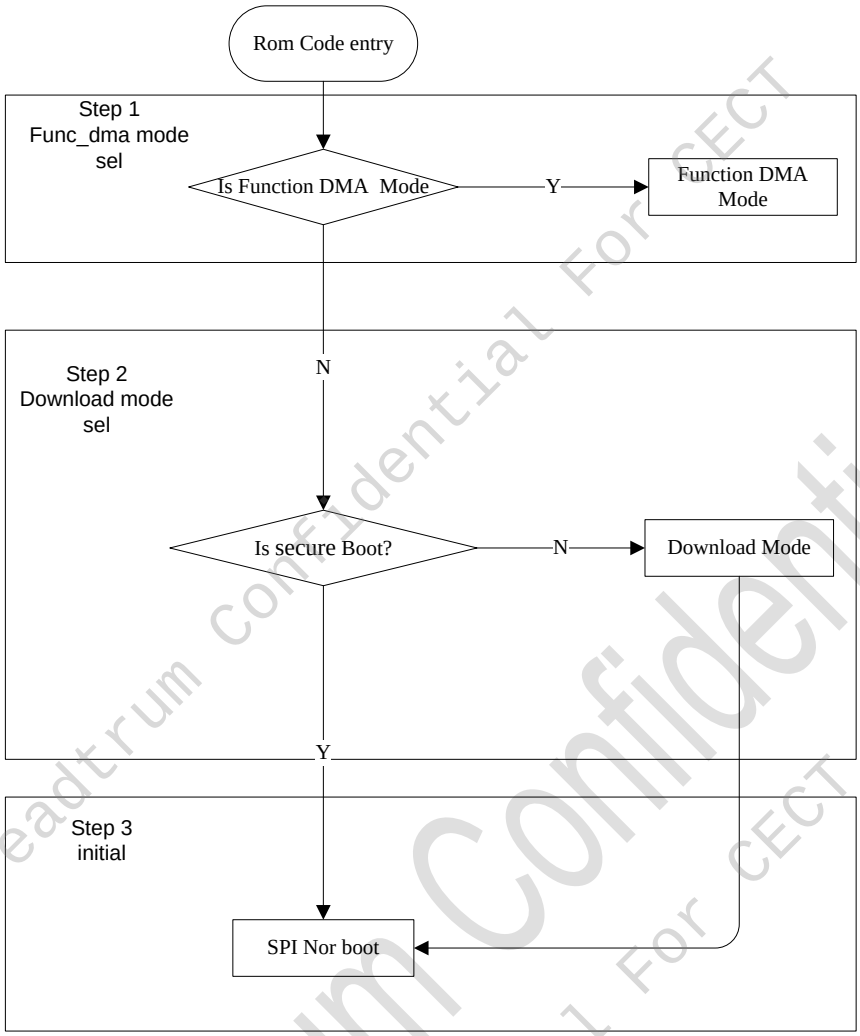


Figure 15-1 ROM code boot flow

Spreadtrum Confidential
Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

11 Audio System

11.1 Overview

AUD subsystem is the digital part of Audio codec..

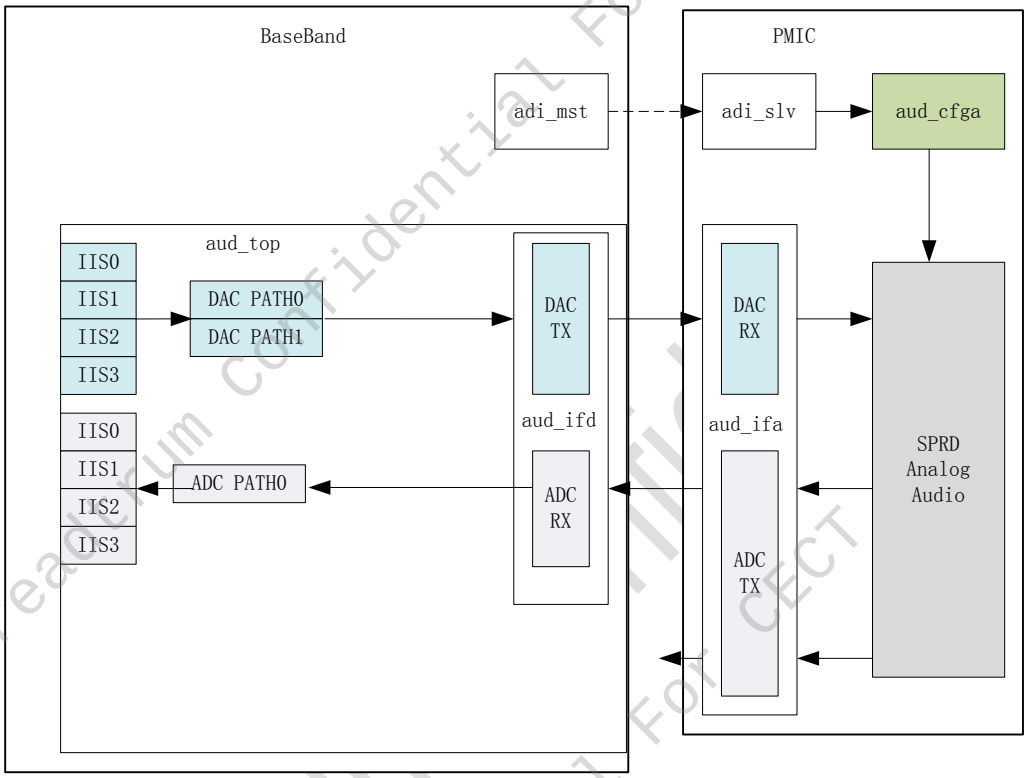


Figure 11.1-1 Audio Chip Architecture

11.2 Features

- Supports 26MHz main clock Frequency
- Supports programmable Fs for DAC : 96/48/44.1/32/24/22.05/16/12/11.025/9.6K/8 KHz
- Supports programmable Fs for ADC: 8/12/16/20/24/28/32/36/40/44/48/52 KHz
- Supports 4 iis master interfaces for DAC and ADC channel:

  dac iis0, dac iis1, dac iis2, dac iis3

  adc iis0, adc iis1, adc iis2, adc iis3
- Supports both left and right DAC channel for stereo splay, left and right ADC channel for stereo MIC
- Supports mute control for DAC channel
- Supports Audio loop path for Production
- Supports DAC loop to ADC in Digital part for debug

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

11.3 Signal Description

Signal Name	Width	I/O	Description
clk_audif	1	O	Main clock for audio interface transmitting, frequency should greater than 26MHz
aud_da_sync	1	O	Sync head for DAC serial bit stream
aud_da_d0	1	O	DAC left channel serial bit stream
aud_da_d1	1	O	DAC left channel serial bit stream
aud_ad_sync	1	I	Sync head for ADC serial bit stream
aud_ad_d0	1	I	ADC serial bit stream, include 2 channel

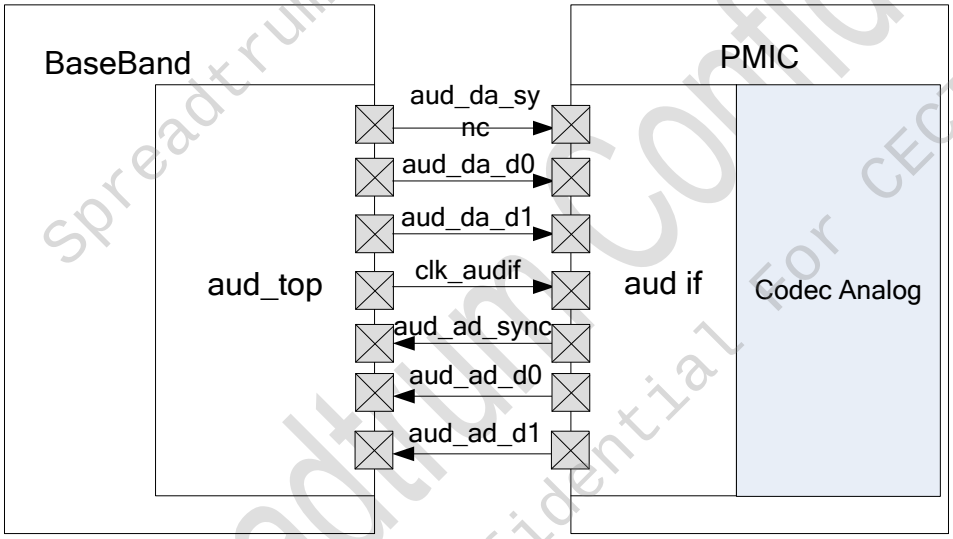


Figure 11.3-3 Audio Interface

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

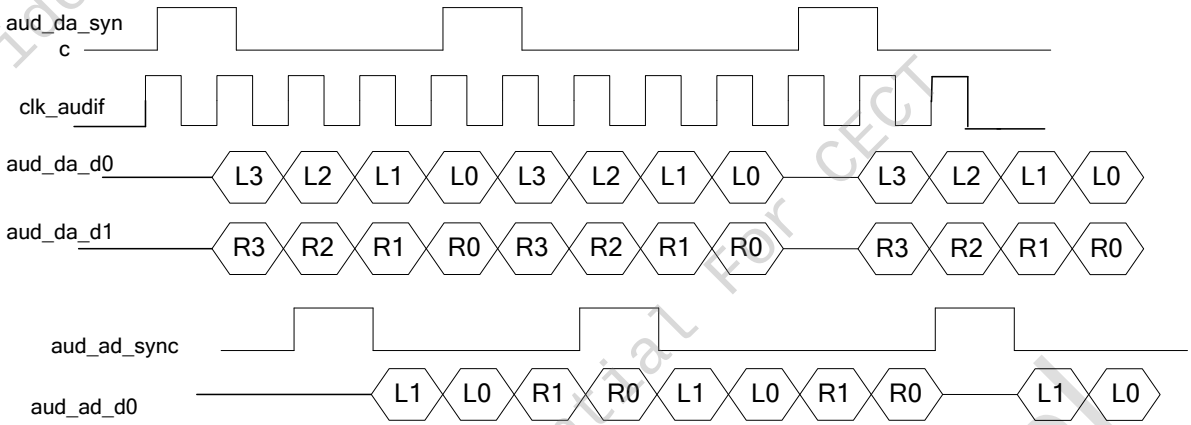
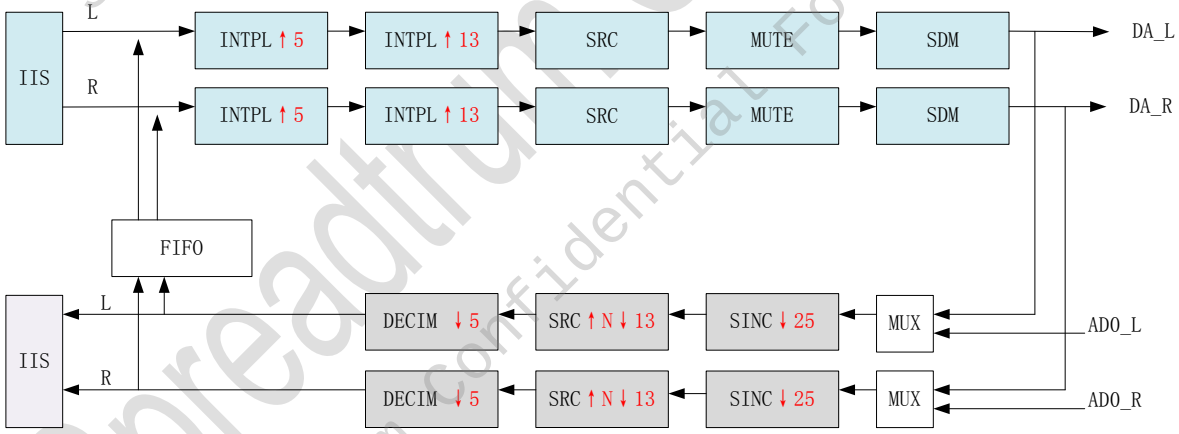


Figure 11.3-4 Audif timing diagram (6 pin mode)

11.4 Function Description

11.4.1 AUD Digital Data Path



11.4.2 AUD clock structure

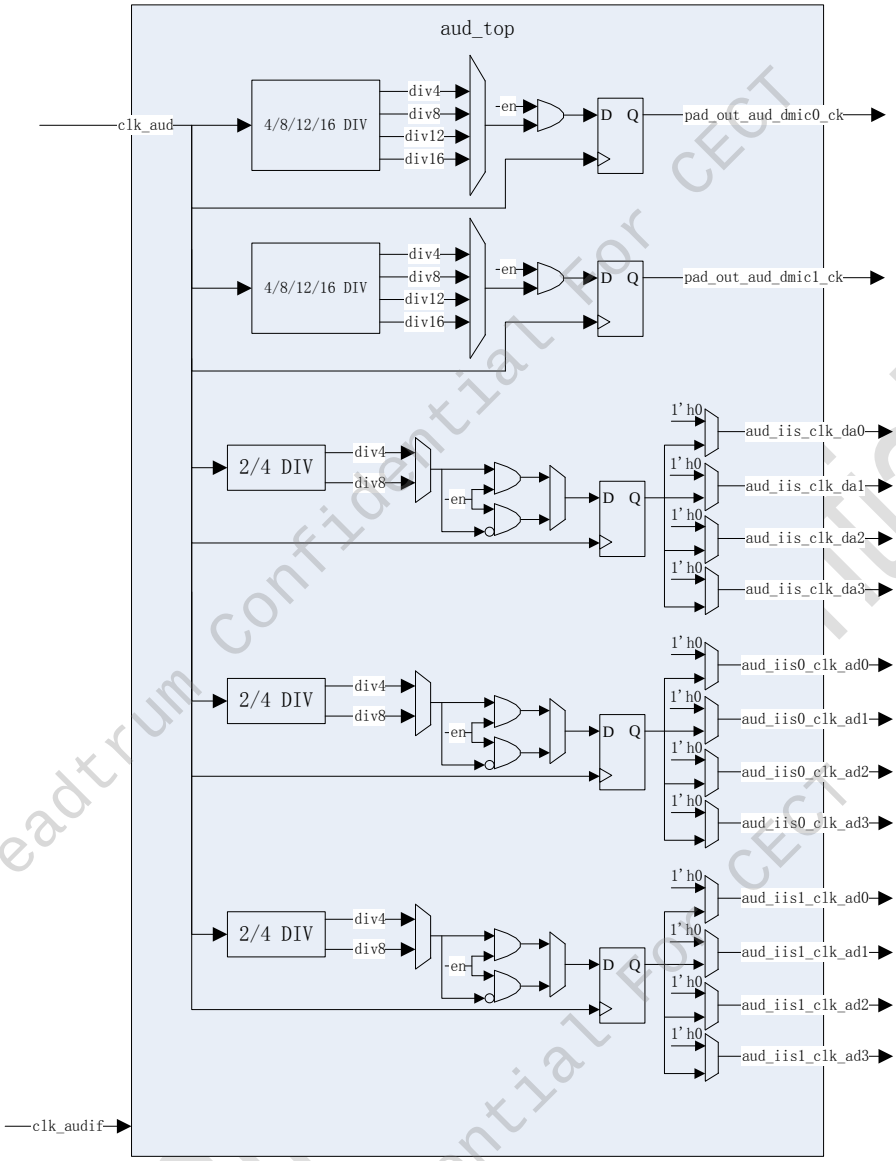
All AUD clock list in table below:

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Clock	Direction	Source	discription
clk_aud	input	External SOC	26MHz, from external SOC
aud_iis_clk_da0	output	clk_aud	2/4 div of clk_aud
aud_iis_clk_da1	output	clk_aud	2/4 div of clk_aud
aud_iis_clk_da2	output	clk_aud	2/4 div of clk_aud
aud_iis_clk_da3	output	clk_aud	2/4 div of clk_aud
aud_iis_clk_ad0	output	clk_aud	2/4 div of clk_aud
aud_iis_clk_ad1	output	clk_aud	2/4 div of clk_aud
aud_iis_clk_ad2	output	clk_aud	2/4 div of clk_aud
aud_iis_clk_ad3	output	clk_aud	2/4 div of clk_aud
clk_audif	input	external SOC	26MHz/38.4MHz/51.2MHz, connect to PAD

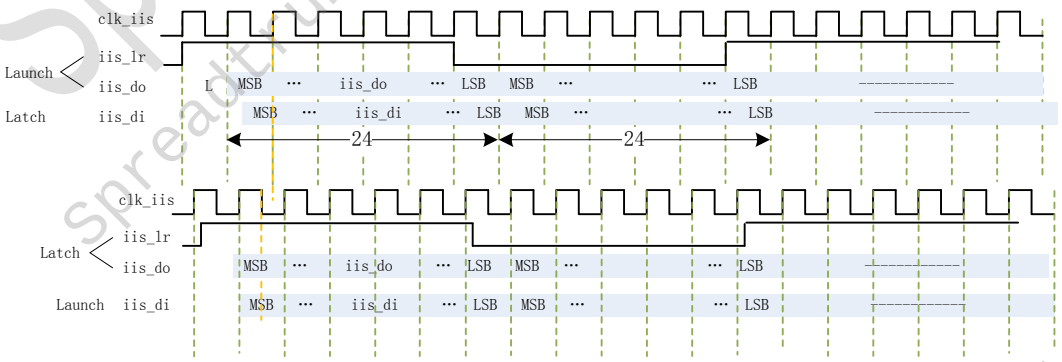
Spreadtrum Confidential
Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.



clk_aud is the main clock of AUD IP, the relationship with other clock shows in the figure above. All iis clock and pad_out_aud_dmic*_ck are generated from clk_aud. clk_audif and clk_aud could set false path between each other.

The IIS in AUD designed as IIS master. The interface timing shows in figure below, iis_do and iis_lr launch at posedge of clk_iis in IIS master, and will be captured at negedge of clk_iis in IIS slave. iis_di is launch at posedge of clk_iis in IIS slave and capture at posedge clk_iis in AUD(IIS Master).



Note: launch in green line, capture in yellow line

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

11.5 Control Registers

11.5.1 Memory map

base address:

Offset Address	Name	Description
0x0000	AUD_TOP_CTL	
0x0004	AUD_CLR	
0x0008	AUD_IIS_CTL	
0x000C	DAC_SRC_CTL	
0x0010	DAC_SDM_CTL0	
0x0014	DAC_SDM_CTL1	
0x0018	ADC_SRC_CTL	
0x001C	AUD_LOOP_TEST	
0x0020	AUD_STS0	
0x0024	AUD_INT_CLR	
0x0028	AUD_INT_EN	
0x002C	AUDIF_FIFO_CTL	
0x0030	AUD_DMIC_CTL	
0x0034	Reserved	
0x0038	DAC_SDM-DC_L	
0x003C	DAC_SDM_DC_H	
0x0040	AUDIF_CTL0	AUDIF control
0x0044	AUDIF_ADC_FIFO_STS	ADC FIFO status
0x0048	AUDIF_DAC_FIFO_STS	DAC FIFO status
0x004C	AUDIF_STS	Internal status
0x0050	AUDIF_FIFO_RAW_STS	DAC/ADC overflow status
0x0054	AUDIF_FIFO_RAW_CLR	DAC/ADC overflow status clear

11.5.2 AUD Register Descriptions

11.5.2.1 AUD_TOP_CTRL

Description : AUDIO Digital Control

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0000			AUD_TOP_CTRL(Reset 0x0)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		Reserved		Reserved	Reserved	ADC_SINC_IN_SEL		ADC_IIS_SEL		DAC_IIS_SEL		ADC_EN_R	DAC_EN_R	ADC_EN_L	DAC_EN_L
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:14]	R/W	0	
Reseved	[13:12]	R/W	0	
Reseved	[11]	R/W	0	
Reserved	[10]	R/W	0	
ADC_SINC_IN_SEL	[9:8]	R/W	0	0: adc sinc data from analog adc sdm data 1: adc sinc data from dac sdm out 2: adc sinc data from D
ADC_IIS_SEL	[7:6]	R/W	0	0: adc path select iis0 1: adc path select iis1 2: adc path select iis2 3: adc path select iis3
DAC_IIS_SEL	[5:4]	R/W	0	0: dac path select iis0 1: dac path select iis1 2: dac path select iis2 3: dac path select iis3
ADC_EN_R	[3]	R/W	0	0: adc path right channel disable 1: adc path right channel enable
DAC_EN_R	[2]	R/W	0	0: dac path right channel disable 1: dac path right channel enable
ADC_EN_L	[1]	R/W	0	0: adc path left channel disable 1: adc path left channel enable
DAC_EN_L	[0]	R/W	0	0: dac path left channel disable 1: dac path left channel enable

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

11.5.2.2 AUD_CLR

Description：AUDIO Digital Clear

0x0004			AUDI_CLR(reset 0x0)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved													Reserved	DAC_CLR	ADC_CLR
Type	RO													WO	WO	WO
Reset														0	0	0

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:3]			
Reserved	[2]	WO	0	
DAC_CLR	[1]	WO	0	1: dac path clear
ADC_CLR	[0]	WO	0	1: adc path clear

11.5.2.3 AUD_IIS_CTRL

Description：AUDIO IIS CONTROL

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0008			AUD_IIS_CTRL(reset 0x0780)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ADC_IIS_CKGATE_EN	DAC_IIS_CKGATE_EN	ADC_BCLK_POL	DAC_BCLK_POL	DAC_SAMPLE_PHASE_SEL	ADC_IOWL		DAC_IOWL		ADC_IO_MODE		DAC_IO_MODE		ADC_LR_SEL	DAC_LR_SEL	IIS_CLK DIV_MODE
Type	R/W	R/W	R/W	R/W	R/W	R/W		R/W		R/W		R/W		R/W	R/W	R/W
Reset	0	0	0	0	0	3		3		0		0		0	0	0

Field Name	Bit	R/W	Reset Value	Description
ADC_IIS_CKGATE_EN	[15]	R/W	0	DAC iis dummy clock gate en
DAC_IIS_CKGATE_EN	[14]	R/W	0	ADC iis dummy clock gate en
ADC_BCLK_POL	[13]	R/W	0	ADC BCLK polarity
DAC_BCLK_POL	[12]	R/W	0	DAC BCLK polarity
DAC_SAMPLE_PHASE_SEL	[11]	R/W	0	Sample phase for DAC IIS data 0: phase 0 1: phase 1
ADC_IOWL	[10:9]	R/W	3	0: 16 bit word length 1: 18 bit word length 2: 20 bit word length 3: 24 bit word length
DAC_IOWL	[8:7]	R/W	3	0: 16 bit word length 1: 18 bit word length 2: 20 bit word length 3: 24 bit word length
ADC_IO_MODE	[6:5]	R/W	0	0: iis mode 1: dsp mode 2: pcm mode 3: reserved
DAC_IO_MODE	[4:3]	R/W	0	0: iis mode 1: dsp mode

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				2: pcm mode 3: reserved
ADC_LR_SEL	[2]	R/W	0	0: low for left channel 1: high for right channel
DAC_LR_SEL	[1]	R/W	0	0: low for left channel 1: high for right channel
IIS_CLKDIV_MODE	[0]	R/W	0	0: iis clk div 1 1: iis clk_div 2

11.5.2.4 DAC_SRC_CTL

Description：AUDIO DAC SRC control

0x000C			DAC_SRC_CTRL(reset 0x83F0)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DAC_MUTE_EN	DAC_MUTE_CTL	DAC_MUTE_DIV1_CTL				DAC_MUTE_DIV0_CTL						DAC_FS_MODE			
Type	R/W	R/W	R/W				R/W						R/W			
Reset	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
DAC_MUTE_EN	[15]	R/W	1	0: disable mute 1: enable mute
DAC_MUTE_CTL	[14]	R/W	0	0: disable soft mute 1: enable soft mute
DAC_MUTE_DIV1_CTL	[13:10]	R/W	0	Dac mute counter1 threshold, step is controlled by counter0
DAC_MUTE_DIV0_CTL	[9:4]	R/W	63	Dac mute counter0 threshold
DAC_FS_MODE	[3:0]	R/W	0	Dac src fs frequency : 0: 96K 1: 48K 2: 44.1K 3: 32K 4: 24K 5: 22.05K 6: 16K

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				7: 12K 8: 11.025K 9: 9.6K 10: 8K

11.5.2.5 DAC_SDM_CTL0

Description：AUDIO DAC SDM control0

0x0010			DAC_SDM0_CTL(reset 0x0100)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				DAC_SDM_DODVL				DAC_SDM_DIDVL				DAC_SDM_DO		DAC_SDM_DI	
Type	RO				R/W				R/W				R/W		R/W	
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:12]	R/W	0	
DAC_SDM_DODVL	[11:8]	R/W	1	Dither out level
DAC_SDM_DIDVL	[7:4]	R/W	0	Dither in level
DAC_SDM_DO	[3:2]	R/W	0	Dither out mode
DAC_SDM_DI	[1:0]	R/W	0	Dither in mode

11.5.2.6 DAC_SDM_CTL1

Description：AUDIO DAC SDM control1

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0014			DAC_SDM0_CTRL(reset 0x0008)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						DAC_SDM_SOFT_RST_R	DAC_SDM_SOFT_RST_L	DAC_SDM_TEST							
Type	RO						R/W	R/W	R/W							
Reset							0	0	0	0	0	0	1	0	0	0

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:10]	R/W	0	
DAC_SDM_SOFT_RST_R	[9]	R/W	0	DAC right sdm soft reset
DAC_SDM_SOFT_RST_L	[8]	R/W	0	DAC left sdm soft reset
DAC_SDM_TEST	[7:0]	R/W	8'h08	Test[7]: select test out ,or sdm out Test[3]: select maping with rotation ,or no rotation Other bits: test input

11.5.2.7 ADC_SRC_CTL

Description：AUDIO ADC SRC control

0x0018			ADC_SDM0_CTRL(reset 0x0000)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								Reserved				ADC_SRC_N			
Type	RO								R/W				R/W			
Reset									0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:4]	R/W	0	
Reserved	[3:0]	R/W	0	Adc1 src upsample tap,
ADC_SRC_N	[3:0]	R/W	0	Adc src upsample tap, Sample rate = N*4

11.5.2.8 AUD_LOOP_TEST

Description：AUDIO loop test control

0x001C			AUD_LOOP_TEST(reset 0x0120)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						Reserved	LOOP_FIFO_AE_LVL			LOOP_FIFO_AF_LVL			LOOP_PATH_SEL		AUD_LOOP_TEST
Type	RO						R/W	R/W			R/W			R/W		R/W
Reset							0	1	0	0	1	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:10]	R/W	0	
Reserved	[9]	R/W	0	
LOOP_FIFO_AE_LVL	[8:6]	R/W	4	Audio loop fifo empty watermark
LOOP_FIFO_AF_LVL	[5:3]	R/W	4	Audio loop fifo full watermark
LOOP_PATH_SEL	[2:1]	R/W	0	Loop_path_sel[0]: Audio loop loop fifo out left channel select, 0 : adc left channel loop to dac left channel, 1 : adc right channel loop to dac left channel Loop_path_sel[1]: Audio loop loop fifo out right channel select, 0 : adc right channel loop to dac right channel,

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

				1 : adc left channel loop to dac right channe
AUD_LOOP_TEST	[0]	R/W	0	Audio loop enable

11.5.2.9 AUD_STS0

Description：AUDIO status

0x0020	AUD_STS0(reset 0x0000)															
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										AUD_INT_MASK		AUD_INT_RAW		ST_MUTE	
Type	RO										RO		RO		RO	
Reset											0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:6]	RO	0	
AUD_INT_MASK	[5:4]	RO	0	Aud int status after mask
AUD_INT_RAW	[3:2]	RO	0	Aud int source status [3]: mute_done_int [2]: mute_start_int
ST_MUTE	[1:0]	RO	0	0: IDLE 1: MUTE UP 2: MUTE DONE 3: MUTE DOWN

11.5.2.10 AUD_INT_CLR

Description：AUDIO INT clear

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0024			AUD_INT_CLR(reset 0x0000)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														AUD_MUTE_DONE_INT_CLR	AUD_MUTE_START_INT_CLR
Type	RO														WO	WO
Reset															0	0

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:2]	RO	0	
AUD_MUTE_DONE_INT_CLR	[1]	WO	0	
AUD_MUTE_START_INT_CLR	[0]	WO	0	

11.5.2.11 AUD_INT_EN

Description：AUDIO INT enable

0x0028			AUD_INT_EN(reset 0x0000)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														AUD_MUTE_DONE_INT_EN	AUD_MUTE_START_INT_EN
Type	RO														R/W	R/W
Reset															0	0

Field Name	Bit	R/W	Reset Value	Description

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reserved	[15:2]	RO	0	
AUD_MUTE_DONE_INT_EN	[1]	WO	0	
AUD_MUTE_START_INT_EN	[0]	WO	0	

11.5.2.12 AUDIF_FIFO_CTL

Description：AUDIO Interface FIFO control

0x002C			ADC_FIFO_AF_LVL(reset 0x0003)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved													ADC_FIFO_AF_LVL		
Type	RO													R/W		
Reset														0	1	1

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:3]	RO	0	
ADC_FIFO_AF_LVL	[2:0]	R/W	3	AUDIF ADC fifo write domain full watermark, for debug

11.5.2.13 AUD_DMIC_CTL

Description：AUDIO ADC DMIC control

0x0030			ADC_FIFO_AF_LVL(reset 0x0000)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								Resrved	Reserved	Reserved		Reserved	ADC_DMIC_CLK_MODE		ADC_DMIC_LR_SEL
Type	RO								R/W	R/W	R/W		R/W	R/W		R/W
Reset									0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:8]	RO	0	
Reserved	[7]	R/W	0	
Reserved	[6]	R/W	0	
Reserved	[5]	R/W	0	
Reserved	[4:3]	R/W	0	
ADC_DMIC_LR_SEL	[2]	R/W	0	Dmic left or right channel select: 0: high for left 1: high for right
ADC_DMIC_CLK_MODE	[1:0]	R/W	0	0: dmic clock frequency is: 6.5MHz 1: dmic clock frequency is: 6.5/2MHz 2: dmic clock frequency is: 6.5/3MHz 3: dmic clock frequency is: 6.5/4MHz

11.5.2.14 DAC_SDM_DC_L

Description：AUDIO DAC SDM DC Low 16 bit control

0x0038			DAC_SDM_DC_L(reset 0x0000)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DAC_SDM_DC_L															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
Reserved	[31:16]	R/W	0	
DAC_SDM_DC_L	[15:0]	R/W	0	DAC sdm dc parameter low 16 bit

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

11.5.2.15 DAC_SDM_DC_H

Description：AUDIO DAC SDM DC High 8 bit control

0x003C			DAC_SDM_DC_H(reset 0x0000)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								DAC_SDM_DC_H							
Type	RO								R/W							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
Reserved	[31:8	R/W	0	
DAC_SDM_DC_H	[70]	R/W	0	DAC sdm dc parameter high 8 bit

11.5.2.16 AUDIF_CTL0_ADDR

Description：AUDIF Control status

0x0040			AUDIF_CTL0_ADDR(Reset 0x1)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved									AUDIF_5P_MODE	AD_SYNC_SEL			Reserved		
Type	RO									RW	RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	R/W	Reset Value	Description
Reserved	[31:7]	RO	25'h0	
AUDIF_5P_MODE	[6]	RW	1'h0	Audio interface pin mode control 1: 5 pins 0: 6 pins
AD_SYNC_SEL	[5:3]	RW	3'h0	Adc sync delay select: 0: 0 cycle 1: 1 cycle …
Reserved	[2:0]	RW	3'h1	Reserved

11.5.2.17 ADC_FIFO_STS

Description：ADC FIFO status

0x0044	ADC_FIFO_STS(Reset 0x0200)															
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved					ADC_FIFO_AF	ADC_FIFO_EMPTY_R	ADC_FIFO_FULL_W	ADC_FIFO_ADDR_R				ADC_FIFO_ADDR_W			
Type	RO					RO	RO	RO	RO				RO			
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
ADC_FIFO_AF	[10]	RO	1'h0	ADC FIFO almost full signal
ADC_FIFO_EMPTY_R	[9]	RO	1'h1	ADC FIFO real empty. There is no data in ADC FIFO
ADC_FIFO_FULL_W	[8]	RO	1'h0	ADC FIFO real full.
ADC_FIFO_ADDR_R	[7:4]	RO	4'h0	ADC FIFO read address
ADC_FIFO_ADDR_W	[3:0]	RO	4'h0	ADC FIFO write address

11.5.2.18 DAC_FIFO_STS

Description：ADC FIFO status

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0048			DAC_FIFO_STS(Reset 0x0200)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved						DAC_FIFO_EMPTY_R	DAC_FIFO_FULL_W	DAC_FIFO_ADDR_R				DAC_FIFO_ADDR_W			
Type	RO						RO	RO	RO				RO			
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
DAC_FIFO_EMPTY_R	[9]	RO	1'h1	DAC FIFO real empty. There is no data in ADC FIFO
DAC_FIFO_FULL_W	[8]	RO	1'h0	DAC FIFO real full.
DAC_FIFO_ADDR_R	[7:4]	RO	3'h0	DAC FIFO read address
DAC_FIFO_ADDR_W	[3:0]	RO	3'h0	DAC FIFO write address

11.5.2.19 AUDIF_STS

Description：AUDIF internal signal status, used for debug

0x004C			AUDIF_STS(Reset 0x0)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															ADC_RX_DATA_RDY
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
Reserved	[15:1]	RO	15'h0	
ADC_RX_DATA_RDY	[0]	RO	1'h0	If "1", begin to receive data from A-die

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

11.5.2.20 AUDIF_RAW_STS

Description：FIFO exception status

0x0050	AUDIF_RAW_STS(Reset 0x02)															
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														ADC_FIFO_UNDERFL_RAW	DAC_FIFO_OVFL_RAW
Type	RO														RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
ADC_FIFO_UNDERFL_STS	1	RO	1'h0	When the ADC FIFO is underflow, this bit is set to "1". Write "1" to ADC_FIFO_UNDERFL_STS_CLR can clear this bit.
DAC_FIFO_OVFL_STS	0	RO	1'h0	When the DAC FIFO is overflow, this bit is set to "1". Write "1" to DAC_FIFO_OVERFL_STS_CLR can clear this bit.

11.5.2.21 AUDIF_RAW_STS_CLR

Description：FIFO exception status clear

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0054			AUDIF_RAW_STS_CLR(Reset 0x0)													
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved														ADC_FIFO_UNDERFL_CLR	DAC_FIFO_OVFL_CLR
Type	RO														WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field Name	Bit	R/W	Reset Value	Description
ADC_FIFO_UNDERFL_CLR	1	WO	1'h0	Write "1" to this bit will clear ADC_FIFO_UNDERFL_STS bit.
DAC_FIFO_OVFL_CLR	0	WO	1'h0	Write "1" to this bit will clear DAC_FIFO_OVFL_STS bit.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

12 PMU (Power Management Unit)

12.1 Overview

SC6531 integrated power management unit (PMU) supports direct connection to battery, which means all supply voltages and current sources are generated on-chip with integrated linear low dropout (LDO) voltage regulators, Charger driver, LED drivers, etc. The inputs of these blocks are from the battery.

PMU contains the following blocks:

- 14 external LDOs, 1 internal LDOs for audio, 1 LDO for back up
- Battery charger, which can be used with lithium ion batteries.
- Aux ADC for detecting or calibrating parameters of the PMIC
- Under/UP Voltage Lock-out Protection
- Over Temperature Protection
- Band-gap
- Power-on reset generator
- LED drivers, vibrator driver

The integrated power management unit also provides sophisticated controls of system startup, including start-up with discharged batteries, trickle charging and system reset. The flexible options of clock frequencies and switching modes allow minimizing the power consumption during the different operation phases. Current consumption in the deep sleep mode can be minimized by reducing the clock frequency to 32 kHz and switching most LDOs off for maximizing battery life.

Spreadtrum Confidential

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

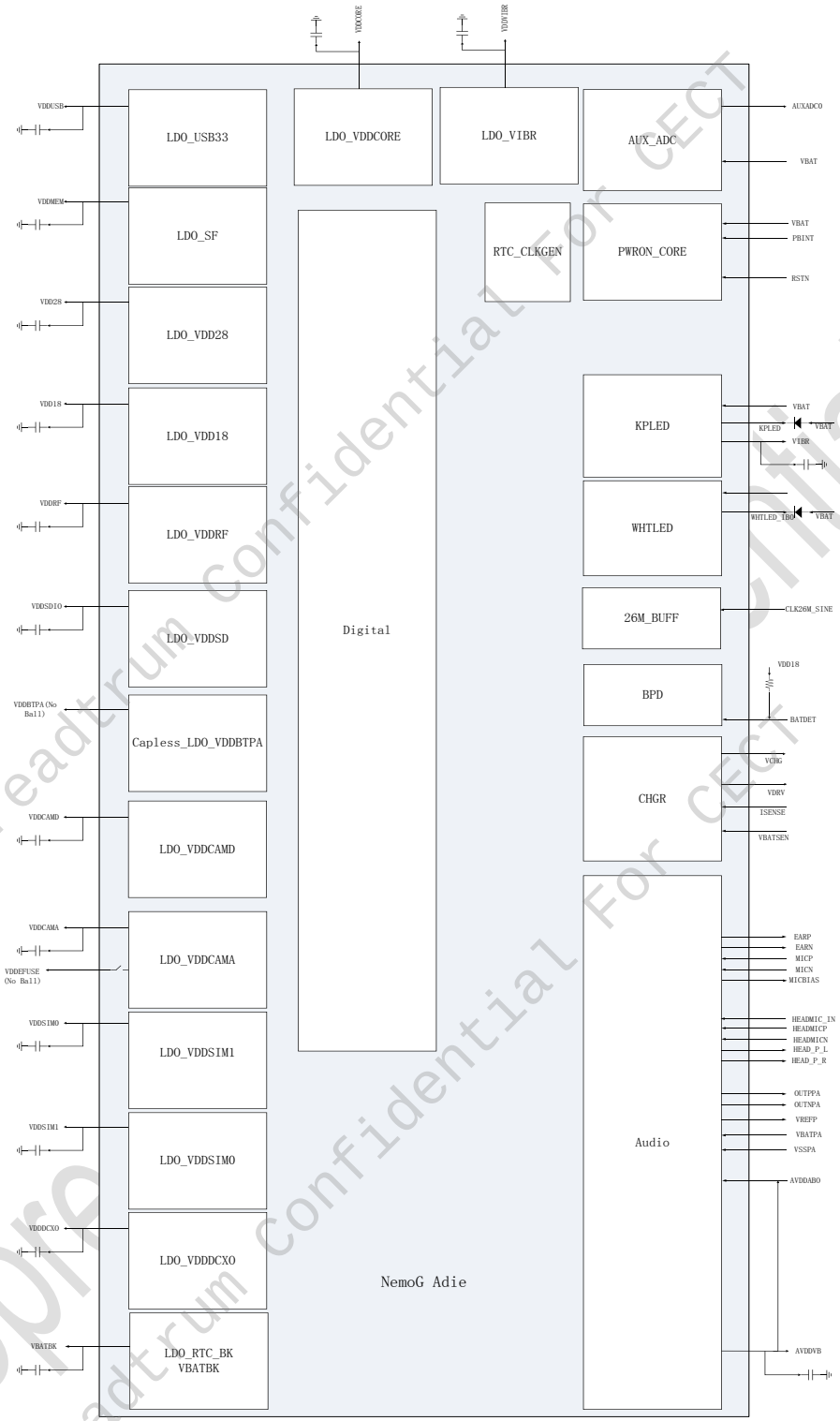


Figure 12-1 SC6531 PMU Architecture

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

12.2 LDO

SC6531 integrated low-voltage and low quiescent current low dropout regulators (LDO) for power supply and power management purposes. Some extra LDO regulators are designed for external use. All LDOs have their own power-down control signals. External tantalum or MLCC ceramic capacitors are recommended to use with the LDOs. The brief specifications are listed below.

Default on LDO will be auto calibrated by hardware during power on,if software need to control default on LDO voltage should set LDO_XX_SW_SEL first. The LDO control mux are as below.

Table 12-1 The performance of the LDOS

Parameter	Comments	Min	Typical	Max	Unit
Small battery supply					
Status after reset	On				
Application	Supply for small battery (internal)				
VBATBK Output Voltage	00	2.45	2.6	2.75	V
	01 (default)	2.65	2.8	2.95	V
	10	2.85	3.0	3.15	V
	11	3.05	3.2	3.35	V
Output Current		10			mA
Sleep current	Vbat		12	15	uA
	Backup battery		1.5	3	uA
Digital 1.8V IO Voltage(VDD18)					
Status after reset	On				
Application	IO/ NAND Flash/PMIC digital				
Output Voltage	1.8 – 3.3V, 10mV/step, 1.8V output default.				
Output Current		150			mA
Output Accuracy		-3		3	%
Drop out Voltage	Io=Imax		500		mv
Line Regulation	Vi=3.6V-4.2V;Io=75mA;		5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=75mA;Tr=10us		15	30	mV
Load regulation	Vi=3.6V; Io=1-150mA;		25	50	mV
Load Transient Regulation	Vi=3.6V; Io=1-150mA; Co=1uF; Tr=50mA/1uS		40	60	mV
Short current limit			150	200	mA
Current limit	Vi=3.6V	300	400		mA
PSRR	F=217Hz,Io=75mA, Vbat=3.6V	50	60		dB
Tpu	Set LDO_PD from 1`b1 to 1`b0 in 1us	30	50	150	us
Tpd	Vo=0.1V (Iout=Imax/2)			2.5	ms
Isleep	Io=0mA	-	5	-	uA

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Parameter	Comments	Min	Typical	Max	Unit
Pull Down Res	LDO in OFF mode		350		ohm
Cext		0.5	1	2.2	uF
2.8V Voltage(VDD28)					
Status after reset	On				
Application	APC/AFC, sinewave buffer, EFUSE (internal)				
Output Voltage	1.8 – 3.3V, 10mV/step, 2.8V output default.				V
Output Current		150			mA
Output Accuracy		-3		3	%
Drop out Voltage	Io=Imax		500		mv
Line regulation	Vi=3.6V-4.2V;Io=75mA;		5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=75mA;Tr=10us		15	30	mV
Load regulation	Vi=3.6V; Io=1-150mA;		25	50	mV
Load Transient Regulation	Vi=3.6V; Io=1-150mA;Co=1uF; Tr=50mA/1uS		40	60	mV
Short current limit			150	200	mA
Current limit	Vi=3.6V	300	400		mA
PSRR	F=217Hz,Io=75mA, Vi=3.6V	50	60		dB
Tpu	Set LDO_PD from 1`b1 to 1`b0 in 1us	40	80	160	us
Tpd	Vo=0.1V (Iout=Imax/2)			2.5	ms
Isleep	Io=0mA	-	5	-	uA
Pull Down Res	LDO in OFF mode		350		ohm
Cext		0.5	1	2.2	uF
SD Core Voltage VDDSD					
Status after reset	Off				
Application	SD Card				
Output Voltage	1.8 – 3.3V, 10mV/step, 3.0V output default.				V
Output Current		200			mA
Output Accuracy		-3		3	%
Drop out Voltage	Io=Imax		500		mv
Line Regulation	Vi=3.6V-4.2V;Io=100mA;		5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=100mA;Tr=10us		15	30	mV
Load regulation	Vi=3.8V; Io=1-200mA;		25	50	mV
Load Transient Regulation	Vi=3.8V; Io=1-200mA; Co=2.2uF; Tr=50mA/1uS		40	60	mV
Short current limit			150	200	mA

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Parameter	Comments	Min	Typical	Max	Unit
Current limit	Vi=3.8V	450	600		mA
PSRR	F=217Hz,Io=150mA Vi=3.6V	50	60	65	dB
Tpu	Set LDO_PD from 1`b1 to 1`b0 in 1us	40	80	160	us
Tpd	Vo=0.1V (Iout=Imax/2)			2.5	ms
Isleep	Io=0mA	-	5	-	uA
Pull Down Res	LDO in OFF mode		350		ohm
Cext		0.5	1	2.2	uF
SIM0 LDO (VSIM0)					
Status after reset	Off				
Application	Supply for SIM Card				
Output Voltage	1.8 – 3.3V, 10mV/step, 1.8V output default.				V
Output Current		50			mA
Output Accuracy		-3		3	%
Drop out Voltage	Io=Imax		500		mv
Line regulation	Vi=3.6V-4.2V;Io=25mA;		5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=25mA;Tr=10us		15	30	mV
Load regulation	Vi=3.8V; Io=1-50mA;		25	50	mV
Load Transient Regulation	Vi=3.8V; Io=1-50mA;Co=1uF; Tr=50mA/1uS		40	60	mV
Short current limit			150	200	mA
Current limit	Vi=3.8V	100	200		mA
PSRR	F=217Hz,Io=25mA, Vi=3.6V	50	60		dB
Tpu	Set LDO_PD from 1`b1 to 1`b0 in 1us	30	50	150	us
Tpd	Vo=0.1V (Iout=Imax/2)			2.5	ms
Isleep	Io=0mA	-	5	-	uA
Pull Down Res	LDO in OFF mode		350		ohm
Cext		0.5	1	2.2	uF
SIM1 LDO (VSIM1)					
Status after reset	Off				
Application	Supply for SIM Card				
Output Voltage	1.8 – 3.3V, 10mV/step, 1.8V output default.				V
Output Current		50			mA
Output Accuracy		-3		3	%
Drop out Voltage	Io=Imax		500		mv
Line regulation	Vi=3.6V-4.2V;Io=25mA;		5	10	mV

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Parameter	Comments	Min	Typical	Max	Unit
Line Transient Regulation	Vi=3.6V-4.2V;Io=25mA;Tr=10us		15	30	mV
Load regulation	Vi=3.8V; Io=1-50mA;		25	50	mV
Load Transient Regulation	Vi=3.8V; Io=1-50mA;Co=1uF; Tr=50mA/1uS		40	60	mV
Short current limit			150	200	mA
Current limit	Vi=3.8V	100	200		mA
PSRR	F=217Hz,Io=25mA, Vi=3.6V	50	60		dB
Tpu	Set LDO_PD from 1`b1 to 1`b0 in 1us	30	50	150	us
Tpd	Vo=0.1V (Iout=Imax/2)			2.5	ms
Isleep	Io=0mA	-	5	-	uA
Pull Down Res	LDO in OFF mode		350		ohm
Cext		0.5	1	2.2	uF
PSRR	F=217Hz,Io=100mA, Vi=3.6V	50	60		dB
Tpu	Supply ramp from 0 to 3.6v in 10μs	30	50	100	us
Tpd	Vo=0.1V (Iout=Imax/2)	40	80	160	us
Isleep	Io=0mA	-	2.5	-	uA
Pull Down Res	LDO in OFF mode		350		ohm
Cext		1	2.2	4.7	uF
General CAMA LDO (VDDCAMA)					
Status after reset	Off				
Application	Supply for external CAM				
Output Voltage	1.8 – 3.3V, 10mV/step, 2.8V output default.				V
Output Current		150			mA
Output Accuracy		-3		3	%
Drop out Voltage	Io=Imax		500		mv
Line regulation	Vi=3.6V-4.2V;Io=75mA;		5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=75mA;Tr=10us		15	30	mV
Load regulation	Vi=3.8V; Io=1-150mA;		25	50	mV
Load Transient Regulation	Vi=3.8V; Io=1-150mA;Co=1uF; Tr=50mA/1uS		40	60	mV
Short current limit			150	200	mA
Current limit	Vi=3.8V	300	400		mA
PSRR	F=217Hz,Io=75mA, Vi=3.6V	50	60		dB
Tpu	Set LDO_PD from 1`b1 to 1`b0 in 1us	40	80	160	us

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Parameter	Comments	Min	Typical	Max	Unit
Tpd	Vo=0.1V (Iout=Imax/2)			2.5	ms
Isleep	Io=0mA	-	5	-	uA
Pull Down Res	LDO in OFF mode		350		ohm
Cext		0.5	1	2.2	uF
LDO for RF(VDDRF)					
Status after reset	On				
Application	RF/TCXO				
Output Voltage	10mV/step, 1.8V output default.				V
Output Current		250			mA
Output Accuracy		-3		3	%
Drop out Voltage	Io=Imax		500		mv
Line regulation	Vi=3.6V-4.2V;Io=125mA;		5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=125mA;Tr=10us		15	30	mV
Load regulation	Vi=3.8V; Io=1-250mA;		25	50	mV
Load Transient Regulation	Vi=3.8V; Io=1-250mA;Co=1uF; Tr=50mA/1uS		40	60	mV
Current limit	Vi=3.8V	500	600		mA
PSRR	F=217Hz,Io=125mA, Vi=3.6V	50	60		dB
Tpu	Set LDO_PD from 1`b1 to 1`b0 in 1us	40	80	160	us
Tpd	Vo=0.1V (Iout=Imax/2)			2.5	ms
Isleep	Io=0mA	-	5	-	uA
Pull Down Res	LDO in OFF mode		350		ohm
Cext		0.5	1	2.2	uF
LDO for DCXO(VDD_DCXO)					
Status after reset	On				
Application	DCXO				
Output Voltage	1.8 – 3.3V, 10mV/step, 1.8V output default.				V
Output Current		50			mA
Output Accuracy		-3		3	%
Drop out Voltage	Io=Imax		500		mv
Line regulation	Vi=3.6V-4.2V;Io=25mA;		5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=25mA;Tr=10us		15	30	mV

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Parameter	Comments	Min	Typical	Max	Unit
Load regulation	Vi=3.8V; Io=1-50mA;		25	50	mV
Load Transient Regulation	Vi=3.8V; Io=1-50mA;Co=1uF; Tr=50mA/1uS		40	60	mV
Short current limit			150	200	mA
Current limit	Vi=3.8V	100	150		mA
PSRR	F=217Hz,Io=25mA, Vi=3.6V	50	60		dB
Tpu	Set LDO_PD from 1`b1 to 1`b0 in 1us	40	80	160	us
Tpd	Vo=0.1V (Iout=Imax/2)			2.5	ms
Isleep	Io=0mA	-	5	-	uA
Pull Down Res	LDO in OFF mode		350		ohm
Cext		0.5	1	2.2	uF
LDO for Camera Core (VDDCAMD)					
Status after reset	Off				
Application	Camera core				
Output Voltage	1.5 – 3.3V, 6.25mV/step, 1.8V output default.				V
Output Current		150			mA
Output Accuracy		-3		3	%
Drop out Voltage	Io=Imax		500		mv
Line Regulation	Vi=3.6V-4.2V;Io=75mA;		5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=75mA;Tr=10us		15	30	mV
Load regulation	Vi=3.6V; Io=1-150mA;		25	50	mV
Load Transient Regulation	Vi=3.6V; Io=1-150mA; Co=1uF; Tr=50mA/1uS		40	60	mV
Short current limit			150	200	mA
Current limit	Vi=3.8V	300	400		mA
PSRR	F=217Hz,Io=75mA, Vbat=3.6V	50	60		dB
Tpu	Set LDO_PD from 1`b1 to 1`b0 in 1us	30	50	150	us
Tpd	Vo=0.1V (Iout=Imax/2)			2.5	ms
Isleep	Io=0mA	-	5	-	uA
Pull Down Res	LDO in OFF mode		350		ohm
Cext		0.5	1	2.2	uF
USB High Voltage(VDDUSB)					
Status after reset	Off				
Application	USB IP (internal)				
Output Voltage	1.8 – 3.3V, 10mV/step, 3.3V output default.				V

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Parameter	Comments	Min	Typical	Max	Unit
Output Current		50			mA
Output Accuracy		-3		3	%
Drop out Voltage	Io=Imax		500		mv
Line regulation	Vi=3.6V-4.2V;Io=25mA;		5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=25mA;Tr=10us		15	30	mV
Load regulation	Vi=3.8V; Io=1-50mA;		25	50	mV
Load Transient Regulation	Vi=3.8V; Io=1-50mA;Co=1uF; Tr=50mA/1uS		40	60	mV
Short current limit			150	200	mA
Current limit	Vi=3.8V	100	150		mA
PSRR	F=217Hz,Io=25mA, Vi=3.6V	50	60		dB
Tpu	Set LDO_PD from 1`b1 to 1`b0 in 1us	40	80	160	us
Tpd	Vo=0.1V (Iout=Imax/2)			2.5	ms
Isleep	Io=0mA	-	5	-	uA
Pull Down Res	LDO in OFF mode		350		ohm
Cext		0.5	1	2.2	uF
VIBR LDO (VIBR_OUT)					
Status after reset	Off				
Application	Voltage mode for VIBR				
Output Voltage	1.8 – 3.3V, 10mV/step, 3V output default.				V
Output Current		100			mA
Output Accuracy		-3		3	%
Drop out Voltage	Io=Imax		500		mv
Line regulation	Vi=3.6V-4.2V;Io=50mA;		5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=50mA;Tr=10us		15	30	mV
Load regulation	Vi=3.8V; Io=1-100mA;		25	50	mV
Load Transient Regulation	Vi=3.8V; Io=1-100mA;Co=1uF; Tr=50mA/1uS		40	60	mV
Short current limit			150	200	mA
Current limit	Vi=3.8V	200	300		mA
PSRR	F=217Hz,Io=50mA, Vi=3.6V	50	60		dB
Tpu	Set LDO_PD from 1`b1 to 1`b0 in 1us	40	80	160	us
Tpd	Vo=0.1V (Iout=Imax/2)			2.5	ms
Pull Down Res	LDO in OFF mode		350		ohm

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Parameter	Comments	Min	Typical	Max	Unit
Cext		0.5	1	2.2	uF
Analog Audio LDO VB Voltage(AVDDVB)(Note5)					
Status after reset	Off				
Application	VB analog/VB output (internal)				
Output Voltage	00000	2.7	2.9	3.1	V
	00100	2.8	3.0	3.2	V
	01000	2.9	3.1	3.3	V
	01100	3.0	3.2	3.4	V
	10000	3.1	3.3	3.5	V
	10100	3.2	3.4	3.6	V
	11000	3.3	3.5	3.7	V
	11100	3.4	3.6	-	V
Output Current		150			mA
Line regulation	Vi=3.6V-4.2V;Io=75mA;		5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=75mA;Tr=10us		10	20	mV
Load regulation	Vi=3.8V; Io=0-150mA;		20	40	mV
Load Transient Regulation	Vi=3.8V; Io=0-150mA;Co=1uF; Tr=50mA/1uS		25	50	mV
PSRR	F=217Hz,Io=75mA, Vi=3.6V	50	60		dB
Tpu	Set LDO_PD from 1`b1 to 1`b0 in 1us	30	50	150	us
Tpd	Vo=0.1V (Iout=Imax/2)			2.5	ms
Cext		0.5	1	2.2	uF
LDO for CORE(VDDCORE)					
Status after reset	On				
Application	RF/TCXO				
Output Voltage	10mV/step, 1.1V output default.				V
Output Current		200			mA
Output Accuracy		-3		3	%
Drop out Voltage	Io=Imax		500		mv
Line regulation	Vi=3.6V-4.2V;Io=100mA;		5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=100mA;Tr=10us		15	30	mV
Load regulation	Vi=3.8V; Io=1-200mA;		25	50	mV
Load Transient Regulation	Vi=3.8V; Io=1-200mA;Co=1uF; Tr=50mA/1uS		40	60	mV
Current limit	Vi=3.8V	400	600		mA

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Parameter	Comments	Min	Typical	Max	Unit
PSRR	F=217Hz,Io=100mA, Vi=3.6V	50	60		dB
Tpu	Set LDO_PD from 1`b1 to 1`b0 in 1us	40	80	160	us
Tpd	Vo=0.1V (Iout=Imax/2)			2.5	ms
Isleep	Io=0mA	-	5	-	uA
Pull Down Res	LDO in OFF mode		350		ohm
Cext		0.5	1	2.2	uF
SF LDO (VDDSF)					
Status after reset	On				
Application	Supply for SF Card				
Output Voltage	1.8 – 3.3V, 10mV/step, 1.8V output default.	V			
Output Current		50			mA
Output Accuracy		-3		3	%
Drop out Voltage	Io=Imax		500		mv
Line regulation	Vi=3.6V-4.2V;Io=25mA;		5	10	mV
Line Transient Regulation	Vi=3.6V-4.2V;Io=25mA;Tr=10us		15	30	mV
Load regulation	Vi=3.8V; Io=1-50mA;		25	50	mV
Load Transient Regulation	Vi=3.8V; Io=1-50mA;Co=1uF; Tr=50mA/1uS		40	60	mV
Short current limit			150	200	mA
Current limit	Vi=3.8V	100	200		mA
PSRR	F=217Hz,Io=25mA, Vi=3.6V	50	60		dB
Tpu	Set LDO_PD from 1`b1 to 1`b0 in 1us	30	50	150	us
Tpd	Vo=0.1V (Iout=Imax/2)			2.5	ms
Isleep	Io=0mA	-	5	-	uA
Pull Down Res	LDO in OFF mode		350		ohm
Cext		0.5	1	2.2	uF
PSRR	F=217Hz,Io=100mA, Vi=3.6V	50	60		dB
Tpu	Supply ramp from 0 to 3.6v in 10μs	30	50	100	us
Tpd	Vo=0.1V (Iout=Imax/2)	40	80	160	us
Isleep	Io=0mA	-	2.5	-	uA
Pull Down Res	LDO in OFF mode		350		ohm
Cext		1	2.2	4.7	uF
BTPACapless LDO (VDDBTPA)					
Status after reset	Off				

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Parameter	Comments	Min	Typical	Max	Unit
Application	Supply for BTPA				
Output Voltage	1.8 – 3.3V, 10mV/step, 1.8V output default.	V			
Output Current				45	mA
Output Accuracy		-3		3	%
Line Transient Regulation	Vi=3.6V-4.2V;Io=25mA;Tr=10us		50		mV
Load Transient Regulation	Vi=3.8V; Io=1-50mA; Tr=10mA/1uS			100	mV
PSRR	F=10KHz,Io=25mA, Vi>3.6V	30			dB
	F=217Hz,Io=25mA, Vi<3.6V	40			dB
Cext			30		pF

Note1: IO voltage 1.8V.

Note2. The PSRR listed means the worst value for all loading statuses and cover all frequency range.

Note3: In our LDO design, it does not need remote cap. But in system application, sometimes power line is very long. So IR drop and noise coupling is worse, which maybe influence performance. If this cap is removed, that means we should give a restriction to PCB layout. For example, power line should be short and parasitic resistance should be small enough.

Note4. The LDO VB is designed for audio block's power supply. For these LDOs are designed for internal power supply purpose, not for external power supply, so we do not care about the output voltage's error from the typical value, which means although the output min and max value is more than 1% error with the typical value, the audio codec can work well under these voltage supply.

The output voltage level of LDO VB will be changed with the VBAT power supply automatically. So, the output voltage level over 3.3V can be achieved. For example, if the VBAT=4.2V, the output voltage of LDO VBO will be 3.8V, if the VBAT dropped to 3.3V, the output voltage will be 2.9V. So, there will be no problem about the output voltage level.

12.3 Charger

SC6531 provides an integrated Li-ion battery charger control module. With an external PNP transistor 、 a NMOS and a current sense resistor, SC6531 can control the charging of Li-ion battery.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

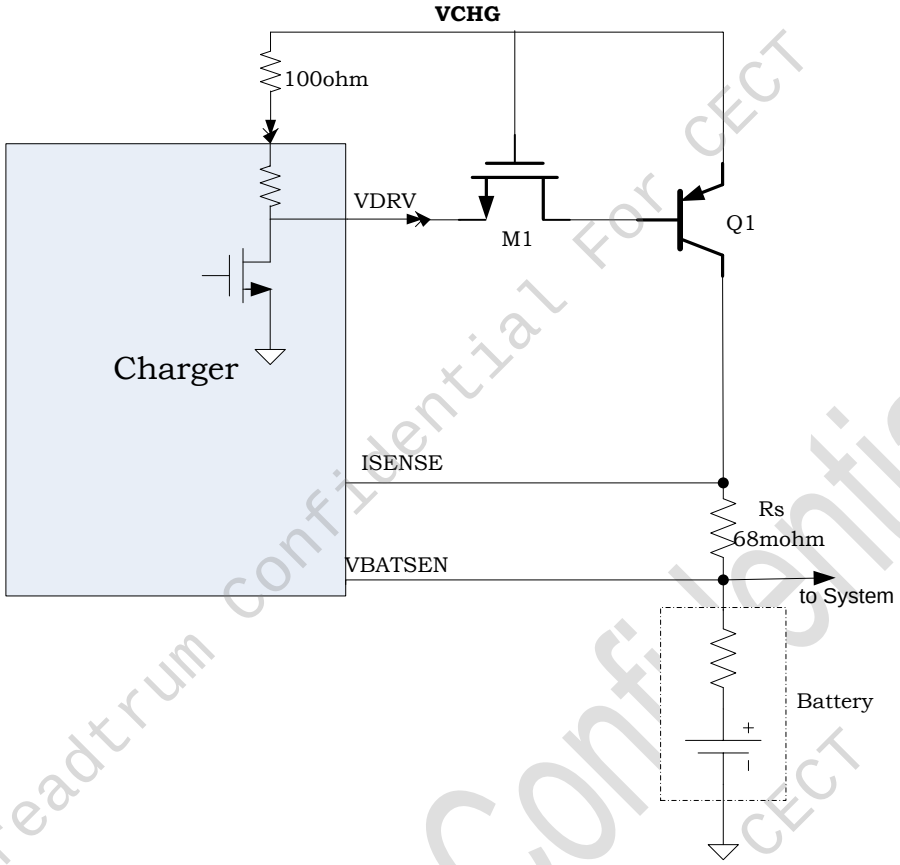


Figure 12-2 Charger application diagram, continuous mode

Note:
Rs: charge current sense resistor, 0.068 ohm. Recommended type: **KOA SL1TTE**

Table 12-2 Performance of charger circuit

Main battery charger						
Symbol	Description	Condition	Min	Typ	Max	Unit
Tol_vchg	Tolerance of VCHG	DC			28	V
VCHG	Power supply	From charger	4.5	5.0	9.2	V
Vchgovi	VCHG over voltage protection value	VCHG_OVP_V<5:0> Set level for low to high. 100mV/step	Typ *0.98	6.1 ~9.2 0.1V/ step	Typ *1.02	V
Vchgovi_hyst	VCHG over voltage protection hysteresis width			600		mV
Vuvh	Supply under voltage high threshold	VCHG low to high	4.1	4.3	4.5	V
Vuvl	Supply under voltage low threshold	VCHG high to low	3.9	4.1	4.3	V

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Vuvhys	Supply under voltage hysteresis			200		mV
Vtrickle	Trickle threshold voltage		1.95	2.05	2.15	V
Itrickle	Trickle charge current	VBAT<1.1V 1.1V<VBAT<2.05V 2.05V<VBAT<3.05 V	3 40 400	4 70 450	5 100 500	mA
Vrego	Programmable regulated output voltage	when charging finished	4.158	4.2	4.242	V
			4.257	4.3	4.73	
			4.356	4.4	4.444	
			4.455	4.5	4.545	
Vbatovi	Battery over voltage protection value	VBAT_OVP_V<3 :0 > 25mV/step	Typ *0.99	4.25 ~4.625 25mV/ step	Typ *1.01	V
Imbat	Charging current in CC mode	300mA to 2200mA to be selected by CHGR_CC_I<4 :0>	Typ. -20%	300 ~400	Typ. +20%	mA
			Typ. -10%	400 ~2300	Typ. +10%	
Istop	Charging termination current threshold when VBAT is in CV mode	Could be controlled by software		CC* 0.1		mA
Idd	Current consumption			2	3	mA
Istdby	Standby current from VCHG	When charging finished		2	3	mA
Iov	Current from VCHG to BB chip when over voltage protection	9.2V<VCHG<28V			35	mA
	Current from VCHG to battery when over voltage protection	9.2V<VCHG<28V	0	0	0.01	
Ipd	Power down leakage	Without VCHG			1	μA
Irev	Reverse leakage current	VCHG=0; VBAT=4.2V			1	μA

12.3.1 Charging Process

A charge cycle begins when the voltage at VCHG pin rises above 4.5v . If the VBAT is less than 1.1v, the charger enters active charge mode. In this mode, charger supplies approximately 10mA charge current to active the battery. If the VBAT is more than 1.1v and less than 2.05v, the charger enters small current charge mode. In this mode, charger supplies approximately 70mA charge current to bring the battery voltage up to a safe level for full current charging. When VBAT voltage rises above 2.05V, the chargers enters full current 450mA charge mode, and after software up when VBAT>3.05V, charger uses a constant-current algorithm mode. When VBAT approaches the final regulated voltage, which could be set by CHGR_END_V<1:0>, charger enters constant-voltage mode and the charge current begins to decrease. When the charge current drops to 50mA~200mA or the timer is out of the time, the charge cycle ends.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

12.3.2 Charge standby

When the charger is in CV mode and the current falls to 40% of the full current, charger produces a signal “CHGR_CV_STATUS” to digital part, and the software knows the charger has been into CV mode and starts a timer to count charge time for an hour or other. The charger will be power down by the software in the time set by the software. Or the charger will be power down by the software if the charging current is less than the termination current which could be setted by software.

In the above two circumstances, charger goes into standby mode. In standby mode, charger ceases to provide charge current to the battery.

12.3.3 Recharge Control

If charger power supply is connected, software can control for recharge after the initial charge is finished. The software will let “CHGR_PD” be “0” when the following conditions are met:

CHGON= 1, indicating the charger power supply is connected and its voltage is > 4.5 V,

The initial charge is done(hardware power down), or counting timer is out of the time (software power down), VBAT is less than some predetermined value, ex. 4.15V.

If the above conditions are met, the charger will recharge the battery until the battery is full charged.

12.3.4 Over current protection

In charge cycle, if the charge current is above 2*programmed current, the charger ceases to provide charge current to battery and enters to power down mode(hardware).

12.3.5 Over voltage protection (hardware)

In the charging process, if VBAT is charged over a value, which could be set by VBAT_OVP_V<3:0>, the charger goes into VBAT over voltage protection mode and will be power down by the hardware and produce the signal “VBAT_OVI” to be high. As long as VBAT is below the maxim value set by VBAT_OVP_V<3:0>, “VBAT_OVI” keeps low.

If VCHG is detected by the hardware over a value, which could be set by VCHG_OVP_V<5:0>, the charger goes into VCHG over voltage protection mode and will also be power down by the software and produce the signal “CHGR_OVI” to be high. And in any time, when VCHG is above 9.2V, the charger will be power down directly by the hardware. When VCHG falls into the normal range of value, the charger will go on working. There is a hysteresis value about 600mV between VCHG over voltage protection value and recovery value.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

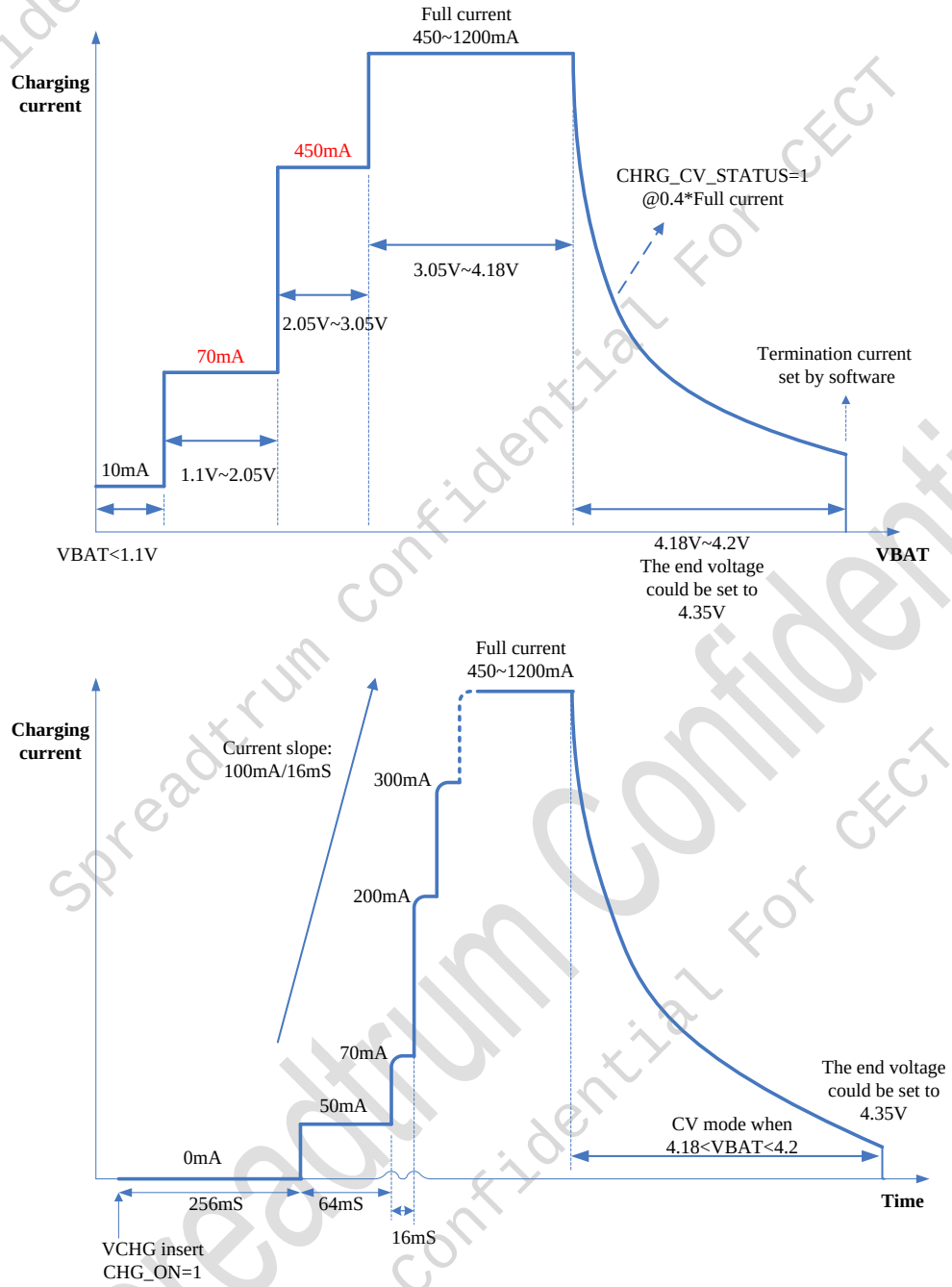


Figure 12-3 Charging current vs time vbat and time

12.3.6 Calibration table

Charging end voltage mainly depends on charger's ref. voltage, which is about +/-5 % accurate. So if +/- 1% accurate charge end voltage is required, charger must be calibrated by software setting CHGR_CV_V<5:0>. Software can calibrates charger depends on the charger's ref. voltage, which could be read through an 10bit AUXADC.

Table 12-3 Calibration table of charger

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

DAC out	delta/step	Voff	bandgap voltage		Real value to AUXADC	CHGR_CV_V[5:0]
1.13444	0.00218	0.0027	1.13174	0.964754	0.965	111111
1.13662	0.00218	0.0027	1.13392	0.966613	0.967	111110
1.1388	0.00218	0.0027	1.1361	0.968471	0.968	111101
1.14098	0.00218	0.0027	1.13828	0.970329	0.97	111100
1.14316	0.00218	0.0027	1.14046	0.972188	0.972	111011
1.14534	0.00218	0.0027	1.14264	0.974046	0.974	111010
1.14752	0.00218	0.0027	1.14482	0.975904	0.976	111001
1.1497	0.00218	0.0027	1.147	0.977763	0.978	111000
1.15188	0.00218	0.0027	1.14918	0.979621	0.98	110111
1.15406	0.00218	0.0027	1.15136	0.981479	0.981	110110
1.15624	0.00218	0.0027	1.15354	0.983338	0.983	110101
1.15842	0.00218	0.0027	1.15572	0.985196	0.985	110100
1.1606	0.00218	0.0027	1.1579	0.987054	0.987	110011
1.16278	0.00218	0.0027	1.16008	0.988913	0.989	110010
1.16496	0.00218	0.0027	1.16226	0.990771	0.991	110001
1.16714	0.00218	0.0027	1.16444	0.992629	0.993	110000
1.16932	0.00218	0.0027	1.16662	0.994488	0.994	101111
1.1715	0.00218	0.0027	1.1688	0.996346	0.996	101110
1.17368	0.00218	0.0027	1.17098	0.998204	0.998	101101
1.17586	0.00218	0.0027	1.17316	1.000063	1	101100
1.17804	0.00218	0.0027	1.17534	1.001921	1.002	101011
1.18022	0.00218	0.0027	1.17752	1.003779	1.004	101010
1.1824	0.00218	0.0027	1.1797	1.005638	1.006	101001
1.18458	0.00218	0.0027	1.18188	1.007496	1.007	101000
1.18676	0.00218	0.0027	1.18406	1.009355	1.009	100111
1.18894	0.00218	0.0027	1.18624	1.011213	1.011	100110
1.19112	0.00218	0.0027	1.18842	1.013071	1.013	100101
1.1933	0.00218	0.0027	1.1906	1.01493	1.015	100100
1.19548	0.00218	0.0027	1.19278	1.016788	1.017	100011
1.19766	0.00218	0.0027	1.19496	1.018646	1.019	100010
1.19984	0.00218	0.0027	1.19714	1.020505	1.021	100001
1.20202	0.00218	0.0027	1.19932	1.022363	1.022	100000

Spreadtrum Confidential
Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

DAC out	delta/step	Voff	bandgap voltage		Real value to AUXADC	CHGR_CV_V<5:0>
1.2042	0.00218	0.0027	1.2015	1.024221	1.024	011111
1.20638	0.00218	0.0027	1.20368	1.02608	1.026	011110
1.20856	0.00218	0.0027	1.20586	1.027938	1.028	011101
1.21074	0.00218	0.0027	1.20804	1.029796	1.03	011100
1.21292	0.00218	0.0027	1.21022	1.031655	1.032	011011
1.2151	0.00218	0.0027	1.2124	1.033513	1.034	011010
1.21728	0.00218	0.0027	1.21458	1.035371	1.035	011001
1.21946	0.00218	0.0027	1.21676	1.03723	1.037	011000
1.22164	0.00218	0.0027	1.21894	1.039088	1.039	010111
1.22382	0.00218	0.0027	1.22112	1.040946	1.041	010110
1.226	0.00218	0.0027	1.2233	1.042805	1.043	010101
1.22818	0.00218	0.0027	1.22548	1.044663	1.045	010100
1.23036	0.00218	0.0027	1.22766	1.046521	1.047	010011
1.23254	0.00218	0.0027	1.22984	1.04838	1.048	010010
1.23472	0.00218	0.0027	1.23202	1.050238	1.05	010001
1.2369	0.00218	0.0027	1.2342	1.052096	1.052	010000
1.23908	0.00218	0.0027	1.23638	1.053955	1.054	001111
1.24126	0.00218	0.0027	1.23856	1.055813	1.056	001110
1.24344	0.00218	0.0027	1.24074	1.057672	1.058	001101
1.24562	0.00218	0.0027	1.24292	1.05953	1.06	001100
1.2478	0.00218	0.0027	1.2451	1.061388	1.061	001011
1.24998	0.00218	0.0027	1.24728	1.063247	1.063	001010
1.25216	0.00218	0.0027	1.24946	1.065105	1.065	001001
1.25434	0.00218	0.0027	1.25164	1.066963	1.067	001000
1.25652	0.00218	0.0027	1.25382	1.068822	1.069	000111
1.2587	0.00218	0.0027	1.256	1.07068	1.071	000110
1.26088	0.00218	0.0027	1.25818	1.072538	1.073	000101
1.26306	0.00218	0.0027	1.26036	1.074397	1.074	000100
1.26524	0.00218	0.0027	1.26254	1.076255	1.076	000011
1.26742	0.00218	0.0027	1.26472	1.078113	1.078	000010
1.2696	0.00218	0.0027	1.2669	1.079972	1.08	000001
1.27178	0.00218	0.0027	1.26908	1.08183	1.082	000000

12.4 Charge Detector

12.4.1 Time out Detect

When VBUS is greater than certain threshold, A voltage of Vdp_src will be applied on th D+ pin after battery voltage exceed the dead voltage threshold and a timer is started at the same time. If battery voltage doesn't exceed weak voltage threshold before it times out, charger will be powered down and FSM go back idle.

12.5 LCD Backlight LED Driver

The LCD Backlight module provides four matched current sources, sinks up to 45 mA of load current to accommodate each of the White LEDs. The module uses current mirror to construct LCD

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

backlight driver. The reference current source ISET internally. It requires no charge pump. Brightness can be controlled by software. The module is in shut down mode when the whtled_pd is active.

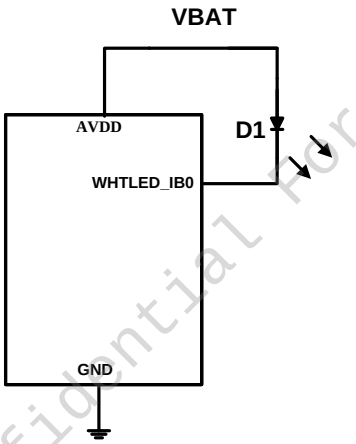


Figure 12-4 LCD backlight LED driver application

Note1: D1 in the diagram must be connected to a LED when in use, otherwise the LED driver current control bits will not be effective.

Table 12-4 Performance of LCD backlight LED driver

Parameter	Conditions/Comments	Min	Typical	Max	Unit
Status after reset	off				
Output current	0000(min current) (default)		5		mA
	0001		10		
	0010		15		
	0011		20		
	0100		25		
	0101		30		
	0110		35		
	0111		40		
	1000		45		
	1001		50		
	1010		55		
	1011		60		
	1100		65		
	1101		70		
	1110		75		
	1111		80		

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

12.6 Keypad Backlight LED Driver

The keypad backlight driver is constructed with current mirror.

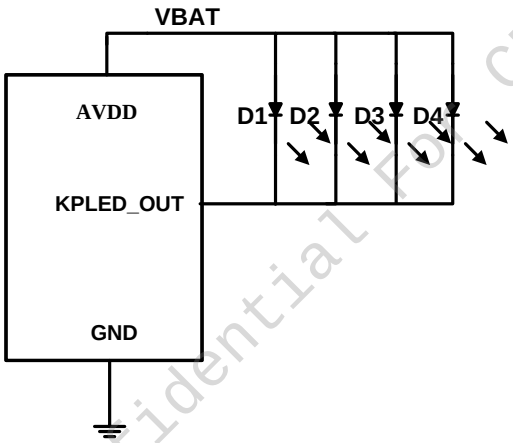


Figure 12-5 Keypad backlight LED driver application

Table 12-5 Performance of Keypad backlight LED driver

Parameter	Conditions/Comments	Min	Typical	Max	Unit
Status after reset	off				
Output current	0000(min current) (default)		0.9		mA
	0001		1.8		
	0010		2.7		
	0011		3.6		
	0100		4.5		
	0101		5.4		
	0110		6.3		
	0111		10.8		
	1000		16.2		
	1001		22.5		
	1010		29.7		
	1011		37.8		
	1100		46.8		
	1101		56.7		
	1110		67.5		
	1111		79.2		

12.7 Auxiliary Analog-to-Digital Converter (ADC)

The auxiliary ADC is a 12-bit successive approximation A/D converter. The ADC has 32 input channels, which include internal analog circuit used to monitor battery voltage, charging current and

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

voltage, and the four channels are for external usage. Four channels are specially used for touch panel. Special offset cancellation is applied in the ADC.

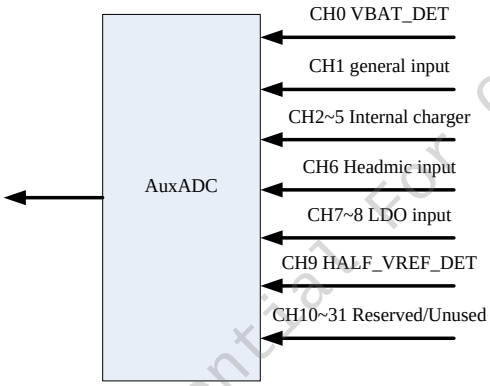


Figure 12-6 AUXADC circuit

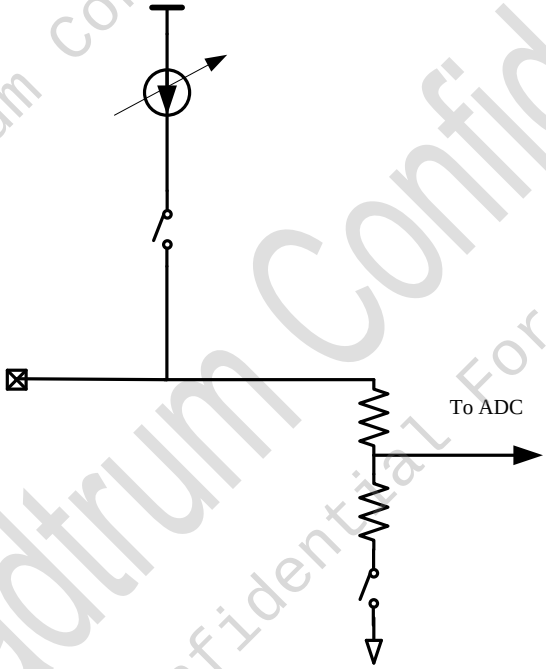


Figure 12-7 AUXADC channel 1 circuit

NOTE: User channel supports the current source detection or resistor divide detection modes.

Table 12-6 Performance of the Auxiliary ADC

Parameter	Conditions/Comments	Min	Typical	Max	Unit
Power supply		2.7	3	3.3	V
Resolution			12		bits
Integral non-linearity		-4		+4	LSB
Differential non-linearity		-1		+1	LSB
Analog General input range	Small range		1.2		V

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Parameter	Conditions/Comments	Min	Typical	Max	Unit
	Large range		3		V
Conversion time				15	μs

12.8 UVLO

The UVLO (Under Voltage Lockout) function prevents startup when initial voltage of the main battery is below the 2.95 V thresholds. The UVLO circuit is used to provide more stable operation. After turning on power, the UVLO function keeps the internal circuit in the standby state until 16ms[1] after the main battery's voltage reaches the UVLO voltage, there is 3.0V, so as to reduce supply current, avoid mis-operation and prohibit PMU to work when supply is surging. If the main battery's voltage is below 2.7V or above 4.9V for longer than 2ms, the UVLO circuit will give a signal to the internal circuit that the main battery is low/high power, which need to be powered down.

A UVLO filter is designed to remove the glitch under 2ms, and 16ms recovery time is added. Once chip enters UVLO state, it draws very low quiescent current, typically < 50 uA.

Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

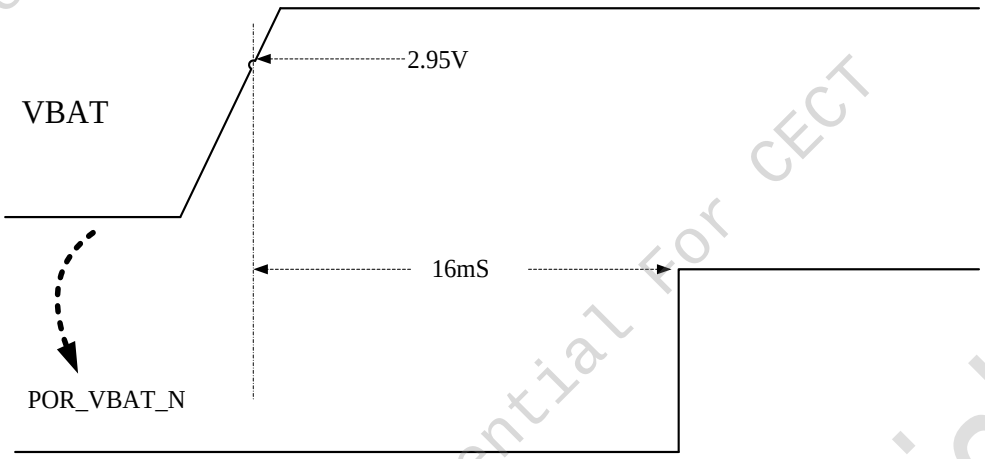


Fig.1

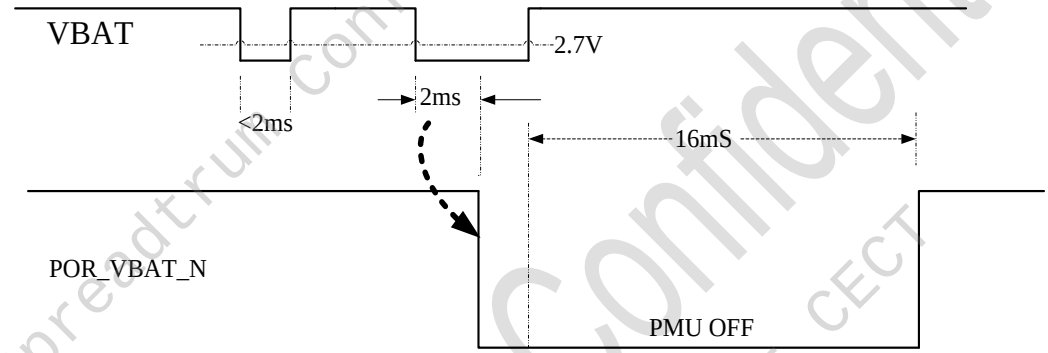


Fig.2

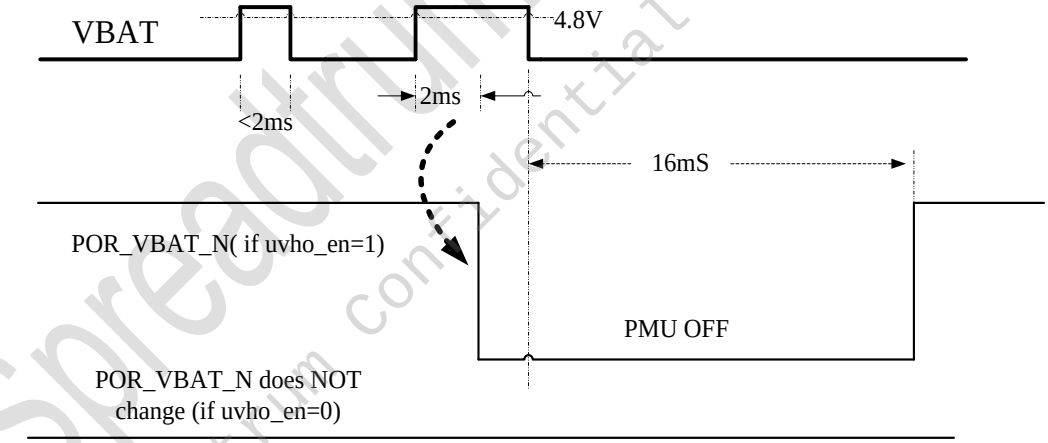


Fig.3

Figure 12-8 UVLO function

Note:

For OPT_AUTO_PWON bonding option 1,the UVLO recovery time is 128ms,and For OPT_AUTO_PWON bonding option 0,the UVO recovery time is 16ms.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

12.9 Band-Gap

The band gap block provides the first level reference for all LDO's except LDO RTC. When system is reset, it will be on.

Note:

When Band-gap is powered off, all LDOs except LDO_RTC will be disabled.

When BG is power off, OTP should Power off too. However, when BG is power on, OTP can be either power on or power off.

12.10 RTC Reset

In this PMIC RTC reset circuits is added to reset real time counter when VDDRTC is too low to keep the RTC domain running. The circuits is supplied by VDDRTC.

Table 12-7 Electrical Characteristics – RTC Reset Part

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Reset voltage of VDDRTC	When VDDRTC drops from a normal level voltage, e.x 2.8V	1.1	1.4	1.7	V
Current consumption	Average current consumption from VDDRTC=2.8V to VDDRTC=1.1V		0.3		uA

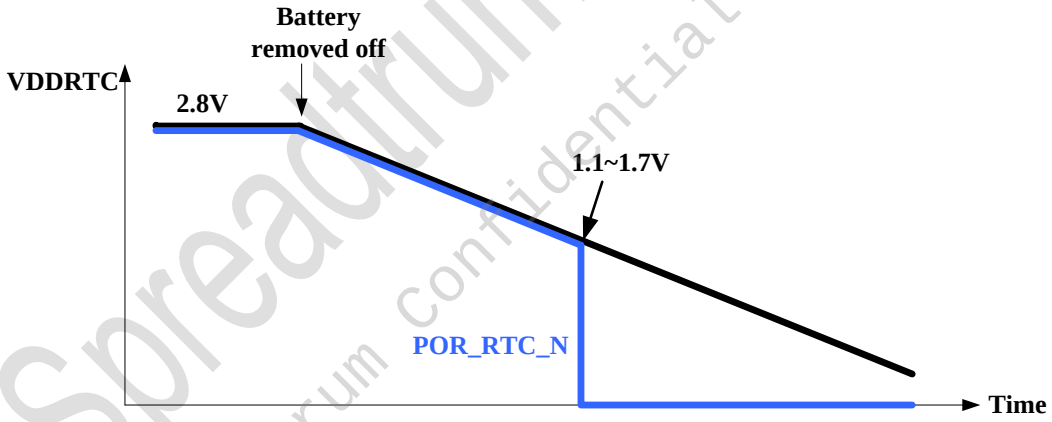


Figure 12-9 RTC reset function

12.11 Battery Presence Detection

BPD works in either voltage mode or current mode. For voltage mode, LDO VDD18 provides a 1.8V reference voltage to external NTC resistor, and for current mode, internal chip provides a accuracy current source, which's range is from 2.5uA to 160uA, to external NTC resistor.

Table 12-8 Electrical Characteristics – BPD

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Output reference voltage at BATDET_VREF	When VBAT>2.95V, system on, or VCHG>4.3V	1.7	1.8	1.9	V
Output current source to NTC resistor	When VBAT>2.95V,system on and current mode is selected	Typ-2%	2.5~160uA,	Typ+2%	
the voltage range of BATDET	When NTC resistor is added and the BPD comparator can detect the presence of a battery	0		1.1	V

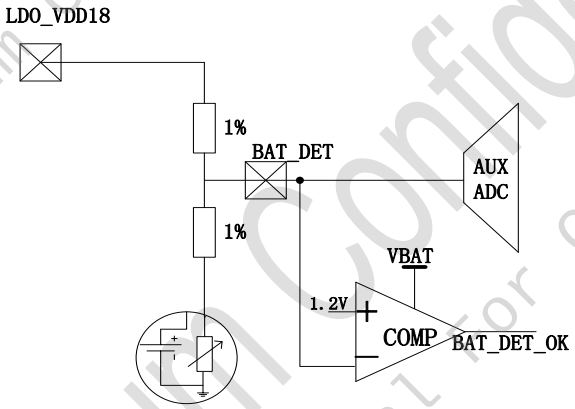


Figure 12-10 1.8V reference voltage mode

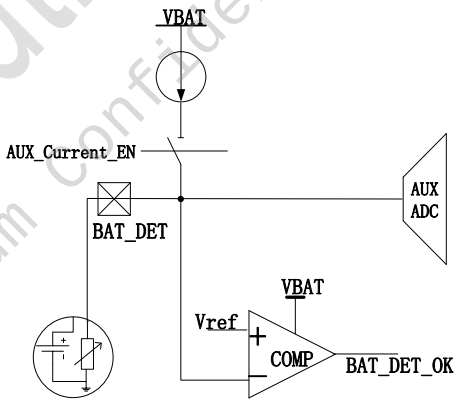


Figure 12-11Current source mode

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

12.12 Power on Control

12.12.1 Power on Procedure

12.12.1.1 Introduction

Baseband chip will be powered on by following three ways when the battery voltage is in normal state(2.95V<VBAT<4.8 V).

- Pulling power key low(user push power key)
- Valid charger plug-in
- RTC alarm expires

Whenever either one of power key, charger plug-in and RTC alarm actives in power-off state, Baseband chip will start the power on sequence as follows. That will turn on BANDGAP，VDDCORE，VDD18，VDDDCXO，VDDRF，VDD28, VDDSF, VDDUSB during power on reset active stage. And the microprocessor will start in nearly 13ms after PWR_RESET_N goes high.

Spreadtrum Confidential
Spreadtrum Confidential For CECT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

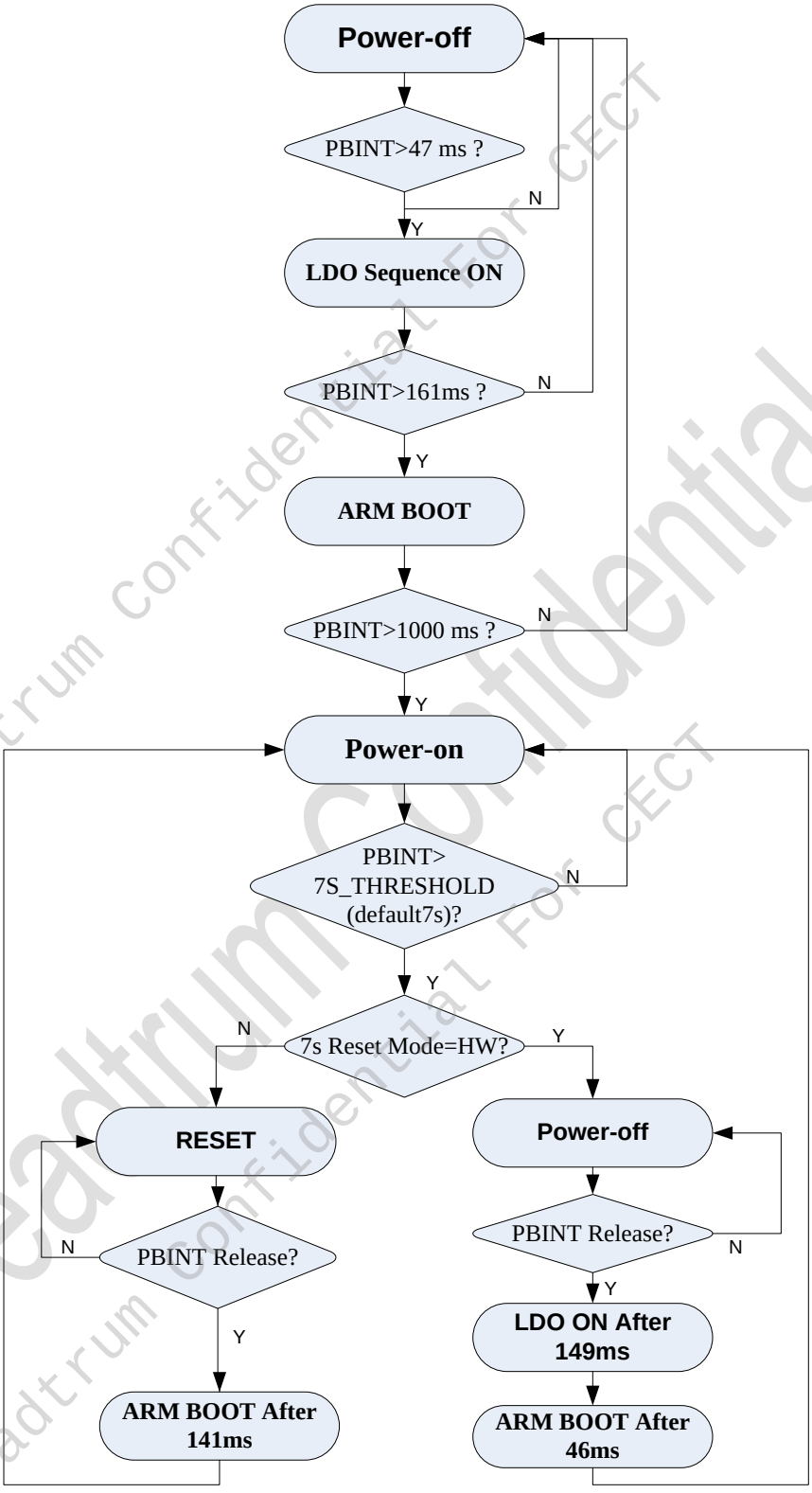
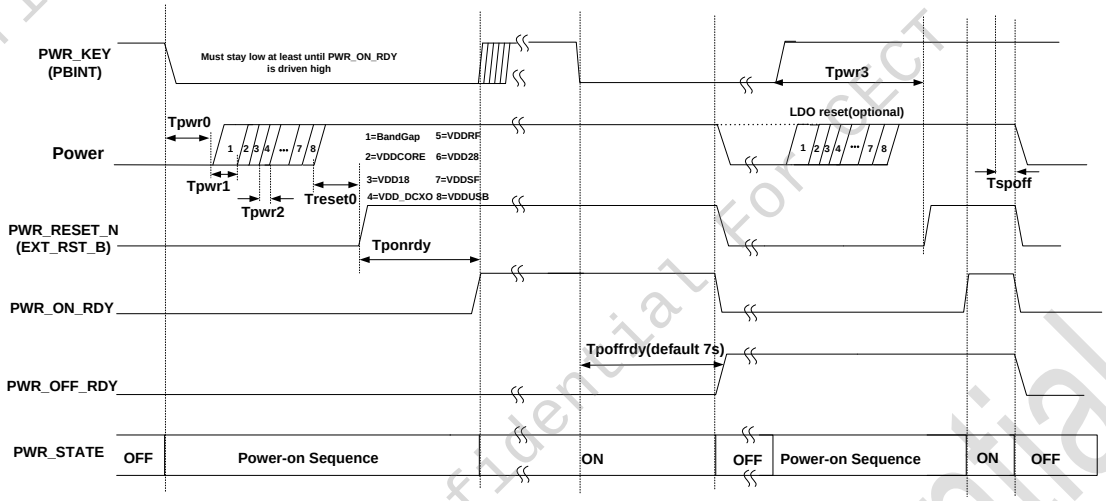


Figure 12-12 Power Button Power-on Progress

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

12.12.1.2 Timing



Integrated 7s reset circuit supports below two mode by SW select:

–Reset PMU together

–Reset ARM core only

Figure 12-13 Power-on/off Sequence by Pressing Power Button

Table 12-9 Power-on timing parameter

Parameter	Comments	Min	Typ	Max	Unit
Sequence time intervals					
Tpwr0	Power-on event to BG on	35	120	287	ms
Tpwr1	BG on to first Power LDOCORE on	5	16	41	ms
Tpwr2	Delay between LDO turn-on	80	244	640	us
Tpwr3	PWR_KEY = H to PWR_ON_RESET = H	64	200	512	ms
Treset0	Last LDO on to PWR_ON_RESET = H	15	48	123	ms
Tponrdy	Power-on ready waiting time		852		ms
Tpoffrdy	Power-off ready waiting time(configurable)		7070		ms
Tspoff	Software power-off delay time		23		ms
Power key delay	De-bounce		47		ms

Note: 1), Typical timing parameter is calculated based on accurate 32.768K clock.

2), Tpwr0/1, Tponrdy, Tpoffrdy and Tspoff could not be measured outside since they are related to internal signals.

3), Tpwr3 can be only measured in the HW long reset mode.

4), Tponrdy, Tpoffrdy and Tspoff depends on different baseband chip.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

12.12.2 Power on Sequence

12.12.2.1 Power on with Initial VBAT

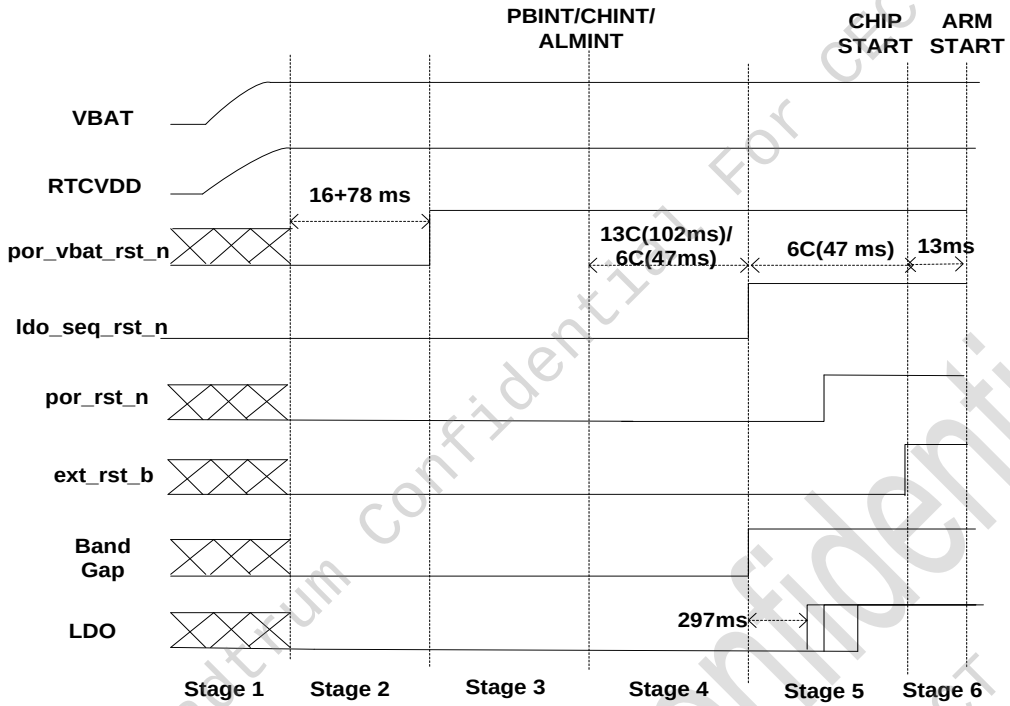


Figure 12-14 Power on with initial VBAT

12.12.2.2 Power on with Stable VBAT

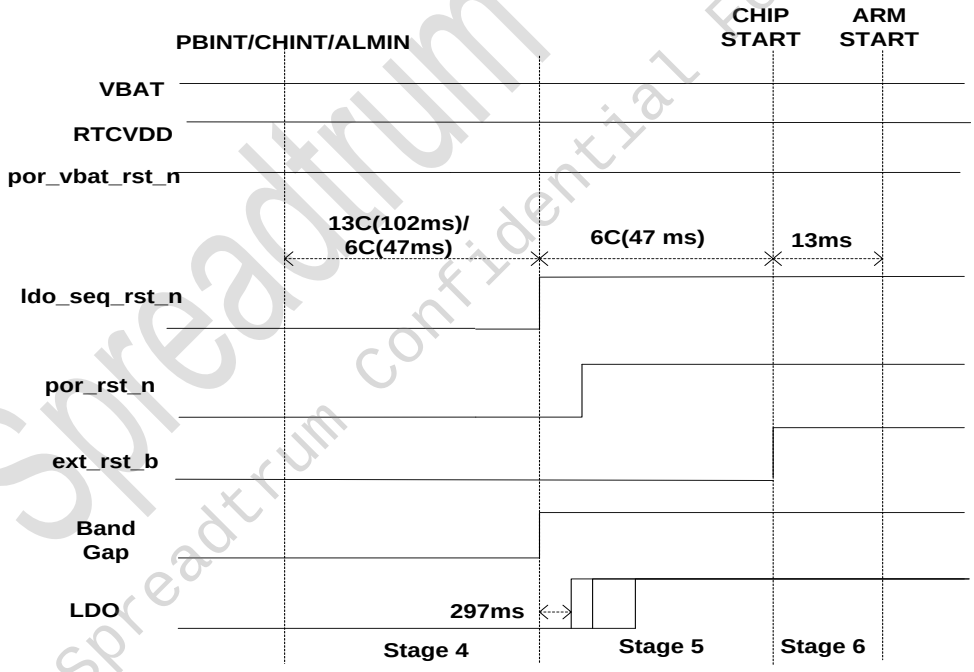


Figure 12-15 Power on with Stable VBAT

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

12.12.2.3 Power on detail sequence between bandgap and LDO/BUCKS

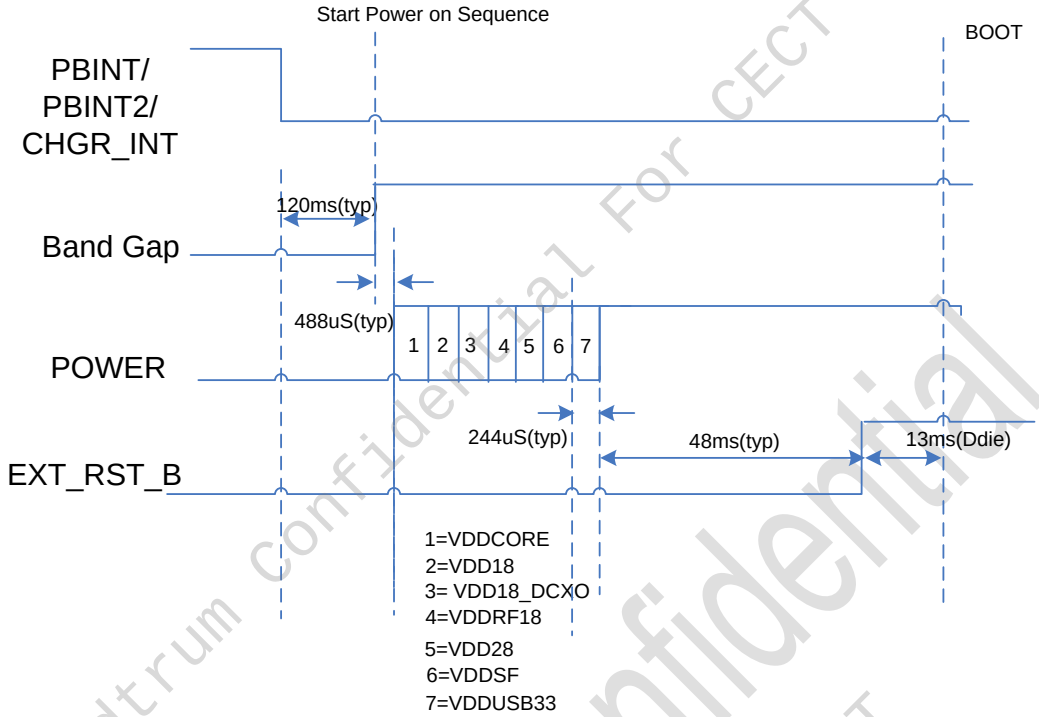


Figure 12-16 Power on detail sequence

12.12.3 Global Reset

There are several ways to generate a global reset to reboot except power-on reset. All the power rails will be reset to default status at the same time.

12.12.3.1 External Pin Reset

A dedicated external pin is implemented to reset global chip. This reset could only work in power-on mode.

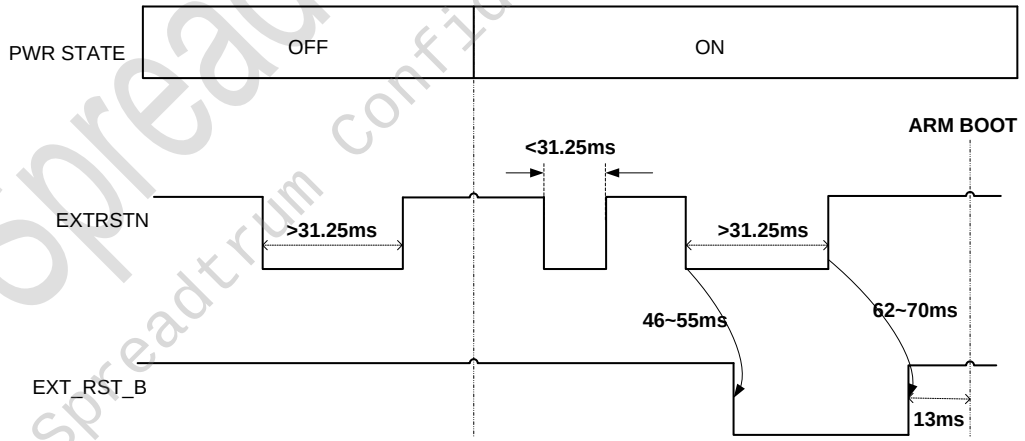


Figure 12-17 External Pin Reset

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

12.12.3.2 VBAT Monitor Reset

The VBAT monitoring circuit of UVLO and UVHO is designed to do the supervision of system supply. Global reset will be triggered once VBAT voltage is abnormal

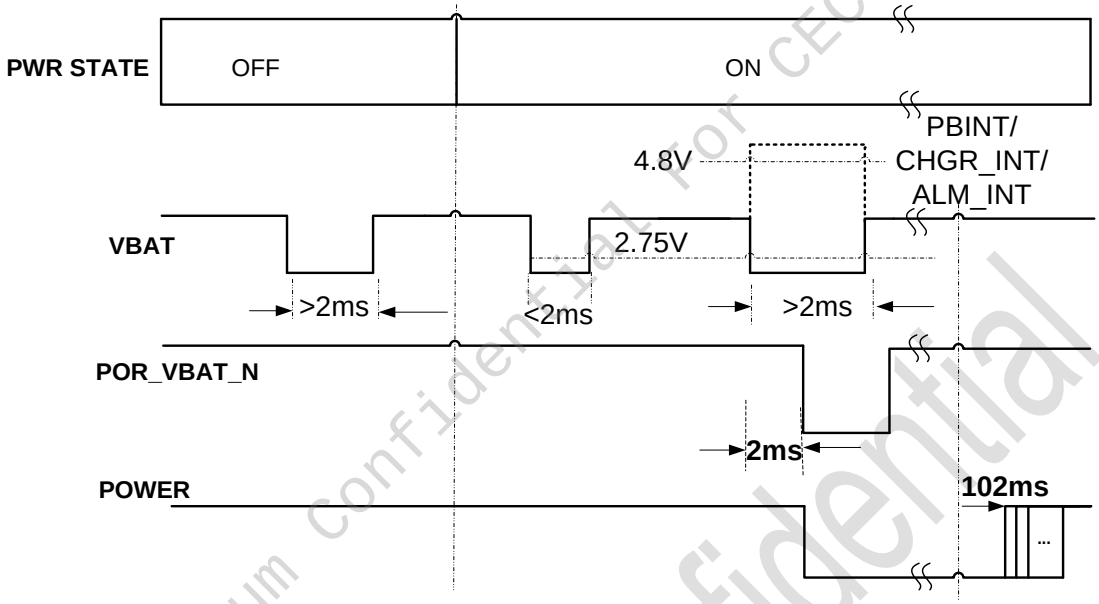


Figure 12-18 VBAT Monitor Reset

12.12.3.3 Watchdog Reset

A watchdog is designed to trigger global reset once software falls into unknown state.

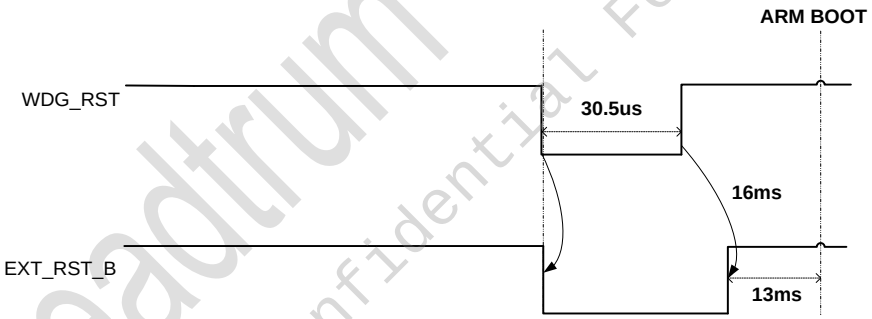


Figure 12-19 Watchdog Reset

12.12.3.4 Power Key 7s Reset

There is a power key 7 seconds reset function can generate global reset, it includes one-key mode and two-key mode. One-key mode only need to press PBINT longer than 7s(default) will generate reset, two-key mode must press PBINT and EXT_RSTN longer than 7s at the same time will generate reset.

Both one-key mode and two-key mode include:

1. hardware long reset;
2. hardware short reset;
3. software long reset;

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

4. software short reset;

Relative Register:

POR_7S_CTRL

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
PBINT_7S_FLAG_CLR	[15]	RW	NA	0	Write 1'b1 to this bit will clear pbint_7s_flag.
EXT_RSTN_FLAG_CLR	[14]	RW	NA	0	Write 1'b1 to this bit will clear ext_rstn_flag.
CHGR_INT_FLAG_CLR	[13]	RW	NA	0	Write 1'b1 to this bit will clear chgr_int_flag.
PBINT2_FLAG_CLR	[12]	RW	NA	0	Write 1'b1 to this bit will clear pbint2_flag.
PBINT_FLAG_CLR	[11]	RW	NA	0	Write 1'b1 to this bit will clear pbint_flag.
reserved	[10]	RO	NA	0	
KEY2_7S_RST_EN	[9]	RW	NA	0x1	1: One-key Reset Mode; 0: Two-key Reset Mode;
PBINT_7S_RST_SWMODE	[8]	RW	NA	0x1	0: long reset; 1: short reset;
PBINT_7S_RST_THRESHOLD	[7: 4]	RW	NA	0x6	The power key long pressing time threshold: 0~1: 2S 2: 3S 3: 4S 4: 5S 5: 6S 6: 7S 7: 8S 8: 9S 9: 10S 10:11S 11:12S 12: 13S 13:14S 14:15S 15:16S
EXT_RSTN_MODE	[3]	RW	NA	0x1	EXT_RSTN PIN function mode when 1key 7S reset 0: EXT_INT 1: RESET
PBINT_7S_AUTO_ON_EN	[2]	RW	NA	0x1	RTC register PBINT_7S_AUTO_ON_EN

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

PBINT_7S_RST_DISABLE	[1]	RW	NA	0	0: enable 7s reset function; 1: disable 7s reset function;
PBINT_7S_RST_MODE	[0]	RW	NA	0x1	0: software reset; 1: hardware reset;

POR_SRC_FLAG

Field Name	Bit	Type	Reset Value	Description
POR_SRC_FLAG	[14: 0]	RO	0x0	Power on source flag: [7]: Long pressing power key reboot hardware flag, set when PBINT=0>PBINT_7S_THRESHOLD, clear after power down. [12]: Long pressing power key reboot software flag, set when PBINT=0>PBINT_7S_THRESHOLD, clear by pbint_7s_flag.

More details as below:

12.12.3.4.1**One-key mode**

Set KEY2_7S_RST_EN=1 to enter One-key mode, In One-key mode, only need press power key longer than 7s will cause reset.There are three kinds of reset。

12.12.3.4.1.1 Hareware 7s Reset

One kind of this action which is named hardware reset will shut down all power rails.

Set register POR_7S_CTRL bit0 PBINT_7S_RST_MODE=1 to use hareware 7s reset.

12.12.3.4.1.1.1 Long Reset

Set POR_7S_CTRL bit8 PBINT_7S_RST_SWMODE=0 to choose long reset,

If the power key is pressed longer than certain time (7s by default). Reboot will be performed as long as the power key is released. It's shown in following figures.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

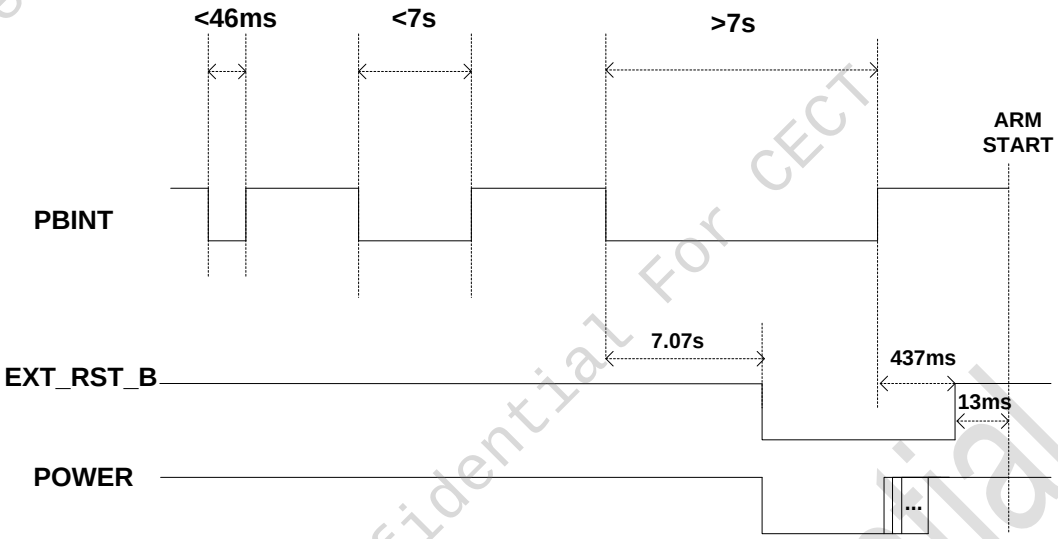


Figure 12-20 Power Key 7s Hardware long Reset

12.12.3.4.1.1.2 Short Reset

Set PBINT_7S_RST_SWMODE=1 to choose short reset.

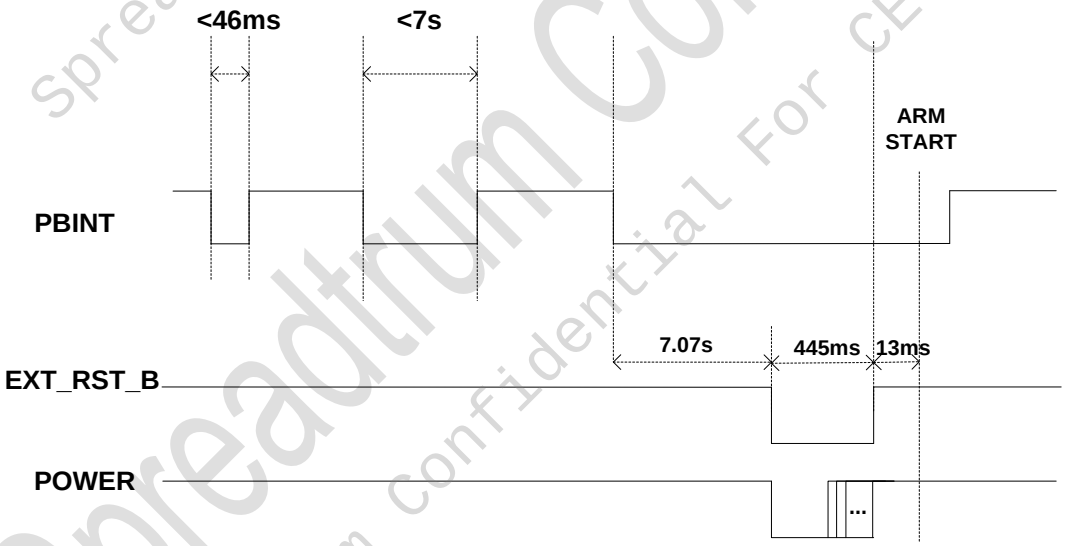


Figure 12-20 Power Key 7s Hardware short Reset

12.12.3.4.1.2 Software 7s Reset

Software reset will not shut down power rails, it will just cause a logic reset.

Set register PBINT_7S_RST_MODE=0 to use software 7s reset.

Software reset also contains long reset and short reset.

12.12.3.4.1.2.1 Long Reset

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Set PBINT_7S_RST_SWMODE=0 to choose long reset,

If the power key is pressed longer than certain time (7s by default). Reboot will be performed as long as the power key is released. It's shown in following figures.

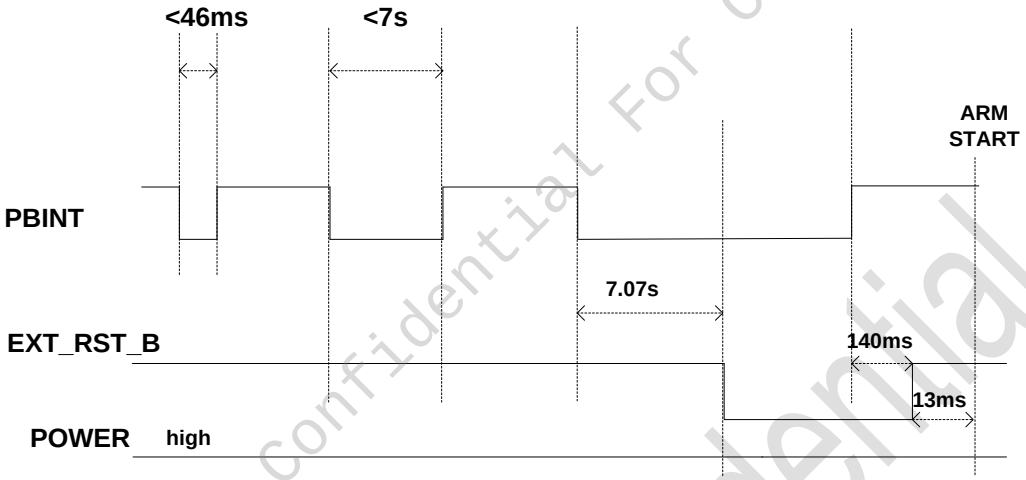


Figure 12-21 Power Key 7s Software Long Reset

12.12.3.4.1.2.2 Short Reset

Set PBINT_7S_RST_SWMODE=1 to choose short reset.

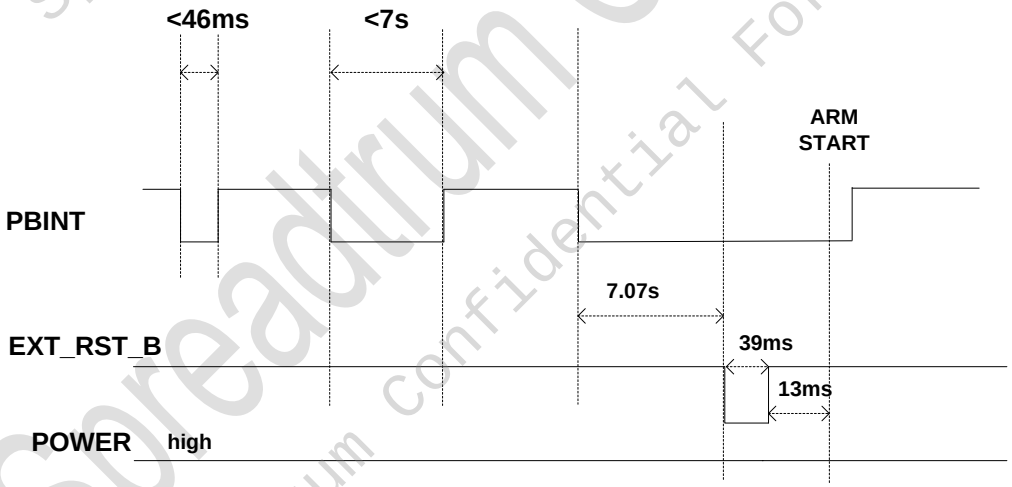


Figure 12-22 Power Key 7s Software Short Reset

12.12.3.4.2 Two-key mode

Set KEY2_7S_RST_EN=0 to enter Two-key mode.

In Two-key mode, It must press both power key and external reset key longer than 7s will cause reset.

12.12.3.4.2.1 Hareware 7s Reset

One kind of this action which is named hardware reset will shut down all power rails.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Set register POR_7S_CTRL bit0 PBINT_7S_RST_MODE=1 to use hareware 7s reset.

12.12.3.4.2.1.1 Long Reset

Set POR_7S_CTRL bit8 PBINT_7S_RST_SWMODE=0 to choose long reset,

If the power key is pressed longer than certain time (7s by default). Reboot will be performed as long as the power key is released. It's shown in following figures.

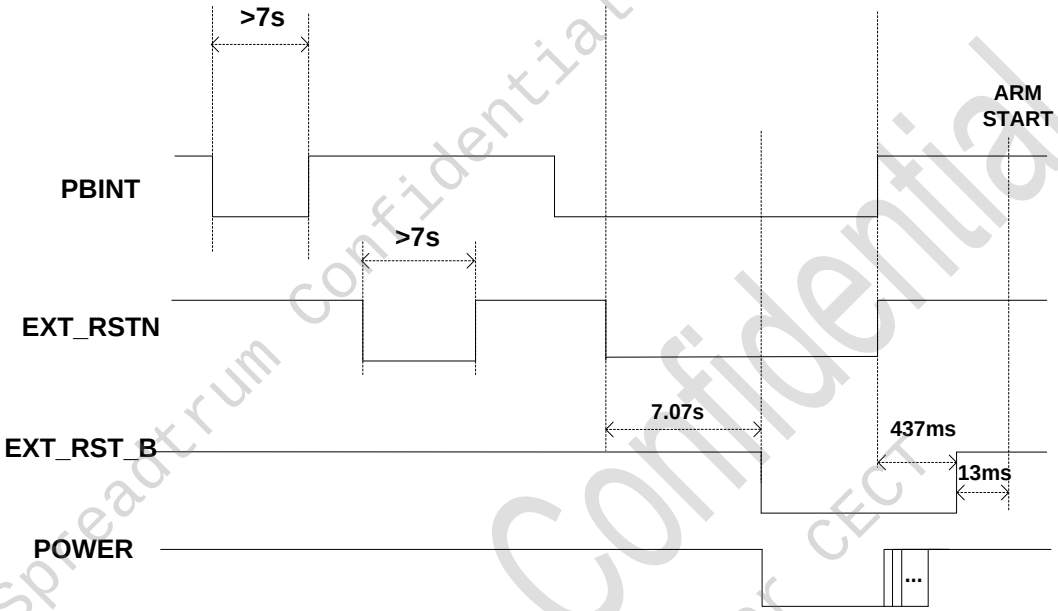


Figure 12-23 Power Key 7s Hardware long Reset

12.12.3.4.2.1.2 Short Reset

Set PBINT_7S_RST_SWMODE=1 to choose short reset.

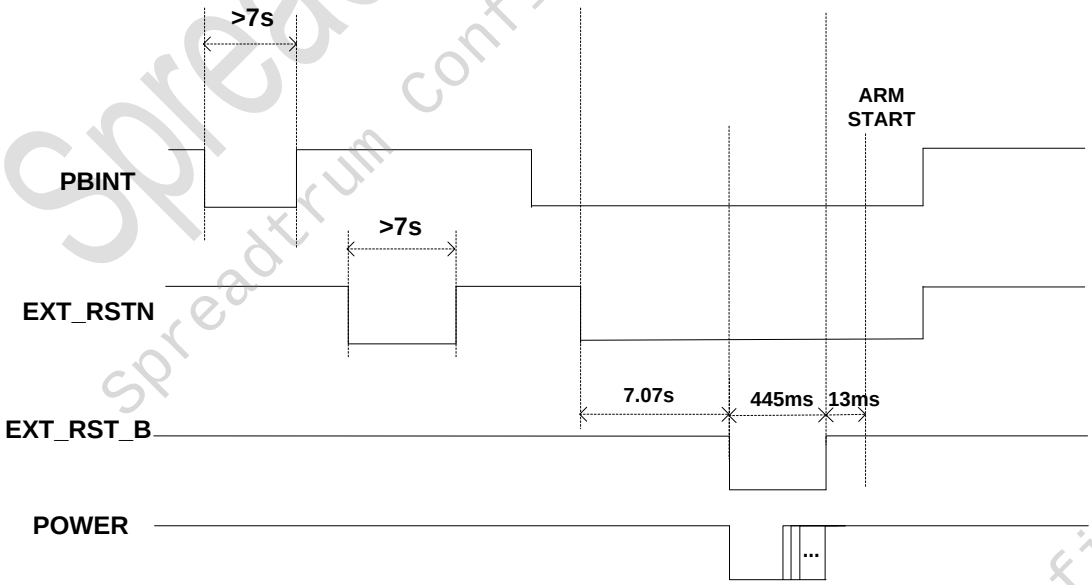


Figure 12-24 Power Key 7s Hardware short Reset

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

12.12.3.4.2.2 Software 7s Reset

Software reset will not shut down power rails, it will just cause a logic reset.

Set register PBINT_7S_RST_MODE=0 to use software 7s reset.

Software reset also contains long reset and short reset.

12.12.3.4.2.2.1 Long Reset

Set PBINT_7S_RST_SWMODE=0 to choose long reset,

If the power key is pressed longer than certain time (7s by default). Reboot will be performed as long as the power key is released. It's shown in following figures.

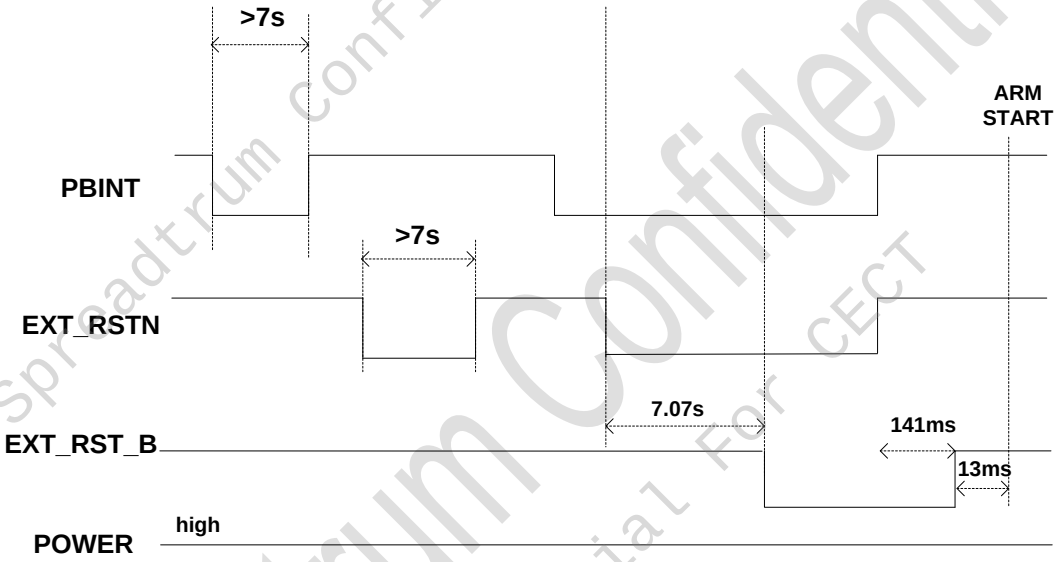


Figure 12-25 Power Key 7s Software Long Reset

12.12.3.4.2.2.2 Short Reset

Set PBINT_7S_RST_SWMODE=1 to choose short reset.

Power key 7s short reset is shown in following figure.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

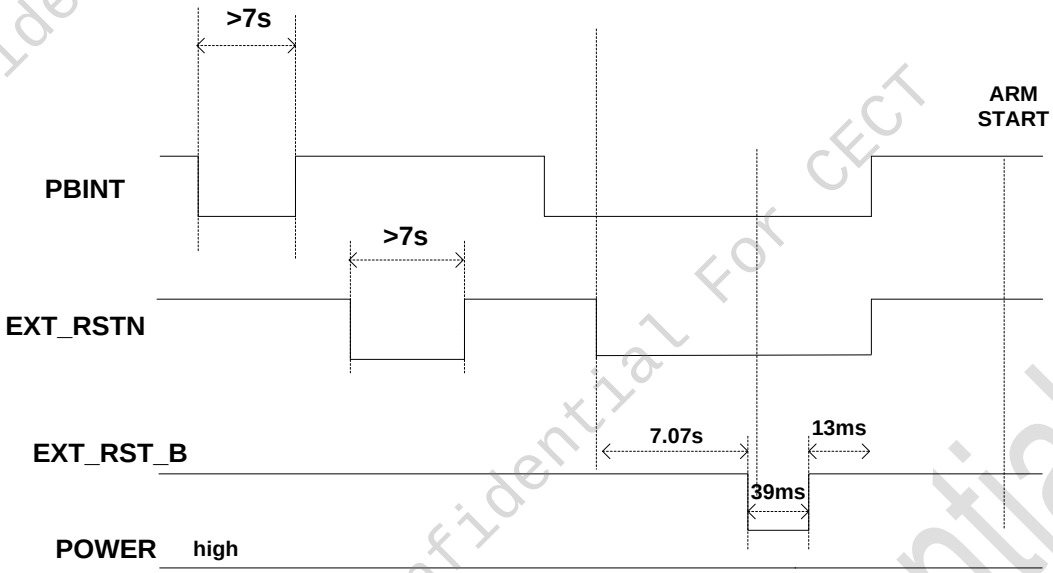


Figure 12-26 Power Key 7s Software Short Reset

12.13 Power Sleep Control

12.13.1 Introduction

Sleep control scheme inside PMIC includes 14 LDOs. All the LDO except VDDBK are divided into three kinds of control: power-off，low power mode and staying on normal mode under sleep mode. The details of power in sleep mode are shown as below.

Table 12-10 Power Sleep Control Introduction

Name	CHIP SLEEP Power Off	CHIP SLEEP Power On	EXT_XTL_EN Power On	XTL_BUF_EN Power On	CHIP SLEEP Into LP	CHIP SLEEP Exit LP	EXT_XTL_EN Exit LP	XTL_BUF_EN Exit LP
VDDCAMA	YES	YES	YES	YES	YES	YES	YES	YES
VDDSIM0	YES	YES	YES	YES	YES	YES	YES	YES
VDDSIM1	YES	YES	YES	YES	YES	YES	YES	YES
VDDSD	YES	YES	YES	YES	YES	YES	YES	YES
VDD28	YES	YES	YES	YES	YES	YES	YES	YES
VBATBK	NO	NO	NO	NO	NO	NO	NO	NO
VDDVIB	YES	YES	YES	YES	NO	NO	NO	NO
VDDBTPA	YES	YES	YES	YES	YES	YES	YES	YES
VDD18_DCXO	YES	YES	YES	YES	YES	YES	YES	YES
VDDUSB	YES	YES	YES	YES	YES	YES	YES	YES
VDD18	NO	NO	NO	NO	YES	YES	YES	YES
VDDSF	YES	YES	YES	YES	YES	YES	YES	YES
VDDCAMD	YES	YES	YES	YES	YES	YES	YES	YES
VDDCORE	NO	NO	NO	NO	YES	YES	YES	YES

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Note:

The behavior of power in sleep mode must be archived by that software configurates relative registers。The all powers stay on normal mode under sleep mode in default state。

The LDOCORE is droped when PMIC goes into sleep mode。The software need set registers to archive this behavior。

12.13.2 Interface

1. CHIP_SLEEP

Pin CHIP_SLEEP controlled the all powers of PMIC into sleep mode，but the influence of CHIP_SLEEP is configurable by software，in other word，software must set relative registers to affect the behavior of power in sleep mode。

If CHIP_SLEEP is high，the PMIC will input into sleep mode。If CHIP_SLEEP is low，the PMIC will be wake up。

2. EXT_XTL_EN，XTL_BUF_EN

The EXT_XTL_EN，XTL_BUF_EN is pins for waking all powers up in sleep mode。Same as above，software need to set relative registers for validation of these PINs。

If the pins are high，the PMIC will be wake up。If the pins are low，the PMIC will not be affected。

12.13.3 Register

SLP_CTRL

0x000000DC			SLP_CTRL(0x00000000)									SLP_CTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												LDO_XTL_EN	Reserved	SLP_IO_EN	SLP_LDO_PD_EN
Type	RO												RW	RO	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLP_CTRL

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 4]	RO	NA	0	
LDO_XTL_EN	[3]	RW	NA	0	LDO can be controlled by external

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					device if this bit is set
reserved	[2]	RO	NA	0	
SLP_IO_EN	[1]	RW	NA	0	IO PAD sleep enable in deep sleep mode
SLP_LDO_PD_EN	[0]	RW	NA	0	ALL LDO and DCDC power down enable in deep sleep mode

SLP_LDO_PD_CTRL0

0x000000E0			SLP_LDO_PD_CTRL0(0x00000000)									SLP_LDO_PD_CTRL0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SLP_LDORF_PD_EN	SLP_LDOSF_PD_EN	SLP_LDODCXO_PD_EN	SLP_LDOBTPA_PD_EN	SLP_LDOVDD28_PD_EN	SLP_LDOSD_PD_EN	Reserved	SLP_LDOUSB_PD_EN	Reserved	Reserved	SLP_LDOCAMD_PD_EN	Reserved	SLP_LDOCAMA_PD_EN	Reserved	SLP_LDOSIM1_PD_EN	SLP_LDOSIM0_PD_EN
Type	RW	RW	RW	RW	RW	RW	RO	RW	RO	RO	RW	RO	RW	RO	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLP_LDO_PD_CTRL0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
SLP_LDORF_PD_EN	[15]	RW	NA	0	LDO RF power down enable in deep sleep mode
SLP_LDOSF_PD_EN	[14]	RW	NA	0	LDO SF power down enable in deep sleep mode
SLP_LDODCXO_PD_EN	[13]	RW	NA	0	LDO DCXO power down enable in deep sleep mode
SLP_LDOBTPA_PD_EN	[12]	RW	NA	0	LDO BTPA power down enable in deep sleep mode
SLP_LDOVDD28_PD_EN	[11]	RW	NA	0	LDO VDD28 power down enable in deep sleep mode
SLP_LDOSD_PD_EN	[10]	RW	NA	0	LDO SD power down enable in deep sleep mode
reserved	[9]	RO	NA	0	
SLP_LDOUSB_PD_EN	[8]	RW	NA	0	LDO USB power down enable in deep sleep mode
reserved	[7]	RO	NA	0	
reserved	[6]	RO	NA	0	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SLP_LDOCAMD_PD_EN	[5]	RW	NA	0	LDO CAMD power down enable in deep sleep mode
reserved	[4]	RO	NA	0	
SLP_LDOCAMA_PD_EN	[3]	RW	NA	0	LDO CAMA power down enable in deep sleep mode
reserved	[2]	RO	NA	0	
SLP_LDOSIM1_PD_EN	[1]	RW	NA	0	LDO SIM1 power down enable in deep sleep mode
SLP_LDOSIM0_PD_EN	[0]	RW	NA	0	LDO SIM0 power down enable in deep sleep mode

SLP_LDO_LP_CTRL0

0x000000E4	SLP_LDO_LP_CTRL0(0x00000000)											SLP_LDO_LP_CTRL0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SLP_LDORF_LP_EN	SLP_LDOSF_LP_EN	SLP_LDODCXO_LP_EN	Reserved	SLP_LDOVDD28_LP_EN	SLP_LDOSD_LP_EN	SLP_LDOVDD18_LP_EN	SLP_LDOUSB_LP_EN	Reserved	Reserved	SLP_LDOCAMD_LP_EN	Reserved	SLP_LDOCAMA_LP_EN	SLP_LDOCORE_LP_EN	SLP_LDOSIM1_LP_EN	SLP_LDOSIM0_LP_EN
Type	RW	RW	RW	RO	RW	RW	RW	RW	RO	RO	RW	RO	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLP_LDO_LP_CTRL0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
SLP_LDORF_LP_EN	[15]	RW	NA	0	LDO RF low power mode enable in deep sleep mode
SLP_LDOSF_LP_EN	[14]	RW	NA	0	LDO SF low power mode enable in deep sleep mode
SLP_LDODCXO_LP_EN	[13]	RW	NA	0	LDO DCXO low power mode enable in deep sleep mode
reserved	[12]	RO	NA	0	
SLP_LDOVDD28_LP_EN	[11]	RW	NA	0	LDO VDD28 low power mode enable in deep sleep mode
SLP_LDOSD_LP_EN	[10]	RW	NA	0	LDO SD low power mode enable in deep sleep mode 0: Disable 1: Enable

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SLP_LDOVDD18_LP_EN	[9]	RW	NA	0	LDO VDD18 low power mode enable in deep sleep mode
SLP_LDOUSB_LP_EN	[8]	RW	NA	0	LDO USB low power mode enable in deep sleep mode 0: Disable 1: Enable
reserved	[7]	RO	NA	0	
reserved	[6]	RO	NA	0	
SLP_LDOCAMD_LP_EN	[5]	RW	NA	0	LDO CAMD low power mode enable in deep sleep mode 0: Disable 1: Enable
reserved	[4]	RO	NA	0	
SLP_LDOCAMA_LP_EN	[3]	RW	NA	0	LDO CAMA low power mode enable in deep sleep mode 0: Disable 1: Enable
SLP_LDOCORE_LP_EN	[2]	RW	NA	0	LDO CORE low power mode enable in deep sleep mode 0: Disable 1: Enable
SLP_LDOSIM1_LP_EN	[1]	RW	NA	0	LDO SIM1 low power mode enable in deep sleep mode 0: Disable 1: Enable
SLP_LDOSIM0_LP_EN	[0]	RW	NA	0	LDO SIM0 low power mode enable in deep sleep mode 0: Disable 1: Enable

LDO_CORE_SLP_CTRL0

0x000000E8			LDO_CORE_SLP_CTRL0(0x00000000)									LDO_CORE_SLP_CTRL0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								Reserved					SLP_LDOCORE_DROP_EN	LDO_CORE_SLP_OUT_STEP_EN	LDO_CORE_SLP_IN_STEP_EN
Type	RO								RO					RW	RW	RW

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_CORE_SLP_CTRL0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
reserved	[7: 3]	RO	NA	0	
SLP_LDOCORE_DROP_EN	[2]	RW	NA	0	LDO CORE power drop enable in deep sleep mode
LDO_CORE_SLP_OUT_STEP_EN	[1]	RW	NA	0	LDO CORE wakeup voltage step enable
LDO_CORE_SLP_IN_STEP_EN	[0]	RW	NA	0	LDO CORE sleep voltage step enable

LDO_CORE_SLP_CTRL1

0x000000EC			LDO_CORE_SLP_CTRL1(0x00000080)									LDO_CORE_SLP_CTRL1				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved				LDO_CORE_V_SLP_STEP1						LDO_CORE_V_DS					
Type	RO				RW						RW					
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

LDO_CORE_SLP_CTRL1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 12]	RO	NA	0	
LDO_CORE_V_SLP_STEP1	[11: 6]	RW	NA	0x2	LDO CORE sleep control of step1
LDO_CORE_V_DS	[5: 0]	RW	NA	0	LDO CORE control bits in deep sleep mode

LDO_CORE_SLP_CTRL2

0x000000F0			LDO_CORE_SLP_CTRL2(0x000001C4)									LDO_CORE_SLP_CTRL2				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				LDO_CORE_V_SLP_STEP3						LDO_CORE_V_SLP_STEP2					
Type	RO				RW						RW					
Reset	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0

LDO_CORE_SLP_CTRL2

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 12]	RO	NA	0	
LDO_CORE_V_SLP_STEP3	[11: 6]	RW	NA	0x7	LDO CORE sleep control of step3
LDO_CORE_V_SLP_STEP2	[5: 0]	RW	NA	0x4	LDO CORE sleep control of step2

LDO_CORE_SLP_CTRL3

0x000000F4	**LDO_CORE_SLP_CTRL3(0x0000034A)**											**LDO_CORE_SLP_CTRL3**				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				LDO_CORE_V_SLP_STEP5						LDO_CORE_V_SLP_STEP4					
Type	RO				RW						RW					
Reset	0	0	0	0	0	0	1	1	0	1	0	0	1	0	1	0

LDO_CORE_SLP_CTRL3

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 12]	RO	NA	0	
LDO_CORE_V_SLP_STEP5	[11: 6]	RW	NA	0xd	LDO CORE sleep control of step5
LDO_CORE_V_SLP_STEP4	[5: 0]	RW	NA	0xa	LDO CORE sleep control of step4

LDO_XTL_EN0

0x000000F8	**LDO_XTL_EN0(0x00000000)**											**LDO_XTL_EN0**				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDO_DCXO_EXT_XTL_EN	LDO_DCXO_XTL_BUF_EN	LDO_CORE_EXT_XTL_EN	LDO_CORE_XTL_BUF_EN	LDO_SIM0_EXT_XTL_EN	LDO_SIM0_XTL_BUF_EN	LDO_SIM1_EXT_XTL_EN	LDO_SIM1_XTL_BUF_EN	LDO_CAMA_EXT_XTL_EN	LDO_CAMA_XTL_BUF_EN	LDO_CAMD_EXT_XTL_EN	LDO_CAMD_XTL_BUF_EN	LDO_VDD18_EXT_XTL_EN	LDO_VDD18_XTL_BUF_EN	LDO_VDD28_EXT_XTL_EN	LDO_VDD28_XTL_BUF_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_XTL_EN0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
LDO_DCXO_EXT_XTL_EN	[15]	RW	NA	0	LDO DCXO can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_DCXO_XTL_BUF_EN	[14]	RW	NA	0	LDO DCXO can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_CORE_EXT_XTL_EN	[13]	RW	NA	0	LDO CORE can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_CORE_XTL_BUF_EN	[12]	RW	NA	0	LDO CORE can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_SIM0_EXT_XTL_EN	[11]	RW	NA	0	LDO SIM0 can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_SIM0_XTL_BUF_EN	[10]	RW	NA	0	LDO SIM0 can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_SIM1_EXT_XTL_EN	[9]	RW	NA	0	LDO SIM1 can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_SIM1_XTL_BUF_EN	[8]	RW	NA	0	LDO SIM1 can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_CAMA_EXT_XTL_EN	[7]	RW	NA	0	LDO CAMA can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_CAMA_XTL_BUF_EN	[6]	RW	NA	0	LDO CAMA can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_CAMD_EXT	[5]	RW	NA	0	LDO CAMD can be controlled by EXT_XTL_EN(from PAD) if this bit is

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

_XTL_EN					set
LDO_CAMD_XTL_BUF_EN	[4]	RW	NA	0	LDO CAMD can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_VDD18_EXT_XTL_EN	[3]	RW	NA	0	LDO VDD18 can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_VDD18_XTL_BUF_EN	[2]	RW	NA	0	LDO VDD18 can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_VDD28_EXT_XTL_EN	[1]	RW	NA	0	LDO VDD28 can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_VDD28_XTL_BUF_EN	[0]	RW	NA	0	LDO VDD28 can be controlled by XTL_BUF_EN(from PAD) if this bit is set

LDO_XTL_EN1

0x000000FC			LDO_XTL_EN1(0x00000000)									LDO_XTL_EN1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LDO_RF_EXT_XTL_EN	LDO_RF_XTL_BUF_EN	LDO_SF_EXT_XTL_EN	LDO_SF_XTL_BUF_EN	Reserved				LDO_VIBR_EXT_XTL_EN	LDO_VIBR_XTL_BUF_EN	LDO_USB_EXT_XTL_EN	LDO_USB_XTL_BUF_EN	LDO_BTPA_EXT_XTL_EN	LDO_BTPA_XTL_BUF_EN	LDO_SD_EXT_XTL_EN	LDO_SD_XTL_BUF_EN
Type	RW	RW	RW	RW	RO				RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_XTL_EN1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
LDO_RF_EXT_XTL_EN	[15]	RW	NA	0	LDO RF can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_RF_XTL_BUF_EN	[14]	RW	NA	0	LDO RF can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_SF_EXT_XTL_EN	[13]	RW	NA	0	LDO SF can be cotrolled by EXT_XTL_EN(from PAD) if this bit is set
LDO_SF_XTL_B	[12]	RW	NA	0	LDO SF can be controlled by

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

UF_EN					XTL_BUF_EN(from PAD) if this bit is set
reserved	[11: 8]	RO	NA	0	
LDO_VIBR_EXT_XTL_EN	[7]	RW	NA	0	LDO VIBR can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_VIBR_XTL_BUF_EN	[6]	RW	NA	0	LDO VIBR can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_USB_EXT_XTL_EN	[5]	RW	NA	0	LDO USB can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_USB_XTL_BUF_EN	[4]	RW	NA	0	LDO USB can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_BTPA_EXT_XTL_EN	[3]	RW	NA	0	LDO BTPA can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_BTPA_XTL_BUF_EN	[2]	RW	NA	0	LDO BTPA can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_SD_EXT_XTL_EN	[1]	RW	NA	0	LDO SD can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_SD_XTL_BUF_EN	[0]	RW	NA	0	LDO SD can be controlled by XTL_BUF_EN(from PAD) if this bit is set

XO_BG_XTL_EN

0x00000100	XO_BG_XTL_EN(0x00000000)											XO_BG_XTL_EN				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DCXO_EXT_XTL_EN	DCXO_XTL_BUF_EN	Reserved													
Type	RW	RW	RO													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

XO_BG_XTL_EN

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

DCXO_EXT_XTL_EN	[15]	RW	NA	0	DCXO can be controlled by EXT_XTL_EN(from PAD) if this bit is set
DCXO_XTL_BUF_EN	[14]	RW	NA	0	DCXO can be controlled by XTL_BUF_EN(from PAD) if this bit is set
reserved	[13: 0]	RO	NA	0	

12.13.4 Application note

12.13.4.1 LDOCORE

In sleep mode，the output voltage of LDOCORE could：

1. keep previous status(default)；
2. drop and rise directly by setting SLP_LDOCORE_DROP_EN = 1，
   LDO_CORE_SLP_OUT_STEP_EN = 0 and LDO_CORE_SLP_IN_STEP_EN = 0；
3. step drop and rise by setting SLP_LDOCORE_DROP_EN = 1，
   LDO_CORE_SLP_OUT_STEP_EN = 1 and LDO_CORE_SLP_IN_STEP_EN = 1；

SLP_LDOCORE_DROP_EN	[2]	RW	NA	0	LDO CORE power drop enable in deep sleep mode
LDO_CORE_SLP_OUT_STEP_EN	[1]	RW	NA	0	LDO CORE wakeup voltage step enable
LDO_CORE_SLP_IN_STEP_EN	[0]	RW	NA	0	LDO CORE sleep voltage step enable
LDO_CORE_V_SLP_STEP1	[11: 6]	RW	NA	0x2	LDO CORE sleep control of step1
LDO_CORE_V_DS	[5: 0]	RW	NA	0	LDO CORE control bits in deep sleep mode
LDO_CORE_V_SLP_STEP3	[11: 6]	RW	NA	0x7	LDO CORE sleep control of step3
LDO_CORE_V_SLP_STEP2	[5: 0]	RW	NA	0x4	LDO CORE sleep control of step2
LDO_CORE_V_SLP_STEP5	[11: 6]	RW	NA	0xd	LDO CORE sleep control of step5
LDO_CORE_V_SLP_STEP4	[5: 0]	RW	NA	0xa	LDO CORE sleep control of step4
LDO_CORE_EXT_XTL_EN	[13]	RW	NA	0	LDO CORE can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_CORE_XTL_BUF_EN	[12]	RW	NA	0	LDO CORE can be controlled by XTL_BUF_EN(from PAD) if this bit is set

12.13.4.2 Other power

First，configure the main switch that affect all powers in sleep mode。

LDO_XTL_EN	[3]	RW	NA	0	LDO can be controlled by external

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					device if this bit is set
SLP_LDO_PD_EN	[0]	RW	NA	0	ALL LDO and DCDC power down enable in deep sleep mode

Second，configure registers corresponded with relative power。

For example：

SLP_LDOSIM0_PD_EN	[0]	RW	NA	0	LDO SIM0 power down enable in deep sleep mode
SLP_LDOSIM0_LP_EN	[0]	RW	NA	0	LDO SIM0 low power mode enable in deep sleep mode 0: Disable 1: Enable
LDO_SIM0_EXT_XTL_EN	[11]	RW	NA	0	LDO SIM0 can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_SIM0_XTL_BUF_EN	[10]	RW	NA	0	LDO SIM0 can be controlled by XTL_BUF_EN(from PAD) if this bit is set

The above registers is for LDO_SIM0，SW can set these registers to take LDO_SIM0 into power down or low power mode，and to wake LDO_SIM0 up from which PINs(EXT_XTL_EN，XTL_BUF_EN)。

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

13 Analog register

13.1 Global Register

13.1.1 Register Address Map

Base address: 0x82001400

Offset Addr	Name	Description
0x0000	CHIP_ID_LOW	CHIP_ID_LOW
0x0004	CHIP_ID_HIGH	CHIP_ID_HIGH
0x0008	MODULE_EN0	MODULE_EN0
0x000C	ARM_CLK_EN0	ARM_CLK_EN0
0x0010	RTC_CLK_EN0	RTC_CLK_EN0
0x0014	SOFT_RST0	SOFT_RST0
0x0018	POWER_PD_SW	POWER_PD_SW
0x001C	POWER_PD_HW	POWER_PD_HW
0x0020	RESERVED_REG0	RESERVED_REG0
0x0024	RESERVED_REG1	RESERVED_REG1
0x0028	RESERVED_REG2	RESERVED_REG2
0x002C	RESERVED_REG3	RESERVED_REG3
0x0030	RESERVED_REG4	RESERVED_REG4
0x0034	RESERVED_REG5	RESERVED_REG6
0x0038	LDO_CAMA_REG0	LDO_CAMA_REG0
0x003C	LDO_CAMA_REG1	LDO_CAMA_REG1
0x0040	LDO_SIM0_REG0	LDO_SIM0_REG0
0x0044	LDO_SIM0_REG1	LDO_SIM0_REG1
0x0048	LDO_SIM0_REG2	LDO_SIM0_REG2
0x004C	LDO_SIM1_REG0	LDO_SIM1_REG0
0x0050	LDO_SIM1_REG1	LDO_SIM1_REG1
0x0054	LDO_SIM1_PD_REG	LDO_SIM1_PD_REG
0x0058	LDO_SD_REG0	LDO_SD_REG0
0x005C	LDO_SD_REG1	LDO_SD_REG1
0x0060	LDO_SD_REG2	LDO_SD_REG2
0x0064	LDO_VDD28_REG0	LDO_VDD28_REG0
0x0068	LDO_VDD28_REG1	LDO_VDD28_REG1
0x006C	LDO_BTPA_REG0	LDO_BTPA_REG0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0070	LDO_BTPA_REG1	LDO_BTPA_REG1
0x0074	LDO_DCXO_REG0	LDO_DCXO_REG0
0x0078	LDO_DCXO_REG1	LDO_DCXO_REG1
0x007C	LDO_USB_REG0	LDO_USB_REG0
0x0080	LDO_USB_REG1	LDO_USB_REG1
0x0084	LDO_CAMD_REG0	LDO_CAMD_REG0
0x0088	LDO_CAMD_REG1	LDO_CAMD_REG1
0x008C	LDO_SF_REG0	LDO_SF_REG0
0x0090	LDO_SF_REG1	LDO_SF_REG1
0x0094	LDO_VDD18_REG0	LDO_VDD18_REG0
0x0098	LDO_VDD18_REG1	LDO_VDD18_REG1
0x009C	LDO_RF_REG0	LDO_RF_REG0
0x00A0	LDO_RF_REG1	LDO_RF_REG1
0x00A4	LDO_CORE_REG0	LDO_CORE_REG0
0x00A8	LDO_CORE_REG1	LDO_CORE_REG1
0x00AC	RESERVED_REG17	RESERVED_REG17
0x00B0	RESERVED_REG18	RESERVED_REG18
0x00B4	RESERVED_REG19	RESERVED_REG19
0x00B8	RESERVED_REG20	RESERVED_REG20
0x00BC	RESERVED_REG21	RESERVED_REG21
0x00C0	RESERVED_REG22	RESERVED_REG22
0x00C4	LDO_CH_CTRL	LDO_CH_CTRL
0x00C8	LDO_REFTRIM_REG	LDO_REFTRIM_REG
0x00CC	RESERVED_REG24	RESERVED_REG24
0x00D0	RESERVED_REG25	RESERVED_REG25
0x00D4	RESERVED_REG26	RESERVED_REG26
0x00D8	RESERVED_REG27	RESERVED_REG27
0x00DC	SLP_CTRL	SLP_CTRL
0x00E0	SLP_LDO_PD_CTRL0	SLP_LDO_PD_CTRL0
0x00E4	SLP_LDO_LP_CTRL0	SLP_LDO_LP_CTRL0
0x00E8	LDO_CORE_SLP_CTRL0	LDO_CORE_SLP_CTRL0
0x00EC	LDO_CORE_SLP_CTRL1	LDO_CORE_SLP_CTRL1
0x00F0	LDO_CORE_SLP_CTRL2	LDO_CORE_SLP_CTRL2
0x00F4	LDO_CORE_SLP_CTRL3	LDO_CORE_SLP_CTRL3
0x00F8	LDO_XTL_EN0	LDO_XTL_EN0
0x00FC	LDO_XTL_EN1	LDO_XTL_EN1

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0100	XO_BG_XTL_EN	XO_BG_XTL_EN
0x0104	RESERVED_REG29	RESERVED_REG29
0x0108	RESERVED_REG30	RESERVED_REG30
0x010C	RESERVED_REG31	RESERVED_REG31
0x0110	RESERVED_REG32	RESERVED_REG32
0x0114	RESERVED_REG33	RESERVED_REG33
0x0118	RESERVED_REG34	RESERVED_REG34
0x011C	CLK32KLESS_CTRL0	CLK32KLESS_CTRL0
0x0120	CLK32KLESS_CTRL1	CLK32KLESS_CTRL1
0x0124	CLK32KLESS_CTRL2	CLK32KLESS_CTRL2
0x0128	CLK32KLESS_CTRL3	CLK32KLESS_CTRL3
0x012C	CLK32KLESS_CTRL4	CLK32KLESS_CTRL4
0x0130	AUXAD_CTL	AUXAD_CTL
0x0134	XTL_WAIT_CTRL	XTL_WAIT_CTRL
0x0138	IB_CTRL	IB_CTRL
0x013C	WHTLED_CTRL	WHTLED_CTRL
0x0140	KPLED_CTRL	KPLED_CTRL
0x0144	VIBR_CTRL	VIBR_CTRL0
0x0148	AUDIO_CTRL0	AUDIO_CTRL0
0x014C	AUDIO_CTRL1	AUDIO_CTRL1
0x0150	CHGR_CTRL0	CHGR_CTRL0
0x0154	CHGR_CTRL1	CHGR_CTRL1
0x0158	CHGR_CTRL2	CHGR_CTRL2
0x015C	CHGR_STATUS	CHGR_STATUS
0x0160	MIXED_CTRL0	MIXED_CTRL0
0x0164	MIXED_CTRL1	MIXED_CTRL1
0x0168	POR_RST_MONITOR	POR_RST_MONITOR
0x016C	WDG_RST_MONITOR	WDG_RST_MONITOR
0x0170	POR_PIN_RST_MONITOR	POR_PIN_RST_MONITOR
0x0174	POR_SRC_FLAG	POR_SRC_FLAG
0x0178	POR_7S_CTRL	POR_7S_CTRL
0x017C	HWRST_RTC	HWRST_RTC
0x0180	ARCH_EN	ARCH_EN
0x0184	MCU_WR_PROT_VALUE	MCU_WR_PROT_VALUE
0x0188	PWR_WR_PROT_VALUE	PWR_WR_PROT_VALUE
0x018C	SMPL_CTRL0	SMPL_CTRL0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

0x0190	SMPL_CTRL1	SMPL_CTRL1
0x0194	RTC_RST0	RTC_RST0
0x0198	RTC_RST1	RTC_RST1
0x019C	RTC_RST2	RTC_RST2
0x01A0	RTC_CLK_STOP	RTC_CLK_STOP
0x01A4	VBAT_DROP_CNT	VBAT_DROP_CNT
0x01A8	SWRST_CTRL0	SWRST_CTRL0
0x01AC	SWRST_CTRL1	SWRST_CTRL1
0x01B0	OTP_CTRL	OTP_CTRL
0x01B4	RESERVED_REG35	RESERVED_REG35
0x01B8	RESERVED_REG36	RESERVED_REG36
0x01BC	LOW_PWR_CLK32K_CTRL	LOW_PWR_CLK32K_CTRL
0x01C0	LOW_PWR_CLK32K_TEST0	LOW_PWR_CLK32K_TEST0
0x01C4	LOW_PWR_CLK32K_TEST1	LOW_PWR_CLK32K_TEST1
0x01C8	LOW_PWR_CLK32K_TEST2	LOW_PWR_CLK32K_TEST2
0x01CC	LOW_PWR_CLK32K_TEST3	LOW_PWR_CLK32K_TEST3

13.1.1.1 CHIP_ID_LOW

0x00000000			CHIP_ID_LOW(0x0000A000)									CHIP_ID_LOW				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHIP_ID_LOW															
Type	RO															
Reset	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

CHIP_ID_LOW

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
CHIP_ID_LOW	[15: 0]	RO	NA	0xa000	CHIP ID low 16 bits

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

13.1.1.2 CHIP_ID_HIGH

0x00000004			CHIP_ID_HIGH(0x00001161)									CHIP_ID_HIGH				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CHIP_ID_HIGH															
Type	RO															
Reset	0	0	0	1	0	0	0	1	0	1	1	0	0	0	0	1

CHIP_ID_HIGH

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
CHIP_ID_HIGH	[15: 0]	RO	NA	0x1161	CHIP ID high 16 bits

13.1.1.3 MODULE_EN0

0x00000008			MODULE_EN0(0x00000082)									MODULE_EN0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								PINREG_EN	PWM_EN	ADC_EN	AUD_EN	EIC_EN	WDG_EN	RTC_EN	CAL_EN
Type	RO								RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

MODULE_EN0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	Reserved
PINREG_EN	[7]	RW	NA	0x1	PINREG module enable 0: Disable the PCLK of pin registers 1: Enable the PCLK of pin registers
PWM_EN	[6]	RW	NA	0	PWM module enable

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					0: Disable the PCLK of PWM 1: Enable the PCLK of PWM
ADC_EN	[5]	RW	NA	0	AUXADC module enable 0: Disable the PCLK of AUXADC 1: Enable the PCLK of AUXADC
AUD_EN	[4]	RW	NA	0	Audio module enable 0: Disable the PCLK of Audio 1: Enable the PCLK of Audio
EIC_EN	[3]	RW	NA	0	EIC module enable 0: Disable the PCLK of EIC 1: Enable the PCLK of EIC
WDG_EN	[2]	RW	NA	0	WDG module enable 0: Disable the PCLK of watchdog 1: Enable the PCLK of watchdog
RTC_EN	[1]	RW	NA	0x1	RTC module enable 0: Disable the PCLK of RTC 1: Enable the PCLK of RTC
CAL_EN	[0]	RW	NA	0	CAL module enable 0: Disable the PCLK of CAL 1: Enable the PCLK of CAL

13.1.1.4 ARM_CLK_EN0

0x0000000C			ARM_CLK_EN0(0x00000000)									ARM_CLK_EN0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								CLK_AUD_SCLK_EN	CLK_AUXAD_EN	CLK_AUXADC_EN	Reserved		CLK_CAL_EN	CLK_AUD_IF_6P5M_EN	CLK_AUD_IF_EN
Type	RO								RW	RW	RW	RO		RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ARM_CLK_EN0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

CLK_AUD_SCLK_EN	[7]	RW	NA	0	Analog clock enable 0: disable CLK_AUD_SCLK 1: enable CLK_AUD_SCLK
CLK_AUXAD_EN	[6]	RW	NA	0	AUXAD clock enable, the clock is connected to AUXADC converter 0: disable AUXAD_CLK 1: enable AUXAD_CLK
CLK_AUXADC_EN	[5]	RW	NA	0	AUXADC module work clock enable 0: disable clk_adc 1: enable clk_adc
reserved	[4: 3]	RO	NA	0	
CLK_CAL_EN	[2]	RW	NA	0	CLK_CAL eanble 0: disable clk_cal 1: enable clk_cal
CLK_AUD_IF_6P5M_EN	[1]	RW	NA	0	Audio 6.5M clock enable 0: disable clk_aud_6p5m_rx and clk_aud_6p5m_tx 1: enable clk_aud_6p5m_rx and clk_aud_6p5m_tx
CLK_AUD_IF_EN	[0]	RW	NA	0	Audio IF clock enable 0: disable CLK_AUDIF 1: enable CLK_AUDIF

13.1.1.5 RTC_CLK_EN0

0x00000010			RTC_CLK_EN0(0x00000003)									RTC_CLK_EN0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											RTC_PWM_EN	RTC_EIC_EN	RTC_WDG_EN	RTC_RTC_EN	RTC_ARCH_EN
Type	RO											RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

RTC_CLK_EN0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 5]	RO	NA	0	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

RTC_PWM_EN	[4]	RW	NA	0	The RTC clock enable of PWM module
RTC_EIC_EN	[3]	RW	NA	0	EIC RTC clock soft enable 0: Disable the RTC clock of EIC 1: Enable RTC clock of EIC
RTC_WDG_EN	[2]	RW	NA	0	Watchdog RTC clock soft enable 0: Disable the RTC clock of Watchdog 1: Enable RTC clock of Watchdo
RTC_RTC_EN	[1]	RW	NA	0x1	RTC RTC clock soft enable 0: Disable the RTC clock of RTC 1: Enable RTC clock of RTC
RTC_ARCH_EN	[0]	RW	NA	0x1	ARCH RTC clock soft enable 0: Disable the RTC clock of ARCH 1: Enable RTC clock of ARCH

13.1.1.6 SOFT_RST0

0x00000014			SOFT_RST0(0x00000000)									SOFT_RST0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							AUDRX_SOFT_RST	AUDTX_SOFT_RST	AUD_IF_SOFT_RST	ADC_SOFT_RST	PWM_SOFT_RST	EIC_SOFT_RST	WDG_SOFT_RST	RTC_SOFT_RST	CAL_SOFT_RST
Type	RO							RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SOFT_RST0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 9]	RO	NA	0	
AUDRX_SOFT_RST	[8]	RW	NA	0	AUD RX soft reset
AUDTX_SOFT_RST	[7]	RW	NA	0	AUD TX soft reset
AUD_IF_SOFT_RST	[6]	RW	NA	0	Audio IF soft reset
ADC_SOFT_RST	[5]	RW	NA	0	Auxadc soft reset
PWM_SOFT_RS	[4]	RW	NA	0	PWM soft reset

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

T					
EIC_SOFT_RST	[3]	RW	NA	0	EIC soft reset
WDG_SOFT_RST	[2]	RW	NA	0	Watchdog soft reset
RTC_SOFT_RST	[1]	RW	NA	0	RTC soft reset
CAL_SOFT_RST	[0]	RW	NA	0	CAL soft reset

13.1.1.7 POWER_PD_SW

0x00000018	POWER_PD_SW(0x00000000)											POWER_PD_SW				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										LDO_DCXO_PD	LDO_CORE_PD	LDO_SF_PD	LDO_VDD18_PD	LDO_VDD28_PD	BG_PD
Type	RO										RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

POWER_PD_SW

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 6]	RO	NA	0	
LDO_DCXO_PD	[5]	RW	NA	0	LDO_DCXO power down 1: power down 0: power on
LDO_CORE_PD	[4]	RW	NA	0	DCDC_CORE power down 1: power down 0: power on
LDO_SF_PD	[3]	RW	NA	0	DCDC_ARM1 power down 1: power down 0: power on
LDO_VDD18_PD	[2]	RW	NA	0	LDO_AVDD18 power down 1: power down 0: power on
LDO_VDD28_PD	[1]	RW	NA	0	LDO_VDD28 power down 1: power down 0: power on
BG_PD	[0]	RW	NA	0	Bandgap power down 1: power down 0: power on

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

13.1.1.8 POWER_PD_HW

0x0000001C			POWER_PD_HW(0x00000000)									POWER_PD_HW				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															PWR_OFF_SEQ_EN
Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

POWER_PD_HW

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 1]	RO	NA	0	
PWR_OFF_SEQ_EN	[0]	RW	NA	0	Power off_sequence enable that is protected by reg PWR_WR_PROT_VALUE.PWR_WR_PROT

13.1.1.9 RESERVED_REG0

0x00000020			RESERVED_REG0(0x00000000)									RESERVED_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

reserved	[15: 0]	RO	NA	0	

13.1.1.10 RESERVED_REG1

0x00000024	RESERVED_REG1(0x00000000)											RESERVED_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.11 RESERVED_REG2

0x00000028	RESERVED_REG2(0x00000000)											RESERVED_REG2				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG2

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

13.1.1.12 RESERVED_REG3

0x0000002C			RESERVED_REG3(0x00000000)									RESERVED_REG3				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG3

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.13 RESERVED_REG4

0x00000030			RESERVED_REG4(0x00000000)									RESERVED_REG4				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG4

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.14 RESERVED_REG5

0x00000034			RESERVED_REG6(0x00000000)									RESERVED_REG5				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG6

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.15 LDO_CAMA_REG0

0x00000038			LDO_CAMA_REG0(0x00000001)									LDO_CAMA_REG0				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved							LDO_CAMA_LP_EN_SW	Reserved						LDO_CAMA_SHPT_PD	LDO_CAMA_PD
Type	RO							RW	RO						RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

LDO_CAMA_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 9]	RO	NA	0	
LDO_CAMA_LP_EN_SW	[8]	RW	NA	0	LDO_CAMA low power mode enable software control 0: depends on SLP_LDO_CAMA_LP_EN control 1: Enable
reserved	[7: 2]	RO	NA	0	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

LDO_CAMA_SHPT_PD	[1]	RW	NA	0	LDO short protection power down
LDO_CAMA_PD	[0]	RW	NA	0x1	LDO_CAMA power down 1: power down 0: power on

13.1.1.16 LDO_CAMA_REG1

0x0000003C			LDO_CAMA_REG1(0x000000A0)									LDO_CAMA_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								LDO_CAMA_V							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

LDO_CAMA_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
LDO_CAMA_V	[7: 0]	RW	NA	0xa0	CAMA LDO program bits: 8'b0 as 1.2V output, 10mV/step, 2.8V default,output range:1.8---3.3V

13.1.1.17 LDO_SIM0_REG0

0x00000040			LDO_SIM0_REG0(0x00000000)									LDO_SIM0_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							LDO_SIM0_LP_EN_SW	Reserved						LDO_SIM0_SHPT_PD	Reserved
Type	RO							RW	RO						RW	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

LDO_SIM0_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 9]	RO	NA	0	
LDO_SIM0_LP_EN_SW	[8]	RW	NA	0	LDO_SIM0 low power mode enable software control 0: depends on SLP_LDO_SIM0_LP_EN control 1: Enable
reserved	[7: 2]	RO	NA	0	
LDO_SIM0_SHPT_PD	[1]	RW	NA	0	LDO short protection power down
reserved	[0]	RO	NA	0	

13.1.1.18 LDO_SIM0_REG1

0x00000044	LDO_SIM0_REG1(0x0000003C)											LDO_SIM0_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								LDO_SIM0_V							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

LDO_SIM0_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
LDO_SIM0_V	[7: 0]	RW	NA	0x3c	VDDSIM0 LDO program bits: 8'b0 as 1.2V output, 10mV/step default 1.8V,output range:1.8---3.3V

13.1.1.19 LDO_SIM0_REG2

0x00000048	LDO_SIM0_REG2(0x00000001)											LDO_SIM0_REG2				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															LDO_SIM0_PD
Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

LDO_SIM0_REG2

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 1]	RO	NA	0	
LDO_SIM0_PD	[0]	RW	NA	0x1	LDO_SIM0 power down 1: power down 0: power on

13.1.1.20 LDO_SIM1_REG0

0x0000004C		LDO_SIM1_REG0(0x00000000)									LDO_SIM1_REG0				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved							LDO_SIM1_LP_EN_SW	Reserved						LDO_SIM1_SHPT_PD	Reserved
Type	RO							RW	RO						RW	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_SIM1_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 9]	RO	NA	0	
LDO_SIM1_LP_E	[8]	RW	NA	0	LDO_SIM1 low power mode enable

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

N_SW					software control 0: depends on SLP_LDO_SIM1_LP_EN control 1: Enable
reserved	[7: 2]	RO	NA	0	
LDO_SIM1_SHPT_PD	[1]	RW	NA	0	LDO short protection power down
reserved	[0]	RO	NA	0	

13.1.1.21 LDO_SIM1_REG1

0x00000050	LDO_SIM1_REG1(0x0000003C)											LDO_SIM1_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								LDO_SIM1_V							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

LDO_SIM1_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
LDO_SIM1_V	[7: 0]	RW	NA	0x3c	VDDSIM1 LDO program bits: 8'b0 as 1.2V output, 10mV/step, 1.8V default,output range:1.8---3.3V

13.1.1.22 LDO_SIM1_PD_REG

0x00000054	LDO_SIM1_PD_REG(0x00000001)											LDO_SIM1_PD_REG				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															LDO_SIM1_PD
Type	RO															RW

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

LDO_SIM1_PD_REG

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 1]	RO	NA	0	
LDO_SIM1_PD	[0]	RW	NA	0x1	LDO_SIM1 power down 1: power down 0: power on

13.1.1.23 LDO_SD_REG0

0x00000058	LDO_SD_REG0(0x00000000)											LDO_SD_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							LDO_SD_LP_EN_SW	Reserved						LDO_SD_SHPT_PD	Reserved
Type	RO							RW	RO						RW	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_SD_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 9]	RO	NA	0	
LDO_SD_LP_EN_SW	[8]	RW	NA	0	LDO_SD low power mode enable software control 0: depends on SLP_LDO_SD_LP_EN control 1: Enable
reserved	[7: 2]	RO	NA	0	
LDO_SD_SHPT_PD	[1]	RW	NA	0	LDO short protection power down
reserved	[0]	RO	NA	0	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

13.1.1.24 LDO_SD_REG1

0x0000005C			LDO_SD_REG1(0x000000B4)									LDO_SD_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								LDO_SD_V							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0

LDO_SD_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
LDO_SD_V	[7: 0]	RW	NA	0xb4	SD CORE LDO program bits: 8'b0 as 1.2V output, 10mV/step, 3.0V default,output range:1.8---3.3V

13.1.1.25 LDO_SD_REG2

0x00000060			LDO_SD_REG2(0x00000001)									LDO_SD_REG2				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															LDO_SD_PD
Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

LDO_SD_REG2

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 1]	RO	NA	0	
LDO_SD_PD	[0]	RW	NA	0x1	LDO_SD power down

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					1: power down 0: power on

13.1.1.26 LDO_VDD28_REG0

0x00000064			LDO_VDD28_REG0(0x00000000)									LDO_VDD28_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							LDO_VDD28_LP_EN_SW	Reserved						LDO_VDD28_SHPT_PD	Reserved
Type	RO							RW	RO						RW	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_VDD28_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 9]	RO	NA	0	
LDO_VDD28_LP_EN_SW	[8]	RW	NA	0	LDO_VDD28 low power mode enable software control 0: depends on SLP_LDO_VDD28_LP_EN control 1: Enable
reserved	[7: 2]	RO	NA	0	
LDO_VDD28_SHPT_PD	[1]	RW	NA	0	LDO short protection power down
reserved	[0]	RO	NA	0	

13.1.1.27 LDO_VDD28_REG1

0x00000068			LDO_VDD28_REG1(0x000000A0)									LDO_VDD28_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	Reserved								LDO_VDD28_V							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

LDO_VDD28_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
LDO_VDD28_V	[7: 0]	RW	NA	0xa0	2.8V LDO program bits: 1.8~3.3 2.8V default,10mv/step

13.1.1.28 LDO_BTPA_REG0

0x0000006C			LDO_BTPA_REG0(0x00000001)									LDO_BTPA_REG0				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved						LDO_BTPA_BYPASS	Reserved	Reserved						LDO_BTPA_SHPT_PD	LDO_BTPA_PD
Type	RO						RW	RO	RO						RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

LDO_BTPA_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 10]	RO	NA	0	
LDO_BTPA_BYPASS	[9]	RW	NA	0	LDO BTPA BYPASS. "1" Output short to VBAT "0" LDO mode
reserved	[8]	RO	NA	0	
reserved	[7: 2]	RO	NA	0	
LDO_BTPA_SHPT_PD	[1]	RW	NA	0	LDO short protection power down

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

LDO_BTPA_PD	[0]	RW	NA	0x1	LDO_BTPA power down 1: power down 0: power on

13.1.1.29 LDO_BTPA_REG1

0x00000070	LDO_BTPA_REG1(0x000000D2)											LDO_BTPA_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								LDO_BTPA_V							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0

LDO_BTPA_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
LDO_BTPA_V	[7: 0]	RW	NA	0xd2	VDDBTPA LDO program bits: 8'b0 as 1.2V output, 10mV/step, 3.3V default

13.1.1.30 LDO_DCXO_REG0

0x00000074	LDO_DCXO_REG0(0x00000000)											LDO_DCXO_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							LDO_DCXO_LP_EN_SW	Reserved						LDO_DCXO_SHPT_PD	Reserved
Type	RO							RW	RO						RW	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_DCXO_REG0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 9]	RO	NA	0	
LDO_DCXO_LP_EN_SW	[8]	RW	NA	0	LDO_DCXO low power mode enable software control 0: depends on SLP_LDO_DCXO_LP_EN control 1: Enable
reserved	[7: 2]	RO	NA	0	
LDO_DCXO_SHPT_PD	[1]	RW	NA	0	LDO short protection power down
reserved	[0]	RO	NA	0	

13.1.1.31 LDO_DCXO_REG1

0x00000078	LDO_DCXO_REG1(0x0000003C)											LDO_DCXO_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								LDO_DCXO_V							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

LDO_DCXO_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
LDO_DCXO_V	[7: 0]	RW	NA	0x3c	DCXO LDO program bits: 8'b0 as 1.2V output, 10mV/step, 1.8V default,output range:1.8---3.3V

13.1.1.32 LDO_USB_REG0

0x0000007C	LDO_USB_REG0(0x00000000)											LDO_USB_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved							LDO_USB_LP_EN_SW	Reserved						LDO_USB_SHPT_PD	LDO_USB_PD
Type	RO							RW	RO						RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_USB_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 9]	RO	NA	0	
LDO_USB_LP_EN_SW	[8]	RW	NA	0	LDO_USB low power mode enable software control 0: depends on SLP_LDO_xxx_LP_EN control 1: Enable
reserved	[7: 2]	RO	NA	0	
LDO_USB_SHPT_PD	[1]	RW	NA	0	LDO short protection power down
LDO_USB_PD	[0]	RW	NA	0	LDO_USB33 power down 1: power down 0: power on

13.1.1.33 LDO_USB_REG1

0x00000080			LDO_USB_REG1(0x000000D2)									LDO_USB_REG1				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								LDO_USB_V							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0

LDO_USB_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

reserved	[15: 8]	RO	NA	0	
LDO_USB_V	[7: 0]	RW	NA	0xd2	USB LDO program bits: 8'b0 as 1.2V output, 10mV/step,3.3V default ,output range:1.8---3.3V

13.1.1.34 LDO_CAMD_REG0

0x00000084			LDO_CAMD_REG0(0x00000001)									LDO_CAMD_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							LDO_CAMD_LP_EN_SW	Reserved						LDO_CAMD_SHPT_PD	LDO_CAMD_PD
Type	RO							RW	RO						RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

LDO_CAMD_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 9]	RO	NA	0	
LDO_CAMD_LP_EN_SW	[8]	RW	NA	0	LDO_CAMD low power mode enable software control 0: depends on SLP_LDO_CAMD_LP_EN control 1: Enable
reserved	[7: 2]	RO	NA	0	
LDO_CAMD_SHPT_PD	[1]	RW	NA	0	LDO short protection power down
LDO_CAMD_PD	[0]	RW	NA	0x1	LDO_CAMD power down 1: power down 0: power on

13.1.1.35 LDO_CAMD_REG1

0x00000088			LDO_CAMD_REG1(0x0000003C)									LDO_CAMD_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								LDO_CAMD_V							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

LDO_CAMD_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
LDO_CAMD_V	[7: 0]	RW	NA	0x3c	CAMD LDO program bits: 8'b0 as 1.2V output, 10mV/step, 1.8V default,output range:1.8---3.3V

13.1.1.36 LDO_SF_REG0

0x0000008C		LDO_SF_REG0(0x00000000)									LDO_SF_REG0				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved					LDO_SF_V_SEL	LDO_SF_OPTION_O	LDO_SF_LP_EN_SW	Reserved						LDO_SF_SHPT_PD	Reserved
Type	RO					RW	RO	RW	RO						RW	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_SF_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 11]	RO	NA	0	
LDO_SF_V_SEL	[10]	RW	NA	0	LDO SF voltage select: 0: from bonding option 1: from software register
LDO_SF_OPTIO	[9]	RO	NA	0	VDDSF LDO Output voltage select

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

N_O					signal, "0" 1.8V (default) "1" 3.0V
LDO_SF_LP_EN_SW	[8]	RW	NA	0	LDO_SF low power mode enable software control 0: depends on SLP_LDO_SF_LP_EN control 1: Enable
reserved	[7: 2]	RO	NA	0	
LDO_SF_SHPT_PD	[1]	RW	NA	0	LDO short protection power down
reserved	[0]	RO	NA	0	

13.1.1.37 LDO_SF_REG1

0x00000090	LDO_SF_REG1(0x0000003C)											LDO_SF_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								LDO_SF_V							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

LDO_SF_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
LDO_SF_V	[7: 0]	RW	NA	0x3c	8'b0 as 1.2V , 1.8V default,10mv/step,output range:1.8---3.3V

13.1.1.38 LDO_VDD18_REG0

0x00000094	LDO_VDD18_REG0(0x00000000)											LDO_VDD18_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	Reserved							LDO_VDD18_LP_EN_SW	Reserved						LDO_VDD18_SHPT_PD	Reserved
Type	RO							RW	RO						RW	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_VDD18_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 9]	RO	NA	0	
LDO_VDD18_LP_EN_SW	[8]	RW	NA	0	LDO_VDD18 low power mode enable software control 0: depends on SLP_LDO_VDD18_LP_EN control 1: Enable
reserved	[7: 2]	RO	NA	0	
LDO_VDD18_SHPT_PD	[1]	RW	NA	0	LDO short protection power down
reserved	[0]	RO	NA	0	

13.1.1.39 LDO_VDD18_REG1

0x00000098			LDO_VDD18_REG1(0x0000003C)									LDO_VDD18_REG1				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								LDO_VDD18_V							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

LDO_VDD18_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
LDO_VDD18_V	[7: 0]	RW	NA	0x3c	VDD18 LDO program bits: 1.8~3.3

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					1.8V default,10mv/step

13.1.1.40 LDO_RF_REG0

0x0000009C			LDO_RF_REG0(0x00000000)									LDO_RF_REG0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved							LDO_RF_LP_EN_SW	Reserved						LDO_RF_SHPT_PD	LDO_RF_PD
Type	RO							RW	RO						RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_RF_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 9]	RO	NA	0	
LDO_RF_LP_EN_SW	[8]	RW	NA	0	LDO_RF low power mode enable software control 0: depends on SLP_LDO_RF_LP_EN control 1: Enable
reserved	[7: 2]	RO	NA	0	
LDO_RF_SHPT_PD	[1]	RW	NA	0	LDO short protection power down
LDO_RF_PD	[0]	RW	NA	0	LDO_RF power down 1: power down 0: power on

13.1.1.41 LDO_RF_REG1

0x000000A0			LDO_RF_REG1(0x00000060)									LDO_RF_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	Reserved									LDO_RF_V							
Type	RO									RW							
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	

LDO_RF_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 7]	RO	NA	0	
LDO_RF_V	[6: 0]	RW	NA	0x60	VDDRF LDO program bits: output:1.2V~2.0V; 10mV/step, default: 1.8V, 7h60;

13.1.1.42 LDO_CORE_REG0

0x000000A4	LDO_CORE_REG0(0x00000000)											LDO_CORE_REG0				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved							LDO_CORE_LP_EN_SW	Reserved						LDO_CORE_SHPT_PD	Reserved
Type	RO							RW	RO						RW	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_CORE_REG0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 9]	RO	NA	0	
LDO_CORE_LP_EN_SW	[8]	RW	NA	0	LDO_CORE low power mode enable software control 0: depends on SLP_LDO_CORE_LP_EN control 1: Enable
reserved	[7: 2]	RO	NA	0	
LDO_CORE_SHP	[1]	RW	NA	0	LDO short protection power down

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

T_PD					
reserved	[0]	RO	NA	0	

13.1.1.43 LDO_CORE_REG1

0x000000A8	LDO_CORE_REG1(0x00000023)											LDO_CORE_REG1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										LDO_CORE_V					
Type	RO										RW					
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1

LDO_CORE_REG1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 6]	RO	NA	0	
LDO_CORE_V	[5: 0]	RW	NA	0x23	VDDCORE LDO program bits; output voltage:0.75V~1.35V; 10mV/step, default: 1.1V

13.1.1.44 RESERVED_REG17

0x000000AC	RESERVED_REG17(0x00000000)											RESERVED_REG17				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG17

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

reserved	[15: 0]	RO	NA	0	

13.1.1.45 RESERVED_REG18

0x000000B0	RESERVED_REG18(0x00000000)											RESERVED_REG18				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG18

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.46 RESERVED_REG19

0x000000B4	RESERVED_REG19(0x00000000)											RESERVED_REG19				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG19

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

13.1.1.47 RESERVED_REG20

0x000000B8			RESERVED_REG20(0x00000000)									RESERVED_REG20				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG20

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.48 RESERVED_REG21

0x000000BC			RESERVED_REG21(0x00000000)									RESERVED_REG21				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG21

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.49 RESERVED_REG22

0x000000C0			RESERVED_REG22(0x00000000)									RESERVED_REG22				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG22

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.50 LDO_CH_CTRL

0x000000C4			LDO_CH_CTRL(0x00005000)									LDO_CH_CTRL				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved	EFS_PROG_SUP_PD	VBATBK_V		Reserved				LDOB_CAL_SEL				LDOA_CAL_SEL			
Type	RO	RW	RW		RO				RW				RW			
Reset	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0

LDO_CH_CTRL

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15]	RO	NA	0	
EFS_PROG_SUP_PD	[14]	RW	NA	0x1	Ddie efuse program mode power supply switch on/off control signal "1" switch off "0" switch on
VBATBK_V	[13: 12]	RW	NA	0x1	Backup battery output program bits 00: 2.6

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					01:2.8 (Default) 10:3.0 11:3.2
reserved	[11: 8]	RO	NA	0	
LDOB_CAL_SEL	[7: 4]	RW	NA	0	VBAT1 LDO TRIM CONTROL BITS: 0000: cal disable (default) 0001: LDO VDDCORE cal enable; 0010: LDO VDDRF cal enable; 0011: LDO VDDBTPA cal enable; 0100: LDO VDDDCXO cal enable; 0101: LDO VDD18 cal enable; 0110: LDO VDD28 cal enable; 0111: LDO_AVSS; 1000:LDO_AVSS; 1001:LDOB REF cal enable; 1010:LDODCXO REF cal enable; others: none
LDOA_CAL_SEL	[3: 0]	RW	NA	0	VBAT1 LDO TRIM CONTROL BITS: 0000: cal disable (default) 0001: LDO VDDSD cal enable; 0010: LDO VDDCAMA cal enable; 0011: LDO VDDCAMD cal enable; 0100: LDO VDDVIBR cal enable; 0101: LDO VDDSIM0 cal enable; 0110: LDO VDDSIM1 cal enable; 0111: LDO VDDSF cal enable; 1000:LDO VDDUSB cal enable; 1001:LDOA REF cal enable; others: none

13.1.1.51 LDO_REFTRIM_REG

0x000000C8	LDO_REFTRIM_REG(0x00004210)											LDO_REFTRIM_REG				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	LDODCXO_REFTRIM					LDOB_REFTRIM					LDOA_REFTRIM				
Type	RO	RW					RW					RW				
Reset	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0

LDO_REFTRIM_REG

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15]	RO	NA	0	
LDODCXO_REFTRIM	[14: 10]	RW	NA	0x10	LDOBTOP DCXOTRIM program bits: 8mV/step 1.2V default
LDOB_REFTRIM	[9: 5]	RW	NA	0x10	LDOBTOP TRIM program bits: 8mV/step 1.2V default
LDOA_REFTRIM	[4: 0]	RW	NA	0x10	LDOATOP TRIM program bits: 8mV/step 1.2V default

13.1.1.52 RESERVED_REG24

0x000000CC	RESERVED_REG24(0x00000000)											RESERVED_REG24				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG24

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.53 RESERVED_REG25

0x000000D0	RESERVED_REG25(0x00000000)											RESERVED_REG25				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG25

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.54 RESERVED_REG26

0x000000D4	RESERVED_REG26(0x00000000)											RESERVED_REG26				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG26

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.55 RESERVED_REG27

0x000000D8	RESERVED_REG27(0x00000000)											RESERVED_REG27				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG27

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

reserved	[15: 0]	RO	NA	0	

13.1.1.56 SLP_CTRL

0x000000DC	SLP_CTRL(0x00000000)											SLP_CTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												LDO_XTL_EN	Reserved	SLP_IO_EN	SLP_LDO_PD_EN
Type	RO												RW	RO	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLP_CTRL

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 4]	RO	NA	0	
LDO_XTL_EN	[3]	RW	NA	0	LDO and DCDC can be controlled by external device if this bit is set
reserved	[2]	RO	NA	0	
SLP_IO_EN	[1]	RW	NA	0	IO PAD sleep enable in deep sleep mode
SLP_LDO_PD_EN	[0]	RW	NA	0	ALL LDO and DCDC power down enable in deep sleep mode

13.1.1.57 SLP_LDO_PD_CTRL0

0x000000E0	SLP_LDO_PD_CTRL0(0x00000000)											SLP_LDO_PD_CTRL0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SLP_LDO_RF_PD_	SLP_LDO_SF_PD_E	SLP_LDO_DCXO_P	SLP_LDO_BTPA_P	SLP_LDO_VD28_P	SLP_LDO_SD_PD_	Reserved	SLP_LDO_USB_PD	Reserved	Reserved	SLP_LDO_CAMD_P	Reserved	SLP_LDO_CAMA_P	Reserved	SLP_LDO_SIM1_PD_	SLP_LDO_SIM0_PD_

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

	EN	N	D_EN	D_EN	D_EN	EN		_EN			D_EN		D_EN		EN	EN
Type	RW	RW	RW	RW	RW	RW	RO	RW	RO	RO	RW	RO	RW	RO	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLP_LDO_PD_CTRL0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
SLP_LDORF_PD_EN	[15]	RW	NA	0	LDO RF power down enable in deep sleep mode
SLP_LDOSF_PD_EN	[14]	RW	NA	0	LDO SF power down enable in deep sleep mode
SLP_LDODCXO_PD_EN	[13]	RW	NA	0	LDO DCXO power down enable in deep sleep mode
SLP_LDOBTPA_PD_EN	[12]	RW	NA	0	LDO BTPA power down enable in deep sleep mode
SLP_LDOVDD28_PD_EN	[11]	RW	NA	0	LDO VDD28 power down enable in deep sleep mode
SLP_LDOSD_PD_EN	[10]	RW	NA	0	LDO SD power down enable in deep sleep mode
reserved	[9]	RO	NA	0	
SLP_LDOUSB_PD_EN	[8]	RW	NA	0	LDO USB power down enable in deep sleep mode
reserved	[7]	RO	NA	0	
reserved	[6]	RO	NA	0	
SLP_LDOCAMD_PD_EN	[5]	RW	NA	0	LDO CAMD power down enable in deep sleep mode
reserved	[4]	RO	NA	0	
SLP_LDOCAMA_PD_EN	[3]	RW	NA	0	LDO CAMA power down enable in deep sleep mode
reserved	[2]	RO	NA	0	
SLP_LDOSIM1_PD_EN	[1]	RW	NA	0	LDO SIM1 power down enable in deep sleep mode
SLP_LDOSIM0_PD_EN	[0]	RW	NA	0	LDO SIM0 power down enable in deep sleep mode

13.1.1.58 SLP_LDO_LP_CTRL0

0x000000E4	SLP_LDO_LP_CTRL0(0x00000000)											SLP_LDO_LP_CTRL0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	SLP_LDORF_LP_EN	SLP_LDOSF_LP_EN	SLP_LDODCXO_LP_EN	Reserved	SLP_LDOVDD28_LP_EN	SLP_LDOSD_LP_EN	SLP_LDOVDD18_LP_EN	SLP_LDOUSB_LP_EN	Reserved	Reserved	SLP_LDOCAMD_LP_EN	Reserved	SLP_LDOCAMA_LP_EN	SLP_LDOCORE_LP_EN	SLP_LDOSIM1_LP_EN	SLP_LDOSIM0_LP_EN
Type	RW	RW	RW	RO	RW	RW	RW	RW	RO	RO	RW	RO	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLP_LDO_LP_CTRL0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
SLP_LDORF_LP_EN	[15]	RW	NA	0	LDO RF low power mode enable in deep sleep mode
SLP_LDOSF_LP_EN	[14]	RW	NA	0	LDO SF low power mode enable in deep sleep mode
SLP_LDODCXO_LP_EN	[13]	RW	NA	0	LDO DCXO low power mode enable in deep sleep mode
reserved	[12]	RO	NA	0	
SLP_LDOVDD28_LP_EN	[11]	RW	NA	0	LDO VDD28 low power mode enable in deep sleep mode
SLP_LDOSD_LP_EN	[10]	RW	NA	0	LDO SD low power mode enable in deep sleep mode 0: Disable 1: Enable
SLP_LDOVDD18_LP_EN	[9]	RW	NA	0	LDO VDD18 low power mode enable in deep sleep mode
SLP_LDOUSB_LP_EN	[8]	RW	NA	0	LDO USB low power mode enable in deep sleep mode 0: Disable 1: Enable
reserved	[7]	RO	NA	0	
reserved	[6]	RO	NA	0	
SLP_LDOCAMD_LP_EN	[5]	RW	NA	0	LDO CAMD low power mode enable in deep sleep mode 0: Disable 1: Enable
reserved	[4]	RO	NA	0	
SLP_LDOCAMA_LP_EN	[3]	RW	NA	0	LDO CAMA low power mode enable in deep sleep mode 0: Disable 1: Enable
SLP_LDOCORE_LP_EN	[2]	RW	NA	0	LDO CORE low power mode enable in deep sleep mode 0: Disable

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					1: Enable
SLP_LDOSIM1_LP_EN	[1]	RW	NA	0	LDO SIM1 low power mode enable in deep sleep mode 0: Disable 1: Enable
SLP_LDOSIM0_LP_EN	[0]	RW	NA	0	LDO SIM0 low power mode enable in deep sleep mode 0: Disable 1: Enable

13.1.1.59 LDO_CORE_SLP_CTRL0

0x000000E8			LDO_CORE_SLP_CTRL0(0x00000000)									LDO_CORE_SLP_CTRL0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								Reserved					SLP_LDO CORE_DROP_EN	LDO_CORE_SLP_OUT_STEP_EN	LDO_CORE_SLP_IN_STEP_EN
Type	RO								RO					RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_CORE_SLP_CTRL0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
reserved	[7: 3]	RO	NA	0	
SLP_LDOCORE_DROP_EN	[2]	RW	NA	0	LDO CORE power drop enable in deep sleep mode
LDO_CORE_SLP_OUT_STEP_EN	[1]	RW	NA	0	LDO CORE wakeup voltage step enable
LDO_CORE_SLP_IN_STEP_EN	[0]	RW	NA	0	LDO CORE sleep voltage step enable

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

13.1.1.60 LDO_CORE_SLP_CTRL1

0x000000EC			LDO_CORE_SLP_CTRL1(0x00000080)									LDO_CORE_SLP_CTRL1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				LDO_CORE_V_SLP_STEP1						LDO_CORE_V_DS					
Type	RO				RW						RW					
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

LDO_CORE_SLP_CTRL1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 12]	RO	NA	0	
LDO_CORE_V_SLP_STEP1	[11: 6]	RW	NA	0x2	LDO CORE sleep control of step1
LDO_CORE_V_DS	[5: 0]	RW	NA	0	LDO CORE control bits in deep sleep mode

13.1.1.61 LDO_CORE_SLP_CTRL2

0x000000F0			LDO_CORE_SLP_CTRL2(0x000001C4)									LDO_CORE_SLP_CTRL2				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				LDO_CORE_V_SLP_STEP3						LDO_CORE_V_SLP_STEP2					
Type	RO				RW						RW					
Reset	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0

LDO_CORE_SLP_CTRL2

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 12]	RO	NA	0	
LDO_CORE_V_SLP_STEP3	[11: 6]	RW	NA	0x7	LDO CORE sleep control of step3
LDO_CORE_V_S	[5: 0]	RW	NA	0x4	LDO CORE sleep control of step2

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

LP_STEP2					

13.1.1.62 LDO_CORE_SLP_CTRL3

0x000000F4			LDO_CORE_SLP_CTRL3(0x0000034A)									LDO_CORE_SLP_CTRL3				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				LDO_CORE_V_SLP_STEP5						LDO_CORE_V_SLP_STEP4					
Type	RO				RW						RW					
Reset	0	0	0	0	0	0	1	1	0	1	0	0	1	0	1	0

LDO_CORE_SLP_CTRL3

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 12]	RO	NA	0	
LDO_CORE_V_SLP_STEP5	[11: 6]	RW	NA	0xd	LDO CORE sleep control of step5
LDO_CORE_V_SLP_STEP4	[5: 0]	RW	NA	0xa	LDO CORE sleep control of step4

13.1.1.63 LDO_XTL_EN0

0x000000F8			LDO_XTL_EN0(0x00000000)									LDO_XTL_EN0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LDO_DCXO_EXT_XTL_EN	LDO_DCXO_XTL_BUF_EN	LDO_CORE_EXT_XTL_EN	LDO_CORE_XTL_BUF_EN	LDO_SIM0_EXT_XTL_EN	LDO_SIM0_XTL_BUF_EN	LDO_SIM1_EXT_XTL_EN	LDO_SIM1_XTL_BUF_EN	LDO_CAMA_EXT_XTL_EN	LDO_CAMA_XTL_BUF_EN	LDO_CAMD_EXT_XTL_EN	LDO_CAMD_XTL_BUF_EN	LDO_VDD18_EXT_XTL_EN	LDO_VDD18_XTL_BUF_EN	LDO_VDD28_EXT_XTL_EN	LDO_VDD28_XTL_BUF_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_XTL_EN0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
LDO_DCXO_EXT_XTL_EN	[15]	RW	NA	0	LDO DCXO can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_DCXO_XTL_BUF_EN	[14]	RW	NA	0	LDO DCXO can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_CORE_EXT_XTL_EN	[13]	RW	NA	0	LDO CORE can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_CORE_XTL_BUF_EN	[12]	RW	NA	0	LDO CORE can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_SIM0_EXT_XTL_EN	[11]	RW	NA	0	LDO SIM0 can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_SIM0_XTL_BUF_EN	[10]	RW	NA	0	LDO SIM0 can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_SIM1_EXT_XTL_EN	[9]	RW	NA	0	LDO SIM1 can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_SIM1_XTL_BUF_EN	[8]	RW	NA	0	LDO SIM1 can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_CAMA_EXT_XTL_EN	[7]	RW	NA	0	LDO CAMA can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_CAMA_XTL_BUF_EN	[6]	RW	NA	0	LDO CAMA can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_CAMD_EXT_XTL_EN	[5]	RW	NA	0	LDO CAMD can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_CAMD_XTL_BUF_EN	[4]	RW	NA	0	LDO CAMD can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_VDD18_EXT_XTL_EN	[3]	RW	NA	0	LDO VDD18 can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_VDD18_XTL_BUF_EN	[2]	RW	NA	0	LDO VDD18 can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_VDD28_EXT_XTL_EN	[1]	RW	NA	0	LDO VDD28 can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_VDD28_XTL_BUF_EN	[0]	RW	NA	0	LDO VDD28 can be controlled by XTL_BUF_EN(from PAD) if this bit is set

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

13.1.1.64 LDO_XTL_EN1

0x000000FC			LDO_XTL_EN1(0x00000000)									LDO_XTL_EN1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LDO_RF_EXT_XTL_EN	LDO_RF_XTL_BUF_EN	LDO_SF_EXT_XTL_EN	LDO_SF_XTL_BUF_EN	Reserved				LDO_VIBR_EXT_XTL_EN	LDO_VIBR_XTL_BUF_EN	LDO_USB_EXT_XTL_EN	LDO_USB_XTL_BUF_EN	LDO_BTPA_EXT_XTL_EN	LDO_BTPA_XTL_BUF_EN	LDO_SD_EXT_XTL_EN	LDO_SD_XTL_BUF_EN
Type	RW	RW	RW	RW	RO				RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LDO_XTL_EN1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
LDO_RF_EXT_XTL_EN	[15]	RW	NA	0	LDO RF can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_RF_XTL_BUF_EN	[14]	RW	NA	0	LDO RF can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_SF_EXT_XTL_EN	[13]	RW	NA	0	LDO SF can be cotrolled by EXT_XTL_EN(from PAD) if this bit is set
LDO_SF_XTL_BUF_EN	[12]	RW	NA	0	LDO SF can be controlled by XTL_BUF_EN(from PAD) if this bit is set
reserved	[11: 8]	RO	NA	0	
LDO_VIBR_EXT_XTL_EN	[7]	RW	NA	0	LDO VIBR can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_VIBR_XTL_BUF_EN	[6]	RW	NA	0	LDO VIBR can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_USB_EXT_XTL_EN	[5]	RW	NA	0	LDO USB can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_USB_XTL_BUF_EN	[4]	RW	NA	0	LDO USB can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_BTPA_EXT_XTL_EN	[3]	RW	NA	0	LDO BTPA can be controlled by EXT_XTL_EN(from PAD) if this bit is

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					set
LDO_BTPA_XTL_BUF_EN	[2]	RW	NA	0	LDO BTPA can be controlled by XTL_BUF_EN(from PAD) if this bit is set
LDO_SD_EXT_XTL_EN	[1]	RW	NA	0	LDO SD can be controlled by EXT_XTL_EN(from PAD) if this bit is set
LDO_SD_XTL_BUF_EN	[0]	RW	NA	0	LDO SD can be controlled by XTL_BUF_EN(from PAD) if this bit is set

13.1.1.65 XO_BG_XTL_EN

0x00000100	XO_BG_XTL_EN(0x00000000)											XO_BG_XTL_EN				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DCXO_EXT_XTL_EN	DCXO_XTL_BUF_EN	Reserved													
Type	RW	RW	RO													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

XO_BG_XTL_EN

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
DCXO_EXT_XTL_EN	[15]	RW	NA	0	DCXO can be controlled by EXT_XTL_EN(from PAD) if this bit is set
DCXO_XTL_BUF_EN	[14]	RW	NA	0	DCXO can be controlled by XTL_BUF_EN(from PAD) if this bit is set
reserved	[13: 0]	RO	NA	0	

13.1.1.66 RESERVED_REG29

0x00000104	RESERVED_REG29(0x00000000)											RESERVED_REG29				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG29

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.67 RESERVED_REG30

0x00000108			RESERVED_REG30(0x00000000)									RESERVED_REG30				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG30

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.68 RESERVED_REG31

0x0000010C			RESERVED_REG31(0x00000000)									RESERVED_REG31				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG31

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.69 RESERVED_REG32

0x00000110	RESERVED_REG32(0x00000000)											RESERVED_REG32				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG32

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.70 RESERVED_REG33

0x00000114	RESERVED_REG33(0x00000000)											RESERVED_REG33				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG33

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.71 RESERVED_REG34

0x00000118			RESERVED_REG34(0x00000000)									RESERVED_REG34				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG34

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.72 CLK32KLESS_CTRL0

0x0000011C			CLK32KLESS_CTRL0(0x00000000)									CLK32KLESS_CTRL0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	RC_MODE_WR_ACK_FLAG	XO_LOW_CUR_FLAG	XO_LOW_CUR_FRC_RTCSET	XO_LOW_CUR_FRC_RTCCLR	RC_MODE_WR_ACK_FLAG_CLR	XO_LOW_CUR_FLAG_CLR	XO_LOW_CUR_CNT_CLR	LDO_DCXO_LP_EN_RTCSET	LDO_DCXO_LP_EN_RTCCLR	SLP_XO_LOW_CUR_EN	Reserved	XO_LOW_CUR_EN	Reserved	RC_32K_SEL	RC_32K_EN
Type	RO	RO	RO	RW	RW	WC	WC	WC	RW	RW	RW	RO	RW	RO	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

CLK32KLESS_CTRL0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15]	RO	NA	0	
RC_MODE_WR_ACK_FLAG	[14]	RO	NA	0	RC_MODE write ack flag
XO_LOW_CUR_FLAG	[13]	RO	NA	0	DCXO sleep low current mode flag, active if DCXO falls into low current mode in chip sleep.
XO_LOW_CUR_FRC_RTCSET	[12]	RW	NA	0	Force DCXO into low current mode RTC SET
XO_LOW_CUR_FRC_RTCCLR	[11]	RW	NA	0	Force DCXO into low current mode RTC CLR
RC_MODE_WR_ACK_FLAG_CLR	[10]	WC	NA	0	RC_MODE write ack flag clear, high effective
XO_LOW_CUR_FLAG_CLR	[9]	WC	NA	0	DCXO low current mode flag clear, high effective
XO_LOW_CUR_CNT_CLR	[8]	WC	NA	0	DCXO low current counter clear, high effective
LDO_DCXO_LP_EN_RTCSET	[7]	RW	NA	0	Low power LDO_DCXO power down set in RTC
LDO_DCXO_LP_EN_RTCCLR	[6]	RW	NA	0	Low power LDO_DCXO power down clear in RTC
SLP_XO_LOW_CUR_EN	[5]	RW	NA	0	DCXO low current mode enable in chip sleep mode
reserved	[4]	RO	NA	0	
XO_LOW_CUR_EN	[3]	RW	NA	0	Force DCXO into low current mode
reserved	[2]	RO	NA	0	
RC_32K_SEL	[1]	RW	NA	0	32K clock select in 32K crystal removal option 0: From XO 1: From RC
RC_32K_EN	[0]	RW	NA	0	RC 32K oscillator enable

13.1.1.73 CLK32KLESS_CTRL1

0x00000120	CLK32KLESS_CTRL1(0x00000000)											CLK32KLESS_CTRL1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RC_MODE															
Type	RW															

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CLK32KLESS_CTRL1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RC_MODE	[15: 0]	RW	NA	0	RC 32K mode in battery drop case: 16'h95A5: RC oscillator stop working. Others: RC oscillator keep working.

13.1.1.74 CLK32KLESS_CTRL2

0x00000124	CLK32KLESS_CTRL2(0x00000000)											CLK32KLESS_CTRL2				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	XO_LOW_CUR_CNT_LOW															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CLK32KLESS_CTRL2

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
XO_LOW_CUR_CNT_LOW	[15: 0]	RO	NA	0	Low 16bits of DCXO low current mode counter to indicate how long DCXO falls into this mode. The unit is 30.5us.

13.1.1.75 CLK32KLESS_CTRL3

0x00000128	CLK32KLESS_CTRL3(0x00000000)											CLK32KLESS_CTRL3				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	XO_LOW_CUR_CNT_HIGH															
Type	RO															

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CLK32KLESS_CTRL3

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
XO_LOW_CUR_CNT_HIGH	[15: 0]	RO	NA	0	High 16bits of DCXO low current mode counter to indicate how long DCXO falls into this mode. The unit is 30.5us.

13.1.1.76 CLK32KLESS_CTRL4

0x0000012C			CLK32KLESS_CTRL4(0x00000008)									CLK32KLESS_CTRL4				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												RC1M_CAL			
Type	RO												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

CLK32KLESS_CTRL4

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 4]	RO	NA	0	
RC1M_CAL	[3: 0]	RW	NA	0x8	RC Calibration bit,step 7%

13.1.1.77 AUXAD_CTL

0x00000130			AUXAD_CTL(0x00000000)									AUXAD_CTL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	AUXAD_RESERVED				Reserved	Reserved	Reserved	AUXAD_REF_S	AUXAD_CURR	Reserved	Reserved				

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

									EL	ENTSEN_EN							
Type	RO	RW				RO	RO	RO	RW	RW	RO	RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

AUXAD_CTL

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15]	RO	NA	0	
AUXAD_RESERVED	[14: 11]	RW	NA	0	RG_AUX_RESERVED[3:1]: reserved bit RG_AUX_RESERVED[0]: HALF_VREF connect to Channel9
reserved	[10]	RO	NA	0	
reserved	[9]	RO	NA	0	
reserved	[8]	RO	NA	0	
AUXAD_REF_SEL	[7]	RW	NA	0	ADC reference source selection, 0: from ADC inner reference gen by current from bandgap (default) 1: from bandgap 1.2V voltage reference
AUXAD_CURRENTSEN_EN	[6]	RW	NA	0	Aux ADC current sense enable signal, active high
reserved	[5]	RO	NA	0	
reserved	[4: 0]	RO	NA	0	

13.1.1.78 XTL_WAIT_CTRL

0x00000134			XTL_WAIT_CTRL(0x00000232)									XTL_WAIT_CTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	AUDIO_FORCE_ON	Reserved	Reserved		XTL_BUF_FOR_26M_EN	EXT_XTL_FOR_26M_EN	SLP_XTLBUF_PD_EN	XTL_EN	XTL_WAIT							
Type	RW	RO	RO		RW	RW	RW	RW	RW							

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reset	0	0	0	0	0	0	1	0	0	0	1	1	0	0	1	0

XTL_WAIT_CTRL

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
AUDIO_FORCE_ON	[15]	RW	NA	0	audio 26M path force on "1" force on "0" Not force on
reserved	[14]	RO	NA	0	
reserved	[13: 12]	RO	NA	0	
XTL_BUF_FOR_26M_EN	[11]	RW	NA	0	26M wake up enable by ext_xtl1_en
EXT_XTL_FOR_26M_EN	[10]	RW	NA	0	26M wake up enable by ext_xtl0_en
SLP_XTLBUF_PD_EN	[9]	RW	NA	0x1	26MHz crystal oscillator power down enable in deep sleep mode
XTL_EN	[8]	RW	NA	0	26MHz crystal oscillator output enable
XTL_WAIT	[7: 0]	RW	NA	0x32	26MHz crystal oscillator wait cycles

13.1.1.79 IB_CTRL

0x00000138	IB_CTRL(0x00000080)											IB_CTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved			IB_CUR_EN	IB_CUR_I			IB_CAL_EN	IB_TRIM						Reserved	
Type	RO			RW	RW			RW	RW						RO	
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

IB_CTRL

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 13]	RO	NA	0	
IB_CUR_EN	[12]	RW	NA	0	current mode enable "0" disable (default) "1" enable (default)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

IB_CUR_I	[11: 9]	RW	NA	0	set current level in current mode bit2~bit0 effective 1.25/2.5/5/10/20/40/80/160uA 7step
IB_CAL_EN	[8]	RW	NA	0	IB trim test mode enable singnal
IB_TRIM	[7: 2]	RW	NA	0x20	Internal resistor for sink current calibration bit.step 1%
reserved	[1: 0]	RO	NA	0	

13.1.1.80 WHTLED_CTRL

0x0000013C			WHTLED_CTRL(0x00000001)									WHTLED_CTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								WHTLED_PD_SEL	Reserved		WHTLED_V				WHTLED_PD
Type	RO								RW	RO		RW				RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

WHTLED_CTRL

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
WHTLED_PD_SEL	[7]	RW	NA	0	White LED driver power down control selection 0: From Software Register 1: From Hareware Auto Control
reserved	[6: 5]	RO	NA	0	
WHTLED_V	[4: 1]	RW	NA	0	Current control bit. 16 steps Min current: 3.125mA ("0000") Max current: 50mA("1111") (default 4'b0)
WHTLED_PD	[0]	RW	NA	0x1	White LED driver power down "1" power down "0" enable PWM signal when WHTLED_V<5:0> = 6'b0 Min current: 0.156mA

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					One step is 0.156mA

13.1.1.81 KPLED_CTRL

0x00000140	KPLED_CTRL(0x00000800)											KPLED_CTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	KPLED_V				KPLED_PD	Reserved										
Type	RW				RW	RO										
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

KPLED_CTRL

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
KPLED_V	[15: 12]	RW	NA	0	Current control bit. 16 steps Min current: 0.9mA ("0000") Max current: 79.2mA("1111") (default 4'b0) 0.9/1.8/2.7/3.6/4.5/5.4/6.3/10.8/16.2/22.5/29.7/37.8/46.8/56.7/67.5/79.2 16 step
KPLED_PD	[11]	RW	NA	0x1	Key PAD LED driver power down "1" power down (default) "0" enable
reserved	[10: 0]	RO	NA	0	

13.1.1.82 VIBR_CTRL

0x00000144	VIBR_CTRL0(0x000003B4)											VIBR_CTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	Reserved					SLP_LDOVIB	LDO_VIBR_	LDO_VIBR_V							

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

							R_PD_EN	PD								
Type	RO	RO					RW	RW	RW							
Reset	0	0	0	0	0	0	1	1	1	0	1	1	0	1	0	0

VIBR_CTRL0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15]	RO	NA	0	
reserved	[14: 10]	RO	NA	0	
SLP_LDOVIBR_PD_EN	[9]	RW	NA	0x1	Vibrator LDO sleep power down enable
LDO_VIBR_PD	[8]	RW	NA	0x1	VIBR LDO power down signal
LDO_VIBR_V	[7: 0]	RW	NA	0xb4	VIBR LDO program bits: 8'b0 as 1.2V output, 10mV/step Default output 3.0V

13.1.1.83 AUDIO_CTRL0

0x00000148	AUDIO_CTRL0(0x00001908)										AUDIO_CTRL0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	AUD_SLP_APP_RST_EN	Reserved		CLK_AUD_HBD_DIV					Reserved			CLK_AUD_LOOP_INV_EN	CLK_AUD_IF_TX_INV_EN	CLK_AUD_IF_RX_INV_EN	CLK_AUD_IF_6P5M_TX_INV_EN	CLK_AUD_IF_6P5M_RX_INV_EN
Type	RW	RO		RW					RO			RW	RW	RW	RW	RW
Reset	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0

AUDIO_CTRL0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

AUD_SLP_APP_RST_EN	[15]	RW	NA	0	audio sleep reset eanble . 0: chip_deep_slp can not effect the audio 1: chip_deep_slp can reset clk_aud_hbd and clk_aud_hid domain
reserved	[14: 13]	RO	NA	0	
CLK_AUD_HBD_DIV	[12: 8]	RW	NA	0x19	clk_aud_hbd divider
reserved	[7: 5]	RO	NA	0	
CLK_AUD_LOOP_INV_EN	[4]	RW	NA	0	Whether Adie audio controller use inverse of clk_aud_loop 0: No 1: Yes
CLK_AUD_IF_TX_INV_EN	[3]	RW	NA	0x1	Whether Adie use inverse of clk_audif to sample Ddie tx data 0: No 1: Yes
CLK_AUD_IF_RX_INV_EN	[2]	RW	NA	0	Whether Adie use inverse of clk_aud6m5 to send rx data to Ddie 0: No 1: Yes
CLK_AUD_IF_6P5M_TX_INV_EN	[1]	RW	NA	0	Whether Adie audio controller use inverse of clk_aud6m5 in tx path 0: No 1: Yes
CLK_AUD_IF_6P5M_RX_INV_EN	[0]	RW	NA	0	Whether Adie audio controller use inverse of clk_aud6m5 in rx path 0: No 1: Yes

13.1.1.84 AUDIO_CTRL1

0x0000014C			AUDIO_CTRL1(0x0000000C)									AUDIO_CTRL1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved									HEAD_INSERT_EIC_EN	AUDIO_CHP_CLK_DIV_EN	AUDIO_CHP_CLK_DIV				
Type	RO									RW	RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

AUDIO_CTRL1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 7]	RO	NA	0	
HEAD_INSERT_EIC_EN	[6]	RW	NA	0	EIC[5] input select 0: AUDIO_HEAD_INSERT2 1: AUDIO_HEAD_INSERT
AUDIO_CHP_CLK_DIV_EN	[5]	RW	NA	0	AUDIO_CHP_CLK divide enable
AUDIO_CHP_CLK_DIV	[4: 0]	RW	NA	0xc	AUDIO_CHP_CLK divide parameter

13.1.1.85 CHGR_CTRL0

0x00000150	CHGR_CTRL0(0x00000400)											CHGR_CTRL0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	Reserved	Reserved		CHGR_CV_V						CHGR_END_V		Reserved			CHGR_PD
Type	RO	RO	RO		RW						RW		RO			RW
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

CHGR_CTRL0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15]	RO	NA	0	
reserved	[14]	RO	NA	0	
reserved	[13: 12]	RO	NA	0	
CHGR_CV_V	[11: 6]	RW	NA	0x10	Charger battery sense DAC (CC-CV trans-point control)
CHGR_END_V	[5: 4]	RW	NA	0	Charger battery charging end voltage 00: Vend=4.2V 01: Vend=4.3V 10: Vend=4.4V 11: Vend=4.5V

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

reserved	[3: 1]	RO	NA	0	
CHGR_PD	[0]	RW	NA	0	"1" charger power down "0" charger power up

13.1.1.86 CHGR_CTRL1

0x00000154	CHGR_CTRL1(0x0000000E)										CHGR_CTRL1					
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved	CHGR_CC_I					VBAT_OVP_V				VCHG_OVP_V					
Type	RO	RW					RW				RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

CHGR_CTRL1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15]	RO	NA	0	
CHGR_CC_I	[14: 10]	RW	NA	0	CC mode charging current 00000:300mA 00001 : 350 00010: 400mA 00011 : 450 00100: 500mA 00101 :550 00110: 600mA 00111: 650 01000: 700mA 01001: 750 01010: 800mA 01011: 850 01100: 900mA 01101: 950 01110: 1000mA 01111: 1050 10000: 1100mA 10001: 1150 10010: 1200mA 10011: 1250 10100: 1300mA 10101: 1350 10110: 1400mA 10111: 1500 11000: 1600mA 11001: 1700 11010: 1800mA 11011: 1900 11100: 2000mA 11101: 2100 11110: 2200mA 11111: 2300 Default5'b0
VBAT_OVP_V	[9: 6]	RW	NA	0	control bits of over voltage protection for VBAT. When VBAT is above some level set by these 4 bits, charger power down and VBAT_OVI becomes high.

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					0000: 4.25V(protection voltage) 0001: 4.275V 0010: 4.3V 0011: 4.325V 0100: 4.35V 0101: 4.375V 0110: 4.4V 0111: 4.425V 1000: 4.45V 1001: 4.475V 1010: 4.5V 1011: 4.525V 1100: 4.55V 1101: 4.575V 1110: 4.6V 1111: 4.625V Default4'b0
VCHG_OVP_V	[5: 0]	RW	NA	0xe	control bits of over voltage protection for VCHG. When VCHG is above some level set by these 6 bits, charger power down and CHGR_OVI becomes high. 000000: 5.6V(protection voltage) 000001: 5.7V 000010: 5.8V 000011: 5.9V 000100: 6.0V 000101: 6.1V 000110: 6.2V 000111: 6.3V 001000: 6.4V 001001: 6.5V 001010: 6.6V 001011: 6.7V 001100: 6.8V 001101: 6.9V 001110: 7.0V 001111: 7.1V 010000: 7.2V 010001: 7.3V 010010: 7.4V 010011: 7.5V 010100: 7.6V 010101: 7.7V 010110: 7.8V 010111: 7.9V 011000: 8.0V 011001: 8.1V 011010: 8.2V 011011: 8.3V 011100: 8.4V 011101: 8.5V 011110: 8.6V

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					011111: 8.7V 100000: 8.8V 100001: 8.9V 100010: 9.0V 100011: 9.1V 100100: 9.2V 100101: 9.3V 100110: 9.4V 100111: 9.5V 101000: 9.6V 101001: 9.7V 101010: 9.7V …… 111111: 9.7V Default 6'b001110

13.1.1.87 CHGR_CTRL2

0x00000158			CHGR_CTRL2(0x00000000)									CHGR_CTRL2				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved		Reserved						CHGR_DRV	CHGR_OSC	CHGR_DPM		CHGR_ITERM		CHGR_CC_EN	RECHG
Type	RO		RO						RW	RW	RW		RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CHGR_CTRL2

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15]	RO	NA	0	
reserved	[14: 8]	RO	NA	0	
CHGR_DRV	[7]	RW	NA	0	CHGR_DRV
CHGR_OSC	[6]	RW	NA	0	CHGR_OSC
CHGR_DPM	[5: 4]	RW	NA	0	CHGR_DPM
CHGR_ITERM	[3: 2]	RW	NA	0	Termination charger current programmable bits 00:cc*0.9 01:cc*0.4 10:cc*0.2

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					11:cc*0.1
CHGR_CC_EN	[1]	RW	NA	0	Select charger CC mode enable, high effective, Default "0"
RECHG	[0]	RW	NA	0	Charging software start up flag, high effective

13.1.1.88 CHGR_STATUS

0x0000015C			CHGR_STATUS(0x00000000)									CHGR_STATUS				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved											CHGR_CV_STATUS	CHGR_ON	CHGR_INT	VBAT_OVI	VCHG_OVI
Type	RO											RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CHGR_STATUS

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 5]	RO	NA	0	
CHGR_CV_STATUS	[4]	RO	NA	0	Flag when charging current below some level(0.5*full current) in CV mode High effective
CHGR_ON	[3]	RO	NA	0	Charger voltage ready indicator, high effective When VCHG<4.1V: "0" When VCHG>4.3V: "1"
CHGR_INT	[2]	RO	NA	0	Charger present indicator, high effective When VCHG<3.1V: "0" When VCHG>3.3V: "1"
VBAT_OVI	[1]	RO	NA	0	VBAT over voltage(programmable) flag When VBAT higher than some voltage set by VBAT_OVP_V<3:0> and lasts 2mS, VBAT_OVI="1" The hysteresis voltage is 25mV.
VCHG_OVI	[0]	RO	NA	0	VCHG over voltage(programmable) flag

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					When VCHG higher than some voltage set by VCHG_OVP_V<5:0> and lasts 2mS, CHGR_OVI="1" The hysteresis voltage is 600mV.

13.1.1.89 MIXED_CTRL0

0x00000160	MIXED_CTRL0(0x00000200)											MIXED_CTRL0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PTEST_PD_RTCSET	Reserved	Reserved	OPT_AUTO_PWON_O	VBAT_CRASH_V		OVLO_EN	Reserved					OVLO_V		OVLO_T	
Type	RW	RO	RO	RO	RW		RW	RO					RW		RW	
Reset	0	0	0	X	0	0	1	0	0	0	0	0	0	0	0	0

MIXED_CTRL0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
PTEST_PD_RTCSET	[15]	RW	NA	0	PTEST PD mode set
reserved	[14]	RO	NA	0	
reserved	[13]	RO	NA	0	
OPT_AUTO_PWON_O	[12]	RO	NA	1'hx	Power on mode, 0:no self test when vbat ready(default) 1:self test when vbat ready
VBAT_CRASH_V	[11: 10]	RW	NA	0	Battery crash voltage setting: 00: 2.1V (default) 01: 2.2V 10: 2.3V 11: 2.5V
OVLO_EN	[9]	RW	NA	0x1	Over voltage locked-out enable (high effective) Default "1"
reserved	[8: 4]	RO	NA	0	
OVLO_V	[3: 2]	RW	NA	0	Over voltage locked-out detecting time 00 : 4.8V (default)

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					01 : 5.0V 10 : 4.6V 11 : 4.2V
OVLO_T	[1: 0]	RW	NA	0	Over voltage locked-out detecting time 00 : 1ms (default) 01 : 0.5ms 10 : 0.25ms 11 : 2ms

13.1.1.90 MIXED_CTRL1

0x00000164			MIXED_CTRL1(0x00000000)									MIXED_CTRL1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				BATON_T		BATDET_OK	Reserved	Reserved	Reserved		Reserved	ALL_GPI_DEB	GPI_DEBUG_EN	ALL_INT_DEB	INT_DEBUG_EN
Type	RO				RW		RO	RO	RO	RO		RO	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIXED_CTRL1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 12]	RO	NA	0	
BATON_T	[11: 10]	RW	NA	0	Control bit of de-glitch time for battery remove "00" 32us "01" 64us "10" 128us "11" no de-glitch default"00"
BATDET_OK	[9]	RO	NA	0	Battery presence flag to SW and POCV, so need RTC domain "0" no battery "1" battery presence
reserved	[8]	RO	NA	0	
reserved	[7]	RO	NA	0	
reserved	[6: 5]	RO	NA	0	
reserved	[4]	RO	NA	0	
ALL_GPI_DEB	[3]	RW	NA	0	ALL GPI source debug
GPI_DEBUG_EN	[2]	RW	NA	0	GPI debug enable

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

ALL_INT_DEB	[1]	RW	NA	0	ALL_INT debug, if 1, interrupt will be sent
INT_DEBUG_EN	[0]	RW	NA	0	Interupt debug enable

13.1.1.91 POR_RST_MONITOR

0x00000168			POR_RST_MONITOR(0x00000000)									POR_RST_MONITOR				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	POR_RST_MONITOR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

POR_RST_MONITOR

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
POR_RST_MONITOR	[15: 0]	RW	NA	0	When POR reset active, this register is reset to 0

13.1.1.92 WDG_RST_MONITOR

0x0000016C			WDG_RST_MONITOR(0x00000000)									WDG_RST_MONITOR				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	WDG_RST_MONITOR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WDG_RST_MONITOR

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
WDG_RST_MONITOR	[15: 0]	RW	NA	0	When WDG reset active, this register is reset to 0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

13.1.1.93 POR_PIN_RST_MONITOR

0x00000170			POR_PIN_RST_MONITOR(0x00000000)									POR_PIN_RST_MONITOR				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	POR_PIN_RST_MONITOR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

POR_PIN_RST_MONITOR

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
POR_PIN_RST_MONITOR	[15: 0]	RW	NA	0	When POR_EXT_RST active, this register is reset to 0

13.1.1.94 POR_SRC_FLAG

0x00000174			POR_SRC_FLAG(0x00000000)									POR_SRC_FLAG				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	POR_SW_FORCE_ON	POR_SRC_FLAG														
Type	RW	RO														
Reset	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

POR_SRC_FLAG

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

POR_SW_FORCE_ON	[15]	RW	NA	0	Setting this bit could disable the 1S debouncing time of power key after boot.
POR_SRC_FLAG	[14: 0]	RO	NA	15'hx	Power on source flag: [0]: Debounced PBINT signal, set when PBINT=0 >50ms, clear when PBINT=1>50ms. [1]: PBINT initiating power-up hardware flag, set when PBINT=0>1s, clear after power down. [2]: Debounced PBINT2 signal, set when PBINT2=0 >50ms, clear when PBINT2=1>50ms. [3]: PBINT2 initiating power-up hardware flag, set when PBINT2=0>1s, clear after power down. [4]: Debounced CHGR_INT signal, set when VCHG=1 >50ms, clear when VCHG=0>50ms. [5]: Charger plug-in initiating power-up hardware flag, set when VCHG=1>1s, clear after power down. [6]: RTC alarm initiating power-up hardware flag [7]: Long pressing power key reboot hardware flag, set when PBINT=0>PBINT_7S_THRESHOLD, clear after power down. [8]: PBINT initiating power-up software flag, set when PBINT=0>1s, clear by pbint_flag_clr. [9]: PBINT2 initiating power-up software flag, set when PBINT2=0>1s, clear by pbint2_flag_clr. [10]: Charger plug-in initiating power-up software flag, set when VCHG=1>1s, clear by chgr_int_flag_clr. [11: External pin reset reboot software flag, set when EXTRSTN=0>30ms, clear by ext_rstn_flag_clr. [12]: Long pressing power key reboot software flag, set when PBINT=0>PBINT_7S_THRESHOLD, clear by pbint_7s_flag. [14:13]: Reserved

13.1.1.95 POR_7S_CTRL

0x00000178	POR_7S_CTRL(0x0000036D)											POR_7S_CTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PBINT_7S_FLAG_CLR	EXT_RSTN_FLAG_CLR	CHGR_INT_FLAG_CLR	PBINT2_FLAG_CLR	PBINT_FLAG_CLR	Reserved	KEY2_7S_RST_EN	PBINT_7S_RST_SWMODE	PBINT_7S_RST_THRESHOLD				EXT_RSTN_MODE	PBINT_7S_AUTO_ON_EN	PBINT_7S_RST_DISABLE	PBINT_7S_RST_MODE
Type	RW	RW	RW	RW	RW	RO	RW	RW	RW				RW	RW	RW	RW
Reset	0	0	0	0	0	0	1	1	0	1	1	0	1	1	0	1

POR_7S_CTRL

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
PBINT_7S_FLAG_CLR	[15]	RW	NA	0	Write 1'b1 to this bit will clear pbint_7s_flag.
EXT_RSTN_FLAG_CLR	[14]	RW	NA	0	Write 1'b1 to this bit will clear ext_rstn_flag.
CHGR_INT_FLAG_CLR	[13]	RW	NA	0	Write 1'b1 to this bit will clear chgr_int_flag.
PBINT2_FLAG_CLR	[12]	RW	NA	0	Write 1'b1 to this bit will clear pbint2_flag.
PBINT_FLAG_CLR	[11]	RW	NA	0	Write 1'b1 to this bit will clear pbint_flag.
reserved	[10]	RO	NA	0	
KEY2_7S_RST_EN	[9]	RW	NA	0x1	1: One-key Reset Mode; 0: Two-key Reset Mode;
PBINT_7S_RST_SWMODE	[8]	RW	NA	0x1	0: long reset; 1: short reset;
PBINT_7S_RST_THRESHOLD	[7: 4]	RW	NA	0x6	The power key long pressing time threshold: 0~1: 2S 2: 3S 3: 4S 4: 5S 5: 6S 6: 7S 7: 8S 8: 9S 9: 10S 10:11S 11:12S 12: 13S 13:14S

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					14:15S 15:16S
EXT_RSTN_MODE	[3]	RW	NA	0x1	EXT_RSTN PIN function mode when 1key 7S reset 0: EXT_INT 1: RESET
PBINT_7S_AUTO_ON_EN	[2]	RW	NA	0x1	RTC register PBINT_7S_AUTO_ON_EN
PBINT_7S_RST_DISABLE	[1]	RW	NA	0	0: enable 7s reset function; 1: disable 7s reset function;
PBINT_7S_RST_MODE	[0]	RW	NA	0x1	0: software reset; 1: hardware reset;

13.1.1.96 HWRST_RTC

0x0000017C			HWRST_RTC(0x00000000)									HWRST_RTC				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	HWRST_RTC_REG_STS								HWRST_RTC_REG_SET							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HWRST_RTC

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
HWRST_RTC_REG_STS	[15: 8]	RO	NA	0	RTC status register, set by HWRST_RTC_SET.
HWRST_RTC_REG_SET	[7: 0]	RW	NA	0	Software set this register to test VBAT and RTC power status.

13.1.1.97 ARCH_EN

0x00000180			ARCH_EN(0x00000001)									ARCH_EN				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															AR

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

																CH_EN
Type	RO															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

ARCH_EN

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 1]	RO	NA	0	
ARCH_EN	[0]	RW	NA	0x1	PCLK_arch enable

13.1.1.98 MCU_WR_PROT_VALUE

0x00000184			MCU_WR_PROT_VALUE(0x00000000)									MCU_WR_PROT_VALUE				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	MCU_WR_PROT	MCU_WR_PROT_VALUE														
Type	RO	WO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MCU_WR_PROT_VALUE

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
MCU_WR_PROT	[15]	RO	NA	0	Arch_en write protect bit status. When mcu_wr_prot_value==16'h3c4d, the bit is "1",else "0"
MCU_WR_PROT_VALUE	[14: 0]	WO	NA	0	Arch_en write protect value

13.1.1.99 PWR_WR_PROT_VALUE

0x00000188			PWR_WR_PROT_VALUE(0x00000000)									PWR_WR_PROT_VALUE				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PWR_WR_PROT	PWR_WR_PROT_VALUE														
Type	RO	WO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PWR_WR_PROT_VALUE

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
PWR_WR_PROT	[15]	RO	NA	0	All power which default on write protect bit status. When mcu_wr_prot_value==16'h6e7f, the bit is "1",else "0"
PWR_WR_PROT_VALUE	[14: 0]	WO	NA	0	Arch_en write protect value

13.1.1.100 SMPL_CTRL0

0x0000018C		SMPL_CTRL0(0x00000000)									SMPL_CTRL0				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMPL_MODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SMPL_CTRL0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
SMPL_MODE	[15: 0]	RW	NA	0	SMPL mode: [15:13]: SMPL timer threshold 0: 0.25s

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					1: 0.5s 2: 0.75s …….. 7: 2s [12:0]: SMPL enable 13'h1935: enable Others: disable

13.1.1.101 SMPL_CTRL1

0x00000190			SMPL_CTRL1(0x00000000)									SMPL_CTRL1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SMPL_PWR_ON_FLAG	SMPL_MODE_WR_ACK_FLAG	SMPL_PWR_ON_FLAG_CLR	SMPL_MODE_WR_ACK_FLAG_CLR	SMPL_PWR_ON_SET	Reserved										SMPL_EN
Type	RO	RO	WC	WC	RO	RO										RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SMPL_CTRL1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
SMPL_PWR_ON_FLAG	[15]	RO	NA	0	Set once SMPL timer not expired.
SMPL_MODE_WR_ACK_FLAG	[14]	RO	NA	0	Set once SMPL mode write finish
SMPL_PWR_ON_FLAG_CLR	[13]	WC	NA	0	Clear SMPL_PWR_ON_FLAG
SMPL_MODE_WR_ACK_FLAG_CLR	[12]	WC	NA	0	Clear SMPL_MODE_WR_ACK
SMPL_PWR_ON_SET	[11]	RO	NA	0	Set once SMPL timer not expired,
reserved	[10: 1]	RO	NA	0	
SMPL_EN	[0]	RO	NA	0	SMPL enable indication

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

13.1.1.102 RTC_RST0

0x00000194			RTC_RST0(0x00000000)									RTC_RST0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_CLK_FLAG_SET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RTC_RST0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RTC_CLK_FLAG_SET	[15: 0]	RW	NA	0	RTC register flag

13.1.1.103 RTC_RST1

0x00000198			RTC_RST1(0x00000000)									RTC_RST1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_CLK_FLAG_CLR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RTC_RST1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RTC_CLK_FLAG_CLR	[15: 0]	RW	NA	0	RTC register flag

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

13.1.1.104 RTC_RST2

0x0000019C			RTC_RST2(0x0000A596)									RTC_RST2				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RTC_CLK_FLAG_RTC															
Type	RO															
Reset	1	0	1	0	0	1	0	1	1	0	0	1	0	1	1	0

RTC_RST2

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
RTC_CLK_FLAG_RTC	[15: 0]	RO	NA	0xa596	RTC register flag, reset by RTC_RST, default is 16'hA596

13.1.1.105 RTC_CLK_STOP

0x000001A0			RTC_CLK_STOP(0x00000010)									RTC_CLK_STOP				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved								RTC_CLK_STOP_FLAG	RTC_CLK_STOP_THRESHOLD						
Type	RO								RO	RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

RTC_CLK_STOP

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 8]	RO	NA	0	
RTC_CLK_STOP	[7]	RO	NA	0	rtc time over thresthold value

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

_FLAG					
RTC_CLK_STOP_THRESHOLD	[6: 0]	RW	NA	0x10	set reset rtc cnt time,default 16s

13.1.1.106 VBAT_DROP_CNT

0x000001A4			VBAT_DROP_CNT(0x00000000)									VBAT_DROP_CNT				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved				VBAT_DROP_CNT											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VBAT_DROP_CNT

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 12]	RO	NA	0	
VBAT_DROP_CNT	[11: 0]	RO	NA	0	VBAT Drop Time Count

13.1.1.107 SWRST_CTRL0

0x000001A8			SWRST_CTRL0(0x00000000)									SWRST_CTRL0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved					EXT_RSTN_PD_EN	PB_7S_RST_PD_EN	Reserved		WDG_RST_PD_EN	Reserved		SW_RST_PD_THRESHOLD			
Type	RO					RW	RW	RO		RW	RO		RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SWRST_CTRL0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 11]	RO	NA	0	
EXT_RSTN_PD_EN	[10]	RW	NA	0	Software reset certain power enable when ext_rstn valid
PB_7S_RST_PD_EN	[9]	RW	NA	0	Software reset certain power enable when pb_7s_rst valid
reserved	[8: 7]	RO	NA	0	
WDG_RST_PD_EN	[6]	RW	NA	0	Software reset certain power enable when wdg_rst valid
reserved	[5: 4]	RO	NA	0	
SW_RST_PD_THRESHOLD	[3: 0]	RW	NA	0	reset LDO to normal mode threshold time 8ms/step,default 8ms

13.1.1.108 SWRST_CTRL1

0x000001AC			SWRST_CTRL1(0x00000000)									SWRST_CTRL1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved												SW_RST_USB_PD_EN	SW_RST_SF_PD_EN	SW_RST_RF_PD_EN	SW_RST_VDD28_PD_EN
Type	RO												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SWRST_CTRL1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 4]	RO	NA	0	
SW_RST_USB_PD_EN	[3]	RW	NA	0	Software reset LDO_USB_PD enable when global reset valid
SW_RST_SF_PD_EN	[2]	RW	NA	0	Software reset LDO_SF_PD enable when global reset valid
SW_RST_RF_PD_EN	[1]	RW	NA	0	Software reset LDO_RF_PD enable when global reset valid

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

SW_RST_VDD28_PD_EN	[0]	RW	NA	0	Software reset LDO_VDD28_PD enable when global reset valid

13.1.1.109 OTP_CTRL

0x000001B0	OTP_CTRL(0x00000006)											OTP_CTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved									OTPINT_OUT	Reserved			OTP_OP		OTP_EN
Type	RO									RO	RO			RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

OTP_CTRL

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 7]	RO	NA	0	
OTPINT_OUT	[6]	RO	NA	0	OTP int flag
reserved	[5: 3]	RO	NA	0	
OTP_OP	[2: 1]	RW	NA	0x3	OTP threshold option, 00 120, 01 130, 10 140, 11 150;
OTP_EN	[0]	RW	NA	0	OTP function enable control bit

13.1.1.110 RESERVED_REG35

0x000001B4	RESERVED_REG35(0x00000000)											RESERVED_REG35				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG35

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.111 RESERVED_REG36

0x000001B8			RESERVED_REG36(0x00000000)									RESERVED_REG36				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_REG36

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 0]	RO	NA	0	

13.1.1.112 LOW_PWR_CLK32K_CTRL

0x000001BC			LOW_PWR_CLK32K_CTRL(0x00000B0C)									LOW_PWR_CLK32K_CTRL				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	dcxo_extra_low_cur_mode_en	dcxo_low_cur_mode_en	ldo_dcxo_lp_auto_en	time_between_calibration				time_for_calibration			time_for_dcxo_stable				Reserved	low_pwr_clk32k_en
Type	RW	RW	RW	RW				RW			RW				RO	RW
Reset	0	0	0	0	1	0	1	1	0	0	0	0	1	1	0	0

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

LOW_PWR_CLK32K_CTRL

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
dcxo_extra_low_cur_mode_en	[15]	RW	NA	0	extra low current mode DCXO for auto calibration 0: disable 1: enable
dcxo_low_cur_mode_en	[14]	RW	NA	0	Low current mode DCXO enable for auto calibration 0: use normal mode DCXO for calibration 1:use low current mode DCXO for calibration
ldo_dcxo_lp_auto_en	[13]	RW	NA	0	LDO DCXO low power enable for auto calibration 0: normal mode when auto calibration 1: low power mode when auto calibration
time_between_calibration	[12: 9]	RW	NA	0x5	0000: 20S 0001: 21S 0010: 22S 0011: 23S 0100: 24S 0101: 25S 0110: 26S 0111: 27S 1000: 28S 1001: 29S 1010: 210S 1011: 211S 1100: 212S 1101: 213S 1110: 214S 1111: 215S
time_for_calibration	[8: 6]	RW	NA	0x4	000: 30ms 001: 60ms 010: 120ms 011: 240ms 100: 480ms 101: 960ms 110: 2s 111: 4s
time_for_dcxo_stable	[5: 2]	RW	NA	0x3	0000: 2ms 0001: 4ms 0010: 6ms 0011: 8ms

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

					0100: 10ms 0101: 12ms 0110: 14ms 0111: 16ms 1000: 18ms 1001: 20ms 1010: 22ms 1011: 24ms 1100: 26ms 1101: 28ms 1110: 30ms 1111: 32ms
reserved	[1]	RO	NA	0	
low_pwr_clk32k_en	[0]	RW	NA	0	Enable low power of clock 32k 0: disable 1: enable

13.1.1.113 LOW_PWR_CLK32K_TEST0

0x000001C0	LOW_PWR_CLK32K_TEST0(0x00000000)											LOW_PWR_CLK32K_TEST0				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	cal_result_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOW_PWR_CLK32K_TEST0

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
cal_result_1	[15: 0]	RO	NA	0	register for test

13.1.1.114 LOW_PWR_CLK32K_TEST1

0x000001C4	LOW_PWR_CLK32K_TEST1(0x00000000)											LOW_PWR_CLK32K_TEST1				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	cal_result_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOW_PWR_CLK32K_TEST1

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
cal_result_0	[15: 0]	RO	NA	0	register for test

13.1.1.115 LOW_PWR_CLK32K_TEST2

0x000001C8			LOW_PWR_CLK32K_TEST2(0x00000000)									LOW_PWR_CLK32K_TEST2				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	div_fac_frac															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOW_PWR_CLK32K_TEST2

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
div_fac_frac	[15: 0]	RO	NA	0	register for test

13.1.1.116 LOW_PWR_CLK32K_TEST3

0x000001CC			LOW_PWR_CLK32K_TEST3(0x00000000)									LOW_PWR_CLK32K_TEST3				
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Reserved										swit	low	div_fac_int			

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

											ch_for_clk	_pwr_clk32k_en_dbg				
Type	RO										RW	RW	RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOW_PWR_CLK32K_TEST3

Field Name	Bit	Type	Set/Clear	Reset Value	Description
reserved	[31: 16]	RO	NA	0	
reserved	[15: 6]	RO	NA	0	
switch_for_clk	[5]	RW	NA	0	clock switch for test
low_pwr_clk32k_en_dbg	[4]	RW	NA	0	Enable low power of clock 32k for test 0: disable 1: enable
div_fac_int	[3: 0]	RO	NA	0	register for test

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.