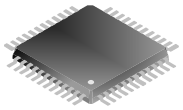
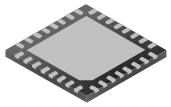
# ENHANCED 8051 MCU INTEGRATED WITH ADC AND PWM

## DESCRIPTION

The SC52F5716/32 MCU is designed intended for motor control and digital control power supply applications. It uses single-cycle SC52 core with built-in 16/32K-byte Flash, 256-byte IRAM, and 1K-byte XDRAM. It is integrated with a 16MHz high-accuracy RC oscillator, multi general purpose timers, and common communication interfaces (such as SPI/UART). It is comprised of three-phase 6-channel complementary PWM generators, A/D converter (up to 1Msps sampling rate), and 5 analog comparators, which realizes maximum flexibility and lowest system cost during design of motor control and digital control power supply applications.



LQFP-48-7×7-0.5



QFN-32-5 x 5 x 0.75-0.5

SSOP-24-225-0.635

## APPLICATION

- Motor control
- Digital control power supply

## FEATURES

- 8-bit single-cycle SC52 CPU
  - 24MHz maximum operating frequency
  - Fully compatible with MCS51 instruction set
  - Dual DPTR
  - The execution time of 80% instructions is one to two clock cycles
- On-chip memory
  - 16/32K-byte FLASH
    - Page size: 128 byte
    - Data retention:> 100 years
    - Erasing endurance: > 100,000 times
  - 256-byte IRAM
  - 1K-byte XDRAM
- Power supply and reset
  - Built-in 1.8V LDO, powered by external power supply
  - Built-In Power-On-Reset (POR)
  - Built-In Low-Voltage-Reset (LVR) with 4 reset points optional
  - Built-In Low-Voltage-Detect (LVD) with 8 levels selectable
  - Built-in watchdog (WDT)
  - Core voltage monitoring reset
  - Supports stack overflow reset
- Clock system
  - Built-In 16MHz high accuracy Oscillator (RCH) with 1% frequency variation at room temperature
  - Built-In 32KHz low frequency Oscillator (RCL), no factory calibration.

- External multimode oscillator (OSCH)
- Built-in PLL, clock comes from RCH or OSCH, multiplication factor: 1~32
- System clock prescaler with factors of 1/2/4/8
- Supports external oscillator stop detection

◆ Debugging and download

- Double-wire debugging, debugging and programming shared
- Support In-System-Programming (ISP), only 5-pins are needed (including VDD/VSS)
- Supports In-Application-Programming (IAP)
- Supports program segment encryption (for users' intellectual property protection)

◆ Supports 21 interrupts maximum

- Four external interrupts INT0, INT1, INT2, and INT3, interrupt polarity settable
- T0/T1/T2 timer overflow interrupt, T2 capture interrupt
- CMP0/CMP1/CMP2 comparator interrupt
- Clock switching error interrupt
- LVD interrupt
- ADC conversion end interrupt, ADC conversion value match interrupt
- SPI interrupt
- PWM interrupt
- WDT interrupt
- UART interrupt
- PWM fault interrupt

◆ Input/output

- Supports up to 30 I/O ports
- Two levels optional for P1 source and sink current
- 4-channel external interrupt input, interrupt polarity settable

◆ Peripherals

- 12-bit 15-channel ADC, maximum conversion rate 1Msps, operating voltage 2.7~5.5V
- 3 analog comparators (ACMP0, ACMP1, ACMP2)
- 1 watchdog timer (WDT)
- 16-bit standard timers T0 and T1
- 1 enhanced timer T2
- 1 SPI interface
- 1 UART interface
- 7-channel 8+4 precision adjustable PWM controllers, maximum operating frequency 64MHz
- 1 multiplication and division arithmetic unit (MDU)

◆ Operating mode

- Normal operating mode
- IDLE mode
- STOP mode(only for QFN-32 package)

◆ Package type

- LQFP-48-7x7-0.5

- SSOP-24-225-0.635
- QFN-32-5x5-0.5

## ORDERING INFORMATION

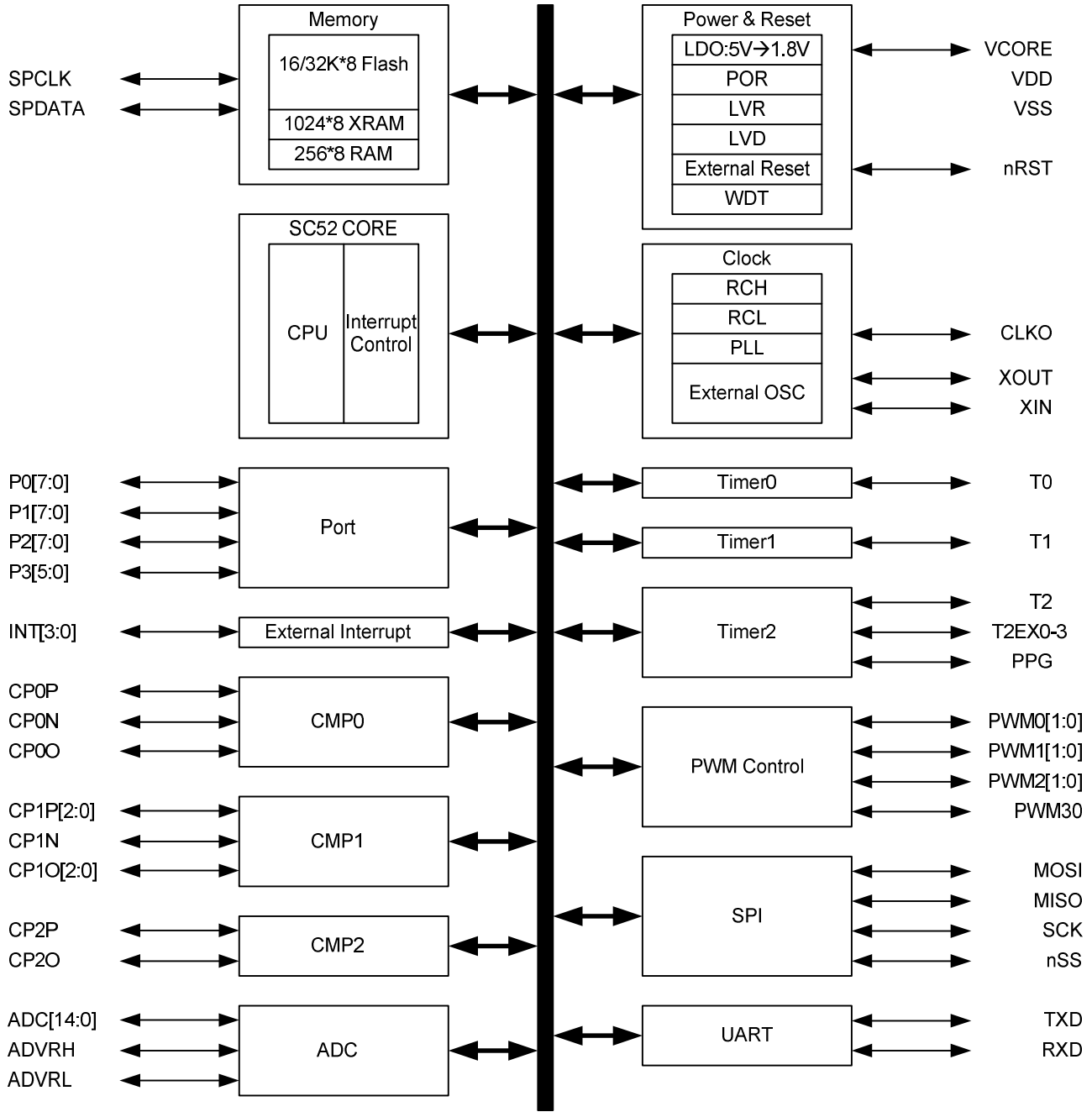
### ORDERING INFORMATION

| Part No. | Package | Marking | Hazardous Substance Control | Packing |
|---|---|---|---|---|
| SC52F5716LL1G | LQFP-48-7×7-0.5 | 5716LL1G | Halogen free | Tray |
| SC52F5716RE1G | SSOP-24-225-0.635 | 5716RE1G | Halogen free | Tube |
| SC52F5716RE1GTR | SSOP-24-225-0.635 | 5716RE1G | Halogen free | Tape&Reel |
| SC52F5732LL1G | LQFP-48-7×7-0.5 | 5732LL1G | Halogen free | Tray |
| SC52F5732RE1G | SSOP-24-225-0.635 | 5732RE1G | Halogen free | Tube |
| SC52F5732RE1GTR | SSOP-24-225-0.635 | 5732RE1G | Halogen free | Tape&Reel |
| SC52F5716RE2G | SSOP-24-225-0.635 | 5716RE2G | Halogen free | Tube |
| SC52F5716RE2GTR | SSOP-24-225-0.635 | 5716RE2G | Halogen free | Tape&Reel |
| SC52F5732NF1G | QFN-32-5×5-0.5 | 5732NF1G | Halogen free | Tray |

### RESOURCE INFORMATION

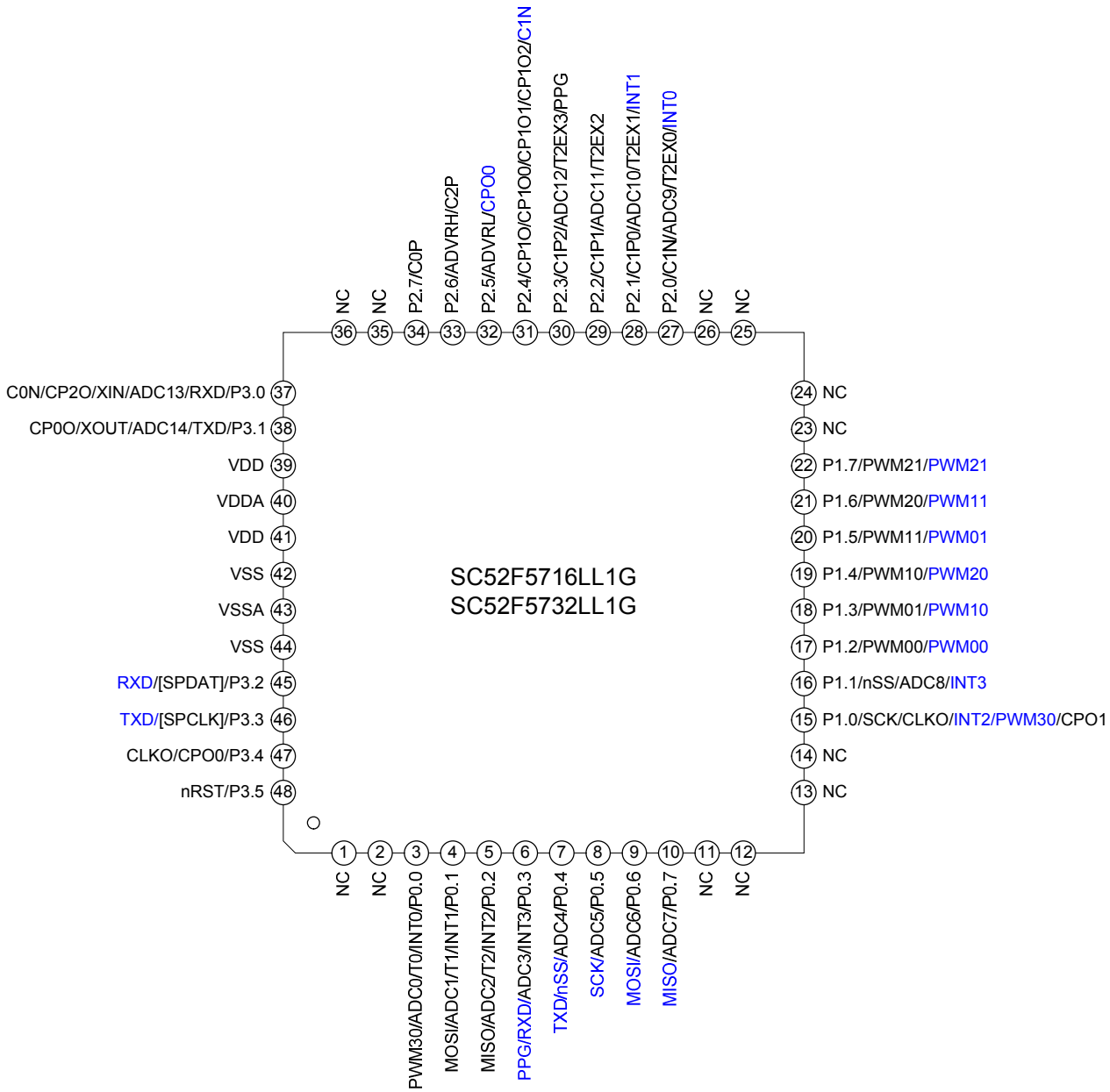
| Features | -LL1 | -NF1 | -RE1 | -RE2 |
|---|---|---|---|---|
| FLASH | 16/32K Byte | | | |
| RAM | 1K Byte XRAM + 256 Byte IRAM | | | |
| I/O | 30 | 29 | 22 | 22 |
| EXTERNAL INTERRUPT | 4 | 4 | 4 | 4 |
| T0 | Yes | Yes | Yes | Yes,, T0 input is inavailable |
| T1 | Yes | Yes | Yes | Yes |
| T2 | Yes | Yes | Yes | Yes |
| PWM | 7 | 7 | 7 | 7 |
| UART | Yes | Yes | Yes | Yes |
| SPI | Yes | Yes | Yes | Yes |
| ACMP | Yes | Yes | Yes, C0P is inavailable | Yes |
| ADC | 15-channel input | 14-channel input | 10-channel input | 9-channel input |

## BLOCK DIAGRAM



## PIN CONFIGURATION

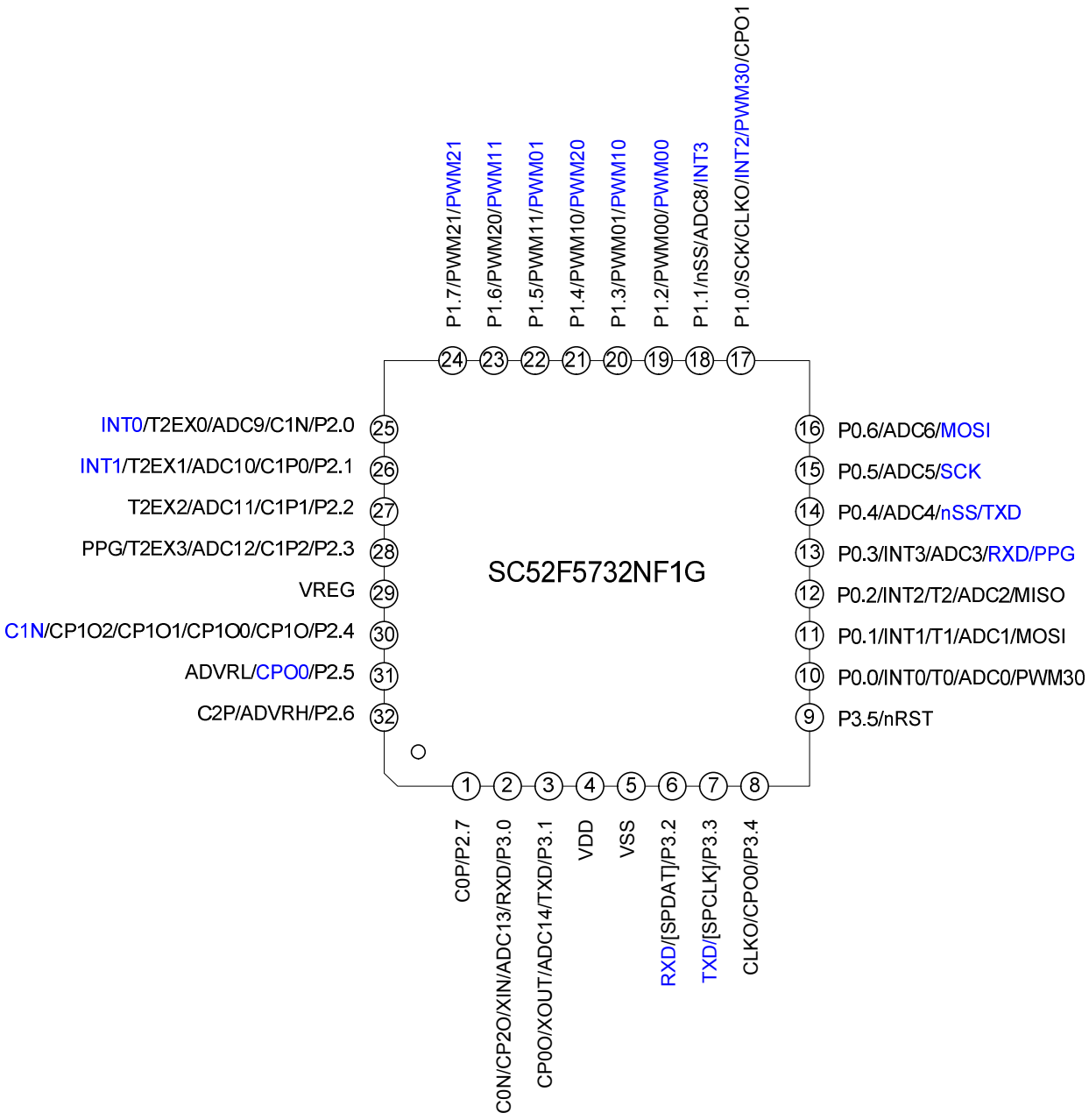
LQFP-48：SC52F5716/32LL1G




**Note 1:** The pin with the name in blue font means it can be realized by remapping through software.

**Note 2:** The pin with the name in [ ] means it is used for programming.

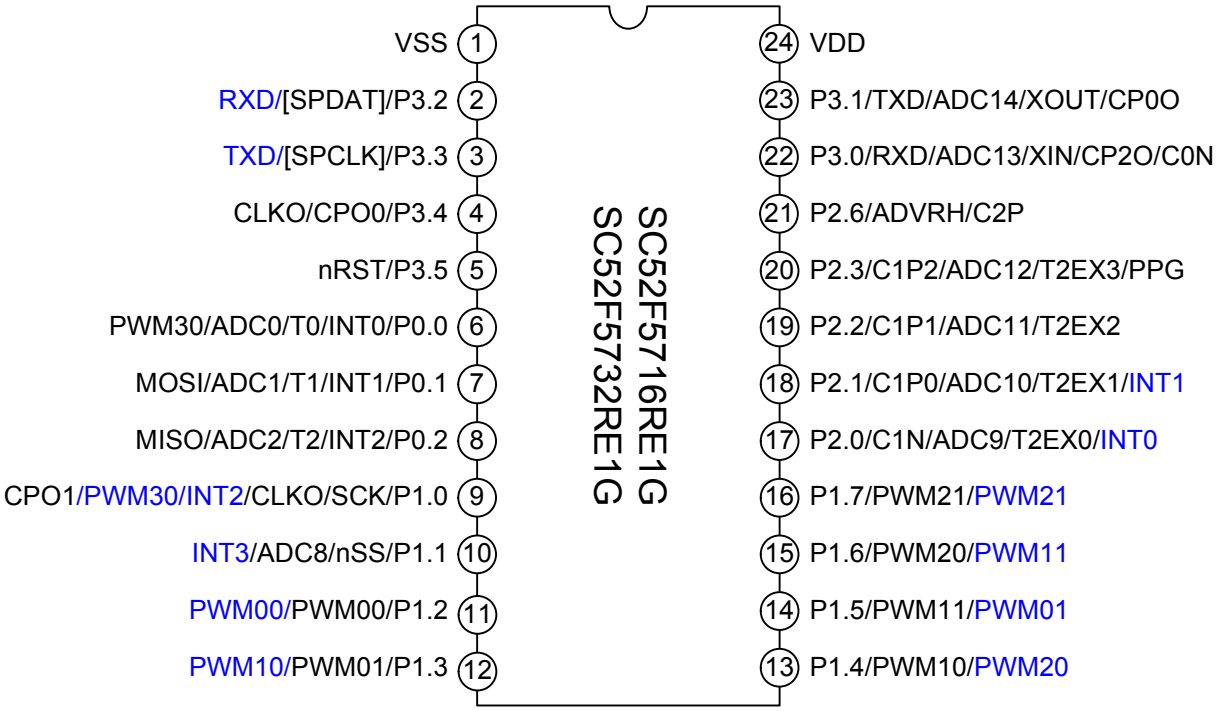
QFN-32：SC52F5732NF1G




**Note 1:** The pin with the name in blue font means it can be realized by remapping through software.

**Note 2:** The pin with the name in [ ] means it is used for programming.

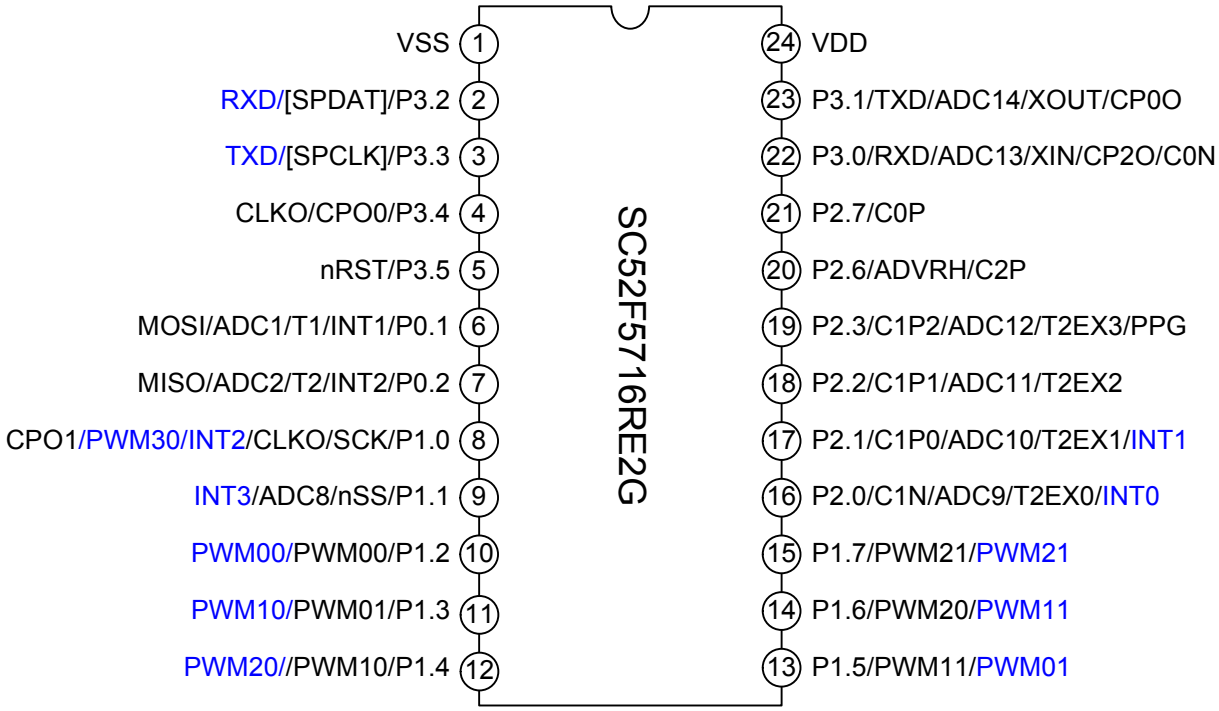
SSOP-24：SC52F5716/32RE1G




**Note 1:** The pin with the name in blue font means it can be realized by remapping through software.

**Note 2:** The pin with the name in [ ] means it is used for programming.

SSOP-24：SC52F5716RE2G




**Note 1:** The pin with the name in blue font means it can be realized by remapping through software.

**Note 2:** The pin with the name in [ ] means it is used for programming

## PIN DESCRIPTION

### PIN MULTIPLEX

| I/O | Pin Number | | | | System | External Interrupt | Timer & PWM | ADC | Serial Port | Comparator |
|---|---|---|---|---|---|---|---|---|---|---|
| | -LL1 | -NF1 | -RE1 | -RE2 | | | | | | |
| P0.0 | 3 | 10 | 6 | -- | -- | INT0 | T0/ PWM30 | ADC0 | -- | -- |
| P0.1 | 4 | 11 | 7 | 6 | -- | INT1 | T1 | ADC1 | MOSI | -- |
| P0.2 | 5 | 12 | 8 | 7 | -- | INT2 | T2 | ADC2 | MISO | -- |
| P0.3 | 6 | 13 | -- | -- | -- | INT3 | PPG | ADC3 | RXD | -- |
| P0.4 | 7 | 14 | -- | -- | -- | -- | -- | ADC4 | TXD/ nSS | -- |
| P0.5 | 8 | 15 | -- | -- | -- | -- | -- | ADC5 | SCK | -- |
| P0.6 | 9 | 16 | -- | -- | -- | -- | -- | ADC6 | MOSI | -- |
| P0.7 | 10 | -- | -- | -- | -- | -- | -- | ADC7 | MISO | -- |
| P1.0 | 15 | 17 | 9 | 8 | CLKO | INT2 | PWM30 | -- | SCK | CPO1 |
| P1.1 | 16 | 18 | 10 | 9 | -- | INT3 | -- | ADC8 | nSS | -- |
| P1.2 | 17 | 19 | 11 | 10 | -- | -- | PWM00 | -- | -- | -- |
| P1.3 | 18 | 20 | 12 | 11 | -- | -- | PWM01/ PWM10 | -- | -- | -- |
| P1.4 | 19 | 21 | 13 | 12 | -- | -- | PWM10/ PWM20 | -- | -- | -- |
| P1.5 | 20 | 22 | 14 | 13 | -- | -- | PWM11/ PWM01 | -- | -- | -- |
| P1.6 | 21 | 23 | 15 | 14 | -- | -- | PWM20/ PWM11 | -- | -- | -- |
| P1.7 | 22 | 24 | 16 | 15 | -- | -- | PWM21 | -- | -- | -- |
| P2.0 | 27 | 25 | 17 | 16 | -- | INT0 | T2EX0 | ADC9 | -- | C1N |
| P2.1 | 28 | 26 | 18 | 17 | -- | INT1 | T2EX1 | ADC10 | -- | C1P0 |
| P2.2 | 29 | 27 | 19 | 18 | CLKO | -- | T2EX2 | ADC11 | -- | C1P1 |
| P2.3 | 30 | 28 | 20 | 19 | -- | -- | T2EX3/ PPG | ADC12 | -- | C1P2 |
| P2.4 | 31 | 30 | -- | -- | -- | -- | -- | -- | -- | CP1O/C1N |
| P2.5 | 32 | 31 | -- | -- | -- | -- | -- | ADVRL | -- | CPO0 |
| P2.6 | 33 | 32 | 21 | 20 | -- | INT2 | -- | ADVRH | -- | C2P |
| P2.7 | 34 | 1 | -- | 21 | -- | INT3 | -- | -- | -- | C0P |
| P3.0 | 37 | 2 | 22 | 22 | XIN | -- | -- | ADC13 | RXD | CP2O/C0N |
| P3.1 | 38 | 3 | 23 | 23 | XOUT | -- | -- | ADC134 | --TXD | CP0O |
| P3.2 | 45 | 6 | 2 | 2 | SPDAT | -- | -- | -- | RXD | -- |
| P3.3 | 46 | 7 | 3 | 3 | SPCLK | -- | -- | -- | TXD | -- |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| P3.4 | 47 | 8 | 4 | 4 | CLKO | -- | -- | -- | -- | CPO0 |
| P3.5 | 25 | 9 | 5 | 5 | nRST | -- | -- | -- | -- | -- |
| VDD | 39 | 4 | 24 | 24 | -- | -- | -- | -- | -- | -- |
| VDDA | 40 | | | | -- | -- | -- | -- | -- | -- |
| VDD | 41 | | | | -- | -- | -- | -- | -- | -- |
| VSS | 42 | 5 | 1 | 1 | -- | -- | -- | -- | -- | -- |
| VSSA | 43 | | | | -- | -- | -- | -- | -- | -- |
| VSS | 44 | | | | -- | -- | -- | -- | -- | -- |
| VREG | -- | 29 | -- | -- | -- | -- | -- | -- | -- | -- |

**PIN DESCRIPTION**

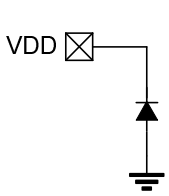
| I/O | PIN TYPE | Function Description |
|---|---|---|
| **Port** | | |
| P0.0-P0.7 | I/O | 8-bit bidirectional I/O ports, bit operation available |
| P1.0-P1.7 | I/O | 8-bit bidirectional I/O ports, bit operation available |
| P2.0-P2.7 | I/O | 8-bit bidirectional I/O ports, bit operation available |
| P3.0-P3.5 | I/O | 6-bit bidirectional I/O ports, bit operation available |
| **Program** | | |
| [SPCLK] | I | Programming clock Input |
| [SPDATA] | I/O | Programming data Input/output |
| **System** | | |
| nRST | I | External reset input, low voltage active |
| CLKO | O | Clock output |
| XIN | I | External oscillator input |
| XOUT | O | External oscillator output |
| **Timer** | | |
| T0 | I | T0 external counting clock input |
| T1 | I | T1 external counting clock input |
| T2 | I | T2 external counting clock input |
| T2EX0 | I | T2 external counting input 0 |
| T2EX1 | I | T2 external counting input 1 |
| T2EX2 | I | T2 external counting input 2 |
| T2EX3 | I | T2 external counting input 3 |
| PPG | O | T2 wave output |
| **PWM** | | |
| PWM00 | O | PWM output |
| PWM01 | O | |
| PWM10 | O | |
| PWM11 | O | |
| PWM20 | O | |
| PWM21 | O | |

| I/O | PIN TYPE | Function Description |
|---|---|---|
| PWM30 | O | |
| **Serial port** | | |
| NSS | I/O | SPI enable pin |
| MISO | I/O | SPI master input/slave output |
| MOSI | I/O | SPI master output/slave input |
| SCK | I/O | SPI clock pin |
| TXD | O | UART0 data output |
| RXD | I | UART0 data input |
| **Analog comparator** | | |
| C0N | I | CMP0 positive input |
| C0P | I | CMP0 negative input |
| C1P0 | I | CMP1 positive input 0 |
| C1P1 | I | CMP1 positive input 1 |
| C1P2 | I | CMP1 positive input 2 |
| C1N | I | CMP1 negative input |
| C2P | I | CMP2 positive input |
| CP0O | O | CMP0 output |
| CP1O | O | CMP1 output |
| CP1O0 | O | CMP1 output 0 |
| CP1O1 | O | CMP1 output 1 |
| CP1O2 | O | CMP1 output 2 |
| CP2O | O | CMP2 output |
| CPO0 | O | CMP output 0 |
| CPO1 | O | CMP output 1 |
| **ADC** | | |
| ADC0~ADC14 | I | 15-channel ADC input |
| ADVRH | I | ADC external reference voltage High |
| ADVRL | I | ADC external reference voltage Low |
| **Power** | | |
| $V_{DD}$ | P | Power |
| $V_{DDA}$ | P | |
| $V_{SSA}$ | G | Ground |
| $V_{SS}$ | G | |
| VREG | P | Core voltage, connecting $V_{SS}$ through 0.1uF capacitor |

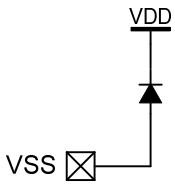
**Note:**

1. In Pin Type column: “P” denotes Power pins, “I/O” denotes normal input/output pins, “I” denotes input pins, “O” denotes output pins; “A” denotes analog pin
2. P35 is external reset pin (actives low) by default, if users want to configure this pin as common I/O, they should set 0x007BH unit of FLASH to 0x3CH.

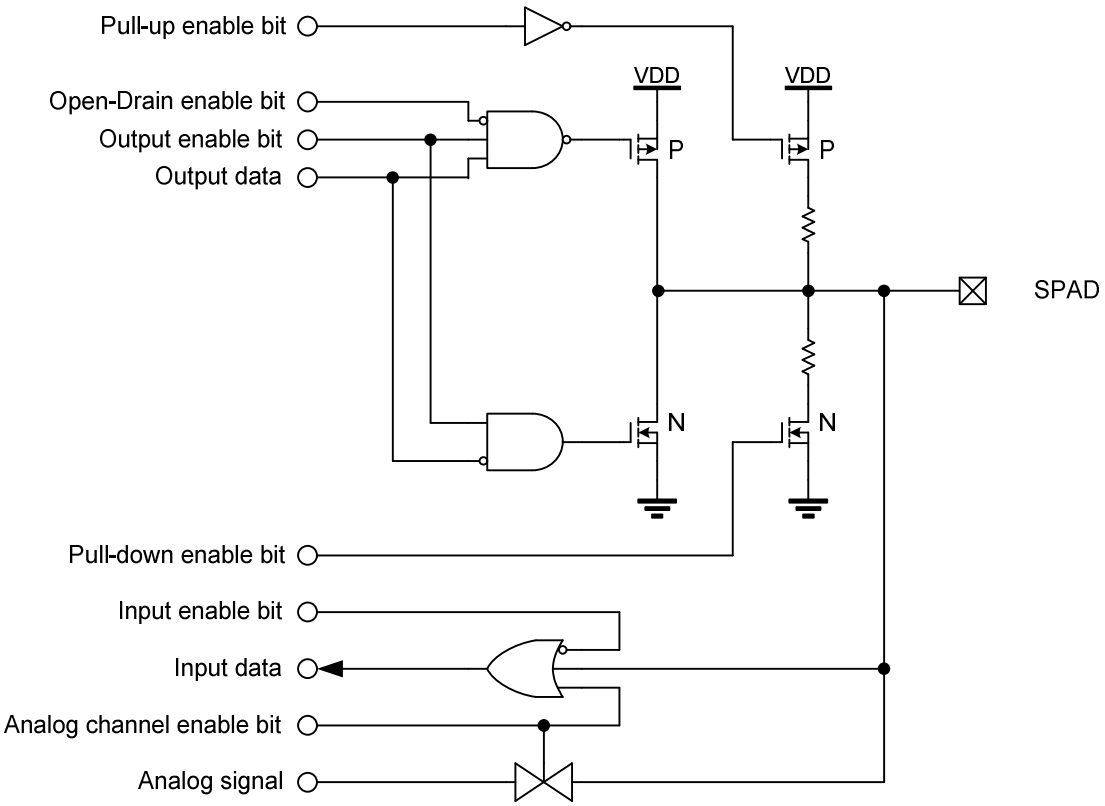
## PIN STRUCTURE




VDD structure




VSS structure




**Note:** the internal logic control makes sure that the pull-up/down resistor will not be enabled at the same time.

## ABSOLUTE MAXIMUM RATINGS

| Characteristics | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.3 ~ 6.0 | V |
| Input Voltage | $V_I$ | -0.3 ~ $V_{DD}$+0.3 | V |
| Storage Temperature Range | $T_{STG}$ | -55 ~ 125 | °C |
| Operating Temperature Range | $T_{OPR}$ | -40 ~ 85 | °C |

## DC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $V_{DD}$=5V, $T_{AMB}$=25°C)

### 1. Power supply characteristics

Table 1: Power supply characteristics

| Characteristics | Symbol | Test condition | | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| Operating voltage | $V_{DD}$ | Normal operation | | | 2.4 | - | 5.5 | V |
| Operating current, considering the temperature | $I_{DD}$ | RCH provides the system clock | MClk=16MHz | $V_{DD}$=5.0 | - | 5 | - | mA |
| | | CRYH provides the system clock, min. gain | MClk=4MHz | $V_{DD}$=5.0 | - | 1.5 | - | |
| | | | MClk=8MHz | $V_{DD}$=5.0 | - | 3 | - | |
| | | PLL provides the system clock | MClk=24MHz | $V_{DD}$=5.0 | - | 7 | - | |
| | | RCL provides the system clock | MClk=$F_{RCL}$ | $V_{DD}$=5.0 | - | 300 | - | μA |
| | Note: when one clock is working, others are off, except PLL, because it depends on RCH or CRYH input. | | | | | | | |
| Idle current | $I_{IDLE}$ | RCH provides the system clock | MClk=16MHz | $V_{DD}$=5.0 | - | 3 | - | mA |
| | | CRYH provides the system clock, min. gain | MClk=4MHz | $V_{DD}$=5.0 | - | 1 | - | |
| | | PLL provides the system clock | MClk=24MHz | $V_{DD}$=5.0 | - | 5 | - | |
| | | RCL provides the system clock | MClk=$F_{RCL}$ | $V_{DD}$=5.0 | - | 250 | - | μA |
| Stop current | $I_{STOP}$ | LVR off | $V_{DD}$=5.0 | | - | 14 | 16 | μA |
| | | Note: Bandgap voltage reference is auto on when LVR is turned on. | | | | | | |

**Note:** The typ. values are based on characterization results, not tested in production.

### 2. IO characteristics

Table 2: IO characteristics

| Characteristics | Symbol | Test condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| High input voltage | $V_{IH}$ | P3.5 | | 0.8$V_{DD}$ | - | $V_{DD}$ | V |
| | | IO except P3.5 | | 0.7$V_{DD}$ | - | $V_{DD}$ | |
| Low input voltage | $V_{IL}$ | P3.5 | | 0 | - | 0.2$V_{DD}$ | V |
| | | IO except P3.5 | | 0 | - | 0.3$V_{DD}$ | |
| Driving when $V_{DD}$=5.0V | | | | | | | |
| Output pin source current | $I_{OH}$ | $V_{OH}$=0.9$V_{DD}$ | IO except P1 | - | 4 | - | mA |
| | | | P1 (low level) | - | 4 | - | |
| | | | P1 (high level) | - | 16 | - | |

| Characteristics | Symbol | Test condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Output pin sink current | $I_{OL}$ | $V_{OL}$=0.1$V_{DD}$ | IO except P1 | - | 8 | - | mA |
| | | | P1 (low level) | - | 8 | - | |
| | | | P1 (high level) | - | 16 | - | |
| Internal pull-up resistor | Rpu | $V_{IN}$=0V | All IOs | - | 50 | - | KΩ |
| Internal pull-down resistor | Rdn | $V_{IN}$=5V | All IOs | - | 50 | - | KΩ |
| Leakage current (high temperature) | $I_{IL}$ | $V_{IN}$=$V_{SS}$ or $V_{DD}$ | All IOs | - | - | ±1 | uA |

**Note:** The typ. values are based on characterization results, not tested in production.

## 3. System monitoring and reset characteristics

Table 3: System monitoring and reset

| Characteristics | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Typical condition: $V_{DD}$=5.0V, temperature=25°C, temperature range: -40～85°C<br>The max. and min. values are tested in full temperature/voltage range. | | | | | | |
| Band gap voltage | $V_{BG}$ | | - | 1.2 | - | V |
| LDO output voltage | $V_{MVR}$ | | - | 1.8 | - | V |
| Low reset voltage | $V_{LVR}$ | $L_{VRS}$=00 | 1.85 | 1.95 | 2.05 | V |
| | | $L_{VRS}$=01 | 2.40 | 2.50 | 2.60 | |
| | | $L_{VRS}$=10 | 2.85 | 3.00 | 3.15 | |
| | | $L_{VRS}$=11 | 3.80 | 4.00 | 4.20 | |
| Low reset release voltage | $V_{LVRR}$ | $L_{VRS}$=00 | 2.05 | 2.25 | 2.40 | V |
| | | $L_{VRS}$=01 | 2.65 | 2.85 | 3.00 | |
| | | $L_{VRS}$=10 | 3.20 | 3.40 | 3.60 | |
| | | $L_{VRS}$=11 | 4.25 | 4.55 | 4.80 | |
| LVD voltage | $V_{LVD}$ | $L_{VDS}$ = 000 | - | 2.2 | - | V |
| | | $L_{VDS}$ = 001 | - | 2.4 | - | |
| | | $L_{VDS}$ = 010 | - | 2.7 | - | |
| | | $L_{VDS}$ = 011 | - | 3.0 | - | |
| | | $L_{VDS}$ = 100 | - | 3.5 | - | |
| | | $L_{VDS}$ = 101 | - | 3.7 | - | |
| | | $L_{VDS}$ = 110 | - | 3.9 | - | |
| | | $L_{VDS}$ = 111 | - | 4.3 | - | |
| LVD release hysteresis voltage | $V_{HYS(LVD)}$ | $V_{DD}$≥3.0 | - | 100 | - | mV |
| | | $V_{DD}$<3.0 | - | 60 | - | |

**Note:** The typ. values are based on characterization results, not tested in production.

## 4. Oscillation and clock characteristics

Table 4: Oscillation and clock characteristics

| Characteristics | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Calibrated oscillation frequency of internal RCH | $F_{RCH}$ | 5.0V，25°C | 15.84 | 16 | 16.16 | MHz |
| | | 5.0V，-40～85°C | 15.52 | 16 | 16.48 | |
| | | 2.4~5.5V，-40～85°C | 15.20 | 16 | 16.80 | |
| Oscillation frequency of internal RCL | $F_{RCL}$ | 2.4~5.5V -40～85°C | - | 32 | - | KHz |
| Test condition for oscillation start time: VDD=1.8～5.5V; -40～85°C | | | | | | |
| CRYH start time | $T_{CRHHST}$ | 8MHz, 20pF load connected to GND | - | 5 | 50 | mS |
| HF oscillation stabilization delay counted period | $T_{DCRYH}$ | Settable through software | $2^{12}$ | - | $2^{15}$ | Cycles |
| PLL reference clock frequency range | $F_{PLLREF}$ | 2.4～5.5V | 1 | - | 4 | MHz |
| PLL output frequency range | $F_{PLL}$ | | 1 | - | 64 | MHz |

**Note:** The typ. values are based on characterization results, not tested in production.

## 5. RAM min. retention voltage

Table 5: RAM data retention voltage

| Characteristics | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| RAM retention voltage | $V_{DR}$ | −40°C < TA < +85°C | 1.5 | - | - | V |

## 6. Analog comparator characteristics

Table 6: Analog comparator characteristics

| Characteristics | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input offset voltage | Vos | | -10 | 0 | 10 | mV |
| Input voltage common mode voltage | Vcm | | 0 | - | $V_{DD}$ | V |
| Common mode rejection ratio | CMRR | | - | 1.5 | - | mV/V |
| Input voltage hysteresis | Vhyster | | - | 10 | - | mV |
| Start-up time | Tstr | | - | 1 | 2 | μs |
| Response time | Trt | CMP0/2, overdrive voltage±30mV | - | 20 | 200 | ns |
| | | CMP1, overdrive voltage ±30mV | - | 150 | 1000 | ns |
| Operating current | Icmp | CMP0/2 | - | 500 | - | μA |
| | Icmp1 | CMP1 | - | 20 | - | μA |
| Built-in comparing reference stabilization time | Tscvr | | - | 1 | 3 | μs |

**Note:** The typ. values are based on characterization results, not tested in production. The CMP1 operating current is the typical value during single-channel operation.

## 7. Analog/digital converter characteristics

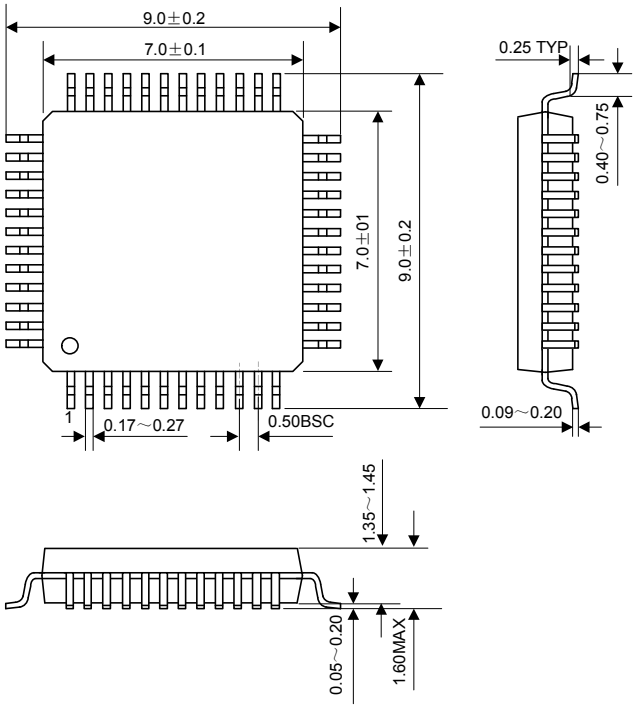
Table 7: ADC characteristics

| Characteristics | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Typical condition: $V_{DD}$=5.0V, temperature=25°C. ADC high reference= $V_{DD}$. | | | | | | |
| ADC operating voltage range | $V_{DDAD}$ | | 2.7 | 5 | 5.5 | V |
| Input analog voltage range | $V_{ADIN}$ | | 0 | - | $V_{DDAD}$ | V |
| Sample & hold capacitor | $C_{ADIN}$ | | - | 12 | - | pF |
| Analog channel impedance | $R_{ADIN}$ | | - | - | 1 | kΩ |
| Input source impedance | $R_{AS}$ | Fadclk=16MHz | - | - | 1 | kΩ |
| ADC clock frequency | Fadclk | Connected to a 0.1uF regulator capacitor externally | - | - | 16 | MHz |
| ADC clock period | $T_{AD}$ | | | 1/Fadclk | | ns |
| Conversion time | Tconv | | - | 17 | - | TAD |
| | | | | | | |
| Differential nonlinearity | DNL | | -4 | - | +4 | LSB |
| Integral nonlinearity | INL | | -4 | - | +4 | LSB |
| Offset error | Ezs | | -6 | - | +2 | LSB |
| Gain error | Efs | | -6 | - | +4 | LSB |
| Global uncorrected error | $E_{TUE}$ | | -8 | - | +2 | LSB |
| No missing code | NMC | | | 10 | | Bit |
| Resolution | NR | | | 12 | | Bit |

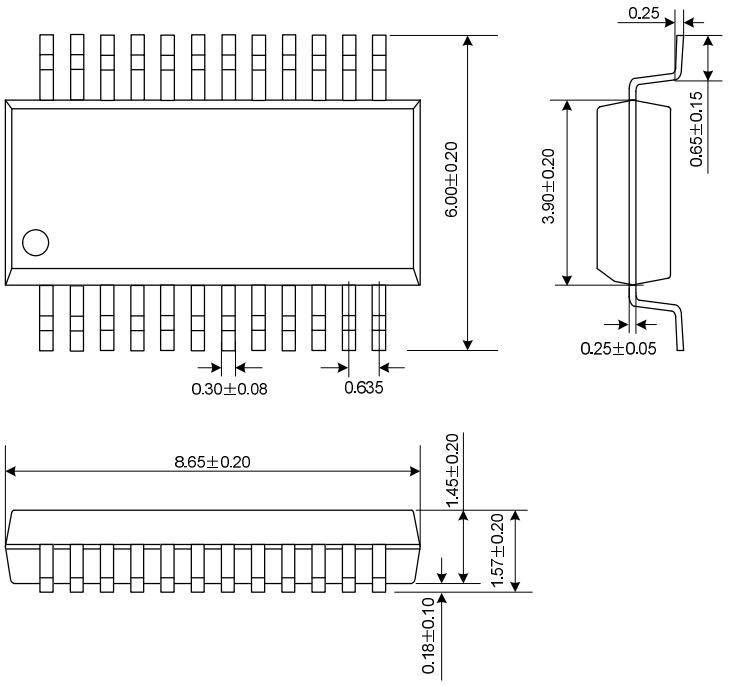
**Note:** The typ. values are based on characterization results, not tested in production.

## PACKAGE OUTLINE

**LQFP-48-7x7-0.5** — **UNIT: mm**

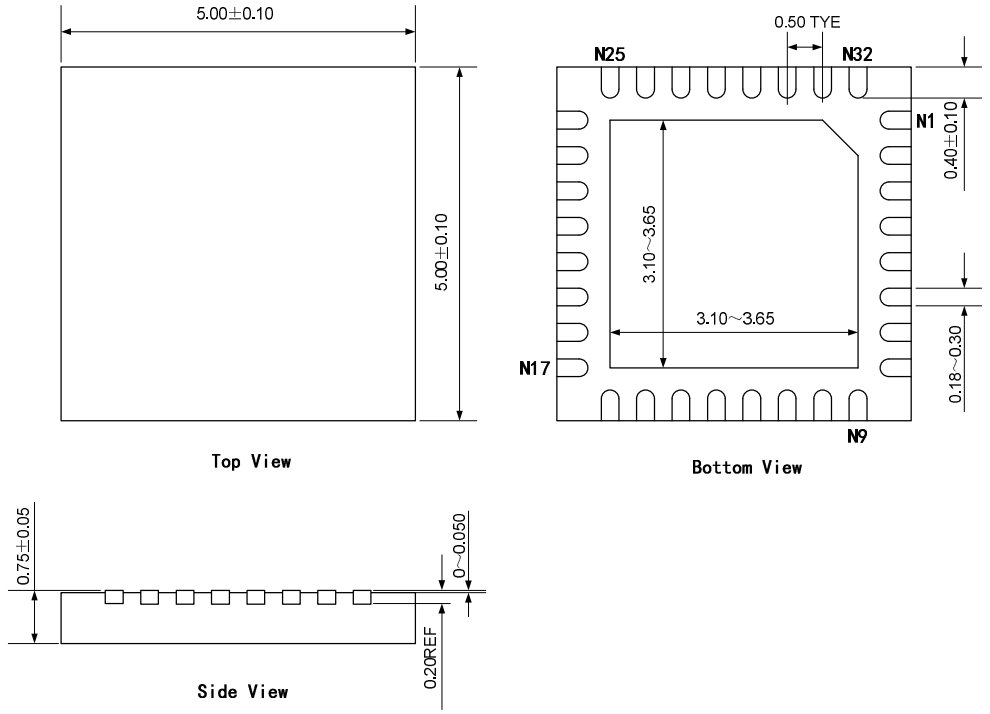



**SSOP-24-225-0.635** — **UNIT: mm**



## PACKAGE OUTLINE(continued)

| QFN-32-5x5-0.5 | UNIT: mm |
|---|---|





**MOS DEVICES OPERATE NOTES:**

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

**Disclaimer :**

- **Silan reserves the right to make changes to the information herein for the improvement of the design and performance without prior notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.**
- **All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.**
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| | | | |
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Rev.: 1.3

Revision History:

1. Modify pin configuration of 5732NF1G and pin description

Rev.: 1.2

Revision History:

1. Add QFN-32 package

Rev.: 1.1

Revision History:

1. Add RE2 package

Rev.: 1.0

Revision History:

1. First release