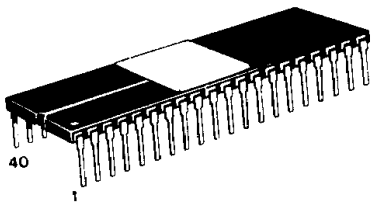
MOTOROLA

SC42584
SC42585

Advance Information

BUBBLE MEMORY CONTROLLERS



GENERAL DESCRIPTION

The SC42584 and SC42585 Bubble Memory controllers are monolithic HMOS integrated circuits which control the operation of the Motorola MBM2256 (256 Kilobit) and MBM2011 (1 Megabit) Magnetic Bubble Memories, respectively. They provide the interface between a Magnetic Bubble Memory (MBM) subsystem and the user system, including data and map loop read and write, redundant loop management, error correction, and all bubble memory timing. The SC42584 and SC42585 are functionally equivalent and pin-compatible. They differ only in data record length and bubble memory control pulse timing. They are packaged in 40-pin dual-in-line packages with 0.6-inch pin row spacing.

FEATURES

- Single-Chip Integrated Circuit
- Generation of All Bubble Memory Timing Signals
- Operation of 1 to 8 Bubble Memories in Parallel
- Complete Error Correction/Detection
- Dynamic Data Buffering of 16 Bytes
- Complete Redundant Loop Management
- Direct 8-bit Microprocessor Bus Interface
- Programmed, Interrupt, or DMA Data Transfer
- Power-Failure Interlock
- On-chip Crystal-Controlled Oscillator
- Simple Software Interface with Diagnostic Capability
- Bootloop Write with Mechanical Interlock

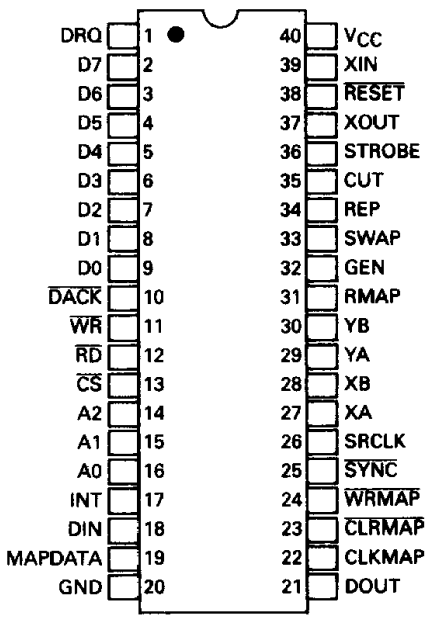
ABSOLUTE MAXIMUM RATINGS*

Characteristics	Value	Unit
Ambient temperature with power applied Commercial device Extended-temperature device	 0 to + 70 −55 to + 125	 °C °C
Storage Temperature	−65 to +150	°C
Voltage — any pin with respect to GND	−0.5 to + 7.0	Volts
Power dissipation	1.0	Watts

* Absolute Maximum Ratings indicate limits beyond which permanent damage may occur to the device. Proper operation of the device requires that it be limited to the conditions specified under DC Electrical Characteristics.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FIGURE 1 — PIN ASSIGNMENTS



40-pin dual in-line package;
0.6-inch row spacing

PIN DESCRIPTIONS

User Interface

$\overline{\text{RESET}}$ — If a command is executing, initiates an orderly termination; resets and preconditions internal registers and control logic.

Data Bus (D7–D0) — Bidirectional transfer of data, commands, and status between the user system and the controller.

Address (A2–A0) — Selects one of eight internal registers for bus transfer.

$\overline{\text{CS}}$ — Chip Select — enables the user data-bus interface.

$\overline{\text{RD}}$ — Read Enable — enables reading from the addressed register in conjunction with $\overline{\text{CS}}$ or $\overline{\text{DACK}}$.

$\overline{\text{WR}}$ — Write Enable — enables writing to the addressed register in conjunction with $\overline{\text{CS}}$ or $\overline{\text{DACK}}$.

INT — Interrupt — programmable to indicate data request or command completion.

DRQ — Data Request — indicates that the contrller is ready for a data byte transfer to or from the user system.

$\overline{\text{DACK}}$ — Data Acknowledge — enables a transfer between the bus and the data buffer in conjunction with $\overline{\text{RD}}$ and $\overline{\text{WR}}$ but independent of A2–A0.

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External Map Memory Interface

MAPDATA — Data from external redundancy-map memory.

$\overline{\text{CLRMAP}}$ — Initializes (clears to zero) the redundancy-map memory address counter.

CLKMAP — Rising edge increments the redundancy-map memory address counter.

$\overline{\text{WRMAP}}$ — Enables writing data from the MBM(s) to the redundancy-map memory.

Supplies and Miscellaneous

XIN, XOUT — Crystal connections for controller clock oscillator. Alternatively, XIN may be driven with an externally-generated square wave at standard TTL levels, in which case, XOUT should be left unconnected.

V_{CC} — Power supply voltage: 5 V ± 5 percent.

GND — System ground.

Bubble Memory Interface

DIN — Data In — serial data from MBM sense amplifier (single-MBM bank) or parallel-to-serial shift register (multiple-MBM bank).

DOUT — Data Out — serial data to MBM operation driver (single-MBM bank) or to serial-to-parallel shift register (multiple-MBM bank).

STROBE — Data timing signal — defines sample window for sense amplifier. Trailing edge latches detected data in sense amplifier. Leading edge latches data into operation driver in single-MBM bank.

$\overline{\text{SYNC}}$ — Data timing for multiple-MBM bank. Loads data from sense amplifiers into a parallel-to-serial shift register. Trailing (rising) edge clocks data from a serial-to-parallel shift register into the operation driver(s).

SRCLK — Clock for shift registers used in a multiple-MBM bank. Rising edge advances shift registers. Falling edge internally samples data on DIN or changes data on DOUT.

GEN — Generate
SWAP — Swap
REP — Replicate
RMAP — Replicate Map
CUT — Cut

} Timing signals to operation driver which control the corresponding currents. Cut current is produced by the conjunction of CUT and REP or CUT and RMAP.

XA — X coil positive current enable.
XB — X coil negative current enable.
YA — Y coil positive current enable.
YB — Y coil negative current enable.

} When the −A and −B signals are both high, the corresponding coil is off and both ends are grounded.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Volts ±5% unless otherwise specified.)

Parameter	Symbol	Min	Max	Unit
Input Low Voltage	V_{IL}	−0.5	0.8	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −500 μA)	V_{OH}	2.4	—	V
V_{OH} for XA,XB,YA,YB (1)	V_{COH}	2.4	—	V
XIN Input Low Voltage	V_{XINL}	−0.5	0.4	V
XIN Input High Voltage	V_{XINH}	2.4	V_{CC} + 0.5	V
Input Current (V_{IN} = 0 to V_{CC})	I_{IL}	—	10	μA
Output Off-state Current (V_{OUT} = .45 to V_{CC})	I_{OZ}	−10	10	μA
V_{CC} Supply Current (V_{CC} = 5.25 V)	I_{CC}	—	150	mA

(Note 1) V_{CC} = 5 V, I_{OH} = − 0.5mA
V_{CC} = 2.8 V, I_{OH} = −0.1mA

AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Clock Period	t_{CY}	100	333	ns
Clock High Time	t_{CH}	0.4	0.6	t_{CY}
Clock Rise Time	t_{CR}	—	25	ns
Clock Fall Time	t_{CF}	—	25	ns
$\overline{RESET}$ Pulse Width	t_{WRE}	64	—	t_{CY}
Reset Disable Delay	t_{DRD}	—	192	t_{CY}
DRQ Turn Of Delay	t_{DDR}	—	300	ns
INT Turn Off Delay	t_{DIN}	—	150	ns
$\overline{CS}$ & Address Set Up	t_{AS}	25	—	ns
$\overline{CS}$ & Address Hold	t_{AH}	0	—	ns
Time Between Successive $\overline{RD}$ Pulses	t_{ROFF}	2.0	—	t_{CY}
Read Data Delay (C_L = 30 pF) (C_L = 100 pF)	t_{DDR}	 — —	 250 300	 ns ns
Data Bus Turn Off (C_L = 20 − 100 pF)	t_{DZ}	20	100	ns
$\overline{WR}$ Pulse Width	t_{WW}	200	—	ns
Time Between Successive $\overline{WR}$ Pulses	t_{WOFF}	2.0	—	t_{CY}
Write Data Set Up	t_{DSW}	25	—	ns
Write Data Hold	t_{DHW}	25	—	ns
DIN, MAPDATA Set Up	t_{DIS}	50	—	ns
DIN, MAPDATA Hold	t_{DIH}	50	—	ns
DOUT Delay	t_{DOD}	—	100	ns

BUBBLE MEMORY DEVICE OPERATION

The magnetic bubble memory (MBM) device stores data as the presence or absence of locally-polarized domains referred to as bubbles in a thin film of magnetic garnet material. A pattern of magnetic material on the surface defines stable locations for the bubbles and paths between them. A rotating magnetic field is produced in the plane of the film by two orthogonal coils within the MBM package. One cycle of field rotation advances all bubbles one position on their respective tracks. The field may be stopped at the end of any cycle, and the bubbles will remain in place.

The data storage area is organized as a number of closed storage loops. Input and output tracks carry bubbles to and from the storage loops and are interconnected with the loops at opposite ends by swap and replicate gates respectively. One physical page of data consists of one bit from each of the storage loops. Figure 2 is a functional diagram of the MBM. Actual implementation may be different. Table 1 gives the MBM capacities.

A generator creates bubbles in the input track as required to write data into the MBM. When a number of data bits equal to the number of storage loops has been entered into the input track and shifted into alignment with the loops, a swap pulse is applied which interchanges each bit in the input track with one bit in the adjacent storage loop. The bits swapped out are shifted to the end of the input track and annihilated.

To read data non-destructively, a replicate-cut-transfer pulse is applied. This pulse causes a stretched bubble at the replicate gate of each storage loop to be cut into two full-sized bubbles with the trailing bubble transferred to the output track while the leading bubble remains in the storage loop. Bubbles in the output track are then shifted to the detector which consists of a matched pair of magneto-resistive elements. Bubbles pass beneath the active detector element causing a change in its resistance, and are then destroyed. A constant current passed through the detector converts the resistance change into a voltage change. The reference detector element provides cancellation of noise induced by the rotating field, through the use of differential detection.

In order to improve MBM device yields, extra redundant storage loops are provided, and the device is permitted to have a limited number of non-functioning loops. Since data transfer between the controller and the MBM is bit serial, if the controller knows the locations of the non-functioning loops, it can skip over them. For this purpose, two additional storage loops are provided, one of which is loaded at the factory with a map of the useable data loops; the other is empty. The map loops communicate with the same input and output tracks as the data loops, but have separate control inputs for replicate and transfer-in (the map write function does not perform a true swap).

SYSTEM DESCRIPTION

The Magnetic Bubble Memory Controller provides the complete interface between a user system and a magnetic bubble memory subsystem. The user communicates with the controller via an eight-bit parallel bidirectional data bus which carries commands, data, status, and associated control information. This data bus is designed to connect directly to a microprocessor system. The controller contains eight internal registers which can be mapped via three address lines directly into memory locations or I/O ports in the user system.

The controller is specifically designed to interface with the following Motorola bubble memory devices and support circuits:

- MBM2256 and MBM2011 Magnetic Bubble Memories — 256 kilobit and one megabit devices respectively.
- SC42468 Coil Pre-driver — provides the necessary drive for the X and Y coil drivers (MOS power FETs) and also provides power supply low-voltage detection.
- MC34046 and MC34047 Operation Drivers — provide the generate, swap, replicate, and map replicate current pulses for the MBM2256 and MBM2011 respectively.
- MC34044 Sense Amplifier — provides the detector bias currents and bubble signal detection.

The controller can operate 1, 2, 4, or 8 MBMs in parallel, each with its own support circuits. Parallel operation multiplies the single-MBM physical page size and data transfer rate by the number of MBMs operated (1, 2, 4, or 8). Consecutive data bits are written to and read from adjacent MBM devices cyclically; therefore each data record is distributed across all the MBMs. Single and multiple MBM systems are shown in Figures 3a and 3b.

The controller can be interfaced to several banks of MBMs, each containing multiple MBMs (not necessarily the same number). This is accomplished by using the chip select inputs on the support devices to enable one bank at a time using an externally latched and decoded address. The controller operates the various banks independently, and it must be reinitialized whenever the active bank is changed. A multiple-bank system is shown in Figure 3c.

A multiple-MBM bank requires additional components as follows:

1) an eight-bit serial-to-parallel shift register which receives data from DOUT clocked by SRCLK, and from which data is transferred in parallel to the operation drivers by $\overline{\text{SYNC}}$. Banks of two or four MBMs use the positions corresponding to the first bits shifted in.

2) a parallel-to-serial shift register which receives data from the sense amplifiers enabled by $\overline{\text{SYNC}}$ and shifts the data to DIN clocked by SRCLK. The bit length need be only as great as the number of MBMs.

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The controller accepts only the first two or four bits shifted in for corresponding bank sizes.

3) an external redundancy-map memory and address counter (not required for two MBM2256s) to augment the controller's internal map memory. This memory subsystem is connected as shown in Figure 4. It uses the following controller signals which are described under PIN DESCRIPTIONS: $\overline{\text{CLRMAP}}$, CLKMAP, $\overline{\text{WRMAP}}$, and MAPDATA. The memory is configured as one bit wide, and is written and read serially. Map memory timing is shown in Figure 9.

In some applications, the user may wish to have the redundancy map data permanently stored in a PROM. This may be done using the configuration described in 3). In this case, the controller's internal map memory is not used.

CONTROLLER OPERATION

A block diagram of the main functional components of the controller is given in Figure 5.

User Interface

The user interface is directly compatible with many 8-bit microprocessors. The data bus provides user communication with any of the eight internal registers as selected by the address input. The INT signal can be used to interrupt the processor to request data or to indicate command termination. The DRQ and $\overline{\text{DACK}}$ signals can interface to a separate Direct-Memory-Access controller. These functions are described in detail under PROGRAMMING INFORMATION.

Data Path

The DATA BUFFER provides sixteen bytes of dynamic buffering between the user and the bubble memory subsystem. Bytes are transferred in parallel between the buffer and the SHIFTER which performs the serial-to-parallel conversion on data read from the MBM(s) through DIN or the parallel-to-serial conversion on data to be written to the MBM(s) over DOUT.

When writing, the OUTPUT MAPPER inserts zeros into the data stream at positions corresponding to the unused loops. The INPUT MAPPER deletes the corresponding bits from the input stream when reading. The redundant loop map is accessed from the MAP MEMORY during these operations and provided to the mappers. The ERROR CORRECTION circuit generates check bits and inserts them into the data stream when writing, and checks these bits when reading. It is capable of correcting any single burst of errors up to three bits long via the READ CORRECTED command.

The redundancy-map data is usually stored in one of the two separate map loops in the MBM. The controller reads this data during initialization, and stores it in the MAP MEMORY from which it is retrieved during data read and write operations. The controller has on-chip map memory sufficient to store the map for one MBM2011 or two MBM2256s. For multiple-MBM banks, additional external memory is required; the controller provides all the control signals necessary to operate this external memory.

Alternatively, the map data can be permanently stored in an external PROM or a completely external RAM may be used. In either case, the entire map is read from the external memory, and the internal map memory is not used.

The map loop also contains a synchronization pattern which is used to locate sector/page zero during initialization. The map loop is normally loaded at the factory and need only be read to initialize the controller. However, commands are provided to read and write the map loops for diagnostic purposes or to change the map loop contents. Since the map loop write uses a transfer-in rather than a swap function, the MBM must be erased using the Z-coil or an external magnetic field prior to a map write. The map transfer-in pulse is generated on the SWAP pin. A switch is required as shown in Figure 6 to properly route the current pulse to the MBM. This switch also protects against accidental destruction of the map data by an unintentional map write.

Redundant loop data are stored in alternate bit positions in one of the map loops in the MBM. The intervening bit positions and the other map loop must contain all zeros (no bubbles). All map operations access only alternate map bits so the intervening zeros are not seen by the controller. (Initialization may start in the wrong phase and read only the intervening zeros. In this case, it automatically shifts one position and rereads.) Data from the two map loops are merged when reading so that loop selection is not required. The WRITE MAP command allows specification of the desired loop.

The format of the map loop data is shown in Table 3.

Bubble Memory Data and Timing

All the necessary MBM coil drive and function-gate timing signals are generated by the controller. The coil drive timing signals are sequenced on and off so as to start and stop the drive field in the proper phase. Data to and from the MBM(s) are transferred bit-serial. The signals STROBE, $\overline{\text{SYNC}}$, and SRCLK are provided to clock this data. Control timing is given in Figure 10 and Table 4.

Oscillator

An on-chip oscillator provides the internal time base to operate the controller when connected to an external crystal as shown in Figure 7. Alternatively, XIN can be driven from an external oscillator and XOUT not used. The crystal or external oscillator frequency is 64 times the coil drive frequency.

Reset and Power-Down

The $\overline{\text{RESET}}$ pin provides internal preconditioning of

the controller logic on power-up or other system reset conditions and also acts as a power-down interrupt which provides an orderly termination of any operation in progress with no loss of data in the MBMs.

$\overline{\text{RESET}}$ initializes the registers as follows (hexadecimal values):

LPC:	0000	
CMDR:	FF	(TERMINATE)
MSR:	01	
SAR:	0000	
RCR:	00	
SFR:	00	
STR:	C1	(while $\overline{\text{RESET}}$ is active)
	01	(after $\overline{\text{RESET}}$ is removed)

The system must be initialized after a reset to synchronize the MBM(s) with the controller. The user should load the SFR according to the system configuration, and then execute an INITIALIZE command.

When $\overline{\text{RESET}}$ is brought low, the controller ensures that all control pulse and coil drive signals are properly sequenced to the off condition so that no data is destroyed in the MBMs. This will occur within three magnetic cycles after $\overline{\text{RESET}}$ goes low. Data being written will usually not have been swapped in, and will have to be rewritten when the system is restarted. Note that if $\overline{\text{RESET}}$ is generated due to detection of low DC voltage, the power supply voltages may already be out of their specified operating ranges, and proper MBM operation may not be guaranteed. The user should provide input power detection or other means of sustaining DC voltages to minimize the chance of data loss.

Error Detection and Correction

In order to ensure the integrity of the data stored in the bubble memory system, the controller employs error detection and correction circuitry which operates automatically, and is in general transparent to the user.

During a normal WRITE DATA operation, the controller calculates and appends a 12-bit error correction code (ECC) field onto each block of 512 bits (64 bytes) written. Extra minor loops are provided in the MBMs for this field. The ECC used is a Fire Code which permits the identification and correction of any single burst of errors up to three bits long.

During a READ DATA operation, the controller recalculates the ECC field to verify the data. If an error is detected, the controller stops (provided the Stop on Error bit is set) and indicates the error in the status register. It also saves the ECC syndrome and data block address to enable re-reading (and error correction) of the erroneous block.

Two types of errors can occur:

1) Soft errors — due to transient phenomena in the detection and sense circuitry. The data in the memory is good and can usually be re-read correctly.
2) Hard errors — due to incorrect data in the MBM(s). The READ CORRECTED command rereads the erroneous block and sends corrected data to the user in most cases. The data should then be re-written to the MBM(s) to correct the memory contents.

Soft and uncorrectable errors are detected and indicated only by the READ CORRECTED command. If an error is detected during a READ DATA command with Stop on Error set, the controller saves the calculated ECC syndrome. The READ CORRECTED command uses two separate ECC circuits: one attempts to do error correction using the error syndrome, the other recalculates the syndrome on the raw data received from the MBM(s). This recalculated syndrome is compared to the saved syndrome from the READ DATA. If they are not equal, the Soft Error bit is set indicating that the data reread was *not the same as the originally-read data.* If the error-*correction* circuit does not find a correctable error, the Uncorrectable Error bit is set.

If a soft error occurs, the error-correction circuit cannot function properly. However it may have been "fooled" and changed some data. Therefore the data received during READ CORRECTED with a soft error indication should be ignored, and the data reread with the READ DATA command.

Hard errors are rare, and the block structure of the MBM, and interleaved operation of multiple MBMs causes most hard errors to be correctable, i.e. a hard failure in a single minor loop affects only one bit in any ECC block (except for a single MBM2256 system).

The controller also calculates and inserts an ECC field during a WRITE MAP operation. This field is checked during the INITIALIZE (L=1) and READ MAP (C=1) operations; however error correction is not performed for the map data.

The ECC details and capabilities are summarized in Table 5.

PROGRAMMING INFORMATION

Nine basic commands with 24 options provide total control of the bubble memory subsystem. The user stores a command into the command register, transfers data bytes as required, then checks the controller status to verify proper completion of the operation.

Registers

Eight registers are directly accessible by the user via the data bus. The desired register is selected by the three-bit address on A2–A0 when $\overline{\text{CS}}$ is true (low). (DATA can also be selected by $\overline{\text{DACK}}$.) All are read-write except the STR which is read only.

While a command is executing (READY = 0), writing is inhibited except to DATA and to CMDR bits 1&0; therefore only a Terminate (Immediate) command can be accepted (CMDR bits 7–2 will not be altered). The registers are summarized in Table 6.

Symbol (Address)	Name and Use
CMDR (000)	— Command Register — loaded by the user with the command to be exe-

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cuted by the controller (see Commands).

MSR (001) — Multiple Sector Register — loaded by the user with the number (0 indicates 256) of sectors/pages to be read or written by the subsequent multiple sector READ DATA or WRITE DATA command (not used for single sector commands).

SARL (010) SARH (011) — Sector Address Register, two bytes, L=Low-order 8 bits, H=high-order bits — loaded by the user with the address of the (first) sector/page to be read or written by the subsequent (multiple sector) command.

RCR (100) — Residual Control Register — selects various options which apply to subsequent commands. Individual bits provide specific options as follows:

Bit	Function
7	Not used, always zero.
6	Read Buffer Enable — used primarily for diagnostic functions. This bit must be set to 1 if it is desired to read from the data buffer when no command is in progress. Otherwise, the buffer may be written into, but not read from. For proper operation, it must be reloaded with a 0 before initiating a subsequent command. 0: Buffer is write-only between commands. 1: Buffer is read-only between commands.
5	Stop on Error — causes the controller to terminate any READ DATA command at the end of any ECC block in which a data error was detected. The ECC logic, SAR, and MSR are left in the proper state for execution of a READ CORRECTED command.
4	Half Buffer — causes DRQ to be set only when the buffer is at least half full* (READ) or half empty (WRITE). When Half Buffer is set to 1, data may be transferred in 8-byte bursts in response to DRQ. The setting of DRQ according to Half Buffer and the number of bytes in the buffer is as follows: HB READ WRITE 0: ≥ 1 byte ≤ 15 bytes 1: ≥ 8 bytes* < 8 bytes *or at end of command if buffer is not empty.
3	Enable READY Interrupt — causes INT to be activated at the termination of any command. INT is cleared by reading STR or writing CMDR. May be set concurrently with bit 2.
2	Enable DRQ Interrupt — causes INT to be activated whenever DRQ is true. May be set concurrently with bit 3.
1	Page Addressing Mode — (see Sector Page Addressing)- 0: Sector Addressing Mode (default). 1: Page Addressing Mode.
0	Write Protect — prevents any WRITE command from being executed. A write protect error will be indicated if any WRITE (Map or Data) is attempted with Write Protect = 1.

SFR (101) — System Features Register — defines the system configuration. Functions of the individual bits are as follows:

Bit	Function
7–3	Not used, always zero.
2	External Map — indicates that all map data is to be stored or is pre-stored in the external map memory (RAM or PROM). The controller does not use its internal map storage.
1, 0	Bank Size — specifies the number of MBMs in the active bank as follows: 00: 1 MBM, 01: 2 MBMs, 10: 4 MBMs, 11: 8 MBMs

STR (110) — Status Register (Read Only) — indicates the status of the command in progress or last ended — cleared when CMDR is loaded (except TERMINATE when busy) or by $\overline{\text{RESET}}$. Certain bits pertain only to specific commands or are defined differently for different commands. The meanings of the bits are as follows:

Bit	Command	Meaning
7	RDC	Soft Error — the recomputed ECC syndrome did not match the previous syndrome (see Error Correction/Detection).
6	WRD,WRM	Write Protect bit is set — command not executed.
7&6	—	$\overline{\text{RESET}}$ pin is active (low).
5	RDD,WRD	Sector/page Address Out of Range for the number of MBMs specified.
	RDM (C=1)	Map compare error — the data read from the

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		MBM(s) did not match that in the map memory.
	INIT	Initialization error — synchronization pattern could not be found.
4	RDC	Non-correctable error.
3	all READS	Data Error detected (ECC). For RDC command, indicates that error is in a different block than previous error.
2	all READS and WRITES	Data Buffer overrun — the user did not read/write the data buffer fast enough to keep up with the MBM data transfer rate, or the user attempted to read/write the buffer when DRQ = 0.
1	all RD & WR	Data transfer request (DRQ).
0	all	Ready — previous command has terminated and controller is ready to receive a new command.
DATA (111)		Data buffer — a 16-byte first-in-first-out (FIFO) buffer used for all data transfers.

Sector/Page Addressing

A *page* of data corresponds to a single physical read or write of the MBM(s) — therefore, the page length is determined by the MBM type (256K or megabit) and the number of MBMs specified in the SFR. The number of pages in a bank is independent of the number of MBMs, and is determined only by the MBM type.

Note: A minimum block size of 64 bytes is required for the ECC. Therefore, a single 256K-bit bank utilizes two physical pages per logical page.

A *sector* is a fixed-length record independent of the number of MBMs specified in the SFR and is equal to the maximum-length page for the MBM type. Therefore, the number of sectors in a bank is proportional to the number of MBMs.

Sector addressing is selected by default. Page addressing may be selected by setting the Page Mode bit = 1 in the RCR. Sector and page addressing are equivalent for a maximum bank of 8 MBMs.

Regardless of the mode or number of MBMs, error detection/correction is performed on blocks of 512 bits (64 bytes). In general, there are multiple ECC blocks within a sector/page.

Table 7 shows the sector and page sizes and counts for all configurations.

Logical Addressing

Propagation of the bubbles along the input or output track causes the data loops to be shifted an equal distance. Thus, following a replicate and clearing of the output track, the physically adjacent page has propagated well past the replicate gates; a similar affect occurs during consecutive writes. In order to provide minimum access time when reading or writing consecutive pages/sectors, the controller uses a logical addressing scheme such that consecutive logical pages are spaced several physical locations apart to account for the latency described above. This spacing is given in Table 8.

The controller maintains the current logical page/sector address in the Logical Page Counter (LPC), a non-accessible register which is incremented by the appropriate value during each active MBM cycle. The LPC is compared to the SAR to locate the desired page/sector for READ & WRITE commands. To synchronize the LPC with the MBM contents, the INITIALIZE or CLEAR LPC command should be used. $\overline{\text{RESET}}$ also clears the LPC to zero regardless of MBM position.

The timing of the WRITE DATA command is such that consecutive commands to consecutive logical addresses (without reloading the SAR) will be accomplished with minimum latency. During a multiple-page/sector READ DATA command, replicates are performed "on the fly" as each logical page reaches the replicate position; however the extra propagation distance between the replicate gates and the detector means that at the termination of a READ DATA command, the next logical address has passed the replicate position. The POSITION READ command will give minimum access time when consecutive logical pages/sectors are to be read with single-page/sector commands.

Commands

The user initiates operation of the controller by writing a command byte into the command register (CMDR). The various commands are described below and summarized in Table 6. For each command, the value to be loaded into the CMDR is given in binary with certain option bits which affect its operation. Use of the SAR and MSR is described where applicable. These registers, when used, as well as the SFR and RCR, must be loaded prior to loading the CMDR.

Data Transfer

All data transfers are made to/from the data buffer which is accessed as register 7. During a read or write command execution, when the controller determines that a data transfer is required, it does the following:

1) sets the DRQ bit in the status register.
2) raises the DRQ pin to the active (high) state.
3) if RCR bit 2 (Enable DRQ Interrupt) is set, raises the INT pin to the active (high) state.

Any of these conditions may be recognized by ap-

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propriate software or hardware as indicating that data transfer is required. The user then transfers one or more bytes to or from the buffer using $\overline{WR}$ or $\overline{RD}$ and either of the following:

1) addressing Register 7 ($\overline{CS}$ = 0, A2,A1,A0 = 111).

2) activating $\overline{DACK}$ ($\overline{CS}$ = 1, $\overline{DACK}$ = 0, A2–A0 ignored).

The DRQ and $\overline{DACK}$ signals may be used with a separate direct memory access (DMA) controller. DRQ and INT (if used) remain active as long as data transfer is required.

If the RCR Half Buffer bit is set to 1, then eight bytes can always be transferred in a burst when a DRQ occurs.

Notes:

The WRITE DATA (S = 0) AND WRITE MAP commands do not begin execution until the first data byte has been written into the data buffer. When using programmed data transfer, the user should always load the first 16 data bytes in a burst as fast as possible so as to provide adequate buffering for the operation. (It is not necessary to check DRQ since the buffer is known to be empty at the start of the command.)

Due to the asynchronous operation of the data buffer, the controller always attempts to keep it full during a write operation. As a result, it may request up to 16 additional bytes at the end of a write depending on the user system response time. Response to these extra DRQs is optional: extra bytes transferred will not be written to the MBM(s); ignoring the DRQ will not cause an error.

Termination and Status

When the command execution is finished, the controller:

1) sets the Ready bit and any other bits which are appropriate in the status register.
2) if RCR bit 3 (Enable Ready Interrupt) is set, raises the INT pin to the active (high) state.

The user should read the status register to verify proper completion of the previous command and take any corrective action indicated. Ready indicates that the controller is able to accept a new command.

INT, if used, is cleared by reading the status register or loading the command register.

Command Descriptions

INITIALIZE (INIT) CMDR = 1111 L100

Read the map loop until the synchronization pattern (64 ZEROs followed by a ONE is detected, then set the logical page counter (LPC) to zero. Then if L = 1, load the redundancy map memory with the map data.

If the synchronization pattern is not found after one complete cycle of the map loop, the map loop is shifted one position and a second attempt is made reading the interleaved bits.

INITIALIZE should be executed after any of the following:

1) Power off-on.
2) Reset.
3) Bank switching or MBM change.

Page synchronization is then maintained until any of the above conditions occurs. The Load Map Memory (L = 1) option should be used unless it is not desired to use the redundant-loop map or the map has been prestored in an external PROM.

Register usage: None.

Errors detected:
Initialization error — the synchronization pattern could not be found on either pass.
Data error — an ECC error was detected when reading the map data.

CLEAR LPC (CLPC) CMDR = 0010 0000

Clear the Logical Page Counter (LPC) to zero without accessing the MBM(s) or loading the map memory. Permits the user to synchronize the controller to sector page zero without using the map loop(s), e.g. by recognizing a page with a unique data pattern.

Useful in systems where the map data are stored in an external PROM and the bulk erase capability of the MBM is utilized, since bulk erase will destroy the synchronization pattern along with the data.

POSITION (POS) CMDR = 0W10 1000

Position the MBM data for minimum access time for a subsequent READ DATA (W = 0) or WRITE DATA (W = 1) command. RDD and WRD will automatically position the MBM(s) if required; POS minimizes the latency at the time the RDD or WRD is executed.

Register Usage:

Start:	SAR:	Address of sector/page to be read or written by a subsequent command.
End:	SAR:	Unchanged. **The SAR should not be reloaded prior to issuing the RDD or WRD command, even with the same address, or the effect of POS will be lost and the RDD or WRD access time will be excessive.**

WRITE DATA (WRD) CMDR = 010M US00

Write one or more sectors/pages of data. Positioning is performed if the MBM(s) have not been pre-positioned.

M = 0:	Write one sector/page.
M = 1:	Number of sectors/pages is specified in MSR.

U = S = 0: Normal Write — user sends only data bits; zeros are inserted for redundant loops, and ECC bits are generated and appended.
U = 1,S = 0: Unmasked Write — user sends data for all loops including redundant and ECC bits.
U = 0,S = 1: Suppress Transfer — the 16 bytes currently in the buffer are written repeatedly, with redundant loop and ECC bits inserted as in a normal write; the user does not send data.
U = S = 1: NOT ALLOWED.

Register Usage:

Start: SAR: Address of (first) sector/page to be written.
MSR: M = 0: Not used.
M = 1: Number of sectors/pages to be written.

End: Norm: SAR: Address of last sector/page written + 1.
MSR: M = 0: Unchanged.
M = 1: MSR = 1.

Error: SAR: Address of the sector/page having the error.
MSR: M = 0: Unchanged.
M = 1: Number of sectors/pages still to be written including the one with the error.

Errors detected:

Write protect — write protect bit is set; WRD is not executed.
Out of Range — if the initial address is out of range, the command is not executed; if a command attempts to write past the end of the installed memory, the command terminates after the last allowable sector/page.
Overrun — the command is terminated immediately.

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READ DATA (RDD) CMDR = 000M US00

Read one or more sectors/pages of data. Positioning is performed if the MBM(s) have not been pre-positioned.

M = 0: Read one sector/page.
M = 1: Number of sectors/pages is specified in MSR.

U = S = 0: Normal Read — redundant loops and ECC are masked and remaining bits are sent to the user; ECC is checked and errors reported.
U = 1,S = 0: Unmasked Read — all bits are sent to the user; ECC is not checked.
U = 0,S = 1: Suppress Transfer — data are not sent to the user; ECC is checked and errors reported.
U = S = 1: NOT ALLOWED (= RDC command).

Register Usage:

Start: SAR: Address of (first) sector/page to be read.
MSR: M = 0: Not used.
M = 1: Number of sectors/pages to be read.

End: Norm: SAR: Address of last sector/page read + 1.
MSR: M = 0: Unchanged.
M = 1: MSR = 1.

Error: SAR: Address of sector/page having the error.
MSR: M = 0: Unchanged.
M = 1: Number of sectors/pages still to be read including the one with the error.

Errors detected:

Out of Range — if the initial address is out of range, the command is not executed; if a command attempts to read past the end of the installed memory, the command terminates after the last allowable sector/page.
Data Error (ECC) — if Stop on Error is set, data transmission to the user stops immediately following the 64-byte ECC block in which the error is detected.
Overrun — the command is terminated immediately.

READ CORRECTED (RDC) CMDR = 0000 1100

Reread the page in which an error was detected and apply error correction to the erroneous block. Only valid immediately following a READ DATA command with a Data Error indication and with the Stop On Error bit set in the RCR.

Corrected data are sent to the user starting at the beginning of the 64-byte ECC block in which the error was detected and continuing to the end of that sector or page; i.e. the last 64 bytes sent by the RDD are repeated with error correction, and the sector or page is completed. A soft or uncorrectable error in the first block or a data error in a subsequent block will be indicated if detected, but the sector/page will be completed regardless of errors or the Stop On Error bit. See *Error Detection and Correction.*

Register Usage:

Start: No registers may be loaded between the end of READ DATA and the issuing of READ CORRECTED.

End: Norm: SAR: Address of next sector/page.
MSR: Remaining sector/page count.

Error: SAR & MSR: Unchanged.

Errors detected:

Soft error — the recalculated ECC syndrome did not match the saved syndrome.
Uncorrectable error — the error was not correctable.
Data error — an error was detected in another ECC block.
Overrun — the command is terminated immediately.

TERMINATE (TERM) CMDR = XXXX XX1I

Terminate the current operation at the end of the current page (I = 0) or terminate immediately (I = 1). TERMINATE permits aborting of any command in progress at any time.

If the controller is not busy, TERMINATE is treated as a no-op, except for resetting the buffer pointers.

Register Usage: Buffer (FIFO) pointers are reset.

Errors detected: Depends upon the command being executed.

READ MAP (RDM) CMDR = 1000 C000

Read the map loop data and send to the user. The order of the data read is as shown in Table 3 grouped into 8-bit bytes with the first bit being the most-significant bit in the byte. In a multiple-MBM system, bits from the MBMs are interleaved.

C = 0: The entire map loop contents (64 or 128 bytes) are sent to the user. Error detection is not performed.

C = 1: Check Data — only the M-field and ECC-field are sent to the user; ECC checking is performed, and the map data (M-field) are compared to the contents of the map memory. Errors are reported.

Register usage: none.

Errors detected:

Map compare error (C = 1 only) — the data read from the map loop did not match that stored in the map memory.
Data error (C = 1 only) — an ECC error was detected (map error correction is not performed by the controller).
Overrun — the command is terminated immediately.

WRITE MAP (WRM) CMDR = 1100 N000

Write map loop 1 (N = 0) or 2 (N = 1) with user-supplied data. The user must supply the entire map loop contents (64 or 128 bytes per MBM) including the sync pattern as described under READ MAP. However, the ECC-field bits are ignored and replaced by ECC bits generated by the controller.

Register usage: None.

Errors detected:

Write protect — the write protect bit is set; WRM is not executed.
Overrun — the command is terminated immediately.

Note:
WRITE MAP will execute in a multiple-MBM system but will not generate correct ECC bits for multiple MBMs. It is intended for loading the map in a single MBM only. The MBM must first be erased using the Z-coil or a suitable external magnetic field. The MBM map pins must be connected as shown in Figure 6.

TABLE 1. BUBBLE MEMORY CAPACITIES

	MBM2256	MBM2011
Number of data loops:	282	584
Number of redundant loops:	20	60
Number of loops used for ECC:	6*	12
Number of usable data loops:	256	512
Number of bits per loop:	1024	2048
Number of bits of data storage:	262,144	1,048,576
Number of map loops:	2	2
Number of bits used in map loops:	512	1024

* Actually 12 bits in every other physical page.

TABLE 2. EXTERNAL MEMORY REQUIREMENTS

MBM Type	Number of MBMs	External Memory Required (bits) SFR bit 2 = 0	1
2256	1	0	282
	2	0	564
	4	534	1128
	8	1662	2256
2011	1	0	584
	2	574	1168
	4	1742	2336
	8	4078	4672

Minimum requirement; additional bits are not used.
Memory must be configured one bit wide.
Internal Map Memory capacity: 594 bits.

Bubble

TABLE 3. MAP LOOP FORMAT

Pattern:	Field	Number of bits		Note
		256K	1M	
MM --- MM	Map Data	282	584	(1)
EE --- EE	ECC	12	12	(2)
UU --- UU	User	152	362	(3)
00 --- 001	Sync	65	65	(4)
X	X	1	1	(5)

(1) Each bit marks the corresponding data loop:
M = 1: good loop.
M = 0: redundant loop.
For correct operation, there should be exactly 262 (256K) or 524 (1M) 1s in this field.

(2) Error Correction (Fire) Code — applies only over the Map Data field.

(3) May be used for any purpose such as an identification number. However, it must not contain any sequence of 64 zeros followed by a one. Such a pattern will be recognized as a sync pattern and cause incorrect initialization.

(4) Synchronization pattern — 64 ZEROs followed by a ONE.

(5) This bit is skipped after synchronization is established before reading the first Map Data bit.

TABLE 4. NOMINAL CONTROL PULSE TIMING

Pulse	256 K		MEGABIT	
	Start	Width	Start	Width
XA	33	31	33	31
shut down	12	—	12	—
XB	1	31	1	31
start up (XB off)	46	—	46	—
YA	49	31	49	31
YB	17	31	17	31
start up (YB off)	62	—	62	—
shut down	60	—	60	—
GEN	17	2	17	2
SWAP	53	63	53	63
MAP TR-IN (SWAP pin)	53	39	53	39
CUT	0	3	63.5	2
REP	1	20	1	18
RMAP	1	20	1	18
STROBE	34	12	34	12
$\overline{\text{SYNC}}$	0	4	0	4
SRCLK	0,8, . . .	4	0,8, . . .	4
$\overline{\text{CLRMAP}}$	0	46	0	46
CLKMAP	0,8, . . .	4	0,8, . . .	4
$\overline{\text{WRMAP}}$	3,11, . . .	4	3,11, . . .	4

1 unit = 1 oscillator cycle.
= 1/64th magnetic cycle.
= 5.625 degrees of rotation.
= 125 ns at 125,000 bits per second.
= 156.25 ns at 100,000 bits per second.

REFERENCE: SRCLK zero (0) transition.
All times except: ± 50 ns
$\overline{\text{SYNC}}$, $\overline{\text{CLRMAP}}$, CLKMAP: +100 / − 0 ns

TABLE 5. ERROR CORRECTION CODE SUMMARY

Type of code:	Fire Code.
Generator polynomial:	$(x^5+1)\cdot(x^7+x^6+x^5+x^4+x^2+x+1)$
No. of data bits per ECC block:	512 (282 or 584 for Map loop)
No. of check bits per ECC block:	12
Total bits per block:	524 (294 or 596 for Map loop)
Correctable errors:	any burst of 1 to 3 bits.

Redundant loop bits and interleaved zeros in the map field are not included in the ECC operation.

Bubble

TABLE 6. REGISTER AND COMMAND SUMMARY

Addr	Reg.	Reset
0	CMDR	FF
1	MSR	01
2	SARL	00
3	SARH	00
4	RCR	00
5	SFR	00
6	STR	01*
7	DATA	—

Cmd.	Byte	Option bits
RDD	0 0 0 M U S 0 0	M = Multiple
RDC	0 0 0 0 1 1 0 0	U = Unmasked
WRD	0 1 0 M U S 0 0	S = Suppress transfer
POS	0 W 1 0 1 0 0 0	W = Write position
RDM	1 0 0 0 C 0 0 0	C = Check data
WRM	1 1 0 0 N 0 0 0	N = Loop #2
INIT	1 1 1 1 L 1 0 0	L = Load map memory
CLPC	0 0 1 0 0 0 0 0	
TERM	- - - - - - 1 1	I = Immediate

* = C1 while $\overline{\text{RESET}}$ is active.

Bit	SFR	RCR	STR	(applicable command)
7:	0	0	Soft Error	(RDC)
6:	0	Read Buffer Enable	Write Protect	(WRD,WRM)
5:	0	Stop on Error	Out of Range	(RDD, RDC, WRD)
			Map Compare Error	(RDM)
			Initialization Error	(INIT)
4:	0	Half Buffer	Non-Correctable Error	(RDC)
3:	0	Enable READY Interrupt	Data Error	(all RD, INIT)
2:	External Map	Enable DRQ Interrupt	Overrun	(all RD WR)
1:	} Log_2	Page Mode	DRQ (data request)	(all RD WR)
0:	} # MBMs	Write Protect	Ready	(all)

TABLE 7. SECTOR AND PAGE SIZES

MBM	Number of MBMs	Sector		Page	
		Length (Bytes)	Number of Sectors	Length (Bytes)	Number of Pages
2256	1	256	128	64*	512
	2	256	256	64	1024
	4	256	512	128	1024
	8	256	1024	256	1024
2011	1	512	256	64	2048
	2	512	512	128	2048
	4	512	1024	256	2048
	8	512	2048	512	2048

* A minimum block size of 64 bytes is required for the ECC. Therefore, a single 256K-bit bank utilizes two physical pages per logical page.

TABLE 8. PAGE SEPARATION AND LATENCY

	256 K	MEGABIT	UNITS
Physical page length:	282	584	bits
Inter-page gap:	15	17	bits
Logical page separation:	297	601	bits
Page transfer time (incl. gap):	297 (1)	601	cycles
Read and write latency (2)			
READ DATA (RDD)			
after POSITION READ (3)	181	92	cycles
after RDD, next logical address	1024	2048	cycles
random address { min:	463	676	cycles
{ max:	1486	2723	cycles
WRITE DATA (WRD)			
after POSITION WRITE (3)	0	0	
after WRD, next logical address (3)	0	0	
random address { min:	1	1	cycle
{ max:	1024	2048	cycles
User peak data transfer rate (4)			
@ 125 kHz:	N*15,625		bytes sec
@ 100 kHz:		N*12,500	bytes sec

(1) 594 cycles for single MBM2256 (2 physical pages).

(2) Number of MBM magnetic cycles before MBM data transfer begins — there is an additional overhead delay in the controller of between three and four cycles from the loading of the CMDR (RDD) or first data byte (WRD).

(3) Provided that the SAR is not reloaded between commands.

(4) @ Field frequency. N = number of MBMs operating in parallel. This is the peak burst rate; average rate is reduced by the ratio of the number of bits transferred to the total page transfer time.

Bubble

FIGURE 2 — MAGNETIC BUBBLE MEMORY FUNCTIONAL DIAGRAM

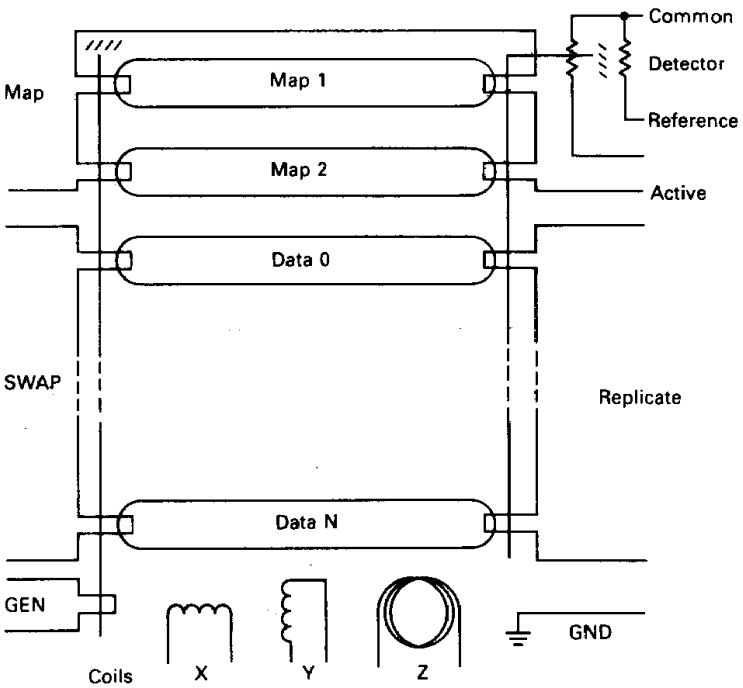


FIGURE 3a — SINGLE-MBM SYSTEM

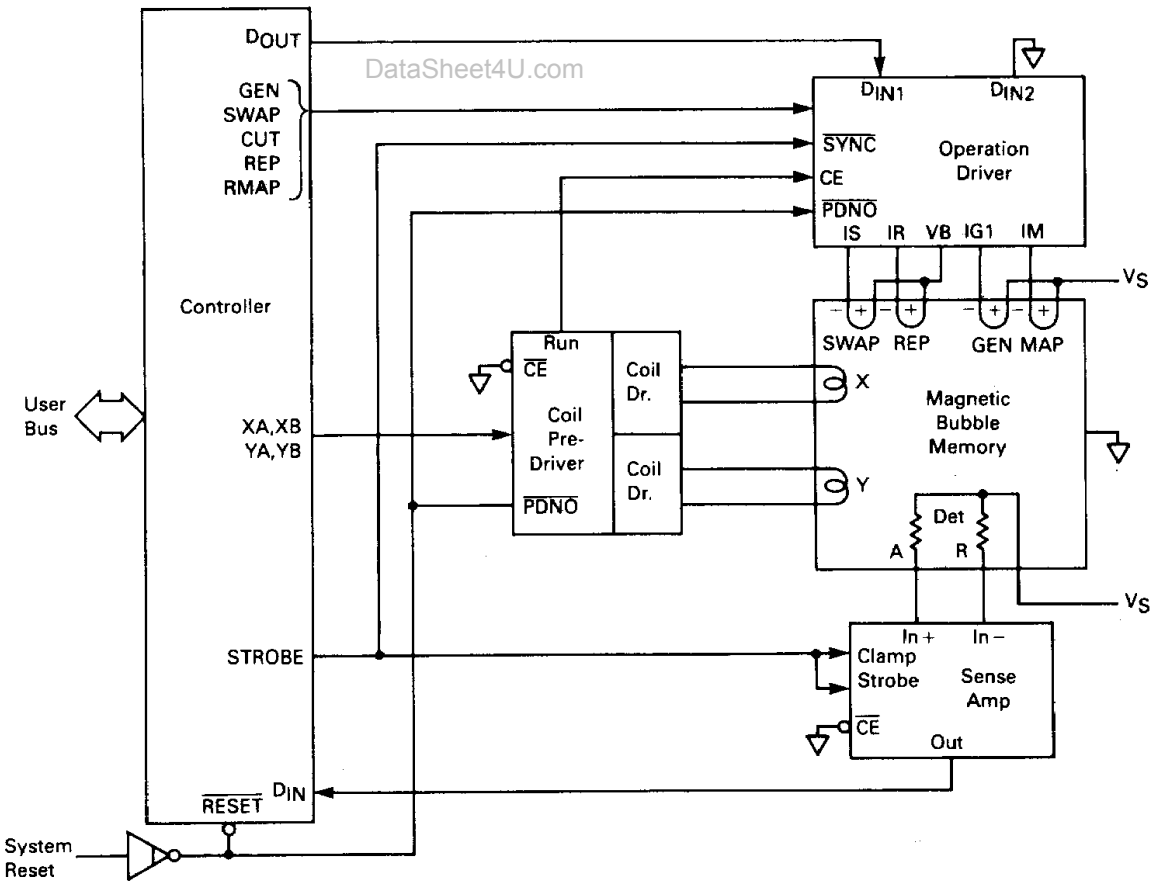


FIGURE 3b — MULTIPLE-MBM SYSTEM

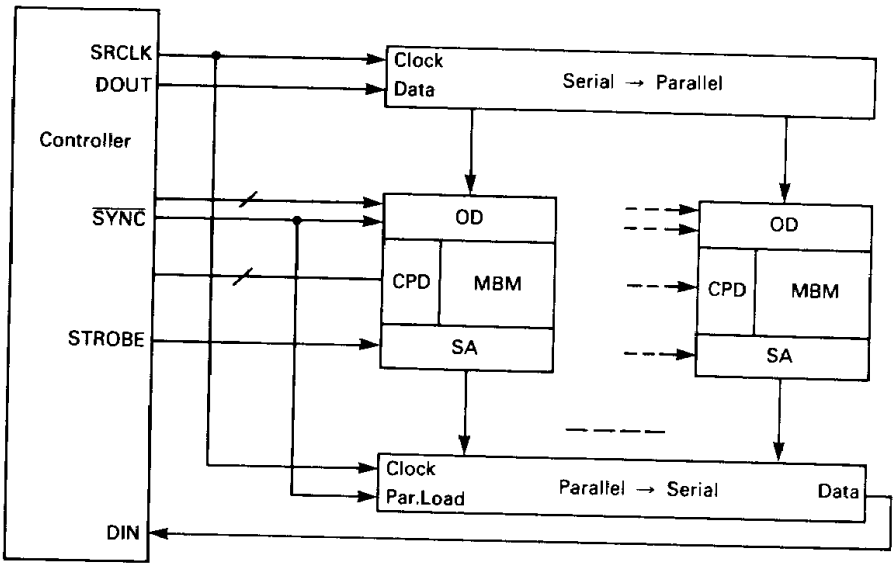
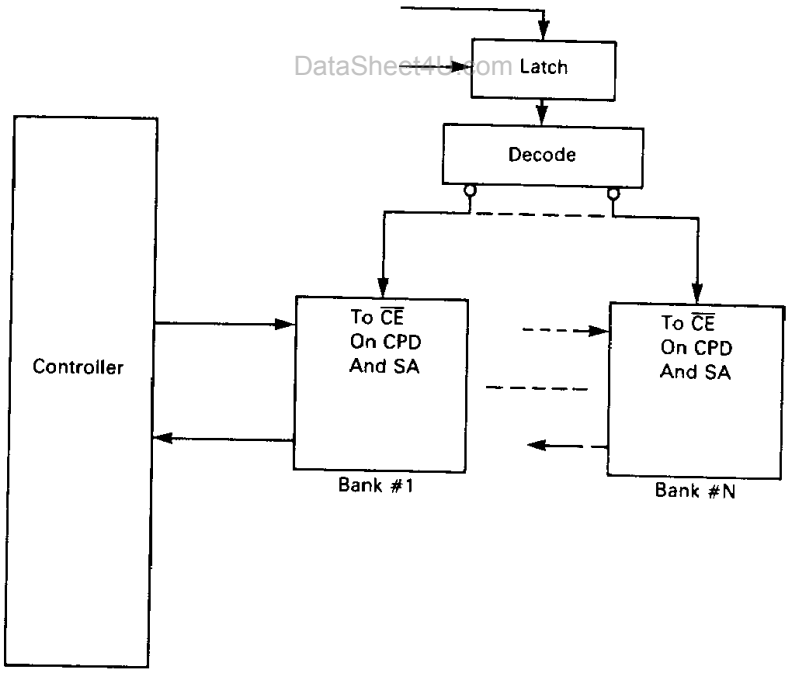


FIGURE 3c — MULTIPLE-BANK SYSTEM



Bubble

FIGURE 4 — EXTERNAL MAP MEMORY CONNECTION

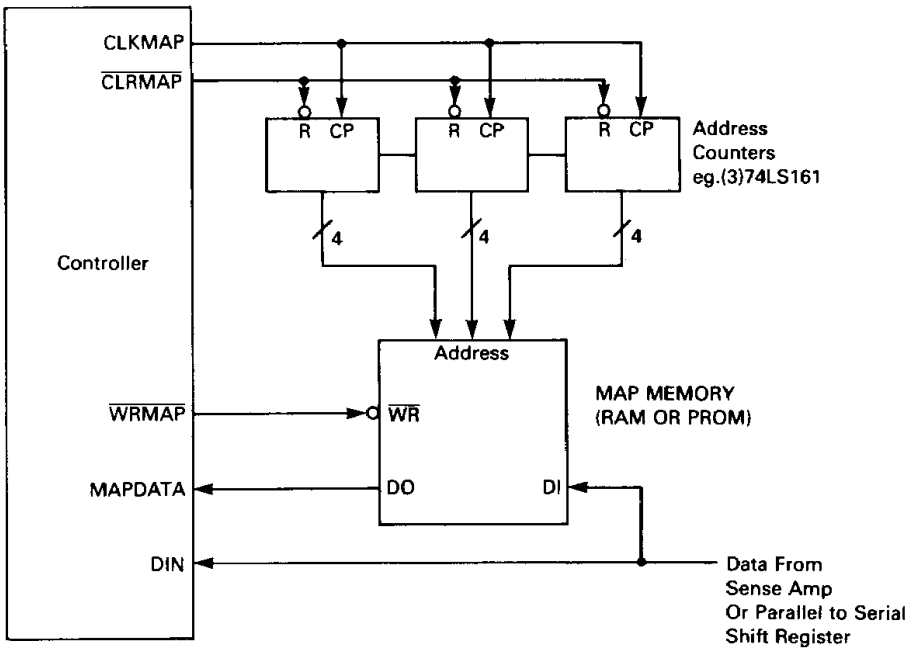


FIGURE 5 — CONTROLLER BLOCK DIAGRAM

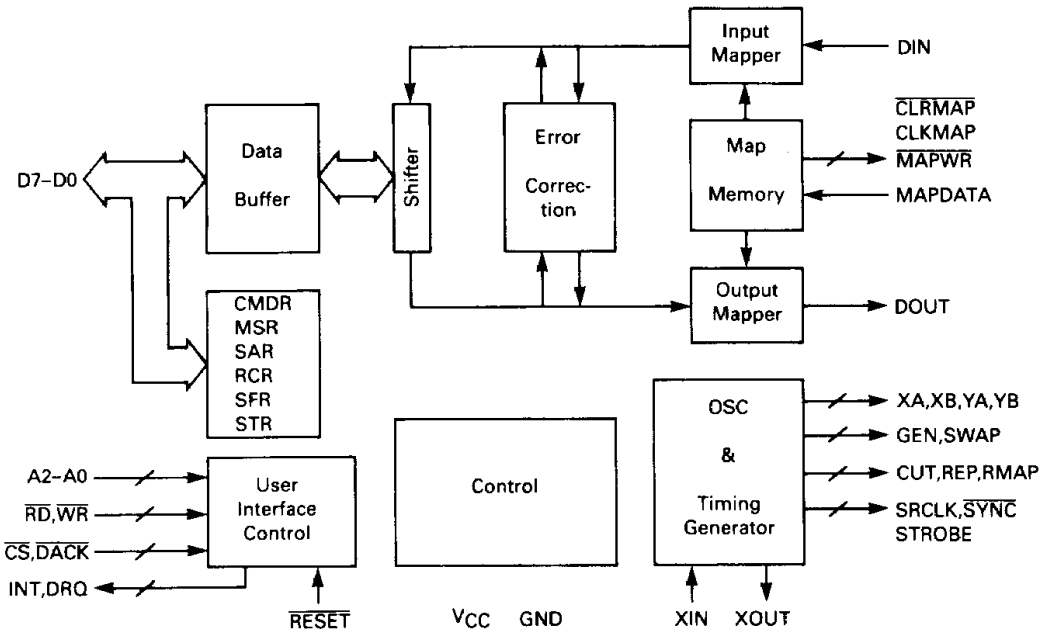


FIGURE 6 — MAP WRITE SWITCH

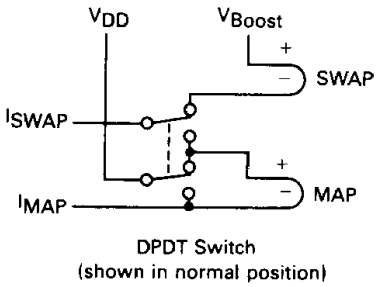


FIGURE 7 — CRYSTAL OSCILLATOR CIRCUIT

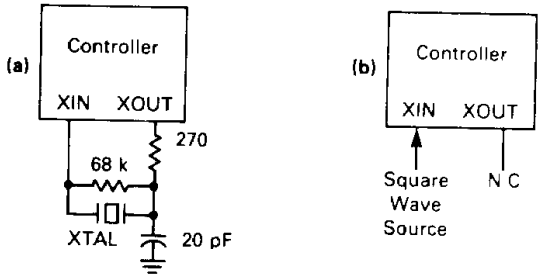


FIGURE 8 — USER INTERFACE TIMING

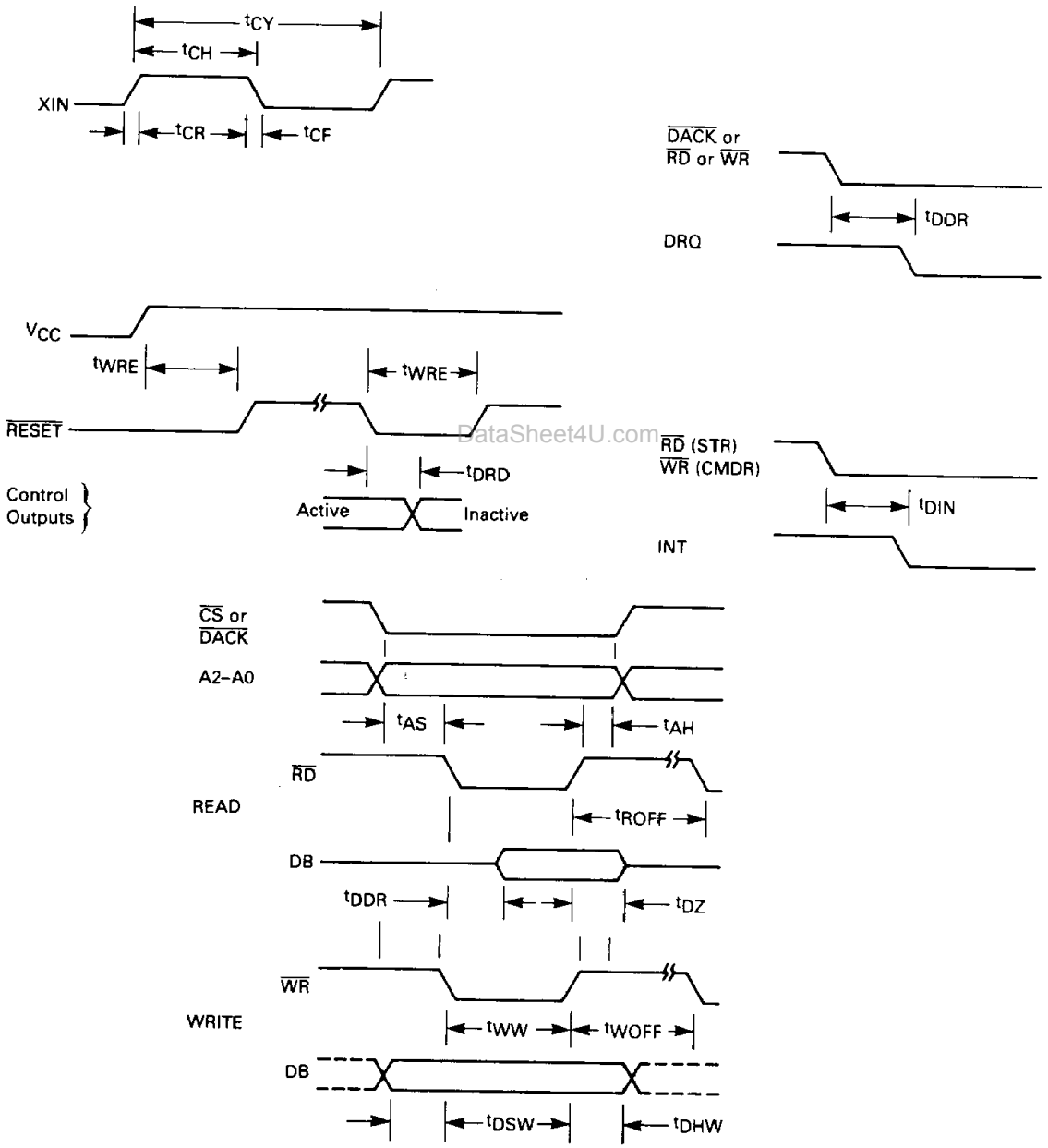
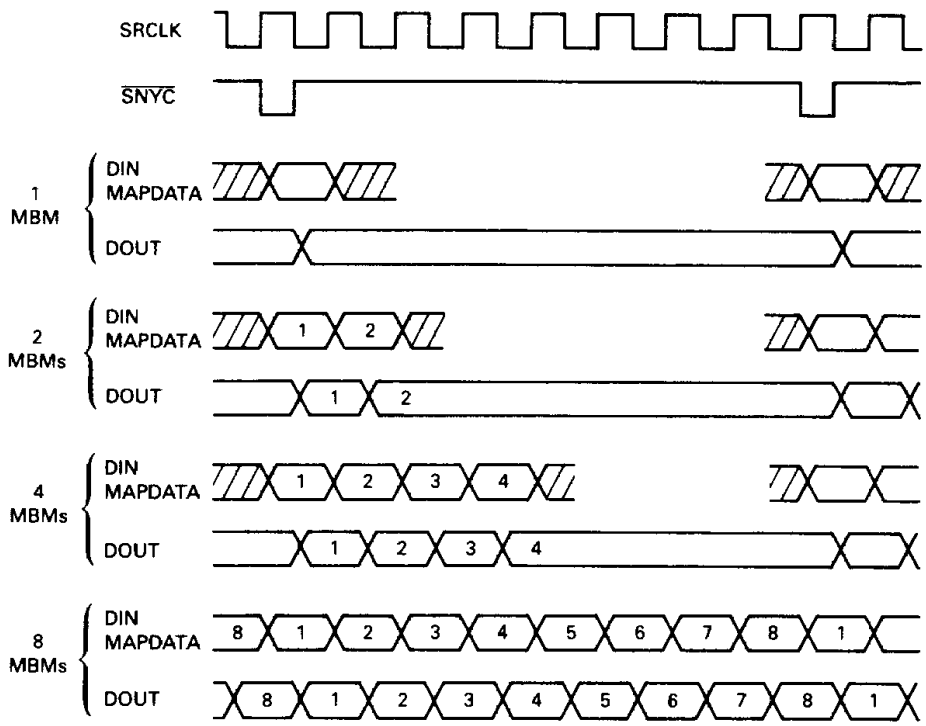


FIGURE 9 — DIN, DOUT, AND MAP MEMORY TIMING



Bubble

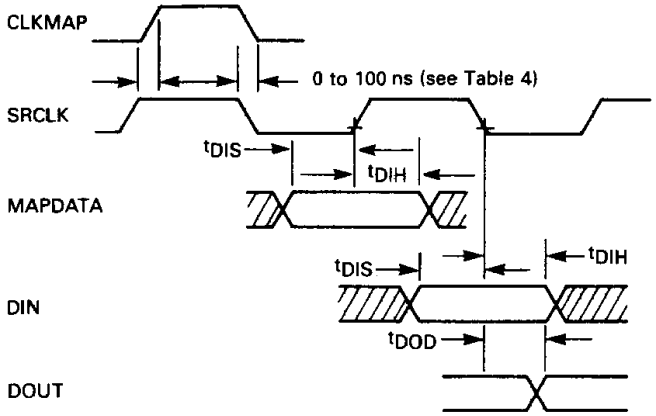


FIGURE 10 — CONTROL SIGNAL TIMING