

Dual-Phase Single or Two Output Synchronous Step-Down Controller

POWER MANAGEMENT

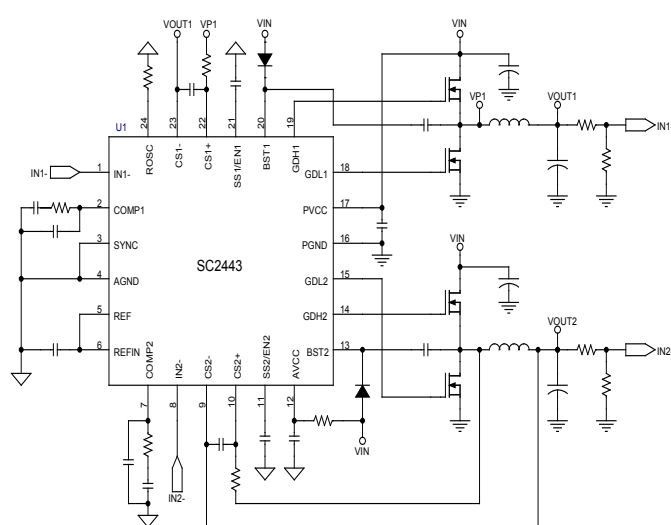
Features

- ◆ Wide input voltage range: 4.7V to 16V
- ◆ 0.5V feedback voltage for low-voltage outputs
- ◆ Programmable frequency up to 1 MHz per phase
- ◆ 2-Phase synchronous continuous conduction mode for high efficiency step-down converters
- ◆ Out-of-phase operation for low input current ripples
- ◆ Output source and sink currents
- ◆ Fixed frequency peak current-mode control
- ◆ 75mV/-110mV maximum current sense voltage
- ◆ Inductor DCR current-sensing for low-cost applications
- ◆ Dual outputs or 2-phase single output operation
- ◆ Excellent current sharing between individual phases
- ◆ Individual soft-start, overload shutdown and enable
- ◆ External reference input for DDR applications
- ◆ External synchronization
- ◆ Industrial temperature range
- ◆ 4mm X 4mm X1mm 24-lead MLPQ package

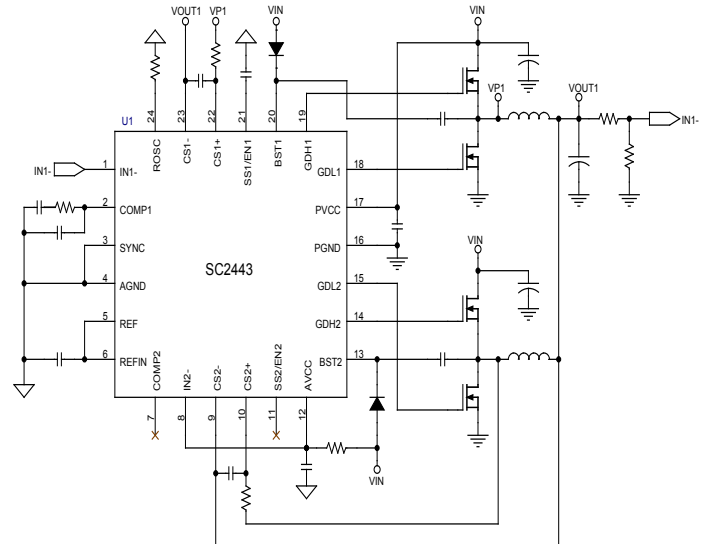
Applications

- ◆ Telecommunication power supplies
- ◆ DDR memory power supplies
- ◆ Graphic power supplies
- ◆ Servers and base stations

Typical Application Circuit



Dual Independent Outputs



Single Output With Current Sharing

Description

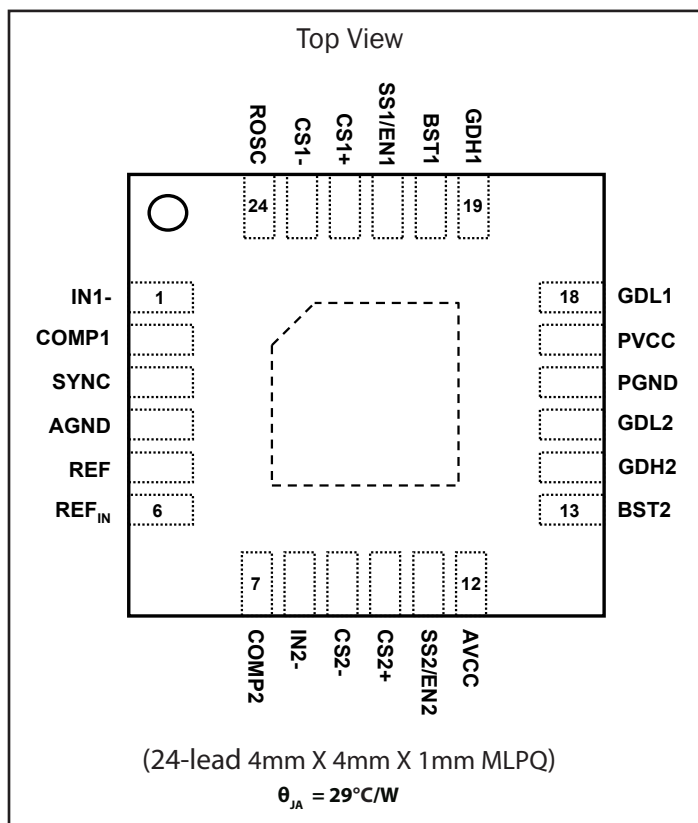
The SC2443 is a high-frequency dual synchronous step-down switching power supply controller. It provides out-of-phase high-current output gate drives to all N-channel MOSFET power stages. The SC2443 operates in synchronous continuous-conduction mode. Both phases are capable of maintaining regulation with sourcing or sinking load currents, making the SC2443 suitable for generating both VDDQ and the tracking VTT for DDR applications.

The SC2443 employs fixed frequency peak current-mode control for the ease of frequency compensation and fast transient response.

The dual-phase step-down controllers of the SC2443 can be used to produce two individually controlled and regulated outputs or a single output with shared current in each phase. The Step-down controllers operate from an input of at least 4.7V and are capable of regulating outputs as low as 0.5V

Individual soft-start and overload shutdown timer is included in each step-down controller. The SC2443 implements hiccup overload protection. In single output current share configuration, the master timer controls the soft-start and overload shutdown functions of both controllers.

Pin Configuration



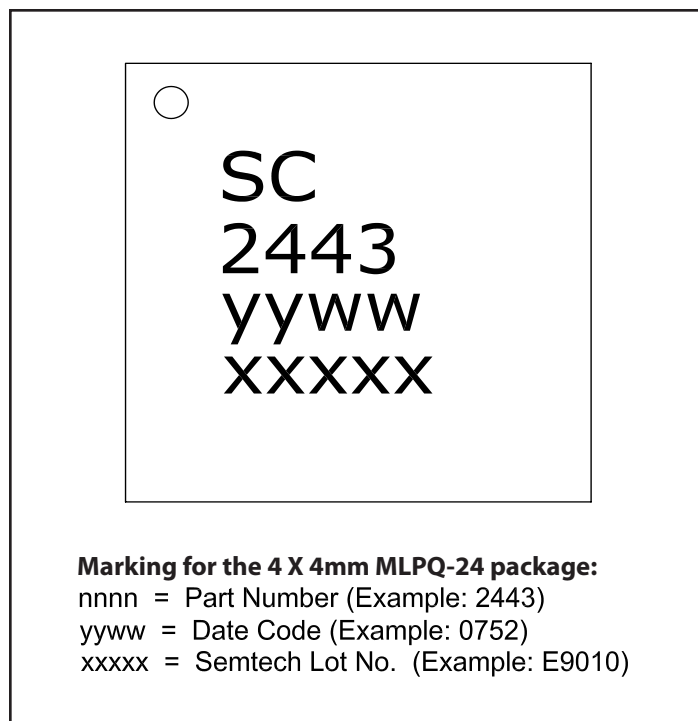
Ordering Information

Device	Package
SC2443MLTRT ^(1,2)	24-lead 4mm X 4mm X 1mm MLPQ
SC2443EVB	Evaluation Board

Notes:

- (1) Available in tape and reel only. A reel contains 3,000 devices.
- (2) Available in lead-free package only. Device is WEEE and RoHS compliant.

Marking Information



Absolute Maximum Ratings

AVCC, PVCC Voltage	-0.3 to 20V
V_{BST1}, V_{BST2} Voltage	-0.3 to 32V
SS1/EN1, SS2/EN2, SYNC Voltage	-0.3 to 6V
IN1-, IN2-, REF Voltage	-0.3 to AVCC+ 0.3V
REF _{IN} , COMP1, COMP2 Voltage	-0.3 to AVCC+ 0.3V
CS1+, CS1-, CS2+, CS2- Voltage	-0.3 to AVCC+ 0.3V
PGND to AGND	± 0.3V
Peak IR Reflow Temperature	260°C

Recommended Operating Conditions

Input Voltage Range	4.75V to 16V
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Thermal Information

Junction to Ambient ⁽¹⁾	29°C/W
Maximum Junction Temperature	150°C
Storage Temperature	-65 to +150°C

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES-

(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JEDEC51 standards.

(2) This device is ESD sensitive. Use of standard ESD handling precautions is required

Electrical Characteristics

Unless otherwise specified: AVCC = PVCC = 12V, $V_{BST1} = V_{BST2} = 12V$, SYNC = 0V, -40°C < T_A = T_J < 85°C, R_{OSC} = 51.1kΩ.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Undervoltage Lockout						
AVCC Start Threshold	AVCC _{TH}	AVCC rising		4.5	4.7	V
AVCC Start Hysteresis	AVCC _{HYST}			170		mV
AVCC Operating Current	I _{CC}			12	16	mA
AVCC Quiescent Current in UVLO	I _q	AVCC = AVCC _{TH} - 0.2V		1.7		mA
Channel 1 Error Amplifier						
Non-inverting Input Voltage	V _{IN1+}		0.49	0.5	0.51	V
Non-inverting Input Line Regulation		AVCC _{TH} < AVCC < 15V			0.02	%/V
Input Offset Voltage				1		mV
Inverting Input Bias Current	I _{IN1-}			-0.1	-0.25	μA
Amplifier Transconductance	G _{M1}			260		μΩ ⁻¹
Amplifier Open Loop Gain	A _{OL1}			65		dB
Amplifier Unity Gain Bandwidth				5		MHz
COMP1 Switching Threshold		V _{CS1+} = V _{CS1-} = 0, V _{SS1} Rising		2.2		V
Amplifier Output Sink Current		V _{IN1-} = 1V, V _{COMP1} = 2.5V		16		μA
Amplifier Output Source Current		V _{IN1-} = 0V, V _{COMP1} = 2.5V		12		μA

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Channel 2 Error Amplifier						
Input Common-mode Range ⁽¹⁾			0		3	V
Inverting Input Voltage Range ⁽¹⁾			0		AVCC	V
Input Offset Voltage				1.5		mV
Non-inverting Input Bias Current	I_{IN2+}			-150	-380	nA
Inverting Input Bias Current	I_{IN2-}			-100	-250	nA
Inverting Input Voltage for 2 phases Single Output Operation			2.5			V
Amplifier Transconductance	G_{M2}			260		$\mu\Omega^{-1}$
Amplifier Open Loop Gain	A_{OL2}			65		dB
Amplifier Unity Gain Bandwidth				5		MHz
COMP2 Switching Threshold		$V_{CS2+}=V_{CS2-}=0, V_{SS2}$ Rising		2.2		V
Amplifier Output Sink Current		$V_{COMP2} = 2.5V$		16		μA
Amplifier Output Source Current		$V_{COMP2} = 2.5V$		12		μA
Oscillator						
Channel Frequency	f_{CH1}, f_{CH2}		450	500	550	kHz
Synchronizing Frequency ⁽¹⁾			$2.1f_{CH}$			kHz
SYNC Input High Voltage			1.5			V
SYNC Input Low Voltage					0.5	V
Channel Maximum Duty Cycle	D_{MAX1}, D_{MAX2}			88		%
Channel Minimum Duty Cycle	D_{MIN1}, D_{MIN2}				0	%
Current Limit Comparator						
Input Common Mode Range			0		AVCC-1	V
Cycle by cycle Peak Current Limit	V_{ILIM1+}, V_{ILIM2+}	$V_{CS1-} = V_{CS2-} = 0.5V$, Sourcing	60	75	90	mV
Valley Current Overload Shutdown Threshold	V_{ILIM1-}, V_{ILIM2-}	$V_{CS1-} = V_{CS2-} = 0.5V$, Sinking	-85	-110	-130	mV
Positive Current sense Input Bias Current	I_{CS1+}, I_{CS2+}	$V_{CS1+} = V_{CS1-} = 0$ $V_{CS2+} = V_{CS2-} = 0$		-0.7	-2	μA
Negative Current sense Input Bias Current	I_{CS1-}, I_{CS2-}	$V_{CS1+} = V_{CS1-} = 0$ $V_{CS2+} = V_{CS2-} = 0$		-0.7	-2	μA

Electrical Characteristics (continued)

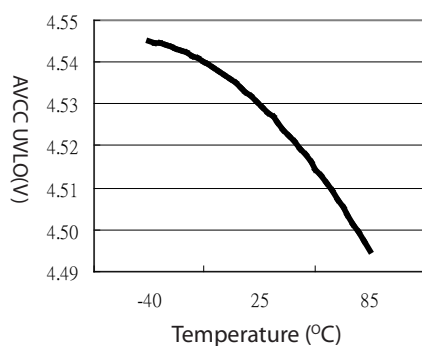
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Gate Drivers						
High side Gate Driver Peak Source Current		$V_{BST1}, V_{BST2} = 12V$		1.5		A
High side Gate Driver Peak Sink Current		$V_{BST1}, V_{BST2} = 12V$		1		A
Low side Gate Driver Peak Source Current		$AVCC = PVCC = 12V$		1.5		A
Low side Gate Driver Peak Sink Current		$AVCC = PVCC = 12V$		1		A
Gate Drive Rise Time		$C_L = 2200pF$		20		ns
Gate Drive Fall Time		$C_L = 2200pF$		20		ns
Low side Gate Driver to High side Gate Driver Non-overlapping delay		$C_L = 0$		90		ns
High side Gate Driver to Low side Gate Driver Non-overlapping delay		$C_L = 0$		90		ns
Minimum On Time		$T_A = 25^{\circ}C$		150		ns
Soft Start, Overload Latchoff and Enable						
Soft Start Charging Current	I_{SS1}, I_{SS2}	$V_{SS1} = V_{SS2} = 1.5V$		2		μA
Overload Enabling Soft Start Voltage		V_{SS1} and V_{SS2} Rising		3.2		V
Overload IN1- Threshold		$V_{SS1} = 3.8V, V_{IN1-}$ falling		$0.75V_{REF}$		V
Overload IN2- Threshold		$V_{SS2} = 3.8V, V_{IN2-}$ falling		$0.72X$		V
Soft Start Discharge Current	I_{SS1_DIS}, I_{SS2_DIS}	$V_{SS1} = V_{SS2} = 3.8V$		1.4		μA
Overload Recovery Soft Start Voltage	V_{SSRCV1}, V_{SSRCV2}	V_{SS1} and V_{SS2} Falling	0.3	0.5	0.7	V
Gate Driver Disable SS/EN Voltage			0.7	0.9		V
Gate Driver Enable SS/EN Voltage				1.2	1.5	V
Internal 0.5V Reference Buffer						
Output Voltage	V_{REF}	$I_{REF} = -1mA$	490	500	510	mV
Load Regulation		$0 < I_{REF} < -5mA$		0.05		%/mA

Notes:

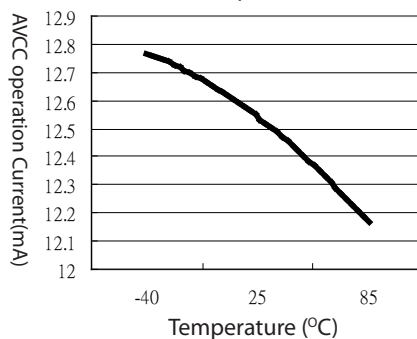
(1) Guaranteed by design.

Typical Characteristics

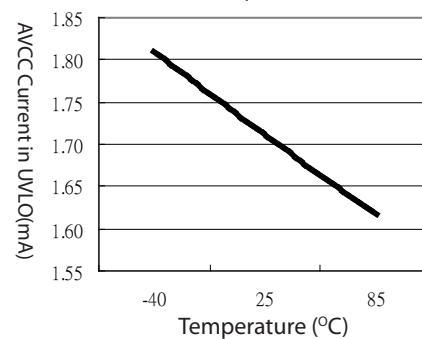
UVLO Threshold vs. Temperature



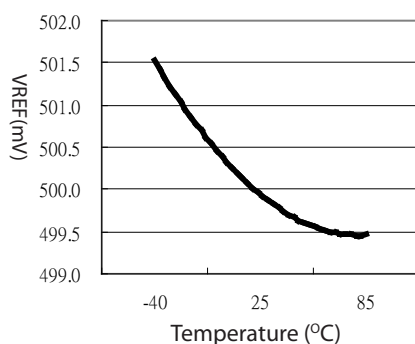
AVCC operation current vs. Temperature



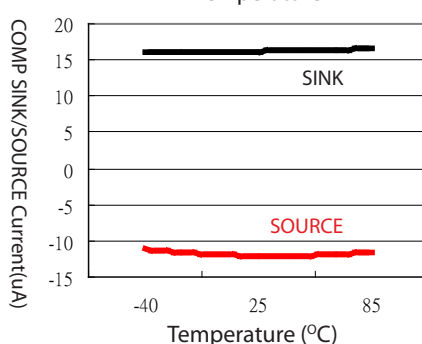
AVCC current in UVLO vs. Temperature



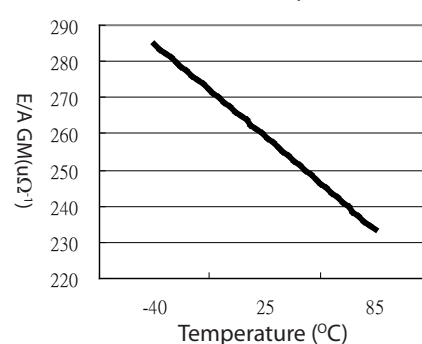
VREF vs. Temperature



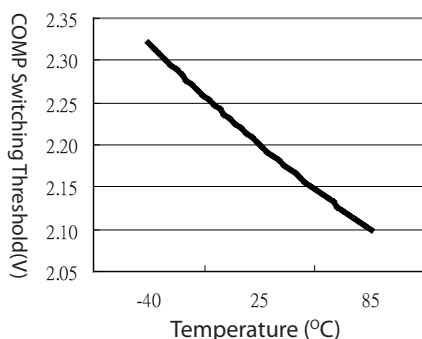
COMP Sink/Source current vs. Temperature



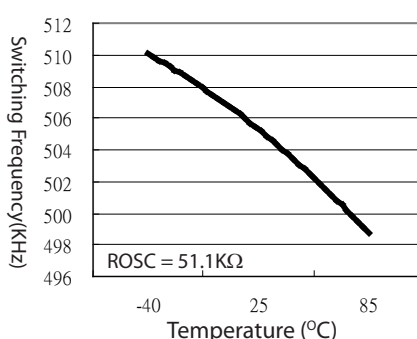
E/A GM vs. Temperature



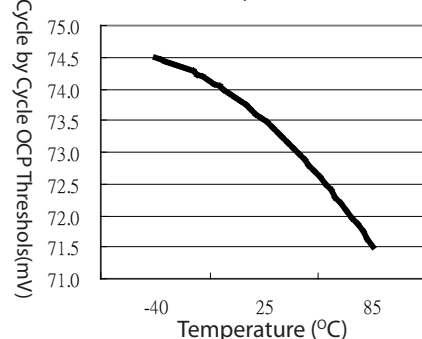
COMP switching Threshold vs. Temperature



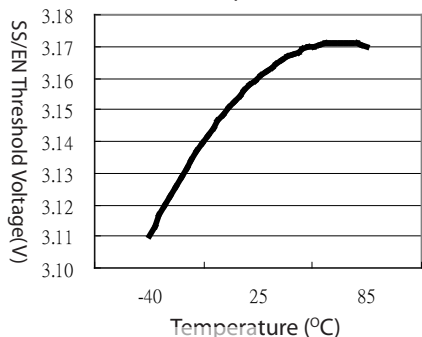
Switching Frequency setting vs. Temperature



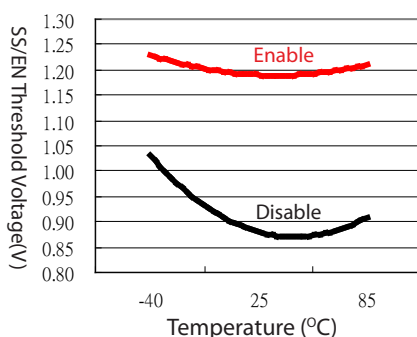
Cycle by Cycle OCP threshold vs. Temperature



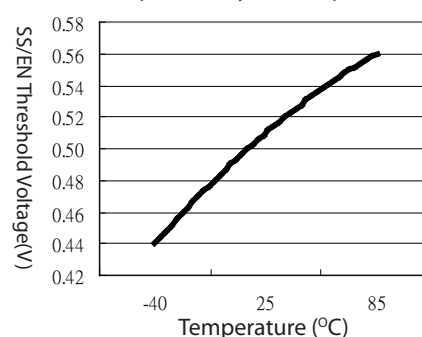
SS/EN Threshold for Overload Hiccup vs. Temperature



SS/EN Threshold for Gate Driver Enable / Disable vs. Temperature

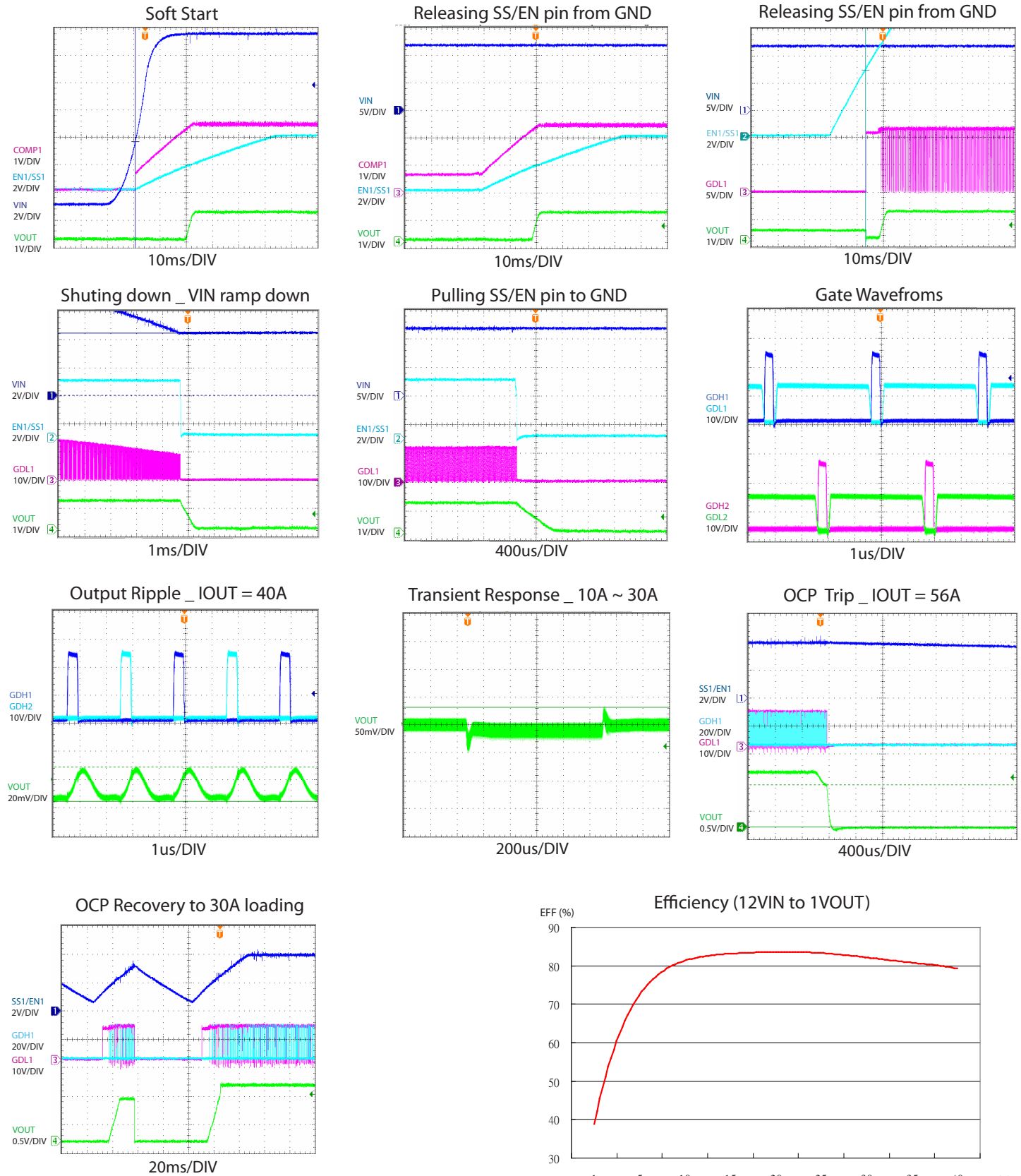


SS/EN Threshold for Overload Hiccup Recovery vs. Temperature



Typical Application Circuit Performance

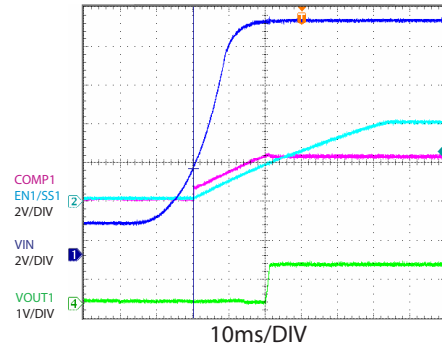
Circuit Conditions : Single output current share configuration as shown in page 15



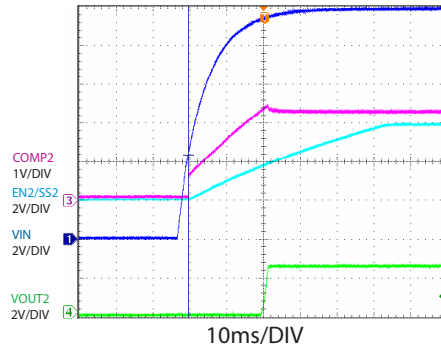
Typical Application Circuit Performance

Circuit Conditions : Dual independent outputs configuration as shown in page 17

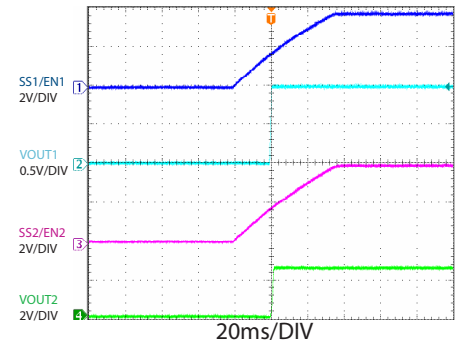
Soft Start (VOUT1)



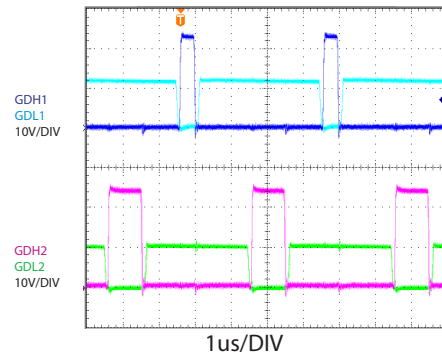
Soft Start (VOUT2)



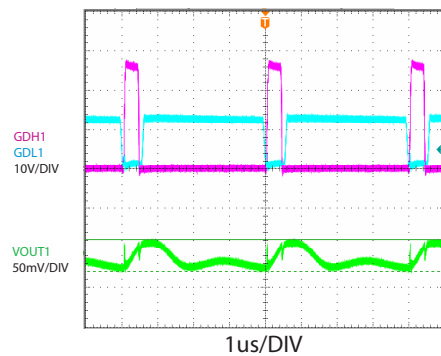
Soft Start (Both outputs)



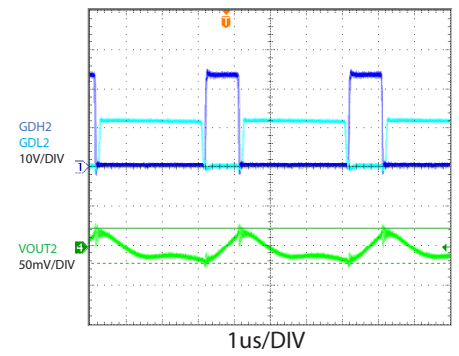
Gate waveforms (VOUT1_2 = 20A)



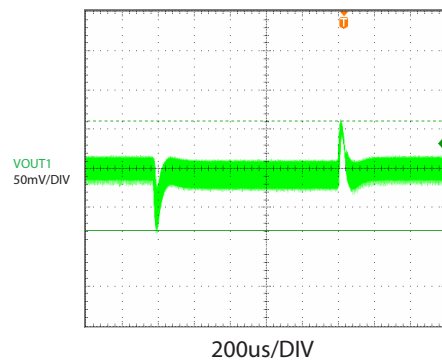
Output Ripple (VOUT1_20A)



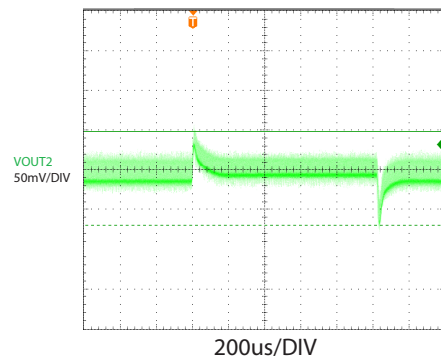
Output Ripple (VOUT2_20A)



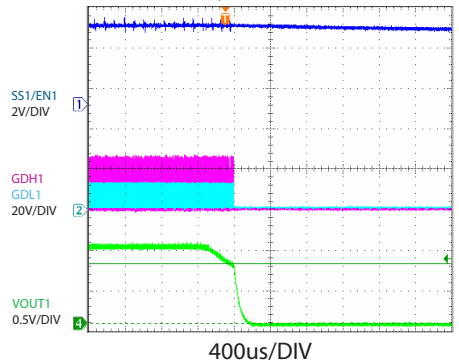
Transient Response (VOUT1_2A ~ 17A)



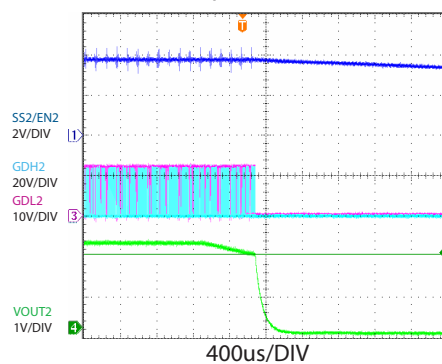
Transient Response (VOUT2_2A ~ 17A)



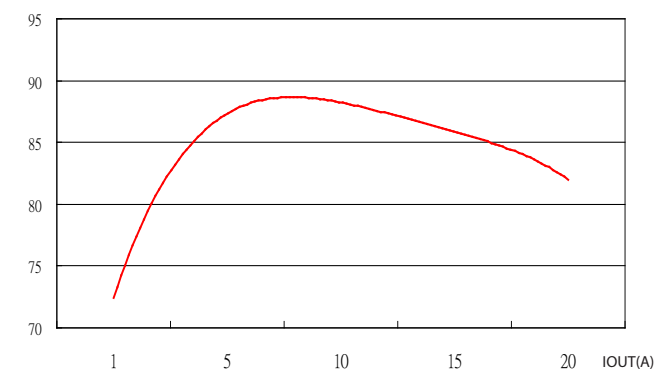
OCP Trip (VOUT1 = 30A)



OCP Trip (VOUT2 = 28A)



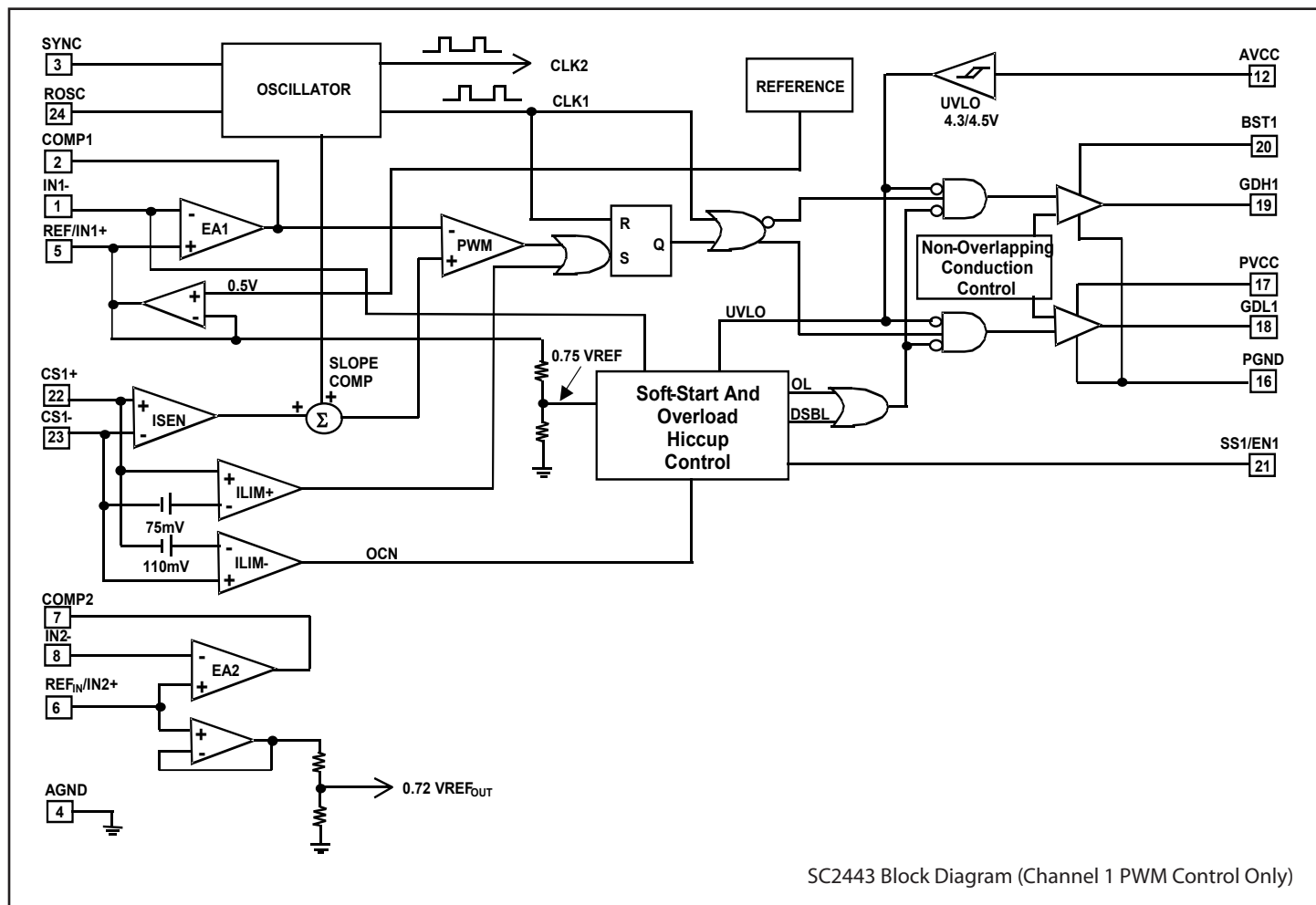
EFF (%) Combined Efficiency (12VIN to 1VOUT & 2.5VOUT)



Pin Descriptions

Pin #	Pin Name	Pin Function
1	IN1-	Inverting Input of the Error Amplifier for the Step-down Controller 1.
2	COMP1	The Error Amplifier Output for Step-down Controller 1.
3	SYNC	Edge-triggered Synchronization Input. When not synchronized, tie this pin to a voltage above 1.5V or the ground. An external clock (frequency > frequency set with ROSC) at this pin synchronizes the controllers.
4	AGND	Analog Signal Ground
5	REF	Buffered Output of the Internal 0.5V Reference. The non-inverting input of the error amplifier for the step-down converter 1 is internally connected to this pin
6	REFIN	An external Reference voltage is applied to this pin. The non-inverting input of the error amplifier for the step-down converter 2 is internally connected to this pin.
7	COMP2	The Error Amplifier Output for Step-down Controller 2.
8	IN2-	Inverting Input of the Error Amplifier for the Step-down Controller 2. Tie to AVCC for two-phase single output applications.
9	CS2-	The Inverting Input of the Current-sense Amplifier/Comparator for the Controller 2.
10	CS2+	The Non-inverting Input of the Current-sense Amplifier/Comparator for the Controller 2.
11	SS2/EN2	An external capacitor tied to this pin sets (i) the soft-start time (ii) output overload latch off time for step-down converter 2. Pulling this pin below 0.7V shuts off the gate drivers for the second controller. Leave open for two-phase single output applications.
12	AVCC	Power Supply Voltage for the Analog Portion of the Controllers.
13	BST2	Bootstrapped Supply for the High-side Gate Drive 2.
14	GDH2	Gate Drive Output for the High-side N-channel MOSFET of Output 2.
15	GDL2	Gate Drive Output for the Low-side N-channel MOSFET of Output 2.
16	PGND	Ground Supply for All the Gate drivers.
17	PVCC	Power Supply Voltage for Low-side MOSFET Drivers.
18	GDL1	Gate Drive Output for the Low-side N-channel MOSFET of Output 1.
19	GDH1	Gate Drive Output for the High-side N-channel MOSFET of Output 1.
20	BST1	Bootstrapped Supply for the High-side Gate Drive 1.
21	SS1/EN1	An external capacitor tied to this pin sets (i) the soft-start time (ii) output overload latch off time for buck converter 1. Pulling this pin below 0.7V shuts off the gate drivers for the first controller.
22	CS1+	The Non-inverting Input of the Current-sense Amplifier/Comparator for the Controller 1.
23	CS1-	The Inverting Input of the Current-sense Amplifier/Comparator for the Controller 1
24	ROSC	An external resistor connected from this pin to GND sets the oscillator frequency
	THPAD	Solder to the Analog ground plane of the PCB.

Block Diagram



SC2443 Block Diagram (Channel 1 PWM Control Only)

Figure 1. SC2443 Block Diagram

Applications Information

Description

The SC2443 is a constant frequency 2-phase current-mode step-down PWM switching controller driving all N-channel MOSFET. The two channels of the controller operate at 180 degrees out-of-phase from each other. Since input currents are interleaved in a two-phase converter, input ripple current is lower and smaller input capacitor can be used for filtering. Also, with lower inductor current and smaller inductor ripple current per phase, overall I^2R losses are reduced.

The SC2443 operates in synchronous continuous-conduction mode. It can be configured either as two independent step-down controllers producing two separate outputs or as a dual-phase single-output controller by tying the IN2- pin to VCC. In single output operation, the channel one error amplifier controls both channels and the channel two error amplifier is disabled. Soft-start and overload hiccup of both channels is synchronized to channel one.

Frequency Setting and Synchronization

The internal oscillator of the SC2443 runs at twice the phase frequency. The free-running frequency of the oscillator can be programmed with an external resistor from the ROSC pin to ground. The step-down controllers are capable of operating up to 1 MHz. It is necessary to consider the operating duty-ratio before deciding the switching frequency. See Applications Information section for more details.

When synchronized externally, the applied clock frequency should be twice the desired phase frequency. The synchronizing clock frequency should also be between 2 - 2.6 times the set free-running channel frequency.

Control Loop

The SC2443 uses peak current-mode control for fast transient response, ease of compensation and current sharing in single output operation. The low-side MOSFET of each channel is turned off at the falling-edge of the phase timing clock. After a brief non-overlapping time interval of 90ns, the high-side MOSFET is turned on. The phase inductor current ramps up. When the sensed inductor current reaches the threshold determined by the error amplifier output and compensation ramp, the high-side MOSFET is turned off. After a non-overlapping conduction time of 90ns, the low-side MOSFET is turned on.

The supply voltages for the high-side gate drivers are obtained from two diode-capacitor bootstrap circuits. If the bootstrap capacitor is charged from VCC, the high-side gate drive voltage swing will be from approximately 2VCC to the ground. The power dissipated in the high-side gate driver is not higher with higher voltage swing because the gate-source voltage of the high-side MOSFET still swing from zero to VCC. The outputs of the low-side gate drivers swing from VCC to ground.

The SC2443 has internal ramp-compensation to prevent sub-harmonic oscillation when operating above 50% duty cycle. There is enough ramp internally for a sensed voltage ripple between 1/4 to 1/3 of the full-scale sensed voltage limit of 75mV. The maximum sensed voltage limit is unaffected by the compensating ramp.

Current-Sensing

There are two ways to sense the inductor current for current-mode control with the SC2443. Since the peak inductor current corresponds to 75mV of sensed voltage ($CS+ - CS-$), resistor current sensing can be used at the output without resulting in excessive power dissipation. Although accurate and far easier to lay out than high-side resistor sensing, a pair of precision sense resistors adds cost to the converter.

With proper RC filter, Inductor DCR sensing can also be used for SC2443 resulting in low cost and without extra power dissipation.

Error Amplifiers

In closed loop operation, the error amplifier output ranges from 1.1V to 3.5V. The upper output operating range of either error amplifier is reserved for positive current-sense voltage ($CS+ - CS-$) and corresponds to positive (sourcing) output current. If the amplifier swings to its lower operating range, the amplifier will still modulate the high-side gate drive duty-ratio. However the peak current-sense voltage (hence the peak inductor current) will be limited to a negative value. The error amplifier output is about 2.2V when the peak sense-voltage is zero. The built-in offset in the current sense amplifier together with synchronous continuous-conduction mode of operation allows the SC2443 to regulate the output irrespective of the direction of the load current.

Applications Information (continued)

The non-inverting input of the first feedback amplifier is tied to the internal 0.5V voltage reference. Both the non-inverting and the inverting inputs of the second error amplifier are brought out as device pins so that the output of the second converter can be made to track the output of the first channel. For example in DDR applications, Channel 1 can be used to generate VDDQ (2.5V) from the input (5V or 12V) and channel 2 is used to produce a tracking VTT (1.25V) with VDDQ being its input.

Current-Limit

The maximum current sense voltage of +75mV is the cycle-by-cycle peak current limit when the load is drawing current from the converter. There is no cycle-by-cycle current limiting when the inductor current flows in the negative direction. However once the valley of the current sense voltage exceeds -110mV, the corresponding channel will undergo shutdown and restart (hiccup).

Soft-Start and Overload Protection

The undervoltage lockout circuit discharges the SS/EN capacitors. After VCC rises above 4.5V, the SS/EN capacitors are slowly charged by internal 2 μ A current source. With internal PNP transistors, the SS/EN voltages clamp the error amplifier outputs. When the error amplifier output rises to 2.2V, the high-side MOSFET starts to switch. As the SS/EN capacitor continues to be charged, the COMP voltage follows. The converter gradually delivers increasing power to the output. The inductor current follows the COMP voltage envelope until the output goes into regulation. The SS/EN clamp on COMP is then released.

After the SS/EN capacitor is charged above 3.2V (high enough for the error amplifier to provide full load current), the overload detection circuit is activated. If the output voltage falls below 70% of its set value or the valley current-sense voltage exceeds -110mV, an overload latch will be set and both the top and the bottom MOSFETs will be turned off. The SS/EN capacitor is slowly discharged with an internal 1.4 μ A current sink. The overload latch is reset when the SS/EN capacitor is discharged below 0.5V. The SS/EN capacitor is then recharged with the 2 μ A current source and the converter undergoes soft-start. If overload persists, the SC2443 will undergo repetitive shutdown and restart.

If the output is short-circuited, the inductor current will not increase indefinitely between the time the inductor

current reaching its current limit and the instant the converter shuts down. This is due to cycle skipping (a consequence of inductor current sense) reduces the actual operating frequency.

The SS/EN pin can also be used as the enable input for that channel. Both the high-side and the low-side MOSFETs will be turned off if the SS/EN pin is pulled below 0.7V.

Operating Frequency (fs)

The switching frequency in the SC2443 is user-programmable. The advantages of using constant frequency operation are simple passive component selection and ease of feedback compensation. Before setting the operating frequency, the following trade-offs should be considered.

- 1) Passive component size
- 2) Circuitry efficiency
- 3) EMI condition
- 4) Minimum switch on time and
- 5) Maximum duty ratio

For a given output power, the sizes of the passive components are inversely proportional to the switching frequency, whereas MOSFET and Diodes switching losses are proportional to the operating frequency. Other issues such as heat dissipation, packaging and the cost issues are also to be considered. The frequency bands for signal transmission should be avoided because of EM interference.

Minimum Switch On Time Consideration

In the SC2443 the falling edge of the clock turns on the top MOSFET. The inductor current and the sensed voltage ramp up. After the sensed voltage crosses a threshold determined by the error amplifier output, the top MOSFET is turned off. The propagation delay time from the turn-on of the controlling FET to its turn-off is the minimum switch on time. The SC2443 has a minimum on time of about 150ns at room temperature. This is the shortest on interval of the controlling FET. The controller either does not turn on the top MOSFET at all or turns it on for at least 150ns.

For a synchronous step-down converter, the operating duty cycle is VO/VIN . So the required on time for the top MOSFET is $VO/(VIN \times F_s)$. If the frequency is set such that the required pulse width is less than 150ns, then the converter will start skipping cycles. Due to minimum on time limitation, simultaneously operating at

Applications Information (continued)

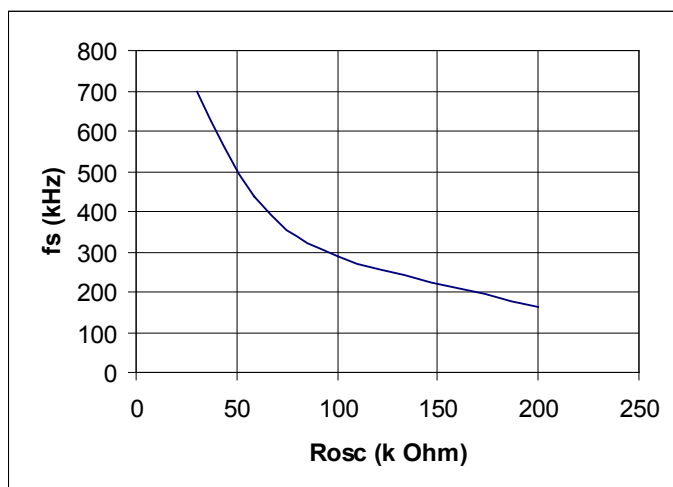
very high switching frequency and very short duty cycle is not practical. If the voltage conversion ratio VO/VIN and hence the required duty cycle is higher, the switching frequency can be increased to reduce the sizes of passive components.

There will not be enough modulation headroom if the on time is simply made equal to the minimum on time of the SC2443. For ease of control, we recommend the required pulse width to be at least 1.5 times the minimum on time.

Setting the Switching Frequency

The switching frequency is set with an external resistor connected from Pin 24 to ground. The set frequency is inversely proportional to the resistor value (Figure 2).

Figure 2. Free running frequency vs. ROSC.



Setting the Output Voltage

The non-inverting input of the channel-one error amplifier is internally tied to the 0.5V voltage reference output (Pin 5). The non-inverting input of the channel-two error amplifier is brought out as a device pin (Pin 6) to which the user can connect Pin 5 or an external voltage reference. A simple voltage divider (R_{o1} at top and R_{o2} at bottom) sets the converter output voltage. The voltage feedback gain $h=0.5/V_o$ is related to the divider resistors value as

$$R_{o2} = \frac{h}{1-h} R_{o1}.$$

PC Board Layout Issues

Circuit board layout is very important for the proper operation of high frequency switching power converters. A power ground plane is required to reduce ground bounces. The following are suggested for proper layout:

Power Stage

1) Separate the power ground from the signal ground. In the SC2443, the power ground PGND should be tied to the source terminal of lower MOSFETs. The signal ground AGND should be tied to the negative terminal of the output capacitor.

2) Minimize the size of high pulse current loop. Keep the top MOSFET, bottom MOSFET and the input capacitors within a small area with short and wide traces. In addition to the aluminum energy storage capacitors, add multi-layer ceramic (MLC) capacitors from the input to the power ground to improve high frequency bypass.

3) Reduce high frequency voltage ringing. Widen and shorten the drain and source traces of the MOSFET to reduce stray inductances. Add a small RC snubber if necessary to reduce the high frequency ringing at the phase node. Sometimes slowing down the gate drive signal also helps in reducing the high frequency ringing at the phase node.

4) Shorten the gate driver path. Integrity of the gate drive (voltage level, leading and falling edges) is important for circuit operation and efficiency. Short and wide gate drive traces reduce trace inductances. Bond wire inductance is about 2~3nH. If the length of the PCB trace from the gate driver to the MOSFET gate is 1 inch, the trace inductance will be about 25nH. If the gate drive current is 2A with 10ns rise and falling times, the voltage drops across the bond wire and the PCB trace will be 0.6V and 5V respectively. This may slow down the switching transient of the MOSFET. These inductances may also ring with the gate capacitance.

5) Put the decoupling capacitor for the gate drive power supplies (BST and PVCC) close to the IC and power ground.

Control Section

6) The frequency-setting resistor R_{osc} should be placed close to Pin 3. Trace length from this resistor to the analog

Applications Information (continued)

ground should be minimized.

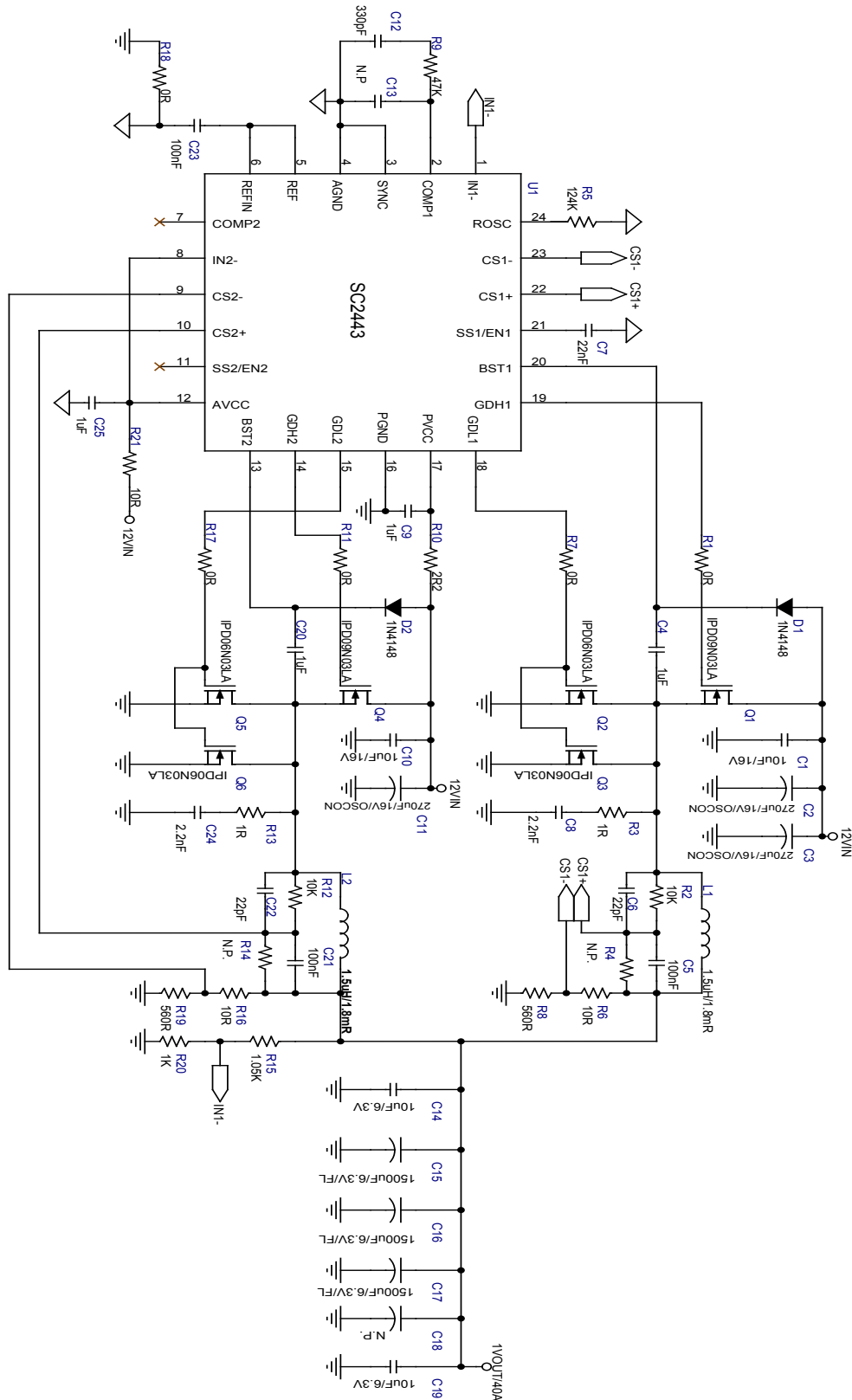
7) Solder the bias decoupling capacitor right across the AVCC and analog ground AGND.

8) Place the inductor DCR sense components away from the power circuit and close to the corresponding CS+ and CS- pins. Use X7R type ceramic capacitor for the DCR sense capacitor because of their temperature stability.

9) Use an isolated local ground plane underneath the controller and tie it to the negative side of output capacitor bank.

10) Comp pin is sensitive to noise. Place compensation network components away from noise signal (i.e. gate driver signals, phase node) and close to corresponding Comp pin .

Evaluation Application Circuit _ Single Output, Current share configuration

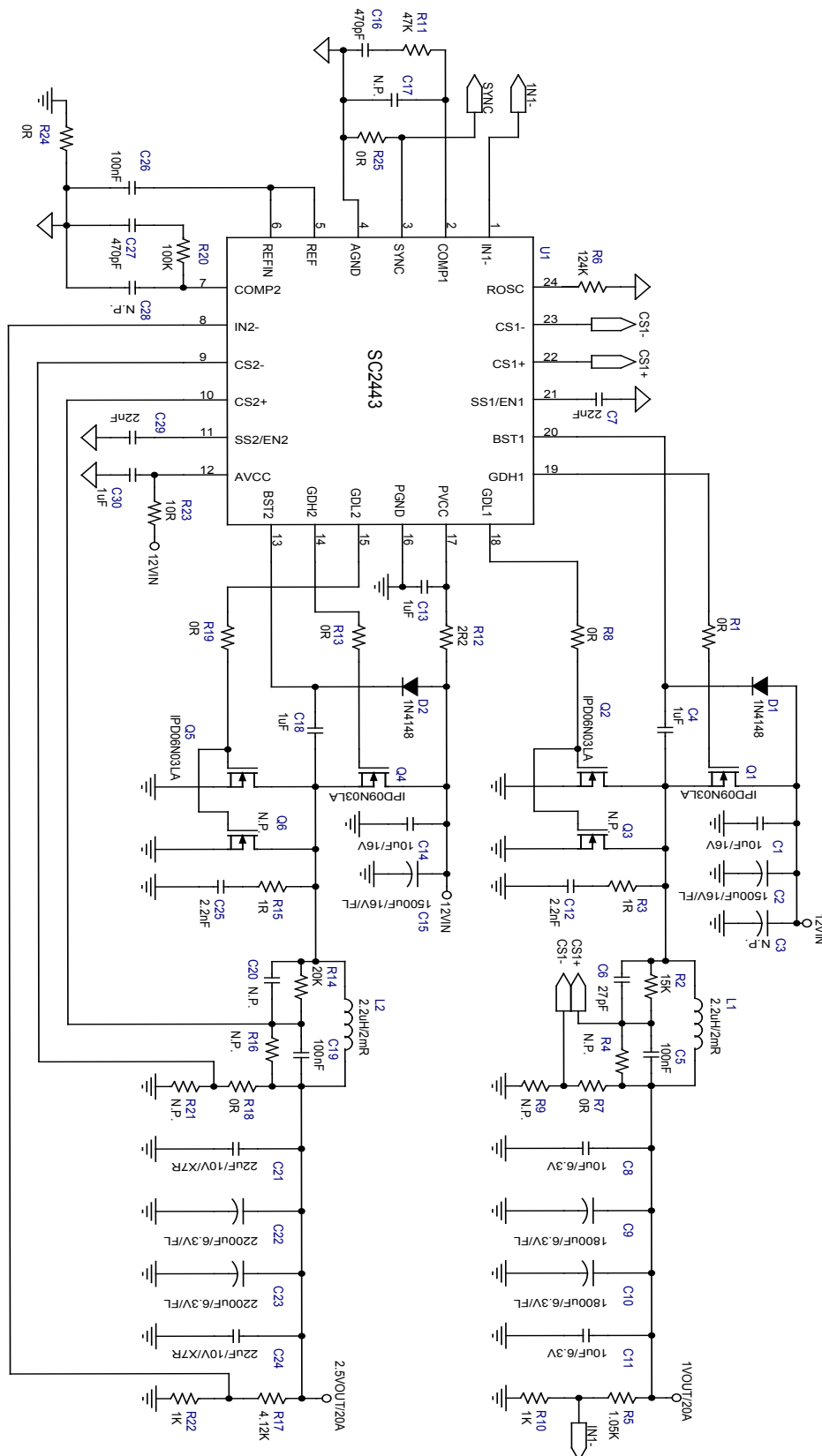


Evaluation Board Bill of Materials

Single Output Current Share Configuration

Item	Reference	Quantity	Description	Package	Part	Vendor
1	C1,C10	2	16V X5R ceramic capacitor	1206	10uF	Murata
2	C2,C3,C11	3	16V Aluminum solid capacitor _SEPC series	8 X 9mm	270uF	Sanyo
3	C4,C9,C20,C25	4	16V X5R ceramic capacitor	0603	1uF	Murata
4	C5,C21,C23	3	16V X7R ceramic capacitor	0603	100nF	Panasonic
5	C6,C22	2	25V X7R ceramic capacitor	0603	22pF	Panasonic
6	C7	1	16V X7R ceramic capacitor	0603	22nF	Panasonic
7	C8,C24	2	25V X7R ceramic capacitor	0603	2.2nF	Panasonic
8	C12	1	25V X7R ceramic capacitor	0603	330pF	Panasonic
9	C14,C19	2	6.3V X7R ceramic capacitor	1206	10uF	Murata
10	C15,C16,C17	3	6.3V Aluminum capacitor _ FL series	8 X 11.5mm	1000uF	Panasonic
11	D1,D2	2	Small signal diode	SMD	1N4148	Any
12	L1,L2	2	SMD inductor	12.5 X 12.5 X 10mm	1.5uH/1.8mR	TRIO
13	Q1,Q4	2	30V N Channel MOSFET	D-pack	IPD09N03LA	Infineon
14	Q2,Q3,Q5,Q6	4	30V N Channel MOSFET	D-pack	IPD06N03LA	Infineon
15	R1,R7,R11, R17,R18	5	5% SMD resistor	0603	0R	Any
16	R2,R12	2	5% SMD resistor	0603	10K	Any
17	R3,R13	2	5% SMD resistor	0603	1R	Any
18	R5	1	1% SMD resistor	0603	124K	Any
19	R6,R16.R21	3	1% SMD resistor	0603	10R	Any
20	R8,R19	2	1% SMD resistor	0603	560R	Any
21	R9	1	5% SMD resistor	0603	47K	Any
22	R10	1	5% SMD resistor	0603	2R2	Any
23	R15	1	1% SMD resistor	0603	1.05K	Any
24	R20	1	1% SMD resistor	0603	1K	Any
25	U1	1	Dual phase Sync. step down controller	MLPQ-24	SC2443	SEMTECH

Evaluation Application Circuit_ Dual Independent Outputs

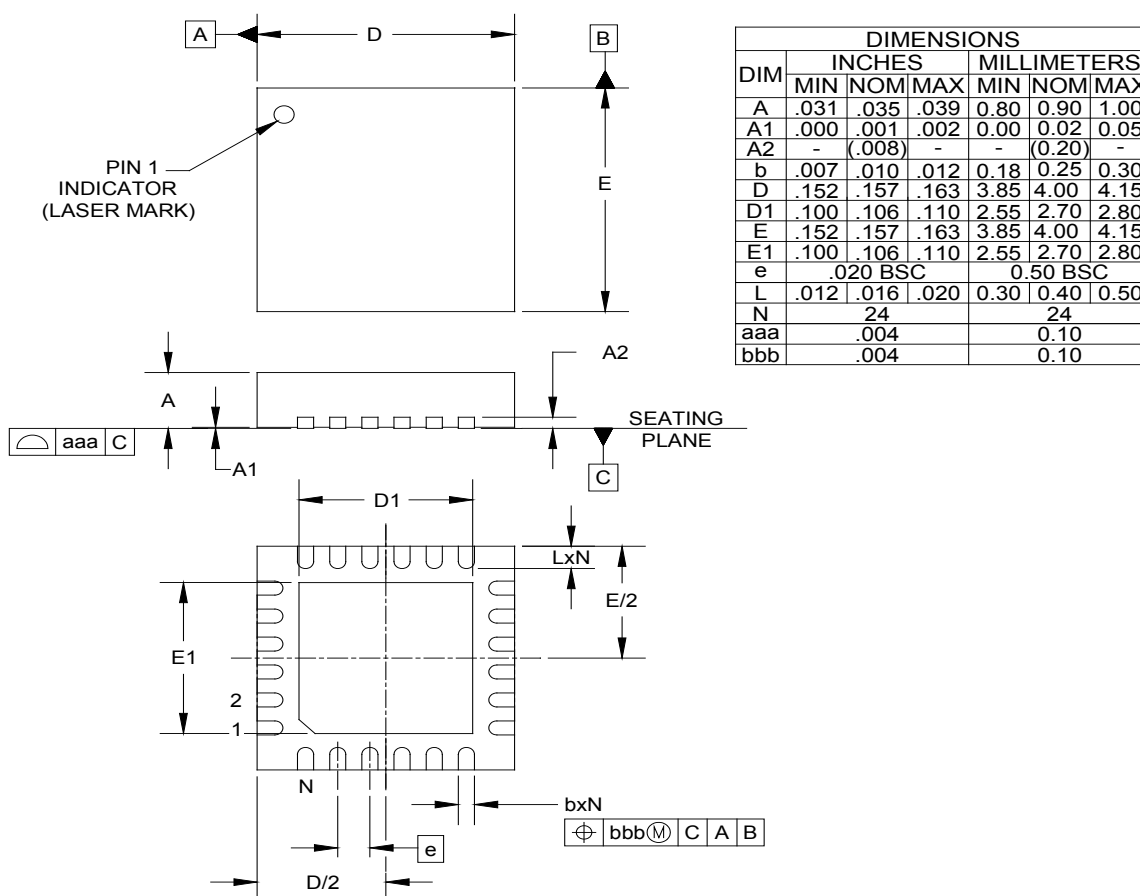


Evaluation Board Bill of Materials

Dual Independent Output Configuration

Item	Reference	Quantity	Description	Package	Part	Vendor
1	C1,C4	2	16V X5R ceramic capacitor	1206	10uF	Murata
2	C2,C15	2	16V Aluminum capacitor _FL series	10 X 20mm	1500uF	Panasonic
3	C4,C13,C18, C30	4	16V X5R ceramic capacitor	0603	1uF	Murata
4	C5,C19,C26	3	16V X7R ceramic capacitor	0603	100nF	Panasonic
5	C6	1	25V X7R ceramic capacitor	0603	27pF	Panasonic
6	C7,C29	2	16V X7R ceramic capacitor	0603	22nF	Panasonic
7	C8,C11	2	6.3V X7R ceramic capacitor	1206	10uF	Murata
8	C9,C10	2	6.3V Aluminum capacitor _FL series	10 X 16mm	1800uF	Panasonic
9	C12,C25	2	25V X7R ceramic capacitor	0603	2.2nF	Panasonic
10	C16,C27	2	25V X7R ceramic capacitor	0603	470pF	Panasonic
11	C21,C24	2	10V X7R ceramic capacitor	1206	10uF	Murata
12	C22,C23	2	6.3V Aluminum capacitor _FL series	10 X 20mm	2200uF	Panasonic
13	D1,D2	2	Small signal diode	SMD	1N4148	Any
14	L1,L2	2	Through hole inductor		2.2uH/2mR	Any
15	Q1,Q4	2	30V N Channel MOSFET	D-pack	IPD09N03LA	Infineon
16	Q2,Q5	2	30V N Channel MOSFET	D-pack	IPD06N03LA	Infineon
17	R1,R7,R11,R13, R18,R19,R24 R25	8	5% SMD resistor	0603	0R	Any
18	R2	1	5% SMD resistor	0603	15K	Any
19	R3,R15	2	5% SMD resistor	0603	1R	Any
20	R5	1	1% SMD resistor	0603	1.05K	Any
21	R6	1	1% SMD resistor	0603	124K	Any
22	R10,R22	2	1% SMD resistor	0603	1K	Any
23	R11	1	5% SMD resistor	0603	47K	Any
24	R12	1	5% SMD resistor	0603	2R2	Any
25	R14	1	5% SMD resistor	0603	20K	Any
26	R17	1	1% SMD resistor	0603	4.12K	Any
27	R20	1	5% SMD resistor	0603	100K	Any
28	R23	1	5% SMD resistor	0603	10R	Any
29	U1	1	Dual phase Sync. step down controller	MLPQ-24	SC2443	SEMTECH

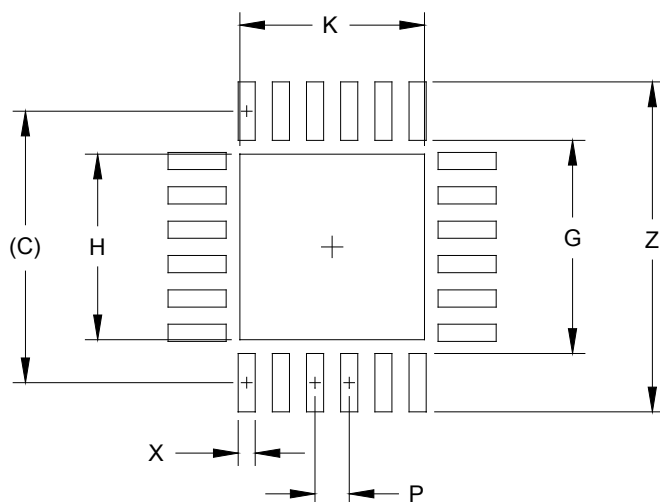
Outline Drawing - MLPQ-24



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

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Land Pattern - MLPQ-24


DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.156)	(3.95)
G	.122	3.10
H	.106	2.70
K	.106	2.70
P	.020	0.50
X	.010	0.25
Y	.033	0.85
Z	.189	4.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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