SC2441A

1.8V to 20V Input 2-Phase Synchronous Step-down Controllers with Step-up Converter

POWER MANAGEMENT

Description

The SC2441A is a programmable frequency dual independent or dual/multiple phase single output peak current-mode step-down switching regulator controller. It is capable of operating from 1.8V to 20V input. A 0.6A step-up converter in the SC2441A generates an auxiliary gate drive supply when VIN is below 4.5V. This makes the SC2441A well suited for applications where a low-voltage input (<3.3V) is to be stepped down for lower voltage logic, yet the input is too low to drive power MOSFETs efficiently.

The SC2441A employs a phase-locked synchronizing circuit that allows the step-up converter to operate at twice the switching frequency of the step-down controllers for miniaturization. The clock output signal enables two or more SC2441As to be daisy chained with programmable phase shift.

Tying the FB2 pin to VIN makes the second step-down channel a slave of the first. Operating in this mode, the SC2441A regulates a single output with shared current in each channel. Each step-down controller has its own soft-start and overload shutdown timer for hiccup overload protection. In the single-output mode, the channel 1 timer controls the soft-start and overload hiccup of both controllers.

Features

2-Phase Synchronous Step-down Controllers

- 2-Phase Synchronous Continuous Conduction Mode
- Out of Phase Operation for Low Input Current Ripple
- Operates up to 1MHz Per Channel
- Excellent Current Sharing Between Phases
- Duty Cycle Up to 90%
- 0.5V Feedback voltages for Low-Voltage Outputs
- Starts into Pre-biased Outputs
- Adaptive Shoot-through Protection
- Lossless Inductor DCR Current Sensing
- 23mV Current-limit Threshold
- Individual Soft-start, Overload Hiccup and Enable

Step-up Regulator

- 0.27V V_{CESAT} Switch at 0.6A
- Fixed frequency Current-mode Control

Common Features

- Wide input Voltage Range: 1.8V to 20V
- Synchronizing Frequency Equal to that of the Step-down Converters
- 28-lead TSSOP-EDP Lead-free package, fully WEEE and RoHS compliant

Applications

- Low voltage distributed DC-DC converters
- Telecommunication power supplies
- Servers and base stations

Typical Application Circuit

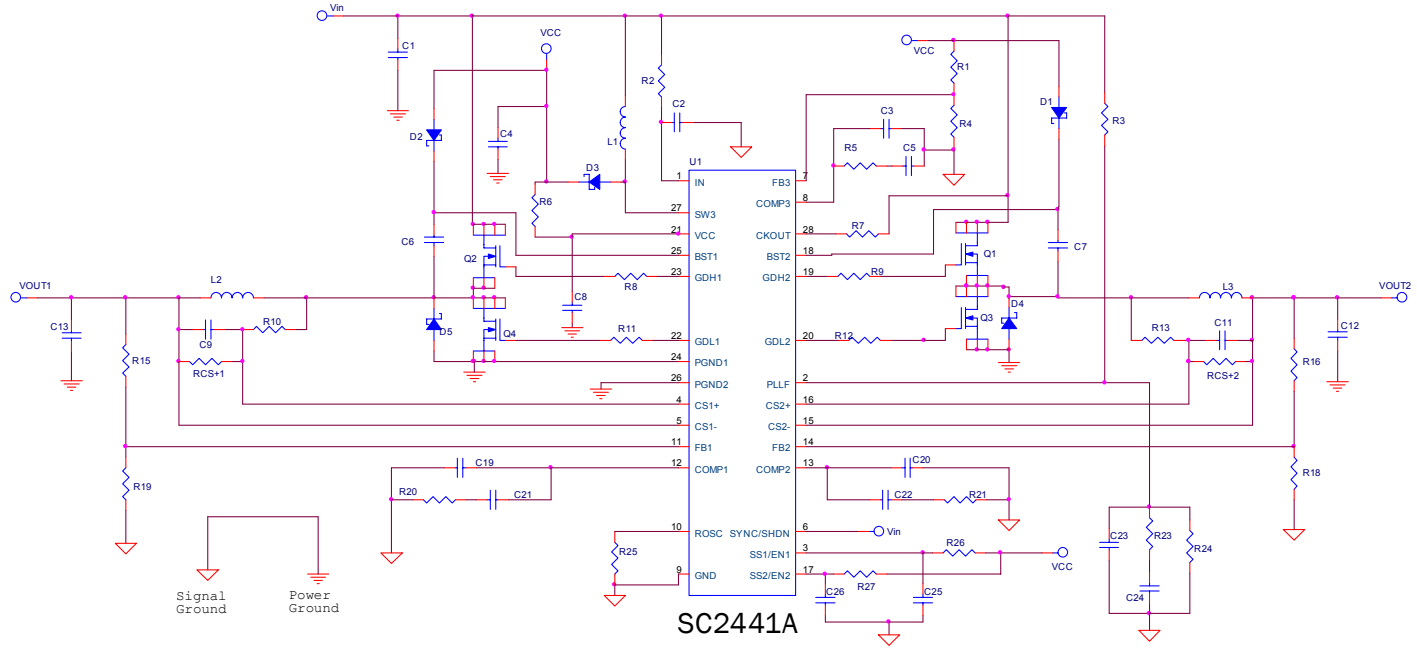


Figure 1

Absolute Maximum Rating

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum Ratings	Units
Input Voltage	V_{IN}	-0.3 to 20	V
Supply Voltage For Step-Down Controller	V_{CC}	-0.3 to 20	V
High-Side Driver Supply Voltages	V_{BST1}, V_{BST2}	-0.3 to 28	V
FB1, FB2 Voltage	V_{FB1}, V_{FB2}	-0.3 to 20	V
COMP1, COMP2 Voltages	V_{COMP1}, V_{COMP2}	-0.3 to 4.5	V
CS1(+), CS1(-), CS2(+) and CS2(-) Voltages	$V_{CS1(+)}$, $V_{CS1(-)}$, $V_{CS2(+)}$, $V_{CS2(-)}$	-0.3 to V_{CC}	V
SYNC/$\overline{SHDN}$ Voltage	$V_{S/S}$	-0.3 to V_{IN}+1	V
ROSC Voltage	V_{ROSC}	-0.3 to 2	V
SS1/EN1 AND SS2/EN2 Voltages	V_{SS1}, V_{SS2}	-0.3 to 4	V
FB3 Voltage	V_{FB3}	4	V
SW3 Voltage	V_{SW3}	-0.3 to 30	V
Maximum Junction Temperature	T_J	150	°C
Thermal Resistance Junction to Case	θ_{JC}	2	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	37	°C/W
Storage Temperature Range	T_{STG}	-60 to 150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	300	°C
ESD Ratings (Human Body Model)	ESD	2000	V

Electrical Characteristics

Unless specified: V_{IN} = 2V, V_{CC} = V_{BST1} = V_{BST2} =8V, SYNC/$\overline{SHDN}$ =2V, ROSC = 51.1kΩ, -40°C < T_A = T_J < 105°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Undervoltage Lockout						
V_{CC} Start Threshold	V_{CCTH}	V_{CC} Increasing		4.45	4.55	V
V_{CC} UVLO Hysteresis	V_{CCTL}	V_{CC} Decreasing		150		mV
V_{CC} Input Current	I_{CC}	V_{CC} = 8V, $V_{S/S}$ = 2V V_{CC} = 4V, V_{CCTL}, $V_{S/S}$ = 2V V_{CC} = 8V, $V_{S/S}$ = 0V (2)		10 0.05 8	15 1.0 11	mA
Channel 1 and 2 Error Amplifiers						
Feedback Voltage	V_{FB1}, V_{FB2}	V_{IN} = 3V, 5V < V_{CC} < 10V	0.494	0.500	0.506	V
		V_{IN} = 3V, 5V < V_{CC} < 10V, -40°C to 85°C	0.495	0.500	0.505	V
Feedback Pin Input Bias Current	I_{FB1}			-60	-200	nA
	I_{FB2}			-280	-500	nA
Amplifier Transconductance	G_{M1}, G_{M2}			315		$\mu\Omega^{-1}$
Open Loop Voltage Gain	a_{o1}, a_{o2}			75		dB
Amplifier Unity Gain Bandwidth		(Note 1)		5		MHz
Amplifier Output Sink Current		$V_{FB1,2}$ = 1V, $V_{COMP1,2}$ = 2.5V	19	24	29	µA
Amplifier Output Source Current		$V_{FB1,2}$ = 0V, $V_{COMP1,2}$ = 2.5V	9	13	16	µA

Electrical Characteristics (Cont.)

Unless specified: V_{IN} = 2V, V_{CC} = V_{BST1} = V_{BST2} =8V, SYNC/$\overline{SHDN}$ =2V, ROSC = 51.1kΩ, -40°C < T_A = T_J < 105°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
COMP Threshold for PWM Operation		$V_{CS1(+)} = V_{CS1(-)} = 0$ $V_{CS2(+)} = V_{CS2(-)} = 0$	1.67	1.85	2.05	V
FB2 Voltage For 2-Phase Single Output Mode of Operation			1.55			V
Oscillator and Phase-Locked Loop						
Free Running Frequency	f_{CCO}	T_J = 25°C; V_{PLLF} > 1V	450	500	550	KHz
Minimum Locking Frequency		V_{PLLF} open		240		KHz
Free Running Frequency / Minimum Locking Frequency		T_J = 25°C	1.7	2.0		
Charge Pump Output Current	I_{PLLF}	V_{PLLF}=1V	10	15	20	µA
Maximum Duty Cycle	D_{MAX1}, D_{MAX2}		88	90		%
Minimum Duty Cycle	D_{MIN1}, D_{MIN2}				0	%
SYNC/$\overline{SHDN}$ Input High Voltage	$V_{S/SH}$		1.5			V
SYNC/$\overline{SHDN}$ Input Low Voltage	$V_{S/SL}$				0.5	V
SYNC/$\overline{SHDN}$ Input Current	$I_{S/S}$	$V_{S/S}$ = 0.2V $V_{S/S}$ = 2V		 40	1 60	µA
Shutdown Delay		(Note 1)		85		µs
Clock Output High Voltage	$CKOUT_H$	I_{CKOUT} = -80µA	1.6	1.8		V
Clock Output Low Voltage	$CKOUT_L$	I_{CKOUT} = 200µA			0.4	V
Current-Sense Amplifiers, PWM and Current-Limit Comparators						
Input Common Mode Range			0		V_{CC} - 1	V
Current Limit Threshold	V_{ILIM1}, V_{ILIM2}	V_{CC} = 8V $V_{CS1(-)} = V_{CS2(-)}$ = 0V	18	23	28	mV
Current Limit Threshold	V_{ILIM1}, V_{ILIM2}	V_{CC} = 8V $V_{CS1(-)} = V_{CS2(-)}$ = 5V	18	23	28	mV
Positive Current-Sense Input Bias Current	$I_{CS1(+)}$, $I_{CS2(+)}$	$V_{CS1(+)} = V_{CS1(-)} = 0$ $V_{CS2(-)} = V_{CS2(-)} = 0$		-0.4	-0.8	µA
Negative Current-Sense Input Bias Current	$I_{CS1(-)}$, $I_{CS2(-)}$	$V_{CS1(+)} = V_{CS1(-)} = 0$ $V_{CS2(+)} = V_{CS2(-)} = 0$		-40	-75	µA
Minimum PWM On-time		T_A = 25°C, (Note 1)		180		ns
Gate Drivers						
High-Side Gate Drive Peak Source Current		(Note 1)		2		A
High-Side Gate Drive Peak Sink Current		(Note 1)		2		A
Low-Side Gate Drive Peak Source Current		(Note 1)		2		A

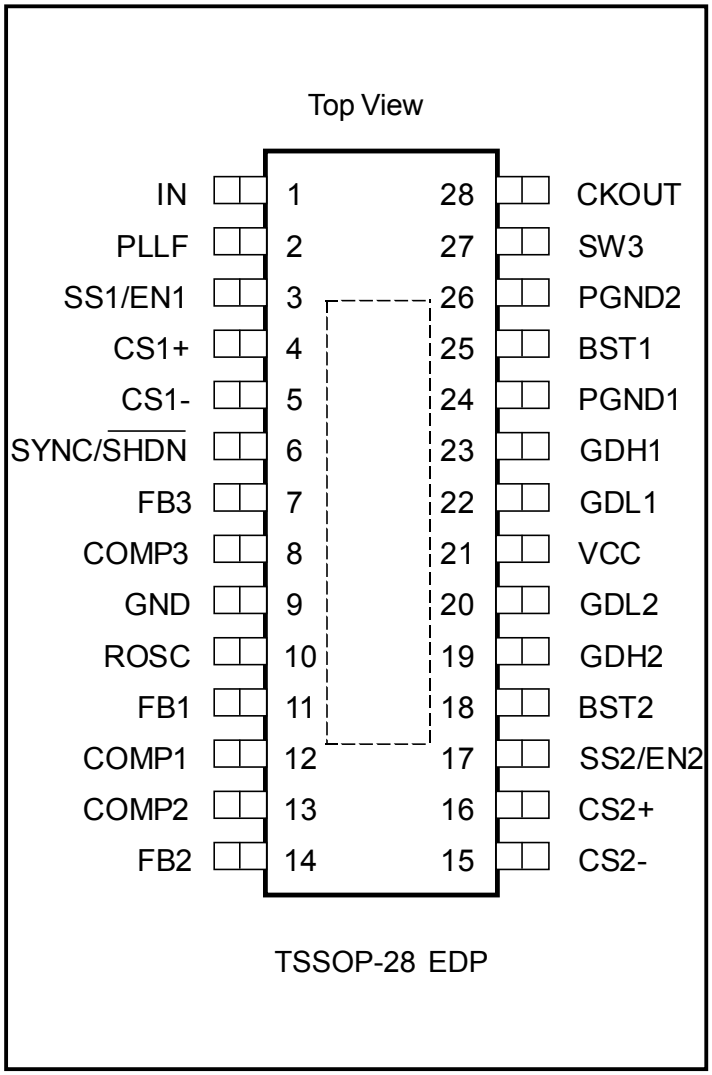
Electrical Characteristics (Cont.)

Unless specified: V_{IN} = 2V, V_{CC} = V_{BST1} = V_{BST2} =8V, SYNC/$\overline{SHDN}$ =2V, ROSC = 51.1kΩ, -40°C < T_A = T_J < 105°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Low-Side Gate Drive Peak Sink Current		(Note 1)		2		A
Gate Drive Rise Time		C_L = 3300pF		30		ns
Gate Drive Fall Time		C_L = 3300pF		30		ns
Soft-Start, Overload Shutoff and Enable						
Soft-Start Voltage to Enable Overload Hiccup	V_{SSEN1}, V_{SSEN2}	V_{SS1} and V_{SS2} Increasing		3.3		V
Overload Hiccup FB Threshold	V_{FBOL1}, V_{FBOL2}	$V_{SS1, 2}$ = 3.5V FB_1 and FB_2 Decreasing	0.35	0.38	0.41	V
Soft-Start Discharge Current	$I_{SS1(DIS)}$, $I_{SS2(DIS)}$	V_{FB1} = V_{FB2} = 0.3V V_{SS1} = V_{SS2} = 3V	6	9	12	µA
Soft-Start Voltage to Restart After Overload Shutdown	V_{SSRST1}, V_{SSRST2}	V_{SS1} and V_{SS2} Decreasing		0.5		V
Channel Disable SS/EN Voltage					0.6	V
SS/EN Threshold for PWM Operation		$V_{CS1(+)}$ = $V_{CS1(-)}$ = 0 $V_{CS2(+)}$ = $V_{CS2(-)}$ = 0	1.23	1.28	1.33	V
Boost Converter						
V_{IN} Start Threshold	V_{INTH}	V_{IN} Increasing		1.73	1.76	V
V_{IN} Hysteresis	V_{INTL}			100		mV
Feedback Pin Bias Current	I_{FB3}			40	250	nA
Feedback Voltage	V_{FB3}	1.8V < V_{IN} < 16.5V	1.225	1.250	1.275	V
Feedback Amplifier Transconductance	G_{M3}			70		$\mu\Omega^{-1}$
Feedback Amplifier Open-Loop Gain	a_{o3}			50		dB
Boost Converter Switching Frequency	f_{OSC3}			1		MHz
Maximum Switch Duty Cycle	D_{MAX3}		85	92		%
Boost Converter Switch Saturation Voltage	V_{CESAT}	I_{SW} = 0.6A		0.27		V
Boost Switch Leakage Current	$I_{LEAKAGE}$	V_{SW} = 12V			5	µA
Boost Switch Current Limit	I_{LIMIT}		0.6	0.8		A
Thermal Shutdown				155		°C
Thermal Shutdown Hysteresis				10		°C

Notes:
(1) Guaranteed by design not tested in production.
(2) Input current is dominated by the equivalent gate drive current to external MOSFETs in active switching condition.

Pin Configurations



Ordering Information

Device	Package	Temperature Range (T_A)
SC2441ATETRT(1,2)	TSSOP-28-EDP	-40 to 85°C
SC2441AEVB	Evaluation Board	

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices for the TSSOP-28-EDP package.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin	Pin Name	Pin Function
1	IN	Supply Voltage for the Boost Converter. Tie to VCC if boost converter is not used to generate auxiliary supply.
2	PLLF	Compensation Pin for the Phase Lock Loop.
3	SS1/EN1	An external resistor and an external capacitor tied to this pin set the first step-down converter soft-start time and its overload hiccup cycle time. Pulling this pin below 0.6V shuts off channel 1 gate drivers.
4	CS1+	The Non-inverting Input to the Channel 1 Current-sense Amplifier/Comparator.
5	CS1-	The Inverting Input to the Channel 1 Current-sense Amplifier/Comparator. Normally tied to the output of the converter.
6	SYNC/$\overline{\text{SHDN}}$	Synchronization and Shutdown Input. Tie this pin to IN (Pin 1) or to a voltage above 1.5V to enable the SC2441A. Pulling this pin below 0.5V shuts off both step-down controllers and the boost regulator. Driving this pin with an external clock synchronizes the SC2441A. The boost converter runs at twice of the external clock frequency whereas the step-down controllers operate at the clock frequency.
7	FB3	The Inverting Input to Boost Error Amplifier. FB3 is tied to an external resistive divider for OUT3 voltage setting.
8	COMP3	Boost Converter Error Amplifier Output. Used for loop compensation. Pulling this pin below 0.4V disables the step-up converter.
9	GND	Analog Ground.
10	ROSC	An external resistor connected from this pin to GND sets the oscillator free-running frequency.
11	FB1	The Inverting Input to the Channel 1 Error Amplifier. Tie to an external resistive divider between OUT1 and the ground for output voltage sensing.
12	COMP1	Channel 1 Error Amplifier Output. Used for loop compensation.
13	COMP2	Channel 2 Error Amplifier Output. Used for loop compensation.
14	FB2	The Inverting Input to the Channel 2 Error Amplifier. Tie to an external resistive divider between OUT2 and the ground for output voltage sensing. Tie to IN or VCC for two-phase single output operation.
15	CS2-	The Inverting Input to the Channel 2 Current-sense Amplifier/Comparator. Normally tied to the output of the converter.
16	CS2+	The Non-inverting Input to the Channel 1 Current-sense Amplifier/Comparator.
17	SS2/EN2	An external resistor and an external capacitor tied to this pin set the second step-down converter soft-start time and its overload hiccup cycle time. Pulling this pin below 0.6V shuts off channel 2 gate drivers. Leave open for two-phase single output operation.
18	BST2	Bootstrapped Supply for Channel 2 Upper Gate Drive. Connect to a bootstrap capacitor and an external diode.
19	GDH2	Gate Drive Output for Channel 2 Upper MOSFET. Gate drive voltage swings from ground to VBST2.

Pin Descriptions (Cont.)

20	GDL2	Gate Drive Output for Channel 2 Synchronous MOSFET. Gate drive voltage swings from ground to VCC.
21	VCC	Supply Voltage for Both Step-down Controllers and the Synchronous MOSFET Gate Drivers. The boost converter generates VCC if VIN is not high enough to fully enhance the power MOSFETs and the boost converter provides an auxiliary supply voltage for the step-down controllers. Tie VCC to VIN if the boost converter is not needed.
22	GDL1	Gate Drive Output for Channel 1 Synchronous MOSFET. Gate drive voltage swings from ground to VCC.
23	GDH1	Gate Drive Output for Channel 1 Upper MOSFET. Gate drive voltage swings from ground to VBST1.
24	PGND1	Power Ground Return of the Gate Drivers.
25	BST1	Bootstrapped Supply for Channel 1 Upper Gate Drive. Connect to a bootstrap capacitor and an external diode.
26	PGND2	Boost Switch Emitter.
27	SW3	Boost Switch Collector. Connect to a boost inductor and freewheeling diode.
28	CKOUT	Clock output. See timing diagram in Figure 5(b).
	Exposed PAD	Must be properly soldered to the signal ground plane to enhance thermal conduction.

Block Diagram

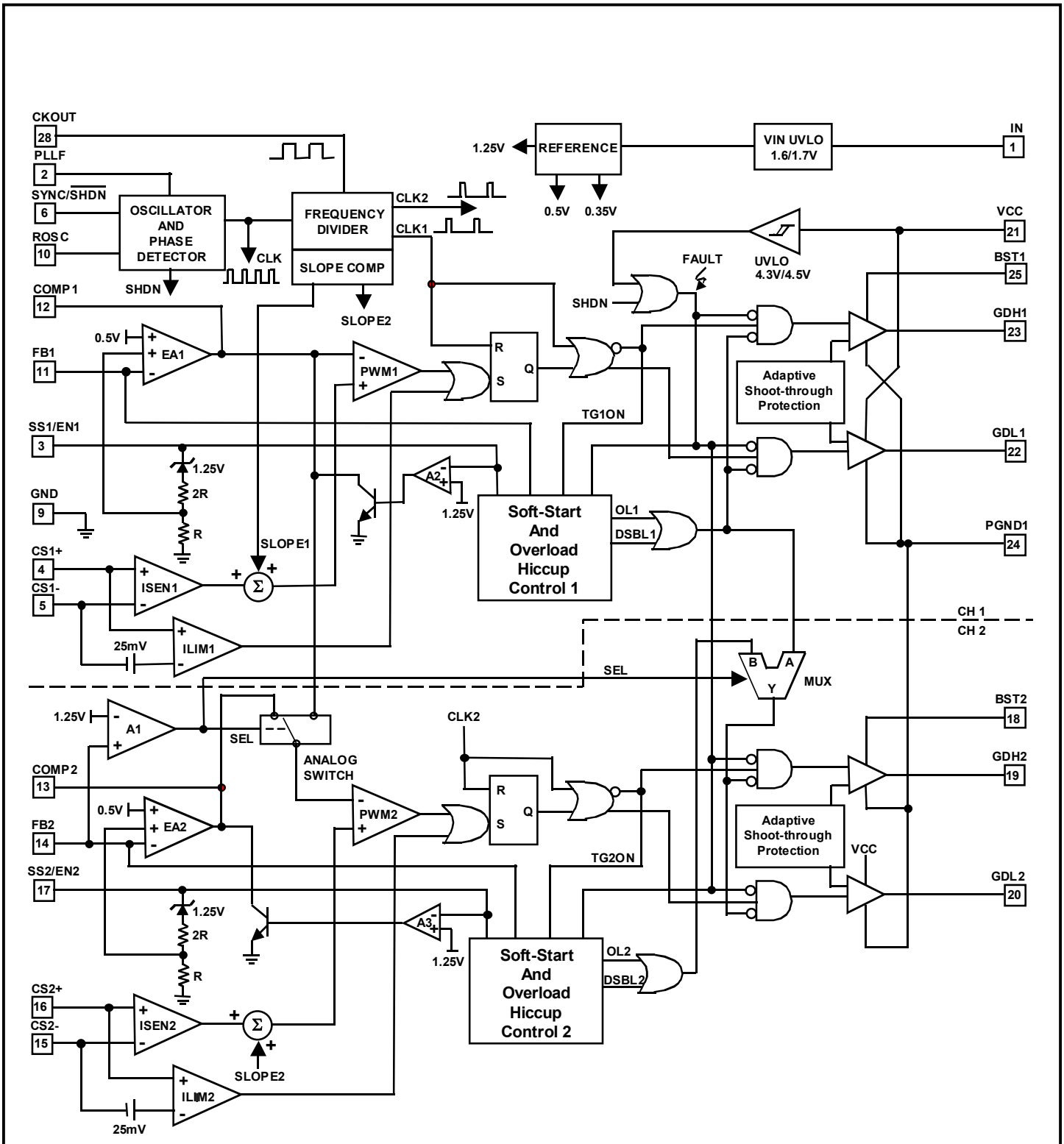


Figure 2 Functional Diagram of the Step-down Controllers

Block Diagram

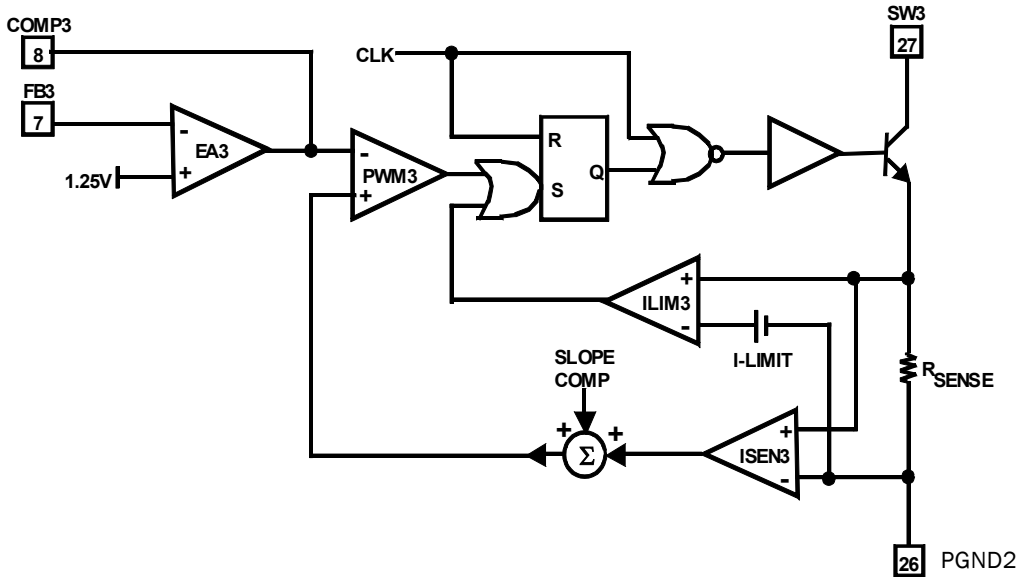


Figure 3. Step-up Converter Functional Diagram

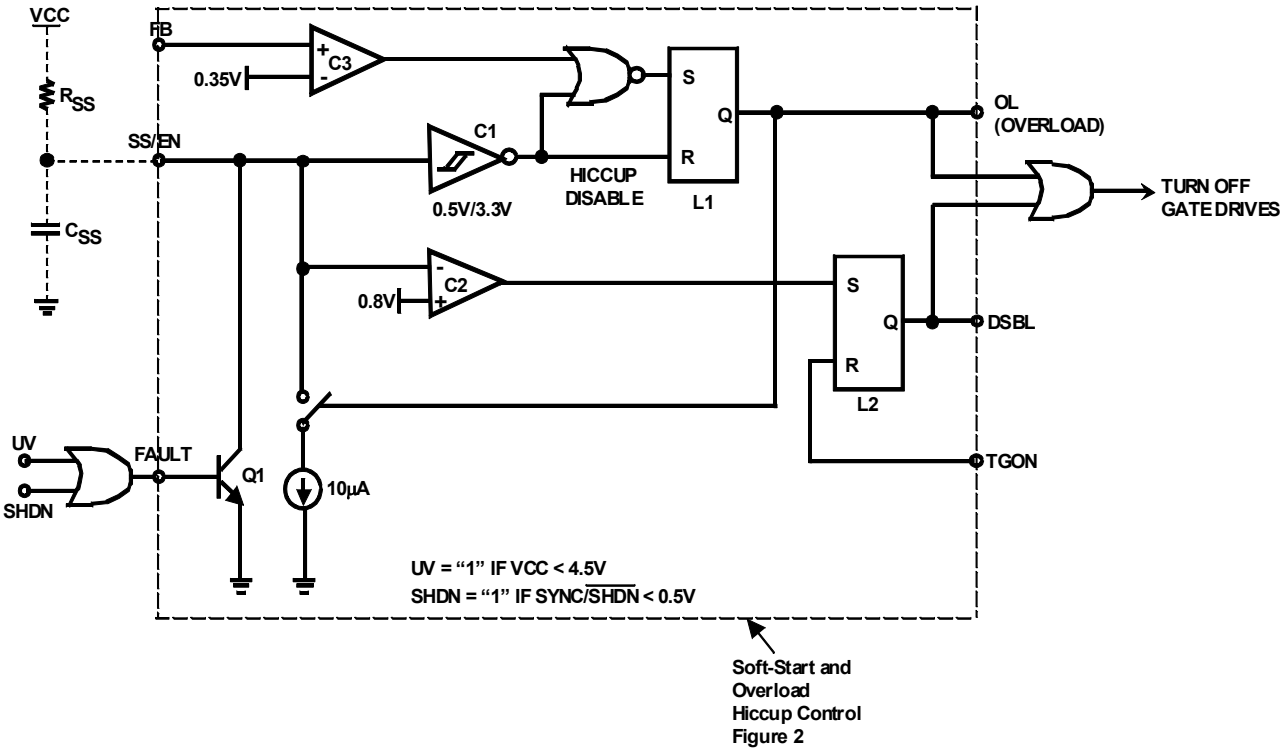
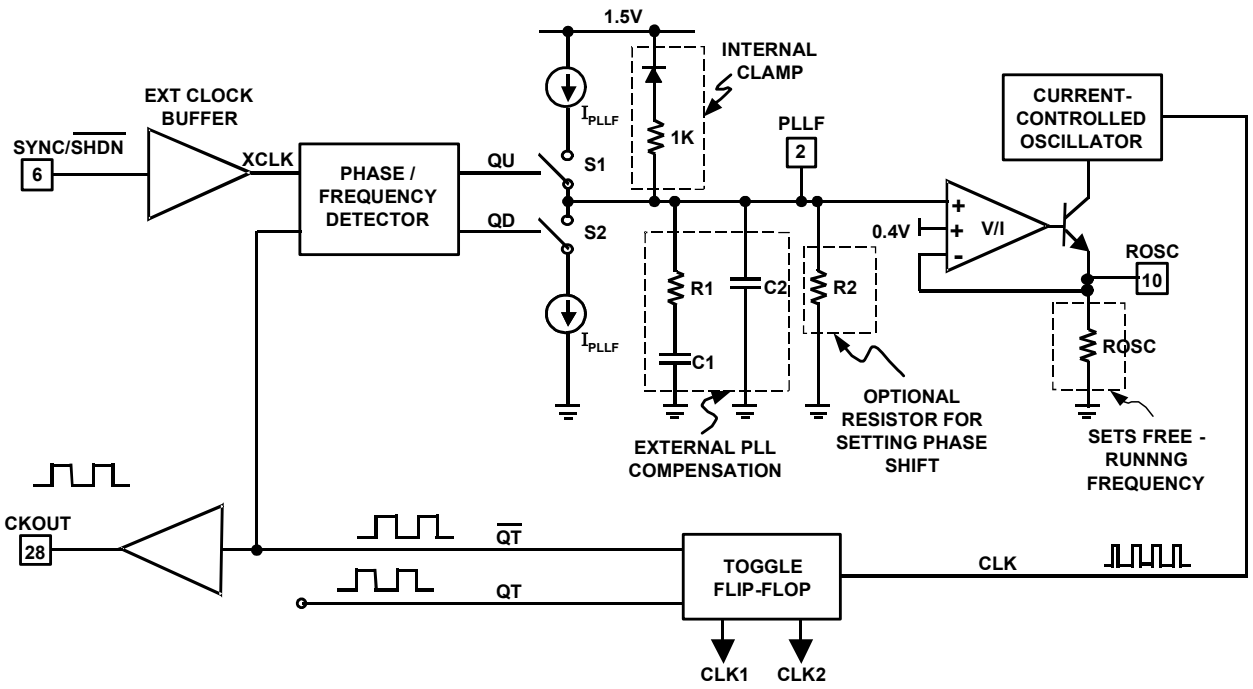
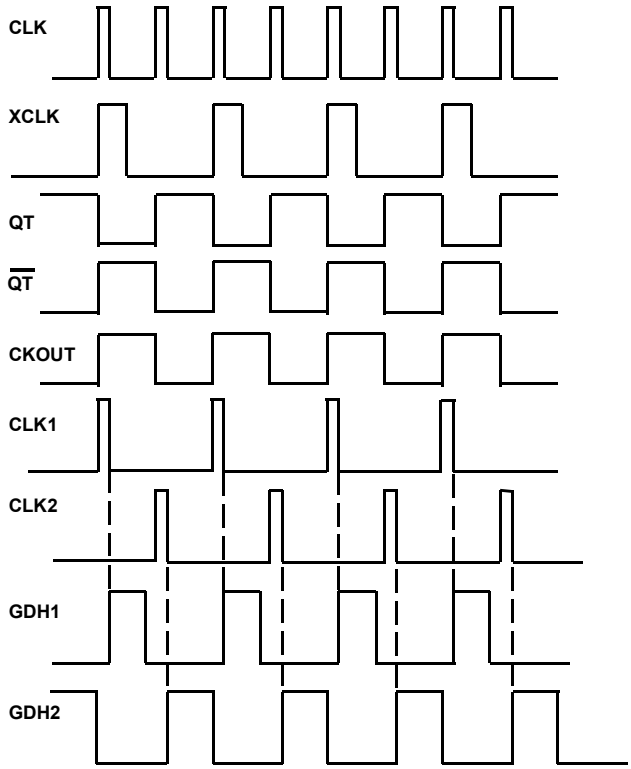


Figure 4 Details of Soft-Start and Overload Hiccup Control Circuit

Block Diagram



(a)



(b)

Figure 5. Phase-Locked Loop (a) and Its Timing Diagram in Locked Condition (R_2 not Used) (b).

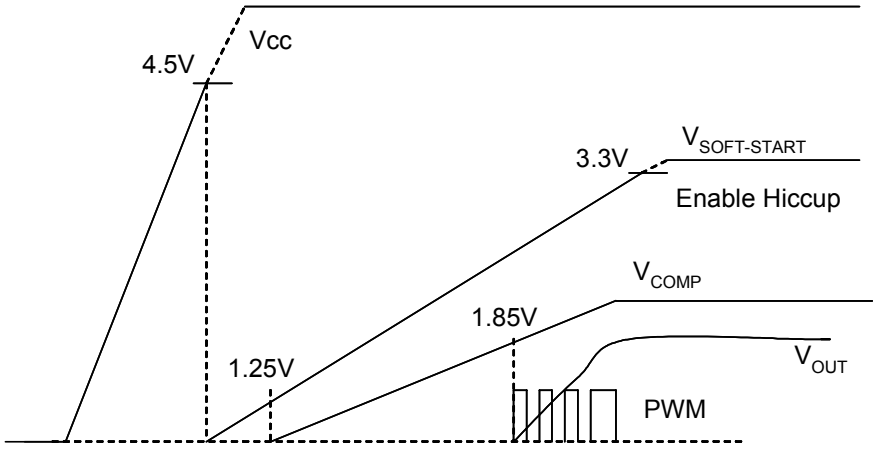


Figure 6a. SC2441A Start-up Timing Diagram

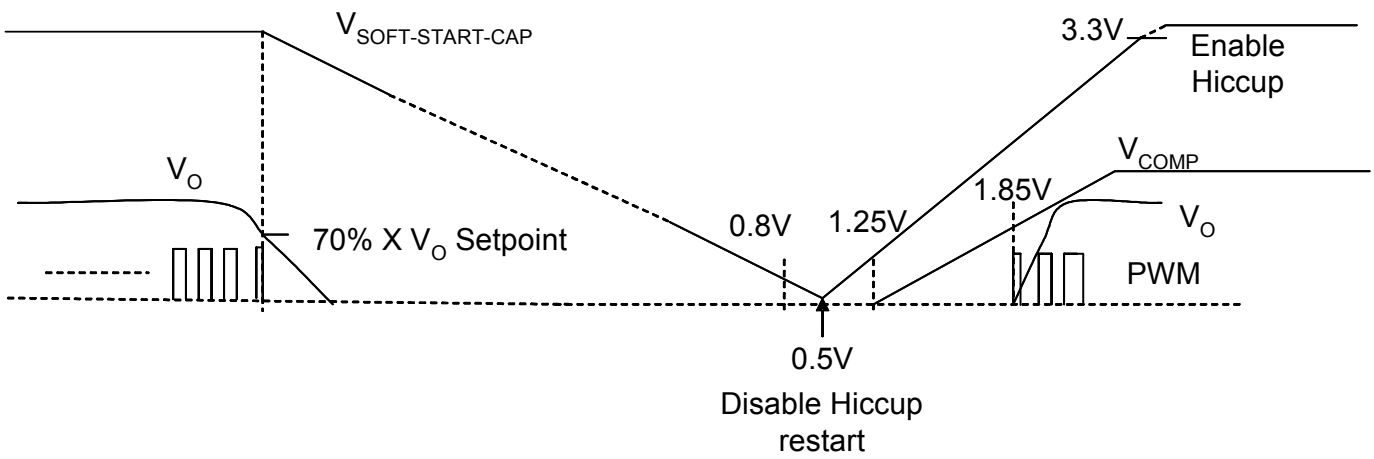
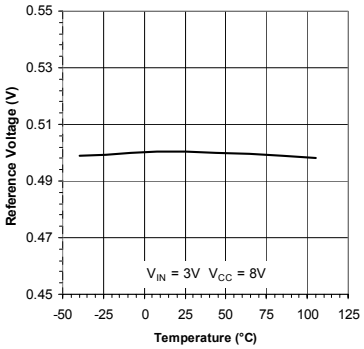


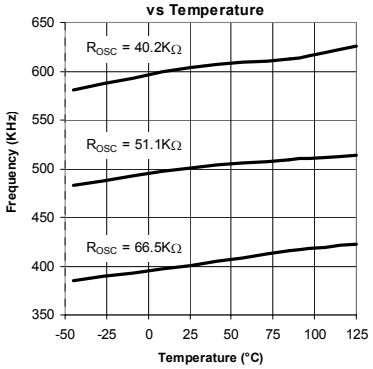
Figure 6b. SC2441A Overload Hiccup Operation Timing Diagram

Typical Characteristics

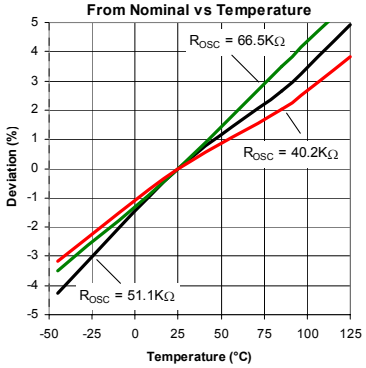
Step-down Channel Feedback vs Temperature



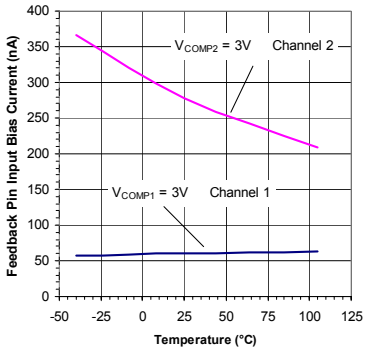
Step-down Channel Switching Frequency vs Temperature



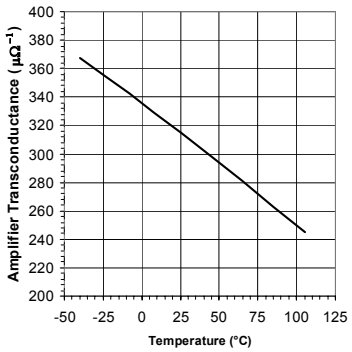
Percenatge Frequency Deviation From Nominal vs Temperature



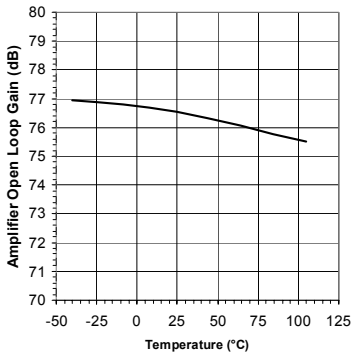
Feedback Pin Input Bias Current vs Temperature



Amplifier Transconductance vs Temperature

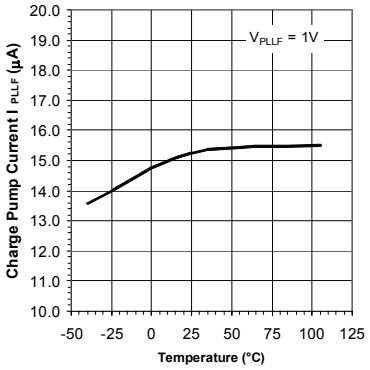


Amplifier Open Loop Gain vs Temperature

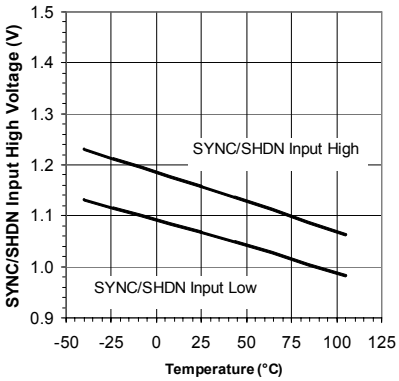


Typical Characteristics

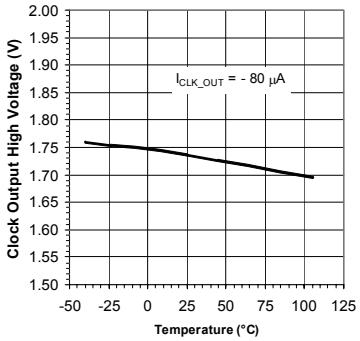
Charge Pump Current I_{PLLF} vs Temperature



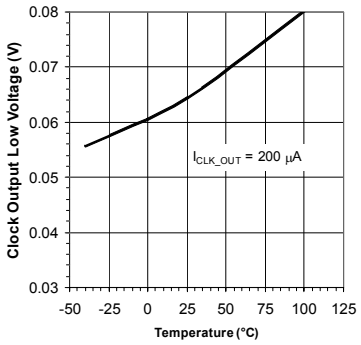
SYNC/SHDN Input Voltage vs Temperature



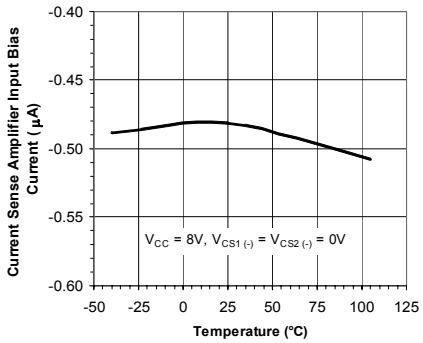
Clock Output High Voltage vs Temperature



Clock Output Low Voltage vs Temperature

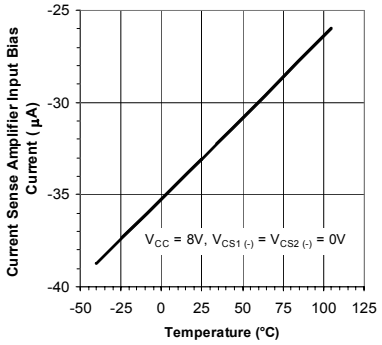


Current Sense Amplifier Input Bias Current vs Temperature (Non-inverting Pin)

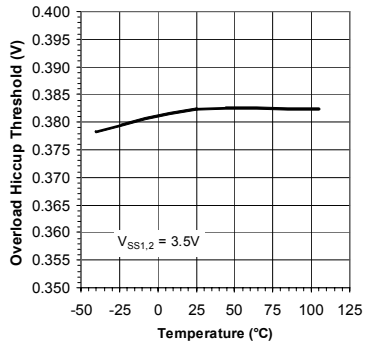


Typical Characteristics

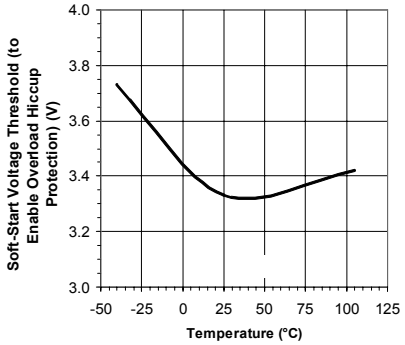
Current Sense Amplifier Input Bias Current vs Temperature (Inverting Pin)



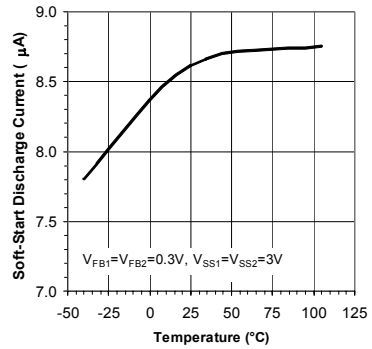
Overload Hiccup Threshold vs Temperature



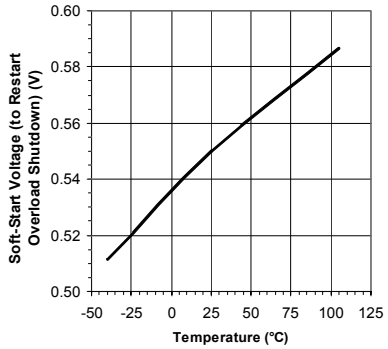
Soft-Start Voltage Threshold (to Enable Overload Hiccup Protection) vs Temperature



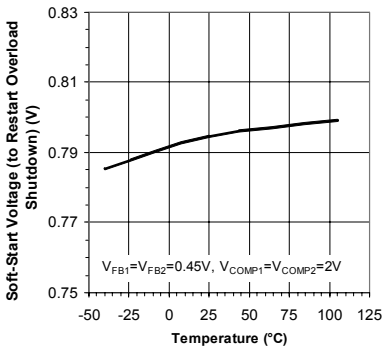
Soft-Start Discharge Current vs Temperature



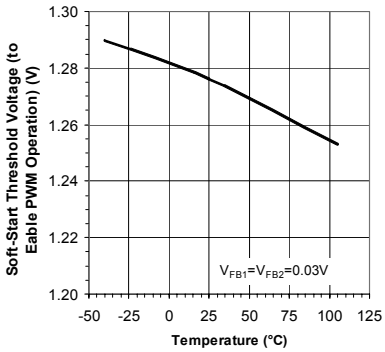
Soft-Start Voltage (to Restart Overload Shutdown) vs Temperature



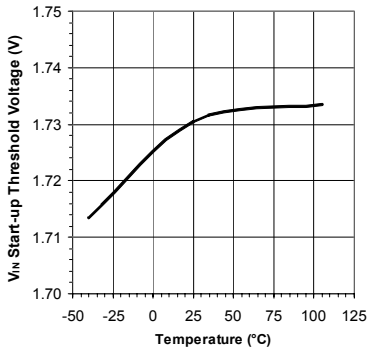
Soft-Start Disable Voltage vs Temperature



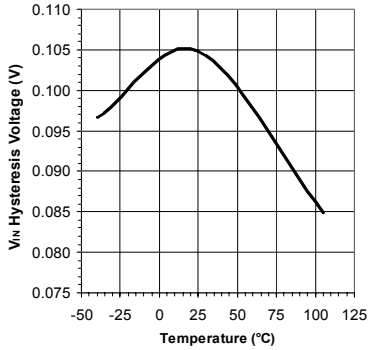
Soft-Start Threshold Voltage (to Eable PWM Operation) vs Temperature



V_{IN} Start-up Threshold Voltage vs Temperature

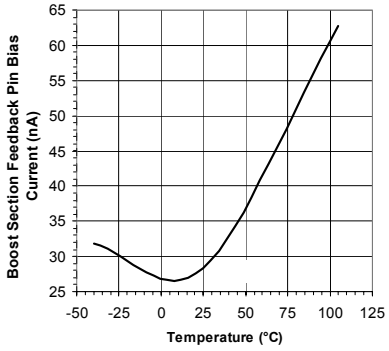


V_{IN} Hysteresis Voltage vs Temperature

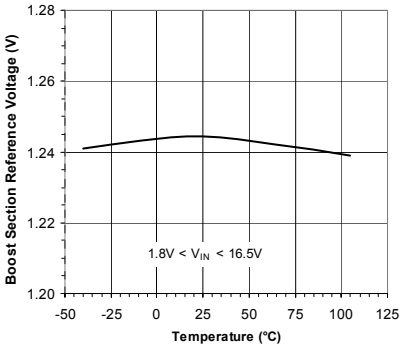


Typical Characteristics

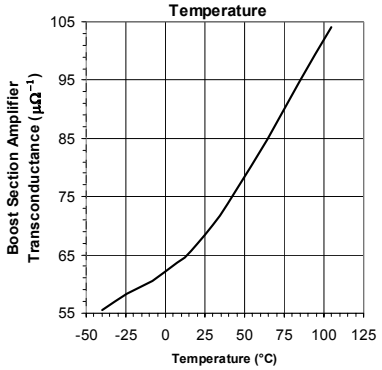
Boost Section Feedback Pin Bias Current vs Temperature



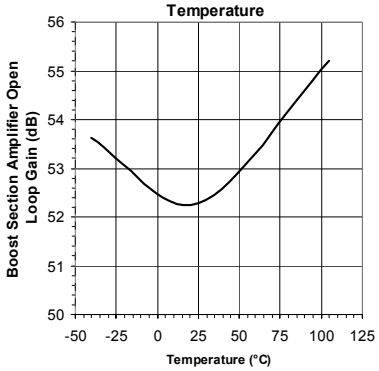
Boost Section Feedback Voltage vs Temperature



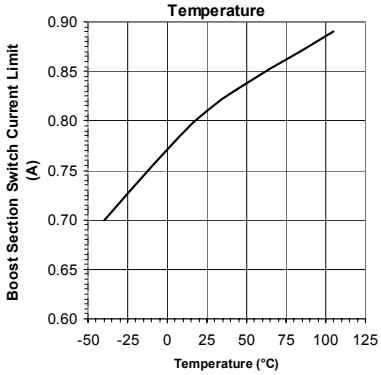
Boost Section Amplifier Transconductance vs Temperature



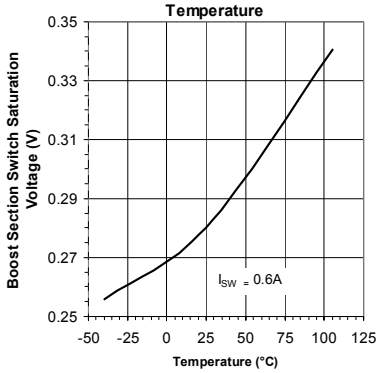
Boost Section Amplifier Open Loop Gain vs Temperature



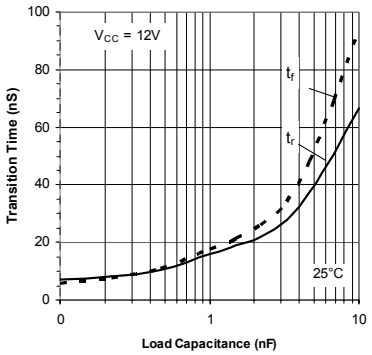
Boost Section Switch Current Limit vs Temperature



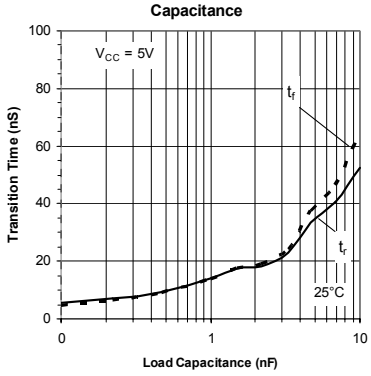
Boost Section Switch Saturation Voltage vs Temperature



Bottom Gate Driver Transition Time vs Load Capacitance

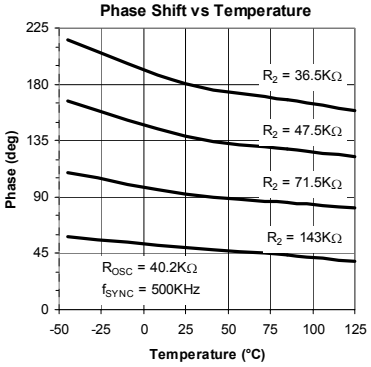


Bottom Gate Driver Transition Time vs Load Capacitance

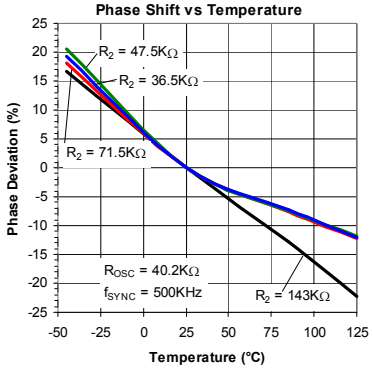


Typical Characteristics

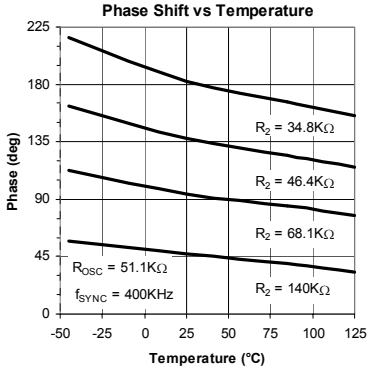
Phase Shift vs Temperature



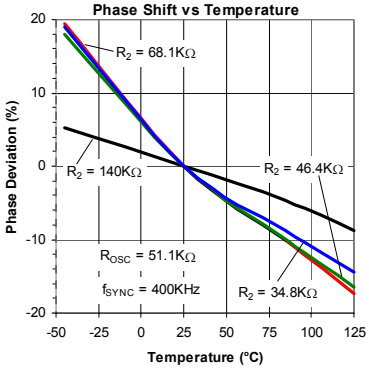
Percentage Deviation In Phase Shift vs Temperature



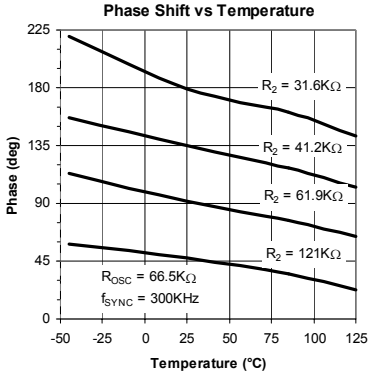
Phase Shift vs Temperature



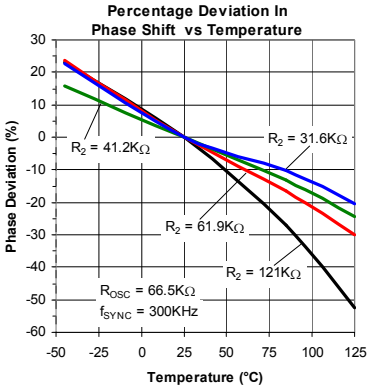
Percentage Deviation In Phase Shift vs Temperature



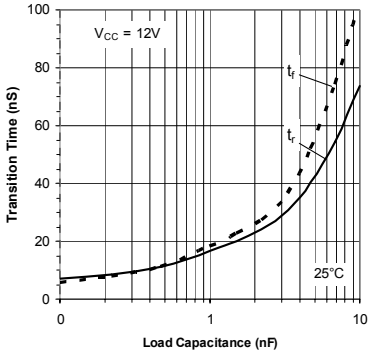
Phase Shift vs Temperature



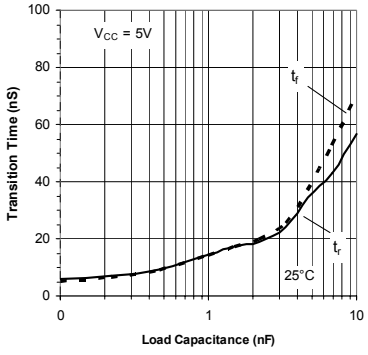
Percentage Deviation In Phase Shift vs Temperature



Upper Gate Driver Transition Time vs Load Capacitance



Upper Gate Driver Transition Time vs Load Capacitance



Operation

Overview

The SC2441A is a constant-frequency switching regulator capable of operating from 1.8V to 20V input. It consists of two current-mode step-down switch-mode PWM controllers driving all N-channel MOSFETs and an auxiliary step-up current-mode converter with an integrated 0.6A power switch. A local supply (>5V) can be generated from a low voltage input (3.3V, 2.5V or 1.8V) to provide sufficient gate drives for the step-down converters.

The two step-down channels of the SC2441A operate at 180 degrees out of phase from each other. Input currents are interleaved in a two-phase converter so input ripple current is lower and lower input capacitance can be used for filtering.

The step-down controllers of the SC2441A operate in synchronous continuous-conduction mode. They can function either as two independent step-down controllers producing two separate outputs or as a dual-phase single-output controller by tying the FB2 pin to V_{IN} (Figure 2). In single output mode, the channel 1 error amplifier controls both channels and the channel 2 error amplifier is disabled. Soft-start and overload hiccup of both channels are also controlled by channel 1. In Figure 2 the output SEL of the comparator A1 determines which error amplifier outputs and fault signals are routed to channel 2. The minimum required FB2 voltage for single output mode is 1.55V.

Phase-Locked Loop and Synchronization

The SC2441A utilizes a phase-locked oscillator (Figure 5) for clock generation and external synchronization. The advantages of using a phase-locked loop (PLL) are: (i) when the step-down channels are synchronized, the auxiliary step-up regulator in the SC2441A can be made to run at twice the external clock frequency to reduce component size and (ii) two or more SC2441A can be daisy chained using the clock output (pin 28) and interleaved with programmable phase shift. Each step-down controller within a SC2441A operates at 180 degrees out of phase from the other step-down controller. The switching frequency of the step-down controllers can be set with an external resistor ROSC. The boost regulator and the step-down controllers are capable of operating up to 2 MHz and 1 MHz respectively. It is necessary to consider the operating duty-ratio range before deciding the switching frequency. See Applications Information section for more details.

Consider the detailed block diagram of the PLL in Figure 5. The phase/frequency detector compares the buffered external clock XCLK with the $\overline{Q_T}$ output of the toggle flip-flop. If the rising edge of XCLK leads that of $\overline{Q_T}$, then Q_U will go high between the two corresponding rising edges. Switch S_1 is closed, charge is delivered to the loop filter and the voltage at the PLLF pin increases. This in turn causes the current output of the voltage to current converter (V/I) and the switching frequency of the current-controlled oscillator (CCO) to increase. If $\overline{Q_T}$ rises before XCLK, then Q_D will go high from the rising edge of $\overline{Q_T}$ to the rising edge of XCLK. Switch S_2 is closed, charge is drawn from the loop filter and the PLLF voltage falls. The switching frequency of the current-controlled oscillator (CCO) decreases. When the PLL is in lock, the rising edges of XCLK and $\overline{Q_T}$ are aligned. Q_U and Q_D will go high for only a few gate delays. The PLLF stabilizes to a constant DC voltage and the CCO runs at the same frequency as the external clock.

In the absence of an external clock, S_2 is closed and the PLL loop filter is continuously discharged. Not shown in Figure 5 is an internal PLLF lower clamp circuit that limits the minimum voltage at the PLLF pin to 0.17V. This sets the lowest operating frequency and thus the lower bound of the PLL lock-range. The V/I in Figure 5 is shown with two non-inverting inputs. The lower voltage non-inverting input takes control of the V/I. If the PLLF pin is tied to VIN (>1.8V) through a current-limiting resistor, then the 0.4V input of the V/I will predominate. The 0.4V input therefore sets the upper excursion limit of the V/I and the maximum operating frequency of the PLL at a given ROSC. The maximum PLL frequency to the minimum locking frequency ratio is about 2. When the SC2441A is not synchronized externally, the PLLF pin should be tied high through a resistor. The CCO will then run at its maximum frequency.

When two SC2441As are used in a master-slave configuration, the PLLF pin of the master SC2441A is tied high and its free running frequency is set with the resistor ROSC. CKOUT of the master is then tied to the SYNC/ $\overline{SHDN}$ input of the slave SC2441A. The free running and the

Operation (Cont.)

minimum locking frequencies of the slave should be selected to accommodate the variation in the master's frequency. Phase shift between the master and the slave can be programmed with an optional resistor (Figure 5). More detailed discussion can be found in the Application Information.

Pulling the SYNC/ $\overline{\text{SHDN}}$ pin below 0.5V shuts off the SC2441A after 85µs time delay.

Control Loop

The step-down controllers and the boost regulator in the SC2441A use peak current-mode control for fast transient response and current sharing in single output operation. Current-mode switching regulators utilize a dual-loop feedback control system. The error amplifier output controls the peak inductor current of that channel. This is the inner current loop. The double reactive poles of the output LC filter are reduced to a single real pole by the inner current loop, easing loop compensation. Fast transient response can be obtained with a simple Type-2 compensation network. In the outer loop, the error amplifier regulates the output voltage.

Referring to the block diagrams in Figures 2 and 3, the sensed inductor current is summed with the slope-compensating ramp before compared to the output of the error amplifier. The PWM comparator trip point determines the switch turn-on pulse width. The current-limit comparator ILIM turns off the power switch when the sensed current exceeds the corresponding current-limit threshold. ILIM therefore provides cycle-by-cycle current limit. All three converters in the SC2441A have internal ramp-compensation to prevent sub-harmonic oscillation when operating above 50% duty cycle. The internal compensating ramp is designed for an inductor ripple-current between $\frac{1}{4}$ and of the maximum inductor current and the peak-to-peak current-sense voltage (CSP-CSN of the step-down controllers) between and of the current-limit threshold (25mV). The current-limits of all three converters are unaffected by the compensation ramps.

Current-Sensing

The inductor current needs to be sensed for use as PWM modulating ramp. Either sense resistor or inductor series resistance (DCR) can be used as the sensing element for the step-down controllers. Since the maximum current-sense voltage (CSP-CSN) is only 25mV, a precision sense resistor in series with the inductor can be used at the output without resulting in excessive power dissipation. Alternatively the DCR of the inductor can also be used. Both methods are less sensitive to supply and ground transients than high-side or low-side sensing because the sensed voltage is developed at the output of the step-down converter. DCR sensing will be described in more details in the Applications Information section.

Boost switch current is sensed with an integrated sense resistor with a minimum current-limit of 0.6A.

Error Amplifiers

All error amplifiers in the SC2441A are of transconductance type. Converters are compensated with series RC network from the COMP pins to the ground. An additional small parallel capacitor may be required for stability.

In Figure 2 the error amplifiers EA1 and EA2 are shown with two non-inverting inputs. The non-inverting input with lower voltage predominates. One positive input is biased to a 0.5V precision reference. The other non-inverting input of the error amplifier is tied to a voltage equal to

$(V_{SS/EN} - 1.25V)/3$.

During converter start up, the effective positive input of the error amplifier stays at 0 until the soft-start capacitor at the SS/EN pin is charged above 1.25V. The corresponding COMP pin is also pulled low by the comparator A_2 or A_3. After the SS/EN voltage exceeds 1.25V, the COMP pin is released. Both the upper and the lower gate drives remain low until the COMP voltage exceeds 1.85V. If the soft-start capacitor charging time is sufficiently long, then both the FB and the output voltage will track the divided SS/EN voltage on their way to regulation. If the starting output voltage is non-zero, then the COMP voltage and the corresponding gate drives will remain low until the divided SS/EN voltage exceeds the feedback voltage. Starting into a pre-existing output is seamless.

Operation (Cont.)

In closed loop operation, EA1 and EA2 output voltage vary from 1.2V to 3.5V with the range 1.2V to 1.85V corresponding to negative peak sense voltages. Both gate drives are kept off until the COMP voltage exceeds 1.85V in start up.

The error amplifier of the step-up converter has a 1.25V reference voltage. Its output voltage excursion is from 0.8V to 1V in closed-loop operation.

Current-Limit

The 25mV maximum current sense voltage is the cycle-by-cycle peak current limit of the step-down controller.

Gate Drivers

The SC2441A uses an adaptive non-overlapping control scheme to switch the upper and the synchronous MOSFETs. The synchronous MOSFET of each step-down channel is turned off at the falling-edge of the phase clock. The control (upper) MOSFET is not turned on until the synchronous gate drive goes low. The phase inductor current ramps up. When the sensed inductor current reaches the threshold determined by the error amplifier output and ramp compensation, the control MOSFET is turned off. The synchronous MOSFET is not turned on until the upper gate drive goes low.

The supply voltage for the upper gate driver is obtained from a diode-capacitor bootstrap circuit. If the bootstrap capacitor is charged from V_{CC}, then the high-side gate drive voltage will swing from approximately $2V_{CC}$ to ground. The synchronous gate drive swings from V_{CC} to ground.

Soft-Start and Overload Protection

Figure 4 shows the functional diagram of the soft-start and overload protection circuit. The soft-start capacitor C_{SS} and its charging resistor R_{SS} are tied to the SS/EN pin. Together they set the soft-start time. Before V_{CC} rises to 4.5V, the undervoltage lockout circuit discharges C_{SS} to ground. After V_{CC} rises above 4.5V, Q_1 turns off and C_{SS} is slowly charged by R_{SS}. Comparator C_2 and latch L_2 first disable both the upper and lower gate drives. Hysteretic comparator C_1 resets the latch L_1 so that hiccup is disabled during start up. As mentioned above, there is no PWM (=TGON) pulse until C_{SS} is above 1.25V and the corresponding COMP rises above 1.85V. Once the first TGON pulse appears, L_2 is reset and both gate drivers of that channel are enabled.

After C_{SS} is charged above 3.3V, C_1 output goes low. Hiccup is armed. If the output voltage is less than 70% of the set value due to improper start up or output overload, then C_3 will set the overload latch L_1. Both gate drivers of the channel are turned off and the 10µA current source discharges C_{SS}. R_{SS} must be large enough to ensure full discharge of C_{SS} down to 0.5V. Soft-start process should be slow enough to allow the output to reach 70% of its final value before hiccup is armed. The overload latch L_1 is reset when the C_{SS} capacitor is discharged below 0.5V. The 10µA current source turns off. C_{SS} capacitor is recharged by R_{SS} and the converter undergoes soft-start. If overload persists, the step-down converters will undergo repetitive shutdown and restart (hiccup).

If the output is short-circuited, the inductor current will not increase indefinitely between the times the inductor current reaching its current limit and shutdown. This is due to cycle skipping reduces the actual operating frequency.

Pulling the SS/EN pin below 0.8V with an open-collector transistor sets the disable latch L_2 and turns off the gate drives. The SS/EN pin can be used as the enable input for the controller.

The soft start timing diagram and the hiccup operation timing diagram are shown in Figures 6a and 6b respectively.

Applications Information

Operating Frequency (f_s)

The switching frequency in the SC2441A is user-programmable. The advantages of constant frequency operation are simple passive component selection and fast transient response with simple frequency compensation. Before setting the operating frequency, the following trade-offs should be considered.

1) passive component sizes
2) converter efficiency
3) EMI
4) Minimum switch on time and
5) Maximum duty ratio

For a given output power, the sizes of the passive components are inversely proportional to the switching frequency, whereas MOSFET's/Diodes switching losses are proportional to the operating frequency. Other issues such as heat dissipation, packaging and the cost issues should be considered. The frequency bands for signal transmission should be avoided because of EM interference.

The switching frequency of both step-down controllers is set with an external resistor from Pin 10 to the signal ground. The set frequency is inversely proportional to the resistor value (Figure 7) and can be approximated as:

$$R_{OSC} = 101618 \cdot F_{SW}^{-1.22}$$

R_{OSC} is in KΩ and F_{SW} is in KHz.

The internal oscillator starts to operate once V_{IN} exceeds its UVLO threshold. The oscillator output, CLK, (see Figure 2) clocks the step-up converter. The frequency divider generates two out-of-phase clocks, CLK1 and CLK2, at a half of CLK frequency. CLK1 and CLK2 clock the step-down channels. The switching frequency of the step-up converter is twice those of the step-down controllers. If both step-down channels are running at 250KHz, then the boost section will be running at 500KHz.

R_{OSC} vs. Step-down Channel Switching Frequency

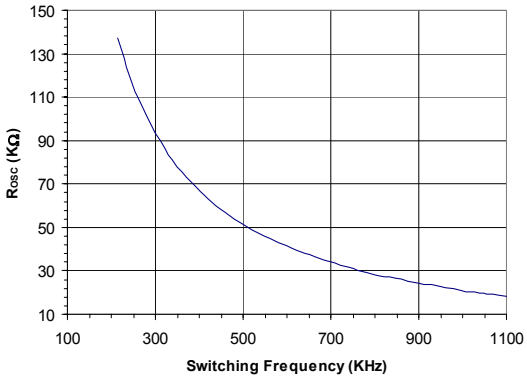


Figure 7. R_{OSC} vs. Step-down Channel Free-running Frequency

Minimum Switch On Time Limitation

In both step-down controllers, the falling edge of the clock turns on the top MOSFET. The inductor current ramps up so does the sensed voltage. After the sensed voltage crosses a threshold determined by the error amplifier output, the top MOSFET is turned off. The propagation delay time from the turn-on of the controlling FET to its turn-off is the minimum switch on time. The SC2441A has a minimum on time of about 180ns at room temperature. This is the shortest on interval of the controlling FET. The controller either does not turn on the top MOSFET at all or turns it on for at least 180ns.

For a synchronous step-down converter, the operating duty cycle is V_O / V_{IN}. So the required on time for the top MOSFET is $V_O/(V_{IN} f_S)$. If the frequency is set such that the required pulse width is less than 180ns, then the converter will start skipping cycles. Due to minimum on time limitation, simultaneously operating at very high

Applications Information

switching frequency and very short duty cycle is not practical. If the input voltage is 3.3V and the operating frequency is 1MHz, the lowest output voltage will be 0.6V. There will not be enough modulation headroom if the on time is simply made equal to the minimum on time of the SC2441A. For ease of control, we recommend that the required pulse width be at least 1.5 times the minimum on time.

Maximum Duty-cycle Consideration

The top MOSFET turns off for at least 200ns every cycle regardless of the switching frequency. This places an upper bound on the voltage conversion ratio at a given switching frequency.

If the desired output voltage requires high operating duty-cycle, then operating frequency will have to be lowered to allow modulating headroom.

RC Filtering network for V_{CC} and V_{IN} pins

A RC filtering network is recommended for the SC2441A V_{CC} and V_{IN} pin connections. As shown in Figure 1, R_6 plus C_8 and R_2 plus C_2 are the filtering networks for V_{CC} pin and V_{IN} pin respectively. The value of the R_6 and R_2 ranges from 3.3Ω to 5.11Ω. C_8 and C_2 should be larger than 1μF.

C_8 and C_2 are the decoupling capacitors for the V_{CC} pin and V_{IN} pin. They should be placed as close as possible to the pins of the SC2441A to achieve the best decoupling performance. Due to the different functionalities of the V_{CC} pin and V_{IN} pin, C_2 should be placed between the V_{IN} pin and the signal ground of the SC2441A. And C_8 should be placed between the V_{CC} pin and the power ground of the SC2441A. The recommended connections for the V_{CC} pin and V_{IN} pin are illustrated in Figure 8.

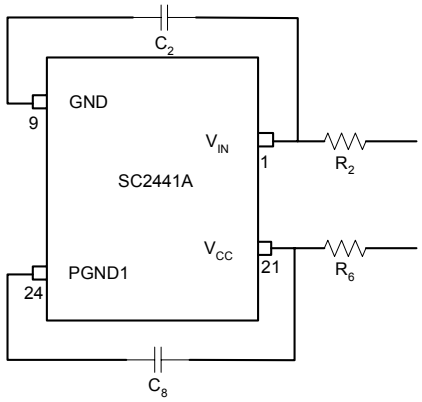


Figure 8. RC Network Connections for V_{IN} and V_{CC} pins

Step-Up Converter

The SC2441A features a step-up regulator and two step-down controllers.

The boost section of the SC2441A comprises of pins 7, 8, 26 and 27. Pin 26 is the independent power ground for the boost converter section, which should be separated from the step-down section power ground pin 24 in layout to minimize the noise influence. The boost section in SC2441A has an internal reference set at 1.25V. The output of the boost section can be programmed with external resistors R_1 and R_4 as shown in Figure 1.

$$V_{BOOST} = 1.25V \times \frac{R_1 + R_4}{R_4}$$

SC2441A utilizes a transconductance error amplifier for the step-up controller and it can be compensated with C_3, R_5 and C_5 as shown in Figure 1. The step-up controller in the SC2441A employs cycle-by-cycle peak current limit to protect the internal switching transistor. Current limit threshold is typically 0.8A.

In the applications where only low input voltage is available, the step-up converter in the SC2441A is very useful for generating an auxiliary output to power the gate drive of the step-down controllers.

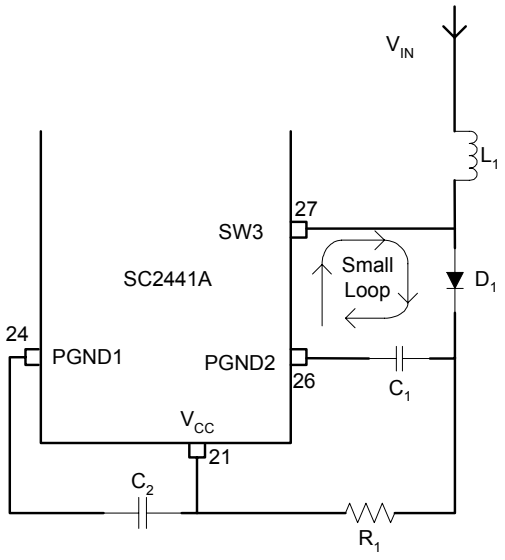


Figure 9. Step-Up Section Layout Illustration

As shown in Figure 9, to minimize the switching noise generated by the step-up converter, the loop formed by D_1, C_1, SW3 and PGND2 should be as small as possible. And the PGND2 pin should be tied to PGND1 at one spot close to the PGND1 pin.

Step-up Converter Inductor Selection

For a specified inductor current ripple ratio δ_3 (peak-to-peak current ripple v.s. actual input current I_{IN}), the inductor value is

$$L_1 = \frac{V_{in}}{f_{s3}\delta_3 I_{o3}}\left(1-\frac{V_{in}}{V_{o3}}\right)\frac{V_{in}}{V_{o3}}.$$

Typically, select δ_3 <2 for a Continous Conduction Mode (CCM) operation.

If V_{in} = 3.3V, V_{o3} = 5V and I_{o3} = 100mA with δ_3 = 1.6 and f_{s3} = 1MHz, then, L_1 = 4.7µH.

Assuming that the efficiency of the boost converter is η and the boost converter is running in CCM with duty ratio D. The peak inductor current is

$$I_{L1PEAK} = \frac{V_{o3}\cdot I_{o3}}{V_{in}\cdot \eta} + \frac{V_{in}}{L_1}\cdot D\cdot T\cdot \frac{1}{2}$$

The saturation current rating of the selected inductor should be at least 1.2 times of the calculated peak current value.

Step-up Converter Capacitor Selection

Input capacitor: The input capacitance should be large such that the input transients due to both the step-up and the step-down converters do not trip the UVLO threshold 1.71V. Since the SC2441A controls a 2-phase low input voltage step-down converter, the input capacitance is sized to handle the input ripple current of the buck converter. This is usually sufficient for the auxiliary boost converter because the input current in a boost converter is continuous.

Output capacitor: Unlike buck converter, pulse current is delivered to the output of a boost converter. To reduce the output ripple voltage, low ESR capacitors should be used. The output capacitor should also be able handle the output ripple current. The SC2441A is designed to use multi-layer ceramic capacitor as the sole output capacitor.

Maximum Output Current of the Step-up Converter

Figure 3 shows that the boost switch current is sensed with an internal sense resistor Rs and it is internally limited at 0.6A. So the maximum output current can be given as (η is the efficiency of the step-up section):

$$I_{o3,max} = (0.6A - \frac{\delta_3}{2})\cdot \frac{V_{in}\cdot \eta}{V_{o3}}$$

Applications Information

Loop Compensation for the Step-Up Converter

A simple small signal model for current-mode boost converter in continuous-conduction mode is shown in Figure 10.

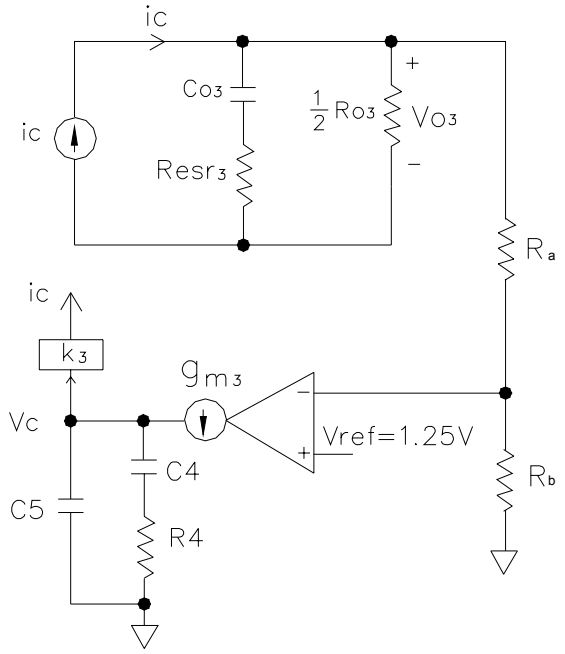


Figure 10. Small signal model of Boost converter.

In Figure 10, C_{o3} and R_{esr3} are the capacitance and the ESR of the output capacitor, g_{m3} is the error amplifier transconductance and k_3 is the current loop gain. If one specifies the loop crossover frequency f_c, the compensation component values are readily calculated as

$$C_4 = h_3 g_{m3} k_3 (1-D_3)\frac{R_{o3}}{2} \left|1-\frac{f_c}{f_{z1}}\right| \frac{1}{2\pi f_c}\frac{R_{esr3}}{R_{esr3}+0.5R_{o3}},$$

$$R_4 = \frac{1}{C_4} C_{o3}(R_{esr3}+\frac{R_{o3}}{2})$$

and

$$C_5 = C_4 \frac{2R_{esr3}}{R_{o3}}$$

$$f_{z1} = \frac{(1-D_3)^2 R_{o3}}{2\pi L_3}.$$

$$h_3 = \frac{R_b}{R_a + R_b}$$

Soft-Starting the Step-Down Controllers

The soft-start of the two step-down converters are independently controlled through SS1 pin and SS2 pin. As lillustrated in Figure 4, if V_{CC} is below 4.5V, Q_1 will be on, keeping C_{SS} discharged. When FAULT goes low, Q_1 is turned off, C_{SS} gets charged via R_{SS} from V_{CC}. Values of R_{SS} and C_{SS} set different start-up times.

As shown in Figure 4, if the output falls below 70% of its setpoint, the Css will be discharged with a 10µA current sink. R_{SS} must be large enough to allow the soft-start capacitor to be discharged below 0.5V. Soft-start process should be long enough to allow the output to reach 70% of its final value before hiccup is armed.

Coincident Soft-Start

The step-down controllers can be made to start coincidently. The method is shown in Figure 11.

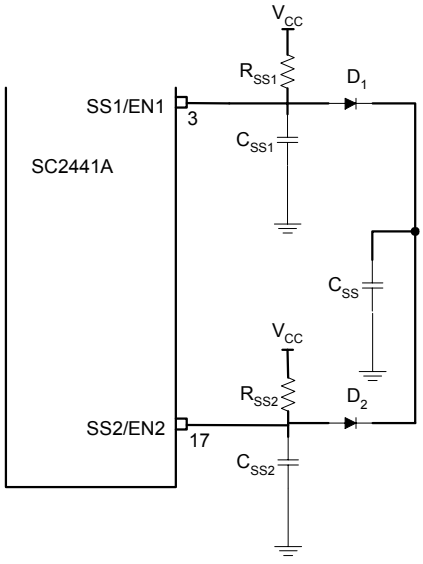


Figure 11. Coincident Soft-Start for Step-Down Converters

The capacitance of C_{SS}, as shown above, should be more than 3 times of the capacitance of the C_{SS1} and C_{SS2}.

Applications Information

DCR Current Sensing

Either precision sense resistor or inductor DCR can be used as the inductor current sensing element.

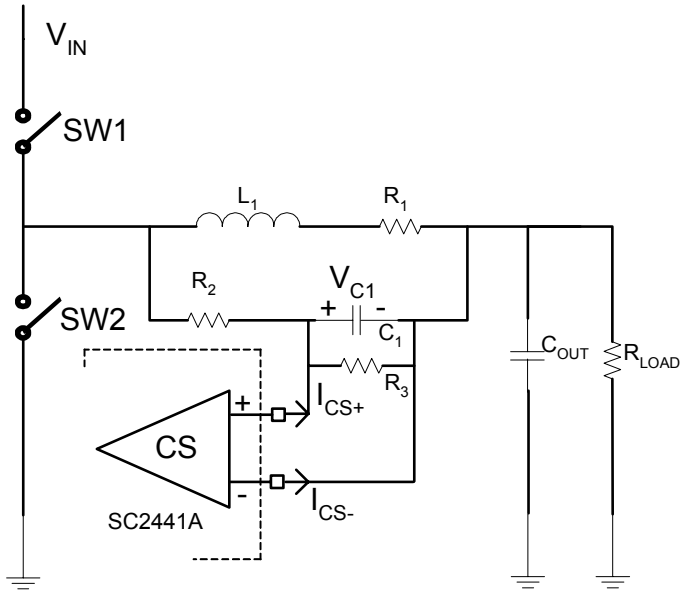


Figure 12. Current Sensing Circuit.

In Figure 12 SW1 and SW2 represent the MOSFET switches. CS is the current sense amplifier. I_{CS+} and I_{CS-} are the input bias currents of the CS. L_1 is the output inductor. R_1 is the DC resistance of L_1. R_2, R_3 and C_1 constitute the DCR current sensing network.

Assuming that CS input bias currents are zero and that R_3 is not used, if the time constant L_1/R_1 is made equal to the time constant R_2C_1, then the voltage across the inductor DCR, R_1, will be replicated across C_1 in the steady state (see Figure 13). The following equations apply:

$$I_{L1\cdot PEAK} = I_O + \Delta I_{L_1}/2$$

$$I_{L1\cdot VALLEY} = I_O - \Delta I_{L_1}/2$$

$$V_{C1}(t) = I_{L1}(t)\cdot R_1$$

where, I_O is the output current and ΔI_{L1} is the peak-to-peak L_1 current ripple. The inductor current can therefore be sensed by monitoring C_1 voltage. L should be selected so that the is between 25% to 33% of the I_O.

However CS input bias currents are not zero. I_{CS+} and I_{CS-} are typically 0.4µA and 40µA respectively (see electrical characteristics) and can not be ignored.

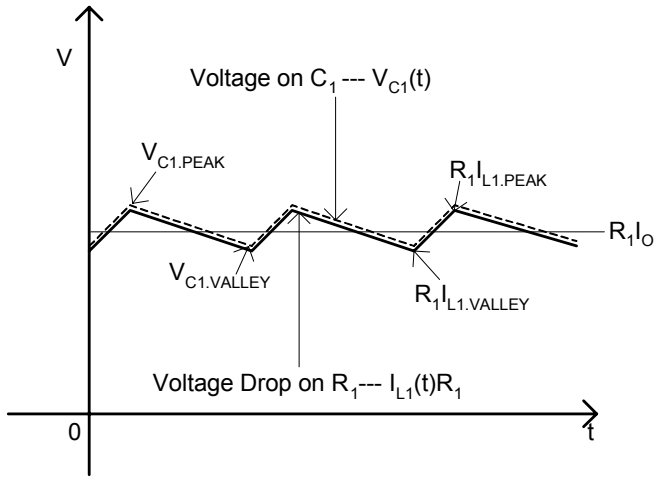


Figure 13. Voltage Waveform C_1 and R_1

In Figure 12, R_2 and R_3 resistive divider attenuates the sensed signals when I . The time constant resulting from L_1 and its DCR R_1 is:

Define R_{EQU}:

The time constant of the DCR sensing network is:

If $\tau_{C1} = \tau_{L1}$, then the peak and valley voltages across C_1will be:

$$V_{C1\cdot VALLEY} = I_{CS+}\cdot R_{EQU} + \frac{R_3\cdot R_1}{(R_2+R_3)}\cdot\left(I_O - \frac{\Delta I_{L1}}{2}\right)$$

I_{CS+} therefore introduces an offset error to the sensed voltage. To reduce this error, R_{EQU} must be minimized.

Suppose V_{IN}=5V; V_{OUT}=2.5V; D=50%; I_{OUT}=20A; F_{SW}=500KHz; L_1=0.5µH; R_1=2mΩ; I_{CS+}=1µA. The output current limit is set at 28A. The time constant formed by L_1 and R_1 is

$$\tau_{L1} = \frac{L_1}{R_1} = 0.25\text{ms} = \frac{R_2\cdot R_3}{R_2+R_3}\cdot C_1$$

$$\Delta I_{L_1} = 5\text{A}$$

$$V_{C1\cdot PEAK} = I_{CS+}\cdot R_{EQU} + \frac{R_3\cdot R_1}{(R_2+R_3)}\cdot\left(28\text{A} + \frac{\Delta I_{L1}}{2}\right) = 25\text{mV}$$

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$$\frac{R_2 \cdot R_3}{R_2 + R_3} \cdot C_1 = 0.25ms$$

$$1\mu A \cdot \frac{R_3 \cdot R_2}{(R_2 + R_3)} + \frac{R_3 \cdot R_1}{(R_2 + R_3)} \cdot \left(28A + \frac{5A}{2} \right) = 25mV$$

With an arbitrary selection of $\frac{R_2 \cdot R_3}{R_2 + R_3} = 3.01K\Omega$, we can get C_1=83nF. Since 83nF is not a standard capacitance value, we use 100nF capacitor for C_1. Consequently, $\frac{R_2 \cdot R_3}{R_2 + R_3} = 2.5K\Omega$. And we can also derive:

$$1\mu A \cdot 2.5K\Omega + \frac{R_1}{R_2} \cdot 2.5K\Omega \left(28A + \frac{5A}{2} \right) = 25mV$$

$$R_2 = 6.80K\Omega$$

$$R_3 = 3.92K\Omega$$

Pre-biased Start Up

Sometimes the step-down converter is to start into a pre-biased output load. The pre-biased voltage is normally lower than the output setpoint of the step-down converter.

As described earlier, pre-bias startup process with the SC2441A is seamless. The testing setup of the pre-biased start-up is shown as in Figure 14.

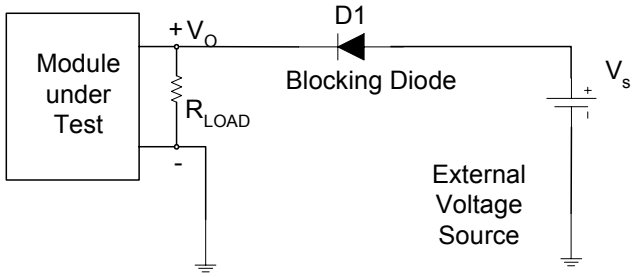

Figure 14. Test Setup for Pre-biased Start Up

In Figure 14, V_S is the external power supply pre-biasing V_O. D_1 blocks the output of the power module under test from V_S during soft-start. R_{LOAD} is the resistive load of the module under test. Before power-up the module, monitor V_O to ensure that it is the desired pre-biased output voltage. Then power-up the module. V_O should rise smoothly.

Free-running Operation

The internal oscillator of the SC2441A can either free-run or it can be phase-locked to an external clock.

In free-running mode, the internal phase-locked loop is disabled by tying an external resistor from the PLLF pin to V_{IN}. The external resistor ROSC (see figure 5(a)) programs the channel frequency. The PLLF pull-up resistor should be carefully selected so that the voltage at the PLLF pin is above 1V. A value between 20KΩ to 50KΩ is recommended.

Pull-up resistor can also be tied to V_{CC} if V_{CC} is present before the SC2441A starts to switch. The advantage tying the pull-up resistor to V_{CC} is because that the V_{CC} is a regulated output from either a boost converter or a sepic converter. The resistor from the PLLF pin can be tied to V_{CC} if V_{CC} is from a boost converter output. The reason is that the V_{CC} will be powered up from the input V_{IN} before output of the boost converter reaches the setpoint. However, in some applications, a SEPIC converter is employed to get stable V_{CC} due to the wide input voltage range. In this case, the resistor from the PLLF pin should not be connected to the V_{CC} due to the presence of a DC blocking capacitor in the converter. The SC2441A will not switch if the PLLF pin is at zero volt.

Applying more than 2.1V at the PLLF pin activates the diode clamp circuit (see Figure 5(a)). The filtering components (R_1,R_2, C_1 and C_2 in Figure 5(a)) are not needed while free-running. The clamp activation will have no effect on the PLL if V_{PLLF} >1V.

The internal clock is brought out to the CKOUT pin. The signal at CKOUT pin can be used as the synchronizing clock for other SC2441As in a master-slave configuration.

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Master - Slave Mode Configuration

The configuration for SC2441A master-slave mode operation is shown in Figure 15. The master is made free running, the master clock frequency should be within the synchronizing range of the slave.

In the Master-Slave mode, the SS2441A can be synchronized to an external clock signal applied to the SYNC pin. External filtering componets (R_1, R_2, C_1 and C_2) on the PLLF pin are necessary for the slave SC2441A . The PLLF pull-up resistor is not necessary for the slave converter.

Phase shift between the master and the slave is the phase lag measured between the sync input and the clock output of the slave. Typical relationship between the phase shift and the slave value of the resistor R_2 is shown in the "Typical Characteristics".

For the SC2441A running at slave mode, its free-runing frequency (internal switching frequency) set with ROSC should be programmed 20% higher than the external synchronization frequency.

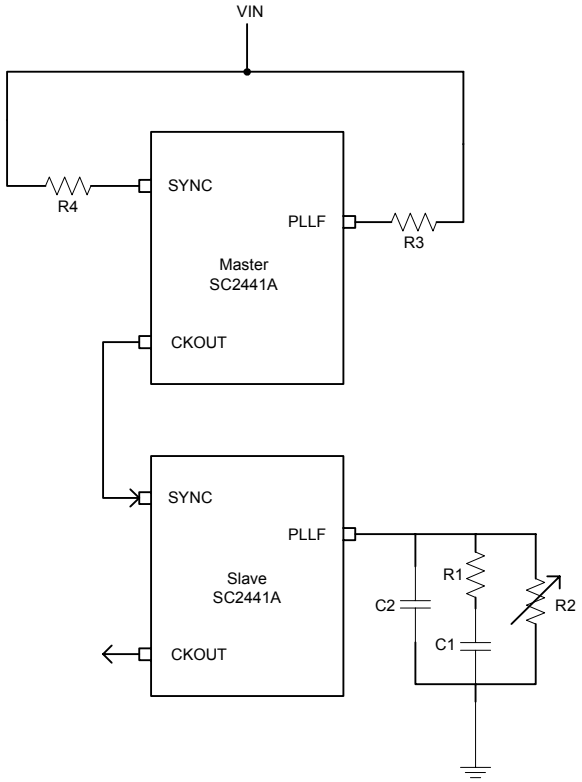

Figure 15. Master-Slave Synchronization

As shown in Figure 15, the CKOUT signal of the master SC2441A is the input sync signal for the slave SC2441A. The R_1, C_1 and C_2 constitute the filtering circuit stabilizing the phase lock loop in the slave SC2441A. R2 (between 30kΩ and 150kΩ) determines the phase shift between the slave CKOUT and its SYNC input.

PLL Frequency Compensation

Applying synchronizing clock with step change in frequency adjust compensation components until overshoot and ringing at PLLF pin is minimized.

Output Inductor and Ripple Current in Step-down Sections

Both step-down controllers in the SC2441A operate in synchronous continuous-conduction mode (CCM) regardless of the output load. The output inductor selection/design is based on the output DC and transient requirements. Both output current and voltage ripples are reduced with larger inductors but it takes longer to change the inductor current during load transients. Conversely smaller inductors results in lower DC copper losses but the AC core losses (flux swing) and the winding AC resistance losses are higher. A compromise is to choose the inductance such that the peak to peak inductor ripple current is 20% to 30% of the rated output current.

Assume that the inductor current ripple (peak-to-peak) is $\delta * I_o$ Then the inductance will be

$$L = \frac{V_o(1-D)}{\delta I_o f_s}.$$

The peak current in the inductor becomes (1+δ/2)*Io and the RMS current is

$$I_{L,rms} = I_o\sqrt{1+\frac{\delta^2}{12}}.$$

The followings are to be considered when choosing inductors.

a) Inductor core material: For high efficiency applications above 350KHz, ferrite, Kool-Mu and polypermalloy materials should be used. Low-cost powdered iron cores can be used for cost sensitive-applications below 350KHz but with attendant higher core losses.

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b) Select inductance value: Sometimes the calculated inductance value is not available off-the-shelf. The designer can choose the adjacent (larger) standard inductance value. The inductance varies with temperature and DC current. It is a good engineering practice to re-evaluate the resultant current ripple at the rated DC output current.
c) Current rating: The saturation current of the inductor should be at least 1.5 times of the peak inductor current under all conditions.

Output Capacitor (C_o) and V_{out} Ripple in Step-down Sections

The output capacitor provides output current filtering in steady state and serves as a reservoir during load transient. The output capacitor can be modeled as an ideal capacitor in series with its parasitic ESR (R_{esr}) and ESL (L_{esl}) (Figure 16).

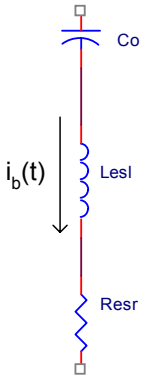

Figure 16. C_o equivalent circuit

If the current through the branch is $i_b(t)$, the voltage across the terminals will then be

$$v_o(t) = V_o + \frac{1}{C_o}\int_0^t i_b(t)dt + L_{esl}\frac{di_b(t)}{dt} + R_{esr}i_b(t).$$

This basic equation illustrates the effects of ESR, ESL and C_o on the output voltage.

The first term is the DC voltage across C_o at time t=0. The second term is the ripple-voltage caused by the inductor ripple-current. The third term is the voltage ripple due to ESL and the fourth term is the voltage ripple due to ESR. The total output voltage ripple is then a *vector* sum of the last three terms.

Since the inductor current is a triangular waveform with peak-to-peak value $\delta * I_o$, the ripple-voltage caused by inductor current ripples is

$$\Delta v_C \approx \frac{\delta I_o}{8C_o f_s}.$$

The ripple-voltage due to ESL is

$$\Delta v_{ESL} = L_{esl} f_s \frac{\delta I_o}{D}$$

and the ESR ripple-voltage is

$$\Delta v_{ESR} = R_{esr}\delta I_o.$$

Aluminum capacitors (e.g. electrolytic, solid OS-CON, POSCAP, tantalum) have high capacitances and low ESL's. The ESR has the dominant effect on the output ripple voltage. It is therefore very important to minimize the ESR.

When determining the ESR value, both the steady state ripple-voltage and the dynamic load transient need to be considered. To keep the steady state output ripple-voltage < ΔV_o, the ESR should satisfy

$$R_{esr1} < \frac{\Delta V_o}{\delta I_o}.$$

To limit the dynamic output voltage overshoot/ undershoot within α (say 3%) of the steady state output voltage) under 0 to full load current swing, the ESR value should be

$$R_{esr2} < \frac{\alpha V_o}{I_o}.$$

The required ESR value of the output capacitors should be

$$R_{esr} = \min\{R_{esr1}, R_{esr2}\}.$$

In the aluminum capacitor selection, the working voltage rating is normally suggested to be greater than $1.5V_o$. The allowable current ripple (RMS) should be greater than

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$$\frac{\delta I_o}{2\sqrt{3}}.$$

Usually it is necessary to have several capacitors of the same type in parallel to satisfy the ESR requirement. The voltage ripple cause by the capacitor charge/discharge should be an order of magnitude smaller than the voltage ripple caused by the ESR. To guarantee this, the capacitance should satisfy

$$C_o > \frac{10}{2\pi f_s R_{esr}}.$$

In many application circuits, several low ESR ceramic capacitors are added in parallel with the aluminum capacitors to further reduce ESR and improve high frequency decoupling. Since the capacitances and the ESR's of ceramic and aluminum capacitors are different, the following remarks are made to clarify some practical issues.

Remark 1: High frequency ceramic capacitors may not carry most of the ripple current. It also depends on the capacitor value. Only when the capacitor value is set properly, the effect of ceramic capacitor low ESR starts to be significant.

For example, if a 10µF, 4mΩ ceramic capacitor is connected in parallel with 2x1500µF, 90mΩ electrolytic capacitors, the ripple current in the ceramic capacitor is only about 42% of the current in the electrolytic capacitors at the ripple frequency. If a 100µF, 2mΩ ceramic capacitor is used, the ripple current in the ceramic capacitor will be about 4.2 times of that in the electrolytic capacitors. When two 100µF, 2mΩ ceramic capacitors are used, the current ratio increases to 8.3. In this case most of the ripple current flows in the ceramic decoupling capacitor. The ESR of the ceramic capacitors will then determine the output ripple-voltage.

Remark 2: The total equivalent capacitance of the filter bank is not simply the sum of all the paralleled capacitors. The total equivalent ESR is not simply the parallel combination of all the individual ESR's either. Instead they should be calculated using the following formulae.

$$C_{eq}(\omega) := \frac{(R_{1a}+R_{1b})^2\omega^2 C_{1a}{}^2 C_{1b}{}^2 + (C_{1a}+C_{1b})^2}{(R_{1a}{}^2 C_{1a}+R_{1b}{}^2 C_{1b})\omega^2 C_{1a}C_{1b}+(C_{1a}+C_{1b})}$$

$$R_{eq}(\omega) := \frac{R_{1a}R_{1b}(R_{1a}+R_{1b})\omega^2 C_{1a}{}^2 C_{1b}{}^2 + (R_{1b}C_{1b}{}^2 + R_{1a}C_{1a}{}^2)}{(R_{1a}+R_{1b})^2\omega^2 C_{1a}{}^2 C_{1b}{}^2 + (C_{1a}+C_{1b})^2}$$

where R_{1a} and C_{1a} are the ESR and capacitance of electrolytic capacitors, and R_{1b} and C_{1b} are the ESR and capacitance of the ceramic capacitors respectively (Figure 17).

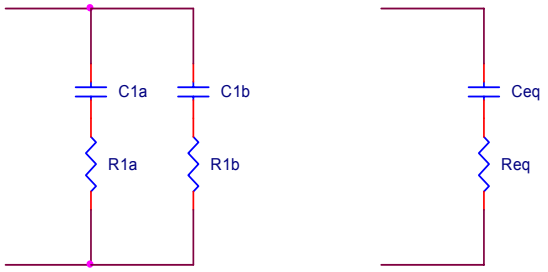

Figure 17. Equivalent RC branch.

R_{eq} and C_{eq} are both functions of frequency. For rigorous design, the equivalent ESR should be evaluated at the ripple frequency for voltage ripple calculation when both ceramic and electrolytic capacitors are used. If $R_{1a} = R_{1b} = R_1$ and $C_{1a} = C_{1b} = C_1$, then R_{eq} and C_{eq} will be frequency-independent and

$$R_{eq} = 1/2\ R_1 \text{ and } C_{eq} = 2C_1.$$

Input Capacitor (C_{in}) in Step-down Sections

The input supply to the converter usually comes from a pre-regulator. Since the input supply is not ideal, input capacitors are needed to filter the current pulses at the switching frequency. A simple buck converter is shown in Figure 18.

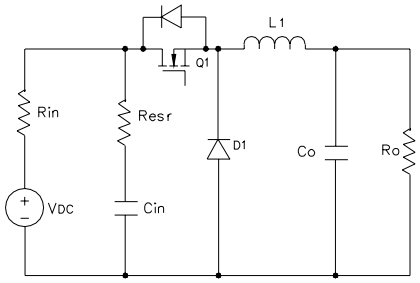

Figure 18. Buck converter input model

As shown in Fig. 18, the internal DC input voltage source

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impedance is R_{in} and the input capacitor C_{in} has an ESR denoted as R_{esr}. MOSFET and input capacitor current waveforms, ESR voltage ripple and input voltage ripple are shown in Figure 19.

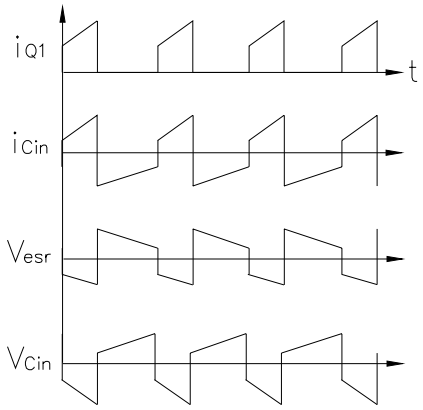

Figure 19. Typical waveforms at the input of a buck converter.

It can be seen that the current in the input capacitor pulses with high di/dt. Capacitors with low ESL should be used. It is also important to place the input capacitor close to the MOSFET's on the PC board to reduce trace inductances around the pulse current loop.

The RMS value of the capacitor current is approximately

$$I_{Cin} = I_o\sqrt{D[(1+\frac{\delta^2}{12})(1-\frac{D}{\eta})^2+\frac{D}{\eta^2}(1-D)]}.$$

The power losses at the input capacitors is then

$$P_{Cin} = I_{Cin}{}^2 R_{esr}.$$

For reliable operation, the maximum power dissipation in the capacitors should not result in more than 10°C of temperature rise. Many manufacturers specify the maximum allowable ripple current (ARMS) rating of the capacitor at a given ripple frequency and ambient temperature. The input capacitance should be high enough to handle the ripple current. For higher power applications, multiple capacitors are placed in parallel to increase the ripple current handling capability.

Sometimes meeting tight input voltage ripple specifications may require the use of larger input capacitance. At full load, the peak-to-peak input voltage ripple due to the ESR is

$$\Delta v_{ESR} = R_{esr}(1+\frac{\delta}{2})I_o.$$

The peak-to-peak input voltage ripple due to the capacitor is

$$\Delta v_C \approx \frac{DI_o}{C_{in}f_s}.$$

From these two expressions, C_{in} can be found to meet the input voltage ripple specification. In a multi-phase converter, channel interleaving can be used to reduce ripple. The two step-down channels of the SC2441A operate at 180 degrees from each other. If both step-down channels in the SC2441A are connected in parallel, both the input and the output RMS currents will be reduced.

Ripple cancellation effect of interleaving allows the use of smaller input capacitors. When converter outputs are connected in parallel and interleaved, smaller inductors and capacitors can be used for each channel. The total output ripple-voltage remains unchanged. Smaller inductors speeds up output load transient.

When two channels with a common input are interleaved, the total DC input current is simply the sum of the individual DC input currents. The combined input current waveform depends on duty ratio and the output current waveform. Assuming that the output current ripple is small, the following formula can be used to estimate the *RMS* value of the ripple current in the input capacitor.

Let the duty ratios and output currents of Channel 1 and Channel 2 be D_1, D_2 and I_{o1}, I_{o2} respectively.

If $D_1<0.5$ and $D_2<0.5$, then

$$I_{Cin} \approx \sqrt{D_1 I_{o1}{}^2 + D_2 I_{o2}{}^2}.$$

If $D_1>0.5$ and $(D_1-0.5) < D_2<0.5$, then

$$I_{Cin} \approx \sqrt{0.5 I_{o1}{}^2 + (D_1-0.5)(I_{o1}+I_{o2})^2 + (D_2-D_1+0.5) I_{o2}{}^2}.$$

If $D_1>0.5$ and $D_2 < (D_1-0.5) < 0.5$, then

$$I_{Cin} \approx \sqrt{0.5 I_{o1}{}^2 + D_2(I_{o1}+I_{o2})^2 + (D_1-D_2-0.5) I_{o2}{}^2}.$$

If D_1>0.5 and D_2 > 0.5, then

$$I_{Cin} \approx \sqrt{(D_1 + D_2 - 1)(I_{o1} + I_{o2})^2 + (1 - D_2)I_{o1}^2 + (1 - D_1)I_{o2}^2}.$$

Power MOSFET Selection and Gate Drive

Main considerations in selecting the MOSFET's are power dissipation, cost and packaging. Switching losses and conduction losses of the MOSFET's are directly related to the total gate charge (C_g) and channel on-resistance ($R_{ds(on)}$). In order to judge the performance of MOSFET's, the product of the total gate charge and on-resistance is used as a figure of merit (FOM). Transistors with the same FOM follow the same curve in Figure 20.

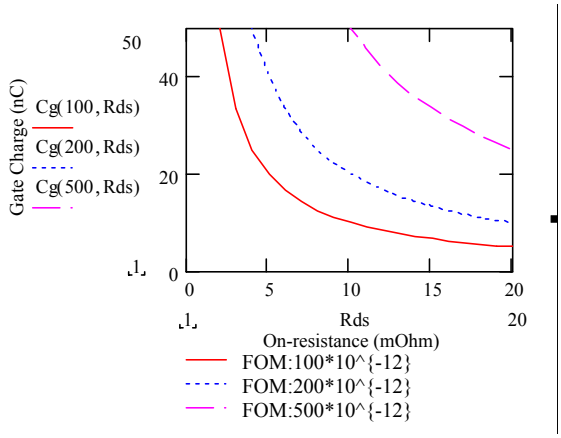

Figure 20. Figure of merit curves.

The closer the curve is to the origin, the lower is the FOM. This means lower switching loss or lower conduction loss or both. It is difficult to find MOSFET's with both low C_g and low $R_{ds(on)}$. Usually a trade-off between $R_{ds(on)}$ and C_g has to be made.

MOSFET selection also depends on applications. In many applications, either switching loss or conduction loss dominates for a particular MOSFET. For synchronous buck converters with high input to output voltage ratios, the top MOSFET is hard switched but conducts with very low duty cycle. The bottom switch conducts at high duty cycle but switches at near zero voltage. For such applications, MOSFET's with low C_g are used for the top switch and MOSFET's with low $R_{ds(on)}$ are used for the bottom switch.

The losses in power MOSFET's consist of
a) conduction loss due to the channel resistance $R_{ds(on)}$,
b) switching loss due to the switch rise time t_r and fall time t_f and
c) the gate loss due to the gate resistance R_G.

Top Switch:
The RMS value of the top switch current is

$$I_{Q1,rms} = I_o\sqrt{D(1+\tfrac{\delta^2}{12})}.$$

Its conduction loss is then

$$P_{tc} = I_{Q1,rms}^2 R_{ds(on)}.$$

$R_{ds(on)}$ varies with temperature and gate-source voltage. Curves showing $R_{ds(on)}$ variations can be found in manufacturers' data sheet. From the Si7882DP datasheet, $R_{ds(on)}$ is less than 4.5mOhm when V_{gs} is greater than 5V. However $R_{ds(on)}$ increases by nearly 40% as the junction temperature increases from 25°C to 125°C.

The switching losses can be estimated using the simple formula

$$P_{ts} = \tfrac{1}{2}(t_r + t_f)(1+\tfrac{\delta}{2})I_o V_{in} f_s.$$

where t_r is the rise time and t_f is the fall time of the switching process. To clarify these, we sketch the typical MOSFET switching characteristics under clamped inductive mode in Figure 21.

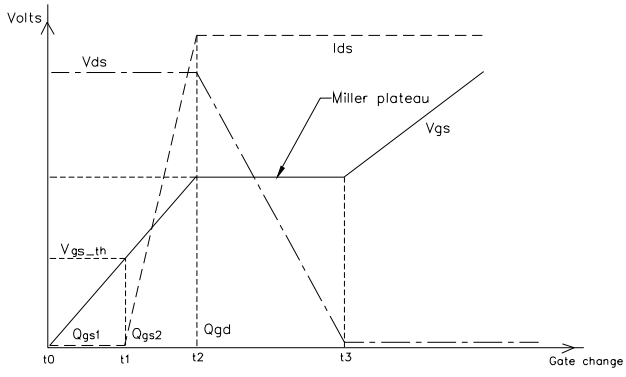

Figure 21. MOSFET switching characteristics

Applications Information

In Figure 21,

Q_{gs1} is the gate charge needed to bring the gate-to-source voltage V_{gs} to the threshold V_{gs_th},
Q_{gs2} is the additional gate charge required for the switch current to reach its full-scale value I_{ds} and
Q_{gd} is the charge needed to charge gate-to-drain (Miller) capacitance when V_{ds} is falling.
Switching losses occur during the time interval [t_1, t_3]. Defining $t_r = t_3 - t_1$. t_r can be approximated as

$$t_r = \frac{(Q_{gs2} + Q_{gd})R_{gt}}{V_{cc} - V_{gsp}}.$$

where R_{gt} is the total resistance from the driver supply rail to the gate of the MOSFET. It includes the gate driver internal impedance R_{gi}, external resistance R_{ge} and the gate resistance R_g within the MOSFET i.e.

$$R_{gt} = R_{gi} + R_{ge} + R_g.$$

V_{gsp} is the Miller plateau voltage shown in Figure 21. Similarly an approximate expression for t_f is

$$t_f = \frac{(Q_{gs2} + Q_{gd})R_{gt}}{V_{gsp}}.$$

Only a portion of the total losses $P_g = Q_g V_{cc} f_s$ is dissipated in the MOSFET package. Here Q_g is the total gate charge specified in the datasheet. The power dissipated within the MOSFET package is

$$P_{tg} = \frac{R_g}{R_{gt}} Q_g V_{cc} f_s.$$

The total power loss of the top switch is then

$$P_t = P_{tc} + P_{ts} + P_{tg}.$$

If the input supply of the power converter varies over a wide range, then it will be necessary to weigh the relative importance of conduction and switching losses. This is because conduction loss is inversely proportional to the input voltage. Switching loss however increases with the input voltage. The total power loss of MOSFET should be calculated and compared for high-line and low-line cases. The worst case is then used for thermal design.

Bottom Switch:

The RMS current in bottom switch can be calculated

$$I_{Q2,rms} = I_o \sqrt{(1-D)(1+\tfrac{\delta^2}{12})}.$$

The conduction loss is then

$$P_{bc} = I_{Q2,rms}{}^2 R_{ds(on)},$$

where $R_{ds(on)}$ is the channel resistance of bottom MOSFET. If the input voltage to output voltage ratio is high (e.g. V_{in}=12V, V_o=1.5V), the duty ratio D will be small. Since the bottom switch conducts with duty ratio (1-D), the corresponding conduction losses can be quite high.
Due to non-overlapping conduction between the top and the bottom MOSFET's, the internal body diode or the external Schottky diode across the drain and source terminals always conducts prior to the turn on of the bottom MOSFET. The bottom MOSFET switches on with only a diode voltage between its drain and source terminals. The switching loss

$$P_{bs} = \tfrac{1}{2}(t_r + t_f)(1+\tfrac{\delta}{2}) I_o V_d f_s$$

is negligible due to near zero-voltage switching.

The gate loss is estimated as

$$P_{bg} = \frac{R_g}{R_{gt}} Q_g V_{cc} f_s.$$

The total bottom switch loss is then

$$P_b = P_{bc} + P_{bs} + P_{bg}.$$

Once the power losses P_{loss} for the top (P_t) and bottom (P_b) MOSFET's are known, thermal and package design at component and system level should be done to verify that the maximum die junction temperature ($T_{j,max}$, usually 125°C) is not exceeded under the worst-case conditions. The equivalent thermal impedance from junction to ambient (θ_{ja}) should satisfy

$$\theta_{ja} \le \frac{T_{j,max} - T_{a,max}}{P_{loss}}.$$

θ_{ja} depends on the die to substrate bonding, packaging material, the thermal contact surface, thermal compound property, the available effective heat sink area and the air flow condition (free or forced convection). Actual temperature measurement of the prototype should be carried out to verify the thermal design.

Integrated Power MOSFET Drivers

There are four internal MOSFET drivers in a dual-channel step-down converter.

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Using low gate charge MOSFETs reduces switching loss. It is possible to trade driver IC losses for MOSFET switching losses by adjusting the gate resistance. Lower gate resistance results in higher gate driving current and faster MOSFET switching. However the driver incurs higher losses. Conversely higher gate drive resistance limits the gate drive current, thus lowering the driver dissipation. MOSFET switching loss is higher.

To prevent shoot-through between the top and the bottom MOSFETs during commutation, one MOSFET should be completely turned off before the other is turned on. The SC2441A uses adaptive non-overlapping timing to prevent shoot-through.

Optimize MOSFET Driving Voltage

The on-state DC resistance of a MOSFET, R_{DS_ON}, is determined by its gate to source voltage. The higher the V_{GS}, the lower the R_{DS_ON} will be. Once the gate-source voltage exceeds a certain level, the R_{DS_ON} becomes relatively constant. There is no benefit except higher dissipation if you further increase the MOSFET gate drive voltage. It is recommended to select gate drive voltage (V_{CC} pin) of the SC2441A in between 5V to 7V.

Setting the Output Voltage of the Step-down Section

The non-inverting inputs of the error amplifiers are internally biased to 0.5V voltage reference. A simple voltage divider (R_{o1} at top and R_{o2} at bottom) sets the converter output voltage. R_{o2} can be expressed as a function of the voltage feedback gain h=0.5/V_o and R_{o1}

$$R_{o2} = \frac{h}{1-h} R_{o1.}$$

caused by the feedback voltage divider ratio. It cannot be corrected by the feedback loop.

Once either R_{o1} or R_{o2} is chosen, the other can be calculated for the desired output voltage V_o. Since the number of standard resistance values is limited, the calculated resistance may not be available as a standard value resistor. As a result, there will be a set error in the converter output voltage. This non-random error is

The following table lists a few standard resistor combinations for realizing some commonly used output voltages.

Vo (V)	**0.6**	0.9	**1.2**	**1.5**	1.8	2.5	3.3
(1-h)/h	**0.2**	0.8	**1.4**	**2**	2.6	4	5.6
Ro1 (Ohm)	**200**	806	**1.4K**	**2K**	2.61K	4.02K	5.62K
Ro2 (Ohm)	**1K**	1K	**1K**	**1K**	1K	1K	1K

Only the voltages in boldface can be precisely set with standard 1% resistors.

The input bias current of the error amplifier also causes an error in the output voltage. The inverting input bias currents of error amplifiers 1 and 2 are –60nA and –280nA respectively. Since the non-inverting input is biased to 0.5V, the percentage error in the second output voltage will be $-100\% \cdot (0.28\mu A) \cdot R_{o1}R_{o2}/[0.5 \cdot (R_{o1}+R_{o2})]$. To keep this error below 0.2%, $R_{o2} < 4k\Omega$.

Loop Compensation in Step-down Section

The SC2441A uses current-mode control for both step-down channels. Current-mode control is a dual-loop control system in which the inductor peak current is loosely controlled by the inner current-loop. The higher gain outer loop regulates the output voltage. Since the current loop makes the inductor appear as a current source, the complex high-Q poles of the output LC networks is split into a dominant pole determined by the output capacitor and the load resistance and a high frequency pole. This pole-splitting property of current-mode control greatly simplifies loop compensation.

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The inner current-loop is unstable (sub-harmonic oscillation) unless the inductor current up-slope is steeper than the inductor current down-slope. For stable operation above 50% duty-cycle, a compensation ramp is added to the sensed-current. In the SC2441A the compensation ramp is made duty-ratio dependent. The compensation ramp is approximately

$$V_{SLOPE}(D) = 230mV \cdot D \cdot e^{0.734 \cdot D}$$

D is the duty ratio.

The slope compensation voltage vs duty ratio is as shown in Figure 22.

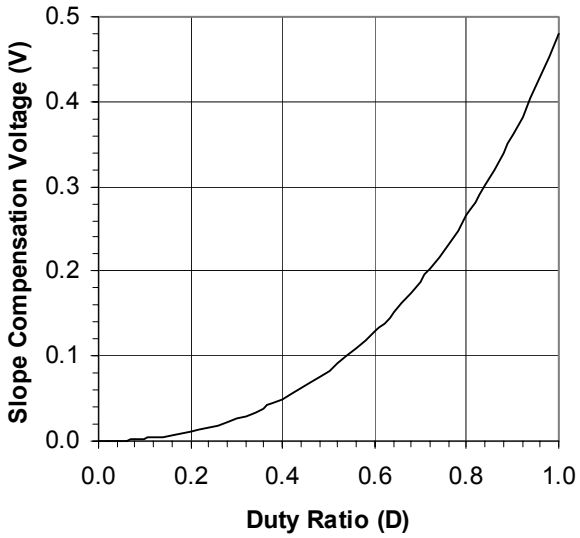

Figure 22. Slope Compensation Voltage Waveform

Illustrated as the picture above, as the duty ratio increases, the slope compensation voltage added into the control loop increases too. And the control loop including the slope compensation is shown in Figure 23.

The voltage transconductance error amplifier (shown in Figure 24) has a g_m of 315µA/V. C_2, C_3 and R_2 construct the compensation network for stable operation with optimized load transient response.

The feedback gain h and the resistor values are determined using the equations given in the “Setting the Output Voltage” section with

$$h = \frac{0.5}{V_o}.$$

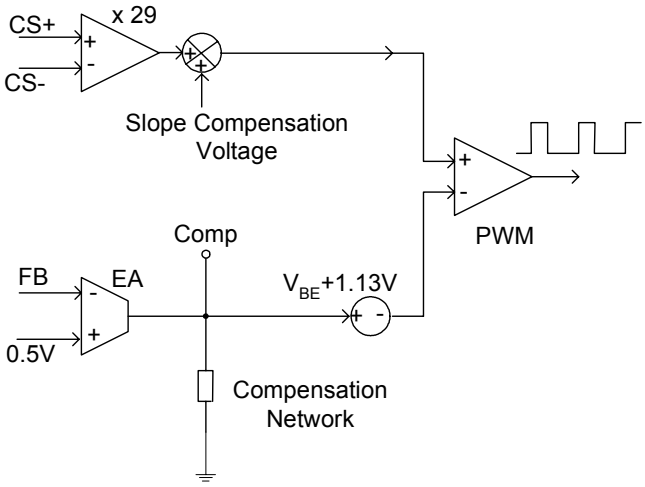

Figure 23. Control Flow Chart with Slope Compensation

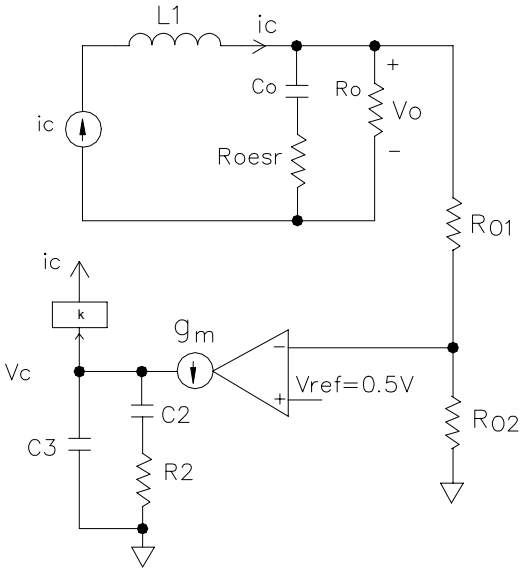

Figure 24. A simple model of current-mode buck converter

For the rated output current I_o, the first-order gain k is determined as

$$k = \frac{\Delta I_o}{\Delta V_c}.$$

k is the product of equivalent current sensing Rs and current amplifier gain Gca=29. Furthermore the transfer

Applications Information

function from the voltage error amplifier output v_c to the converter output v_o can be derived from Figure 24.

$$\frac{V_o(s)}{V_c(s)} := G_{vc}(s) = kR_o \frac{1+\frac{s}{s_{z1}}}{1+\frac{s}{s_{p1}}},$$

where the single dominant-pole is

$$s_{p1} = \frac{1}{(R_o + R_{oesr})C_o}$$

and the zero associated with the output capacitor ESR is

$$s_{z1} = \frac{1}{R_{oesr}C_o}.$$

The dominant-pole changes with the converter output load.

The controller transfer function (from the converter output v_o to the voltage error amplifier output v_c) is

$$C(s) = \frac{g_m h}{s(C_2 + C_3)} \frac{1+\frac{s}{s_{z2}}}{1+\frac{s}{s_{p2}}},$$

where

$$s_{z2} = \frac{1}{R_2 C_2}$$

and

$$s_{p2} = \frac{1}{R_2 \frac{C_2 C_3}{C_2 + C_3}}.$$

The loop transfer function is then

$$T(s)=G_{vc}(s)C(s).$$

P_2 is a pole for suppressing high-frequency switching noise. So $P_2 >> Z_2$. To simplify design, one usually assumes that $C_3<<C_2$, $R_{oesr}<<R_o$, $S_{p1}=S_{z2}$ and specifies the loop crossover frequency f_c. The loop crossover frequency determines the converter dynamic response. With these assumptions, the controller parameters are determined as follows

$$C_2 = \frac{g_m h k R_o}{2\pi f_c},$$

$$R_2 = \frac{R_o C_o}{C_2}$$

and

$$C_3 = \frac{R_{oesr} C_o}{R_2}.$$

For example, if V_{in}=3.3V, V_o=1.2V, I_o=4A, f_s=500kHz, C_o=390µF, R_{oesr}=16mΩ, one can calculate that

$$R_o = \frac{V_o}{I_o} = 300m\Omega,$$

$$h = \frac{0.5}{V_o} = 0.42$$

and

$$k = \frac{\Delta I_o}{\Delta V_c} = 2.60.$$

If the converter crossover frequency is set around 1/10 of the switching frequency, f_c=50kHz, the controller parameters then can be calculated.

$$C_2 = \frac{g_m h k R_o}{2\pi f_c} \approx 0.326nF,$$

use C_2=0.33nF.

$$R_2 = \frac{R_o C_o}{C_2} \approx 354.5k\Omega,$$

use R_2=357kΩ.

It is further calculated that

$$C_3 = \frac{R_{oesr} C_o}{R_2} \approx 17.48pF,$$

use C_3=22pF. The Bode plots of the loop transfer function (magnitude and phase) are shown in Fig. 25.

Applications Information

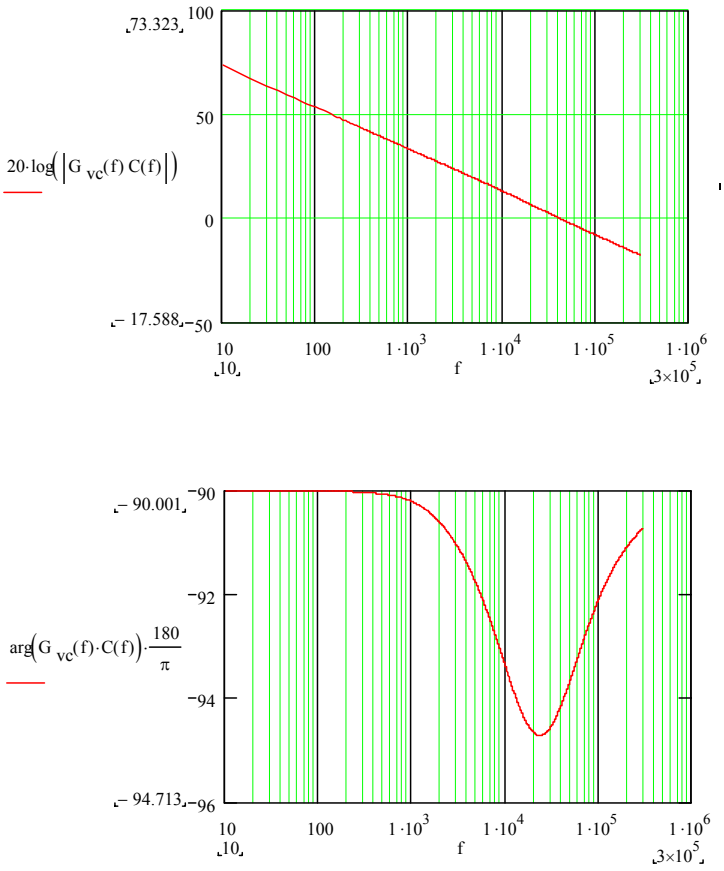

Figure 25. Bode plots of the loop response.

The resulting crossover frequency is about 49.2kHz with phase margin 90°.

If the circuit noise makes the converter jitter, a larger C_3 than the calculated value can be used. Effectively the converter bandwidth is reduced to reject high frequency noises. The final circuit should be checked for stability under load transients at different line voltages. The load transient also needs to be measured to ensure that the output voltage is within the specification window.

PC Board Layout Issues

Circuit board layout is very important for the proper operation of high frequency switching power converters. A power ground plane is required to reduce ground bounces. The followings are suggested for proper layout.

Power Stage

1) Separate the power ground from the signal ground. In SC2441A the power ground PGND1 should be tied to the source terminal of lower MOSFETs. The signal ground AGND should be tied to the negative terminal of the output capacitor (output return terminal).

2) Minimize the size of pulse current loop. Place the top MOSFET, the bottom MOSFET and the input capacitors close to each other with short and wide traces. In addition to the aluminum energy storage capacitors, add multi-layer ceramic (MLC) capacitors from the input to the power ground to improve high frequency bypass.

3) Reduce high frequency voltage ringing. Widen and shorten the drain and source traces of the MOSFETs to reduce stray inductances. Add a small RC snubber if necessary to reduce the high frequency ringing at the phase node. Sometimes slowing down the gate drive signal also helps in reducing the high frequency ringing at the phase node.

4) Shorten the gate driver path. Integrity of the gate drive (voltage level, leading and falling edges) is important for circuit operation and efficiency. Short and wide gate drive traces reduce trace inductances. Bond wire inductance is about 2~3nH. If the length of the PCB trace from the gate driver to the MOSFET gate is 1 inch, the trace inductance will be about 25nH. If the gate drive current is 2A with 10ns rise and falling times, the voltage drops across the bond wire and the PCB trace will be 0.6V and 5V respectively. This may slow down the switching transient of the MOSFETs. These inductances may also ring with the gate capacitance.

5) Put the decoupling capacitor for the gate drive power supplies (BST and VCC) close to the IC and power ground.

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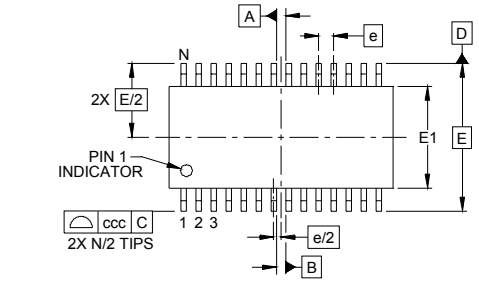
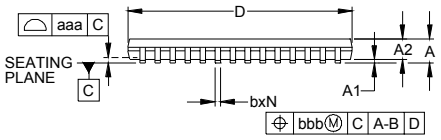
Control Section

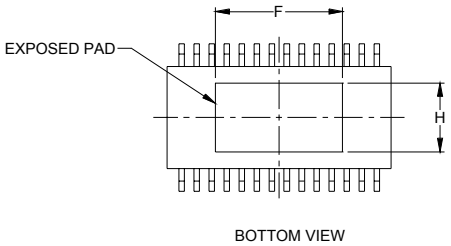
6) The frequency-setting resistor Rosc should be placed close to Pin 10. Trace length from this resistor to the analog ground should be minimized.
7) Solder the VCC decoupling capacitor next to the VCC and power ground PGND pins.
8) Place the current-sensing components away from the power circuit and close to the corresponding CS+ and CS- pins. Use X7R type ceramic capacitors for current sensing due to their thermal stability. The distance between the two trace should be as close as possible to minize the noise pick-up.
9) Use an isolated local ground plane for the controller and tie it to the negative side of output capacitor bank.
10) A large copper area underneath the SC2441A IC is nessary for heat sinking purpose. And multiple layers of large copper area connected through vias can be used for better thermal performance. The size of the vias as the connection between multiple layers should not be too large or solder may seep through the big vias to the the bottom layer during the re-flow process.

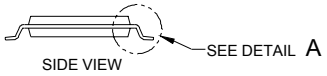
Outline Drawing - TSSOP-28

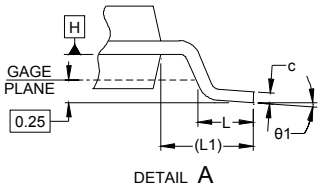




DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.000	-	.006	0.00	-	0.15
A2	.031	-	.041	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.008	0.09	-	0.20
D	.378	.382	.386	9.60	9.70	9.80
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
F	.210	.216	.220	5.35	5.50	5.60
H	.112	.118	.122	2.85	3.00	3.10
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	28			28		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		



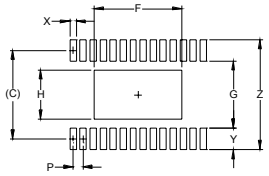




NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AET.

Land Pattern - TSSOP-28



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
F	.224	5.70
G	.161	4.10
H	.126	3.20
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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