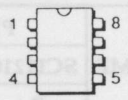
FEATURES

- ☐ 8 pin PDIP Version for Small Size
- ☐ Power Down Circuitry
- ☐ Selectable Energy Detection
- ☐ Energy Detection can be used as Call Progress Filter
- ☐ FSK Demodulator

GENERAL DESCRIPTION

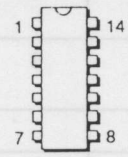
The SC11210 and SC11211 are analog front ends which can be used to support the Caller Number Delivery (CND) feature in a General Switched Telephone Network (GSTN). This service is provided by the telephone company and is intended for residential and business telephone customers. It allows called customers to receive a calling party's number during the ringing cycle. The data corresponding to the caller number is transmitted to the customer premises when the telephone is on-hook and a voice path has been established. If power ringing is used to establish the voice path, then data transmission occurs during the silent interval between the first and second power ringing signal. Sierra's SC11210 and SC11211 are designed to interface to the signalling scheme that is shown in Table 1.

8-PIN DIP PACKAGE



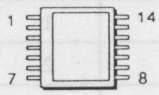
SC11210CN

14-PIN DIP PACKAGE



SC11211CN

14-PIN SOIC PACKAGE



SC11211CM

Link Type	Simplex, two wire
Transmission Scheme	Analog, phase-coherent frequency shift keying (FSK)
Logical 1 (Mark)	1200 ±12 Hz
Logical 0 (Space)	2200 ±22 Hz
Transmission Rate	1200 bps
Application of Data	Serial, binary, asynchronous
Transmission Level	–13.5 ±1 dBm at the point of data application into a resistive load of 900 Ω
Insertion Loss @ 3KHz	10–14dB

Table 1. Caller I.D. Signaling Scheme

BLOCK DIAGRAM

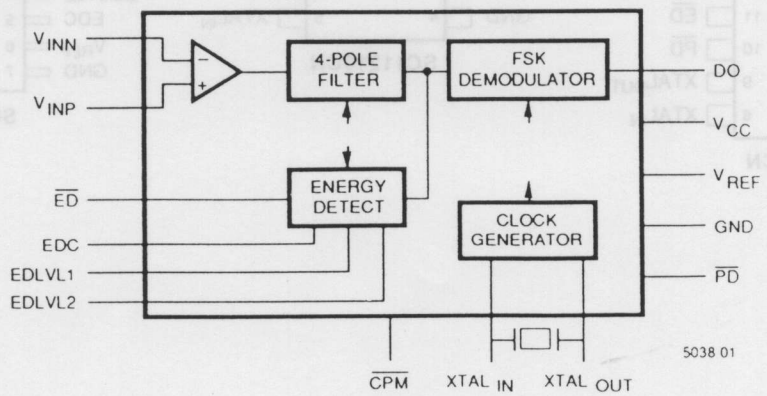


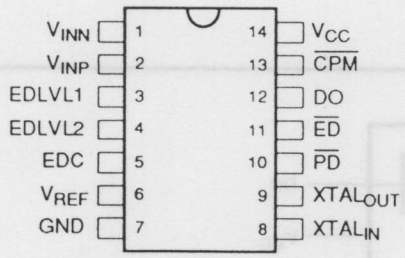
Figure 1.

PIN DESCRIPTIONS

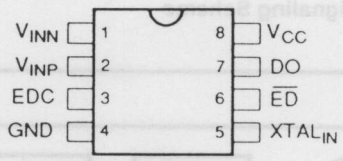
The chip is available in an 8 or 14 pin package. Only the 14 pin version supports the power-down and call progress detect function and has four energy detect levels. The following is a description of the pins.

PIN NAME	PIN NO. SC11210 P_1	PIN NO. SC11211 P_2, P_3	DESCRIPTION
$\overline{CPM}$		13	Call progress control pin. When pulled low the input bandpass filter shifts center frequency and bandwidth.
DO	7	12	The output of the FSK demodulator appears at this pin.
$\overline{ED}$	6	11	Energy-Detect output. Goes low when inband energy is present and detected by the energy detect circuit.
EDC	3	5	Energy-Detect Capacitor. A 0.1 µF capacitor should be connected between this pin and ground.
EDLVL1		3	Energy detect level control one.
EDLVL2		4	Energy detect level control two.
GND	4	7	Ground pin (0V).
$\overline{PD}$		10	Power-down pin. When pulled low the chip will enter a sleep mode to reduce power consumption.
V_{CC}	8	14	Positive power supply pin (4.5–5.5 Volts).
V_{INN}	1	1	Negative input of differential input buffer.
V_{INP}	2	2	Positive input of differential input buffer.
V_{REF}		6	Reference ground pin. For improved performance a 1 µF capacitor should be connected between this pin and ground. This voltage is nominally halfway between the positive and ground.
$XTAL_{IN}$	5	8	The input pin of the oscillator.
$XTAL_{OUT}$		9	The output pin of the oscillator.

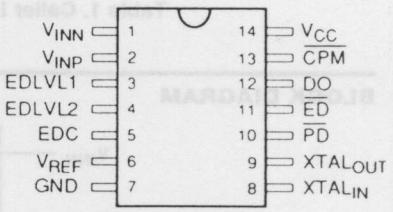
NOTE: P_1 is the 8 pin dip, P_2 is the 14 pin dip, P_3 is the 14 pin SOIC.



SC11211CN



SC11210CN



SC11211CM

CIRCUIT DESCRIPTION

The Caller Identification Circuit is a CMOS device that operates with a single power supply over a range of 4.5–5.5 Volts. A block diagram of the chip is shown in Figure 1. It consists of an input differential buffer, a 4-pole bandpass filter, an FSK demodulator, a user selectable energy detect circuit , a clock generator, and a power down feature. The frequency response for the bandpass filter is shown in Figures 3a and 3b. In a typical application, the circuit accepts the incoming FSK signals through the differential input buffer, which in turn is passed through the 4 pole band pass filter. Depending on the setting of the energy detect pins (see Table 1), $\overline{ED}$ will go low when enough in-band energy is present or high when the energy level of the signal is insufficient. The chip accepts a 3.5795454 MHz clock or a crystal (see Figure 4) and uses it to generate timing for the internal blocks. The chip has a power-down mode which is controlled by the $\overline{PD}$ pin. When this pin is pulled low the power-down feature is activated. The device is available in an 8 or 14 pin package. The 8 pin version has one energy detect level and does not support the call progress detection function and the power down feature.

Analog Input Section

The analog input section accepts a differential signal which should be AC coupled to the V_{INN} and V_{INP} pins. Since the chip operates with a single power supply, an analog reference ground is generated internally which is nominally halfway between the positive supply and ground. To preserve approximately the same internal and external DC levels, the circuit of Figure 2 should be used for AC coupling the differential signal to the input pins.

Energy Detect Circuit

The energy detect circuit takes its input from the output of the bandpass filter. It rectifies the signal and uses an averaging circuit to determine the energy level. It needs an external capacitor for its operation. With the external capacitor equal to 0.1 µF, the on-to-off and off-to-on response times of the energy detect will nominally be 5 mS. The energy detect level has four distinct values and is controlled by the two EDLVL1 and EDLVL2 pins according to the listings in Table 2.

These levels are valid for the positive power supply equal to 5V DC. In the 8 pin package the EDLVL1 and EDLVL2 pins are not available and they are held low with internal pulldowns. Therefore in the 8 pin package the only available energy detect level is –30 dBm.

Power-Down Mode

In the 14 pin package the $\overline{PD}$ pin controls the power-down function. When this pin is pulled low the chip will be power-downed and the supply current will reach to its minimum level and the oscillator is inactive. In the 8 pin package this pin is not available and it is held high with an internal pullup.

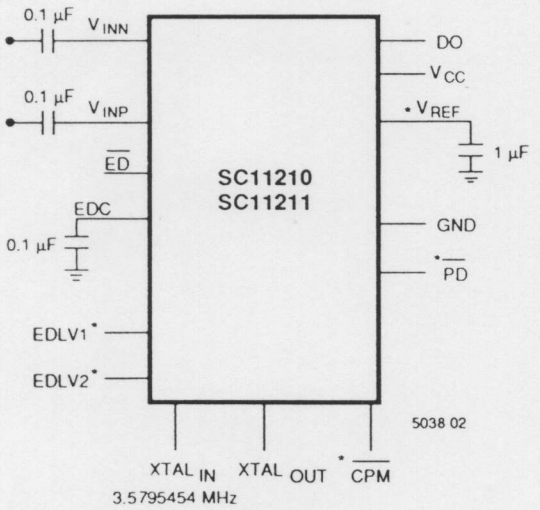


Figure 2.

*SC11211 Only

EDLVL2	EDLVL1	DETECT LEVEL[1]
0 (or open)	0 (or open)	–30 dBm on –35 dBm off
0 (or open)	1	–27 dBm on –32 dBm off
1	0 (or open)	–24 dBm on –29 dBm off
1	1	–21 dBm on –26 dBm off

NOTE 1: dBm = decibels above or below a reference power of 1 mW into a 600Ω load.

Table 2. Energy detection levels

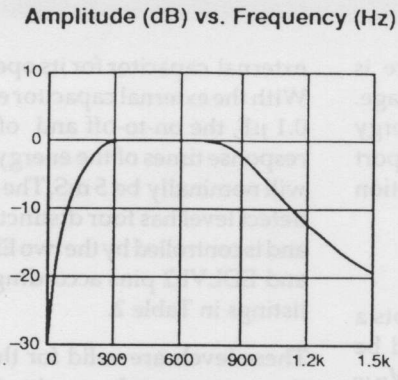


Figure 3a. Band Pass Filter in Call Progress Monitor Mode

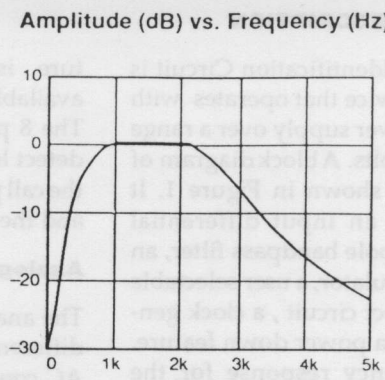


Figure 3b. Band Pass Filter in Caller Number Delivery Mode

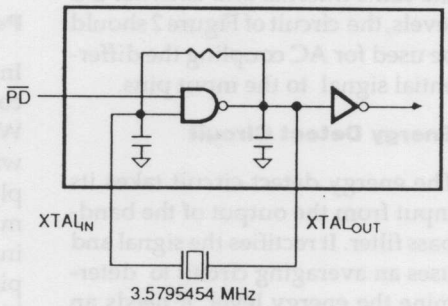


Figure 4. Typical Crystal Connection

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, & 3)

Supply Voltage, V_{CC} – GND	+6V
Voltage on any Pin	GND – 0.3 to V_{CC} + 0.3 V
Current at any Pin	10 mA
Storage Temperature	–65 to +150°C
Power Dissipation (Note 3)	100 mW
Lead Temperature (Soldering 10 sec)	300°C

OPERATING CONDITIONS (Note 4)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
GND	Ground			0		V
F_C	Crystal Frequency		3.576	3.579545	3.583	MHz

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.

NOTE 2: Unless otherwise specified all voltages are referenced to ground.

NOTE 3: Power dissipation temperature derating: Plastic package: –12mW/C from 65°C to 85°C.
Ceramic package: –12mW/C from 100°C to 125°C.

NOTE 4: Min and max values are valid over the full temperature and operating voltage range. Typical values are for 25°C and 5 V operations.

DC ELECTRICAL CHARACTERISTICS (Notes 1 and 2)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
V_{CC}	Operating Supply Voltage		4.5		5.5	V
I_{CC}	Operating Supply Current				7	mA
P_O	Power Consumption $\overline{PD}$ = 1	f = 3.579 MHz; V_{CC} = 5 V			35	mW
PD	Power Consumption $\overline{PD}$ = 0				15	µA
INPUTS						
V_{IL}	Low Level Input Voltage				.8	V
V_{IH}	High Level Input Voltage		2			V
I_{IH}/I_{IL}	Input Leakage Current	V_{IN} = GND or V_{CC}		0.1		µA
$\overline{PD}$	Pull Up (Source) Current			100		µA
EDLVL	Pull Down (Sink) Current			100		µA
CLK_{IN}	Load Capacitance			20		pF
CLK_{IN}	High Level Input Leakage Current		3	50	µA	
CLK_{IN}	Low Level Input Leakage Current		3	50	µA	
OUTPUTS						
I_{OL}	Output Low (Sink) Current	V_{OUT} = 0.4 V	1.0	2.5		mA
I_{OH}	Output High (Source) Current	V_{OUT} = 4.6 V	0.4	0.8		mA
CLK_{OUT}	Driving Capacitance				100	µA
CLK_{OUT}	High Level	V_{OUT} = 2.8V			200	µA
CLK_{OUT}	Low Level	V_{OUT} = 0.4V			20	pF

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.

NOTE 2: Unless otherwise specified all voltages are referenced to ground.

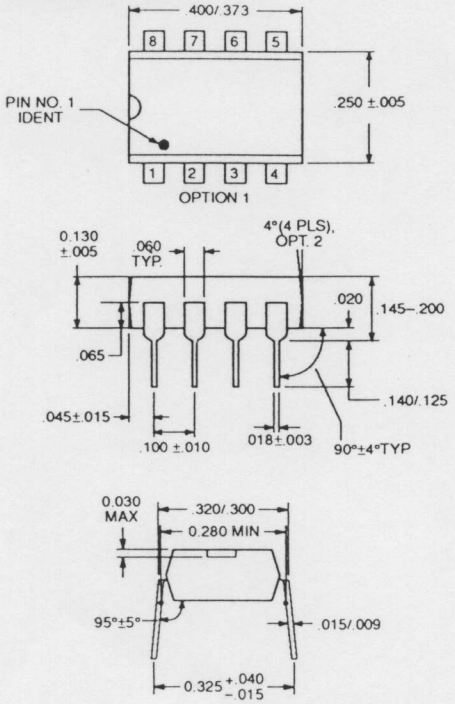
AC CHARACTERISTICS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{INT} to GND	Impedance ($\overline{PD}$ = 1)	75	100	125	kΩ
V_{INR} to GND	Impedance ($\overline{PD}$ = 0)		3.3		kΩ
V_{INT} to	Impedance ($\overline{PD}$ = 1)	150	200	250	kΩ
V_{INR}	Impedance ($\overline{PD}$ = 0)		6.6		kΩ
V_{INT} V_{INR}	Differential Voltage on High Input Imp. ($\overline{PD}$ = 1)	24.5			mV[1]
V_{INT} V_{INR}	Differential Input Level into 600Ω ($\overline{PD}$ = 1)	–30			dBm[1]
V_{INT} V_{INR}	Voltage on either tip or ring (14 to 65 Hz) ($\overline{PD}$ = 0)	600			mVRMS

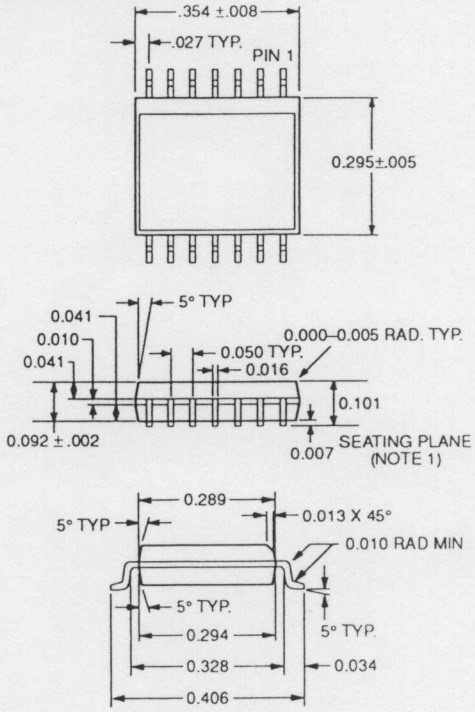
NOTE 1: Maximum Differential Input Voltage Peak to Peak: 0.75 V

PHYSICAL DIMENSIONS

Package 8-Lead Molded DIP



Package 14-Lead SOIC



Package 14-Lead Molded DIP