FILE - SIERRA DATA

PRELIMINARY

SIERRA SEMICONDUCTOR

SC11086/SC11196
Facsimile Modem Analog Processor

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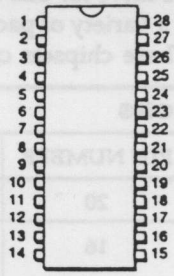
FEATURES

- SC11086 Supports CCITT Group 3 Facsimile
- SC11196 Supports CCITT Groups 1, 2 & 3
- Internal Hybrid
- Direct Interface to SC11006, SC11026 MAPs
- Compatible with CCITT V.27, V.27ter, V.29
- Internal constellation pattern DACs
- Cable compensation selectable
- Ring Detector
- Dynamic Range -47dBm to 0dBm
- Programmable transmit levels to +5dBm ±1dB
- Power consumption 240mW typical
- 10 bit ADC & DAC voice band sampling

28-PIN DIP PACKAGE



SC11196CN

GENERAL DESCRIPTION

40-PIN QFP PACKAGE

28-PIN PLCC PACKAGE

The SC11196 and SC11086 are Facsimile Modem Analog Processors (FMAP) designed to work with Sierra's SC11198 series DSP ICs to form a 9600 bps data pump. The combination of FMAC and DSP provides a register compatible replacement for the Rockwell 96MD fax data pump. The chipset offers sev-

PRELIMINARY

BLOCK DIAGRAM

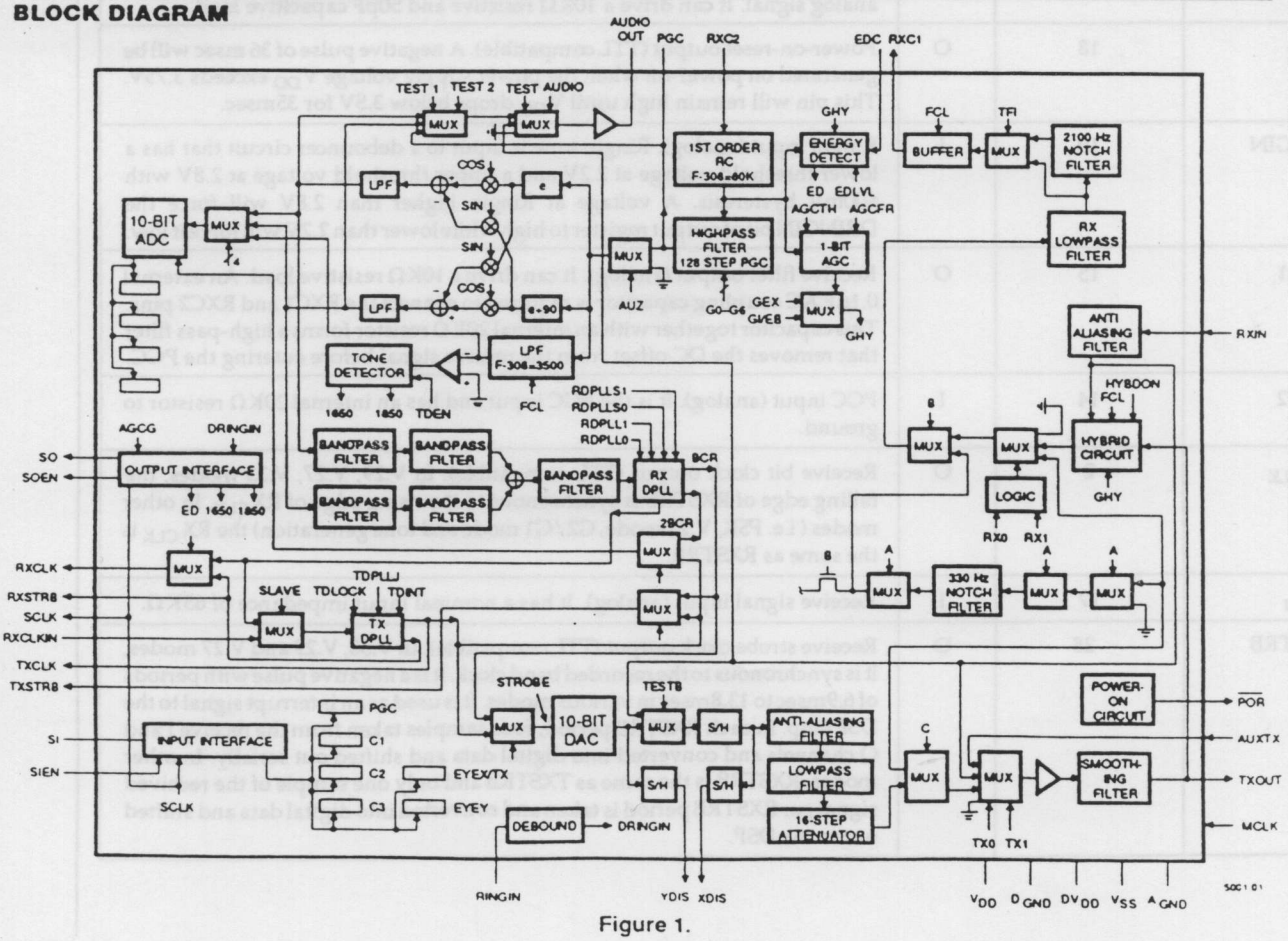


Figure 1.

GENERAL DESCRIPTION (continued)

eral advantages including internal hybrid, DTMF detection, voice mail modes, direct line drive for dial up applications and a variety of packaging options. These chipsets can also be combined with Sierra data modem kits to form EIA Class 2 fax and data modems supporting the developing standard PN2388 command set as well as AT commands for data modems. Versions to support V.42bis, MNP5 and other protocols are available. Please consult the SC11196 series data sheet for further details of the chip set.

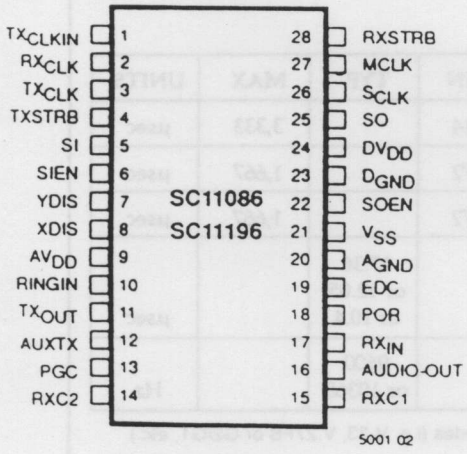
PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
A_{GND}	20	P	Analog ground input; A_{GND} = 0V.
AUDIO-OUT	16	O	Audio signal output (analog). The receive signal is passed through a unit gain buffer which can drive 10KΩ resistive load. It drives an external gain amplifier to drive a speaker for line monitoring.
AUXTX	12	I	Auxillary transmit signal input (analog). It can be summed up with the transmit signal or it can be sent directly to the TXOUT pin.
AV_{DD}	9	P	Analog positive power supply input; AV_{DD} = +5V ±10%.
D_{GND}	23	P	Digital ground input; D_{GND} = 0V.
DV_{DD}	24	P	Digital positive power supply input; DV_{DD} = +5V +±10%.
EDC	19	O	Energy detect capacitor input (analog). An external 0.47µF capacitor should be connected between this pin and A_{GND} pin.
MCLK	27	I	Master clock input (TTL compatible). Its frequency must be 9.792MHz. This clock is used to generate various timing signals for internal and external use.
PGC	13	O	Programmable Gain Control (PGC) output (analog). It is a sampled and held analog signal. It can drive a 10KΩ resistive and 50pF capacitive load.
POR	18	O	Power-on-reset output (TTL compatible). A negative pulse of 36 msec will be generated on power-on when the power supply voltage V_{DD} exceeds 3.75V. This pin will remain high until V_{DD} drops below 3.5V for 35msec.
RINGIN	10	I	Ringin input (analog). Ringin tone is input to a debouncer circuit that has a lower threshold voltage at 2.2V and a upper threshold voltage at 2.8V with 600mV hysteresis. A voltage at Ringin higher than 2.8V will force the DRINGIN bit of output register to high while lower than 2.2V will force it low.
RXC1	15	O	Receive filter output (analog). It can drive a 10KΩ resistive load. An external 0.1µF AC coupling capacitor is required to connect the RXC1 and RXC2 pins. This capacitor together with an internal 20KΩ resistor forms a high-pass filter that removes the DC offset from the receive signal before entering the PGC.
RXC2	14	I	PGC input (analog). It is the PGC input and has an internal 20KΩ resistor to ground.
RX_{CLK}	2	O	Receive bit clock output (TTL compatible). In V.29, V.27, V.33 modes, the falling edge of RXSTRB is synchronous to the rising edge of RX_{CLK}. In other modes (i.e. FSK, V.21 mode, G2/G1 mode and tone generation) the RX_{CLK} is the same as RXSTRB.
RX_{IN}	17	I	Receive signal input (analog). It has a nominal input impedance of 65KΩ.
RXSTRB	28	O	Receive strobe clock output (TTL compatible). In V.33, V.29 and V.27 modes, it is synchronous to the recorded band clock. It is a negative pulse with periods of 6.9msec to 13.8msec in various modes. It is used as an interrupt signal to the DSP chip. In each RXSTRB period, four samples taken from the receive I and Q channels and converted into digital data and shifted out serially. In other modes, RXSTRB is the same as TXSTRB and only one sample of the received signal per RXSTRB period is taken and converted into digital data and shifted out to the DSP.

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
S_{CLK}	26	O	Shift clock output (TTL compatible). Its frequency is 1/4 of MCLK. Its duty cycle is 50%. It is used for serially shifting both transmit and receive data in and out of the chip.
SI	5	I	Serial data input (TTL compatible). Input data is shifted serially into a 13-bit register by using the falling edge of S_{CLK}. The three most significant bits (D12-D10) destinate the contents of 10 least significant bits (D9-D0) into data/control register. The MSB is shifted in first.
SIEN	6	I	Serial enable input (TTL compatible). It enables the writing of serial data into the 13-bit input register.
SO	25	O	Serial data output (TTL compatible). Output 16 bit data is shifted out serially by using the rising edge of SCLK. The ten most significant bits (D15-D6) correspond to the ADC output data. The next five bits (D5-D1) correspond to various status bits, such as D5 corresponds to ED output, D4 to AGCG output, D3 to DRINGIN output, D2 to 1650Hz tone detected and D1 to 1850Hz tone detected. The LSB (D0) is a don't care.
SOEN	22	O	Serial enable output (TTL compatible). A positive pulse enables the 16 bit data stored in a receive shift register to be read out serially through the SO pin.
TX_{CLK}	3	O	Transmit bit clock output (TTL compatible). It is synchronous to the TX_{CLKIN} in the external clock mode. In the free run (internal) mode it is derived from the crystal clock.
TX_{CLKIN}	1	I	External transmit clock input (TTL compatible). It is for the input clock of the transmit phase-locked loop.
TXSTRB	4	O	Transmit strobe clock output (TTL compatible). It is used to interrupt the DSP to transfer transmit eye-x/eye-y or control data. In G2/G1 mode TXSTRB is 10.368kHz. It is 9600Hz in all other modes.
TX_{OUT}	11	O	Transmit signal output (analog); It can drive a 600Ω resistive load directly.
V_{SS}	21	P	Negative power supply input; V_{SS} = -5V ± 10%.
XDIS	8	O	Eye-X display output (analog); 10 bits D/A output from Eye-X register.
YDIS	7	O	Eye-Y display output (analog); 10 bits D/A output from eye-Y register. Both X and Y data word are written into the chip within a given strobe period and they will appear simultaneously at XDIS and YDIS two strobes later.

CONNECTION DIAGRAMS



SC11086/SC11196 INTERFACE TIMING I

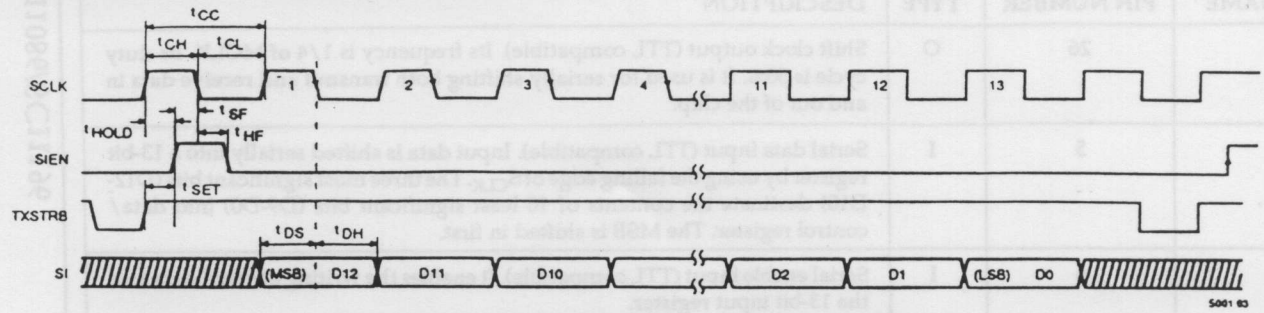


Figure 2. Serial Input Timing with Respect to TXSTRB

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{CC}	Cycle Time of SCLK		408		ns
t_{CH}	SCLK High Period		204		ns
t_{CL}	SCLK Low Period		204		ns
t_{HOLD}	Holding Time From SCLK High to SIEN High	0			ns
t_{SF}	Set up Time From SIEN High to SCLK low	50			ns
t_{HF}	Holding Time From SCLK Low to SIEN low	100			ns
t_{SET}	Set up Time from TXSTRB High to SIEN High	0			ns
t_{DS}[1]	Data Setup Time with Respect to SCLK Low	104			ns
t_{DH}	Data Hold Time with Respect to SCLK Low			304	ns

NOTE 1: Only 13 bits of data are written serially into an internal shift register between two consecutive SIEN high pulses. It latches data which appear on the SI line using the falling edge of SCLK. The first three MSBs of D12, D11 and D10 represent a unique address of various internal data/control registers. The MSB is shifted in first.

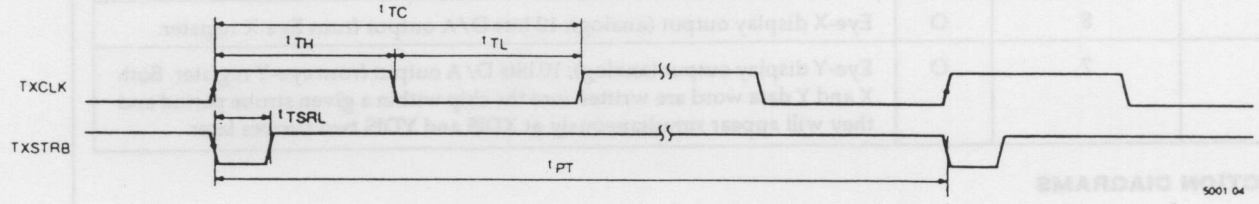


Figure 3. Transmit Clock Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{TC}[1]	Cycle Time of TXCLK	69.44		3,333	µsec
t_{TH}[2]	TXCLK High Period	34.72		1,667	µsec
t_{TL}	TXCLK Low Period	34.72		1,667	µsec
t_{TSRL}[3]	TXSTRB Low Pulse Width		17.36 or 12.05 or 10.4		µsec
$1/t_{PT}$[4]	Frequency of TXSTRB		9600 or 10368		Hz

NOTE 1: The frequency of TXCLK is varied from 300Hz to 14,400Hz according to operation modes (i.e. V.33, V.27FB or G2/G1, etc.)
NOTE 2: The TXCLK is a square wave with a typical duty cycle of 50%.
NOTE 3: 17.36ms of t_{TSRL} correspond to 9600Hz of $1/t_{PT}$ except for V.33 FB mode. It is 10.4ms of t_{TSRL} for V.33FB mode and 12.05ms of t_{TSRL} for G2/G1 mode.
NOTE 4: All TXSTRB frequencies are equal to 9600Hz except for G2/G1 mode which is 10368Hz.

SC11086/SC11196 INTERFACE TIMING II

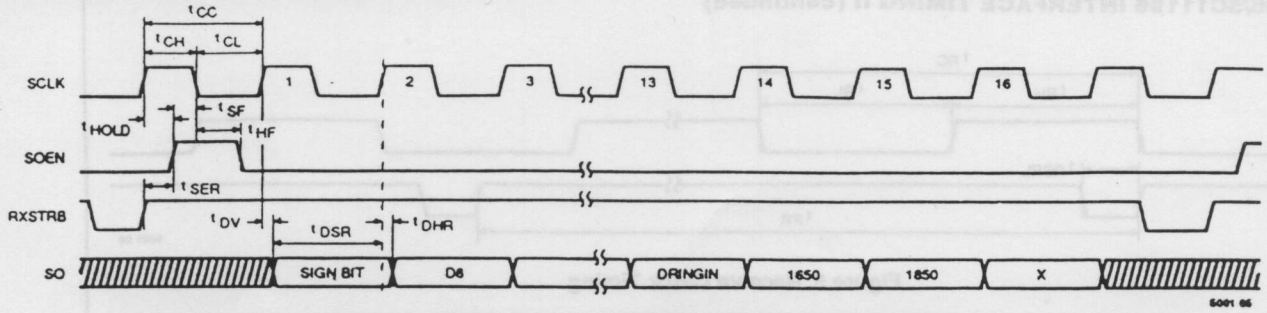


Figure 4. Serial Output Timing With Respect To RXSTRB

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{CC}	Cycle Time of SCLK		408		ns
t_{CH}	SCLK High Period		204		ns
t_{CL}	SCLK Low Period		204		ns
t_{HOLD}	Holding Time from SCLK High to SOEN High	0			ns
t_{SF}	Set up Time from SOEN High to SCLK Low	50			ns
t_{HF}	Hoding Time from SCLK Low to SOEN Low	100			ns
t_{SER}	Set up Time from RXSTRB High to Soen High	0			ns
t_{DV}	SO Data Valid after SCLK goes High			100	ns
t_{DSR}	Data Setup Time with Respect to SCLK High	304			ns
t_{DHR}[1]	Data Hold Time with Respect to SCLK High			100	ns

NOTE 1: A total of 16 bits of data are shifted out from an internal shift register between two consecutive SOEN high pulses. Data will be available after each rising edge of SCLK. The MSB is shifted out first. The LSB is don't care.

SC11086/SC11196 INTERFACE TIMING II (continued)

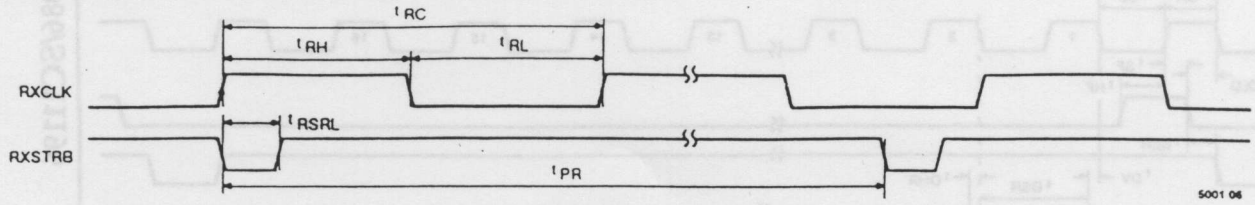


Figure 5. Receive Clock Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{RC}[1]	Cycle time of RXCLK	416.6		3,333	µsec
t_{RH}[2]	RXCLK High Period	208.3		1,667	µsec
t_{RL}	RXCLK Low Period	208.3		1,667	µsec
t_{RSRL}[3]	RXSTRB Low Pulse Width		6.9 or 13.8 or 12.05		µsec
$1/t_{PR}$[4]	Frequency of RXSTRB		2400 or 1600 or 1200 or 9600 or 10368		Hz

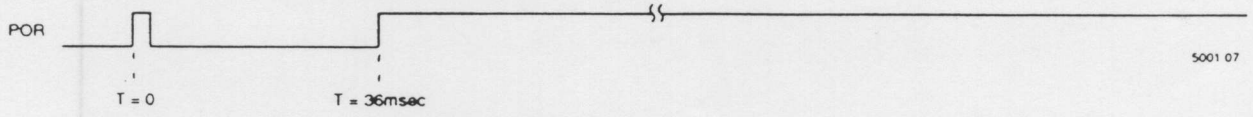
NOTE 1: The frequency of RXCLK is varied from 2400Hz to 14,400Hz according to operation modes (i.e. V.33, V.29, V.27 FB, etc.)

NOTE 2: The RXCLK is a square wave with a typical duty cycle of 50%.

NOTE 3: 6.9msec of t_{RSRL} correspond to all operation mode except for V.27FB mode, G2/G1 mode and FSK,V.21 mode. It is 13.8msec of t_{RSRL} for V.27FB mode. The RXSTRB will be the same as TXSTRB for the G2/G1 and FSK,V.21 modes. therefore, the t_{RSRL} will be identical to t_{TSRL} under the G2/G1 mode and FSK, V.21 mode. It is 12.05ms of t_{RSRL} for G2/G1 mode and 17.36ms of t_{RSRL} for FSK, V.21 mode.

NOTE 4: The frequency of RXSTRB is 2400Hz for V.33, V.33FB,V.29,V.29FB1l and V.29FB2 modes. The frequency of RXSTRB is 1600Hz for V.27 mode. The frequency of RXSTRB is 1200Hz for V.27FB and 9600Hz for FSK,V.21 mode. The frequency of RXSTRB is 10368Hz for the G2/G1 mode.

SC11086/SC11196 INTERFACE TIMING III



NOTE 1: Assume V_{DD} is turned on (V_{DD} > 3.75V) at T=0, POR pin goes low to activate the power-on-reset function for the DSP chip. After 36msec, the POR pin goes back to normally high until the V_{DD} drops below 3.5V.

Figure 5. Timing Diagram for Power-on-Reset pin (POR)