PRELIMINARY

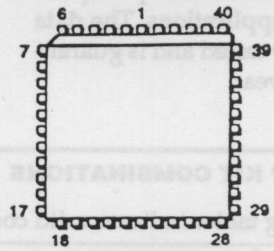
SIERRA SEMICONDUCTOR

SC11077/SC11087/SC11088/SC11198
9600 bps Facsimile Modem DSPs

FEATURES

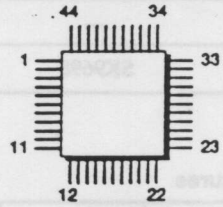
- ☐ Low Power
  - Single supply +5V + 10%
  - 130mw (typical) operating
  - 50mw (typical) standby.
- ☐ Fax Modes
  - V.29, V.27ter, V.21 Channel 2
- ☐ Voice Mode (SC11087)
  - 10-12 bit linear
  - 8 bit μ-Law
  - 9.6, 8, 7.3, 4.8, ksps options
- ☐ HDLC Flag Detection
- ☐ DTE Interface
  - Parallel PC bus
  - RS232C CCITT V.24 serial
- ☐ Controller Interface
  - Dual port RAM
  - R96MD register compatible
- ☐ Data Modes (SC11088 only)
  - V.22bis, V.22, V.23, V.21
  - Bell 103, 212A, 202
  - Caller I.D. support
  - Synchronous, Asynchronous
- ☐ DTE Interface
  - Parallel PC bus
  - RS232C CCITT V.24 serial
- ☐ Serial FMAP interface
- ☐ Equalizer
  - Automatic adaptive receive equalize
  - Selectable fixed compromise
- ☐ Small Size
  - PLCC or PQFP packages
- ☐ DTMF detect
- ☐ 200 ns Instruction cycle time
- ☐ 256 x 8 RAM
- ☐ Internal ROM program

44 PIN PLCC PACKAGE



SC11077CV
SC11087CV
SC11088CV
SC11198CV

44 PIN PQFP PACKAGE



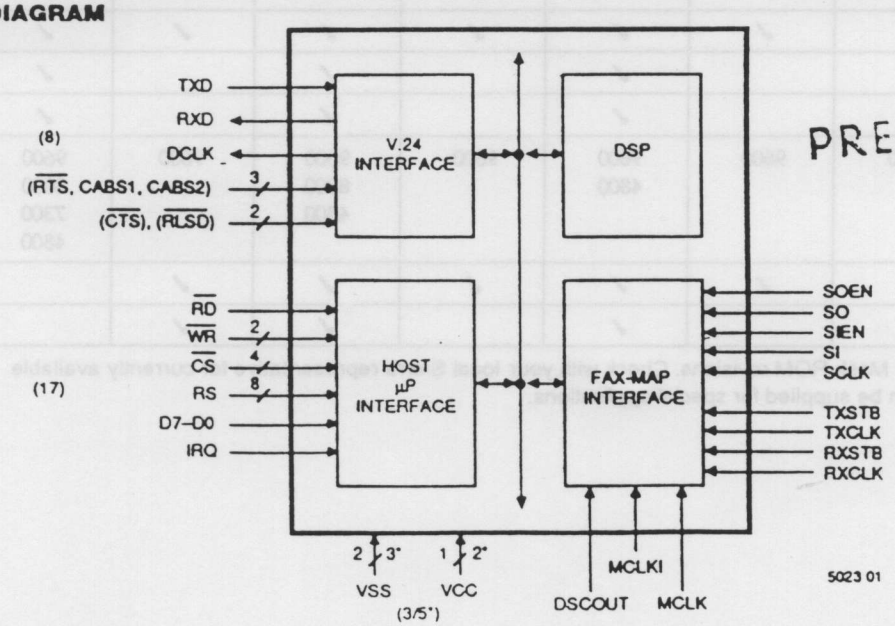
SC11077CQ
SC11087CQ
SC11088CQ
SC11198CQ

GENERAL DESCRIPTION

The SC11077 series products are low power facsimile modem Digital Signal Processors designed for use with Sierra's SC11086, SC11092, SC11094, and SC11196 family of Fax Modem Analog Processors (FMAP).

Together, the two-chip sets comprise a complete modem data pump supporting CC1TT facsimile standards up to 9600 bit/s. All models support group 3, V.21 channel 2, V.27 ter & V.29 standards. In addition the SC11198 supports groups 1 & 2 modes and provides a Rockwell R96MD register compatible interface. The SC11077/87 features voice mail modes including simultaneous voice transmission & DTMF tone detection and optional μ-LAW compression. The SC11088, in conjunction with SC11092 or SC11094, comprises a complete synchronous 9600 bit/s facsimile modem and 2400 bit/s data modem supporting synchronous and also asynchronous full duplex V.21, V.22, V.22bis, V.23, Bell 103, Bell 212, 212A, and half duplex V.26ter CCITT recommendations. The set includes DTMF tone detection,

BLOCK DIAGRAM



PRELIMINARY

Figure 1.

Rev 0.9

GENERAL DESCRIPTION (continued)

programmable transmit level, HDLC flag detection, ring input and elimination of external op amp for dial up line applications. The data pump is fully tested and is guaranteed for one year.

The SC11086 & SC11198 chipset can be used with Sierra's SK0611 and other chipsets to build a complete intelligent Fax and Data modem compatible with EIA 2388 class 2 specifications. A special four chip kit, SQ0196, is offered for this application. Firmware and application software are available.

DATA PUMP KIT COMBINATIONS

The following tables indicate valid combinations of FMAP and FDSP.

FMAP	FDSP			
	SC11198	SC11087	SC11088	SC11077
SC11086	SK8698	SK8687	—	—
SC11092	—	—	SK9288	SK9277
SC11094	—	—	SK9488	SK9477
SC11196	SK9698	—	—	—

General Kit Features

	KIT	SK8698	SK9698	SK8687	SK9288	SK9277	SK9488	SK9477
	CODE	AAB	AAC	AAA	AAB		AAB	AAC
G3		✓	✓	✓	✓	✓	✓	✓
G1, 2			✓					
Supply Voltage		±5V	±5V	±5V	±5V	+5V	+5V	+5V
Power Consumption		400	400	400/250	400/50	400/50	400/40	400/40
V.27, V.27ta, V.29		✓	✓	✓	✓	✓	✓	✓
V.21, 22, 22bis, 23					✓	✓	✓	✓
Bell 103, 202, 212A					✓	✓	✓	✓
DTMF detect		✓	✓	✓	✓	✓	✓	✓
Voice Mail Mode				✓		✓		✓
μ-Law Conversion				✓		✓		✓
Voice Sample Rate		9600	9600	9600 4800	9600	9600 8000 4800	9600	9600 8000 7300 4800
Ring Detect ✓		✓	✓	✓	✓	✓	✓	
Caller I.D.				✓		✓	✓	

Features may vary depending on Mask ROM revisions. Check with your local Sierra representative for currently available options. Custom ROM Masks can be supplied for special applications.

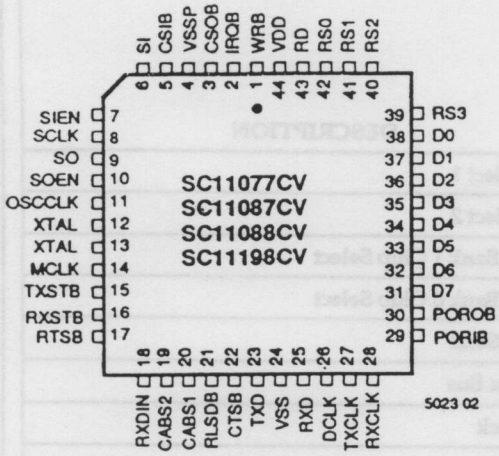
PIN DESCRIPTIONS

PIN NAME	PIN NUMBER SC11077CV SC11087CV SC11088CV SC11198CV PLCC	PIN NUMBER SC11077CQ SC11087CQ SC11088CQ SC11198CQ PQFP	TYPE[1]	DESCRIPTION
CABS1	20	14	IA	Cable Select 1
CABS2	19	13	IA	Cable Select 2
CSIB	5	43	IA	Register Bank 1 Chip Select
CSOB	3	41	IA	Register Bank 0 Chip Select
CTSB	22	16	O	Clear-to-Send
D_7–D_0	31–38	25–32	I/O A	8 Bit Data Bus
DCLK	26	20	O	Data Clock
IRQB	2	40	O	Interrupt Request
MCLK	14	8	O	Clock Output (9.8304 mhz)
OSCCLK	11	5	O	Oscillator Output (19.6608 mhz)
PORIB	29	23	IB	Power-on-Reset Input
POROB	30	24	I/O B	Power-on-Reset Input/Output
RD	43	37	IA	Read Enable
RLSDB	21	15	O	Received Line Signal Detector
RS_3–RS_0	39–42	33–36	IA	Register Select Lines
RTSB	17	11	IA	Request-to-Send
RXCLK	28	22	IA	Receiver Clock
RXD	25	19	O	Receiver Data
RXDIN	18	12	IA	Receiver Data Input
RXSTB	16	10	IA	Receiver Strobe
SCLK	8	2	IA	Serial Input Clock
SD	9	3	O	Serial Data Output
SI	6	44	IA	Serial Data Input
SIEN	7	1	IA	Serial Input Enable
SOEN	10	4	O	Serial Output Enable
TXCLK	27	21	IA	Transmitter clock
TXD	23	17	IA	Transmitter Data
TXSTB	15	9	IA	Transmitter Strobe
V_{DD}	44	8	PWR	+5 Volt Supply
V_{SS}	24	18	PWR	Ground
V_{SSP}	4	42	PWR	Ground
WRB	1	39	IA	Enable
XTAL	12	6	X	Crystal Output (19.6608 MHz)
XTAL	13	7	X	Crystal Input (19.6608 MHz)

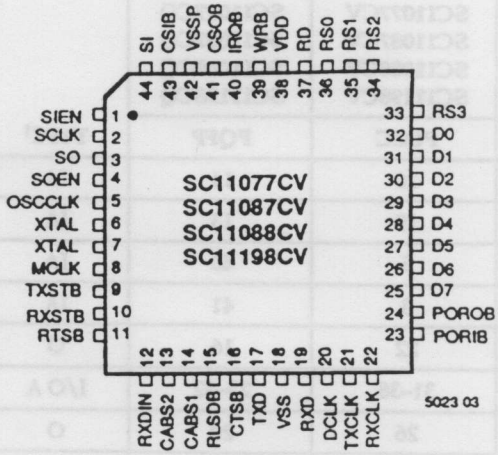
NOTE 1: See table on page 11, "Digital Interface Characteristics"
NOTE 2: I = Input, O = Output

CONNECTION DIAGRAMS

44L PLCC



44L PQFP



FUNCTIONAL DESCRIPTION

The Fax Modem DSP (FMDSP) processor is a DSP engine for Fax Modem applications. It is designed to do all signal processing tasks for a Fax Modem except the sample rate processing for the group 3 receiver, which is done in the FaxMAP front end chip. Since this is a half duplex modem, the maximum computation load is presented by symbol processing for the V.29 receiver, combined with simultaneous tone generation. This includes the following routines which are completed in one V.29 symbol period of 416 ms:

- Equalizer
- Carrier Tracker
- Slicer
- Differential Decoder
- Grey to Binary Converter
- Descrambler
- Sync Recovery PLL
- Tone Generator

Other functions which are handled, but not in the critical path are:

- Group 1 Transmitter and Receiver
- Group 2 Transmitter and Receiver
- V.21 Transmitter and Receiver
- Tone Generators (Including DTMF)
- Tone Detector

Processor Architecture Overview

The FMDSP processor is a 16-bit processor dedicated to the FAX Modem DSP functions. Designed with RISC philosophy, its instructions are mostly single word and execute in a single clock cycle. The processor uses a two stage pipeline, fetch and execute. Therefore, all branch instructions take two clock cycles to execute. Delay Jump Instructions are included to achieve single cycle branch as most RISC processors do.

The FMDSP processor utilizes the so-called Harvard achitecture similar to TMS320. The Data memory space of 512 words total is completely on chip, while the program space of 64K words can be either on chip or off chip. The program memory is read only. A TMS320-like TLBR instruction is provided to load coefficient table from program space into on chip RAMs.

The FMDSP is organized around one 16 bit data bus and one 9 bit address bus. Except for four hardware registers, all processor resources are addressable Data Memory locations. All I/O are also memory mapped.

Special hardware is incorporated on chip to achieve high throughput in critical DSP functions. The most notable is the 16 by 16 hardware multiplier that can do a 2's complement multiplication in 63 ns. An 8 bit accumulator together with the 16 bit ALU combine to perform the 24 bit accumulation of multiply results which is 32 bits wide with lower 7 bits discarded. There is also a 6 bit loop counter used by the RPT and RPT2 instructions to perform loops with zero overhead. Saturation arithmetic is supported by the ALU.

The FMDSP is supplied as a pre-programmed ASIC product with features as outlined on page 2. The functions provided by these versions are described in the following pages.

Transmitter Tonal Signaling and Carrier Frequencies

T.30 Tonal Signaling Frequencies

Function	Freq. (Hz) (±0.01%)
Calling Tone (CNG)	1100
Answer Tone (CED)	2100
Group 2 Identification (C12)	1850
Group 2 Command (GC2)	2100
Group 2 Confirmation (CFR2, MCF2)	1650
Line Conditioning Signal (LCS)	1100
End of Message (EOM)	1100
Procedure Interrupt (PIS)	462
Group 1 White Black	1500 2400

Carrier Frequencies

Function	Freq. (Hz) (±0.01%)
T.3 Carrier (Group 2)	2100
V.27 ter Carrier	1800
V.29 Carrier	1700

Tone Generation

Under control of the host processor, the modem can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3400 Hz are attenuated.

Tone Detection

In the 300 bit/s FSK receive configuration, the presence of tones at preset frequencies is indicated by bits in the interface memory.

Data Encoding

The modem data encoding conforms to CCITT reccommendations V.29 and V.27 ter.

Signaling and Data Rates

Specification	Baud Rate (Symbols/Sec.)	Bits per Baud	Data Rate (bit/s) (±0.01%)	Symbol Points
V.29	2400	4	9600	16
V.29	2400	3	7200	8
V.27ter	1600	3	4800	8
V.27ter	1200	2	2400	4
V.26	1200	2	2400	4
V.22bis	600	4	2400	16
V.23	1200/75	1	1200/75	N/A
V.22	600	2	1200	4
V.21	300	1	300	N/A
Bell 103	300	1	300	N/A
Bell 212A	600	2	1200	4

Equalizers

The data pump provides the following equalization functions which can be used to improve performance when operating over poor lines:

Cable Equalizers—Selectable compromise cable equalizers are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Automatic Adaptive Equalizer—An automatic adaptive equalizer is provided in the receiver circuit for V.27 and V.29 configurations. The equalizer is configured as a T/2 equalizer with 32 taps.

Transmitted Data Spectrum

The transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud*. Square root of 90 percent.
2. *1600 Baud*. Square root of 50 percent.
3. *2400 Baud*. Square root of 20 percent.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules, and typically exceed the requirements of foreign telephone regulatory bodies.

Scrambler/Descrambler

The modem incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 ter or V.29 depending on the selected configuration.

Received Signal Frequency Tolerance

The receiver circuit of the modem can adapt to received carrier frequency error of up to ± 10 Hz with less than a 0.2 dB degradation in BER performance. However, the symbol rate must be within 0.01% for proper operation. Group 2 carrier recovery capture range is 2100 ± 30 Hz. The Group 2 receiver operates properly when the carrier is varied by ± 16 Hz at a 0.1 Hz per second rate.

Tone Detection

Three tone detectors are active in the FSK or tone receive mode. Tone detectors are active in the Group 2 transmit mode. The frequencies for the detectors are programmable through the RAM access. Refer to the Rockwell Application Note (Order No. 668) for the procedures. Be aware that the sampling rate in the Group 2 mode is 10368 s/s; therefore, use 10368 instead of 9600 to calculate the coefficients for Group 2 tone detectors in those equations.

HDLC Flag Detection

In Group 3 or FSK receive mode, HDLC flag sequence can be detected by enabling the FDEN bit in the interface memory. In Group 3 mode, the hardware 1850/1650 Hz detector is enabled and monitored to determine the presence of flag sequence. In FSK mode, the firmware monitors the received data to decide the flag detection.

Voice Mode Application

When the modem is configured in the voice mode, the 10(12) bit data are read/written through the interface register 0:1 (MSBs) and 0:0 (LSBs). The data are sampled at 9600, 8000, 7300 or 4800 samples per second as set in the modem chip configuration register.

In the transmit mode, only the 10(12) MSBs are written to the 10(12) bit D/A. In the receive mode, the 6(4) LSBs are filled with zeroes. During voice transmissions, the DTMF receiver is also activated. This allows the host to terminate voice transmission once a DTMF tone is detected.

To use the voice capability, the host processor first sets the DSP to voice mode by writing 82H to register (0:4) and setting SETUP bit (0:E:3) to one. This also enables the DTMF receive function in SC11087. (The SC11198 cannot simultaneously detect DTMF tones while transmitting voice.)

The MDA0 (0:E:0) bit (Modem Data Available) is set by the DSP when it is ready for the host processor to read or write data is YSM and YSL. After the processor has read or written 16 bit data to these RAM locations, it resets MDA0 to "0". In transmit mode the most significant 12 bits of YSM and YSL will be written to the DAC for transmission. In the receive mode, the 12 bit ADC output is written to YSM & YSL and the 4 LSB's are filled with "0".

Receive Timing

In the receive state, the FDSP provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the center of the received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ± 1%.

Transmit Level

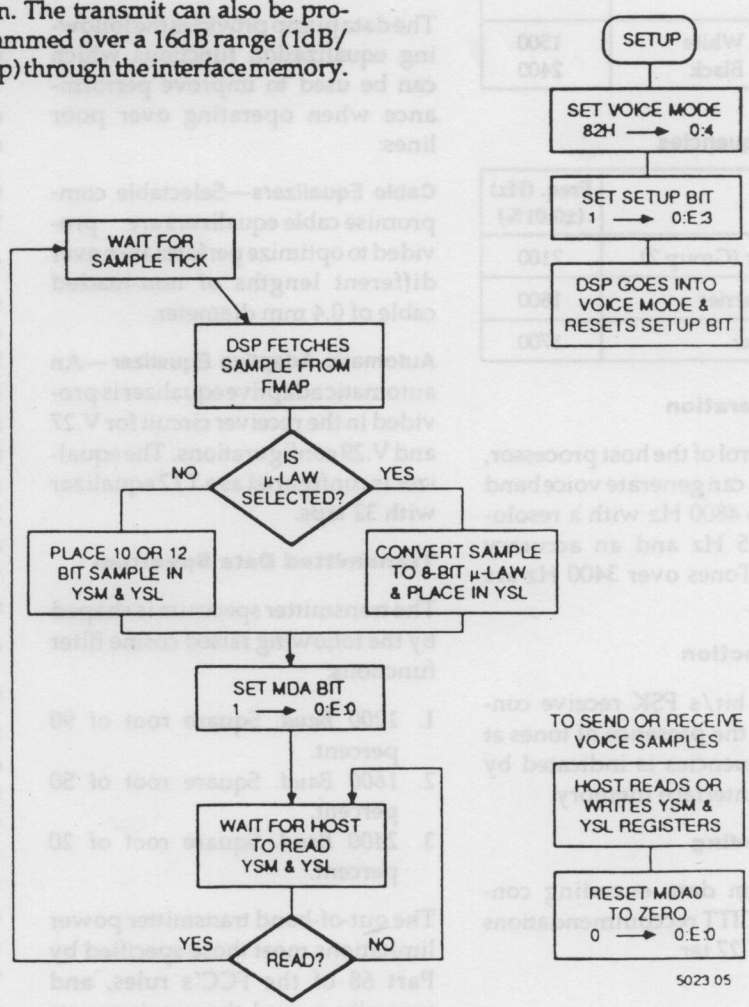
The transmitter output level defaults to +5 dBm ± 1 dB at power on. When using the default transmit level and driving a 600 ohm load, the TXA output requires a 600 ohm series resistor to provide -1 dBm ±1 dB to the load. The output level can be programmed over a 10 dB range by performing a RAM write operation. The transmit can also be programmed over a 16dB range (1dB/step) through the interface memory.

Transmit Timing

In the transmit state, the FDSP provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, 2400, or 300 Hz (±0.01%). In Group 2 and Group 1, DCLK tracks an external 10368 Hz clock. If the external clock input (XCLK) is grounded the Group 1 and Group 2 DCLK is 10372.7 Hz ±0.01% and group 1.
2. *Duty Cycle.* 50 ± 1%

Transmit Data (TXD) must be stable during the 1 microsecond period immediately preceding and the 1 microsecond period immediately following the rising edge of DCLK.



Turn-On Sequence

A total of ten selectable turn-on sequences can be generated by the modem, as defined in Table 1.

Turn-Off Sequence

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy. In V.21 the transmitter turns off within 7 ms after $\overline{RTS}$ goes false. In Group 2 and Group 1 the transmitter turns off within 200 µs after $\overline{RTS}$ goes false.

Clamping

The following clamps are provided with the modem:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{RSLD}$ is off.
2. *Received Line Signal Detector ($\overline{RSLD}$).* $\overline{RSLD}$ is clamped off (squelched) during the time when $\overline{RTS}$ is on.
3. *Extended Squelch.* Optionally, $\overline{RSLD}$ remains clamped off for 130 ms after the turn-off sequence

Response Times of Clear-to-Send ($\overline{CTS}$)

The time between the off-to-on transition of $\overline{RTS}$ and the off-to-on transition of $\overline{CTS}$ is dictated by the length of the training sequence. Response time is 253 ms for V.29, 708 ms for V.27 ter at 4800 bit/s, and 943 ms for V.27 ter at 2400 bit/s. In V.21 $\overline{CTS}$ turns on in 14 ms or less. In Group 2 $\overline{CTS}$ turns on in 400 µs or less.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in the data state is a maximum of 2 baud times for all configurations.

Received Line Signal Detector ($\overline{RLSD}$)

For either V.27 ter or V.29, $\overline{RSLD}$ turns on at the end of the training sequence. If training is not detected at the receiver, the $\overline{RSLD}$ off-to-on response time is 15 ± 10 ms. The $\overline{RSLD}$ on-to-off response time for V.27 is 10 ± 5 ms and for V.29 is 30 ± 9 ms. Response times are measured with a signal at least 3 dB above the actual $\overline{RSLD}$ on threshold or at least 5 dB below the actual $\overline{RSLD}$ off threshold.

The $\overline{RSLD}$ on-to-off response time ensures that all valid data bits have appeared on RXD.

Two threshold options are provided:

1. Greater than -43 dBm ($\overline{RSLD}$ on)
   Less than -48 dBm ($\overline{RSLD}$ off)
2. Greater than -47 dBm ($\overline{RSLD}$ on)
   Less than -52 dBm ($\overline{RSLD}$ off)

NOTE
Performance may be at a reduced level when the received signal is less than -43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

Table 1. Turn-On Sequences

Specification	$\overline{RTS}$–$\overline{CTS}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V.29	253 ms	438 ms
V.27 4800 bit/s	708 ms	913 ms
V.27 2400 bit/s	943 ms	1148 ms
V.21 300 bit/s	≤ 14 ms	≤ 14 ms
Group 2	≤ 400 µs	≤ 400 µs

MODES OF OPERATION

The DSP operates in either a serial or a parallel mode.

Serial Mode

The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data.

Parallel Mode

The data pump can transfer channel data eight bits at a time via the microprocessor bus.

Mode Selection

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to 1. The modem automatically defaults to the serial mode at power-on. In either mode the modem is configured by the host processor via the microprocessor bus.

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits.

Hardware Circuits

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed i the Modem Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital or Analog Interface Characteristics.

Microprocessor Interface

Sixteen hardware circuits provide address (RS_0–RS_3), data (D_0–D_7), control ($\overline{CS}$, Read and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8088 microprocessor or Sierra ASIC SC11011 series controller family.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion.

Cable Equalizer Selection

CABS2	CABS1	Length of 0.4 mm Dia. Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Overhead

Except for the power-on-reset signal $\overline{POR}$, the overhead signals are dc power or ground points. When the modem is initially energized a signal called Power-On-Reset ($\overline{POR}$) causes the modem to assume a valid operational state. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready for normal use. The POR sequence is reinitiated aytime the + 5V supply drops below + 3.5V for more than 30 ms, or an external device drives pin 29 low for at least 3 µs. When an external low input is applied to pin 29, the modem is ready for normal use approximately 10 ms after the low input is removed. In all cases, the POR sequence requires from 50 ms to 350 ms to complete. The POR sequence leaves the modem configured as follows:

- V.29/9600 bit/s
- T/2 equalizer
- Serial mode
- Training enabled
- Echo protector tone enabled
- No extended squelch
- Higher receive threshold
- Interrupts disabled
- RAM Access S = 00
- RAM Access B = 22
- Eye pattern disabled
- Transmit signal is summed with AUX input before sending to TXA
- Transmit level control with 0dB attenuation
- HDLC flag detection disabled
- Receive input control normal

This configuration is suitable for performing high speed data transfer on the PSTN with the serial data port selected as the input and output point for data terminal equipment (DTE).

Modem Hardware Circuits

Name	Type	PLCC Pin No.	Description
A. OVERHEAD:			
Ground	GND	4, 24	Power Supply Return
+ 5 volts	PWR	44	+ 5 volt supply
$\overline{POR}$	I/OB	29	Power-on-reset
B. MICROPROCESSOR INTERFACE:			
D_7	I/OA	31	Data Bus (8 bits)
D_6	I/OA	32	
D_5	I/OA	33	
D_4	I/OA	34	
D_3	I/OA	35	
D_2	I/OA	36	
D_1	I/OA	37	
D_0	I/OA	38	
RS_3	IA	42	Register Select (4 bits) Select Reg. 0 – F
RS_2	IA	41	
RS_1	IA	40	
RS_0	IA	39	
$\overline{CS0}$	IA	3	Chip Select Sample Rate Register
$\overline{CS1}$	IA	5	Chip Select Baud Rate Register
READ	IA	43	Read Enable
$\overline{WRITE}$	IA	1	Write Enable
$\overline{IRQ}$	OB	2	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	26	Data Clock
$\overline{RTS}$	IB	17	Request-to-Send
$\overline{CTS}$	OC	22	Clear-to-Send
TXD	IB	23	Transmitter Data
RXD	OC	25	Receiver Data
$\overline{RSLD}$	OC	21	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABS1	IB	20	Cable Select 1
CABS2	IB	19	Cable Select 2

Software Signals

The FDSP contains 32 registers to which an external (host) microprocessor has access. Although these registers are within the DSP, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers update at the modem sample rate (9600 bit/s) in the transmit mode and at the selected baud rate in the receive mode. In Group 2 FSK configuration they update at the sample rate of 10368/9600 Hz.

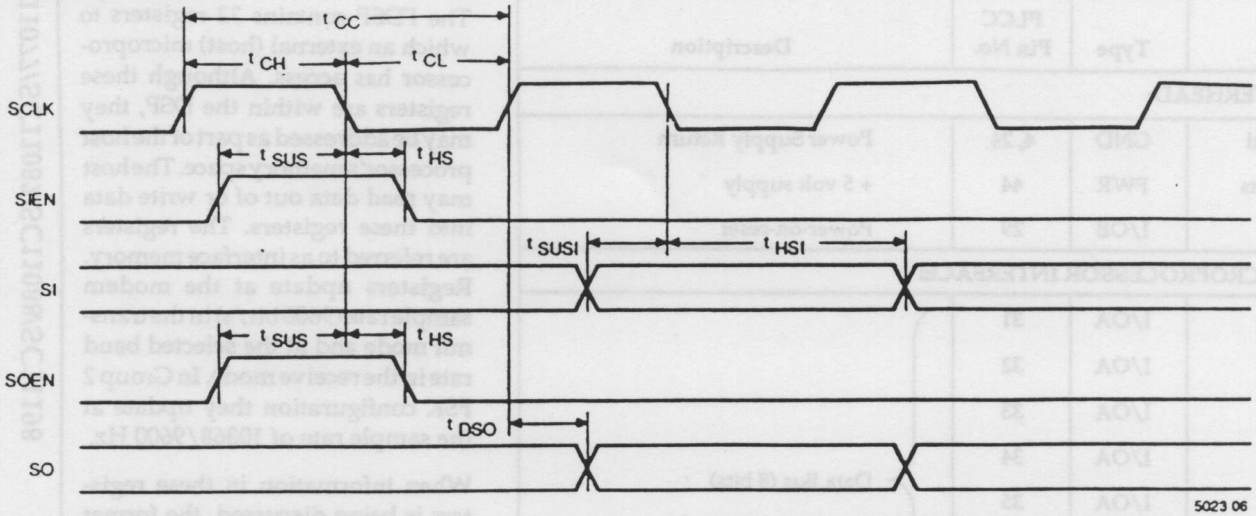
When information in these registers is being discussed, the format Y:Z:Q is used. The chip includes two blocks of 16 registers. The block is specified by Y (0 or 1), the register by Z (0-F), and the bit by Q (0-7, 0 = LSB). A bit is considered to be "on" when set to a 1.

Status/Control Bits

Modem operation is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined on the Interface Memory table. Bits designated by a '—' are reserved for modem use only and must not be changed by the host.

Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-write-modify operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits are written back into the register of the interface memory.

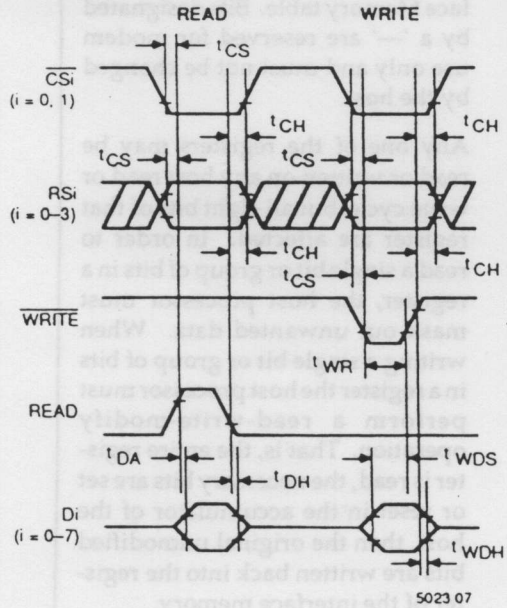
SIO PORT TIMING



SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
t_{CC}	SCLK Cycle Time		408		ns
t_{CH}	SCLK High Pulse Width*		204		ns
t_{CL}	SCLK Low Pulse Width*		204		ns
t_{SUS}	SIEN/SOEN setup before SCLK falling	50			ns
t_{HS}	SIEN/SOEN hold time after SCLK falling	100			ns
t_{SUSI}	SI setup before SCLK falling	50			ns
t_{HSI}	SI Hold time after SCLK falling	50			ns
t_{DSO}	SO Valid after SCLK rising			100	ns

*Duty Cycle Must Be Within 40-60%

MICROPROCESSOR INTERFACE TIMING DIAGRAM



CRITICAL TIMING REQUIREMENTS

CHARACTERISTIC	SYMBOL	MIN	MAX	UNITS
$\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$	t_{CS}	30	—	ns
Data Access time after Read	t_{DA}	—	140	ns
Data hold time after Read	t_{DH}	10	50	ns
CSi, RSi hold time after Read or $\overline{Write}$	t_{CH}	10	—	ns
Write data setup time	t_{WDS}	75	—	ns
Write data hold time	t_{WDH}	10	—	ns
Write strobe pulse width	t_{WR}	75	—	ns

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage	+6 V
Input Voltage	-0.6 V to V_{CC} + 0.6V
Storage Temperature Range	-65 to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature Range	0 to 70°C

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = +5 V ± 10%)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	V
I_{CC}	Nominal Operating Current @ V_{CC} = 5.5V		40	90	mA
I_{CC}	Power Down mode (SC11077/87/88 Only)		12	25	mA
F_{CLK}	Crystal Clock Frequency	19.589	19.6608	19.6627	MHz

DIGITAL INTERFACE CHARACTERISTICS (DC)

Symbol	Parameter	Units	IA	IB	IC	ID	IE	OA	OB	OC	I/OA	I/OB
V_{IH}	Input High Voltage	V	2.0min	3.15min	2.0min	2.0min	3.15min				2.0min	2.0min
V_{IL}	Input Low Voltage	V	0.8max	1.35max	0.8max	1.35max					0.8max	0.8max
V_{OH}	Output High Voltage	V							3.65min[1]	3.65min[1]	2.4min[1]	2.4min[3]
V_{OL}	Output Low Voltage	V						0.4max[2]	0.85max[2]	0.85max[2]	0.4max[2]	0.4max[2]
I_{OH}	Output High Current	mA							-0.1	-0.1		
I_{OL}	Output Low Current	mA						1.6	1.6	1.6		
IPU	Short Circuit Pullup Current	µA			-240max -100min		-240max -100min	-240max -100min				-240max -100min
	Circuit Type		TTL	CMOS	TTL with Pullup	TTL Sch.Trig.	CMOS with Pullup	OPEN-DRAIN with Pullup	CMOS	CMOS 3-state	TTL Trans-ceiver	OPEN-DRAIN with Pullup

NOTE 1: I_{LOAD} = -100 mA
NOTE 2: I_{LOAD} = 1.6 mA
NOTE 3: I_{LOAD} = -40 mA
NOTE 4: V_{CC} = 5V ± 10%

RAM Data Access

The user can access much of the data stored in the modem's memories. This data is a useful tool in performing certain diagnostic functions.

The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register 0:F (RAM ACCESS S) or 1:F (RAM ACCESS B). The RAM Access Codes table lists access codes for storage in registers 0:F or 1:F and the corresponding diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long.

These bits are written into interface memory registers 0:3, 0:2, 0:1 and 0:0, or 1:3, 1:2, 1:1 and 1:0, in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit 0:5:5 (RAMWS) or bit 1:D:0 (RAMWB) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM in bank 0 or in bank 1, respectively. When writing into the RAM, only 16 bits are transfered, not 32 bits as for a read operation. The 16 bit written in XRAM or YRAM come from registers 1 and 0, with register 1 being the most significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAM Access B bits of register 1:F for chip 1, or by means of 0:5:4 (RAE) and 0:F (RAM Access S) for chip 0. When bit 1:F:7 or 0:5:4 is set to one, the XRAM is selected. When 1:F:7 or 0:5:4 equals zero, YRAM is selected.

When the host processor reads or writes register 0, the modem data available bit 0:E:0 or 1:E:0 (MDA1) is reset to zero. When the FDSP reads or writes register 0, MDA1 is set to a one. When set to a one by the host, bit 0:E:2 or 1:E:2 (IE1) enables the MDA1 bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit 0:E:7 or 1:E:7 (IA1) goes to a one.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem. This information is scaled as shown in the Diagnostic Data Scaling table.

RAM Access Codes

NODE	FUNCTION	ACCESS	RAE	BLOCK	READ REG. NO.
1	Received Signal Samples	40	X	0	2, 3
2	Demodulator Output				NAV
3	Low Pass Filter Output	54	X	0	0, 1, 2, 3
4	Average Power	5C	X	0	2, 3
5	AGC Gain	3C	X	0	2, 3
6	Tone 1 Frequency	71	1	0	0, 1
7	Tone 1 Level	72	1	0	0, 1
8	Tone 2 Frequency	71	0	0	0, 1
9	Tone 2 Level	72	0	0	0, 1
10	Output Level	4C	0	0	0, 1
11	Equalizer Input	40	N.A.	1	0, 1, 2, 3
12	Equalizer Tap Coefficients	01-20	N.A.	1	0, 1, 2, 3
13	Unrotated Equalizer Output	61	N.A.	1	0, 1, 2, 3
14	Rotated Equalizer Output (Received Point—Eye Pattern)	22	N.A.	1	0, 1, 2, 3
15	Decision Points (Ideal)	62	N.A.	1	0, 1, 2, 3
16	Error Vector	63	N.A.	1	0, 1, 2, 3
17	Rotation Angle	00	N.A.	1	0, 1
18	Frequency Correction	A8	N.A.	1	2, 3
19	Eye Quality Monitor (EQM)	AB	N.A.	1	2, 3

RAE = X is don't care since this location should only be read from, and not written to, by the host. N.A. is not applicable since RAE is not used in bank one.

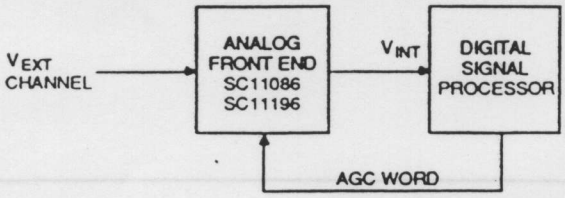
NAV = Not Available

In Group 2 receive mode the modem does the training internally. It does not require the extensive interaction from the external processor.

DIAGNOSTIC DATA SCALING

NODE 1

Received Signal Samples = A/D Sample Word (signed 16 bits, twos complement)



$$V_{IN} = \frac{(\text{A/D Sample Word})_{16}}{40_{16}} \times \frac{3}{256} \text{ Volts}$$

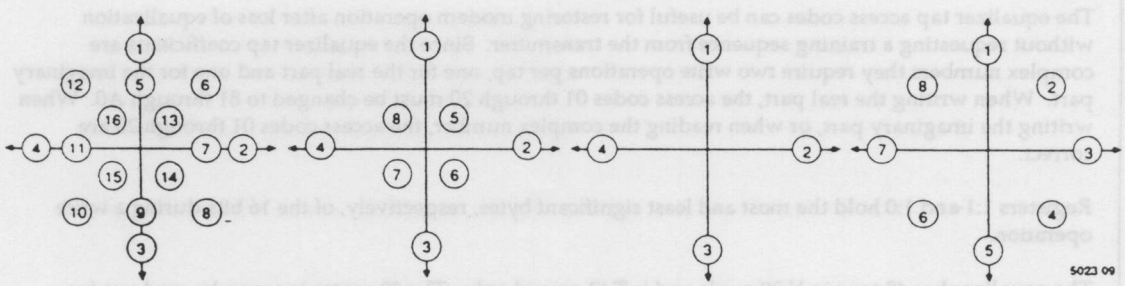
$$V_{EXT} = V_{INT} \; / \; \text{LOG}_{10}^{-1} \frac{\text{AGC Gain (dB)}}{20}$$

1438 eq 1

NODE 3, 11, 13, 14, 15

All Baseband Signal Nodes (32 bits, complex, twos complement)

POINT	CONFIGURATION			
	V.29/9600 X, Y	V.29/7200 X, Y	V.29/4800 & V.27/2400 X, Y	V.27/4800 X, Y
1	0000, 2800	0000, 2400	0000, 1F00	0000, 1F00
2	2800, 0000	2400, 0000	1F00, 0000	1600, 1600
3	0000, D800	0000, DC00	0000, E100	1500, 0000
4	D800, 0000	DC00, 0000	E100,0000	1600, EA00
5	0000, 1800	0C00, 0C00		0000, E100
6	1800, 1800	0C00, F400		EA00, EA00
7	1800, 0000	F400, F400		E100, 0000
8	1800, E800	F400, 0C00		EA00, 1600
9	0000, E800			
10	E800, E800			
11	E800, 0000			
12	E800, 1800			
13	0800, 0800			
14	0800, F800			
15	F800, F800			
16	F800, 0800			



4 **Average Power (16 bits, unsigned)**

Typical value: 0889_{16} (corresponding to 0 dBm)

$$\text{Post-AGC Average Power in dBm} = 10 \;\; \text{Log} \frac{(\text{Average Power Word})_{16}}{889_{16}}$$

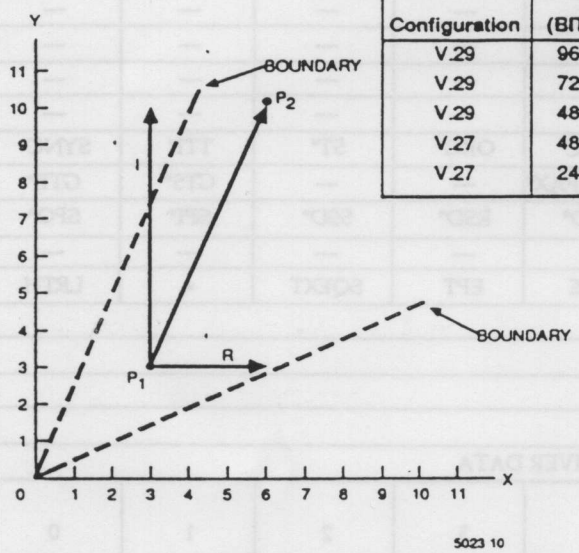
Pre-AGC Power in dBm = Post-AGC Avg. Power in dBm – AGC gain in dB

Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
5	**AGC Gain (16 bits, unsigned)** Range: $0FC0_{16}$ to $7FFF_{16}$ for LRTH = 0 (–43 dBm Threshold) 0640_{16} to $7FFF_{16}$ for LRTH = 1 (–47 dBm Threshold) $\text{AGC Gain in dB} = 50 - \frac{(\text{AGC Gain Word})_{16}}{40_{16}} \times 0.098$
6, 8	**Tone 1 and 2 Frequency (16 bits, unsigned)** N = 6.8267 (Frequency in Hz) Convert N to hexadecimal then store in RAM.
7, 9	**Tone 1 and Tone 2 Level** Calculate the power of each tone independently by using the equation for Output Number given at node 10 with M=16337. Convert these numbers to hexadecimal then store in RAM. Total power transmitted in tone configuration is the result of both tone 1 power and tone 2 power.
10	**Output Level (16 bits, unsigned)** Output Number = $M\,[10^{(Po/20)}]$ Po = output power in dBm with series 600 ohm resistor into 600 ohm load. Convert Output Number to hexadecimal and store in RAM. M varies depending on configuration. The output level can only be changed after RTS is active. **Configuration / M** V.29/9600 — 17408 V.29/7200 — 26880 V.27/4800 — 16640 V.27/2400 — 16640 FSK, Group 1 — 16337 Group 2 — 30976
12	**Equalizer Taps (32 bits, complex, twos complement)** Node 12 is not a single point but is acutally a set of RAM locations containing adaptive equalizer tap coefficients. In V.29 configuration, access codes 01 through 20 hexadecimal represent 32 complex center taps. In V.27 configuration, access codes 01 through 20 hexadecimal represent all 32 complex taps, since the equalizer for V.27 is not as long as the equalizer for V.29. The equalizer tap access codes can be useful for restoring modem operation after loss of equalization without requesting a training sequence from the transmitter. Since the equalizer tap coefficients are complex numbers they require two write operations per tap, one for the real part and one for the imaginary part. When writing the real part, the access codes 01 through 20 must be changed to 81 through A0. When writing the imaginary part, or when reading the complex number, the access codes 01 through 20 are correct. Registers 1:1 and 1:0 hold the most and least significant bytes, respectively, of the 16 bits during a write operation. The equalizer has 48 taps in V.29 mode and is T/2 spaced only. The 32 center taps can be read out for diagnostic purposes. In V.27 mode the equalizere has 32 taps and all taps can be read out.

Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
16	**Error vector (32 bits, complex, twos complement)** Represents the difference between the received point (P2) and the nearest ideal point (P1).

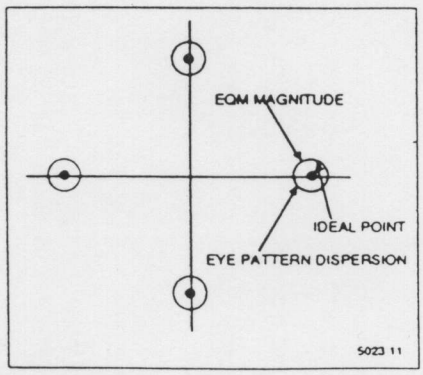


Configuration	Bit Rate (BIT/S)	Registers 3 and 2 Real Error	Registers 1 and 0 Imag. Error	Magnitude $\sqrt{Re^2 + Im^2}$
V.29	9600	$<0C00_{16}$	$<0C00_{16}$	$<0E66_{16}$
V.29	7200	$<2400_{16}$	$<2400_{16}$	$<1AD4_{16}$
V.29	4800	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$
V.27	4800	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$
V.27	2400	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$

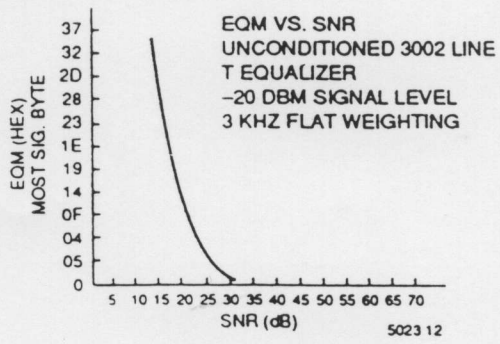
Error Vector Maximum Values

$P_1 = x_1 + iy_1$
$P_2 = x_2 + iy_2$
$P_2 - P_1 = (x_2 - x_1) + i(y_2 - y_1)$
= REAL ERROR + IMAGINARY ERROR

17	**Rotation Angle (16 bits, twos complement)** Represents instantaneous correction for phase and frequency errors Rotation Angle in degrees = $\frac{(\text{Rot. Angle Word})_{16}}{10000_{16}} \times 180$
18	**Frequency Correction (16 bits, twos complement)** Represents componemt of rotation angle caused by frequency error. Range: $FC00_{16}$ to 0400_{16} representing ± 37.5 Hz Frequency Correction in Hz = $\frac{(\text{Freq. Correction Word})_{16}}{10000_{16}} \times$ Baud Rate in Hz
19	**Eye Quality Monitor, EQM (16 bits, unsigned)** Equals the filtered squared magnitude of the error vector. Proportionally to bit error rate is determined by particular application. Stabilizes in approximately 700 baud times from $\overline{RLSD}$ going active.



Relationship of EQM to Eye Pattern



Typical Eye-Quality Versus Signal-to-Noise Ratio for V.29/9600

Interface Memory Bank 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	PDM	RAM ACCESS S						
E	IA0	—	—	—	SETUP	IE0	—	MDA0
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	DL*	RDL*	AL*	ERDC*	ORG*	ST*	TTI*	SYNC*
8	DTR*	DSR*	RXMARK*	DATA/FAX*	—	—	GTS*	GTE*
7	DISS*	LL*	WSI*	WSO*	RSD*	SSD*	SPI*	SPO*
6	—	—	—	—	—	—	—	—
5	RTS	TDIS	RAMWS	RAE	EPT	SQEXT	=	LRTH
4	CONFIGURATION							
3	RAM DATA XSM; FREQM							
2	RAM DATA XSL; FREQL							
1	RAM DATA YSM							
0	RAM DATA YSL; TRANSCEIVER DATA							
Register \ Bit	7	6	5	4	3	2	1	0

— = Reserved (modem use only) * 11088 only

Interface Memory Bank 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS B							
E	IA1	EYE/TX	=	TXI	TX0	IE1	AUDIO	MDA1
D	—	—	—	OHRC*	ALC1*	ALC0*	FRT	RAMWB
C	RX0	SETUP2	FDEN	TL3	TL2	TL1	TL0	—
B	FR3	FR2	FR1	—	—	—	—	—
A	COL4	COL3	COL2	COL1	ROW4	ROW3	ROW2	ROW1
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	$\overline{PNDET}$	FLAG	RINGIN	—	—	=	$\overline{CDET}$
6	—	—	—	—	—	—	—	—
5	—	$\overline{FED}$	—	—	—	—	—	PD*
4	MUEN**	RDREN**	—	—	=	$\overline{P2DET}$	CTSP	=
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register \ Bit	7	6	5	4	3	2	1	0

— = Reserved (modem use only) *11088 only **11087/77 only = Reserved

Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
None	Transceiver Data	0:0:0-7	In receiver parallel mode, the modem presents eight bits of channel data in register 0:0 for reading by the host microprocessor. After the eight bits have been accumulated in register 0:C, they are transferred to 0:0 and bit 0:E:0 goes to a one. When the host reads 0:0, bit 0:E:0 resets to a zero. The first bit of received data is not necessarily located in bit 0:0:0. The host must frame the received data by searching for message sync characters. Bit 0:E:0 sets at one eighth the bit rate in parallel data mode rather than at the sample rate (9600 Hz) as it does when reading RAM locations. In transmit parallel data mode the host stores data at location 0:0. This action causes bit 0:E:0 to reset to a 0. When the modem transfers the data from 0:0 to 0:2 bit 0:E:0 sets to a 1. The data is serially transmitted from register 0:2 least significant bit first. Received data is shifted into register 0:C fror MSB toward LSB.
None	RAM DATA	0:0:0-7	Least significant byte of 16-bit word y used in reading or writing RAM location in Chip 0 (sample rate device). Shared by parallel data mode for presentinf channel data to the host microprocessor bus. See Transceiver Data and DA0.
None	RAM DATA	0:1:0-7	Most significant byte of 16-bit word y used in reading or writing RAM location in Chip 0 (sample rate device).

Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
None	RAM DATA	0:2:0-7	Least significant byte of 16-bit word x used in reading RAM location in Chip 0 (sample rate device).
None	RAM DATA	0:3:0-7	Most significant byte of 16-byte word x used in reading RAM location in Chip 0 (sample rate device).
(None)	FREQL/FREQM	0:2:0-7, 0:3:0-7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below.

FREQM Register (0:3)

Bit:	7	6	5	4	3	2	1	0
Data Word:	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}

FREQL Register (0:2)

Bit:	7	6	5	4	3	2	1	0
Data Word:	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

The frequency number (N) determines the frequency (F) as follows:

F = (0.146486) (N) Hz ± 0.01%.

Hexadecimal frequency numbers (FREQM, FREQL) for commonly generated tones are given below:

Frequency (Hz)	FREQM	FREQL
462	0C	52
1100	1D	55
1650	2C	00
1850	31	55
2100	38	00

None	Configuration	0:4:0-7	The host processor configures the modem by writing a control code into the configuration register in the interface memory space. (See SETUP.)

Control codes for the 19 available configurations (12 for facsimile applications and 7 for full duplex data transmission) are:

CONFIGURATION	CONFIGURATION CODE (HEX)
A. Facsimile Applications	
1. V.29 (9600)	14
2. V.29f (7200)	12
3. V.27 (4800)	0A
4. V.27f (2400)	09
5. V.21 FAX	20
6. Group 2	40
7. Group 1 (1)	41
8. Group 1 (2)	42
9. Group 1 (3)	43
10. Tone mode	80
11. DTMF mode	81
12. Voice Mode	82

Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description

CONFIGURATION	CONFIGURATION CODE (HEX)
B. Data Applications	
1. V.22bis (2400)	20
2. V.21 (300)	21
3. V.22 (1200)	22
4. V.23 (1200)	23
5. CMP	24
6. Bell 103	25
7. Bell 212	26

CONFIGURATION DEFINITIONS (cont'd)

A. Facsimile Applications

1. *V.29.* When a V.29 configuration has been selected, the modem operates as specified in CCITT Recommendation V.29.
2. *V.27.* When a V.27 configuration has been selected, the modem operates as specified in CCITT Recommendation V.27 ter.
3. *FSK.* The modem operates as a CCITT T.30 compatible 300 bit/s FSK modem having characteristics of the CCITT V.21 channel 2 modulation system.
4. *Group 2.* The modem operates as a CCITT T.3 compatible AM modem. This configuration permits transmission to and reception from Group 2 facsimile apparatus. A carrier frequency of 2100 Hz is used. A black signal is transmitted as no carrier. The phase of the carrier representing white is reversed after each transition through black.

   When in the receive state, the modem recovers the carrier of the remote transmitting modem to perform a coherent demodulation of the incoming signal. This technique allows a baseband of 3400 Hz to be recovered. The recovered baseband signal is available on the microprocessor bus.

   The baseband signal is converted to black or white by comparing the received signal level with a preset threshold number. This number may be changed by the user.

   Receiver data is presented to the RXD output at a rate of 10368 samples per second. The user should strobe the data on the rising edge of the data clock (DCLK). A logical 1 level (high voltage) represents white. A logical 0 level (low voltage) represents black.
5. *Group 1.* The modem operates as a CCITT T.2 compatible FSK modem. This configuration permits transmission to and reception from Group 1 facsimile apparatus. Modulation method is FSK. The frequencies are:

   Black: 2400 Hz

   White: 1500 Hz

   The input data is clocked in at a rate of 5184 Hz. To reduce bandwidth the black pixels are extended by n trailing pixels, where n is selected among 1, 2 or 3. The corresponding configuration codes are 41, 42 or 43.
6. *Tone Mode.* In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by the user. Two registers in the host interface memory space contain the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents 0.146486 Hz ± 0.01%. The frequency generated is:

   $f = 0.146486 (256 * FREQM + FREQL)$ Hz ± 0.01%.

Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
			7. *DTMF Mode.* In this configuration, activating RTS causes the modem to transmit two tones at frequencies and output levels specified by the user. By using the RAM Data Access routines, the user can program the tones and levels. When RTS is deactivated, the tone transmitter is halted and the circuit enters the tone detection mode. The detected results are output to R0, R1, C0 and C1. VTD will go high when a valid tone is detected and will stay high as long as the tone is valid. 8. *Voice Mode.* When the Voice Mode Configuration is selected, the A/D and the D/A converters are available for voice reception and transmission. **B. Data Modem Applications** 1. *V.22bis.* This mode provides full duplex information transmission over the GTSN. Its operation complies to CCITT recommendation V.22bis (modulation scheme: 16 QAM). 2. *V.21.* When selected, this mode provides 300 bit/s full duplex transmission over the GTSN (modulation scheme: FSK). 3. *V.22.* This mode provides 1200 bit/s CCITT recommendation V.22 compatible full duplex transmission over the GTSN (modulation scheme: QPSK). 4. *V.23.* This mode provides full duplex asymmetrical data transmission over the GTSN. Its operation complies to CCITT V.23 (modulation scheme: FSK). 5. *CPM.* This mode detects the presence of busy tone, reorder tone and ring tone. 6. *Bell 103.* The operation of this mode is very similar to the CCITT V.21 standard, except that its carrier frequencies (both high and low band) are different from V.21 (modulation scheme: FSK). 7. *Bell 212.* This mode is similar to the CCITT V.22 but with different carrier frequencies (modulation scheme: QPSK).
DL	Digital Loopback	0:9:7	When configuration bit DL is a one, the modem is manually placed in digital loopback. DL should be set during the data mode. DSR and CTS will be at zero. The local modem can then be tested from the far-end by using the terminal equipment at the far-end to transmit a test pattern and examine the looped data. At the far end modem, all interface circuits behave normally as in the data mode. At the conclusion of the test, DL must be reset to zero. The local modem will then return to the normal data mode with control reverting the DTEs, DTR. (V.22bis, V.22)

Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
RDL	Remote Digital Loopback	0:9:6	When configuration bit RDL is a one, it causes the modem to initiate a request for the remote modem to go into digital loopback. (V.22bis, V.22)
AL	Analog Loopback	0:9:5	When configuration bit AL is a one, the modem is placed in (V.54 Loop 3) local analog loopback. In this loop, the transmitter's analog output is coupled to the receiver's analog input at a point near the modem's telephone line interface. An attenuator is introduced into the loop such that the signal level coupled into the receive path is attenuated 14+/-1dB. (V.22bis, V.22, V.21, 103)
ERDL	Enable Respond to Remote Digital Loopback	0:9:4	When configuration bit ERDL is a one, it enables the modem to respond to another modem's remote digital loopback request, thus going into loopback. When 0 no response will be generated.
ORG	Originate/Answer	0:9:3	When configuration bit ORG is a one, it puts the modem in originate mode and when a zero answer mode. (V.22bis, V.22, V.23, V.21, 103)
ST	Self test	0:9:2	When configuration bit ST is a one, self test is activated. ST must be at zero to end the test. It is possible to perform test with or without DTE connected. During any self test do not test asynchronous to asynchronous converter circuits in either the transmitter or receiver. Error detection is accomplished by monitoring the self test error counter in the RAM. If the counter increments during the self test, an error was made. The counter contents are available in the diagnostic register when the RAM access code 00 is loaded in the diagnostic control register (0:F). Self Test End to End Upon activation of self-test an internally generated data pattern of alternate binary ones and zeros (reversals) at the selected bit rate are applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals are connected to the output of the descrambler. Self Test with Loop 3 Loop 3 is applied to the modem as defined in recommendation V.54. Self-test is activated and DCE operation is as in the end to end test. In this test DTR is ignored. Self Test with Loop 2 The modem is conditioned to instigate a loop 2 at the remote modem as specified in recommendation V.54. Self-test is activated and DCE operation is as in the end to end test. (V.22bis, V.22, V.21, 103)
TM	Test Mode	0:9:1	When status bit TM is a one, it indicates that the modem has completed the handshake and is in one of the following test modes: AL, RDL, or DL. (V.22bis, V.22, V.21, 103)

Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
SYNC	Synchronous Mode	0:9:0	When configuration bit SYNC is a one, the modem is operated in synchronous mode, when 0 in async mode. This bit is not used in the fax mode.
DTR	Data Terminal Ready	0:8:7	Control bit DTR must be a one, before the modem will enter the data state, either manually or automatically. DTR must also be at a one in order for the modem to automatically answer an incoming call. (V.22bis,V.22, V.21, 103, V.23)
DSR	Data Set Ready	0:8:6	The on condition of the status of the status bit DSR indicates that the modem is in the data transfer state. The off condition of DSR is an indication that the DTE is to disregard all signals appearing on the interchange circuits- except RI, DSR will switch to the off state when indicates the following: The modem is not in the talk state, i.e. an associated telephone handset is not in control of the line. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing. The modem has generated an answer tone or detected answer tone. After ring indicate goes on, DSR waits at least two seconds before turning on to allow the telephone company equipment to be engaged. DSR will go off 50 msec after DTR goes off or 50 msec plus a maximum of 4 sec when the SSD bit is enabled.
RXMARX	Receive Mark	0:8:5	When RXMARX bit is a one in receive mode, the receive data is clamped to mark. (V.22bis,V.22, V.21, 103, V.23)
DATA/FAX	Data Mode/ Fax Mode	0:8:4	When the configuration bit DATA/FAX is a one, the modem is operated in data mode, when zero it selects the FAX mode.
GTS	Guard Tone Select	0:8:1	When configuration bit GRS is a zero, it selects the 1800 Hz tone and when a one it selects the 550 Hz tone. (V.22bis, V.22)
GTE	Guard Tone Enable	0:8:0	When configuration bit GTE is a one, it causes the specified guard tone to be transmitted (CCITT Configurations only).
DISS	Disable Scrambler	0:7:7	When configuration bit DISS is a one, the scrambler in the DSP processor is disabled.
LL	Lease Line	0:7:6	When configuration bit LL is a one, it places the modem in leased line operation. When LL is set the modem immediately goes OFF-HOOK and into data mode.
WS1 - WS0	Word Length Select	0:7:5-4	These character length bits select either 8,9, 10, 11 bit characters (includes data, stop, and start bits) as shown below: Configuration / WS1 / WS0 8 bits / 0 / 0 9 bits / 0 / 1 10 bits / 1 / 0 11 bits / 1 / 1 (V.22bis,V.22, V.21, 103, V.23)
RSD	Receive Space Disconnect	0:7:3	When configuration bit RSD is a one, it causes the modem to go on-hook after receiving approximately 1.6 seconds of continuous spaces. (V.22bis,V.22, V.21, 103)

Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
SSD	Send Space Disconnect	0:7:2	When configuration bit SSD is a one, it causes the modem to send approximately 1.6 seconds of continuous space before going on-hook. (V.22bis, V.22, V.21, 103)
SPEED	Speed Indicate Bits	0:7:1-0	When status bits are active they reflect the speed at which the modem is operating. The SPEED bit representations are shown. 00 = 0 to 300 bit/s 10 = 1200 bit/s 01 = 1200/75 bit/s 11 = 2400 bit/s (V.22bis, V.22, V.21, 103, V.23)
RTS	Request to Send	0:5:7	The one state of RTS begins a transmit sequence. The modem will continue to transmit until RTS is turned off, and the turn-off sequence has been completed. RTS parallels the operation of the hardware/RTS control input. These inputs are "ORed" by the modem.
TDIS	Training Disable	0:5:6	If TDIS is a one in the receive state, the modem is prevented from entering the training phase. If TDIS is a one prior to $\overline{RTS}$ going on, the generation of a training sequence is prevented at the start of transmission.
RAMWS	RAM Write Chip 0	0:5:5	RAMWS is set to a one by the host processor when performing diagnostic writes to the sample rate device (chip 0). RAMWS is set to a zero by the host when reading RAM diagnostic data from Chip 0.
RAE	RAM Address Extension	0:5:4	This bit is an extension of RAM Access S when RAMWS is a one. During a RAM write to Chip 0 when RAE is a 1 the XRAM is selected and when RAE is a 0 the YRAM us selected.
EPT	Echo Protect Tone	0:5:3	If EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence. This option is available in both the V.27 and V.29 configurations, although it is not specified in the CCITT V.29 recommendation.
SQEXT	Squelch Extended	0:5:2	The one state of SQEXT inhibits reception of signals for 130 ms after the turnoff sequence.
LRTH	Lower Receive	0:5:0	The one state of LRTH lowers the receiver turn on threshold from -43 dBm to -47 dBm. (See SETUP)
IA0	Interrupt Active (Zero)	0:E:7	IA0 is a one when chip 0 is driving $\overline{IRQ}$ to zero volt.
SETUP	Setup	0:E:3	The one state of SETUP caused the modem to reconfigure to the control word in the configuration register, and to assume the options specified for equalizer (0:5:1), threshold (0:5:0) and (1:E:3-4) the black pixel extending option in Group 1. SETUP returns to zero when acted on by the modem. The time required for the SETUP bit to cause a change depends on the current state of the modem. The following table lists worst case delays.
IE0	Interrupt Enable (Zero)	0:E:2	The one state of IE0 causes the $\overline{IRQ}$ output to be low when the DA0 bit is a one.

Current State	V.21	G2	High Speed Receiver	High Speed Transmitter
DELAY	14 ms	400 us	33 BAUD	2 BAUD + TURN OFF Sequence + Training (if applicable) + SQUELCH (if applicable)

Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
MDA0	Modem Data Available (Zero)	0:E:0	MDA0 goes to one when the modem reads or writes register 0:0. MDA0 goes to zero when the host processor reads or writes register 0:0. MDA0 is used for parallel mode as well as for diagnostic data retrieval.
PDM	Parallel Data Mode	0:F:7	The one state of PDM places the modem in the parallel mode and inhibits the reading of Chip 0 diagnostic data.
None	RAM Access S	0:F:0-6	Contains the RAM access code used in reading or writing RAM locations in Chip 0 (sample rate device).
None	RAM Access B	1:F:0-7	Contains the RAM access code used in reading or writing RAM locations in Chip 1.
IA1	Interrupt	1:E:7	IA1 is a one when Chip 1 is driving $\overline{IRQ}$ to zero volt.
EYE/TX	Eye/Normal Mode	1:E:6	When EYE/TX is a one, the transmit DAC operates in the eye pattern monitor mode. When EYE/TX is zero, it operates in the normal mode. (See SETUP2). To display the eye pattern, connect the X, Y inputs of an oscilloscope to the TP1 an TP2 on the module.
TX0-TX1	Transmit Section Control	1:E:3-4	TX1 and TX0 control the transmit signal path output according to the following table. (See SETUP2) TX1 TX0 PATH 0 0 Normal mode. Modem transmit signal is connected to TXOUT pin. Auxiliary input signal is ignored. 0 1 Auxilary mode. The signal on the AUXTX pin is routed to the TXOUT pin. 1 0 Auxiliary & Modem TX mode. The signal on the AUXTX pin is summed with the modem transmit signal and routed to the TXOUT pin. 1 1 Squelch mode. The transmit signal is squelched and TXOUT pin is connected to zero volt. At the power up the modem is configured at Auxiliary & Modem TX mode.
IE1	Interrupt Enable (one)	1:E:2	The one state of IE1 causes the $\overline{IRQ}$ output to be low when the DA1 bit is a one.
AUDIO	Audio out	1:E:1	When AUDIO is one the receiver input signal is routed to the AUDIO OUT pin. When AUDIO is zero, the AUDIO OUT pin is disabled. When the AUDIO OUT pin is enabled, it is advisable to disable the receiver input by setting RX0 to one. (See SETUP)
MDA1	Modem Data Available (one)	1:E:0	MDA1 goes to one when the modem writes register 1:0. MDA1 goes to zero when the host processor reads register 1:0.
FRT	Freeze Taps	1:D:1	When FRT is a one, adaptive equalization taps are prevented from changing.
RAMWB	RAM Write (Chip 1)	1:D:0	RAMWB is set to a one by the host processor when performing diagnostic writes to the baud rate device (Chip 1). RAMWB is set to zero by the host when reading RAM diagnostic data from Chip 1
RXO	Receive Section Input Control	1:C:7	When RXO is one, the analog input of the receive section is connected to ground. When RXO is zero, the input is taken from the line. (See SETUP2)

Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
SETUP2	Setup 2	1:C:6	The one state of SETUP2 causes the modem to reconfigure the analog section to the control word in the interface register, and to assume the options specified for eye pattern control (1:E:6), receive section input control (1:C:7), Audio-out control (1:E:1), Transmit section output control (1:E:3-4), and Transmit level control (1:C:1-4). SETUP2 returns to zero when acted on by the modem.
FDEN	Flag Detector Enable	1:C:5	While the modem is receiving data according to V.29 or V.27ter mode, it is also performing HDLC Flag detection according to the V.21 channel 2 mode. The flag detection can also be performed in the V.21 FSK mode. If FDEN is one the flag detector is enabled. If it is zero, the flag detector is disabled. The detected result is output to the FLAG bit (1:7:5) in the interface register.
TL0–TL3	Transmit Level	1:C:1-4	TL0-TL3 control a 15 step 1dB/step programmable attenuator; the range is 0 – 15dB. The attenuation control is according to the following table. See SETUP2)

TL3	TL2	TL1	TL0	LOSS (dB)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	1	0	0	4
1	0	0	0	8

Mnemonic	Name	Memory Location	Description
FR1–FR3	Frequency 1, 2, 3	1:B:5-7	The one state of FR1, FR2 or FR3 indicates reception of the respective tonal frequency when the modem is configured for FSK and tone receive or Group 2 transmit mode. The default frequencies for FR1, FR2 and FR3 are:

Bit	Frequency (Hz)
FR1	2100
FR2	1100
FR3	462

In Group 2 transmit mode, only FR2 and FR3 detectors are enabled, and their default frequencies are the same as above.

Mnemonic	Name	Memory Location	Description
COL1–COL4 ROW1–ROW4	DTMF Detect	1:A:0-7	Indicate the DTMF detection result in Tone mode.

1	2	3	A	ROW1	697 Hz
4	5	6	B	ROW2	770 Hz
7	8	9	C	ROW3	852 Hz
*	0	#	D	ROW4	941 Hz
COL1	COL2	COL3	COL4		
1209 Hz	1336 Hz	1477 Hz	1633 Hz		

COL4 not supported in SC11087

Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
$\overline{\text{PNDET}}$	Period 'N' Detector	1:7:6	The zero state of $\overline{\text{PNDET}}$ indicates a PN sequence has been detected. $\overline{\text{PNDET}}$ sets to a one at the end of the PN sequence.
FLAG	HDLC Flag	1:7:5	When the HDLC Flag detector is enabled by setting the FDEN (1:C:5) to a one, the one state of the FLAG bit indicates the valid detection of an HDLC Flag.
RINGIN	Ringing Input	1:7:4	The state of the RINGIN bit represents the state of the signal applied to the RINGIN pin after passing through a debounce circuit.
CTSP	Clear To Send Parallel	1:4:1	When set to a 1, status bit CTSP indicates to the DTE that the training sequence has been completed and any data present at TXD or DBUFF (PDM=1) will be transmitted. CTSP parallels the operation of the $\overline{\text{CTS}}$ pin.
$\overline{\text{CDET}}$	Carrier Detector	1:7:0	The zero state of $\overline{\text{CDET}}$ indicates passband energy is being detected, and a training sequence is not present. $\overline{\text{CDET}}$ goes to zero at the start of the data state, and returns to one at the end of the received signal. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$.
$\overline{\text{FED}}$	Fast Energy Detector	1:5:6	The zero state of $\overline{\text{FED}}$ indicates energy is present above the receiver threshold in the passband. $\overline{\text{FED}}$ is not used for Group 2 Facsimile.
$\overline{\text{P2DET}}$	Period '2'	1:4:2	The zero state of $\overline{\text{P2DET}}$ indicates a P2 sequence has been detected. $\overline{\text{P2DET}}$ sets to a one at the start of the PN sequence.
None	RAM DATA XBL	1:2:0-7	Least significant byte of 16-bit work x used in reading RAM locations in Chip 1.
None	RAM DATA XBM	1:3:0-7	Most significant byte of 16-bit work x used in reading RAM locations in Chip 1.
None	RAM DATA RAM YBL	1:0:0-7	Least significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device). See DA1.
None	RAM DATA RAM YBM	1:1:0-7	Most significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device).

PERFORMANCE

Whether functioning in V.27 ter or V.29 configuration, the modem provides the user with unexcelled high performance.

Typical Bit Error Rates

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of -20 dBm as illustrated.

Typical Phase Jitter

At 2400 bit/s, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ration of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bit/s (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 21 dB in the presence of 15° peak-to-peak phase jitter at 300 Hz.

At 7200 bit/s (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 25 dB in the presence of 12° peak-to-peak phase jitter at 300 Hz.

At 9600 bit/s, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 26 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 26 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

The BER curves shown were prepared from data obtained using a PTT communication test system.

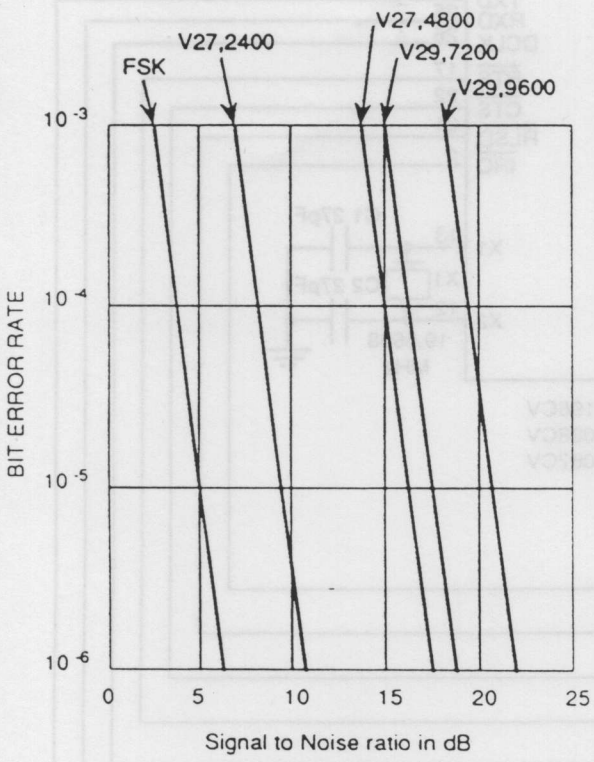


Figure 3
Typical Bit Error Rate
(Back-to-Back, T/2 Equalizer, Level -20 dBm)

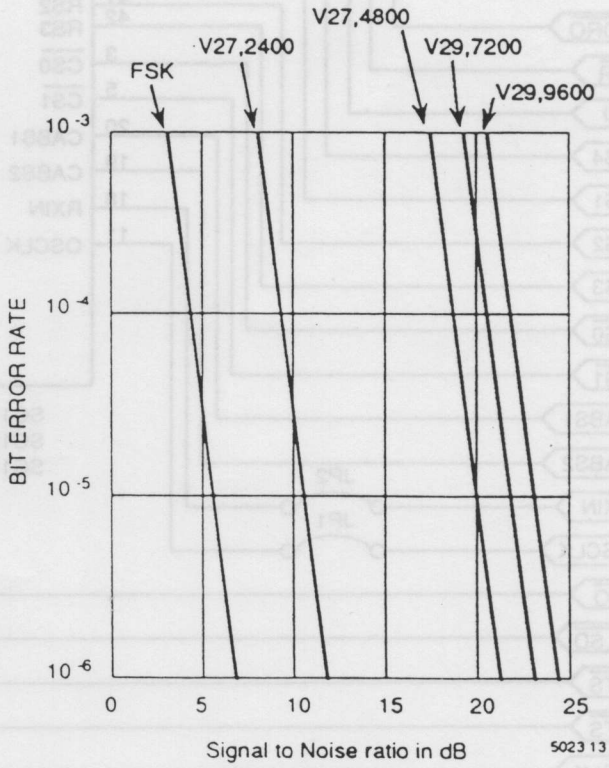


Figure 4
Typical Bit Error Rate
(Unconditioned 3002 Line, T/2 Equalizer, Level -20 dBm)

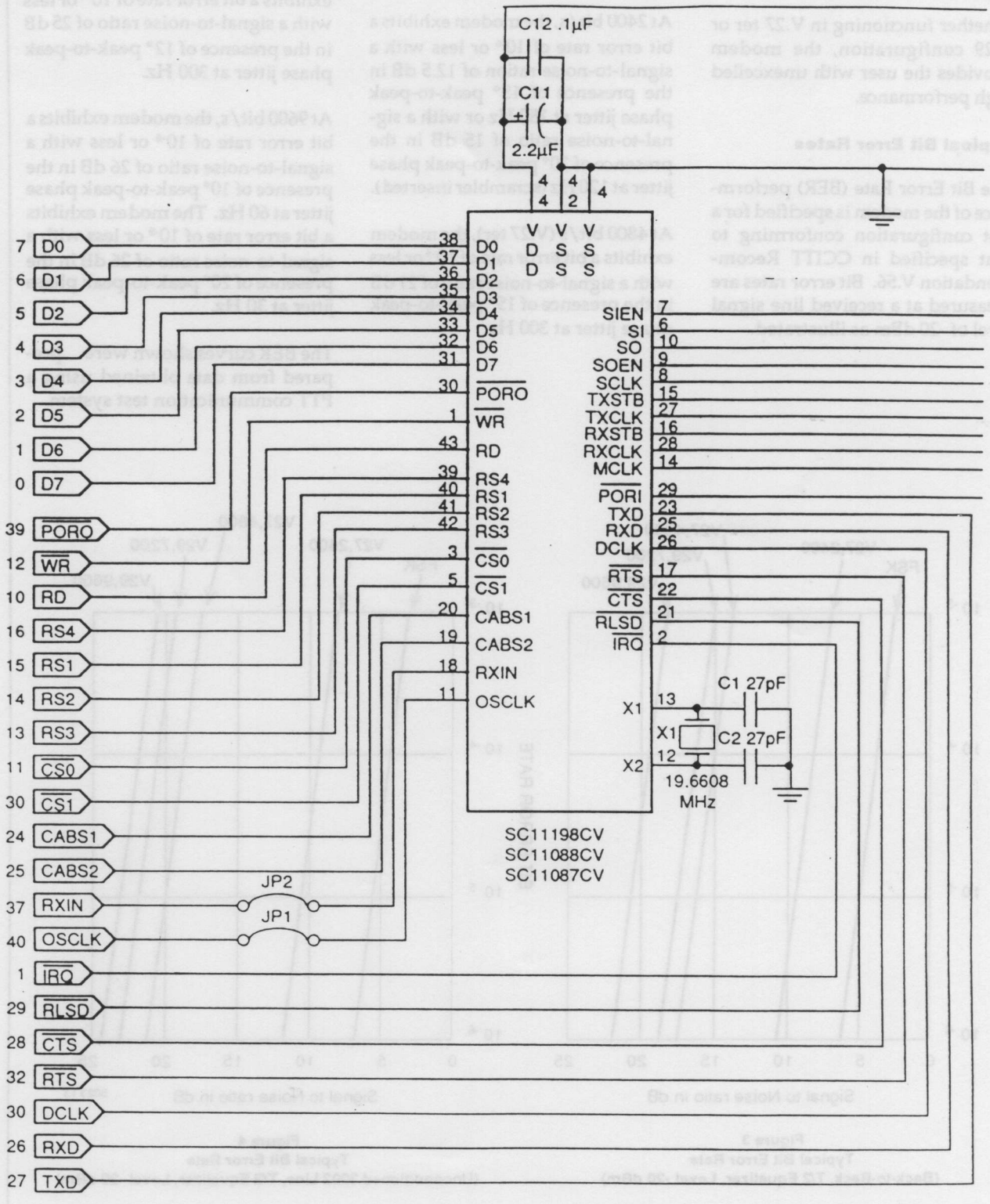
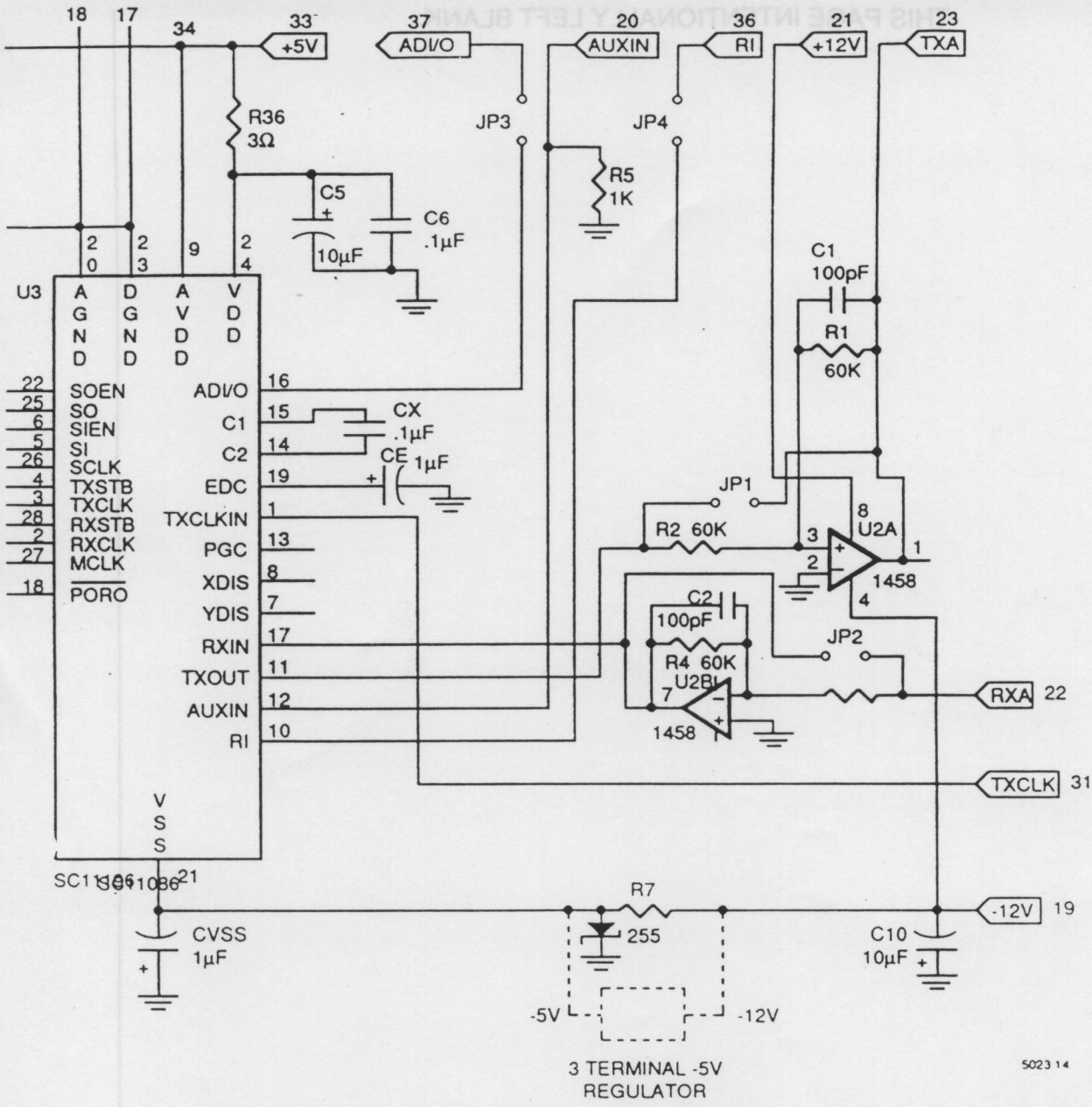

C12 .1µF
C11
2.2µF
4
4
4
4
2
V D D
V S S
V S S
7 D0
6 D1
5 D2
4 D3
3 D4
2 D5
1 D6
0 D7
39 PORO
12 WR
10 RD
16 RS4
15 RS1
14 RS2
13 RS3
11 CS0
30 CS1
24 CABS1
25 CABS2
37 RXIN
40 OSCLK
1 IRQ
29 RLSD
28 CTS
32 RTS
30 DCLK
26 RXD
27 TXD
38 D0
37 D1
36 D2
35 D3
34 D4
33 D5
32 D6
31 D7
30 PORO
1 WR
43 RD
39 RS4
40 RS1
41 RS2
42 RS3
3 CS0
5 CS1
20 CABS1
19 CABS2
18 RXIN
11 OSCLK
SIEN 7
SI 6
SO 10
SOEN 9
SCLK 8
TXSTB 15
TXCLK 27
RXSTB 16
RXCLK 28
MCLK 14
PORI 29
TXD 23
RXD 25
DCLK 26
RTS 17
CTS 22
RLSD 21
IRQ 2
X1 13
X1
X2 12
C1 27pF
C2 27pF
19.6608 MHz
JP2
JP1
SC11198CV
SC11088CV
SC11087CV

Figure 5.



U2 op amp. is not required for dial-up line applications, as the SC11196 can drive 600Ω to 0dBm. For dial-up line remove U2 and close JP1, JP2; then ±12V supply is not required. JP3 may be closed to make use of the AUDIOOUT, an extra input for use when combining a fax and data modem. JP4 provides optional use of the ring input pin.

SK9698 configured as plug-in replacement for R96MD module.

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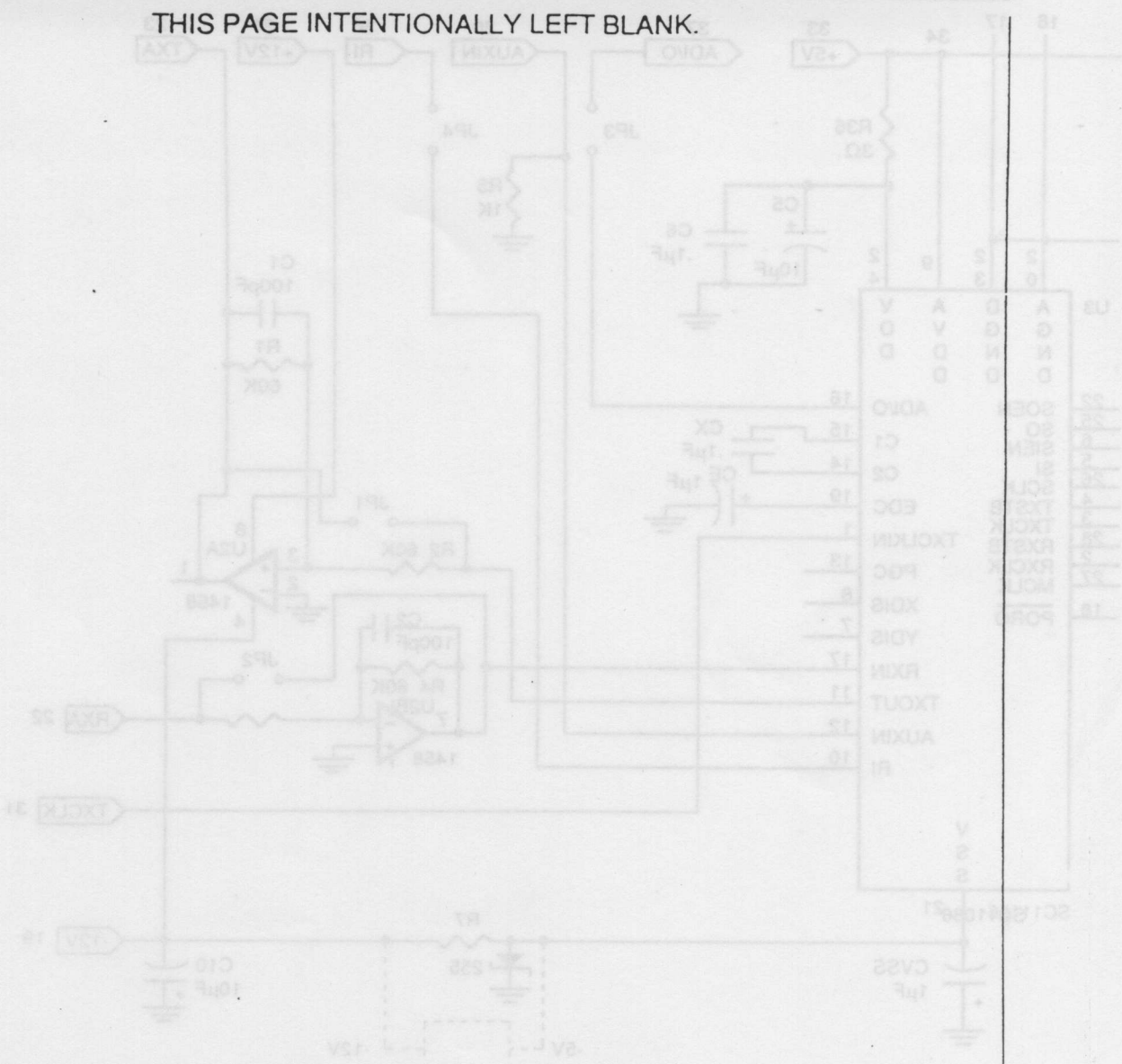

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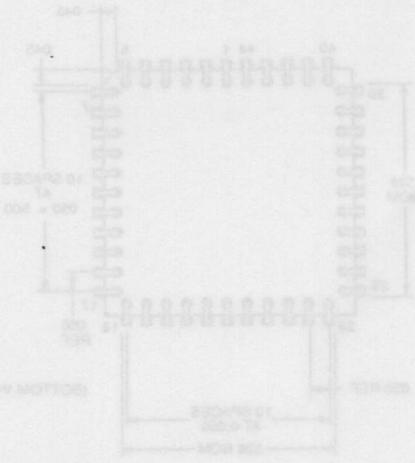
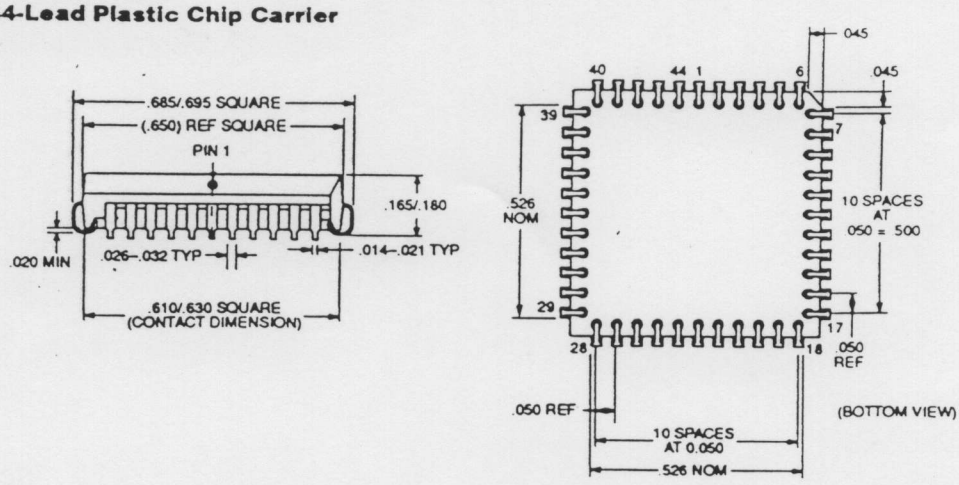


PHYSICAL DIMENSIONS

Package 44-Lead Plastic Chip Carrier



Package 44-Lead PQFP