LINEAR INTEGRATED CIRCUIT

SAJ 210

7-STAGE FREQUENCY DIVIDER FOR ELECTRONIC ORGANS

- HIGH CROSSTALK IMMUNITY - TYP. 70 dB
- OUTPUT SHORT CIRCUIT PROTECTION

The SAJ 210 is a monolithic integrated circuit in a 14-lead quad in-line or dual in-line plastic package. It has been created by means of the standard bipolar technique and especially developed for use as frequency divider for electronic organs. Seven flip-flops connected in 5 groups are housed on one silicon chip. The input and the output of each flip-flop is externally accessible.

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	14 V
V_i	Input voltage	$V_i = V_s$
I_o*	Output current	5 mA
P_{tot}	Power dissipation at $T_{amb} \leq 70$ °C	0.5 W
T_{stg}	Storage temperature	-55 to 125 °C
T_{op}	Operating temperature	0 to 70 °C

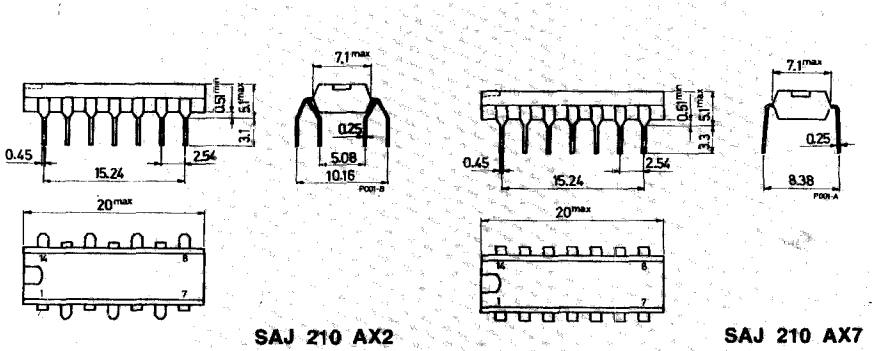
* With reference to Fig. 5, the current can be greater than 5 mA, but for $t < 0.1$ ms

ORDERING NUMBERS:

SAJ 210 AX2 (for 14-lead quad in-line plastic package)
SAJ 210 AX7 (for 14-lead dual in-line plastic package)

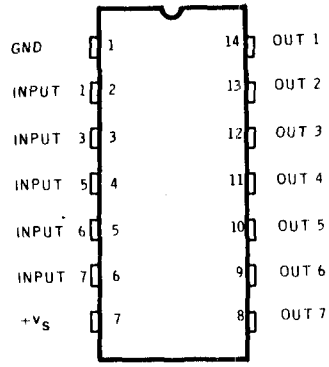
MECHANICAL DATA

Dimensions in mm

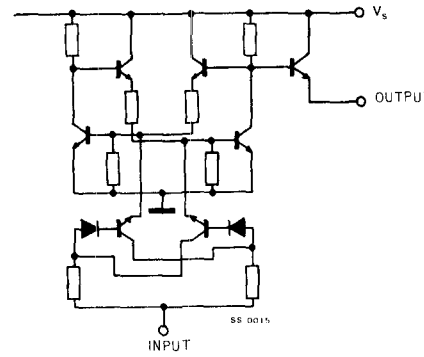


SAJ 210

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(each flip-flop)



ELECTRICAL CHARACTERISTICS
(T_{amb} = 25 °C, V_s = 9 V unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
DATA INPUT						
V_{IL}	Input low level	V_s = 8 to 14 V	0		1.5	V
V_{IH}*	Input high level	V_s = 8 to 14 V	6			V
I_{IH}	Input high level current	V_i = 8 V		1	3	mA
DATA OUTPUT						
V_{OL}	Output low level	R_L = 3 kΩ			0.1	V
V	Output voltage impressed	Low level			6	V
V_{OH}	Output high level	R_L = 3 kΩ V_s = 12 V R_L = 3 kΩ	7 9.5			V V
t_r	Rise time	V_i = 8 V C_L = 10 pF			0.1	µs
t_f	Fall time	R_L = 3 kΩ C_L = 10 pF			0.2	µs
I_d	Total current drain	R_L = 3 kΩ All flip-flops at high level All flip-flops at low level		35 16		mA mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output swing	$R_L = 3\ k\Omega$		7.6		V
**	Cross talk immunity level	$R_L = 3\ k\Omega$ $C_L = 10\ pF$		70		dB
R_o	Dynamic output resistance	V_o impressed = 0 to 2 V				
		at high level		160		Ω
		at low level	1	6		MΩ
	Ripple on output voltage at 2 f out (peak to peak)	$V_i = 8$ V		5		mV

* Input high level is never reached if the input pulse is lower than 3.5 V

** Two independent dividers are triggered
Divider A: triggering frequency 20 kHz
Divider B: triggering frequency 2240 Hz

$$\text{Cross talk level} = 20 \log \frac{V_o \text{ B } 1120\text{ Hz}}{V_o \text{ B } 10\text{ kHz}}$$

Fig. 1 - Typical input current vs input voltage

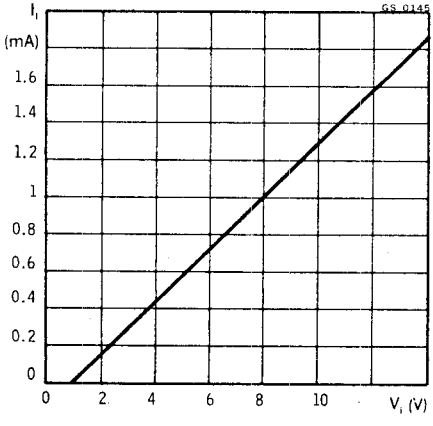


Fig. 2 - Typical output level vs supply voltage

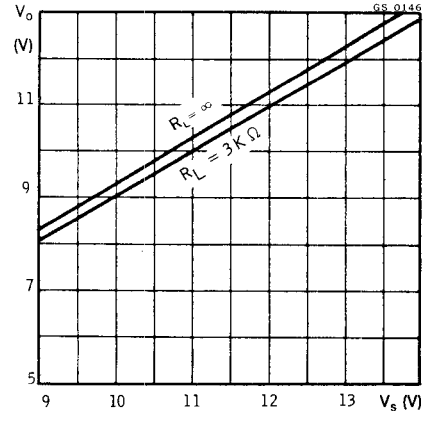


Fig. 3 - Typical input voltage for triggering

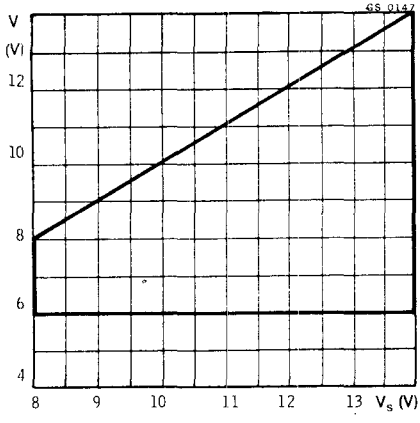


Fig. 4 - Power rating chart

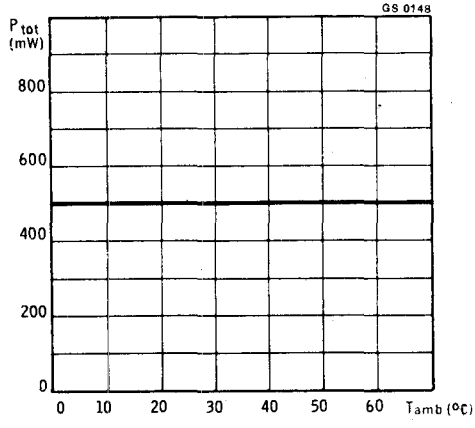
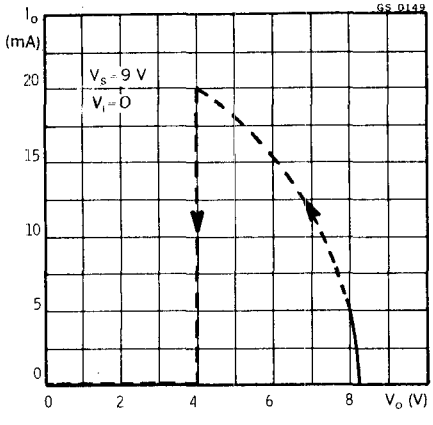


Fig. 5 - Typical output current vs output voltage



TYPICAL APPLICATIONS