SA26066

High-Efficiency, 7V/6A Synchronous Step-Down Regulator

General Description

The SA26066 is a high-efficiency synchronous step-down DC/DC regulator featuring internal power and synchronous rectifier switches capable of delivering 6A of continuous output current over an input voltage range from 3V to 7V.

Silergy's proprietary Instant-PWM™ fast-response, constant-on-time (COT) control method supports high input/output voltage ratios (low duty cycles) and responds to load transients within approximately 100ns, while maintaining a near-constant operating frequency over line, load, and output voltage ranges. This control method provides stable operation without complex compensation, even with low-ESR ceramic capacitors.

Internal 22.1mΩ power and 8.1mΩ synchronous rectifier switches provide excellent efficiency over a wide range of applications, especially for low output voltages and low duty cycles. Cycle-by-cycle current limit, input undervoltage lock-out, internal soft-start, output undervoltage/overvoltage protection, and thermal shutdown provide safe operation in all operating conditions.

The SA26066 is available in a compact QFN2mmx3mm-14 package.

Features

- 3V to 7V Input Voltage Range
- Up to 6A Output Current
- ±1% Reference Voltage over -40°C to +125°C Junction Temperature Range
- Internal 22.1mΩ Power Switch and 8.1mΩ Synchronous Rectifier
- Instant-PWM™ Provides Fast Transient Response
- 660kHz,1100kHz, and 2200 kHz Operating Frequency
- Selectable PFM/FCCM Operation
- Programmable Valley Current Limit
- Cycle-by-Cycle Valley and Peak Current Limit (OCP) and Reverse Current Limit if FCCM is Selected
- Automatic Recovery for Output Overvoltage (OVP), Output Undervoltage (UVP), and Overtemperature (OTP)
- Hiccup Mode after 32 Consecutive Cycles of Valley Current-Limit Protection
- Pre-Biased Startup
- Power-Good Indicator
- RoHS-Compliant and Halogen-Free
- Compact Package: QFN2mmx3mm-14
- AEC-Q100 Qualified for Automotive Applications

Applications

- Telecom and Networking Systems
- Servers
- High-Power AP
- Automotive

Typical Application

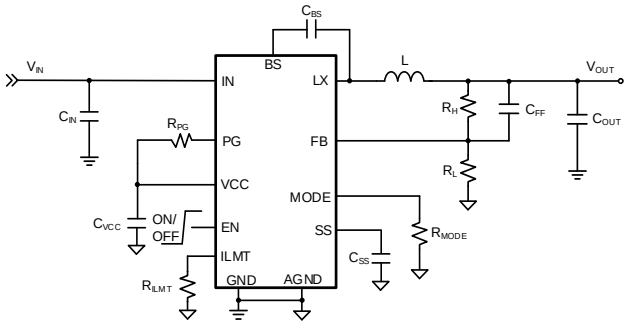


Figure 1. Application Circuit

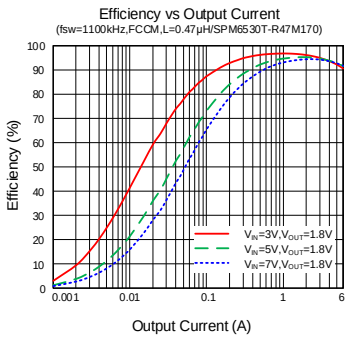


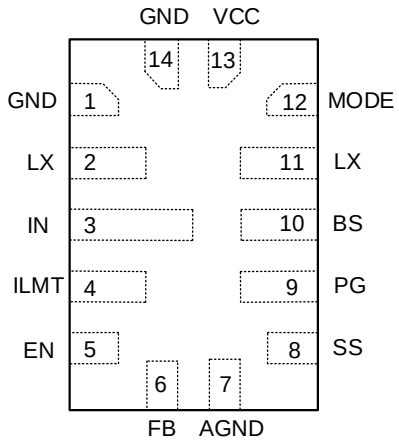
Figure 2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SA26066WYQ	QFN2×3-14 RoHS-Compliant and Halogen-Free	**GME*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1, 14	GND	Power GND.
2, 11	LX	Inductor pin. Connect this pin to the switching node of the inductor.
3	IN	Input pin. Decouple this pin to the GND pin with at least a 30μF ceramic capacitor.
4	I_{LMT}	Synchronous rectifier current-limit setting. Connect a resistor to AGND to set the inductor valley current-limit value.
5	EN	Enable input. Pull low to disable the device and pull high to enable the device. Do not leave this pin floating. May be used for increasing startup voltage or sequencing.
6	FB	Feedback sense. Connect this pin to the center point of the output resistor-divider to program the output voltage.
7	AGND	Analog ground.
8	SS	External soft-start setting. Optionally adjust the soft-start time by adding an appropriate external capacitor between this pin and the AGND pin.
9	PG	Power-good indicator. Open-drain output when the output voltage is within 92.5% to 116.5% of the regulation set point.
10	BS	Bootstrap supply for the high-side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.
12	MODE	Operation mode selection. Program MODE to select FCCM/PFM and the operating switching frequency.
13	V_{CC}	Internal 3V LDO output. Power supply for internal analog circuits and the driving circuit. Decouple this pin to AGND with at least one 1μF ceramic capacitor. Use short, direct connections and avoid the use of vias.

Block Diagram

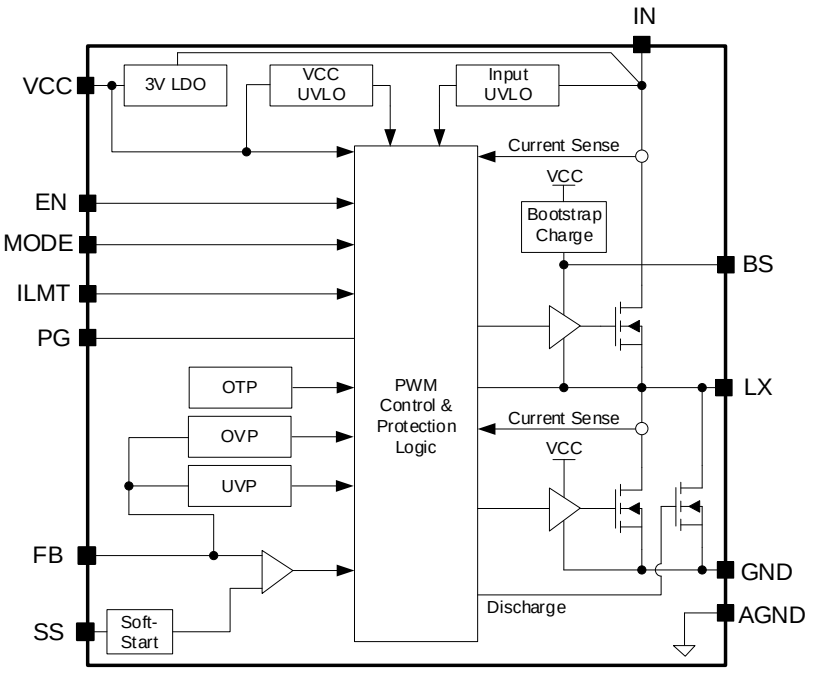


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	10	V
LX	-0.3	V_{IN} + 0.3	
LX, 25ns Duration	GND - 5	V_{IN} + 5	
BS	V_{LX} - 0.3	V_{LX} + 4	
FB, AGND, V_{CC}, EN, PG, MODE, SS, I_{LMT}	-0.3	4	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	35	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	6	
P_D Power Dissipation T_A = 25°C	2.8	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	3	7	V
Junction Temperature	-40	125	°C

Electrical Characteristics

(V_{IN} = 5V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise specified (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V_{IN}		3		7	V
	UVLO, Rising	$V_{IN,UVLO}$	V_{CC} = 3V	2.25	2.55	2.85	V
	UVLO, Hysteresis	$V_{IN,HYS}$			500		mV
	Shutdown Current	I_{SHDN}	V_{EN} = 0V, T_J = 25°C		4	10	μA
	Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 0.62V, PFM mode, no Switching		850	1250	μA
V_{CC}	UVLO, Rising	$V_{VCC,UVLO\_RISE}$		2.6	2.8	2.95	V
	UVLO, Falling	$V_{VCC,UVLO\_FALL}$		2.3	2.5	2.7	V
	Output Voltage	V_{CC}	I_{VCC} = 0mA	2.88	3	3.12	V
	Load Regulation	$V_{CC,REG}$	I_{VCC} = 25mA		0.8		%V_{CC}
FB	Reference Voltage	V_{REF}		0.594	0.6	0.606	V
	Input Current	I_{FB}	V_{EN} = 2V, V_{FB} = 1V	-50	0	50	nA
Power Switch	On-Resistance	$R_{DS(ON)HS}$	V_{BS-LX} = 3V, T_J = 25°C		22.1	26	mΩ
	Leakage	$I_{HS,LKG}$	V_{EN} = 0V, V_{LX} = 0V		0.01	10	μA
	Current Limit	$I_{LMT,HS}$			11		A
Synchronous Rectifier	On-Resistance	$R_{DS(ON)LS}$	V_{CC} = 3V, T_J = 25°C		8.1	10	mΩ
	Leakage	$I_{LS,LKG}$	V_{EN} = 0V, V_{LX} = 5V		0.04	30	μA
	Reverse Current	$I_{LMT,RVS}$			4		A
	Forward Current	$I_{LMT,BOT}$	R_{ILMT} = 0kΩ	7.5			A
I_{LMT} Pin Output Voltage		V_{ILMT}		1.15	1.2	1.25	V
I_{LMT} Ratio		$I_{ILMT}/I_{LMT,BOT}$	$I_{LMT,BOT}$ > 2A	36	40	44	μA/A
Discharge FET Resistance		R_{DIS}			125		Ω
Enable (EN)	Rising Threshold	$V_{EN,R}$		1.17	1.22	1.27	V
	Threshold Hysteresis	$V_{EN,HYS}$			0.2		V
	Input Current	I_{EN}	V_{EN} = 2V		0		μA
Soft-Start (SS)	Charging Current	I_{SS1}	V_{SS} = 0V		15		μA
	Discharge Current	I_{SS2}	V_{SS} = 1V		120		mA
	Min Soft-Start Time	$t_{SS,MIN}$	C_{SS} = 1nF		2.2		ms
Overvoltage Protection Threshold		V_{OVP}		113.5	116.5	119.5	%V_{REF}
Undervoltage Protection	Threshold	V_{UVP}		45	50	55	%V_{REF}
	Delay	$t_{UVP,DLY}$	(Note 4)		20		μs
UVP/OCP Hiccup On-Time		$t_{HICCUP,ON}$	C_{SS} = 1nF (Note 4)		4		ms
UVP/OCP Hiccup Off-Time		$t_{HICCUP,OFF}$	C_{SS} = 1nF (Note 4)		18		ms

Electrical Characteristics (cont.)

(V_{IN} = 5V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise specified (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Power-Good	Thresholds	V_{PG}	V_{FB} falling, PG from high to low	77	80	83	%V_{REF}
			V_{FB} rising, PG from low to high	89.5	92.5	95.5	
			V_{FB} rising, PG from high to low	113.5	116.5	119.5	
			V_{FB} falling, PG from low to high	102	105	108	
	Delay	$t_{PG,R}$	PG from low to high		1		ms
		$t_{PG,F}$	PG from high to low (Note 4)		20		µs
	Output Low Voltage	$V_{PG,LOW}$	V_{IN} = 0V, Pull PG to 3.3V through 100kΩ Resistor		550	750	mV
			V_{IN} = 0V, Pull PG to 3.3V through 10kΩ Resistor		660	850	
			V_{EN} = 2V, V_{FB} = 0V, I_{PG} = 10mA			0.4	V
	Leakage Current	$I_{PG,LKG}$	V_{PG} = 3.3V			3	µA
Switching Frequency		f_{SW}	R_{MODE} = 60.4kΩ, I_{OUT} = 0A, FCCM, V_{OUT} = 1V, T_J = 25°C	530	660	790	kHz
			R_{MODE} = 0Ω, I_{OUT} = 0A, FCCM, V_{OUT} = 1V, T_J = 25°C	935	1100	1265	
			R_{MODE} = 30.1kΩ, I_{OUT} = 0A, FCCM, V_{OUT} = 1V, T_J = 25°C	1870	2200	2530	
Min On-Time		$t_{ON,MIN}$	I_{OUT} = 3A (Note 4)		50		ns
Min Off-Time		$t_{OFF,MIN}$	I_{OUT} = 3A (Note 4)		180		ns
Thermal Shutdown Temperature		T_{SD}	(Note 4)		160		˚C
Thermal Shutdown Hysteresis		T_{HYS}	(Note 4)		20		˚C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

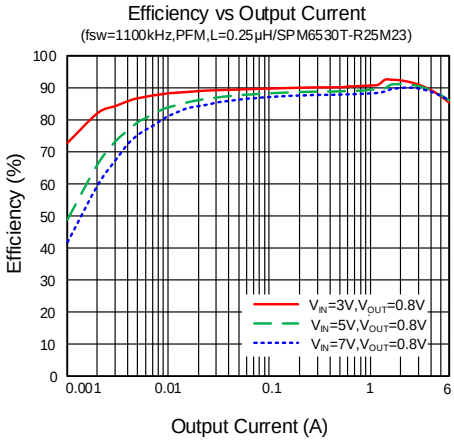
Note 2: θ_{JA} and θ_{JC} are measured in the natural convection at T_A = 25˚C on a 6cm×6cm size four-layer Silergy Evaluation Board.

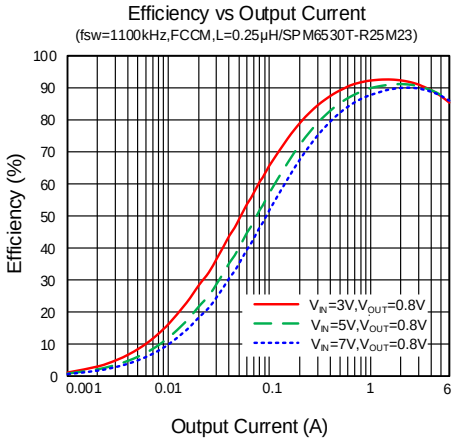
Note 3: The device is not guaranteed to function outside its operating conditions.

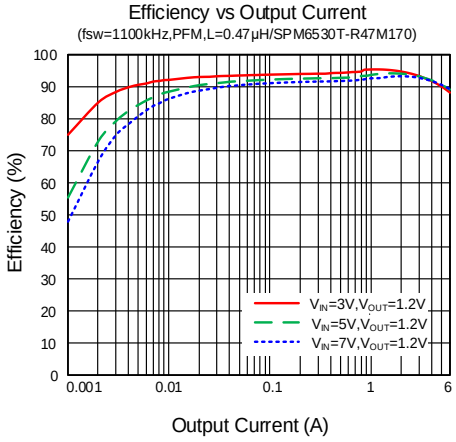
Note 4: Guaranteed by design.

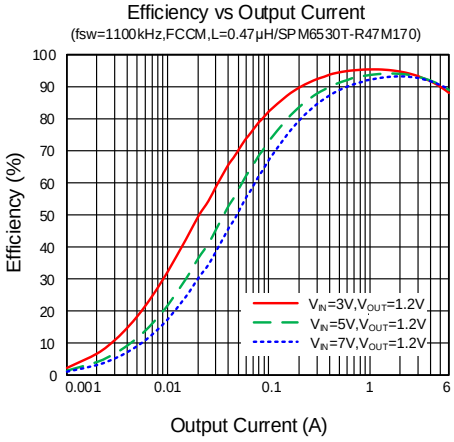
Typical Performance Characteristics

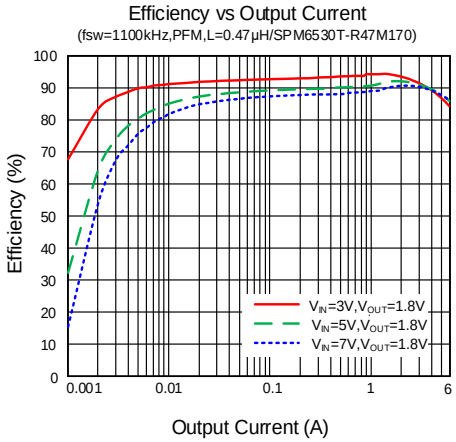
(T_A = 25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L = 0.47μH, C_{OUT} = 94μF, f_{SW} = 1100kHz, R_{ILMT} = 4.7kΩ, unless otherwise noted)

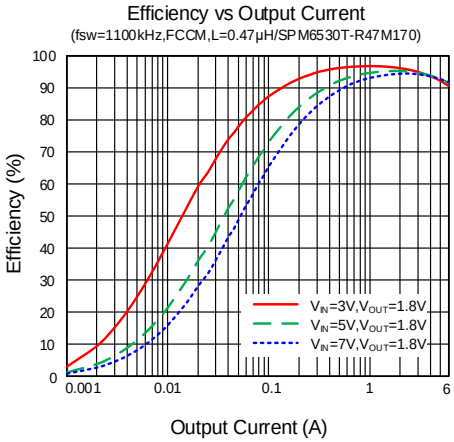




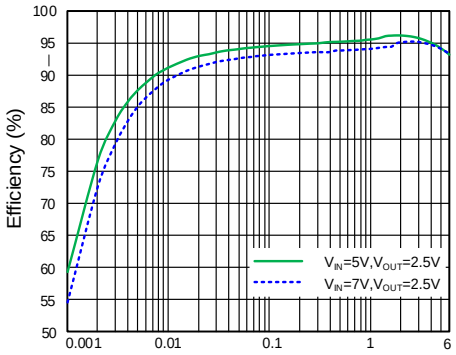






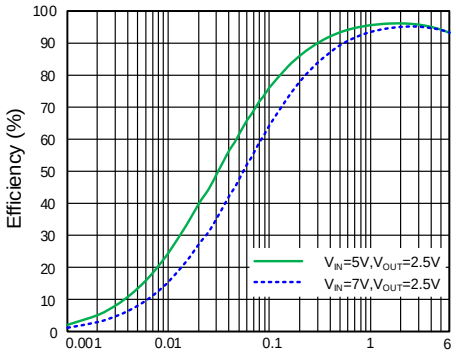


Efficiency vs Output Current
(fsw=1100kHz,PFM,L=0.47μH/SPM6530T-R47M170)



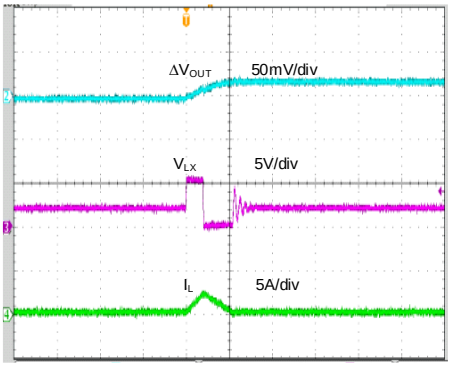
Output Current (A)

Efficiency vs Output Current
(fsw=1100kHz,FCCM,L=0.47μH/SPM6530T-R47M170)



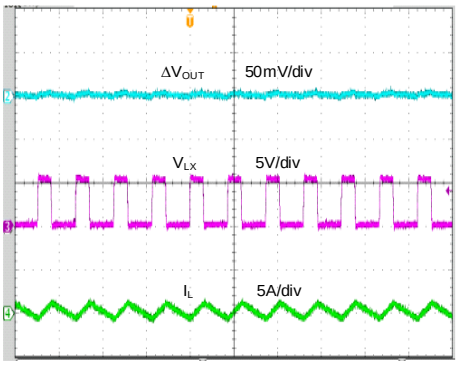
Output Current (A)

Output Ripple
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A，PFM)



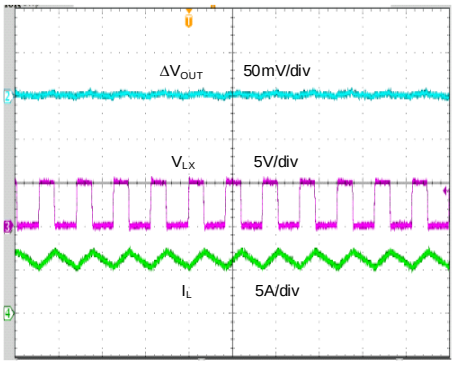
Time (1μs/div)

Output Ripple
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A，FCCM)



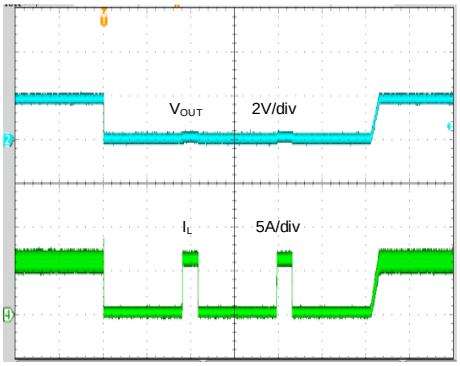
Time (1μs/div)

Output Ripple
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=6A，CCM)



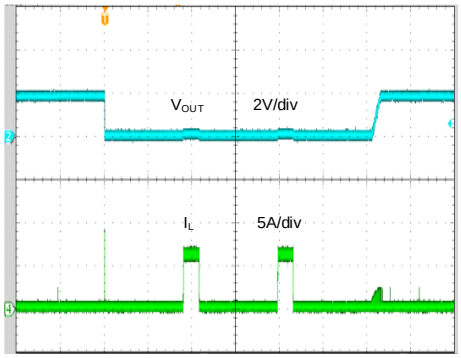
Time (1μs/div)

Short Circuit Protection
V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=6A~Short,CCM)



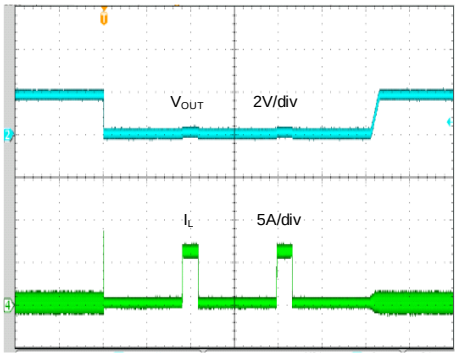
Time (10ms/div)

Short Circuit Protection
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=0A~Short,PFM)



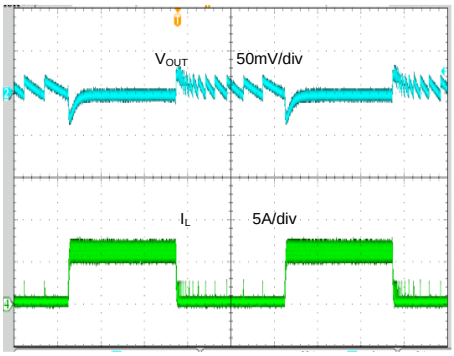
Time (10ms/div)

Short Circuit Protection
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=0A~Short,FCCM)



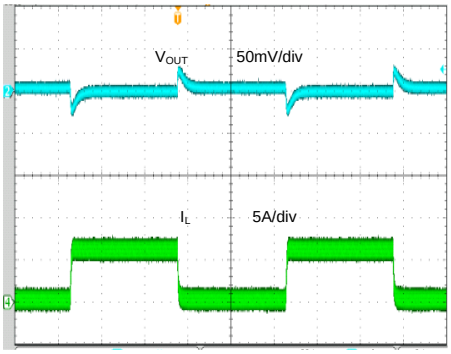
Time (10ms/div)

Load Transient
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=0A~6A, PFM)



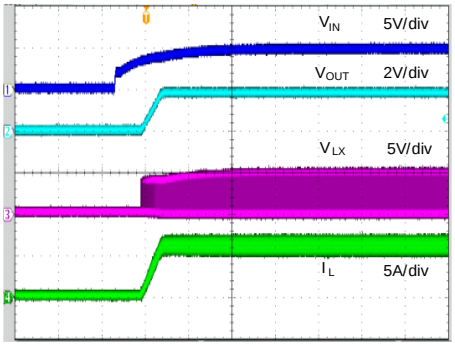
Time (200μs/div)

Load Transient
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=0A~6A, FCCM)



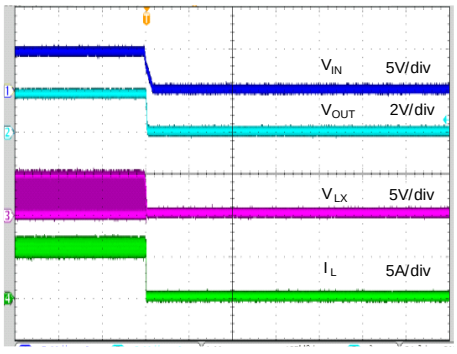
Time (200μs/div)

Start up from V_{IN}
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=6A, CCM)



Time (4ms/div)

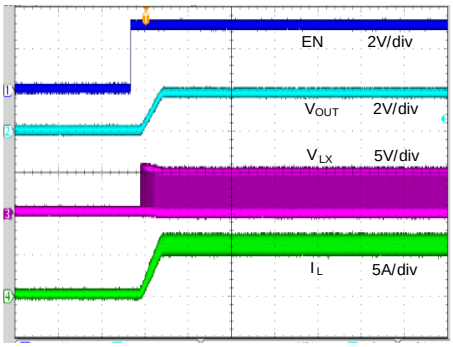
Shutdown from V_{IN}
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=6A, CCM)



Time (4ms/div)

Start up from EN

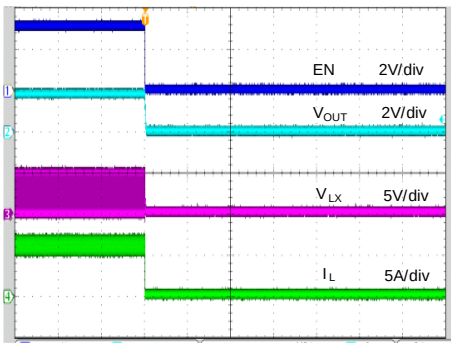
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=6A, CCM)



Time (4ms/div)

Shutdown from EN

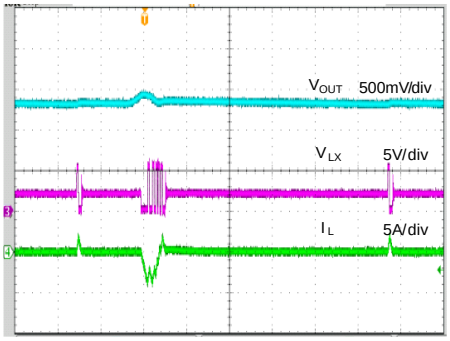
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=6A, CCM)



Time (4ms/div)

OSM Operation

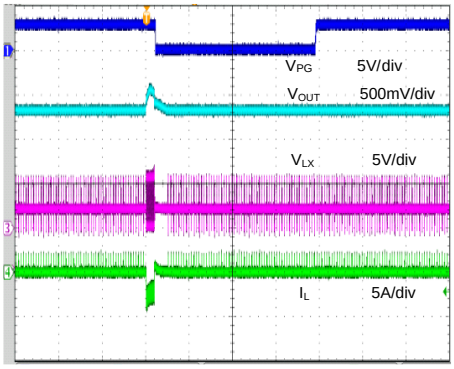
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=50mA, PFM)



Time (10µs/div)

OVP Operation

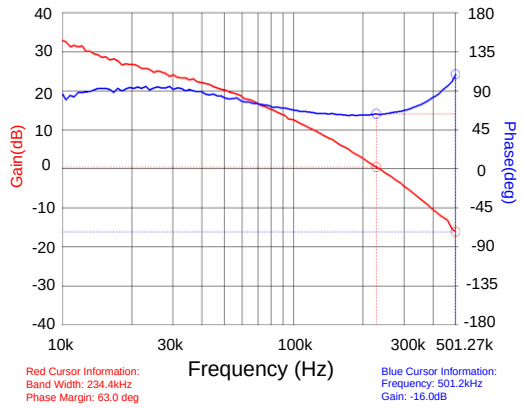
(V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=50mA,PFM)



Time (200µs/div)

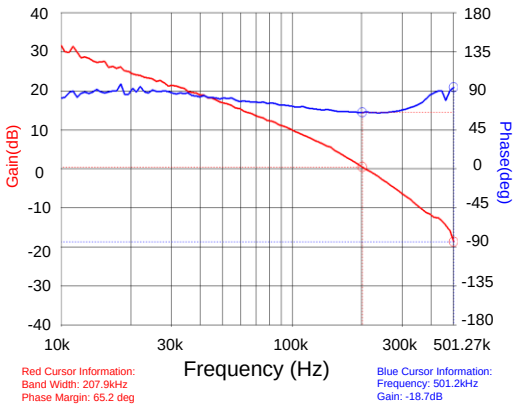
Bode Plot

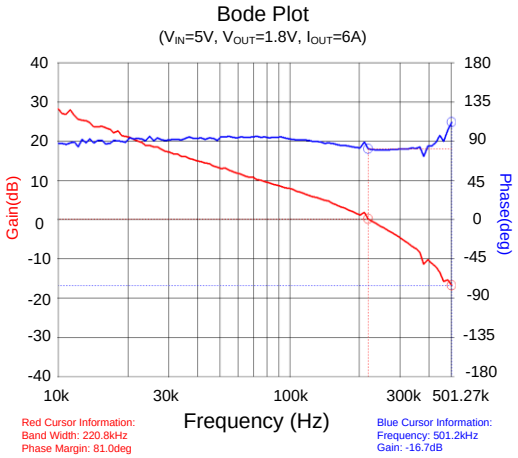
(V_{IN}=5V, V_{OUT}=0.8V, I_{OUT}=6A)

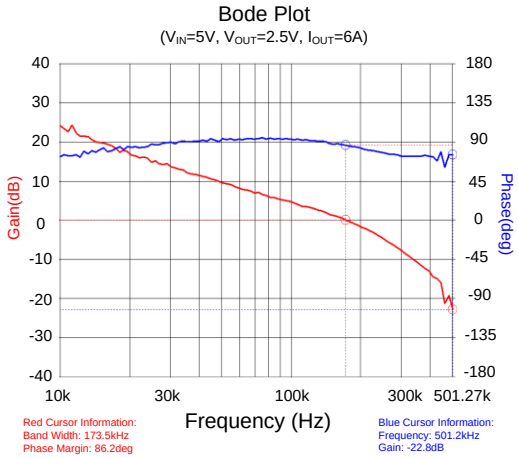


Bode Plot

(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=6A)







Detailed Description

Constant-On-Time Architecture

The one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch, is fundamental to any constant-on-time (COT) architecture. Each on-time (t_{ON}) is a fixed period internally calculated to operate the step-down regulator at the desired switching frequency, considering the input and output voltage ration, $t_{ON} = (V_{OUT}/V_{IN}) \times (1/f_{SW})$. For example, considering that a hypothetical converter targets 1.8V output from a 5V input at 1100kHz, the target on-time is (1.8V/5V)×(1/1100kHz) = 327ns. Each t_{ON} pulse is triggered by the feedback comparator when the output voltage measured at the FB pin drops below the internal voltage reference value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is less than the target. This approach avoids making any switching decisions during the noisy periods immediately after switching events, or while the switching node (LX) is rapidly rising or falling.

There is no fixed clock in the COT architecture, so the high-side power switch can turn on almost immediately after a load transient. Subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. Conventional current-mode or voltage-mode control methods determine when to turn off the high-side power switch and turn on the low-side synchronous rectifier based on current feedback, feedback voltage, internal ramps, and internal compensation signals, so these must all be monitored. These small signals are difficult to observe in a noisy switching environment immediately after switching large currents, which makes such architectures difficult to use.

Instant-PWM Operation

Silergy's instant-PWM control method adds several proprietary improvements to the traditional COT architecture. First, whereas most legacy COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, the instant-PWM control method derives this signal internally.

Additionally, it optimizes operation with low-ESR ceramic output capacitors. In many applications it is desirable to utilize very low-ESR ceramic output capacitors, but legacy COT regulators may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may become too small to maintain stable operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum t_{OFF} has been satisfied and the inductor current measured flowing through the low-side synchronous rectifier is lower than the bottom FET current limit. When the t_{ON} pulse is

triggered, the low-side synchronous rectifier turns off and the high-side power switch turns on. The inductor current then ramps up linearly during the t_{ON} period. At the end of the t_{ON} period, the high-side power switch turns off, the low-side synchronous rectifier turns on, and the inductor current ramps down linearly.

This action also initiates the minimum t_{OFF} timer to ensure sufficient time for stabilizing any transient conditions and settling of the feedback comparator before the next cycle is initiated. This minimum t_{OFF} is relatively short so that transient t_{ON} can be retriggered with minimal delay during high-speed load, allowing the inductor current to ramp quickly and provide sufficient energy to the load.

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between the high-side power switch turn-off and the low-side synchronous rectifier on-period or the low-side synchronous rectifier turn-off and the high-side power turn-on period.

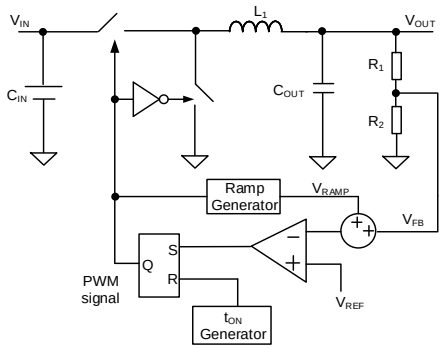


Figure 4. Instant-PWM

Mode Selection

The SA26066 provides both PFM and FCCM operation in light-load conditions, and provides three options for the switching frequency in CCM mode. Set the value of the resistor connected between the MODE pin and AGND or V_{CC} to select the operation mode and switching frequency. See Table 1.

Table 1: Mode Selection

MODE	Light-Load Mode	Switching Frequency
AGND	FCCM	1100kHz
30.1kΩ (±20%) to AGND	FCCM	2200kHz
60.4kΩ (±20%) to AGND	FCCM	660kHz
121kΩ (±20%) to AGND	PFM	660kHz
243kΩ (±20%) to AGND	PFM	2200kHz
V_{CC}	PFM	1100kHz

Programmable Soft-Start Time

The soft-start time can be programmed using the SS pin. Connect one capacitor between the SS pin and the AGND pin to program the soft-start time as follows:

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}}{I_{SS}(\mu A)}$$

The typical value of SS charging current I_{SS} is 15μA. To guarantee the programmable soft-start time is not too short when using a smaller SS capacitor, the device uses a minimum soft-start time of 2.2ms (typical).

Pre-Biased Startup

If the output voltage is not 0V at startup, the power switch and synchronous rectifiers will not begin switching until the soft-start ramp exceeds the sensed output voltage at V_{FB}.

Output Voltage Discharge

The SA26066 discharges the output voltage when the converter shuts down (from V_{IN} falling, EN driven low, or thermal shutdown), so that output voltage can be discharged in a minimal amount of time, even if the output load current is zero. The discharge MOSFET in parallel with the low-side synchronous rectifier turns on after the low-side synchronous rectifier turns off when shutdown logic is triggered. The output discharge resistance is typically 125Ω. Note that the discharge MOSFET is not active outside of these shutdown conditions.

Power-Good Indicator

The power good indicator is an open-drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is greater than 92.5% V_{REF} and less than 116.5% V_{REF} for at least the power-good delay time (low to high), PG will be high-impedance.

PG should be connected to V_{CC} or another voltage source less than 3.6V through a resistor (e.g. 100kΩ). After the input voltage exceeds its own UVLO (rising) threshold, the PG MOSFET is turned on, so that PG is pulled to GND before output voltage is ready. After the feedback voltage V_{FB} reaches 92.5% V_{REF}, PG is pulled high by the external resistor (after a delay time within 1.0ms). When V_{FB} drops to less than 80% of V_{REF}, PG is pulled low (after a delay time within 20μs). When V_{FB} rises to 116.5% of V_{REF}, PG is pulled low immediately.

If the input voltage is zero, PG is clamped low even though PG is connected to an external voltage source through a 10kΩ to 100kΩ pullup resistor.

External Bootstrap Capacitor

The SA26066 integrates a floating power supply for the gate driver of the high-side MOSFET. Proper operation requires a 0.1μF low-ESR ceramic capacitor to be connected between BS and LX.

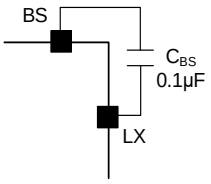


Figure 5. Bootstrap Capacitor Connection

Fault Protection Modes

Overcurrent Protection and Undervoltage Protection

If the high-side power switch current exceeds the peak current-limit threshold, the high-side power switch will turn off and the low-side synchronous rectifier will turn on. If the low-side synchronous rectifier current exceeds the valley current-limit threshold, the low-side synchronous rectifier will keep turning on until the low-side synchronous rectifier current decreases below the valley current-limit threshold. As a result, both peak and valley currents are limited.

The valley current-limit threshold can be programmed using the I_{LMT} pin by connecting a resistor between this pin and AGND. The I_{LMT} output voltage is constant, and the I_{LMT} resistor current is sensed by the device, comparing with the low-side synchronous rectifier current mirror value. If the mirror current is larger than the I_{LMT} resistor current, the device operates in the valley current-limit state, and t_{ON} is inhibited. The valley current-limit threshold equation is:

$$I_{ILMT,VALLEY} = \frac{V_{ILMT}}{G_{MIRROR} \times R_{ILMT}}$$

$$I_{ILMT,OUT} = \frac{V_{ILMT}}{G_{MIRROR} \times R_{ILMT}} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2L \times V_{IN} \times F_{SW}}$$

where $I_{ILMT,VALLEY}$ is the valley configured current limit, $I_{ILMT,OUT}$ is the maximum output current, V_{ILMT} is 1.2V, and G_{MIRROR} is 40μA/A.

If SA26066 detects 32 consecutive cycles of valley current limit protection, or detects 1 cycle of valley current-limit protection when the V_{FB} drops below the undervoltage threshold, the switching will be disabled for a hiccup off-time period.

Reverse-Current Limit

The SA26066 features cycle-by-cycle reverse-current limit. The low-side synchronous rectifier current is continuously monitored, and if the current is lower than the reverse-current limit, the low-side synchronous rectifier is turned off, the high-side power switch is turned on again for the on-time determined by V_{IN}, V_{OUT}, and f_{SW}.

Output-Sinking Mode Protection

The SA26066 includes output-sinking mode. When the FB voltage becomes higher than 106% of V_{REF}, the high-side power switch turns off and the low-side synchronous rectifier turns on until the current flowing through it reaches the reverse-current limit (-4A typical). Then the low-side synchronous rectifier turns off and the high-side power switch turns on again for the on-time determined by V_{IN}, V_{OUT}, and f_{SW}. This sequence continues until the FB voltage falls below 102% of V_{REF}.

Overtemperature Protection

The SA26066 includes overtemperature protection to prevent overheating due to excessive power dissipation. The junction temperature is monitored, and if it exceeds 160°C, the device will shuts down. Once the junction temperature cools down by approximately 20°C, the device will resume normal operation with a complete soft-start cycle.

Minimum Duty Cycle and Maximum Duty Cycle

There is no limitation for minimum duty cycle in COT architecture. This is because when the on-time is close to the minimum value, the switching frequency can be reduced as needed to always ensure proper operation.

The SA26066 can support at least 70% maximum duty cycle operation for the entire temperature range of -40°C –125°C, if the 1100kHz switching frequency is selected.

During PFM light-load operation, when the duty-cycle reaches the maximum value, the device will enter CCM mode even when the load current is low.

Enable and Adjusting Input Undervoltage Lockout

The EN input is a low-voltage-capable input with logic-compatible threshold. The comparator design uses an accurate EN rising threshold. When EN voltage rises to ~0.8V, and V_{CC} is present, the EN comparator is enabled. When EN is driven above 1.22V, normal device operation is enabled. When EN voltage falls below the EN rising threshold by more than the threshold hysteresis $V_{EN,HYS}$, the device is turned off. When EN voltage is driven below ~0.4V, the internal supply will be shut down, reducing input current to <10μA (typ).

A resistor-divider can be used if a higher UVLO threshold is required in the application, as shown in Figure 6. Note that EN voltage should not higher than 3.6V.

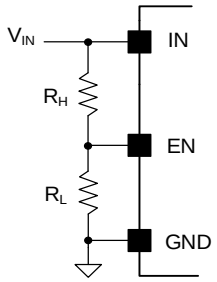


Figure 6. Adjusting Input UVLO

Application Information

Feedback Resistor Selection

Choose R_H and R_L to program the proper output voltage. Choose large resistance values between 1kΩ and 100kΩ for both R_H and R_L to minimize power consumption under light loads. For example, if V_{OUT_SET} is 1.8V, and 10kΩ is selected for the R_H value, then R_L can be calculated as 5kΩ using following equation:

$$R_L = \frac{0.6V}{V_{OUT\_SET} - 0.6V} R_H$$

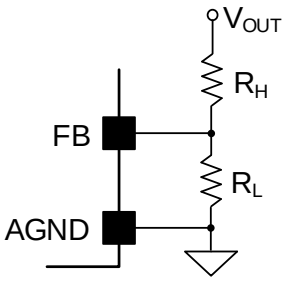


Figure 7. Feedback Resistor

Inductor Selection

Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off between efficiency, cost, and size for a particular application. Selecting a low inductor value will help reduce size and cost, and enhance transient response, but will increase the peak inductor ripple current, reducing efficiency and increasing output voltage ripple. Using a low DC resistance (DCR) for the inductor may help reduce DC losses and increase efficiency. Higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be obtained by selecting a ripple current (ΔI_L) of approximately 20%–50% of the desired full-output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), and the maximum output current ($I_{OUT,MAX}$), then estimating a ΔI_L as some percentage of that current in the recommended range.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

$$I_{L,PEAK} = I_{OUT,MAX} + \Delta I_L/2$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If FCCM light-load operation is selected, make sure the inductor value is high enough to avoid the reverse-current limit being triggered during a steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size, and cost targets. Low-loss ferrite materials should be considered.

Inductor Selection Example

Consider a typical design for a device providing $1.8V_{OUT}$ at 6A from $5V_{IN}$, operating at 1100kHz and using target inductor ripple current (ΔI_L) of 40% or 2.4A. Determine the approximate inductance value at first:

$$L_1 = \frac{1.8V \times (5V - 1.8V)}{5V \times 1100kHz \times 2.4A} = 0.44\mu H$$

Next, select the nearest standard inductance value, in this case 0.47µH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{1.8V \times (5V - 1.8V)}{5V \times 1100kHz \times 0.47\mu H} = 2.2A$$

$I_{L,PEAK}$ = 6A + 2.2A/2 = 7.1A

The resulting 2.2A ripple current is 2.2A/6A (36.7%), well within the 20%–50% target.

$I_{L,PEAK,RVS}$ = 2.2A/2 = 1.1A < $I_{LIM,RVS}$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 7.1A.

Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply, and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long (and therefore inductive) cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

where D is the switching converter duty cycle.

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor determines the input voltage ripple of the converter. If there is a voltage ripple requirement in

the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1\text{-}D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications, a single 10µF X5R capacitor is sufficient. Place the ceramic input capacitor as close as possible to the device IN and GND pins. Note that a small 100nF ceramic capacitor, placed in parallel, is highly recommended to decouple the high-frequency switching noise.

Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Output Voltage Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 2.2A using three 22µF ceramic capacitors, each with an ESR of approximately 6mΩ for a parallel total of 66µF and 2mΩ ESR.

$$V_{RIPPLE,ESR} = 2.2A \times 2m\Omega = 4.4mV$$

$$V_{RIPPLE,ESR} = \frac{2.2A}{8 \times 66\mu F \times 1100kHz} = 3.8mV$$

Total ripple = 8.2mV. The actual capacitive ripple may be higher than the calculated value because the capacitance decreases with the voltage on the capacitor.

Load-Transient Considerations

The SA26066 integrates the compensation components to achieve good stability and fast transient responses. Adding a small ceramic capacitor C_{FF} in parallel with R_H may further speed up the load-transient responses, and is therefore highly recommended for applications with large load-transient step requirements.

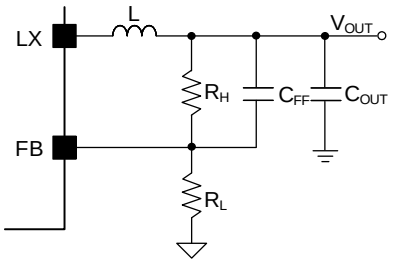


Figure 8. Feed-Forward Capacitor

Thermal Design Considerations

The maximum power dissipation depends on multiple factors: PCB layout, IC package thermal resistance, local airflow, and the junction temperature relative to ambient. The maximum power dissipation may be calculated as:

$$P_{D,MAX} = (T_{J,MAX} - T_A) / \theta_{JA}$$

where $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature should not exceed 125°C. The junction-to-ambient thermal resistance θ_{JA} is layout-dependent. For the QFN2×3-14 package, the thermal resistance θ_{JA} is 35°C /W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2oz. copper traces connected to each IC pin and very large, unbroken 1oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical small evaluation board area requires wide copper traces well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A = 25℃ may be calculated using the following formula:

$$P_{D,MAX} = (125℃-25°C)/(35°C /W) = 2.86W$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.

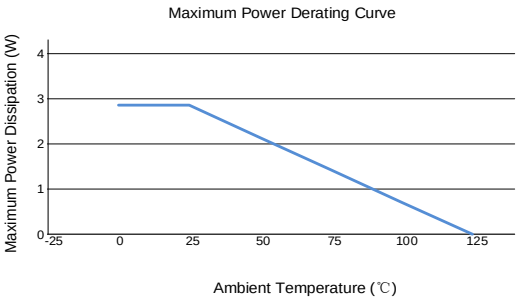
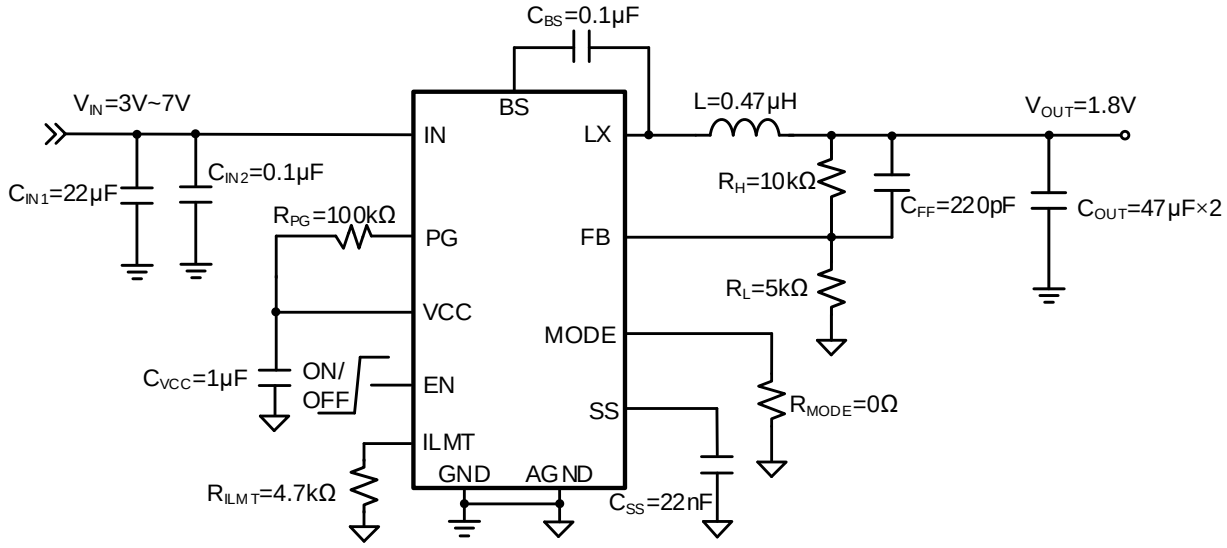


Figure 9. Maximum Power Dissipation

Application Schematic (V_{OUT} = 1.8V)



BOM List

Designator	Description	Part Number	Manufacturer
C_{IN1}	22μF/25V/X5R,1206	GRM31CR61E226ME15L	muRata
C_{IN2}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mμRata
C_{FF}	220pF/50V/C0G, 0603	GRM1885C1H221JA01D	muRata
C_{OUT}	47μF/6.3V/X5R, 1206	GRM31CR60J476KE19L	muRata
C_{SS}	22nF/50V/X7R, 0603	GRM188R71H223KA01D	muRata
C_{BS}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mμRata
C_{VCC}	1μF/50V/X5R, 0603	GRM188R61H105KAALD	muRata
L	0.47μH/inductor	SPM6530T-R47M170	TDK
R_H	10kΩ, 1%, 0603		
R_L	5kΩ, 1%, 0603		
R_{PG}	100kΩ, 1%, 0603		
R_{MODE}	0Ω, 1%, 0603		
R_{ILMT}	4.7kΩ, 1%, 0603		

Recommend Component Values for Typical Applications

V_{OUT}(V)	R_{MODE}(kΩ)	Frequency (kHz)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/(Rated/Saturating Current)	C_{OUT}
0.8	0	1100, FCCM	10	30	220	0.25μH/(10A/14A)	47μF×2/6.3V/X5R, 1206
1.2	0	1100, FCCM	10	10	220	0.47μH/(10A/14A)	47μF×2/6.3V/X5R, 1206
1.8	0	1100, FCCM	10	5	220	0.47μH/(10A/14A)	47μF×2/6.3V/X5R,1206
2.5	0	1100, FCCM	10	3.16	220	0.47μH/(10A/14A)	47μF×2/6.3V/X5R, 1206

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- Place the input capacitor close to the IN and GND pins, minimizing the loop formed by these connections.
- Keep the high current traces as short and wide as possible.
- Place the V_{CC} decoupling capacitor close to the V_{CC} pin.
- Connect AGND and GND at the point of the V_{CC} capacitor's GND pad.
- Connect the feedback sampling point at C_{OUT}, rather than the inductor output terminal.
- Place the FB components (R_H, R_L, and C_{FF}) as close to FB as possible. Avoid routing the FB trace near LX as it is noise sensitive.
- The LX connection has large voltage swings and fast edges, and can easily radiate noise to adjacent components. Keep its area small to prevent excessive EMI, while using a wide copper trace to minimize parasitic resistance and inductance. Keep sensitive components away from the switching node, or add ground shielding around them, to prevent capacitive noise pickup.
- Provide dedicated wide copper traces for the power path ground between the device and the input and output capacitor grounds, rather than connecting each of these individually to an internal ground plane.
- Place vias in GND copper for heat sinking.
- A four-layer layout is strongly recommended to achieve better thermal performance.
- Keep the BS voltage path (BS, LX, and C_{BS}) as short as possible.

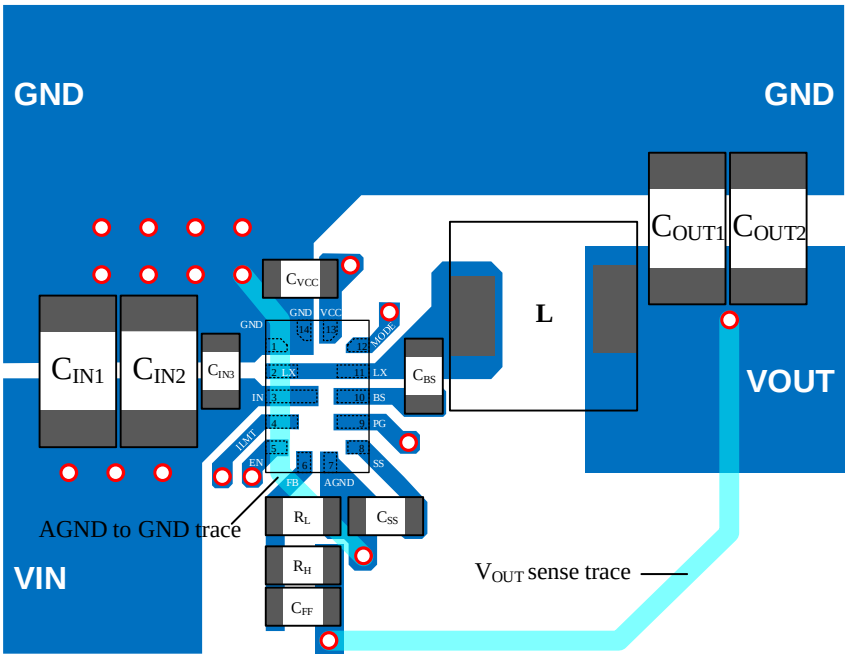
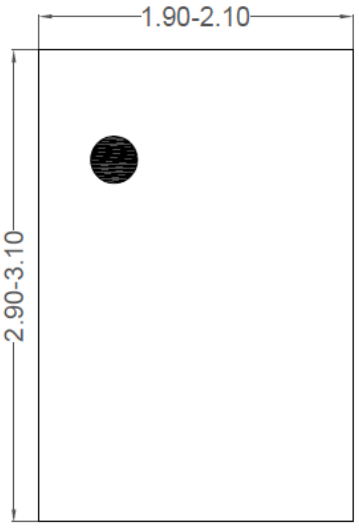
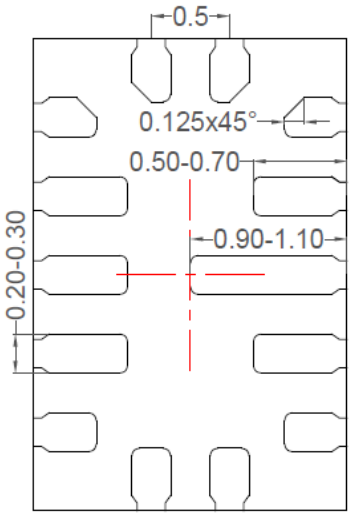


Figure 10. PCB Layout Suggestion

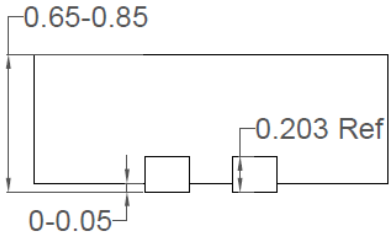
QFN2×3-14 Package Outline Drawing



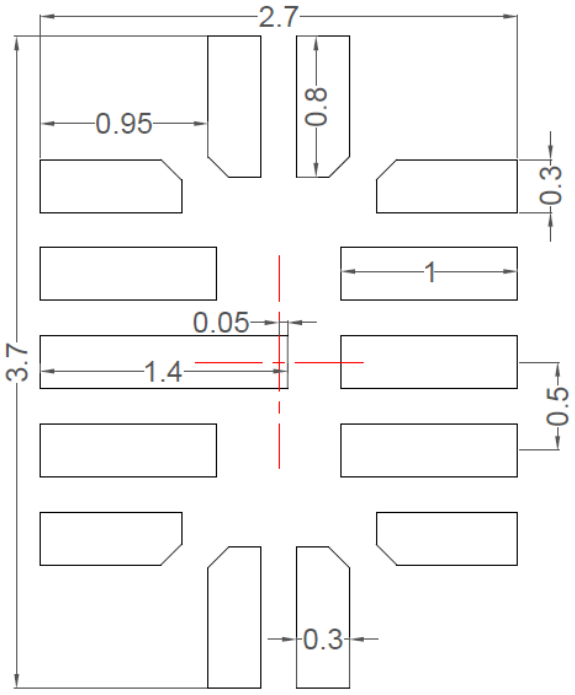
Top View



Bottom view



Front View



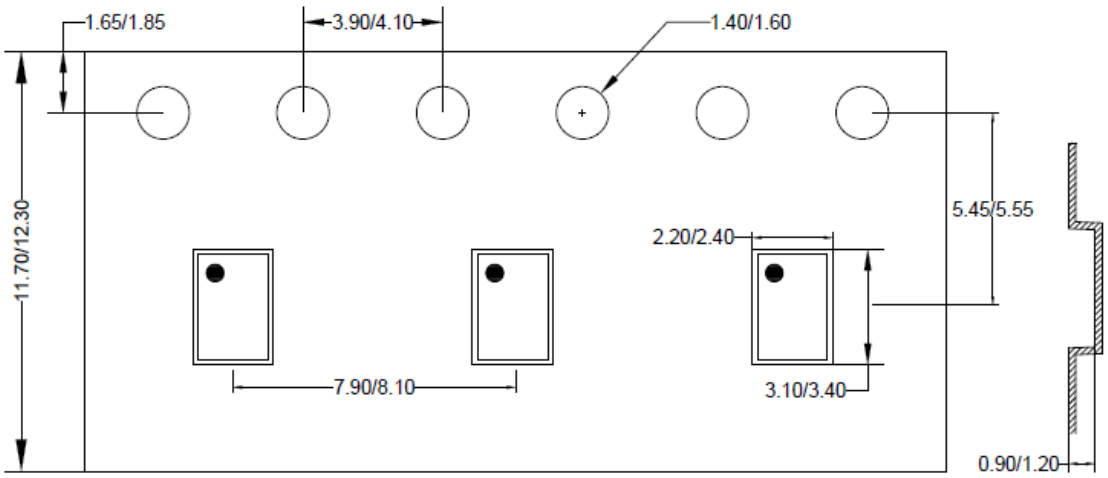
Recommended PCB layout

(Reference only)

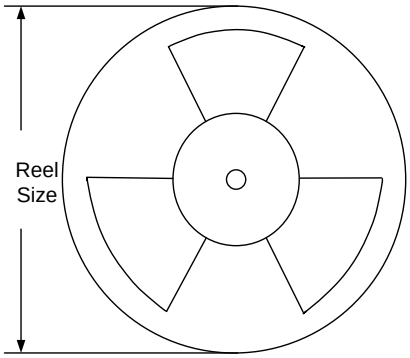
Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Taping and Reel Specification

QFN2×3 taping orientation



Carrier tape and reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel （pcs）
QFN2×3-14	12	8	13"	400	400	5000

Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Nov.6, 2023	Revision 1.0A	On pages 4 and 5, in Electrical Characteristics form, Note 4 is added to the four items: $t_{UVP,DLY}$ $t_{PG,F}$ T_{SD} T_{HYS}
Aug.1, 2023	Revision 1.0	Initial Release

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