9Mb Sync. Flow-Through SRAM Specification

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Document Title

256Kx36 & 512Kx18 Bit Flow-Through SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial Draft	Aug. 2011	Preliminary
1.0	1. Final Spec Release 2. Insert ICC Parameters	Nov. 2011	Final
1.1	Correct Typo	Mar. 2018	Final

256Kx36 & 512Kx18 Bit Flow-Through SRAM

Features

- V_{DD} = 2.5V(2.3V ~ 2.7V) or 3.3V(3.1V ~ 3.5V) Power Supply
- V_{DDQ} = 2.3V~2.7V I/O Power Supply (VDD=2.5V) or 2.3V~3.5V I/O Power Supply (VDD=3.3V)
- Synchronous Operation
- Self-Timed Write Cycle
- On-Chip Address Counter and Control Registers
- Byte Writable Function
- Global Write Enable Controls a full bus-width write
- Power Down State via ZZ Signal
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP
- Asynchronous Output Enable Control
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins
- TTL-Level Three-State Output
- Operating in commeical and industrial temperature range
- 100-TQFP-1420A (Lead free package)

General Description

The S7B803635M and S7B801835M are 9,437,184-bit Synchronous Static Random Access Memory designed for high performance.

It is organized as 256K(512K) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS_1}$ high, $\overline{ADSP}$ is blocked to control signals.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The S7B803635M and S7B801835M are fabricated using high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

Key Parameters

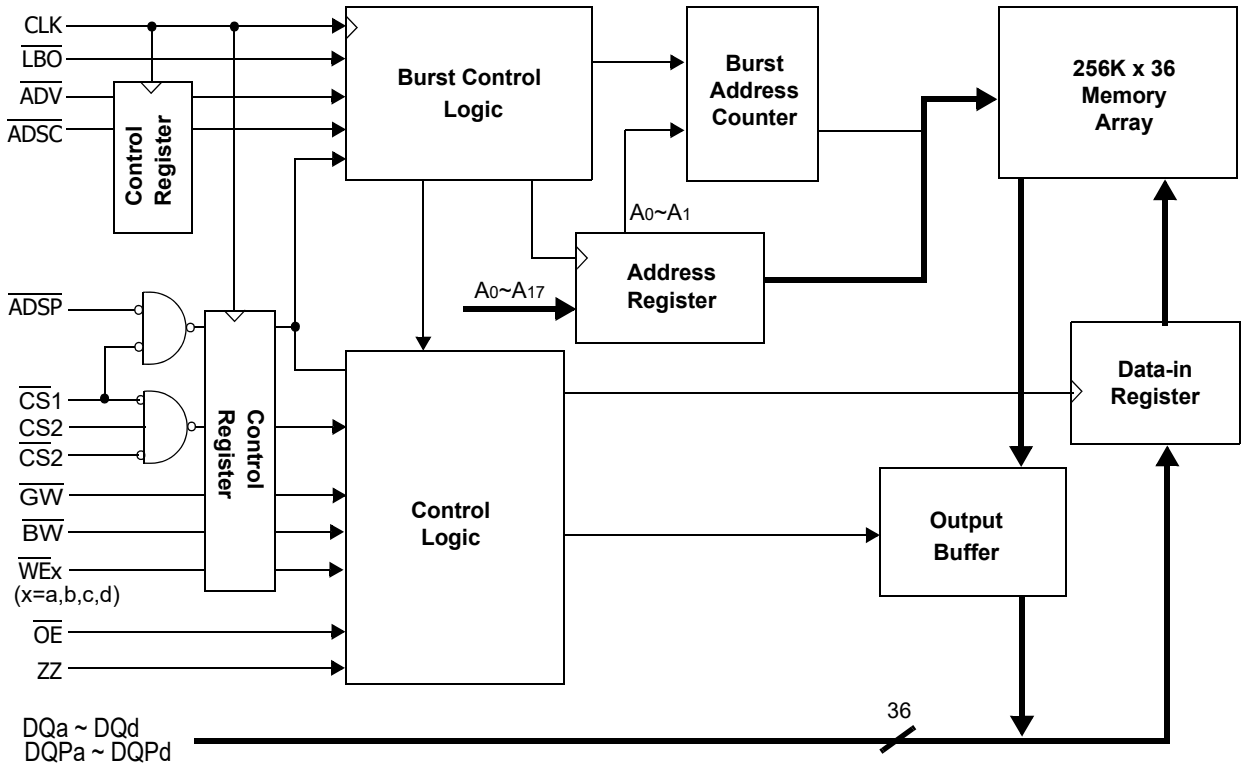
Parameter	Symbol	-65	-75	Unit
Cycle Time	tCYC	7.5	8.5	ns
Clock Access Time	tCD	6.5	7.5	ns
Output Enable Access Time	tOE	3.5	3.5	ns
Operating Current	I_{CC}	110	100	mA
Standby Current	I_{SB2}	30	30	mA

9Mb Synchronous Burst SRAM Ordering Information

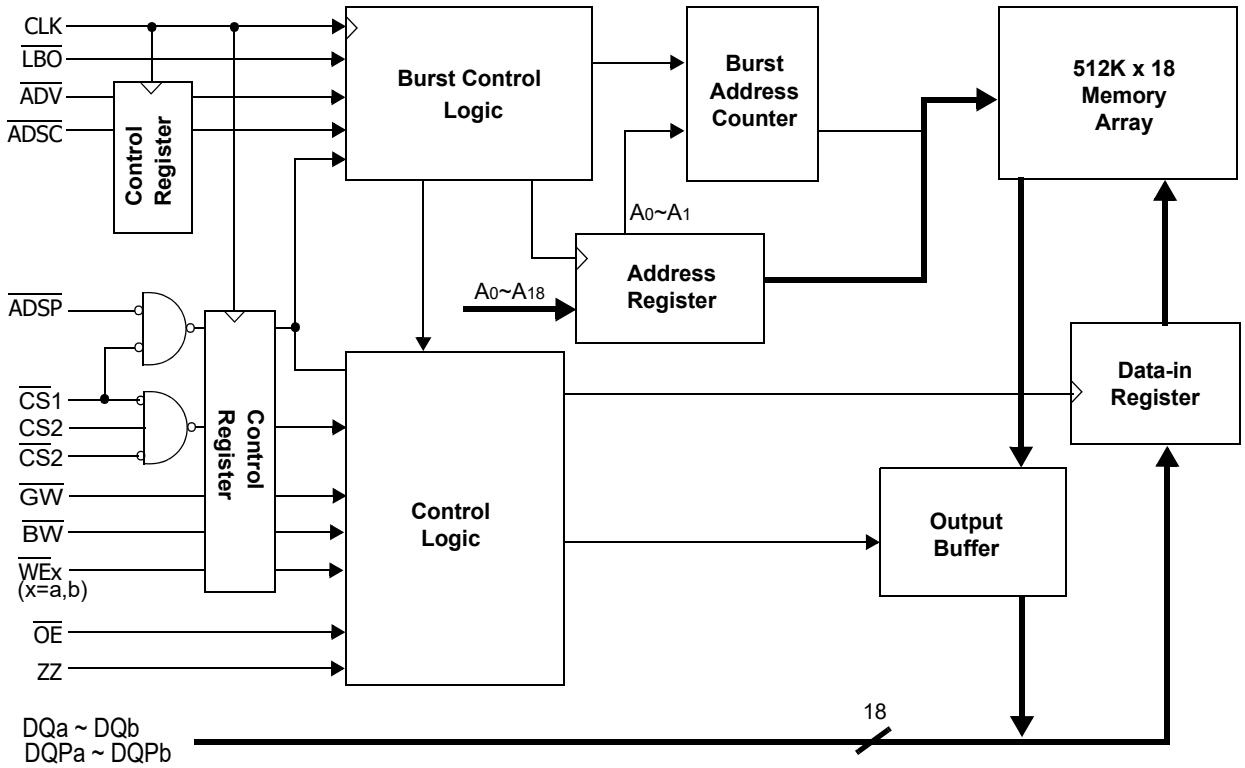
Org.	VDD (V)	Speed (ns)	Access Time (ns)	Part Number	RoHS Avail.
512Kx18	3.3/2.5	7.5	6.5	S7B801835M-PC(I)65	O
	3.3/2.5	8.5	7.5	S7B801835M-PC(I)75	O
256Kx36	3.3/2.5	7.5	6.5	S7B803635M-PC(I)65	O
	3.3/2.5	8.5	7.5	S7B803635M-PC(I)75	O

Note 1. P [Pakage type] : P - Pb Free
2. C(I) [Operating Temperature] : C-Commertial, I-Industrial

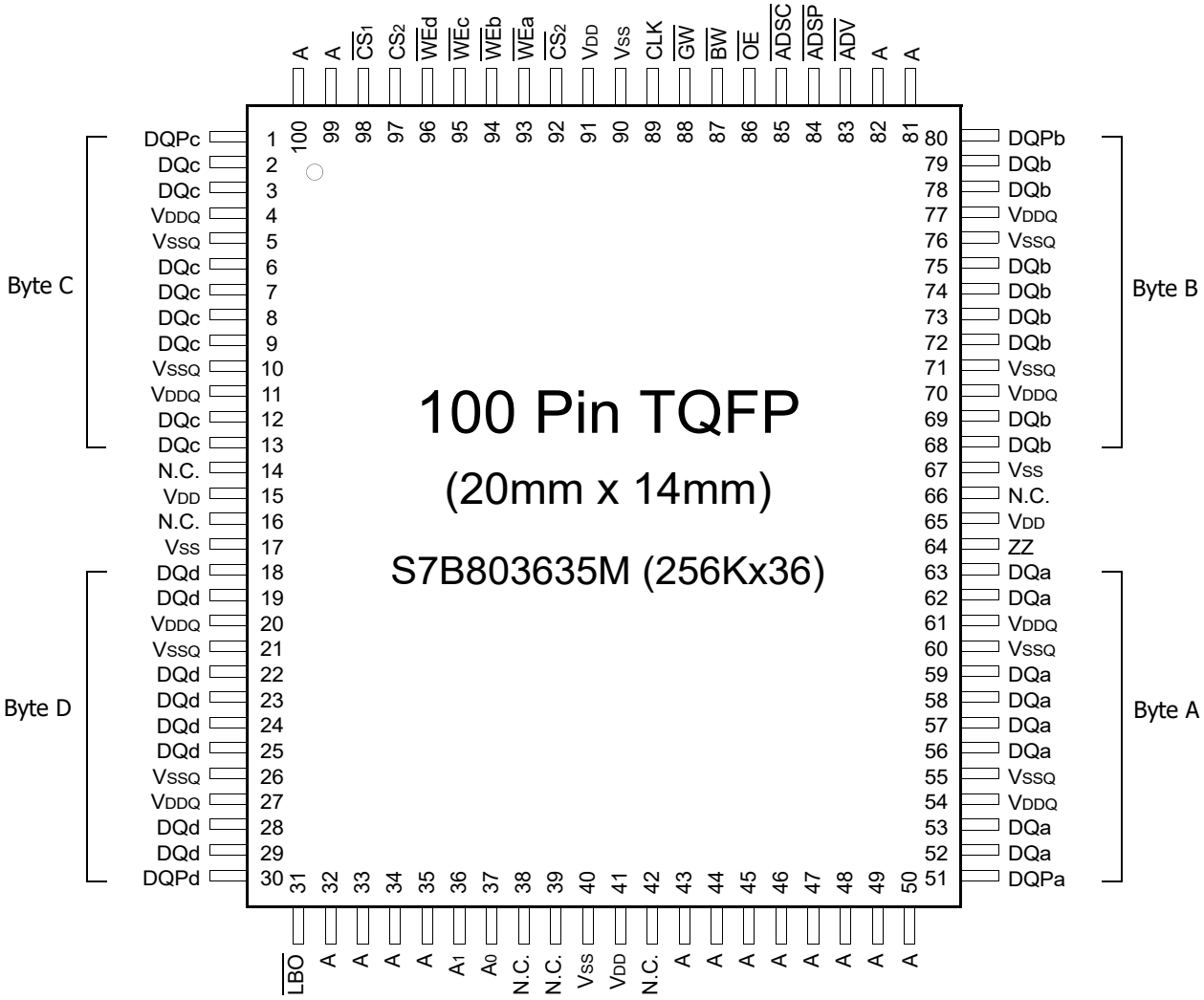
Logic Block Diagram - S7B803635M (256K x 36)



Logic Block Diagram - S7B801835M (512K x 18)



100 TQFP Package Pin Configurations(Top View)

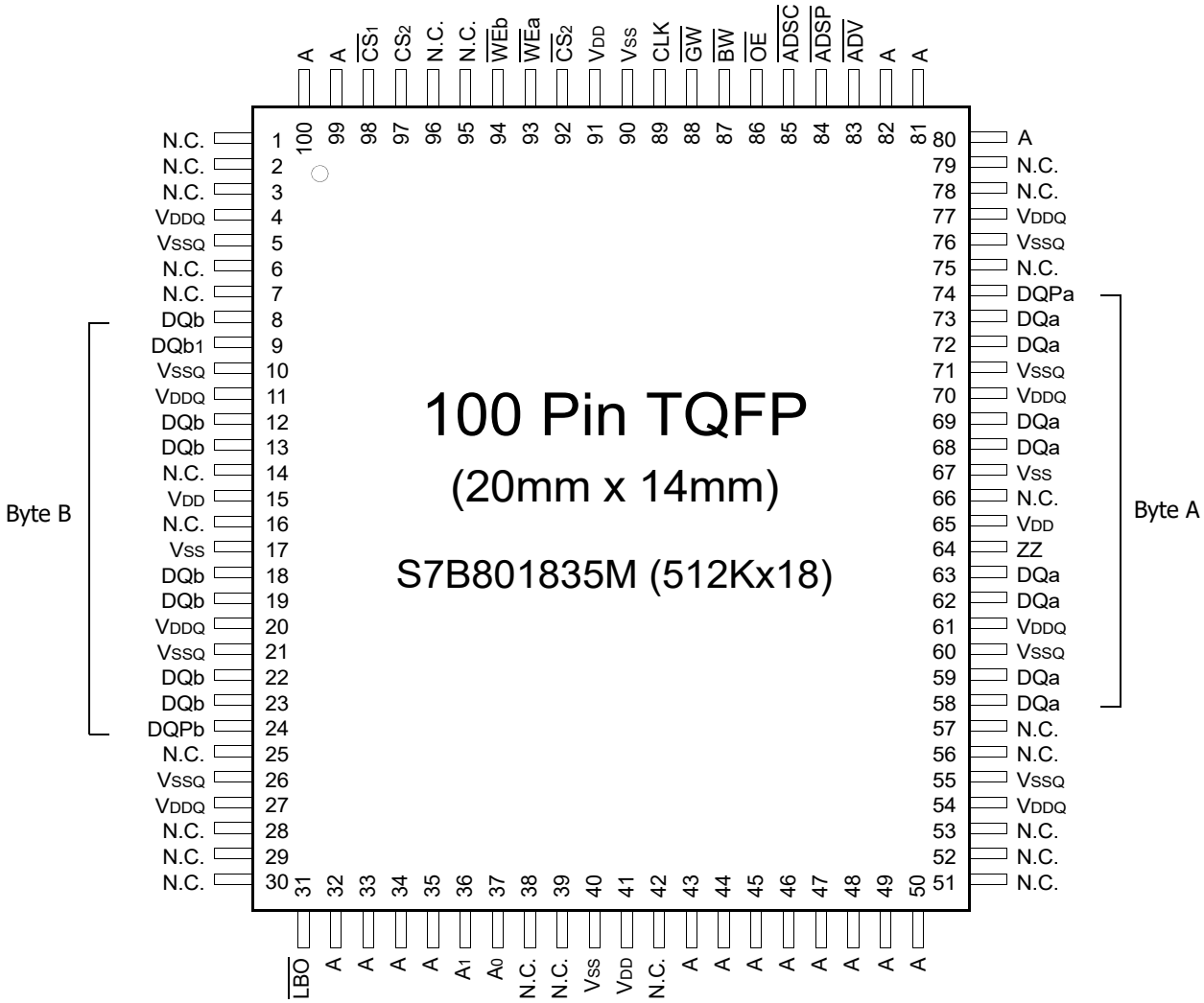


Pin Name

Symbol	Pin Name	TQFP Pin NO.	Symbol	Pin Name	TQFP Pin NO.
A	Address Inputs	32,33,34,35,43,44,45 46,47,48,49,50,81,82, 99,100	VDD	Power Supply (2.5V~3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
A0,A1	Burst Address Inputs	37,36			
$\overline{ADV}$	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,42,66
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85	DQa	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CLK	Clock	89	DQb		68,69,72,73,74,75,78,79
$\overline{CS1}$	Chip Select	98	DQc		2,3,6,7,8,9,12,13
CS2	Chip Select	97	DQd		18,19,22,23,24,25,28,29
$\overline{CS2}$	Chip Select	92	DQPa~Pd		51,80,1,30
$\overline{WE}$x(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
$\overline{OE}$	Output Enable	86	VDDQ	Output Power Supply (2.5V~3.3V)	4,11,20,27,54,61,70,77
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{ZZ}$	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

Note : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

100 TQFP Package Pin Configurations(Top View)



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			VSS	Ground	17,40,67,90
A0,A1	Burst Address Inputs	37,36			
$\overline{ADV}$	Burst Address Advance	83	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29
$\overline{ADSP}$	Address Status Processor	84			30,38,39,42,51,52,53,56
$\overline{ADSC}$	Address Status Controller	85			57,66,75,78,79,95,96
CLK	Clock	89			
$\overline{CS1}$	Chip Select	98	DQa	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CS2	Chip Select	97	DQb		8,9,12,13,18,19,22,23
$\overline{CS2}$	Chip Select	92	DQPa, Pb		74,24
$\overline{WE}$x(x=a,b)	Byte Write Inputs	93,94			
$\overline{OE}$	Output Enable	86	VDDQ	Output Power Supply (2.5V~3.3V)	4,11,20,27,54,61,70,77
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{ZZ}$	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

Function Description

The S7B803635M and S7B801835M are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.
The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and $\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c, and $\overline{WE}$d are high. When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$(or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.
All byte write occurs by enabling $\overline{GW}$(independent of $\overline{BW}$ and $\overline{WE}$x.), and individual byte write is performed only when $\overline{GW}$ is high and $\overline{BW}$ is low. In S7B803635M, a 256Kx36 organization, $\overline{WE}$a controls DQa and DQPa, $\overline{WE}$b controls DQb and DQPb, $\overline{WE}$c controls DQc and DQPc and $\overline{WE}$d controls DQd and DQPd.

$\overline{CS}_1$ is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

Burst Sequence Table

(Interleaved Burst, $\overline{LBO}$=High)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
↓		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst, $\overline{LBO}$=Low)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
↓		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

Asynchronous Truth Table

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

Truth Tables

Synchronous Truth Table

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{Write}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by (↑) .

3. $\overline{Write}$ = L means Write operation in Write Truth Table.
   $\overline{Write}$ = H means Read operation in Write Truth Table.

4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

Write Truth Table(x36)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	Read
H	L	H	H	H	H	Read
H	L	L	H	H	H	Write Byte A
H	L	H	L	H	H	Write Byte B
H	L	H	H	L	L	Write Byte C And D
H	L	L	L	L	L	Write All Bytes
L	X	X	X	X	X	Write All Bytes

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

Write Truth Table(x18)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	Operation
H	H	X	X	Read
H	L	H	H	Read
H	L	L	H	Write Byte A
H	L	H	L	Write Byte B
H	L	L	L	Write All Bytes
L	X	X	X	Write All Bytes

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to V_{SS}		V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to V_{SS}		V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to V_{SS}		V_{IN}	-0.3 to V_{DD}+0.3	V
Voltage on I/O Pin Relative to V_{SS}		V_{IO}	-0.3 to V_{DDQ}+0.3	V
Power Dissipation		P_D	1.6	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial	T_{OPR}	0 to 70	°C
	Industrial	T_{OPR}	-40 to 85	°C
Storage Temperature Range Under Bias		T_{BIAS}	-10 to 85	°C

Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD1}	2.3	2.5	2.7	V
	V_{DDQ1}	2.3	2.5	2.7	V
	V_{DD2}	3.1	3.3	3.5	V
	V_{DDQ2}	2.3	3.3	3.5	V
Ground	V_{SS}	0	0	0	V

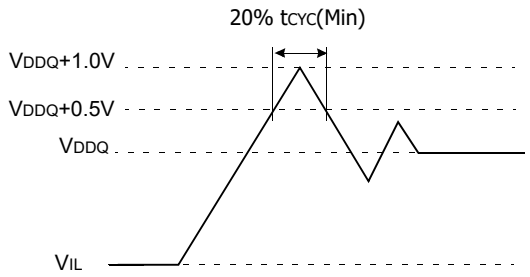
Notes: 1. The above parameters are also guaranteed at industrial temperature range.
2. It should be $V_{DDQ} \leq V_{DD}$

Capacitence(T_A=25°C, f=1MHz)

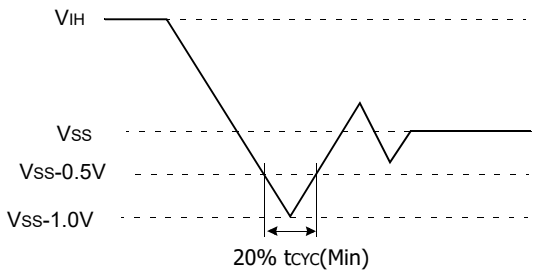
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

Note : Sampled not 100% tested.

Overshoot Timing



Undershoot Timing



DC Electrical Caracteristics

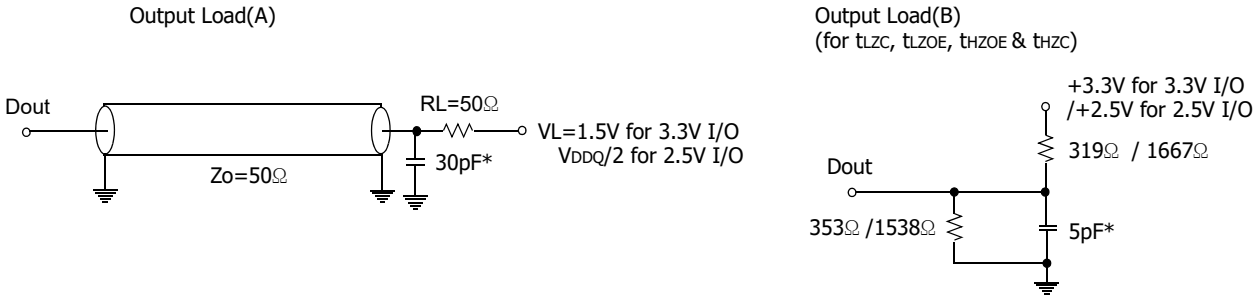
Parameter	Symbol	Test Conditions		Min	Max	Unit	Notes
Input Leakage Current(except ZZ)	I_{IL}	V_{DD}=Max ; V_{IN}=V_{SS} to V_{DD}		-2	+2	uA	
Output Leakage Current	I_{OL}	Output Disabled, V_{out}=V_{SS} to V_{DDQ}		-2	+2	uA	
Operating Current	I_{CC}	Device Selected, I_{OUT}=0mA,	-65	-	110	mA	1,2
		ZZ ≤ V_{IL}, Cycle Time ≥ t_{CYC} Min	-75	-	100		
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA, ZZ ≤ V_{IL}, f=Max, All Inputs ≤ VIL or ≥ VIH		-	50	mA	
	I_{SB1}	Device deselected, I_{OUT}=0mA, ZZ ≤ 0.2V, f=0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	30	mA	
	I_{SB2}	Device deselected, I_{OUT}=0mA, ZZ ≥ V_{DD}-0.2V, f=Max, All Inputs ≤ V_{IL} or ≥ V_{IH}		-	30	mA	
Output Low Voltage(3.3V I/O)	V_{OL}	I_{OL}=8.0mA		-	0.4	V	
Output High Voltage(3.3V I/O)	V_{OH}	I_{OH}=-4.0mA		2.4	-	V	
Output Low Voltage(2.5V I/O)	V_{OL}	I_{OL}=1.0mA		-	0.4	V	
Output High Voltage(2.5V I/O)	V_{OH}	I_{OH}=-1.0mA		2.0	-	V	
Input Low Voltage(3.3V I/O)	V_{IL}			-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V_{IH}			2.0	V_{DD}+0.3**	V	3
Input Low Voltage(2.5V I/O)	V_{IL}			-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V_{IH}			1.7	V_{DD}+0.3**	V	3

Notes : The above parameters are also guaranteed at industrial temperature range.
1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V

Test Conditions

Parameter	Value
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3/2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V_{DDQ}/2
Output Load	See Fig. 1

The above parameters are also guaranteed at industrial temperature range.



* Including Scope and Jig Capacitance

Fig. 1

AC Timing Characteristics

Parameter	Symbol	-65		-75		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	7.5	-	8.5	-	ns
Clock Access Time	t_{CD}	-	6.5	-	7.5	ns
Output Enable to Data Valid	t_{OE}	-	3.5	-	3.5	ns
Clock High to Output Low-Z	t_{LZC}	2.5	-	2.5	-	ns
Output Hold from Clock High	t_{OH}	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	t_{LZOE}	0	-	0	-	ns
Output Enable High to Output High-Z	t_{HZOE}	-	3.5	-	3.5	ns
Clock High to Output High-Z	t_{HZC}	-	3.8	-	4.0	ns
Clock High Pulse Width	t_{CH}	2.5	-	2.5	-	ns
Clock Low Pulse Width	t_{CL}	2.5	-	2.5	-	ns
Address Setup to Clock High	t_{AS}	1.5	-	1.5	-	ns
Address Status Setup to Clock High	t_{SS}	1.5	-	1.5	-	ns
Data Setup to Clock High	t_{DS}	1.5	-	1.5	-	ns
Write Setup to Clock High ($\overline{WE}$, $\overline{BW}$x)	t_{WS}	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	t_{ADVS}	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	t_{CSS}	1.5	-	1.5	-	ns
Address Hold from Clock High	t_{AH}	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t_{SH}	0.5	-	0.5	-	ns
Data Hold from Clock High	t_{DH}	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{WE}$, $\overline{BW}$x)	t_{WH}	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t_{ADVH}	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t_{CSH}	0.5	-	0.5	-	ns
ZZ High to Power Down	t_{PDS}	2	-	2	-	cycle
ZZ Low to Power Up	t_{PUS}	2	-	2	-	cycle

Notes : 1. The above parameters are also guaranteed at industrial temperature range.
2. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
3. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.
4. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

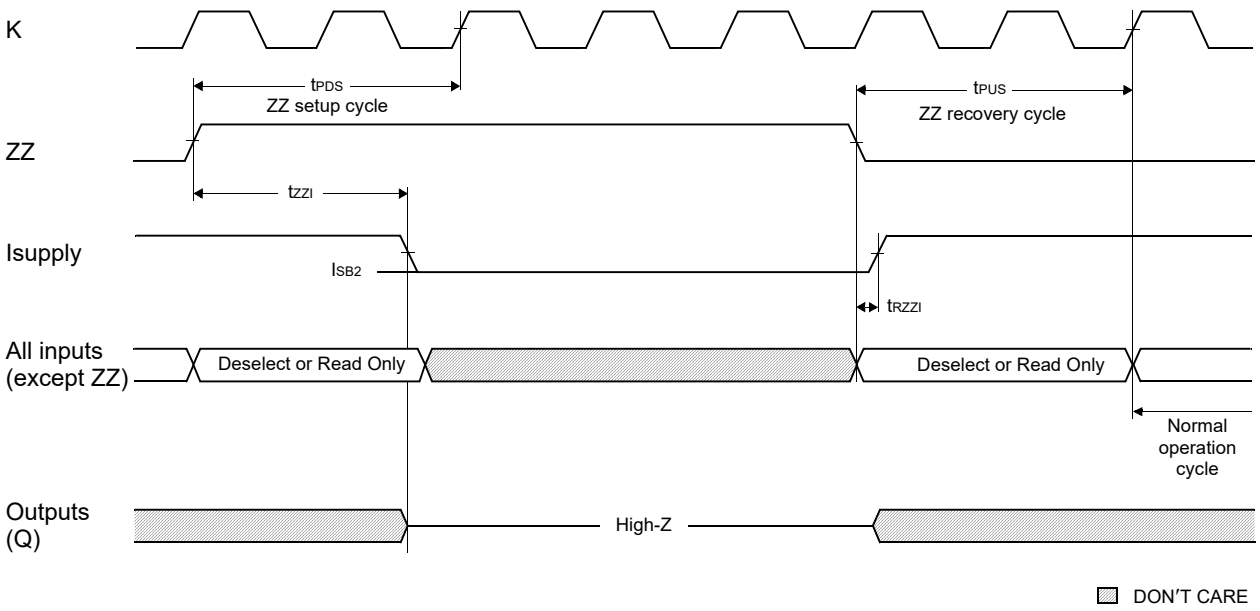
Sleep Mode

Sleep Mode is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2}. The duration of Sleep Mode is dictated by the length of time the ZZ is in a High state.
After entering Sleep Mode, all inputs except ZZ become disabled and all outputs go to High-Z.
The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep Mode.
When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. Any operation pending when entering Sleep Mode is not guaranteed to successful complete. Therefore, Sleep Mode (Read or Write) must not be initiated until valid pending operations are completed. similarly, when exiting Sleep Mode during t_{PUS}, only a Deselect or Read cycle should be given while the SRAM is transitioning out of Sleep Mode.

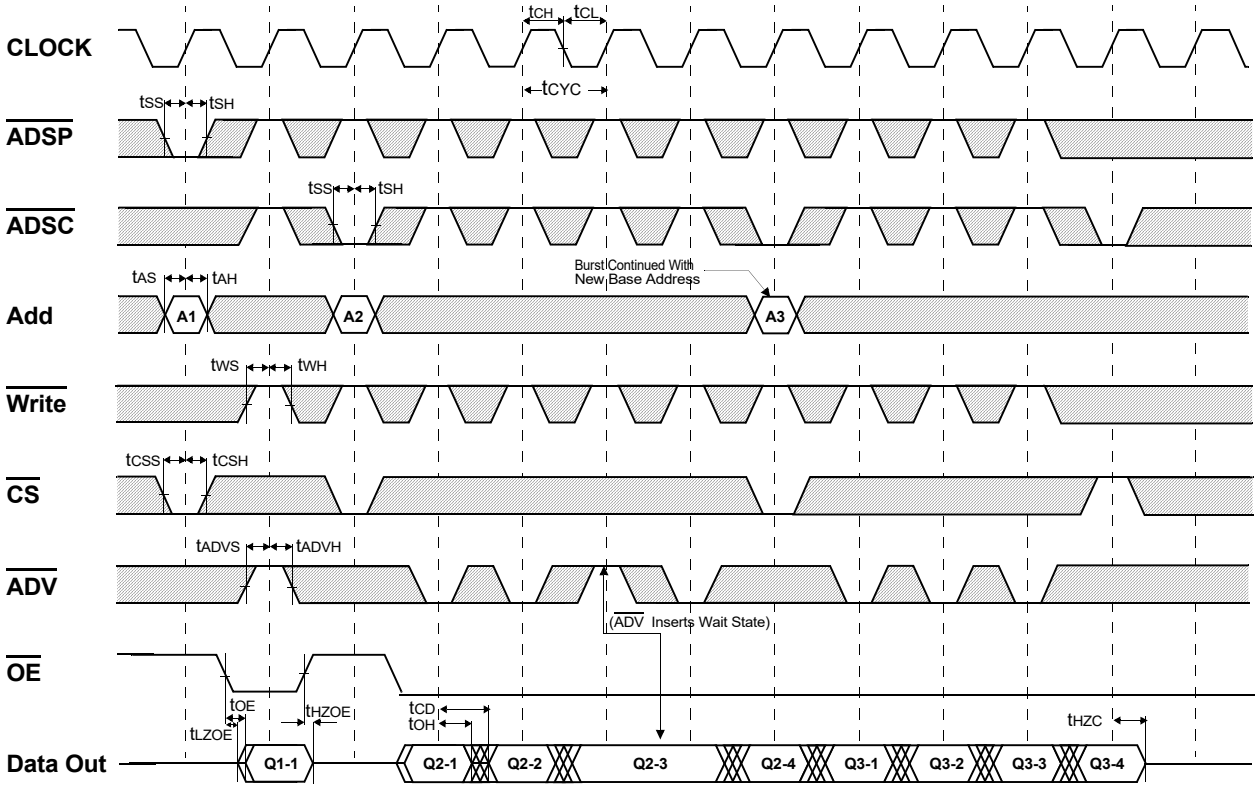
Sleep Mode Electrical Characteristics

Description	Condition	Symbol	Min	Max	Unit
Current during SLEEP MODE	ZZ ≥ V_{IH}	I_{SB2}		30	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SLEEP current		t_{ZZI}		2	cycle
ZZ inactive to exit SLEEP current		t_{RZZI}	0		

Sleep Mode Waveform



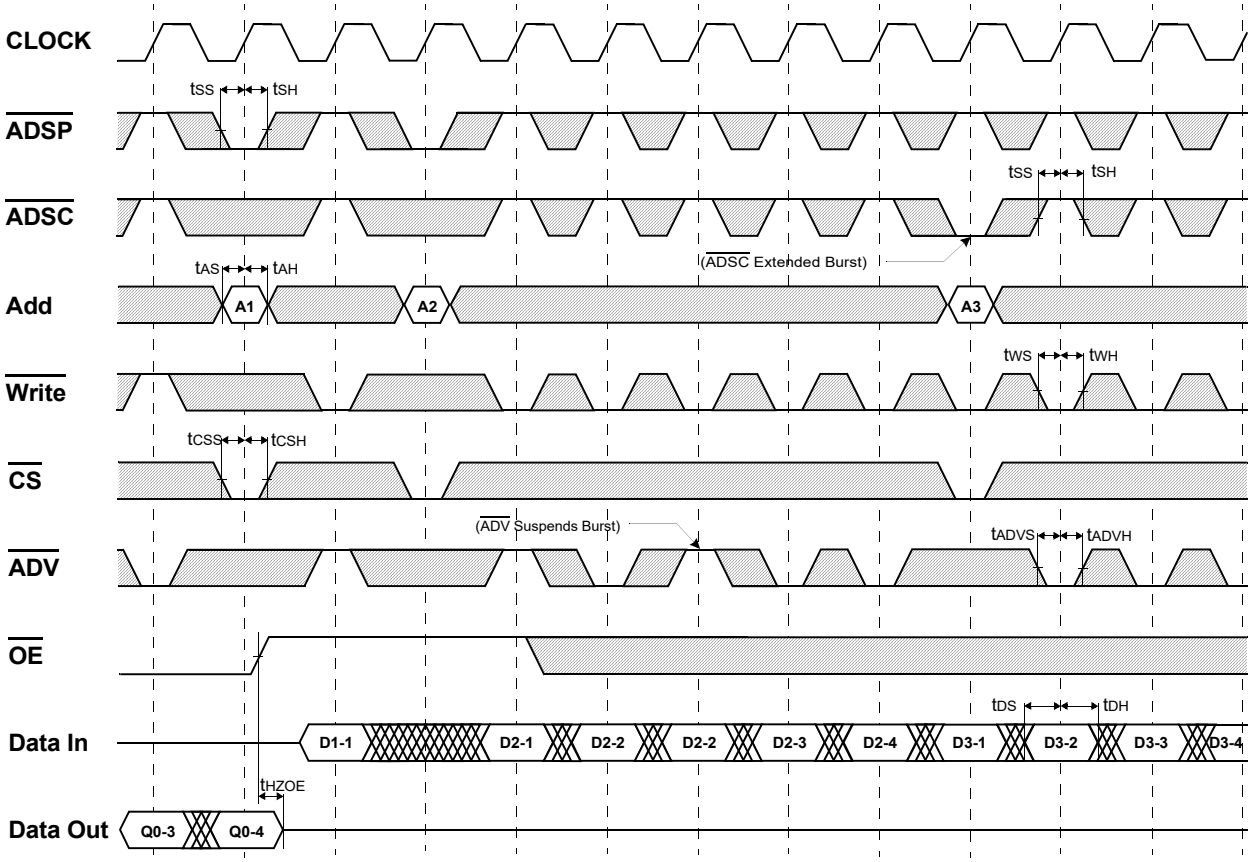
Timing Waveform of Read Cycle



NOTES : $\overline{Write}$ = L means GW = L, or GW = H, BW = L, WEx = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

Don't Care
Undefined

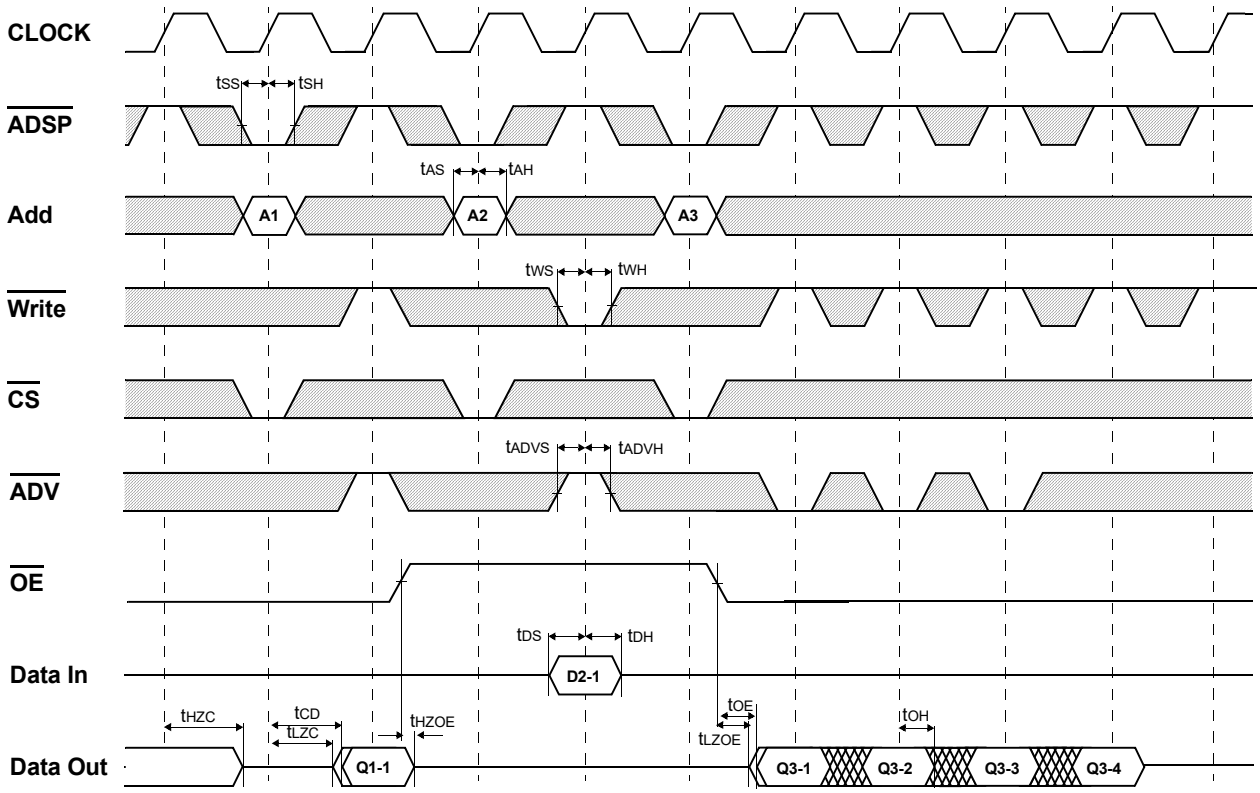
Timing Waveform of Write Cycle



NOTES : $\overline{Write}$ = L means GW = L, or GW = H, BW = L, WEx = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

Don't Care
Undefined

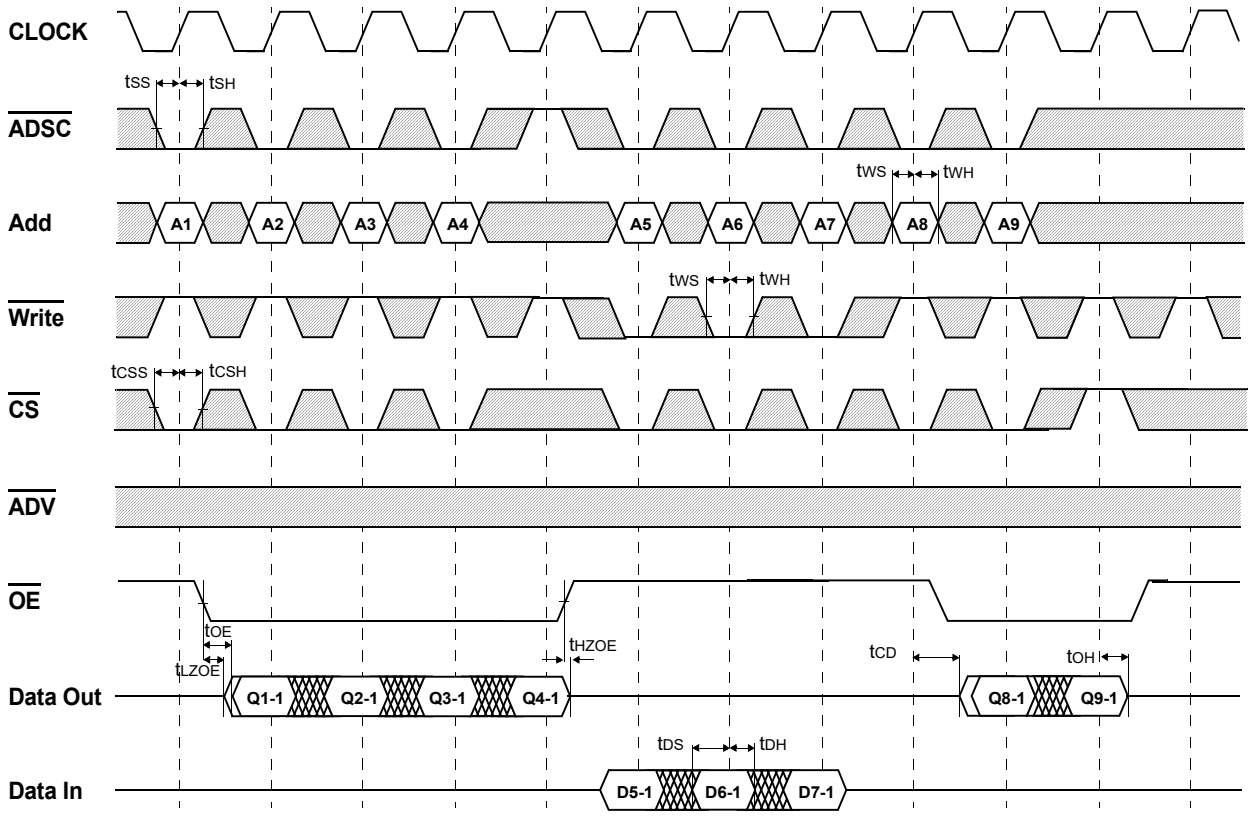
Timing Waveform of Combination Read/Write Cycle($\overline{ADSP}$ Controlled , $\overline{ADSC}$=High)



NOTES : $\overline{Write}$ = L means GW = L, or GW = H, BW = L, WEx = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

Don't Care
Undefined

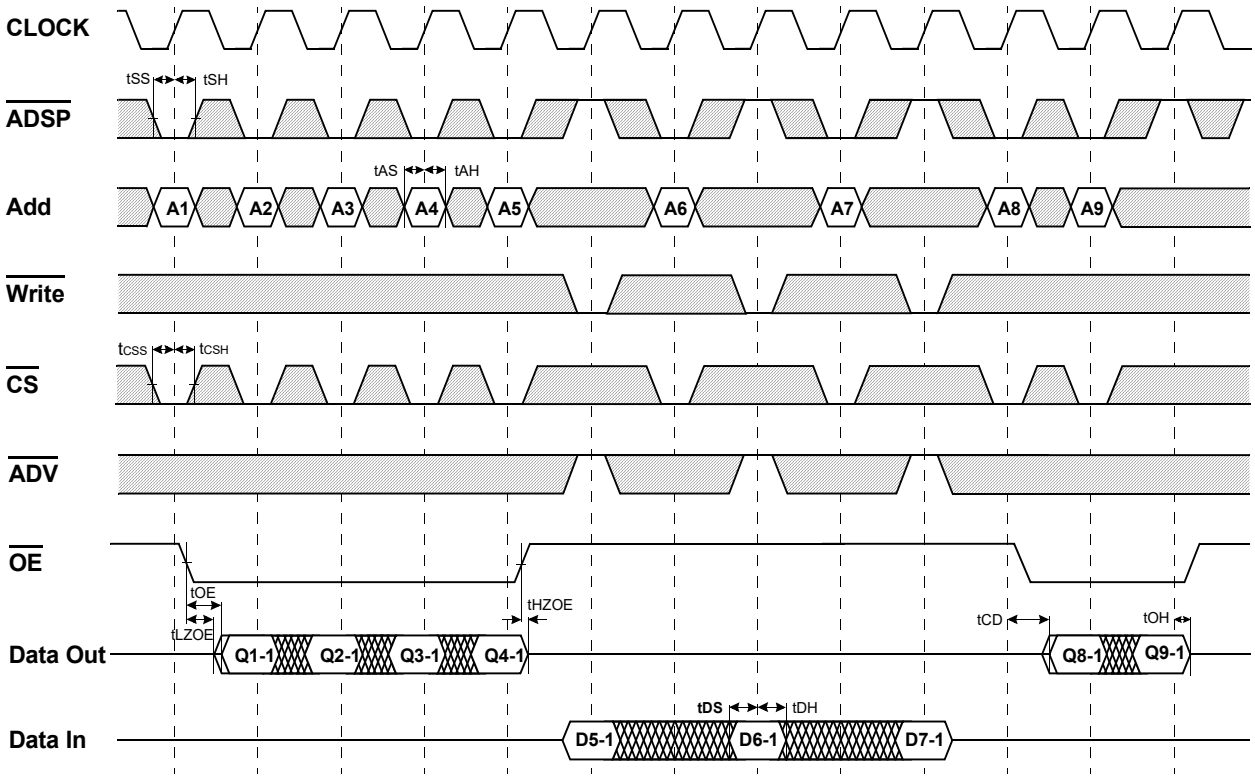
Timing Waveform of Single Read/Write Cycle ($\overline{ADSC}$ Controlled , $\overline{ADSP}$=High)



NOTES : $\overline{Write}$ = L means GW = L, or GW = H, BW = L, WEx = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

Don't Care
Undefined

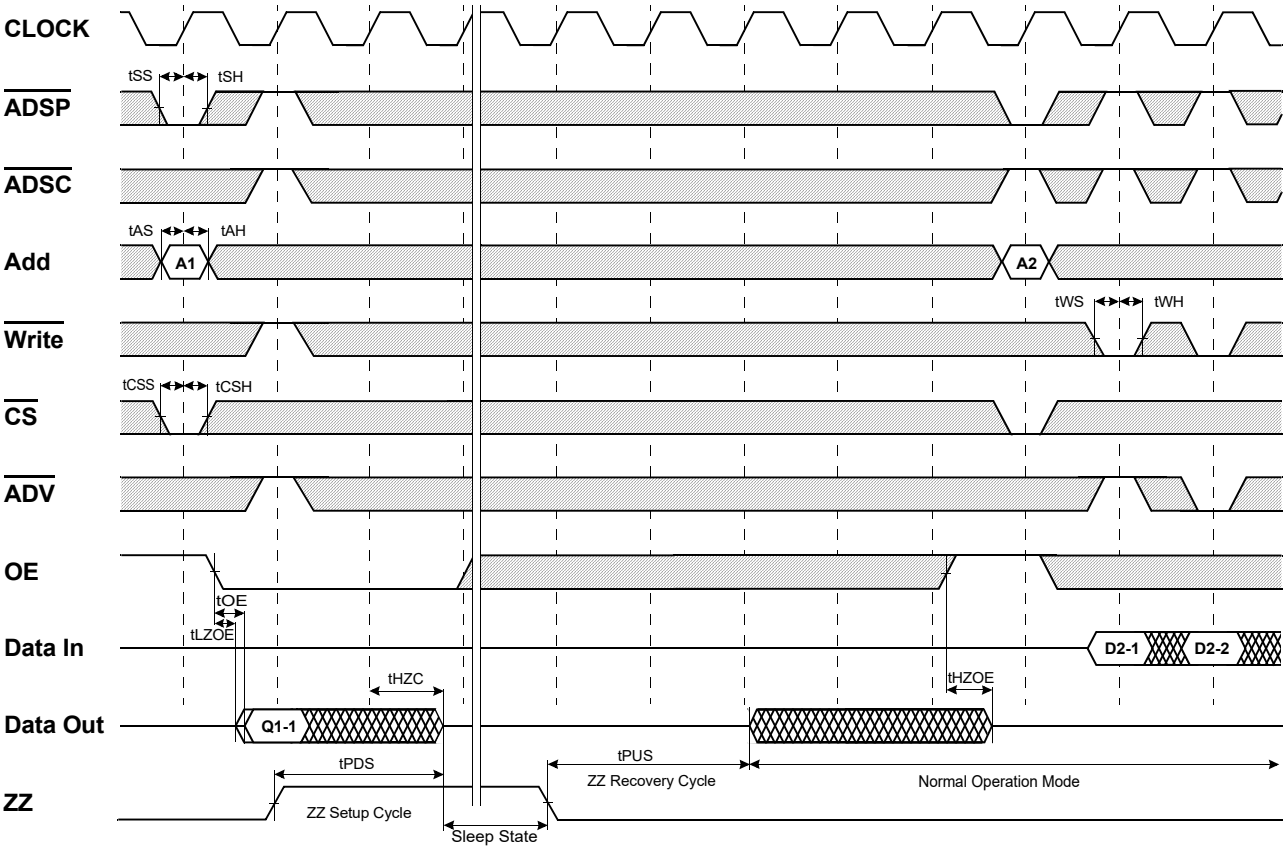
Timing Waveform of Single Read/Write Cycle ($\overline{ADSP}$ Controlled , $\overline{ADSC}$=High)



NOTES : $\overline{Write}$ = L means GW = L, or GW = H, BW = L, WEx = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

Don't Care
Undefined

Timing Waveform of Power Down Cycle



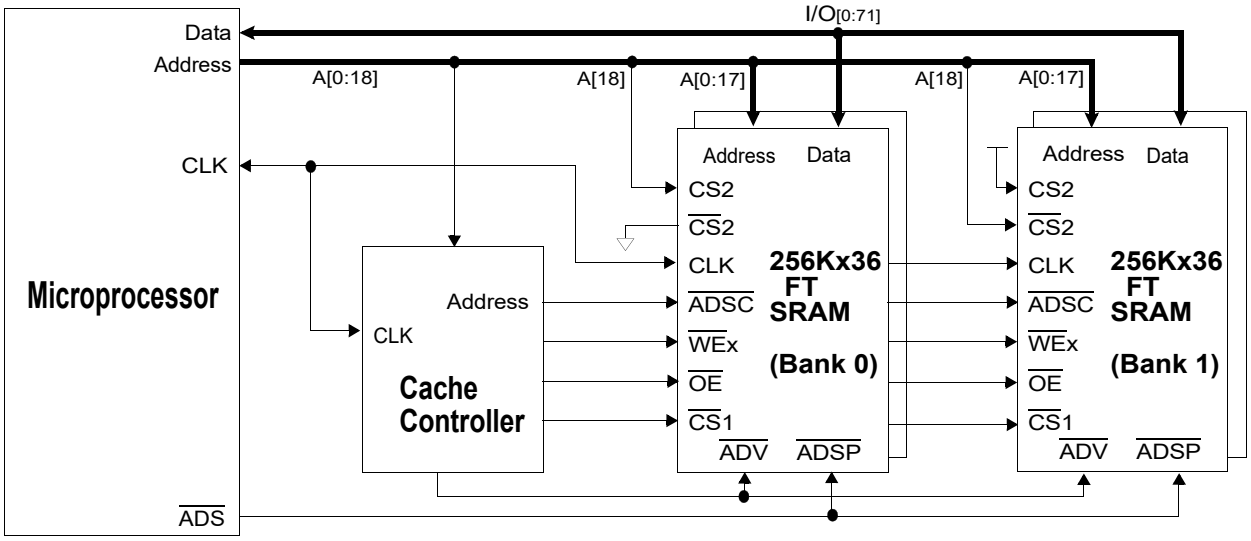
NOTES : $\overline{Write}$ = L means GW = L, or GW = H, BW = L, WEx = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

Don't Care
Undefined

Application Information

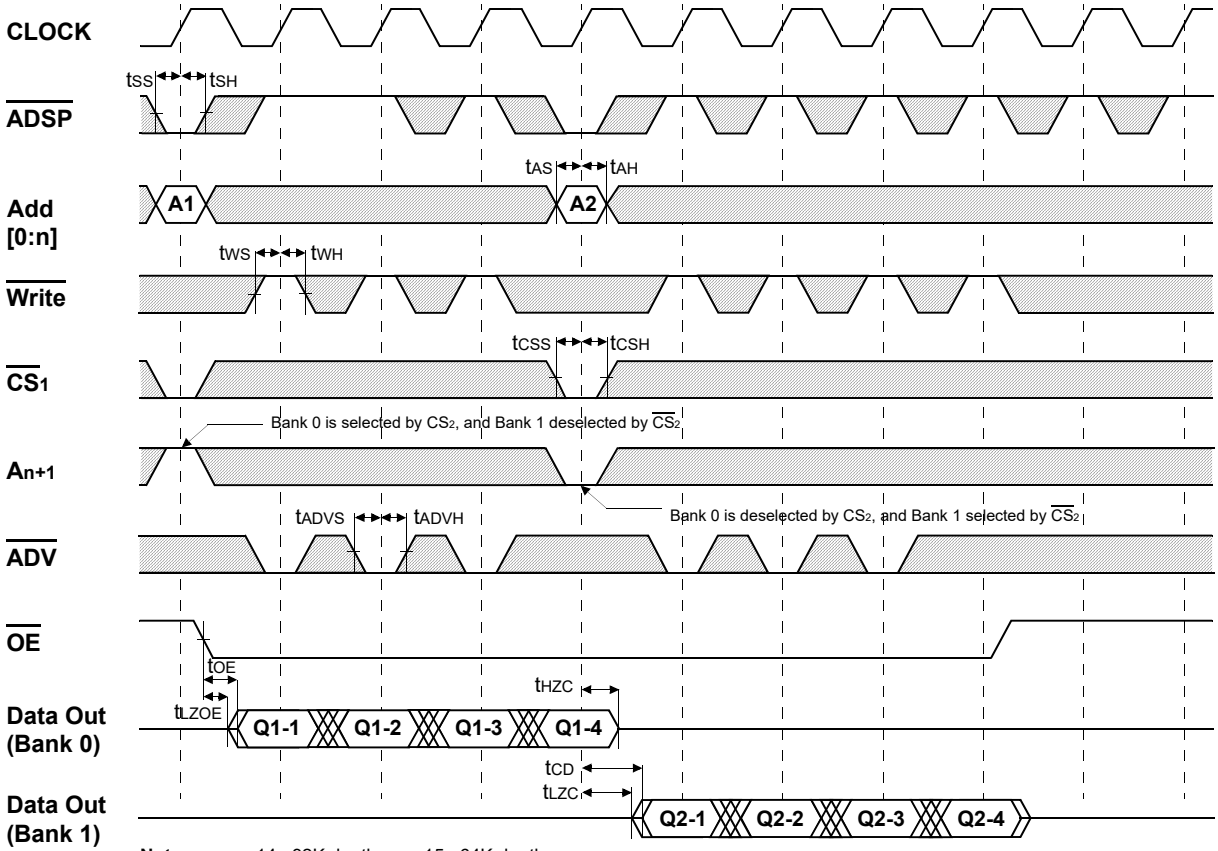
Depth Expansion

The Netsol 256Kx36 Flow-Through SRAM has two additional chip selects for simple depth expansion.
This permits easy secondary cache upgrades from 256K depth to 512K depth without extra logic.



Interleave Read Timing (Refer to non-interleave write timing for interleave write timing)

($\overline{ADSP}$ Controlled , $\overline{ADSC}$=HIGH)



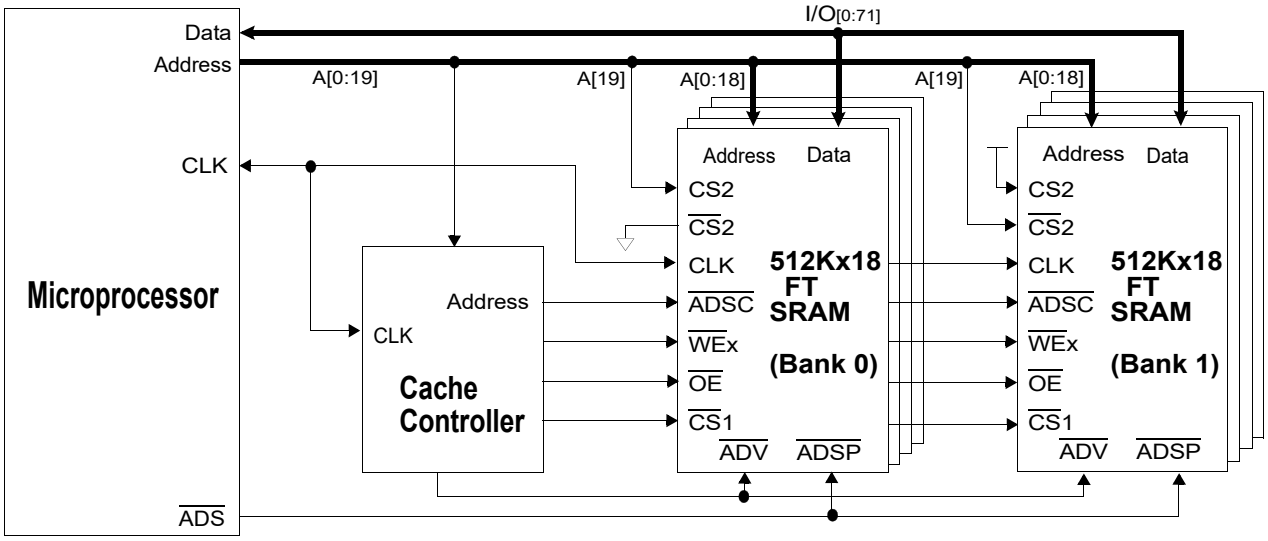
Notes : n = 14 32K depth , 15 64K depth
16 128K depth , 17 256K depth
18 512K depth , 19 1M depth

Don't Care Undefined

Application Information

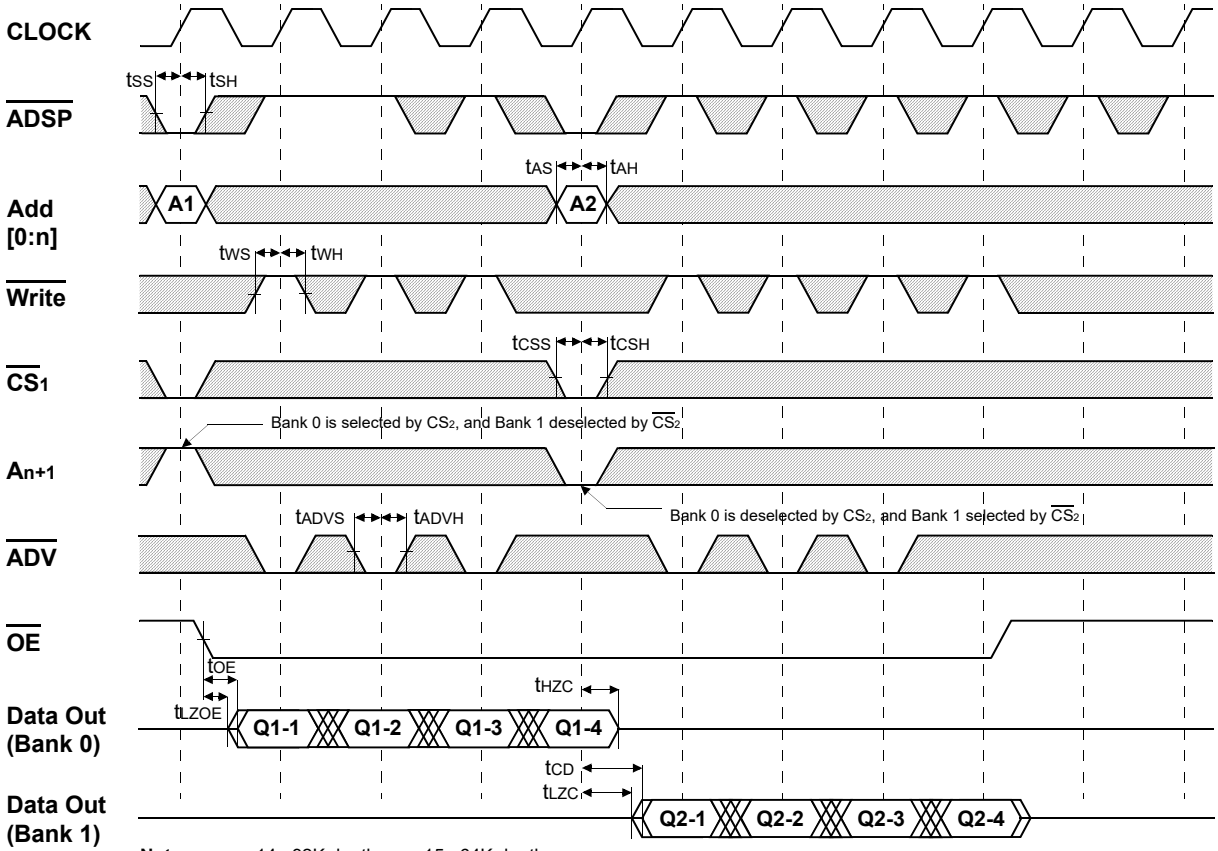
Depth Expansion

The Netsol 512Kx18 Flow-Through SRAM has two additional chip selects for simple depth expansion.
This permits easy secondary cache upgrades from 512K depth to 1M depth without extra logic.



Interleave Read Timing (Refer to non-interleave write timing for interleave write timing)

($\overline{ADSP}$ Controlled , $\overline{ADSC}$=HIGH)



Notes : n = 14 32K depth , 15 64K depth
16 128K depth , 17 256K depth
18 512K depth , 19 1M depth

Don't Care Undefined

Package Dimensions

100-TQFP-1420A (Lead Free)