18Mb Sync. Flow-Through SRAM Specification

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Document Title

512Kx36 & 1Mx18 Bit Flow-Through SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial Draft	Feb. 2012	Advanced
1.0	Final spec release Insert Icc spec parameters	Jul. 2012	Final
1.1	Correct Typo	Sep. 2012	Final
1.2	Correct Typo	Mar. 2018	Final



Features

- VDD = 2.5V(2.3V ~ 2.7V) or 3.3V(3.1V ~ 3.5V) Power Supply
- VDDQ = 2.3V~2.7V I/O Power Supply (VDD=2.5V) or 2.3V~3.5V I/O Power Supply (VDD=3.3V)
- Synchronous Operation
- Self-Timed Write Cycle
- On-Chip Address Counter and Control Registers
- Byte Writable Function
- Global Write Enable Controls a full bus-width write
- Power Down State via ZZ Signal
- LBO Pin allows a choice of either a interleaved burst or a linear burst
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP
- Asynchronous Output Enable Control
- ADSP, ADSC, ADV Burst Control Pins
- TTL-Level Three-State Output
- Operating in commeical and industrial temperature range
- 100-TQFP-1420A (Lead free package)

General Description

The S7B163635M and S7B161835M are 18,874,368-bit Synchronous Static Random Access Memory designed for high performance.

It is organized as 512K(1M) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance applications; $\overline{\text{GW}}$, $\overline{\text{BW}}$, $\overline{\text{LBO}}$, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{\text{GW}}$, and each byte write is performed by the combination of $\overline{\text{WEx}}$ and $\overline{\text{BW}}$ when $\overline{\text{GW}}$ is high. And with $\overline{\text{CS}}_1$ high, $\overline{\text{ADSP}}$ is blocked to control signals.

Burst cycle can be initiated with either the address status processor($\overline{\text{ADSP}}$) or address status cache controller($\overline{\text{ADSC}}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{\text{ADV}}$) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The S7B163635M and S7B161835M are fabricated using high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

Key Parameters

Parameter	Symbol	-65	-75	Unit
Cycle Time	tCYC	7.5	8.5	ns
Clock Access Time	tCD	6.5	7.5	ns
Output Enable Access Time	tOE	3.5	3.5	ns
Operating Current	Icc	100	90	mA
Standby Current	ISB2	35	35	mA

18Mb Flow-Through SRAM Ordering Information

Org.	VDD (V)	Speed (ns)	Access Time (ns)	Part Number	RoHS Avail.
1Mv19	3.3/2.5	7.5	6.5	S7B161835M-PC(I)65	0
10010	3.3/2.5	8.5	7.5	S7B161835M-PC(I)75	0
512Ky26	3.3/2.5	7.5	6.5	S7B163635M-PC(I)65	0
512KX30	3.3/2.5	8.5	7.5	S7B163635M-PC(I)75	0

Note 1. P [Pakage type] : P - Pb Free

2. C(I) [Operating Temperature] : C-Commertial, I-Industrial





Logic Block Diagram - S7B163635M (512K x 36)

Logic Block Diagram - S7B161835M (1M x 18)







100 TQFP Package Pin Configurations(Top View)

Pin Name

Symbol	Pin Name	TQFP Pin NO.	Symbol	Pin Name	TQFP Pin NO.
A	Address Inputs	32,33,34,35,42,43,44	VDD	Power Supply	15,41,65,91
		45,46,47,48,49,50,81		(2.5V~3.3V)	
		82,99,100	VSS	Ground	17,40,67,90
A0,A1	Burst Address Inputs	37,36			
ADV	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,42,66
ADSP	Address Status Processor	84			
ADSC	Address Status Controller	85	DQa	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CLK	Clock	89	DQb		68,69,72,73,74,75,78,79
CS1	Chip Select	98	DQc		2,3,6,7,8,9,12,13
CS2	Chip Select	97	DQd		18,19,22,23,24,25,28,29
CS2	Chip Select	92	DQPa~Pd		51,80,1,30
$\overline{WE}x(x=a,b,c,d)$	Byte Write Inputs	93,94,95,96			
OE	Output Enable	86	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
GW	Global Write Enable	88		(2.5V~3.3V)	
BW	Byte Write Enable	87	VSSQ	Output Ground	5,10,21,26,55,60,71,76
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

Note: 1. Ao and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.





Pin Name

Symbol	Pin Name	TQFP Pin NO.	Symbol	Pin Name	TQFP Pin NO.
A	Address Inputs	32,33,34,35,42,43,44,	VDD	Power Supply	15,41,65,91
		45,46,47,48,49,50,80,		(2.5V~3.3V)	
		81,82,99,100	VSS	Ground	17,40,67,90
A0,A1	Burst Address Inputs	37,36			
ADV	Burst Address Advance	83	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29
ADSP	Address Status Processor	84			30,38,39,42,51,52,53,56
ADSC	Address Status Controller	85			57,66,75,78,79,95,96
CLK	Clock	89			
CS1	Chip Select	98	DQa	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CS2	Chip Select	97	DQb		8,9,12,13,18,19,22,23
CS2	Chip Select	92	DQPa, Pb		74,24
$\overline{WE}x(x=a,b)$	Byte Write Inputs	93,94			
OE	Output Enable	86	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
GW	Global Write Enable	88		(2.5V~3.3V)	
BW	Byte Write Enable	87	VSSQ	Output Ground	5,10,21,26,55,60,71,76
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			



Function Description

The S7B163635M and S7B161835M are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of \overline{OE} , LBO and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by \overline{ADSC} , \overline{ADSP} and \overline{ADV} and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with ADV.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{\text{ADSP}}$ (or $\overline{\text{ADSC}}$) using the new external address clocked into the on-chip address register when both $\overline{\text{GW}}$ and $\overline{\text{BW}}$ are high or when $\overline{\text{BW}}$ is low and $\overline{\text{WEa}}$, $\overline{\text{WEb}}$, $\overline{\text{WEc}}$, and $\overline{\text{Wed}}$ are high. When $\overline{\text{ADSP}}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{\text{OE}}$. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with ADSP(or ADSC) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.

All byte write occurs by enabling \overline{GW} (independent of \overline{BW} and \overline{WEx} .), and individual byte write is performed only when \overline{GW} is high and \overline{BW} is low. In S7B163635M, a 512Kx36 organization, \overline{WEa} controls DQa and DQPa, \overline{WEb} controls DQb and DQPb, \overline{WEc} controls DQc and DQPc and \overline{WEd} controls DQd and DQPd.

 $\overline{\text{CS}}_1$ is used to enable the device and conditions internal use of $\overline{\text{ADSP}}$ and is sampled only when a new external address is loaded.

ADV is ignored at the clock edge when ADSP is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when ADV is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

Burst Sequence Table

	нісн	Cas	se 1	Ca	se 2	Cas	se 3	Cas	se 4
LBOFIN		A 1	A0						
First Address		0	0	0	1	1	0	1	1
	Í		1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fou	urth Address	1	1	1	0	0	1	0	0

(Linear Burst, LBO=Low)

(Interleaved Burst, LBO=High)

LBO PIN	LOW	Cas	se 1	Cas	se 2	Cas	se 3	Case 4	
	LOW	A 1	A0	A 1	A0	A 1	A0	A 1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
	\checkmark	1	0	1	1	0	0	0	1
Fou	urth Address	1	1	0	0	0	1	1	0

Note : 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.

Asynchronous Truth Table

Operation	ZZ	OE	I/O STATUS
Sleep Mode	Н	Х	High-Z
Pood	L	L	DQ
Redu	L	Н	High-Z
Write	L	Х	Din, High-Z
Deselected	L	Х	High-Z

Notes

1. X means "Don't Care".

2. ZZ pin is pulled down internally

- 3. For write cycles that following read cycles, the output buffers must be disabled with OE, otherwise data bus contention will occur.
- Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- 5. Deselected means power down state of which stand-by current depends on cycle time.



Truth Tables

Synchronous Truth Table

CS ₁	CS2	CS ₂	ADSP	ADSC	ADV	Write	CLK	Address Accessed	Operation
Н	Х	Х	Х	L	Х	Х	\uparrow	N/A	Not Selected
L	L	Х	L	Х	Х	Х	\uparrow	N/A	Not Selected
L	Х	Н	L	Х	Х	Х	\uparrow	N/A	Not Selected
L	L	Х	Х	L	Х	Х	↑	N/A	Not Selected
L	Х	Н	Х	L	Х	Х	↑	N/A	Not Selected
L	Н	L	L	Х	Х	Х	\uparrow	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	Х	L	\uparrow	External Address	Begin Burst Write Cycle
L	Н	L	Н	L	Х	Н	\uparrow	External Address	Begin Burst Read Cycle
Х	Х	Х	Н	Н	L	Н	\uparrow	Next Address	Continue Burst Read Cycle
Н	Х	Х	Х	Н	L	Н	↑	Next Address	Continue Burst Read Cycle
Х	Х	Х	Н	Н	L	L	\uparrow	Next Address	Continue Burst Write Cycle
Н	Х	Х	Х	Н	L	L	↑	Next Address	Continue Burst Write Cycle
Х	Х	Х	Н	Н	Н	Н	↑	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Х	Н	Н	Н	\uparrow	Current Address	Suspend Burst Read Cycle
Х	Х	Х	Н	Н	Н	L	↑	Current Address	Suspend Burst Write Cycle
Н	Х	Х	Х	Н	Н	L	\uparrow	Current Address	Suspend Burst Write Cycle

Notes: 1. X means "Don't Care".

2. The rising edge of clock is symbolized by (\uparrow) .

3. $\overline{\text{Write}}$ = L means Write operation in Write Truth Table.

 $\overline{\text{Write}}$ = H means Read operation in Write Truth Table.

4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

Write Truth Table(x36)

GW	BW	WEa	WEb	WEc	WEd	Operation
Н	Н	Х	х	х	Х	Read
Н	L	Н	Н	Н	Н	Read
Н	L	L	Н	Н	Н	Write Byte A
Н	L	Н	L	Н	Н	Write Byte B
Н	L	Н	Н	L	L	Write Byte C And D
н	L	L	L	L	L	Write All Bytes
L	Х	Х	Х	Х	Х	Write All Bytes

Notes: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK($\uparrow\,$).

Write Truth Table(x18)

GW	BW	WEa	WEb	Operation
Н	Н	Х	Х	Read
Н	L	н	Н	Read
Н	L	L	Н	Write Byte A
Н	L	Н	L	Write Byte B
Н	L	L	L	Write All Bytes
L	Х	Х	Х	Write All Bytes

Notes: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK($\uparrow\,$).



Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss		Vdd	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to Vss		Vddq	Vdd	V
Voltage on Input Pin Relative to Vss		VIN	-0.3 to VDD+0.3	V
Voltage on I/O Pin Relative to Vss		Vio	-0.3 to VDDQ+0.3	V
Power Dissipation		PD	1.6	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TOPR	0 to 70	°C
Operating remperature	Industrial	Topr	-40 to 85	°C
Storage Temperature Range Under Bias		TBIAS	-10 to 85	°C

Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions (0°C \leq TA \leq 70°C)

Parameter	Symbol	Min	Тур.	Мах	Unit
Supply Voltage	VDD1	2.3	2.5	2.7	V
	VDDQ1	2.3	2.5	2.7	V
	Vdd2	3.1	3.3	3.5	V
	VDDQ2	2.3	3.3	3.5	V
Ground	Vss	0	0	0	V

Notes: 1. The above parameters are also guaranteed at industrial temperature range.

2. It should be VDDQ \leq VDD

Capacitence(TA=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	Cin	VIN=0V	-	5	pF
Output Capacitance	Соит	Vout=0V	-	7	pF

Note : Sampled not 100% tested.

Overshoot Timing



Undershoot Timing





DC Electrical Caracteristics

Parameter	Symbol	Test Conditions		Min	Max	Unit	Notes
Input Leakage Current(except ZZ)	IIL	VDD=Max ; VIN=Vss to VDD	-2	+2	uA		
Output Leakage Current	Iol	Output Disabled, Vout=Vss to VDDQ		-2	+2	uA	
Operating Current	Icc	Device Selected, IOUT=0mA,	-65	-	100	mA	1,2
Operating Current		$ZZ \leq VIL$, Cycle Time \geqtcycMin	-75	-	90		
	Isв	Device deselected, Iout=0mA, ZZ \leq VIL	1	-	45	mA	
		f=Max, All Inputs \leq VIL or \geq VIH					
Standby Current	ISB1			-	35	mA	
	ISB2	Device deselected, IOUT=0mA, $ZZ \ge VDD-0.2V$,		-	35	mA	
		f=Max, All Inputs \leq VIL or \geq VIH					
Output Low Voltage(3.3V I/O)	Vol	IoL=8.0mA		-	0.4	V	
Output High Voltage(3.3V I/O)	Vон	Іон=- 4.0mA		2.4	-	V	
Output Low Voltage(2.5V I/O)	Vol	IoL=1.0mA		-	0.4	V	
Output High Voltage(2.5V I/O)	Vон	Іон=-1.0mA		2.0	-	V	
Input Low Voltage(3.3V I/O)	VIL			-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	VIH			2.0	VDD+0.3**	V	3
Input Low Voltage(2.5V I/O)	VIL			-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	VIH			1.7	VDD+0.3**	V	3

Notes : The above parameters are also guaranteed at industrial temperature range.

1. Reference AC Operating Conditions and Characteristics for input and timing.

Data states are all zero.
In Case of I/O Pins, the Max. VIH=VDDQ+0.3V

Test Conditions

Parameter	Value
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3/2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	VDDQ/2
Output Load	See Fig. 1

The above parameters are also guaranteed at industrial temperature range.

Output Load(A)







* Including Scope and Jig Capacitance





AC Timing Characteristics

Parameter	Symbol	-65		-	Unit	
Farameter	Symbol	Min	Мах	Min	Max	Onit
Cycle Time	tcyc	7.5	-	8.5	-	ns
Clock Access Time	tcd	-	6.5	-	7.5	ns
Output Enable to Data Valid	toe	-	3.5	-	3.5	ns
Clock High to Output Low-Z	tlzc	2.5	-	2.5	-	ns
Output Hold from Clock High	tон	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tlzoe	0	-	0	-	ns
Output Enable High to Output High-Z	thzoe	-	3.5	-	3.5	ns
Clock High to Output High-Z	tHZC	-	3.8	-	4.0	ns
Clock High Pulse Width	tсн	2.5	-	2.5	-	ns
Clock Low Pulse Width	tcL	2.5	-	2.5	-	ns
Address Setup to Clock High	tas	1.5	-	1.5	-	ns
Address Status Setup to Clock High	tss	1.5	-	1.5	-	ns
Data Setup to Clock High	tDS	1.5	-	1.5	-	ns
Write Setup to Clock High (\overline{WE} , \overline{BWx})	tws	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	tadvs	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	tcss	1.5	-	1.5	-	ns
Address Hold from Clock High	tан	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tsн	0.5	-	0.5	-	ns
Data Hold from Clock High	tDн	0.5	-	0.5	-	ns
Write Hold from Clock High (\overline{WE} , \overline{BW} x)	twн	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tadvh	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tсsн	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tpus	2	-	2	-	cycle

Notes: 1. The above parameters are also guaranteed at industrial temperature range.
2. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
3. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
4. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.





S7B163635M S7B161835M

Sleep Mode

Sleep Mode is a low current, power-down mode in which the device is deselected and current is reduced to ISB2. The duration of Sleep Mode is dictated by the length of time the ZZ is in a High state.

After entering Sleep Mode, all inputs except ZZ become disabled and all outputs go to High-Z.

The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep Mode.

When the ZZ pin becomes a logic High, ISB2 is guaranteed after the time tzzI is met. Any operation pending when entering Sleep Mode is not guaranteed to successful complete. Therefore, Sleep Mode (Read or Write) must not be initiated until valid pending operations are completed. similarly, when exiting Sleep Mode during tPUS, only a Deselect or Read cycle should be given while the SRAM is transitioning out of Sleep Mode.

Sleep Mode Electrical Characteristics

Description	Condition	Symbol	Min	Max	Unit
Current during SLEEP MODE	$ZZ \geq VIH$	ISB2		35	mA
ZZ active to input ignored		t PDS	2		cycle
ZZ inactive to input sampled		tpus	2		cycle
ZZ active to SLEEP current		tzzı		2	cycle
ZZ inactive to exit SLEEP current		trzzi	0		



Sleep Mode Waveform

DON'T CARE





Timing Waveform of Read Cycle

Don't Care





NOTES : $\overline{Write} = L$ means GW = L, or GW = H, BW = L, WEx = L $\overline{CS} = L$ means $\overline{CS}_1 = L$, $CS_2 = H$ and $\overline{CS}_2 = L$ $\overline{CS} = H$ means $\overline{CS}_1 = H$, or $\overline{CS}_1 = L$ and $\overline{CS}_2 = H$, or $\overline{CS}_1 = L$, and $CS_2 = L$ Don't Care







Timing Waveform of Combination Read/Write Cycle(ADSP Controlled , ADSC=High)





Timing Waveform of Single Read/Write Cycle (ADSC Controlled , ADSP=High)



Timing Waveform of Single Read/Write Cycle (ADSP Controlled , ADSC=High)



 Don't Care





Application Information

Depth Expansion

The Netsol 512Kx36 Flow-Through SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 512K depth to 1M depth without extra logic.



Interleave Read Timing (Refer to non-interleave write timing for interleave write timing)





Application Information

Depth Expansion

The Netsol 1Mx18 Flow-Through SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 1M depth to 2M depth without extra logic.



Interleave Read Timing (Refer to non-interleave write timing for interleave write timing)





S7B163635M S7B161835M

512Kx36 & 1Mx18 Flow-Through SRAM

Package Dimensions

