S5N8944B

G.Lite
ADSL Transceiver for CO and CPE

Preliminary Information
(Revision 2.1)

June 2000

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1. Features

· Full Compliance with ITU-T **G.Lite** and **G.hs**
· FDM based **DMT** Line Coding
· Data Rate: Up to **3.5 Mbps** for Downstream and **600 kbps** for Upstream.
· Reach: **5.4 km** (18 kft) on **24 AWG** and **4 km** (13.5kft) on **26 AWG**
· **Rate Adaptive** Modem (steps of 32kbps)
· Reed-Solomon **Forward Error Correction** with **Interleaver**
· Frequency and Time Domain **Equalizer**
· Support **Fast Retraining** Function
· Support **Network Management** Function
· Support **Power Management** Function
· **Host Interface** (Intel/Motorola) and **ATM(UTOPIA-2)/non-ATM** Interface
· **0.25㎜, 2.5V** CMOS Technology
· Operating Temperature**: -40** °C to **85** °C
· Package Type: **160-QFP**

2. General Description

The S5N8944B is a complete ATM-based rate adaptive G.Lite ADSL modem solution with associated F/W and an Analog Front-End (S5N8943). The S5N8944B provides all the digital functions such as ATM TC, FEC codec with interleaver/de-interleaver, adaptive QAM codec, FFT/IFFT, equalizers, digital filters and so on.

There are four interfaces for external communications; UTOPIA-2 interface for direct connection to ATM systems, serial interface for non-ATM applications, 16-bit ADC/DAC interface, and host interface for general CPUs like Intel or Motorola.

The same chipset can be used at both sides of the link, Central Office and Customer Premises Equipment. The S5N8944B uses 17.664MHz Xtal oscillator as a master clock for CO side and 17.664MHz VCXO for CPE.

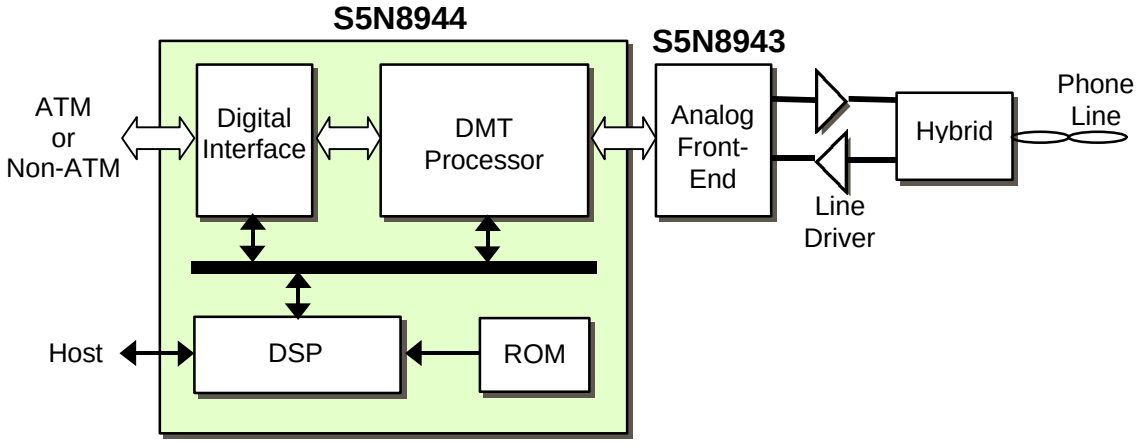


Figure 1: General Block Diagram

3. Logical Symbol Diagram

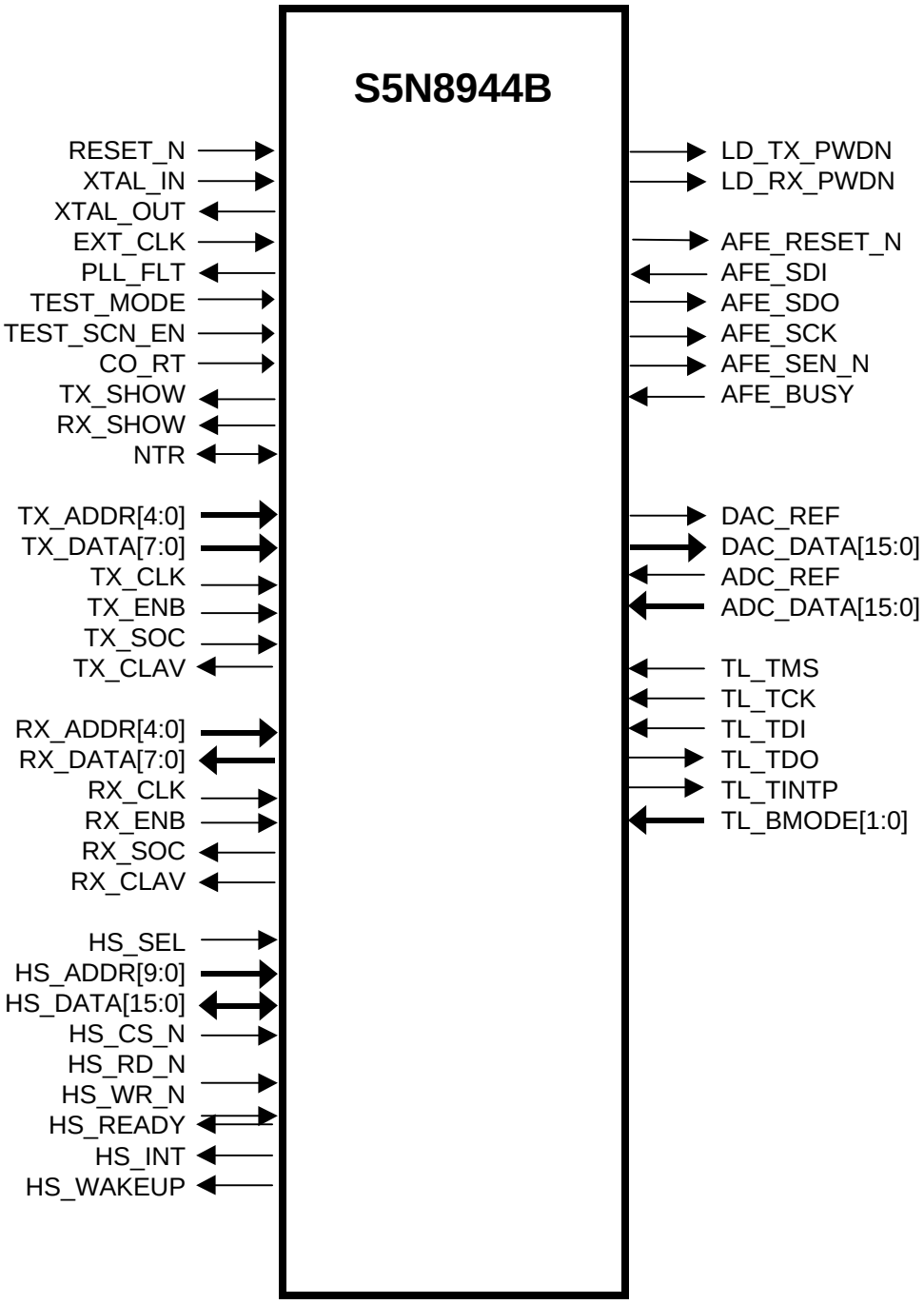


Figure 2: Logical Symbol Diagram of the S5N8944B

4. Pin Configuration

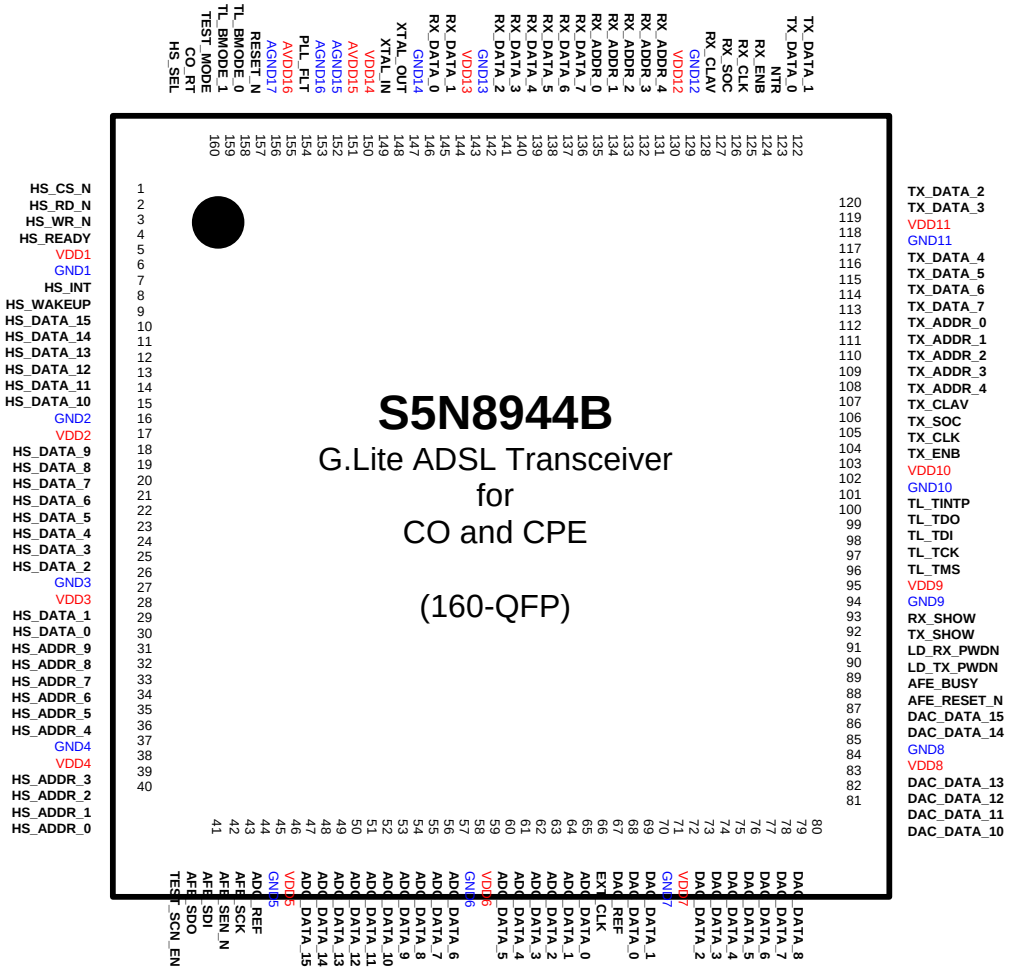


Figure 3: Pin Configuration of the S5N8944B

5. Pin Description

Table 1: Pin Description of the S5N8944B

No	Name	I/O	Description
155	**RESET_N**	I	System Master Reset (Active Low)
147	**XTAL_IN**	I	System Master Clock (17.664MHz Xtal Oscillator for CO, VCXO for CPE)
146	**XTAL_OUT**	O	
67	**EXT_CLK**	I	External Clock for Test (Not Used in Normal Mode, Pull-Down)
152	**PLL_FLT**	O	PLL Pump Out
158	**TEST_MODE**	I	[0] Normal Mode, [1] Test Mode
41	**TEST_SCN_EN**	I	Scan Enable (Set to '0' in Normal Mode)
159	**CO_RT**	I	[0] CO, [1] CPE
93	**TX_SHOW**	O	Tx Showtime (Active High. Connect to LED)
94	**RX_SHOW**	O	Rx Showtime (Active High. Connect to LED)
123	**NTR**	I/O	ATM Network Timing Reference (8KHz) (I: CO_RT=1, O: CO_RT=0)
108	**TX_ADDR_4**	I	Utopia Tx Address [4:0]
109	**TX_ADDR_3**		
110	**TX_ADDR_2**		
111	**TX_ADDR_1**		
112	**TX_ADDR_0**		
113	**TX_DATA_7**	I	Utopia Tx Data [7:0]
114	**TX_DATA_6**		
115	**TX_DATA_5**		
116	**TX_DATA_4**		
119	**TX_DATA_3**		
120	**TX_DATA_2**		
121	**TX_DATA_1**		
122	**TX_DATA_0**		
105	**TX_CLK**	I	Utopia Tx Clock (25MHz)
104	**TX_ENB**	I	Utopia Tx Enable
106	**TX_SOC**	I	Utopia Tx Start of Cell
107	**TX_CLAV**	OZ	Utopia Tx Cell Available
130	**RX_ADDR_4**	I	Utopia Rx Address [4:0]
131	**RX_ADDR_3**		
132	**RX_ADDR_2**		
133	**RX_ADDR_1**		
134	**RX_ADDR_0**		
135	**RX_DATA_7**	OZ	Utopia Rx Data [7:0]
136	**RX_DATA_6**		
137	**RX_DATA_5**		
138	**RX_DATA_4**		
139	**RX_DATA_3**		

140	**RX_DATA_2**		
143	**RX_DATA_1**		
144	**RX_DATA_0**		
125	**RX_CLK**	I	Utopia Rx Clock (25MHz)
124	**RX_ENB**	I	Utopia Rx Enable
126	**RX_SOC**	OZ	Utopia Rx Start of Cell
127	**RX_CLAV**	OZ	Utopia Rx Cell Available
160	**HS_SEL**	I	Host Interface Type Selection [0] Motorola, [1] Intel
29	**HS_ADDR_9**	I	Host Address [9:0]
30	**HS_ADDR_8**		
31	**HS_ADDR_7**		
32	**HS_ADDR_6**		
33	**HS_ADDR_5**		
34	**HS_ADDR_4**		
37	**HS_ADDR_3**		
38	**HS_ADDR_2**		
39	**HS_ADDR_1**		
40	**HS_ADDR_0**		
9	**HS_DATA_15**	B	Host Data [15:0]
10	**HS_DATA_14**		
11	**HS_DATA_13**		
12	**HS_DATA_12**		
13	**HS_DATA_11**		
14	**HS_DATA_10**		
17	**HS_DATA_9**		
18	**HS_DATA_8**		
19	**HS_DATA_7**		
20	**HS_DATA_6**		
21	**HS_DATA_5**		
22	**HS_DATA_4**		
23	**HS_DATA_3**		
24	**HS_DATA_2**		
27	**HS_DATA_1**		
28	**HS_DATA_0**		
1	**HS_CS_N**	I	Host Chip Select (Active Low)
2	**HS_RD_N**	I	**Motorola**: Not Used **Intel**: Host Read Enable (Active Low)
3	**HS_WR_N**	I	**Motorola**: [0] Write Enable, [1] Read Enable **Intel**: Write Enable (Active Low)
4	**HS_READY**	OZ	**Motorola**: DTACK (Active Low) **Intel**: Ready (Active High)
7	**HS_INT**	O	**Motorola**: IRQ (Active Low) **Intel**: INT (Active High)
8	**HS_WAKEUP**	OZ	Host Wakeup [0] Active, [Hi-Z] Disable
91	**LD_TX_PWDN**	O	Tx Line Driver Power-down (Active High)
92	**LD_RX_PWDN**	O	Rx Line Driver Power-down (Active High)

89	**AFE_RESET_N**	O	AFE Reset (Active Low)
43	**AFE_SDI**	I	AFE Serial Input Data (Pull-Up)
42	**AFE_SDO**	O	AFE Serial Output Data
45	**AFE_SCK**	O	AFE Serial Clock
44	**AFE_SEN_N**	O	AFE Serial Enable (Active Low)
90	**AFE_BUSY**	I	AFE Serial Busy (Active High, Pull-Down)
68	**DAC_REF**	O	DAC Data Reference (4.416MHz)
88	**DAC_DATA_15**	O	DAC Data [15:0]
87	**DAC_DATA_14**		
84	**DAC_DATA_13**		
83	**DAC_DATA_12**		
82	**DAC_DATA_11**		
81	**DAC_DATA_10**		
80	**DAC_DATA_9**		
79	**DAC_DATA_8**		
78	**DAC_DATA_7**		
77	**DAC_DATA_6**		
76	**DAC_DATA_5**		
75	**DAC_DATA_4**		
74	**DAC_DATA_3**		
73	**DAC_DATA_2**		
70	**DAC_DATA_1**		
69	**DAC_DATA_0**		
46	**ADC_REF**	I	Not Used in Normal Mode (Pull-Down)
49	**ADC_DATA_15**	I	ADC Data [15:0]
50	**ADC_DATA_14**		
51	**ADC_DATA_13**		
52	**ADC_DATA_12**		
53	**ADC_DATA_11**		
54	**ADC_DATA_10**		
55	**ADC_DATA_9**		
56	**ADC_DATA_8**		
57	**ADC_DATA_7**		
58	**ADC_DATA_6**		
61	**ADC_DATA_5**		
62	**ADC_DATA_4**		
63	**ADC_DATA_3**		
64	**ADC_DATA_2**		
65	**ADC_DATA_1**		
66	**ADC_DATA_0**		
97	**TL_TMS**	I	TeakLite JTAG Test Mode Selection
98	**TL_TCK**	I	TeakLite JTAG Test Clock
99	**TL_TDI**	I	TeakLite JTAG Test Data In
100	**TL_TDO**	OZ	TeakLite JTAG Test Data Out
101	**TL_TINTP**	O	TeakLite TJAM Interrupt to Host
157	**TL_BMODE_1**	I	TeakLite Boot Mode Selection [0] Reset, [1] Boot from Host [2] Boot from JTAG, [3] Self-Booting

156	**TL_BMODE_0**		
5	**VDD1**	P1	2.5V Supply Voltage
26	**VDD3**		
48	**VDD5**		
60	**VDD6**		
85	**VDD8**		
103	**VDD10**		
118	**VDD11**		
142	**VDD13**		
149	**AVDD15**	P1	2.5V Analog Supply Voltage
153	**AVDD16**		
16	**VDD2**	P1	3.3V Supply Voltage
36	**VDD4**		
72	**VDD7**		
96	**VDD9**		
129	**VDD12**		
148	**VDD14**		
6	**GND1**	P0	Digital Ground
15	**GND2**		
25	**GND3**		
35	**GND4**		
47	**GND5**		
59	**GND6**		
71	**GND7**		
86	**GND8**		
95	**GND9**		
102	**GND10**		
117	**GND11**		
128	**GND12**		
141	**GND13**		
145	**GND14**		
150	**AGND15**	P0	Analog Ground
151	**AGND16**		
154	**AGND17**		

I = Input
O = Output
OZ = Tri-state Output
B = Bi-direction
P1 = Power
P0 = Ground

6. Functional Description

The G.Lite ADSL modem consists of two main chips; ADSL Transceiver chip (S5N8944) and Analog Front-End chip (S5N8943). The Analog Front-End provides an analog interface with line

drivers and hybrid components to connect the PSTN. The ADSL Transceiver provides all the digital functions as depicted in Figure 4.

The input bit stream is divided into bit slices and they are fed into the QAM which are allocated to 128 subchannels according to the bit loading table. The bit slices are then converted to frequency-domain complex samples by the QAM encoders. The 256 complex samples are changed to 256 time-domain samples by IFFT. The Tx filter performs band separation and interpolation functions.

The received signals are attenuated and distorted in terms of both phase and amplitude. PLL fixes the phase errors within 4 samples using the 276kHz pilot tone transmitted from the CO side. The ones over 4 samples are fixed by the sync recovery algorithm using a known synchronization symbol. The TEQ is a filter that adaptively alters the channel so that the impulse response is reduced to the length of the cyclic prefix which will be removed prior to FFT. The FEQ is a one tap complex adaptive filter for each subchannel, which adjusts the gains and phases of the received signals. The equalizers are adaptively updated due to the transmission channel environment.

In FDM-based DMT (Discrete MultiTone) modulation, the frequency band, 0 to 552kHz, is divided into 128 equi-spaced subchannels, of which 26kHz (#6) to 134kHz (#31) is allocated for the upstream, and 142kHz (#33) to 548kHz (#127) for the downstream. The Nyquist rate, therefore, should be 1.104MHz(276kHz) .

DMT inherently transmits an optimized time-variable spectrum. This spectrum is adjusted according to the desired data rate and the transmission characteristics (transfer function and noise spectrum) on each and every subchannel. For this, CO and CPE transmit 128 4kHz-wide tone downstream and upstream respectively to each other during initialization. They measure the quality of each of these received tones and then decide whether a tone has sufficient quality to be used for further transmission and, if so, how much data this tone should carry relative to the other tones that are used. They inform the bit loading result to each other.

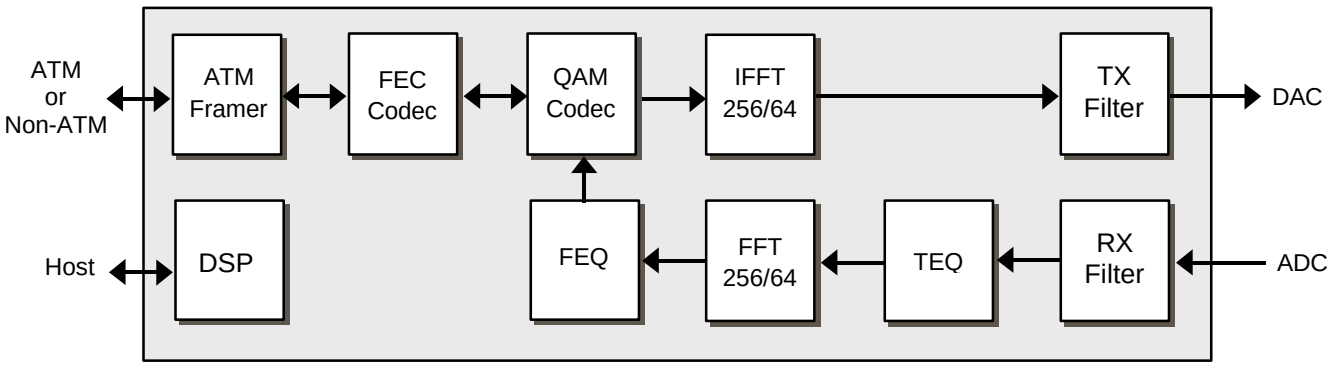
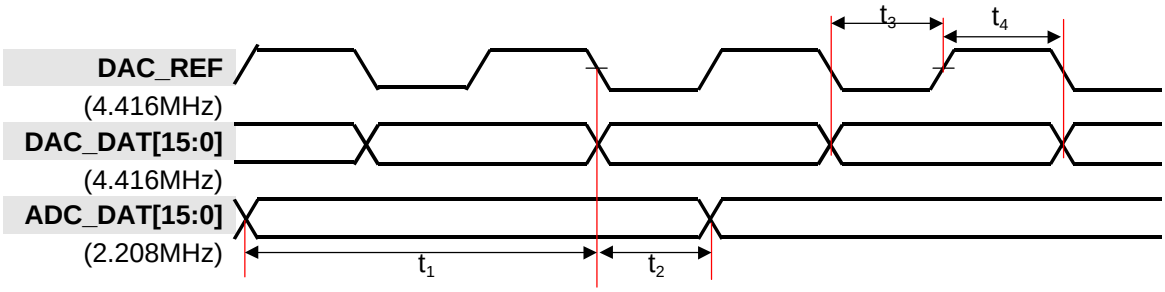


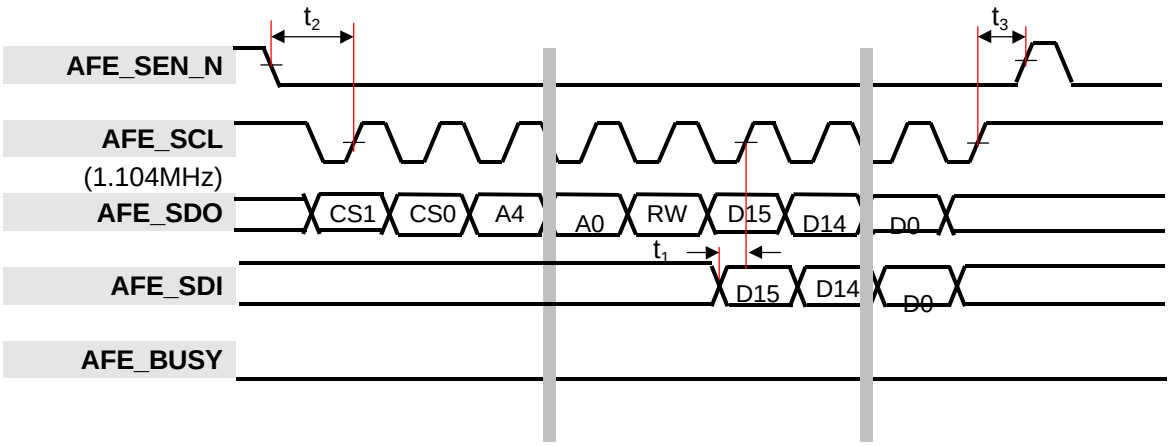
Figure 4: Functional Block Diagram of the S5N8944B

7. I/O Timing Description



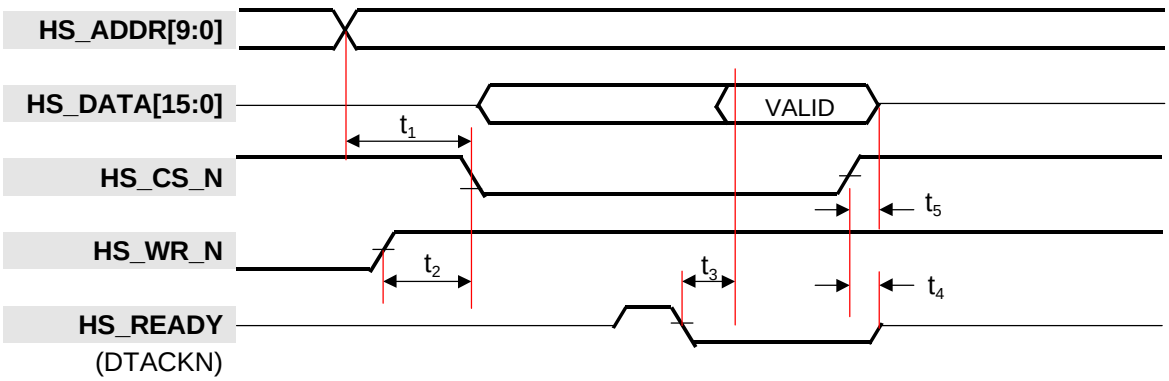
Parameter	Description	Min	Max	Unit
t_1	ADC_DAT setup to DAC_REF ↓	30		ns
t_2	ADC_DAT hold after DAC_REF ↓	1		ns
t_3	DAC_DAT setup to DAC_REF ↑	15		ns
t_4	DAC_DAT hold after DAC_REF ↑	15		ns

Figure 5: AFE Data I/F Timing Diagram



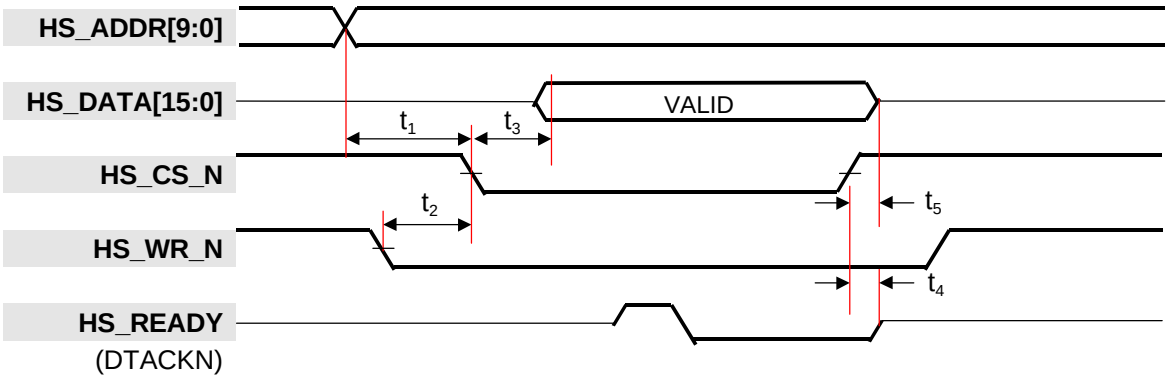
Parameter	Description	Min	Max	Unit
t_1	AFE_SDI setup to AFE_SCL ↑	30		ns
t_2	AFE_SEN_N ↓ before AFE_SCL ↑	30		ns
t_3	AFE_SEN_N ↑ from AFE_SCL ↑	15		ns

Figure 6: AFE Control I/F Timing Diagram



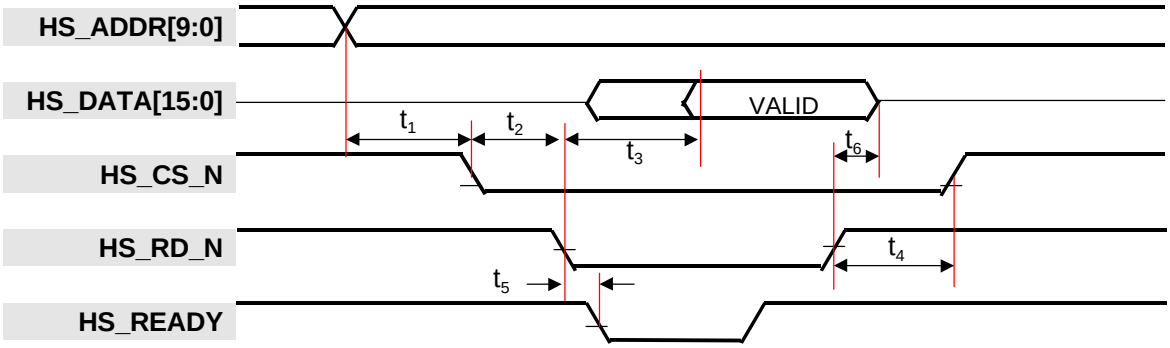
Parameter	Description	Min	Max	Unit
t_1	HS_ADDR setup to HS_CS_N ↓	0		ns
t_2	HS_WR_N ↑ before HS_CS_N ↓	0		ns
t_3	HS_DATA valid from HS_READY ↓		10	ns
t_4	HS_READY hi-Z from HS_CS_N ↑	1	5	ns
t_5	HS_DATA hold after HS_CS_N ↑		5	ns

Figure 7: Motorola Read Cycle Timing Diagram



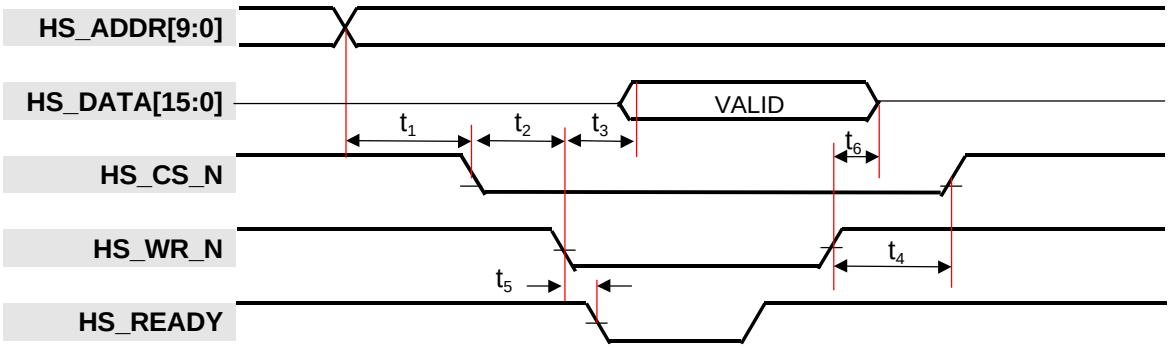
Parameter	Description	Min	Max	Unit
t_1	HS_ADDR setup to HS_CS_N ↓	0		ns
t_2	HS_WR_N ↓ before HS_CS_N ↓	0		ns
t_3	HS_DATA valid from HS_CS_N ↓		50	ns
t_4	HS_READY hi-Z from HS_CS_N ↑	1	5	ns
t_5	HS_DATA hold after HS_CS_N ↑	5		ns

Figure 8: Motorola Write Cycle Timing Diagram



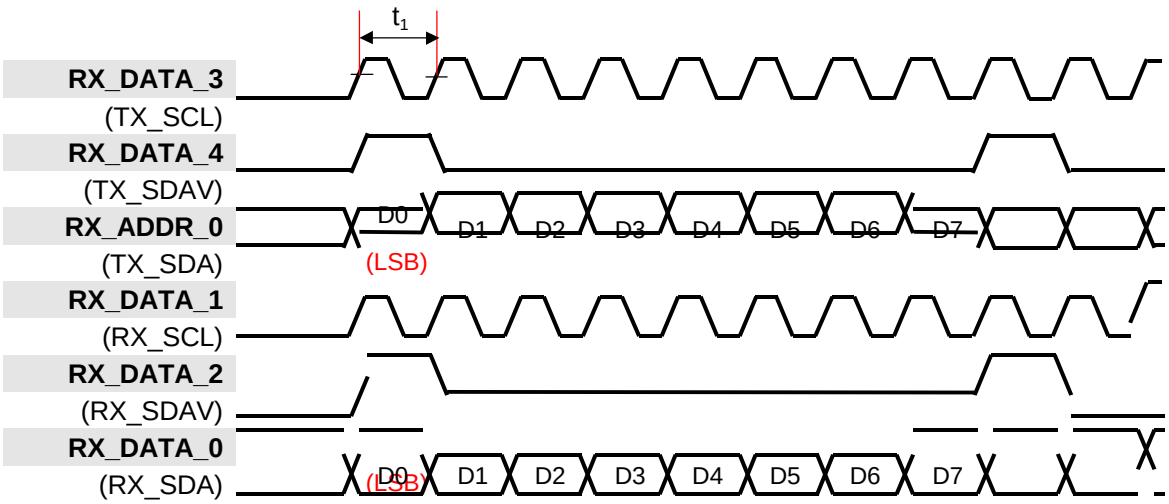
Parameter	Description	Min	Max	Unit
t_1	HS_ADDR setup to HS_CS_N ↓	0		ns
t_2	HS_CS_N ↓ before HS_RD_N ↓	0		ns
t_3	HS_DATA valid from HS_RD_N ↓		170	ns
t_4	HS_CS_N ↑ from HS_RD_N ↑	0		ns
t_5	HS_READY ↓ from HS_RD_N ↓	0	20	ns
t_6	HS_DATA hold after HS_RD_N ↑		5	ns

Figure 9: Intel Read Cycle Timing Diagram



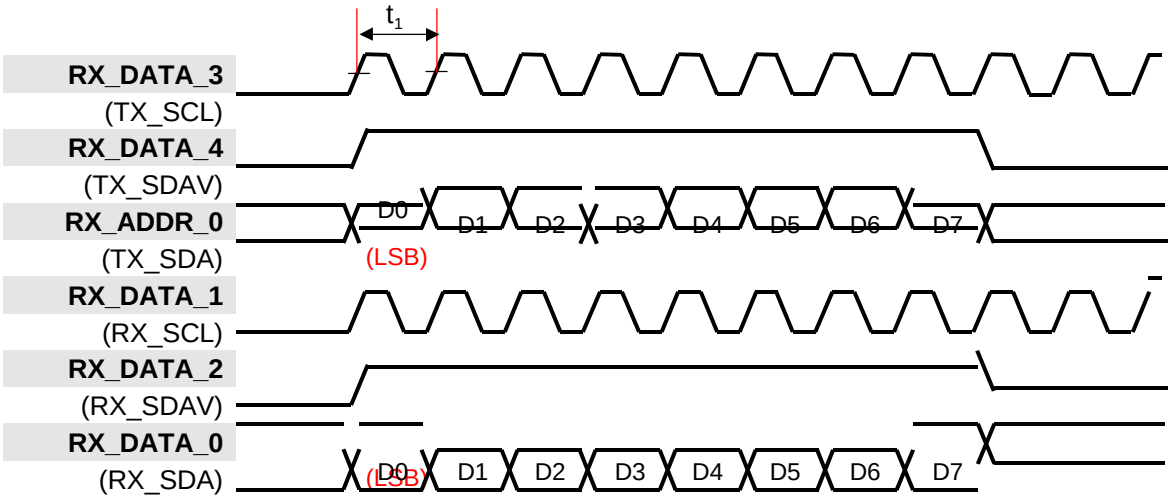
Parameter	Description	Min	Max	Unit
t_1	HS_ADDR setup to HS_CS_N ↓	0		ns
t_2	HS_CS_N ↓ before HS_WR_N ↓	0		ns
t_3	HS_DATA valid from HS_WR_N ↓		50	ns
t_4	HS_CS_N ↑ from HS_WR_N ↑	0		ns
t_5	HS_READY ↓ from HS_WR_N ↓	0	20	ns
t_6	HS_DATA hold after HS_WR_N ↑	5		ns

Figure 10: Intel Write Cycle Timing Diagram



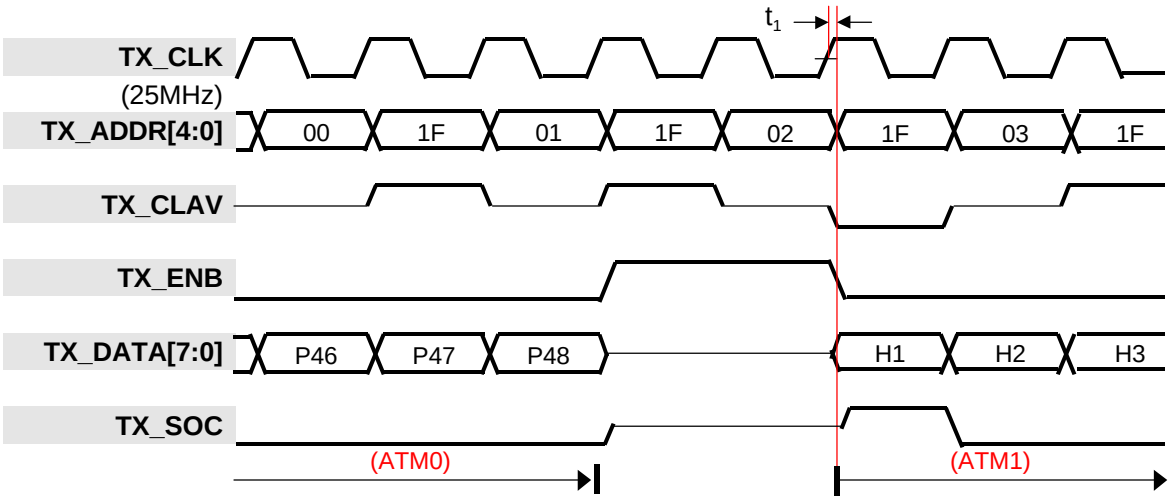
Parameter	Description	Min	Max	Unit
t_1	TX_SCL frequency	1	25	MHz

Figure 11: Non-ATM I/F (Byte Mode) Timing Diagram



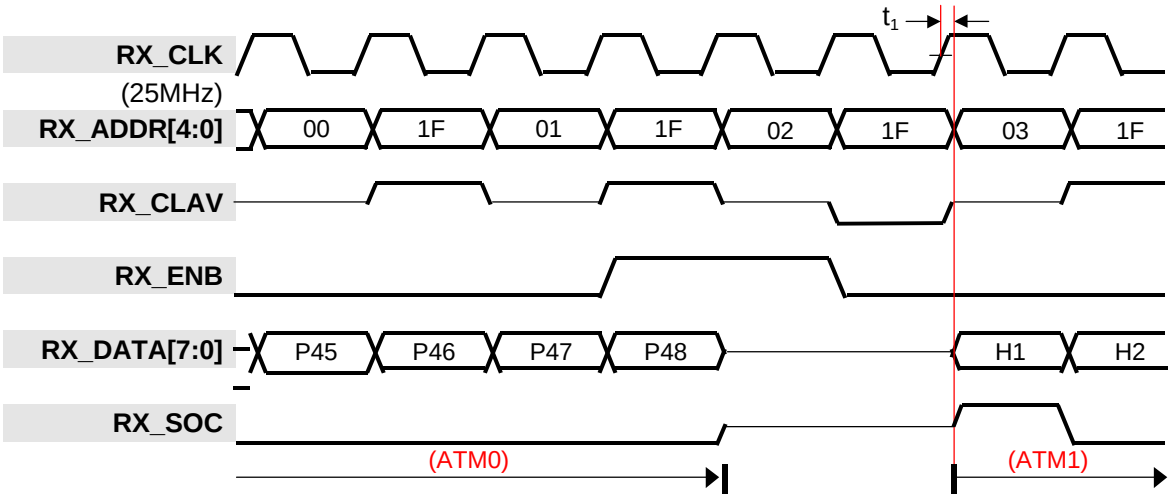
Parameter	Description	Min	Max	Unit
t_1	RX_SCL frequency	1	25	MHz

Figure 12: Non-ATM I/F (Envelope Mode) Timing Diagram



Parameter	Description	Min	Max	Unit
t_1	Signal Hold after TX_CLK ↑	5	10	ns

Figure 13: ATM I/F (UTOPIA-2 Transmit) Timing Diagram



Parameter	Description	Min	Max	Unit
t_1	Signal Hold after RX_CLK ↑	5	10	ns

Figure 14: ATM I/F (UTOPIA-2 Receive) Timing Diagram

8. Electrical Characteristics

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit
V_{DD}	DC Supply Voltage	3.6		V
V_{IN}	DC Input Voltage	2.5V Input Buffer	3.6	
		3.3V Input Buffer	4.6	
		5V-tolerant Input Buffer	6.5	
V_{OUT}	DC Output Voltage	2.5V Buffer	3.6	
		3.3V Buffer	4.6	
I_{LATCH}	Latch-up Current	±200		mA
T_{STG}	Storage Temperature	-65 to 150		°C

Table 3: Recommended Operating Conditions

Symbol	Parameter	Rating		Unit
V_{DD}	DC Supply Voltage	2.5V I/O	2.3 to 2.7	V
		3.3V I/O	3.0 to 3.6	
		5V-tolerant I/O	3.0 to 3.6	
	Analog Core DC Supply Voltage	2.5V Core	2.5±5%	
T_A	Operating Temperature (Ambient)	Industrial	-40 to 85	°C

Table 4: Power Dissipation

Symbol	Parameter	Min	Typ	Max	Unit
P_D	Power Dissipation	-	0.35	0.4	W

Table 5: DC Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
V_{IH}	Input High Voltage	1.7(0.7V_{DD})	-	-	V
V_{IL}	Input Low Voltage	-	-	0.7(0.3V_{DD})	
V_{OH}	Output High Voltage	1.9(2.4)	-	-	
V_{OL}	Output Low Voltage	-	-	0.5(0.4)	
VT	Switching Threshold	-	0.5V_{DD}	-	
VT^+	Schmitt Trigger, Positive-going Threshold	-	-	1.9(2.0)	
VT-	Schmitt Trigger, Negative-going Threshold	0.6(0.8)	-	-	
V_H	Schmitt Trigger , VT^+ - VT-	0.5	0.65(0.575)	0.8(0.65)	
I_{IH}	Input High Current (V_{IN}=V_{DD})	-10	-	10	µA
		10*	25(33)*	50(60)*	
I_{IL}	Input Low Current (V_{IN}=V_{SS})	-10	-	10	
		-50(-60)*	-25(-33)*	-10*	
I_{OZ}	Tri-state Output Leakage Current	-10	-	10	
I_{OS}	Output Short Circuit Current	-55	-	55	
I_{DD}	Quiescent Supply Current	-	-	100	
C_{IN}	Input Capacitance	-	-	4	pF
C_{OUT}	Output Capacitance	-	-	4	

NOTES:
1. () – in case of 5V-tolerant
2. * - input buffer with pull-up or pull-down.
3. C_{IN} and C_{OUT} exclude package parastics.

9. Package Description

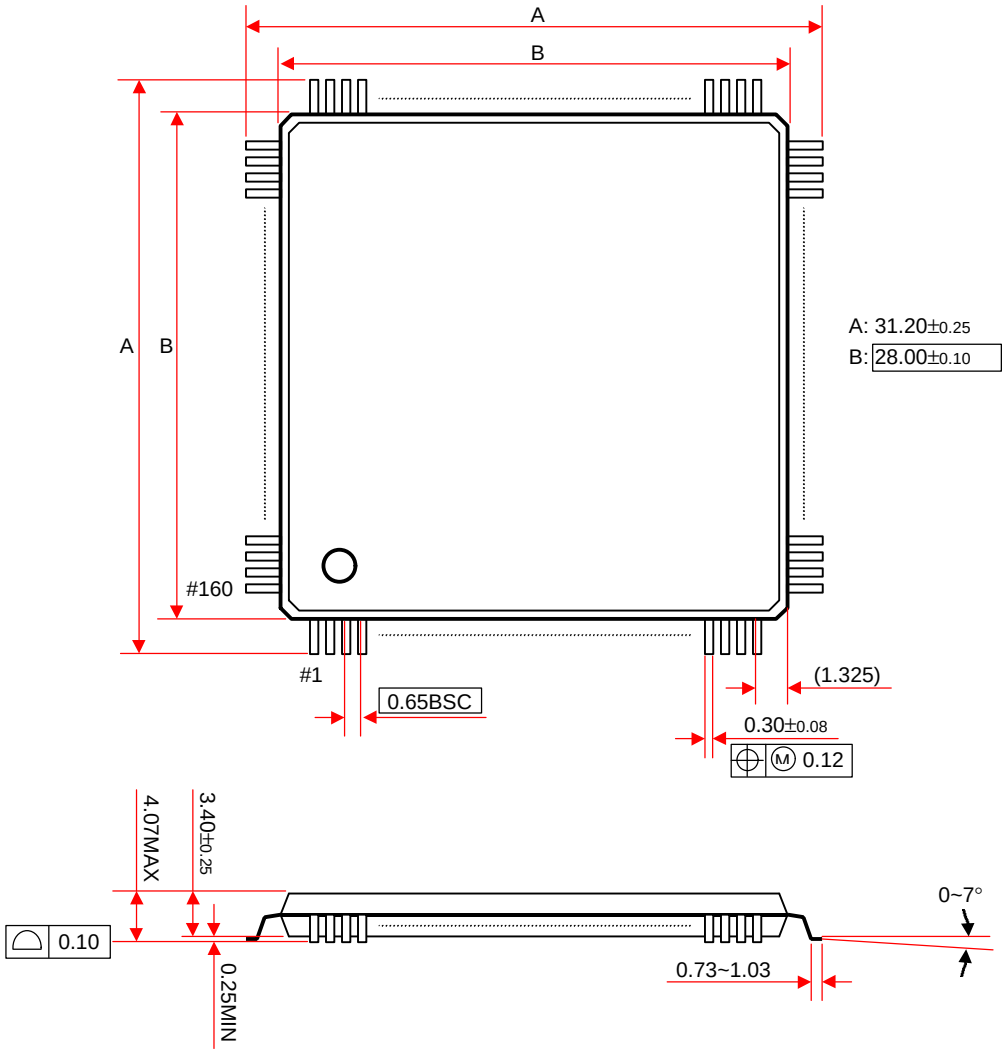


Figure 15: 160-QFP Package Diagram

Revision History

Revision No.	Date	Description
1.0	2000-02-01	**KS8944A** (Rev.1) Released.
2.0	2000-06-15	**S5N8944B** (Rev.2) Released. - Internal Memories Reduced. - Input Pin, **NOISE_DET** (41) changed to **TEST_SCN_EN**. - Output Pin, **GP_OUT_1** (93) changed to **TX_SHOW**. - Output Pin, **GP_OUT_0** (94) changed to **RX_SHOW**. - TC byte alignment problem fixed. - TX_DATA latched at the rising edge of TX_CLK.
2.1	2000-06-22	**160-QFP** Package Description Added. Pin Description Modified.

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