S5N8943B

G.Lite
ADSL Analog Front End IC

Preliminary Information
(Revision 1.0)

July 2000

Contents ***Page***

1. OVERVIEW

This chapter provides an overview of the S5N8943B01 ADSL ATU-C & ATU-R Analog Front End Chip.

1.1 General Descriptions

The S5N8943B01 is Analog Front End IC designed for DMT based universal ADSL(Asymmetric Digital Subscribe Line) modems with 0.35u fully CMOS technology.

It has 25.875 ~ 138KHz Upstream channel and 142.312 ~ 552KHz bandwidth Downstream channel. The S5N8943B01 includes AGC, LPF, ADC, DAC. The AGC has 42dB gain 0.4dB step in RX mode and –24dB gain 2dB step in TX mode with 12bit/8bit control bits. Anti alias LPF has 552KHz passband frequency in RX path and 138KHz in TX path. Samsung' s ADSL AFE chip provides 14bit ADC at 2.208M, 4.416M or 8.832M sample rates and 14bit 4.416MHz, 8.832MHz DAC.

An 10bit DAC support VCXO control for timing recovery. The VCXO is divided into a crystal driver at 35.328MHz.

1.2 Features

- Integrated Analog Front End(AFE) for ADSL ATU-C & ATU-R
- Complies with G.lite
- Up to 552Kbit/s down stream and 138Kbit/s upstream channel
- 14bit 2.208MS/s, 4.416MS/s or 8.832MS/s ADC
- 14bit 4.416MHz or 8.832MHz DAC
- 5^{th}-order Low Pass anti-alias Filter TX/RX paths
- RX 42dB 0.4dB step gain range with 12bit control signal
- TX -24dB 2dB step gain range with 8bit control signal
- 10bit 4KHz VCXO DAC
- Fully 0.35um CMOS technology
- 3.3V Power supply operation
- 0.4W Power comsumption

1.3 Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	DC Supply Voltage	-0.3		3.8	V
V_{IN}	DC input Voltage	-0.3		V_{DD}+0.3	V
	5V tolerant	-0.3		5.5	V
I_{IN}	DC input Current	-10		10	mA
T_{OPR}	Operation Temperature	-40		85	degree C
T_{STG}	Storage Temperature	-40		125	degree C

1.4 Electrical Specifications

Parameter	Min	Typ	Max	Units	Notes/Conditions
General					
Power Supply	3.0	3.3	3.6	V	
Power Consumption		450		mW	Normal Operation
Rx Path					
THD		70			
SNR		70			
AGC Gain Range	0		42	dB	12bit Control
AGC Step Size		0.4		dB	
AGC Step Error			0.2	dB	
AGC Input Range			2	Vppd	
LPF Cut Off Frequency		552		KHz	5^{th} Butterworth
LPF Output Range			2	Vppd	
LPF Pass Band Ripple	-0.5		0.5	dB	
LPF Stop Band Attenuation	60			dB	at 4.416MHz
TX Path					
THD		70			
SNR		70			
AGC Gain Range	-24		0	dB	8bit Control
AGC Step Size		2		dB	
AGC Step Error			0.2	dB	
AGC Output Range			2	Vppd	
LPF Cut Off Frequency		138		KHz	5^{th} Chebyshev
LPF Pass Band Ripple	-0.5		0.5	dB	
LPF Stop Band Attenuation	24			dB	at 276KHz
LPF Input Range			2	Vppd	
ADC					

Resolution		14		bits	
Effective Number Of Bits		13		bits	
Sampling Rate		2.208		MHz	Selectable 4.416MHz, 8.832MHz
Full Scale Input Range		2.0		Vppd	
DAC					
Resolution		14		bits	
Effective Number Of Bits		12		bits	
Sampling Rate		4.416		MHz	Selectable 8.832MHz
Full Scale Output Range		2.0		Vppd	
VCXO DAC					
Resolution		10		bits	
Sampling Rate		4		KHz	
Maximum Output Range		2.5		V	
Minimum Output Range		0.5		V	

2. SIGNAL DESCRIPTION

2.1 Functional Block Diagram

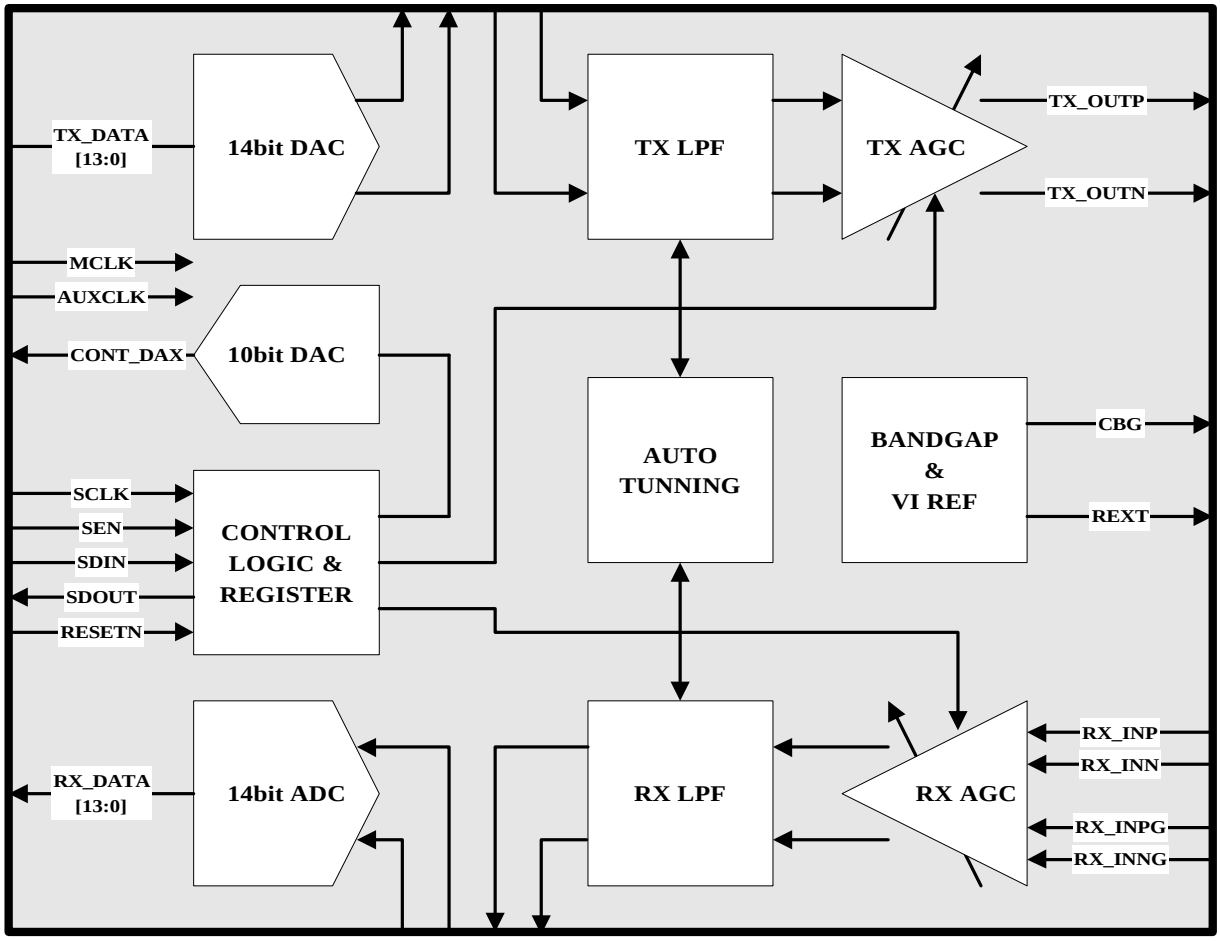


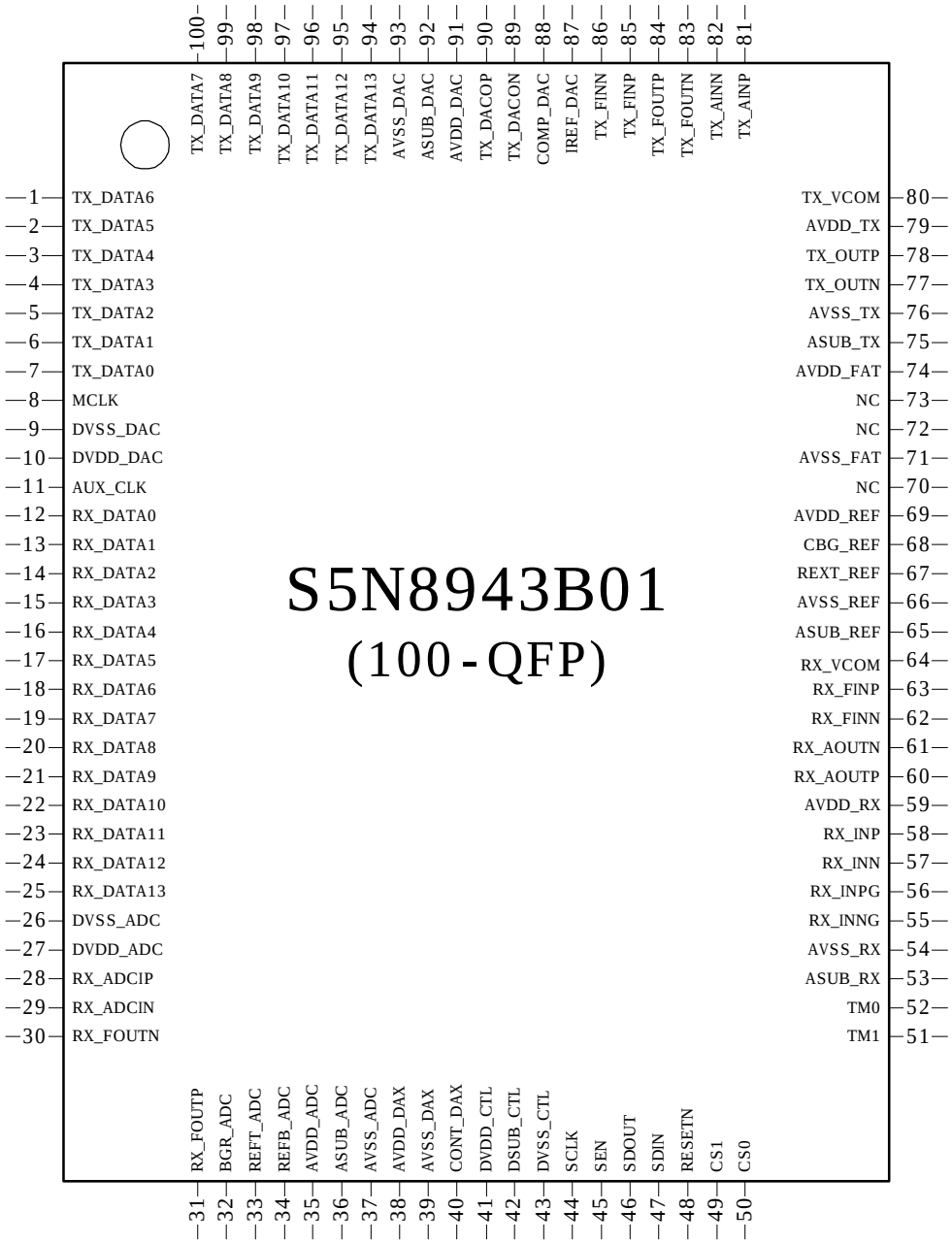
Figure 2.1.1 S5N8943B01 Functional Block Diagram

2.2 I/O Pins Description

Signal Name	Num	Type	I/O	Description
General Pins				
RESETN	48	CMOS	I	System Reset. Active Low
CS1	49	CMOS	I	Chip Select
CS0	50	CMOS	I	Chip Select
TM1	51	CMOS	I	Digital Interface Selection “0” = 14bits , “1”=7bits*2
TM0	52	CMOS	I	“0” = RT , “1” = CO
DAC Interface				
TX_DATA[13:0]	94~100, 1~7	CMOS	I	DAC 14bit Data Inputs If TM1=1, TX_DATA[13:7] is invalid
MCLK	8	CMOS	I	Master Clock 4.416MHz(Selectable 8.832M or 17.664M)
AUXCLK	11	CMOS	I	In 7bits Data Interface mode, AUXCLK=MCLK/2 In 14bits Data Interface mode, pin is open or ground.
TX_DACOP	90	Analog	-	DAC Current Positive Output for TX path
TX_DACON	89	Analog	-	DAC Current Negative Output for TX path
COMP_DAC	88	Analog	-	Compensation Capacitor 0.1uF Connection for TX path
IREF_DAC	87	Analog	-	External Resistor 1.24k Connection
ADC Interface				
RX_DATA[13:0]	12 ~ 25	CMOS	O	ADC 14bit Data Outputs (If TM1=1, [13:7] is always low)
RX_ADCIP	28	Analog	-	ADC Positive Input
RX_ADCIN	29	Analog	-	ADC Negative Input
BGR_ADC	32	Analog	-	ADC Band gap Reference Output
REFT_ADC	33	Analog	-	ADC Top Reference Output
REFB_ADC	34	Analog	-	ADC Bottom Reference Output
DSP Interface				
SCLK	44	CMOS	I	Serial Data Clock
SEN	45	CMOS	I	Serial Data Enable
SDOUT	46	CMOS	O	Serial Data Output
SDIN	47	CMOS	I	Serial Data Input
TX Pass Interface				
TX_OUTP	78	Analog	-	Tx Analog Positive Output
TX_OUTN	77	Analog	-	Tx Analog Positive Output
TX_FINP	85	Analog	-	Tx Filter Analog Positive Input
TX_FINN	86	Analog	-	Tx Filter Analog Negative Input
RX Pass Interface				
RX_INP	58	Analog	-	Rx Analog Positive Input
RX_INN	57	Analog	-	Rx Analog Negative Input
RX_INPG	56	Analog	-	Rx Analog External -14dB Gain Positive Input
RX_INNG	55	Analog	-	Rx Analog External -14dB Gain Negative Input
RX_FOUTP	31	Analog	-	Rx Filter Analog Positive Output
RX_FOUTN	30	Analog	-	Rx Filter Analog Negative Output
Voltage Reference				

TX_VCOM	80	Analog	-	TX Pass Common Mode Voltage
RX_VCOM	64	Analog	-	Rx Pass Common Mode Voltage
CBG_REF	68	Analog	-	Bandgap Reference Compensation Capacitor 100pF
REXT_REF	67	Analog	-	Reference Current External Resistor 6.8K
VCXO Interface				
CONT_DAX	40	Analog	-	VCXO Control Voltage Output **(Only RT)**
CO Pass (TM0 = "1")				
RX_AOUTP	60	Analog	-	Rx AGC Analog Positive Output
RX_AOUTN	61	Analog	-	Rx AGC Analog Negative Output
RX_FINN	62	Analog	-	Rx Filter Analog Negative Input
RX_FINP	63	Analog	-	Rx Filter Analog Positive Input
TX_AINP	81	Analog	-	Tx AGC Analog Positive Input
TX_AINN	82	Analog	-	Tx AGC Analog Positive Input
TX_FOUTN	83	Analog	-	Tx Filter Analog Negative Output
TX_FOUTP	84	Analog	-	Tx Filter Analog Negative Output
Power Supply				
AVDD_DAC	91	Supply	-	Tx Analog DAC VDD
ASUB_DAC	92	Supply	-	Tx Analog DAC SUB
AVSS_DAC	93	Supply	-	Tx Analog DAC VSS
DVDD_DAC	10	Supply	-	Tx Digital DAC VDD
DVSS_DAC	9	Supply	-	Tx Digital DAC VSS
AVDD_DAX	38	Supply	-	VCXO DAC Analog VDD
AVSS_DAX	39	Supply	-	VCXO DAC Analog VSS
AVDD_ADC	35	Supply	-	Rx Analog ADC VDD
ASUB_ADC	36	Supply	-	Rx Analog ADC SUB
AVSS_ADC	37	Supply	-	Rx Analog ADC VSS
DVDD_ADC	27	Supply	-	Rx Digital ADC VDD
DVSS_ADC	26	Supply	-	Rx Digital ADC VSS
AVDD_TX	79	Supply	-	Tx Path VDD
AVSS_TX	76	Supply	-	Tx Path VSS
ASUB_TX	75	Supply	-	TX Path SUB
AVDD_FAT	74	Supply	-	Filter Auto Tuning VDD
AVSS_FAT	71	Supply	-	Filter Auto Tuning VSS
AVDD_RX	59	Supply	-	Rx Filter VDD
AVSS_RX	54	Supply	-	Rx Filter VSS
ASUB_RX	53	Supply	-	Rx Filter SUB
AVDD_REF	69	Supply	-	Reference VDD
AVSS_REF	66	Supply	-	Reference VSS
ASUB_REF	65	Supply	-	Reference SUB
DVDD_CTL	41	Supply	-	Control Logic VDD
DSUB_CTL	42	Supply	-	Digital Substrate VSS
DVSS_CTL	43	Supply	-	Control Logic VSS

2.3 Pin Configurations (Top View)



3. BLOCK DESCRIPTIONS

3.1 ADC / DAC

S5N8943B01 has a 14bit resolution ADC 2.208M/4.416M/8.832M sample frequency. The input of ADC is fully differential 2.0Vppd Max. The ADC transforms the signal into a digital 14bit output.

There are two type of DAC' s in S5N8943B01. One is for TX. It is 14bit 4.416MHz/8.832MHz frequency. Samsung' s DMT(S5N8944) transmit 14bit parallel data to the AFE chip. The other DAC is for VCXO control. It has 10bit resolution 4KHz frequency. Internal registers of S5N8943B01 transform 10bit VCXO control serial data from DSP into 10bit parallel data. And VCXO output analog signal CONT_DAX(Pin #40).

3.2 TX/RX LPF

3.2.1 RX FILTERS

The combination of the external filter (an LC ladder filter typically) with the integrated low pass filter must provide:

- DMT sidelobe and out of band (anti-aliasing) attenuation
- Anti alias filter (60dB rejection @ image frequency)
- On chip tuning circuit included.

3.2.2 TX FILTERS

The TX Filters act not only to suppress the DMT sidebands but also as smoothing filters on the D/A converter' s output to suppress the image spectrum. For this reason they are realized in a time continuous approach and on chip tuning circuit included

3.3 TX/RX AGC

TX AGC has 0~-24dB gains with 2dB step. It is controlled through 8bit serial digital signal from DSP. Internal registers of Samsung AFE Chips transform 8bit parallel control data. It outputs 2Vppd fully differential signal to line driver.

RX AGC has low noise 0~42dB gains with 0.4dB step and It is controlled through 12bit + 1MSB control signal. If 1MSB is high, another RX input pass pin#55 RX_INNG #56 RX_INNP(external -14dB gain pass) is seclected. It inputs 2Vppd fully differential signal to RX LPF.

4. DIGITAL SIGNAL INTERFACE

4.1 Command Signal Interface

This description hold for ATU-R (S5N8943B01).

The chip consists of four kinds of register map:
- Power Control
- Transmitter AGC
- Receiver AGC
- VCXO Control
- Clock Selection

Serial interfaces use three pins:
- Clock
- Serial data input(25-bit: 2bit cs + 5bit address + 1bit r/w + 16 bit data + 1bit dummy)
- Serial data output(16 bit data)
- Enable

Serial Data Configuration

REGISTER	Serial Data (SDAT)																									
	CS		ADDRESS					R/W	DATA																	DUMMY
	CS1	CS0	A4	A3	A2	A1	A0	R/W	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X
PWR_CTL	CS1	CS0	X	X	0	0	0	R/W	X	X	X	X	X	X	X	X	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	X
TX_AGC	CS1	CS0	X	X	0	0	1	R/W	X	X	X	X	X	X	X	X	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0	X
RX_AGC	CS1	CS0	X	X	0	1	0	R/W	X	X	X	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	X
VCXO_CTL	CS1	CS0	X	X	0	1	1	R/W	X	X	X	X	X	X	VC9	VC8	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	X
CLK_SEL	CS1	CS0	X	X	1	0	0	R/W	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CK1	CK0	X

X = Don' t care

R/W =0 -> Read
R/W =1 -> Write

4.1.1 Register Map

4.1.1.1 Power Control

The power on/off control of AFE blocks on this chip is set by the PWR_CTL register, (XX000), as described below:

PWR_CTL Register (A4A3A2A1A0=XX000)

DATA	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME									PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET VALUE									0	0	0	0	0	0	0	0

Power Control is as follow.

PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	HEX	DESCRIPCION
0	0	0	0	0	0	0	0	0000	Normal Operation
0	0	0	0	0	0	0	1	0001	N/A
0	0	0	0	0	0	1	0	0002	N/A
0	0	0	0	0	1	0	0	0004	TX DAC Power Down
0	0	0	0	1	0	0	0	0008	TX Filter & AGC Power Down
0	0	0	1	0	0	0	0	0010	RX ADC Power Down
0	0	1	0	0	0	0	0	0020	Rx Filter Power Down
0	1	0	0	0	0	0	0	0040	Rx AGC Power Down
1	0	0	0	0	0	0	0	0080	VCXO DAC Power Down
Adding Power Down (based on upper power down)									
0	0	0	0	0	0	1	1	0003	N/A
0	0	0	0	1	1	0	0	000C	TX Path Power Down
0	1	1	1	0	0	0	0	0070	Rx Path Power Down
1	1	1	1	1	1	1	1	00FF	Whole Chip Power Down

4.1.1.2 Transmitter AGC

The main functions of the TX path are controlled by the TX_AGC registers, as described below:

TX_AGC Register (A4A3A2A1A0=XX001)

DATA	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME									TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0
RESET VALUE									0	0	0	1	0	0	0	1

TA[7:0] TX path output attenuator gain setting. 0 to –24dB attenuation in 2 dB steps. (default is 0 dB).

TA[7]	TA[6]	TA[5]	TA[4]	TA[3]	TA[2]	TA[1]	TA[0]	HEX	GAIN(dB)
0	0	0	1	0	0	0	1	0011	0
0	0	0	1	0	0	1	0	0012	-2
0	0	0	1	0	1	0	0	0014	-4
0	0	0	1	1	0	0	0	0018	-6
0	0	1	0	0	0	0	1	0021	-6
0	0	1	0	0	0	1	0	0022	-8
0	0	1	0	0	1	0	0	0024	-10
0	0	1	0	1	0	0	0	0028	-12
0	1	0	0	0	0	0	1	0041	-12
0	1	0	0	0	0	1	0	0042	-14
0	1	0	0	0	1	0	0	0044	-16
0	1	0	0	1	0	0	0	0048	-18
1	0	0	0	0	0	0	1	0081	-18
1	0	0	0	0	0	1	0	0082	-20
1	0	0	0	0	1	0	0	0084	-22
1	0	0	0	1	0	0	0	0088	-24

4.1.1.3 Recieve AGC

The main functions of the RX path are controlled by the RX_AGC register, as described below:

RX_AGC Register (A4A3A2A1A0=XX010)

DATA	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME				RA 12	RA 11	RA 10	RA9	RA8	RA7	RA6	RA4	RA4	RA3	RA2	RA1	RA0
RESET VALUE				0	0	0	0	0	1	0	0	1	0	0	0	0

RA[11:0]: Receive path input gain setting 0 to 42dB gain in 0.4 dB steps. (default is 0 dB).
RA[12] is "1",the external attenuation gain(ex, –14dB) path pin#55 RX_INNG #56 RX_INPG will be enable. RA[12] should only be utilized the short line conditions.

RA [12]	RA [11]	RA [10]	RA [9]	RA [8]	RA [7]	RA [6]	RA [5]	RA [4]	RA [3]	RA [2]	RA [1]	RA [0]	HEX	GAIN(dB)
1	0	0	0	0	1	0	0	1	0000 ~ 1111				1090~109F	-14.0~-8.0
1	0	0	0	1	0	0	0	1	0000 ~ 1111				1110~111F	-8.0~-2.0
1	0	0	1	0	0	0	0	1	0000 ~ 1111				1210~121F	-2.0~4.0
0	0	0	0	0	1	0	0	1	0	0	0	0	0090	0
0	0	0	0	0	1	0	0	1	0	0	0	1	0091	0.4
0	0	0	0	0	1	0	0	1	0	0	1	0	0092	0.8
0	0	0	0	0	1	0	0	1	0	0	1	1	0093	1.2
0	0	0	0	0	1	0	0	1	0	1	0	0	0094	1.6
0	0	0	0	0	1	0	0	1	0	1	0	1	0095	2.0
0	0	0	0	0	1	0	0	1	0	1	1	0	0096	2.4
0	0	0	0	0	1	0	0	1	0	1	1	1	0097	2.8
0	0	0	0	0	1	0	0	1	1	0	0	0	0098	3.2
0	0	0	0	0	1	0	0	1	1	0	0	1	0099	3.6
0	0	0	0	0	1	0	0	1	1	0	1	0	009A	4.0
0	0	0	0	0	1	0	0	1	1	0	1	1	009B	4.4
0	0	0	0	0	1	0	0	1	1	1	0	0	009C	4.8
0	0	0	0	0	1	0	0	1	1	1	0	1	009D	5.2
0	0	0	0	0	1	0	0	1	1	1	1	0	009E	5.6
0	0	0	0	0	1	0	0	1	1	1	1	1	009F	6.0
0	0	0	0	1	0	0	0	1	0000 ~ 1111				0110~011F	6.0~12.0
0	0	0	1	0	0	0	0	1	0000 ~ 1111				0210~021F	12.0~18.0
0	0	1	0	0	0	0	0	1	0000 ~ 1111				0410~041F	18.0~24.0
0	1	0	0	0	0	0	0	1	0000 ~ 1111				0810~081F	24.0~30.0
0	1	0	0	0	0	0	1	0	0000 ~ 1111				0820~082F	30.0~36.0
0	1	0	0	0	0	1	0	0	0000 ~ 1111				0840~084F	36.0~42.0

4.1.1.4 VCXO Control

The VCXO DAC is 10-bit voltage-mode DAC designed to be monotonic and intended to be operated at a 4 kHz update rate. In order to update the DAC, the user must write to the VCXO register through the serial port. The individual bit definitions are given below.

VCXO_CTL Register (A4A3A2A1A0=XX011)

DATA	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME							VC9	VC8	VC7	VC6	VC4	VC4	VC3	VC2	VC1	VC0
RESET VALUE							1	0	0	0	0	0	0	0	0	0

VC[9:0]: VCXO DAC 10-bit word. The DAC nominal output voltages for extreme and mid-scale codes are as follows.

VC[9:0] = 0000000000 = 0.5 V
VC[9:0] = 1000000000 = 1.5 V (mid-range)
VC[9:0] = 1111111111 = 2.5 V

A general expression for the DAC output voltage is
0.5 V + (CODE / 1024) X (2.0 V)

where *CODE* is the decimal integer value of the 10-bit word formed by VCXO[9:0].

4.1.1.5 Clock Selection

Main functions of Clock Selection are frequency selection of each MCLK/AUXCLK/ADC. The individual bit definitions are given below.

CLK_SEL Register (A4A3A2A1A0=XX100)

DATA	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME															CK1	CK0
RESET VALUE															0	0

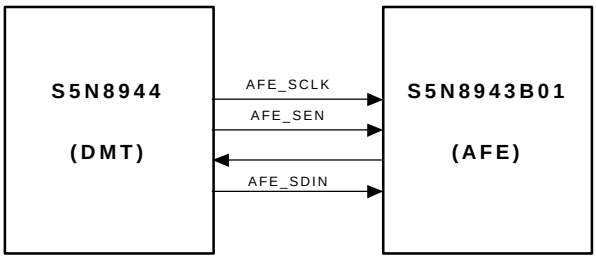
TM1, CK[1:0] : Clock Selection has eight possible clocking configuration as follow.

TM1	2 Phase	CK1	CK0	HEX	MCLK	AUXCLK	DAC	ADC
0	OFF	0	0	0000	4.416 MHz	0	4.416 MHz	2.208 MHz
0	OFF	0	1	0001	4.416 MHz	0	4.416 MHz	4.416 MHz
0	OFF	1	0	0002	8.832MHz	0	8.832MHz	4.416 MHz
0	OFF	1	1	0003	8.832MHz	0	8.832MHz	8.832MHz
1	ON	0	0	0000	8.832MHz	4.416 MHz	4.416 MHz	4.416 MHz
1	ON	0	1	0001	8.832MHz	4.416 MHz	4.416 MHz	2.204 MHz
1	ON	1	0	0002	17.664MHz	8.832MHz	8.832MHz	8.832 MHz
1	ON	1	1	0003	17.664MHz	8.832MHz	8.832MHz	4.416 MHz

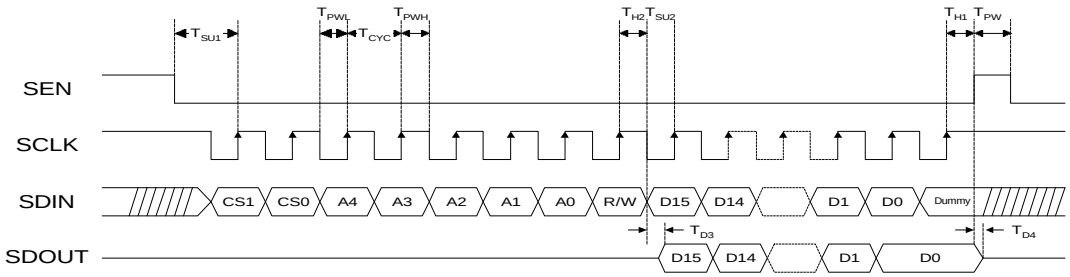
4.1.2 Serial Data Interface

4.1.2.1 Physical Interface

Serial interfaces use three pins:
- Clock
- Serial data (25-bit: 2bit cs + 5bit address + 1bit r/w + 16 bit data + 1bit dummy)
- Enable



4.1.2.2 Waveform

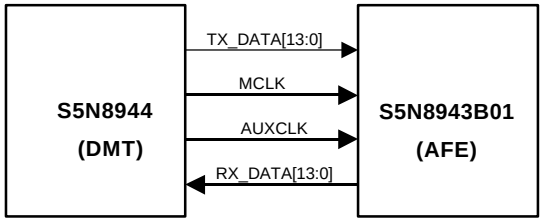


Parameter	Symbol	Min	Typ	Max	Unit
SCLK Clock Period	T_{CYC}		905		nS
SCLK High Time	T_{PWH}	452			nS
SCLK Low Time	T_{PWL}	452			nS
SEN Low To SCLK High	T_{SU1}	30			nS
SCLK High To SEN High	T_{H1}	15			nS
SEN Inactive Pulse Time	T_{PW}	905			nS
SDIN Setup time	T_{SU2}	15			nS
SDIN Hold time	T_{H2}	15			nS
SCLK low to SDOUT delay	T_{D3}			30	nS
SEN inactive to SDOUT HiZ	T_{D4}			30	nS

4.2 Data Interface

4.2.1 Physical Interface

- **ADC and DAC data transmission between S5N8943B01 and S5N8944**
- **Parallel Interface(S5N8944) : 29 pin (14 ADC bit data, 14 DAC bit data, MCLK)**
- **Parallel Interface : 16 pin (7 ADC bit data, 7 DAC bit data, MCLK,AUXCLK)**



4.2.2 Waveform

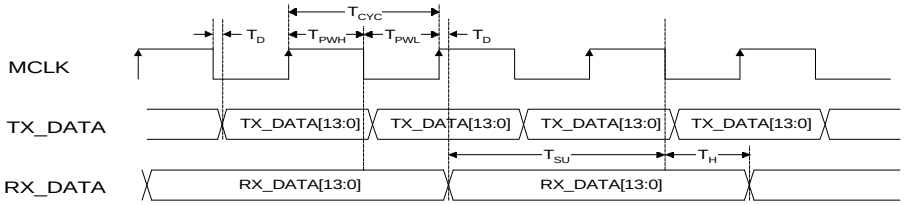


Figure 4.2.1 Waveform of 14bit parallel interface (TM1=0)

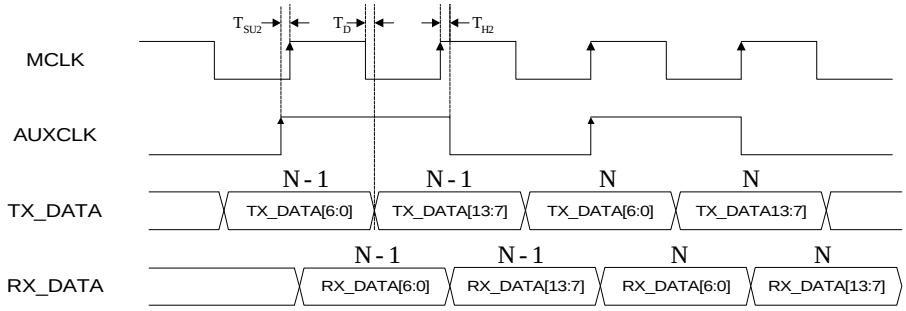
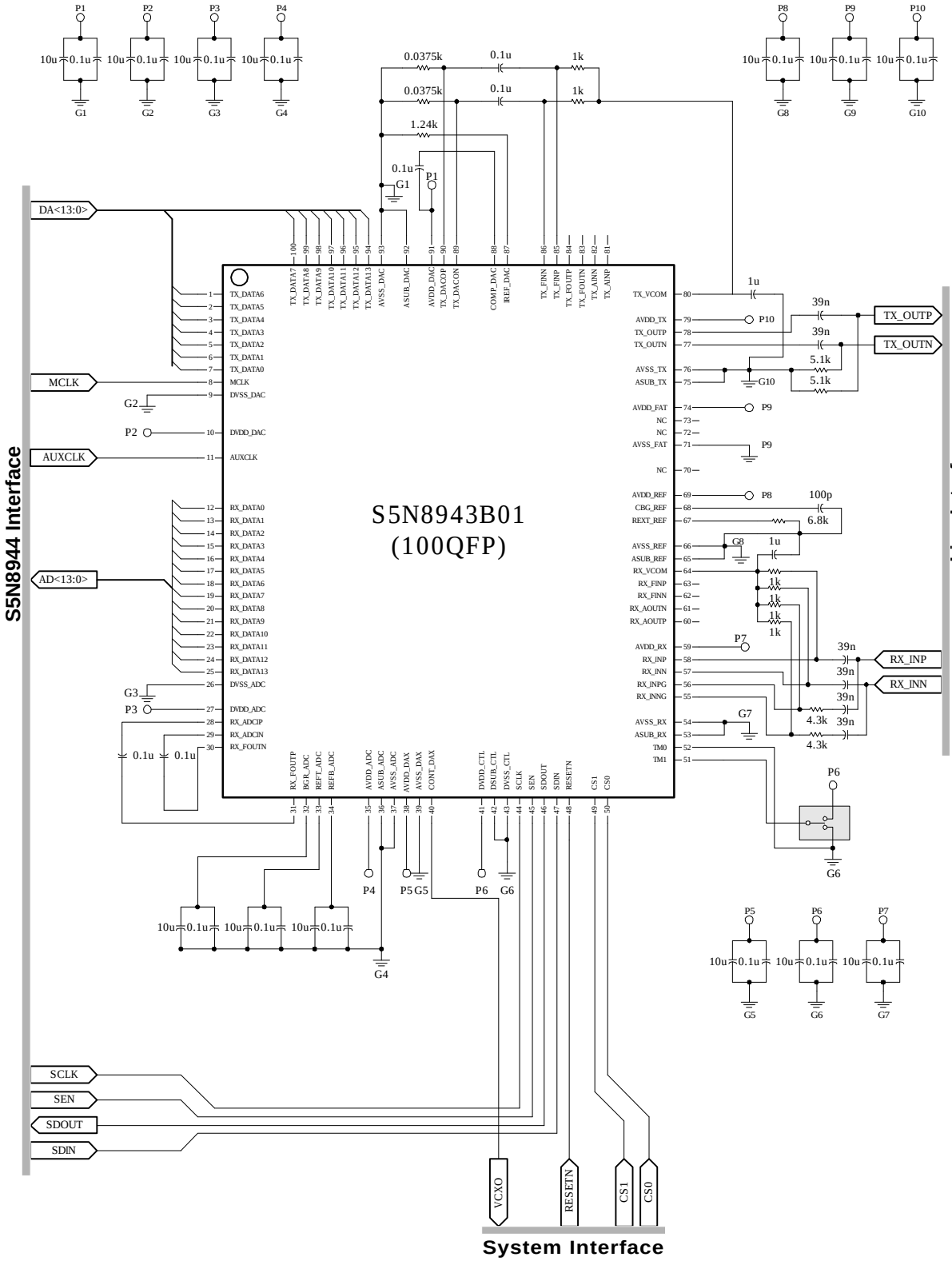


Figure 4.2.2 Waveform of 7bit parallel interface (TM1=1)

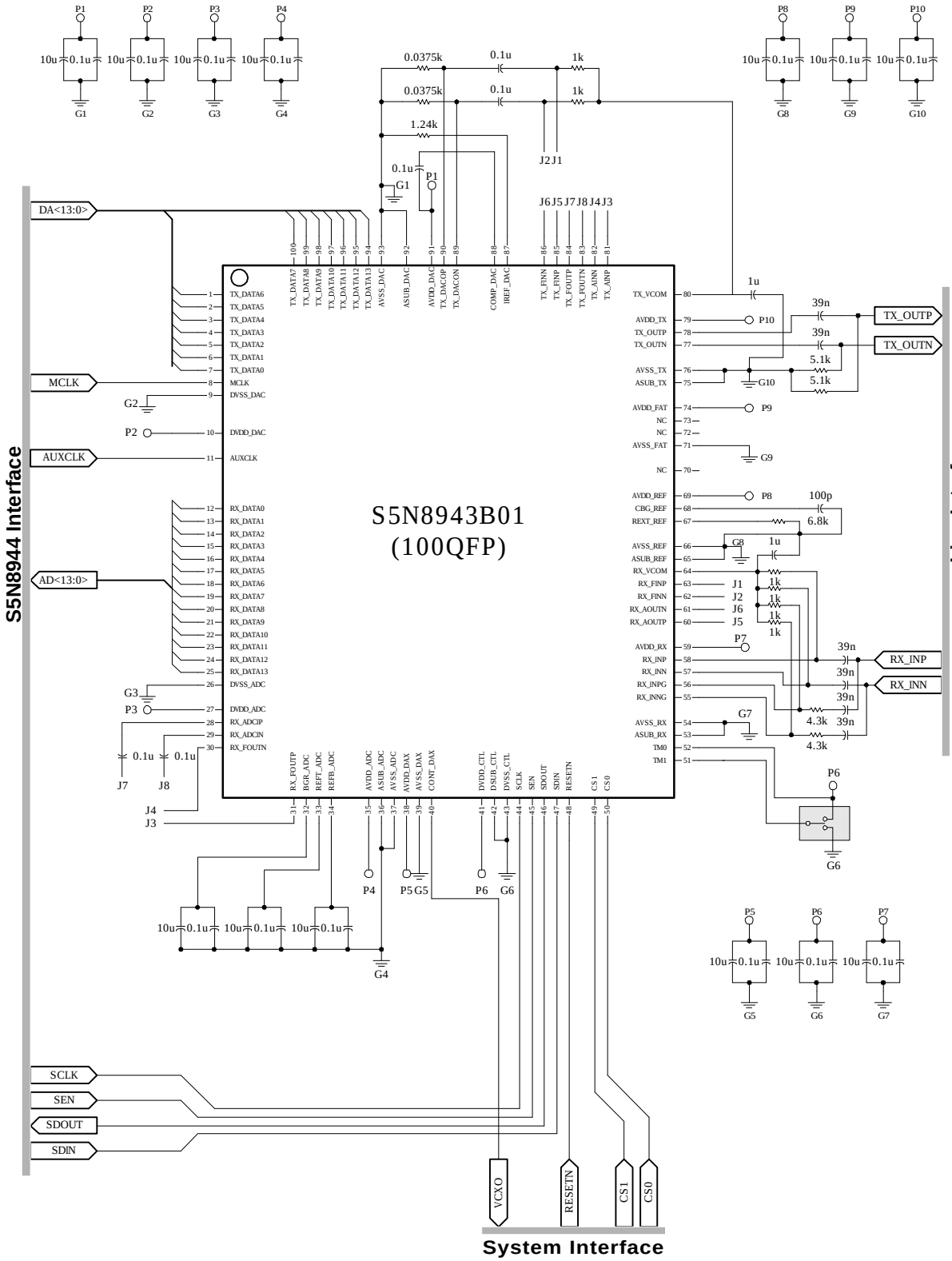
Parameter	Symbol	Min	Typ	Max	Unit	Note
MCLK Clock Period	T_{CYC}		226		nS	MCLK=4.416MHz
MCLK High Time	T_{PWH}		113		nS	MCLK=4.416MHz
MCLK Low Time	T_{PWL}		113		nS	MCLK=4.416MHz
DATA Delay after MCLK	T_D			10	nS	
RX_DATA setup to MCLK	T_{SU}	30			nS	MCLK=4.416MHz
RX_DATA hold to MCLK	T_H	84			nS	MCLK=4.416MHz
AUXCLK setup to MCLK	T_{SU2}			10	nS	
AUXCLK hold to MCLK	T_{H2}			10	nS	

5. Application Circuit

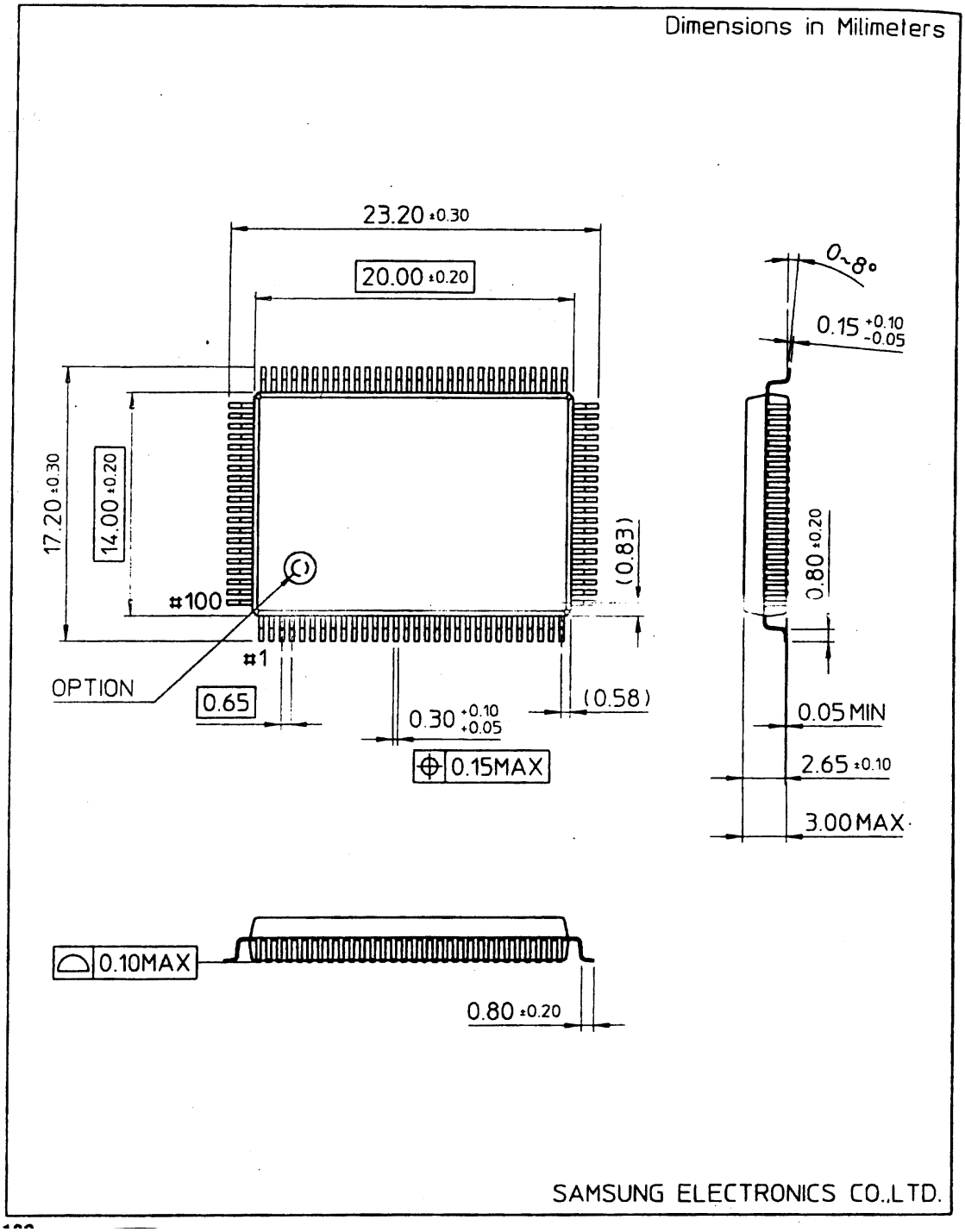
5.1 ATU-R



5.2 ATU-C


S5N8943B01
(100QFP)
S5N8944 Interface
Line Interface
System Interface
DA<13:0>
AD<13:0>
MCLK
AUXCLK
SCLK
SEN
SDOUT
SDIN
VCXO
RESETN
CS1
CS0
TX_OUTP
TX_OUTN
RX_INP
RX_INN

6. Package Information (100QFP-1420C)



Revision History

Revision No.	Date	Description
1.0	2000-07-20	**S5N8943B** (Rev.1) Released.

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