S5K3A1EA
(1/3” SXGA CMOS Image Sensor)

Preliminary Specification

Revision 0.4

Jun, 2004

DOCUMENT TITLE

1/3" Optical Size 1280x1024(SXGA) 2.8V / 1.8V CMOS Image Sensor

REVISION HISTORY

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	Feb.03, 2004	Preliminary
0.1	DC Characteristics Changed.	Mar.29.2004	
0.2	Register Map Updated.	Apr.09.2004	
0.3	Imaging Characteristics Changed	Jun.10.2004	
0.4	Imaging Characteristics Changed S5K3A1EA13 Product Added AC Characteristics Changed Ob_area Recommended Setting Changed	Jun.11.2004	

INTRODUCTION

The S5K3A1EA is highly integrated single chip CMOS image sensor, fabricated by SAMSUNG 0.18um CMOS image sensor process technology. It is developed for image application to realize high efficiency photo sensor. The sensor has 1280 x 1024 effective pixels with 1/3 inch optical format. The sensor has on-chip 10-bit ADC blocks to digitize the pixel output and also on-chip CDS to reduce Fixed Pattern Noise (FPN) drastically. With its few interface signals and 10-bit raw data directly connected to the external devices, a camera system can be configured easily.

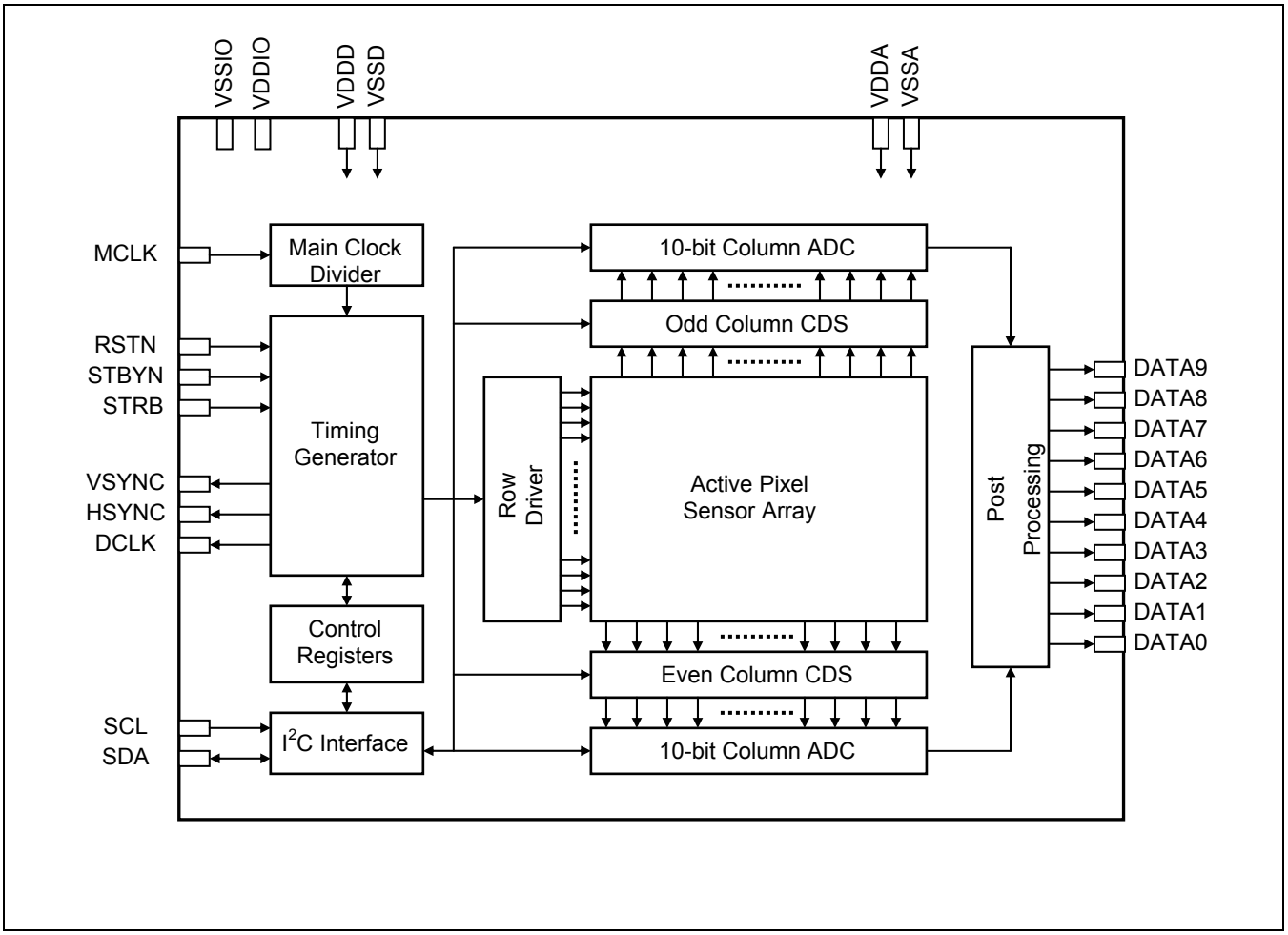
FEATURES

- Process Technology: 0.18μm Dual Gate Oxide SPQM CMOS
- Optical Size: 1/3 inch
- Unit Pixel: 3.8 μm X 3.8 μm
- Effective Resolution: 1280X1024, SXGA
- Line Progressive Read Out.
- 10-bit Raw Image Data Output
- Windowing and Panning
- Sub-Sampling (2X, 4X, 8X)
- Timing Generator for Frame Memoryless Scaler
- Timing Generator for Stepless Zooming
- Continuous and Single Frame Capture Mode
- Programmable Exposure Time and Gain Control
- Auto Dark Level Compensation
- Standby Mode for Power Saving
- Maximum 15 Frames per Second for Full Frame Readout with 24 MHz Output Data Rate
- Bad Pixel Replacement
- Dual Power Supply Voltage: 2.8V/1.8V (2.8V for analog, 1.8V for digital)
- Package Type: 48-CLCC/PLCC

PRODUCTS

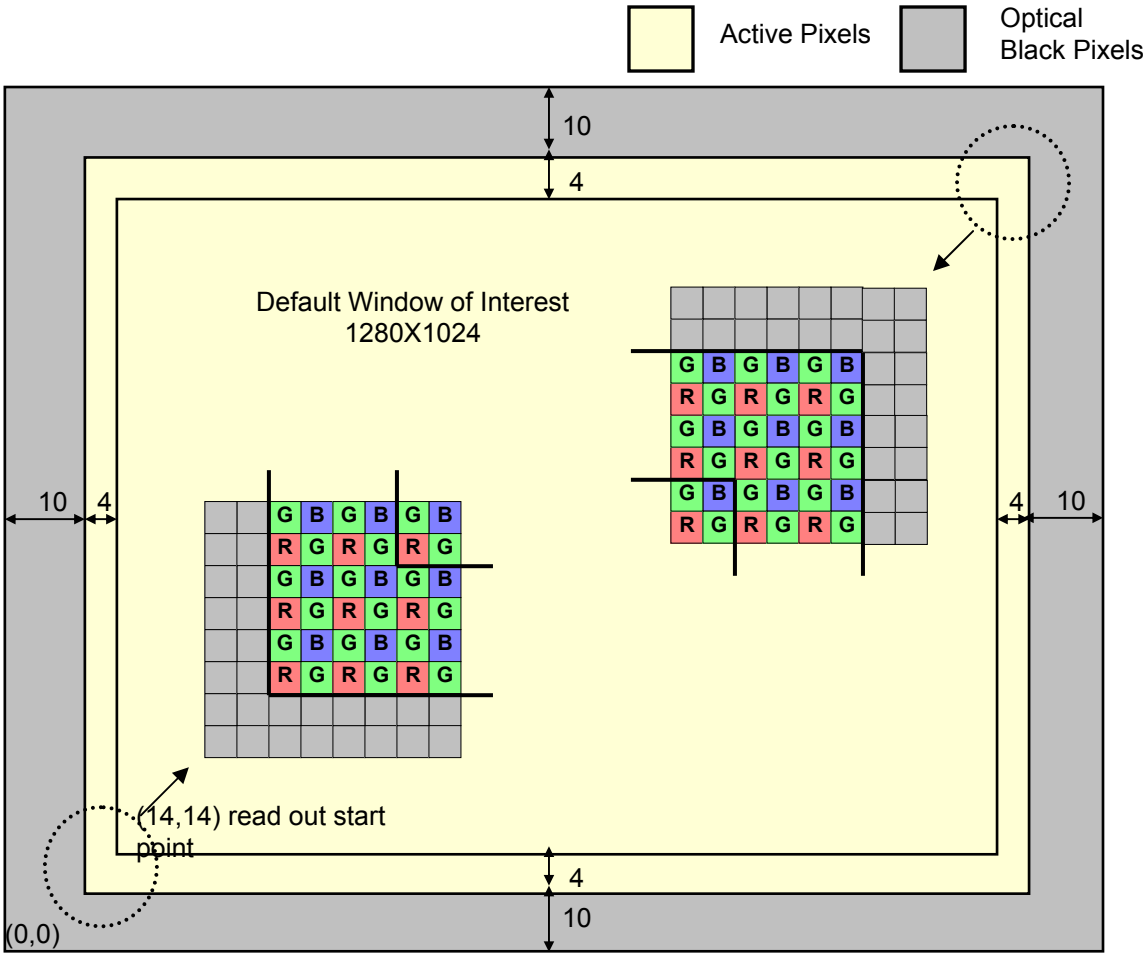
Product Code	Power Supply	Backend Process	Description
S5K3A1EA01	2.8V / 1.8 V	None	Monochrome image sensor
S5K3A1EA02	2.8V / 1.8 V	On-chip micro lens	High sensitivity monochrome Image sensor
S5K3A1EA03	2.8V / 1.8 V	On-chip color filter and micro lens	RGB color image sensor
S5K3A1EA13	2.8V / 1.8 V	On-chip color filter and micro lens	RGB color image sensor

BLOCK DIAGRAM

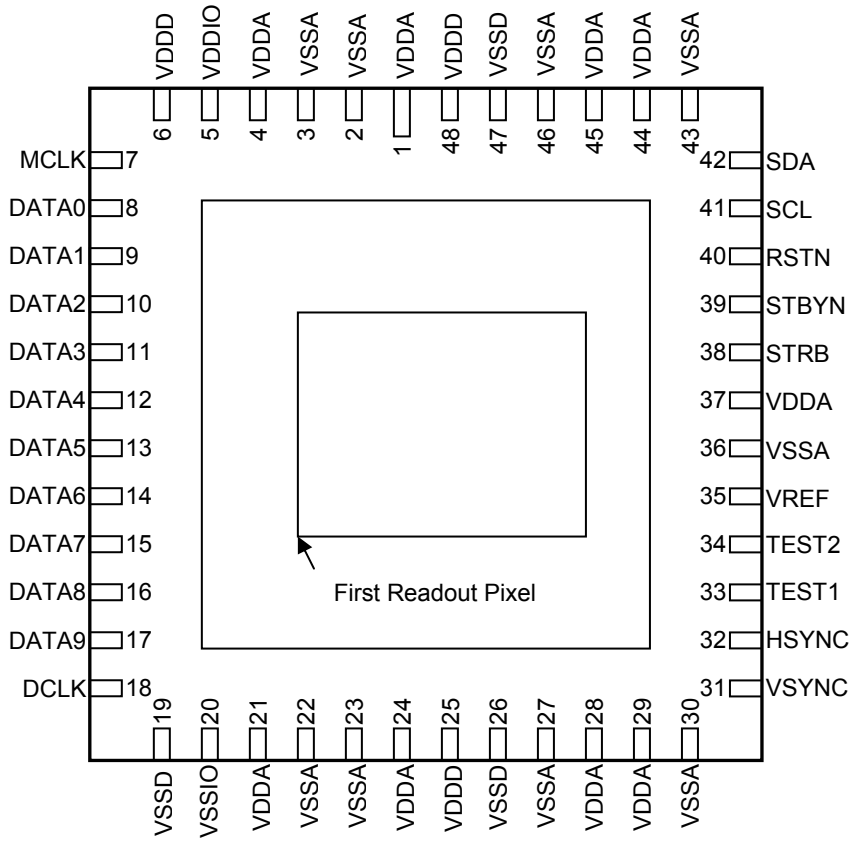


PIXEL ARRAY MAP

(TOP VIEW ON CHIP. DISPLAYED IMAGE WILL BE FLIPPED.)



PIN CONFIGURATION



SAMSUNG ELECTRONICS

MAXIMUM ABSOLUTE RATINGS

Characteristic	Symbol	Value	Unit
Analog maximum absolute voltage (VDDA supply relative to VSSA)	V_{DDH}	-0.3 to 3.8	V
Digital and I/O maximum absolute voltage (VDDIO supply relative to VSSIO VDDD supply relative to VSSD)	V_{DDL}	-0.3 to 2.7	
Input voltage	V_{IN}	-0.3 to 2.7	
Operating temperature	T_{OPR}	-20 to +60	°C
Storage temperature	T_{STG}	-40 to +125(1)	
		-40 to +85(2)	

NOTES:

1. The maximum allowed storage temperature for S5K3A1EA01.
2. The maximum allowed storage temperature for S5K3A1EA02 and S5K3A1EA03.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(T_A = -20 to +60°C, C_L = 15pF)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Operating voltage	V_{DDH}	applied to VDDA pins	2.6	2.8	3.0	V
	V_{DDL}	applied to VDDIO and VDDD pin	1.65	1.8	1.95	
Input voltage(1)	V_{IH}	-	1.27	-	-	
	V_{IL}	-	-	-	0.57	
Input leakage current(2)	I_{IL}	V_{IN} = V_{DDL}	-10	-	10	μA
Input leakage current with pull-down(3)	I_{ILD}	V_{IN} = V_{DDL}	5	18	40	
High level output voltage(4)	V_{OH}	I_{OH} = -1μA	V_{DDL}-0.05	-	-	V
		I_{OH} = -4mA	1.2	-	-	
Low level output voltage(5)	V_{OL}	I_{OL} = 1μA	-	-	0.05	
		I_{OL} = 4mA	-	-	0.45	
High-Z output leakage current(6)	I_{OZ}	V_{OUT} = V_{SS} or V_{DDL}	-10	-	10	μA
Input capacitance(1)	C_{IN}	-	-	-	4	pF
Supply current	I_{STBL}	STBYN=Low(Active) All input clocks = Low 0 lux illumination applied to VDDIO and VDDD pin	-	-	10	μA
	I_{STBH}	STBYN=Low(Active) All input clocks = Low 0 lux illumination applied to VDDA pin	-	-	10	μA
	I_{DDL}	f_{MCLK} = 12MHz 0 lux illumination applied to VDDIO and VDDD pin	-	10	15	mA
	I_{DDH}	f_{MCLK} = 12MHz 0 lux illumination applied to VDDA pin	-	20	25	mA

NOTES:

1. Applied to MCLK, RSTN, STBYN, STRB, SCL, SDA, TEST1, TEST2 pins.
2. Applied to MCLK, RSTN, STBYN, STRB, SCL, SDA pins
3. Applied to TEST1, TEST2 pin
4. Applied to DCLK, HSYNC, VSYNC, DATA0 to DATA9 pin. I_{OH} : High level output current
5. Applied to DCLK, HSYNC, VSYNC, DATA0 to DATA9, SCL, SDA pin. I_{OL} : Low level output current
6. Applied to SDA pin when in High-Z output state

Imaging Characteristics

(Light source with 3200K of color temperature and IR cut filter (CM-500S, 1mm thickness) is used. Electrical operating conditions follow the recommended typical values. The control registers are set to the default values. T_A = 25°C if not specified.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Saturation level(1)	V_{SAT}	-	600	650	-	mV
Sensitivity(2)	S	-	-	1500	-	mV/lux sec
Dark level(3)	V_{DARK}	T_A = 40°C	-	4	8	mV/sec
		T_A = 60°C	-	20	40	
Dynamic range(4)	DR	-	-	60	-	dB
Signal to noise ratio(5)	S/N	-	-	40	-	
Dark signal non-uniformity(6)	DSNU	T_A = 60°C	-	-	40	mV/sec
Photo response non-uniformity(7)	PRNU	-	-	4	8	%
Vertical fixed pattern noise(8)	VFPN	-		4	8	%
Horizontal fixed pattern noise(9)	HFPN	-		4	8	%

NOTES:

1. Measured minimum output level at 100 lux illumination for exposure time 1/30 sec. 7X7 rank filter is applied for the whole pixel area to eliminate the values from defective pixels.
2. Measured average output at 25% of saturation level illumination for exposure time 1/30 sec. Green channel output values are used for color version.
3. Measured average output at zero illumination without any offset compensation for exposure time 1/30 sec.
4. 20 log (saturation level/ dark level RMS noise excluding fixed pattern noise). 60dB is limited by 10-bit ADC.
5. 20 log (average output level / RMS noise excluding fixed pattern noise) at 25% of saturation level illumination for exposure time 1/30 sec.
6. Difference between maximum and minimum pixel output levels at zero illumination for exposure time 1/30 sec. 7X7 median filter is applied for the whole pixel area to eliminate the values from defective pixels.
7, Difference between maximum and minimum pixel output levels divided by average output level at 25% of saturation level illumination for exposure time 1/30 sec. 7X7 median filter is applied for the whole pixel area to eliminate the values from defective pixels.
8. For the column-averaged pixel output values, maximum relative deviation of values from 7-depth median filtered values for neighboring 7 columns at 25% of saturation level illumination for exposure time 1/30 sec.
9. For the row-averaged pixel output values, maximum relative deviation of values from 7-depth median filtered values for neighboring 7 rows at 25% of saturation level illumination for exposure time 1/30 sec.

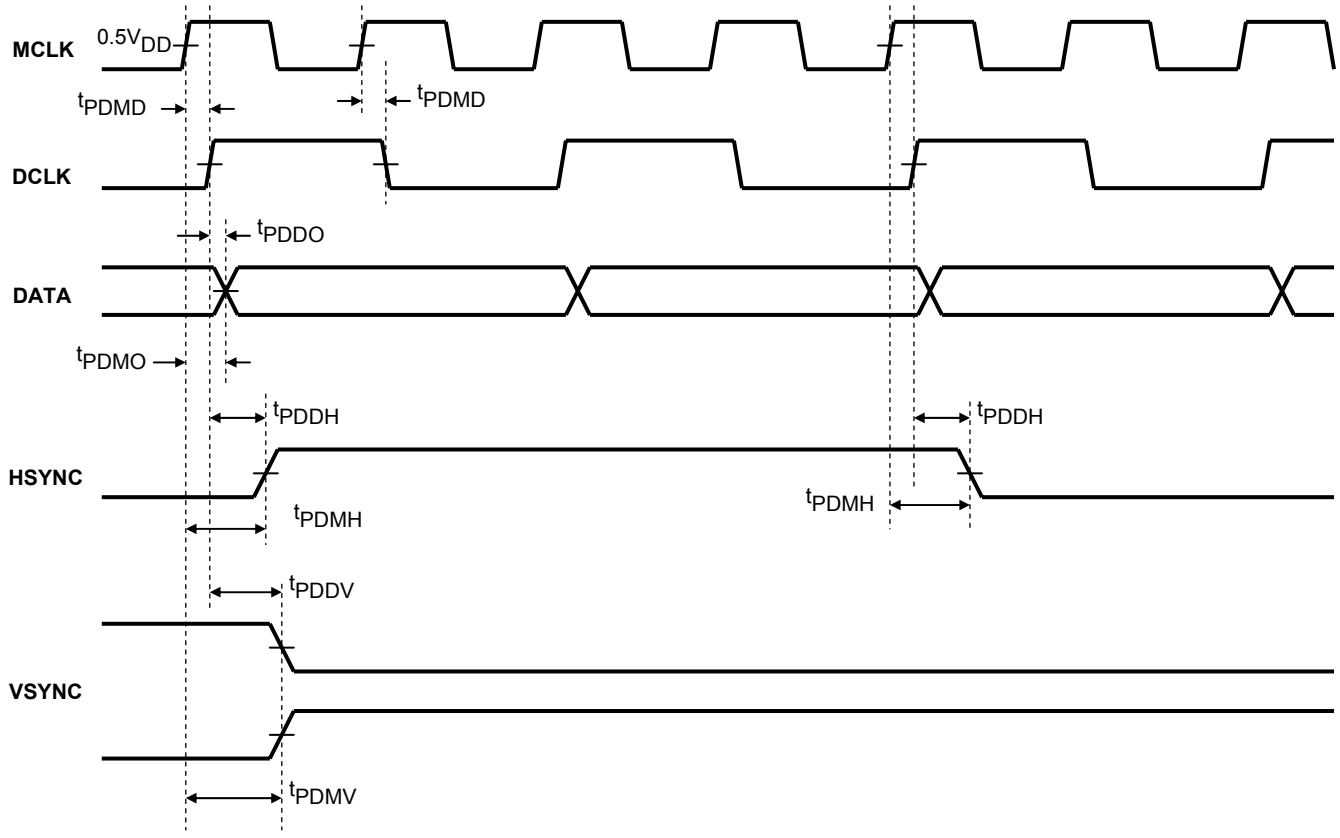
AC Characteristics

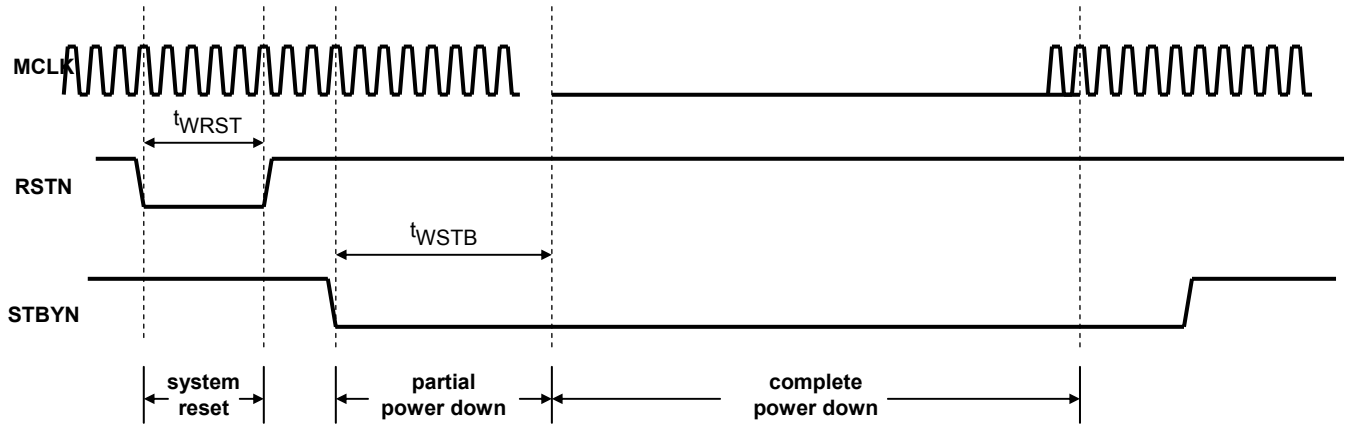
(V_{DDH} = 2.8V ± 0.25V, V_{DDL} = 1.8V ± 0.15V, T_A = -20 to + 60 °C, C_L = 10pF)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Main input clock frequency	f_{MCLK}	Duty = 50%	6	12	48	MHz
Data output clock frequency	f_{DCLK}	-	6	12	30	
Propagation delay time from main input clock	t_{PDMV}	VSYNC output	-	-	10	ns
	t_{PDMH}	HSYNC output	-	-	10	
	t_{PDMD}	DCLK output	-	-	6	
	t_{PDMO}	DATA output	-	-	10	
Propagation delay time from data output clock	t_{PDDV}	VSYNC output	-	-	4	
	t_{PDDH}	HSYNC output	-	-	4	
	t_{PDDO}	DATA output	-	-	4	
Reset input pulse width	t_{WRST}	RSTN=low(active)	5	-	-	T_{MCLK}(1)
Standby input pulse width	t_{WSTB}	STBYN=low(active)	4	-	-	

NOTES:

1. T_{MCLK} is the period of the master input clock, MCLK.



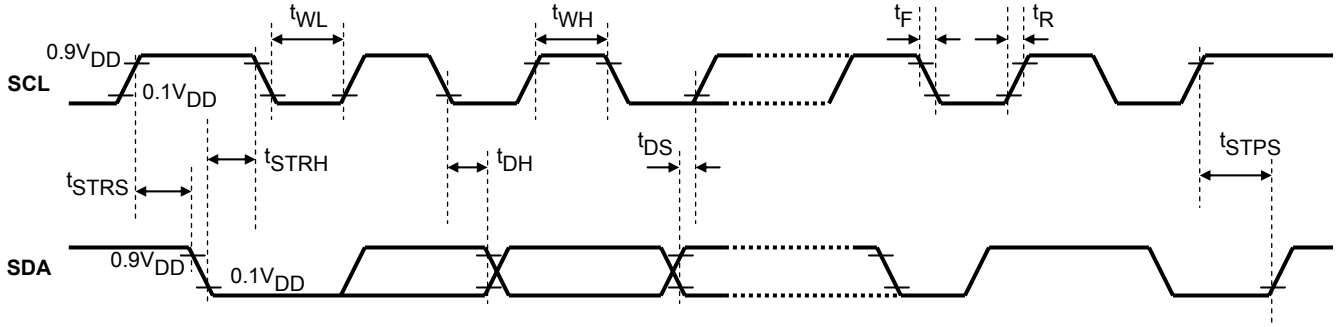


I²C Serial Interface Characteristics (1)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Clock frequency	f_{SCL}	-	-	-	400	kHz
Clock high pulse width	t_{WH}	SCL	0.6	-	-	µs
Clock low pulse width	t_{WL}	SCL	1.3	-	-	
Clock rise/fall time	t_R/t_F	SCL, SDA	-	-	0.3	
Data set-up time	t_{DS}	SDA to SCL	0.1	-	-	
Data hold time	t_{DH}	SCL to SDA	-	-	0.9	
START condition setup time	t_{STRS}	-	4			T_{MCLK}(2)
START condition hold time	t_{STRH}	-	4			
STOP condition setup time	t_{STPS}	-	4	-	-	
STOP to new START gap	t_{GSS}	-	8	-	-	
Capacitance for each pin	C_{PIN}	SCL, SDA	-	-	4	pF
Capacitive bus load	C_{BUS}	SCL, SDA	-	-	200	
Pull-up resistor	R_{PU}	SCL, SDA to V_{DD}	1.5	-	10	kΩ

NOTES:

1. I²C is a proprietary Phillips interface bus.
2. T_{MCLK} is the period of the master input clock, MCLK.



SAMSUNG ELECTRONICS

PIN DESCRIPTION

Pin No	I/O	Name	Function
VDDD (6,25,48)	Power	Digital power supply	For logical circuit (V_{DDL})
VDDIO (5)	Power		For I/O circuit (V_{DDL})
VSSD (19,26,47)	Power		0V (GND)
VSSIO (20)	Power		0V (GND)
VDDA(1,4,21,24, 28,29,37,44,45)	Power	Analog power supply	For analog circuit (V_{DDH})
VSSA(2,3,22,23, 27,30,36,43,46)	Power		0V (GND)
MCLK (7)	I	Master clock	Master clock pulse input for all timing generators.
RSTN (40)	I	Reset	Initializing all the device registers. (Active low)
STBYN (39)	I	Standby	Activating power saving mode. (high=normal operation, low=power saving mode)
STRB (38)	I	Strobe	Triggering the integration start and stop when single frame capture mode.
DATA0~DATA9 (8 ~ 17)	O	Image data output	10-bit image data outputs. When ADC resolution is reduced, the unused lower bits are set to 0.
DCLK (18)	O	Data clock	Image data output synchronizing pulse output.
HSYNC (32)	O	Horizontal sync clock	Horizontal synchronizing pulse or data valid signal output.
VSYNC (31)	O	Vertical sync clock	Vertical synchronizing pulse or line valid signal output.
SCL (41)	I	Serial interface clock	I2C serial interface clock input
SDA (42)	I/O	Serial interface data	I2C serial interface data bus (external pull-up resistor required)
VREF (35)	I/O	Reference voltage	For proper operation, the external capacitor larger than 0.1uF must be connected between VREF and VDDA.
TEST1 (33)	I	Test input 1	Test input signal. Though it can be opened in normal operation (internally pulled down), it is recommended to ground the test pins.
TEST2 (34)	I	Test input 2	Test input signal. Though it can be opened in normal operation (internally pulled down), it is recommended to ground the test pins.

CONTROL REGISTERS

Address (Hex)	Reset Value	Bits	Mnemonic	Description
00h	01h	[7]	**p2_r_con**	(Factory use only) CDS timing control
		[6]	**bprm**	Bad pixel replacement mode 0b: disabled (default), 1b: enabled
		[5]	**ccsm**	Color channel separation mode 0b: not separated (default), 1b: separated
		[4:2]	**mcdiv**	Main clock divider 000b: DCLK=MCLK(default), 001b: DCLK=MCLK÷2 010b: DCLK=MCLK÷4, 011b: DCLK=MCLK÷8 100b: DCLK=MCLK÷16, 101b: DCLK=MCLK÷32 111b: forbidden value
		[1]	**shutc**	Electronic shutter mode 0b: disabled (default), 1b: enabled
		[0]	**adcres**	ADC resolution 0b: 8-bit, 1b: 10-bit (default)
01h	00h	[7]	**shut_err_cor**	Shutter error correction register
		[6]	**Not_use**	
		[5]	**mircv**	Vertical mirror control 0b: normal (default), 1b: mirrored
		[4]	**mirch**	Horizontal mirror control 0b: normal (default), 1b: mirrored
		[3:2]	**subsr**	Row sub-sampling mode 00b: disabled (default), 01b: 2X, 10b: 4X, 11b: 8X
		[1:0]	**subsc**	Column sub-sampling mode 00b: disabled (default), 01b: 2X, 10b: 4X, 11b: 8X
02h	00h	[2:0]	**wrp_high**	Row start point for window of interest wrp[10:0] = 14d(default)
03h	0Eh	[7:0]	**wrp_low**	
04h	00h	[2:0]	**wcp_high**	Column start point for window of interest wcp[10:0] = 14d(default)
05h	0Eh	[7:0]	**wcp_low**	
06h	04h	[2:0]	**wrd_high**	Row depth for window of interest wrd[10:0] = 1024d(default)
07h	00h	[7:0]	**wrd_low**	
08h	05h	[2:0]	**wcw_high**	Column width for window of interest wcw[10:0] = 1280d(default)
09h	00h	[7:0]	**wcw_low**	
0Ah	80h	[7:0]	**offsdef**	(Factory use only) Analog offset reference offsdef[7:0] = 128d (default)

Address (Hex)	Reset Value	Bits	Mnemonic	Description
0Bh	04h	[7:0]	**sint_high**	Integration time in single frame capture mode sint[15:0] = 1125d (default)
0Ch	65h	[7:0]	**sint_low**	
0Dh	04h	[7:0]	**cintr_high**	Row-step integration time in continuous frame capture mode cintr[15:0] = 1125d (default)
0Eh	65h	[7:0]	**cintr_low**	
0Fh	00h	[7:0]	**cintc_high**	Column-step integration time in continuous frame capture mode cintc[15:0] = 0d (default)
10h	00h	[7:0]	**cintc_low**	
11h	00h	[7]	**hspolar**	HSYNC polarity 0: active high (default), 1: active low
		[6]	**hsdisp**	HSYNC display mode 0: sync mode (default), 1: data valid mode
		[5]	**vspolar**	VSYNC polarity 0: active high (default), 1: active low
		[4]	**vsdisp**	VSYNC display mode 0: sync mode (default), 1: data valid mode
		[3]	**global_mod**	Single frame capture integration mode Field shift shutter mode
		[2]	**roll_mod**	Single frame capture integration mode Rolling shutter mode
		[1]	**mech_mod**	Single frame capture integration mode simultaneous frame integration with mechanical shutter
		[0]	**sfcen**	Single frame capture mode enable 0b: disabled (default), 1b: enabled
12h	01h	[7:0]	**vswd**	VSYNC width vswd[7:0] = 1d (default)
13h	00h	[7:0]	**vsstrt_high**	VSYNC start position vsstrt[9:0] = 0d (default)
14h	00h	[7:0]	**vsstrt_low**	
15h	00h	[7:0]	**vblank_high**	Vertical blank depth vblank[12:0] = 101d (default)
16h	65h	[7:0]	**vblank_low**	
17h	20h	[7:0]	**hswd**	HSYNC width hswd[7:0] = 32d (default)
18h	00h	[7:0]	**hsstrt_high**	HSYNC start position hsstrt[9:0] = 0d (default)
19h	00h	[7:0]	**hsstrt_high**	
1Ah	00h	[7:0]	**hblank_high**	Horizontal blank depth hblank[15:0] = 142d (default)
1Bh	8Eh	[7:0]	**hblank_low**	

Address (Hex)	Reset Value	Bits	Mnemonic	Description
1Ch	00h	[6:0]	**pgcr**	Red channel gain pgcr[6:0] = 0d (default)
1Dh	00h	[6:0]	**pgcg1**	Green(Red row) channel gain or all channel gain (**ccsm**=0) pgcg1[6:0] = 0d (default)
1Eh	00h	[6:0]	**pgcg2**	Green(Blue row) channel gain pgcg2[6:0] = 0d (default)
1Fh	00h	[6:0]	**pgcb**	Blue channel gain pgcb[6:0] = 0d (default)
20h	0Fh	[4:0]	**sgg1**	1st quadrisectional global gain sgg1[4:0] = 0F(default)
21h	0Fh	[4:0]	**sgg2**	2nd quadrisectional global gain sgg2[4:0] = 0F(default)
22h	0Fh	[4:0]	**sgg3**	3rd quadrisectional global gain sgg3[4:0] = 0F(default)
23h	0Fh	[4:0]	**sgg4**	4th quadrisectional global gain sgg4[4:0] = 0F(default)
24h	80h	[7:0]	**offsr**	Red channel analog offset Offsr[7:0] = 128 (default)
25h	80h	[7:0]	**offsg1**	Green(Red row) channel analog offset or all channel offset (**ccsm**=0) offsg1[7:0] = 128 (default)
26h	80h	[7:0]	**offsg2**	Green(Blue row) channel analog offset offsg2[7:0] = 128 (default)
27h	80h	[7:0]	**offsb**	Blue channel analog offset offsb[7:0] = 128 (default)
28h	14h	[7]	**clipen**	(Factory use only) Reset clipping enable
		[6:0]	**pthresh**	Bad pixel threshold pthresh[6:0] = 20d (default)
29h	00h	[7:0]	**adcoffs**	ADC offset (count delay register) adcoffs[7:0] = 0d (default) ADLC formula : D_{final} = D(n) + adcoffs When adcoffs[7] is 1 , adc offset is +adcoffs[6:0], else adc offset is - adcoffs[6:0]

Address (Hex)	Reset Value	Bits	Mnemonic	Description
2Ah	40h	[7:5]	**stbystrt**	(Factory use only) Stand-by start
		[4:0]	**stbystp**	(Factory use only) Stand-by stop
2Bh	00h	[7:0]	**rxstrt**	(Factory use only) Reset start control
2Ch	00h	[7:0]	**blank**	Blank register for general purpose
2Dh	02h	[7:6]	**Not_use**	
		[5]	**id_inv**	(Factory use only) Line color inversion
		[4]	**sck_inv**	(Factory use only) Column color inversion
		[3:2]	**Not_use**	
		[1]	**i2ctest**	(Factory use only) IIC test mode
		[0]	**nandtree**	(Factory use only) NAND tree test mode
2Eh	06h	[7]	**adlc_mod_d**	Adlc mode always enable when this register is high. 0b: disabled (default), 1b: enabled
		[6]	**adlc_mod_c**	Adlc mode works when gain values are changed 0b: disabled (default), 1b: enabled
		[5]	**adlc_mod_b**	Adlc mode works when shutter values are changed 0b: disabled (default), 1b: enabled
		[4]	**adlc_mod_a**	Adlc mode works till adlc length value 0b: disabled (default), 1b: enabled
		[3:2]	**feedback_gain_B**	Feedback gain value about ADLC 00b : 0, 01b : 0.5(default), 10b : 0.75, 11b : 1 ADLC formula : D_{final} = D(n) + adcoffs D(n) = A*(OB(n) + OB(n-1)) + B*D(n-1)
		[1:0]	**feedback_gain_A**	Feedback gain value about ADLC 00b : 0, 01b : 0.5, 10b : 0.25(default), 11b : 0.125

Address (Hex)	Reset Value	Bits	Mnemonic	Description
2Fh	00h	[7]	**dckout_en**	DCK pad control 0b : output enable (default), 1b : stable value
		[6]	**dfo**	I/O driver fan-out control register.
		[5]	**fixvs**	VSYNC always high at frame start point. 0b: disabled (default), 1b: enabled
		[4]	**isp_sel**	(Factory use only)
		[3]	**ob_sel**	ADLC formula : D = D(n) + adcoff D(n) = A*(OB(n) + OB(n-1)) + B*D(n-1) 0b : OB(n-1) = OB(n-1) (default) 1b : OB(n-1) = OB(n)
		[2]	**ob_area**	OB area selection 0b:128*8 (default), 1b:512*2 (recommended)
		[1:0]	**adlc_length**	ADLC function works only during this value when adlc_mod_a enabled, 00b : 1 frame, 01b : 2 frames, 10b : 3 frames, 11b : 4 frames
30h	02h	[7:6]	**Not_use**	
		[5]	**pwr_save2**	(Factory use only) rx & tx signals are enable only active area. 0b: disabled (default), 1b: enabled
		[4]	**pwr_save1**	(Factory use only) 0b: disabled (default), 1b: enabled
		[3]	**ggo_en**	(Factory use only) 0b: disabled (default), 1b: enabled
		[2]	**rsm_en**	(Factory use only)When this register is zero, H-sync keeps same period in one frame.
		[1]	**gbmod**	Guardband mode 0b: disabled, 1b: enabled(default)
		[0]	**stpless_mod**	Stepless mode enable 0b: disabled (default), 1b: enabled
31h	1Eh	[7:0]	**gb_start**	Guardband start position
32h	32h	[7:0]	**gb_end**	Guardband end position
33h	00h	[5:0]	**vs_postc_high**	Keep the same frame in zoom mode. This register compensates remainder of frame.
34h	00h	[7:0]	**vs_postc_low**	
35h	CCh	[7:4]	**p12_stp**	(Factory use only) CDS timing control
		[3:0]	**p11_stp**	(Factory use only) CDS timing control
36h	CCh	[7:4]	**p2r_stp**	(Factory use only) CDS timing control
		[3:0]	**p2_stp**	(Factory use only) CDS timing control

Address (Hex)	Reset Value	Bits	Mnemonic	Description
37h	00h	[7:0]	**holdline_high**	Active output delay about its register value
38h	00h	[7:0]	**holdline_low**	
39h	0Ah	[7:0]	**vsend_ofset-high**	This register value is must larger than OB line.
3Ah	1Ah	[7]	**Not use**	
		[6]	**tx_add**	(Factory use only)Add tg to reduce NIT.
		[5]	**shutx_sel**	(Factory use only)Enlarge shutter TX width to reduce NIT.
		[4]	**cal_en**	(Factory use only) calibration enable
		[3:0]	**cal_stp**	(Factory use only) calibration signal control

OPERATION DESCRIPTION

1. Output Data Format

1-1. Main Clock Divider

All the data output and sync signals are synchronized to data clock output (**DCLK**). It is generated by dividing the input main clock (**MCLK**). The dividing ratio is 1, 2, 4, 8, 16, and 32 according to main clock dividing control register (**mcdiv**). For 10-bit ADC and SXGA resolution, dividing ratio of 1 is required. If dividing ratio of 1 is used, the duty must be within 40% to 60%.

1-2. Synchronous Signal Output

The horizontal sync(**HSYNC**) and vertical sync(**VSYNC**) signals are also available. The sync pulse width, polarity and position are programmable by control registers (ref. timing chart). When display mode is enabled, the sync signal outputs indicate that the output data is valid (**hsdisp**=1) or the output rows are valid (**vsdisp**=1).

1-3. Window of Interest Control

Window of Interest (WOI) is defined as the pixel address range to be read out. The WOI can be assigned anywhere on the pixel array. It is composed of four values: row start pointer(**wrp**), column start pointer(**wcp**), row depth(**wrd**) and column width(**wcw**). Each value can be programmed by control registers. For convenience of color signal processing, **wcp** is truncated to even numbers so that the starting data of each line is the red and green column of Bayer pattern. Figure 1 refers to a pictorial representation of the WOI on the displayed pixel image.

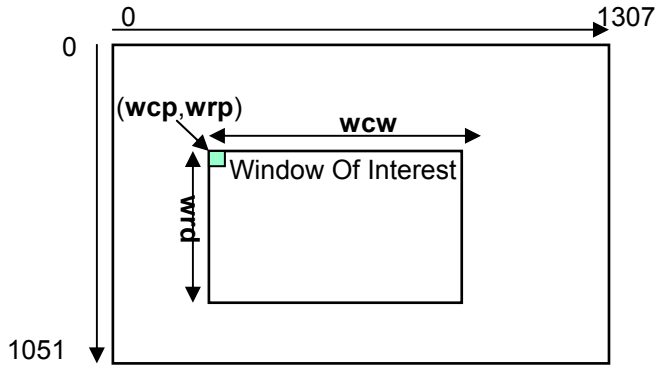


Figure 1. WOI definition.

1-4. Vertical Mirror and Horizontal Mirror Mode Control

The pixel data are read out from left to right in horizontal direction and from top to bottom in vertical direction normally. By changing the mirror mode, the read-out sequence can be reversed and the resulting image can be flipped like a mirror image. Pixel data are read out from right to left in horizontal mirror mode and from bottom to top in vertical mirror mode. The horizontal and the vertical mirror mode can be programmed by Horizontal Mirror Control Register (**mirch**) and Vertical Mirror Control Register (**mircv**).

1-5. Sub-sampling Control

The user can read out the pixel data in sub-sampling rate in both horizontal and vertical direction. Sub-sampling can be done in four rates : full, 1/2, 1/4 and 1/8. The user controls the sub-sampling using the Sub-sampling

Control Registers, **subsr** and **subsc**. The sub-sampling is performed only in the Bayer space. In Figure 2, the Bayer space sub-sampling examples are shown.

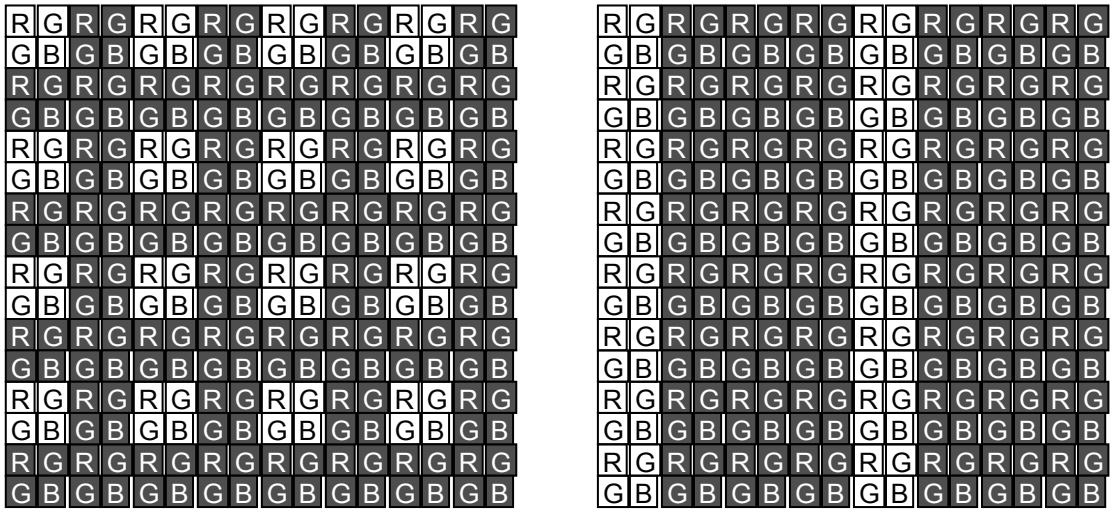


Figure 2. Bayer Space Sub-Sampling Examples

1-6. Line Rate and Frame Rate Control (Virtual Frame)

The line rate and the frame rate can be changed by varying the size of virtual frame. The virtual frame's width and depth are controlled by effective WOI and blank depths. The effective WOI is scaled by the subsampling factors from WOI set by register values. For CDS and ADC function, the virtual column width must be larger than (**adcres**+1)*256/(2^**mcdiv**)+264, where **adcres** is the ADC resolution control register value. The horizontal and vertical blanking time (**hblank**, **vblank**) should be over 60 and 4, respectively. The detailed restriction of h-blank period is shown in table 1.

Table 1. Restriction of h-blank period (minimum 1H-period(dck)

	minimum 1H-period(dck)	
mcdiv[2:0]	adcres = 1	adcres = 0
0	1412	548
1	836	404
2	548	332
3	404	300
4	332	278
5	300	270

Setting procedure of hblank, vblank and vs_postc is as follows.

Frame cycle = ((wcw>>subsc) + hblank) x ((wrd>>subsr) + vblank) + vs_postc

vblank >= 4 (isp_sel=1)

vs_postc < 1H ((wcw>>subsc) + hblank))

1-7. Continuous Frame Capture Mode(CFCM) Integration Time Control (Electronic Shutter Control)

In CFCM operation, the integration time is controlled by shutter operation. The shutter operation is done when shutter control register (**shutc**) is set to "1". In shutter operation, the integration time is determined by the Row Step Integration Time Control Register(**cintr**) and Column Step Integration Time Control Register(**cintc**)

In CFCM integration time control. There are two different modes. One is normal shutter mode. The other is shutter TX wide mode to reduce nonlinear integration time. The effective integration time(EIT) formulas of each mode are as follows.

1) normal mode (00h[2] = 1, 01h[7] = 1, 3Ah[5] = 1)
EIT = (cintr - 1) x ((wcw>>subsc) + hblank) + cintc + 145 (dck)
restriction of cintr?
1 <= cintr <= (wrd>>subsr) + vblankr –1
restriction of cintc?
0 <= cintc <= (wcw>>subsc) + hblank - 7

2) shutter TX wide mode (00h[2] = 1, 01h[7] = 0, 3Ah[5] = 1)
EIT = (cintr - 1) x ((wcw>>subsc) + hblank) + cintc + 145 (dck)
restriction of cintr?
1 <= cintr <= (wrd>>subsr) + vblankr - 1
restriction of cintr?
case of (1 <= cintr <= (wrd>>subsr) + vblankr - 2)
0 <= cintc <= (wcw>>subsc) + hblank - 7
case of (cintr = (wrd>>subsr) + vblankr - 1)
0 <= cintc <= (wcw>>subsc) + hblank - 195

1-8. Single Frame Capture Mode(SFCM) Integration Time Control

To capture a still image, SFCM can be set by Single Frame Capture Enable Register(**sfcen**). There are two types of integration mode implemented. In the rolling shutter mode (**sfcim**=0), the integration time is controlled by SFCM Integration Time Register (**sint**). The light integration period for each rows progresses with reading rows. The integration time is expressed as :

Integration Time = **sint** * (1 line time)

In the mechanical shutter mode (**sfcim**=1), the integration time for all rows is the period during the external input signal, **STRB** is active. After **STRB** goes to be inactive, the external mechanical shutter should shut off incident lignt on image sensor and the data readout sequence starts.

2. Analog to Digital Converter (ADC)

The image sensor has on-chip ADC. Two-channel column parallel ADC scheme is used for separated color channel gain and offset control.

2-1. ADC resolution

The default value of ADC resolution is 10bit and can be changed to 8bit or 9bit by control the ADC Resolution Control Register (**adcres**). Lowering ADC resolution reduces the required minimum line time. When the number of effective output bits is reduced, upper n-bits of output ports are valid and lower bits always have values of "0".

2-2. Correlated Double Sampling (CDS)

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action

and some fixed pattern noise by the in-pixel amplifier offset deviation. To eliminate those noise components, a correlated double sampling(CDS) circuit is used before converting to digital. The output signal of each pixel is sampled twice, once for the reset level and once for the actual signal level.

2-3. Programmable Gain and Offset Control

The user can controls the gain of individual color channel by the Programmable Gain Control Registers (**pgcr**, **pgcg1**, **pgcg2**, **pgcb**) and offset by Offset Control Registers (**offsr**, **offsg1**, **offsg2**, **offsb**). If the Color Channel Separation Mode is disabled (**ccsm**=0), **pgcg1** and **offsg1** change the gains and offsets for all channels. As increasing the gain control register, the ADC conversion input range decreases and the gain increases as following equation and the relative channel gain is shown in figure 3

R	G1	R	G1
G2	B	G2	B
R	G1	R	G1
G2	B	G2	B

Channel Gain = 128 / (128 – Programmable Gain Control Register Value[6:0])

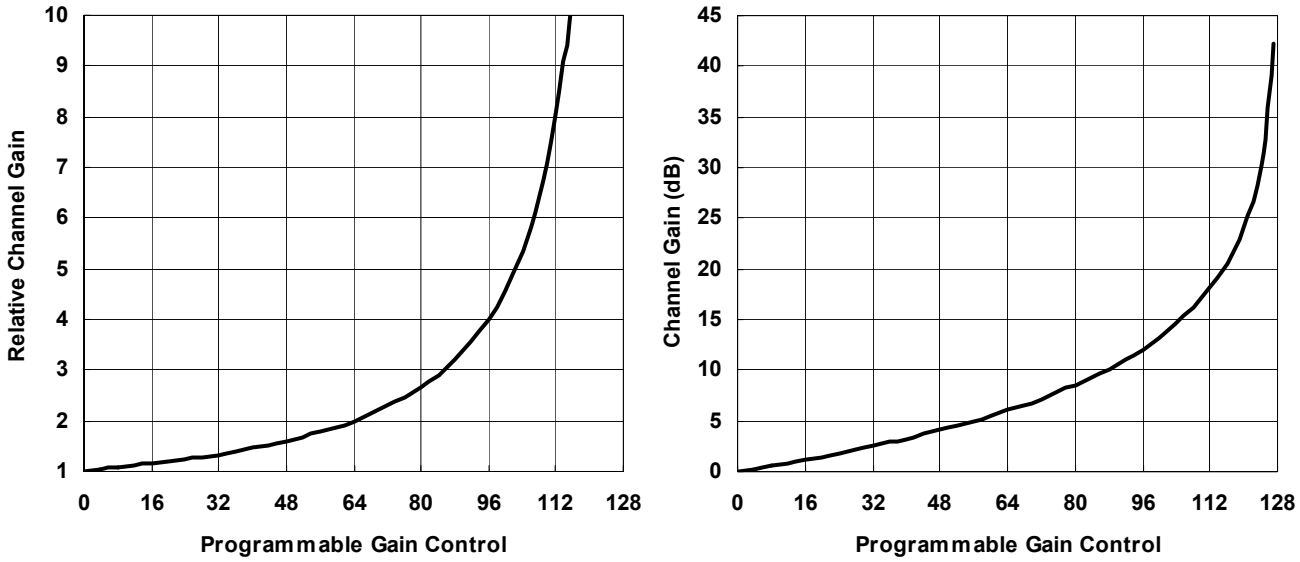


Figure 3. Relative Channel Gain

2-4. Quadrisectional Global Gain Control

The user can controls the global gain to change the gain for all color channels by the Global Gain Control Registers (**sgg1**, **sgg2**, **sgg3**, **sgg4**). The global gain control register is composed of four register groups and each register value decides the gain for each quarter section of output code level. At MCLK=12MHz and ggo_en=L, the global gain is determined by the following formula.

Global Gain = (**sgg**[4:0]+1) / 16

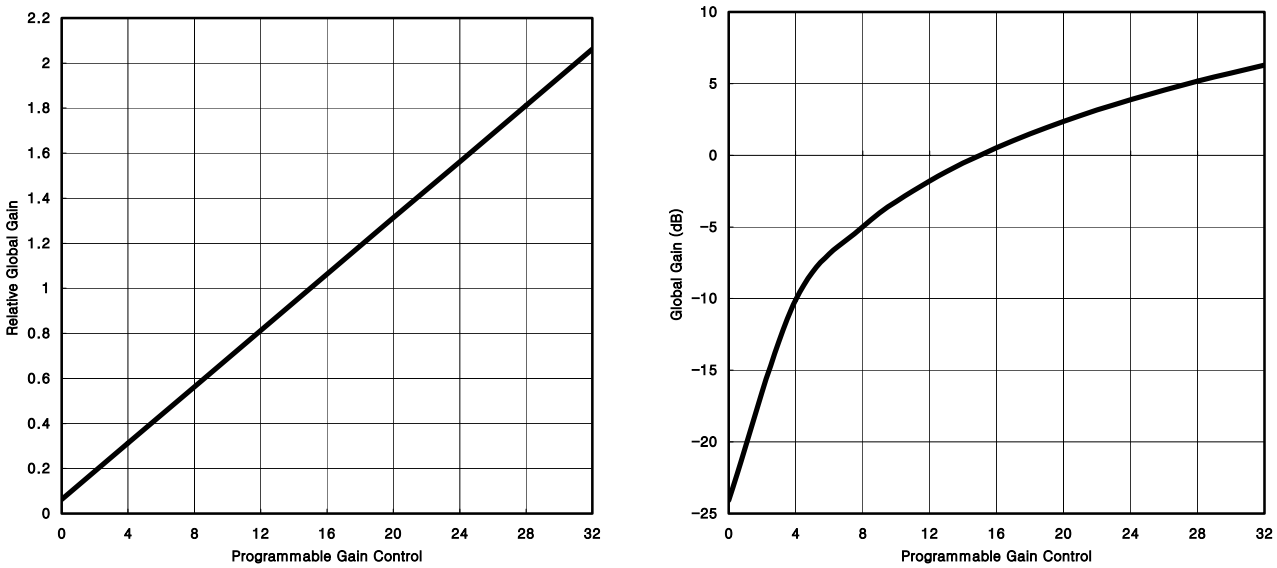


Figure 4. Relative Global Gain

The ADC gain is dependent on **MCLK** frequency (not on **DCLK** frequency) and ADC resolution. The default global gain is set for typical **MCLK** frequency (12MHz) and 10-bit ADC. When the frequency and ADC resolution is changed, the global gain should be changed to maintain the resulting gain over unity for assuring appropriate ADC conversion range. The recommended minimum global gain setting depending on **ggo_en** and **adcres** is shown in figure 5 and table 2.

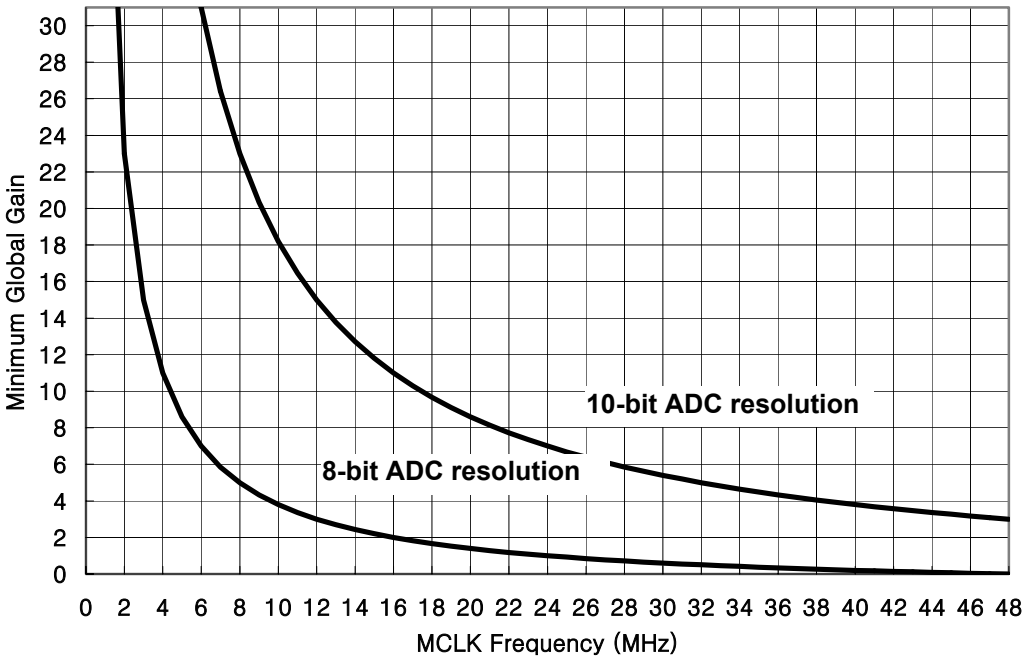


Figure 5. Recommended Minimum Global Gain Control Value (ggo_en = L)

Table 2. Recommended Minimum Global Gain Setting (adcres = H)

MCLK [MHz]	**ggo_en** = L		**ggo_en**=H	
	Decimal	Hexadecimal	Decimal	Hexadecimal
6	31	1F	-	-
7	27	1B	-	-
8	23	17	-	-
9	21	15	-	-
10	19	13	-	-
11	17	11	-	-
12	15	0F	31	1F
13	14	0E	29	1D
14	13	0D	27	1B
15	12	0C	25	19
16	11	0B	23	17
17	11	0B	22	16
18	10	0A	21	15
19	10	0A	20	14
20	9	09	19	13
21	9	09	18	12
22	8	08	17	11
23	8	08	16	10
24	7	07	15	0F
25	7	07	15	0F
26	7	07	14	0E
27	7	07	14	0E
28	6	06	13	0D
29	6	06	13	0D
30	6	06	13	0C
30	6	06	13	0D
31	6	06	12	0C
32	5	05	11	0B
33	5	05	11	0B
34	5	05	11	0B
35	5	05	10	0A
36	5	05	10	0A
37	5	05	10	0A
38	5	05	10	0A
39	4	04	9	09

40	4	04	9	09
41	4	04	9	09
42	4	04	9	09
43	4	04	8	08
44	4	04	8	08
45	4	04	8	08
46	4	04	8	08
47	4	04	8	08
48	3	03	7	07

By appropriately programming these four register values, the different output resolution according to the signal can be achieved and the intra-scene dynamic range can be increased by 16 times. In another application, the sectional global gain control can be used as a rough gamma correction with four sectional linear approximation curve as shown in Figure 6.

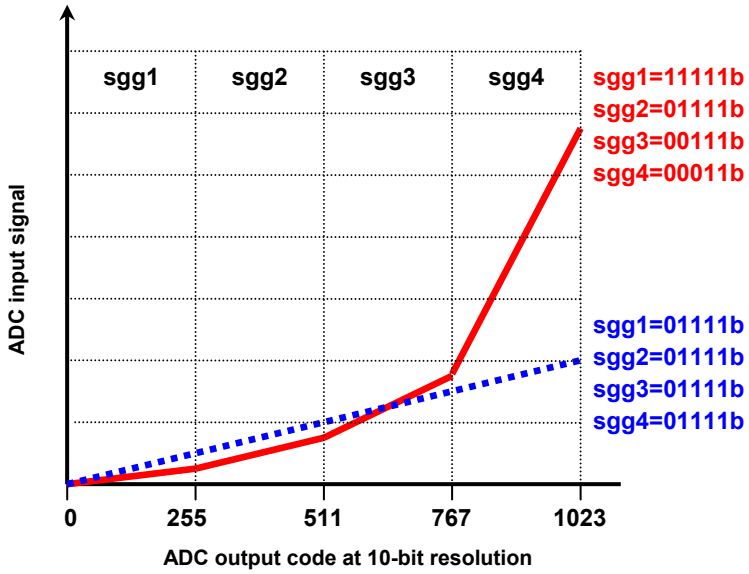


Figure 6. Quadrisectional Glabal Gain Control

3. Post Processing

3-1. Dark Level Compensation

The dark level of Image sensor is defined as average output level without illumination. It includes pixel ouput caused by leakage current of the photodiodes and ADC offset. To compensate the dark level, the output level of optical black(OB) pixels can be a good reference value. When Auto Dark Level Compensation Register (**dlcm**) is set, the image sensor detects the OB pixel level at the start of every frame and anglog-to-digital conversion range is shifted to compensate the dark level for that frame. So, the resulting output data of that frame will be almost zero under dark state. If user wants the dark level which is not zero, the ADC Offset Register (**adcoffs**) can be used. The lower 7-bit value represent the offset value in outout code for compensation and the MSB is the sign to define whether the offset is positive (**adcoffs**[7]=0) or negative (**adcoffs**[7]=1). When not in auto dark level compensation mode, the **adcoffs**[7:0] act as a output code value to subtract the output image data. Please notify that the all the 8-bit data are used for an offset value without sign bit.

ADLC formula : $D_{final} = D(n) + adcoffs$

$D(n) = (feed\_gain\_a)*(OB(n) + OB(n-1)) + (feed\_gain\_b)*D(n-1)$

3-2. Bad Pixel Replacement

When the Bad Pixel Replacement Register (**bprm**) is enabled, the image sensor check that the image data is less or greater than horizontally neighboring pixels in same color channel by the preset threshold value (**pthresh**). If satisfied, the output of the pixel is replaced by the averaged value of the neighboring two pixels. The detectable defected pixels are rare and the bad pixel replacement action can remove defected image effectively. But it reduces the line resolution in horizontal direction.

4. I^2C Serial Interface

The I^2C is an industry standard serial interface. The I^2C contains a serial two-wire half duplex interface that features bi-directional operation, master or slave mode. The general **SDA** and **SCL** are the bi-directional data and clock pins, respectively. These pins are open-drain type ports and will require a pull-up resistor to VDD. The image sensor operates in salve mode only and the **SCL** is input only. The I^2C bus interface is composed of following parts : START signal, 7-bit slave device address (0010001b) transmission followed by a read/write bit, an acknowledgement signal from the slave, 8-bit data transfer followed by an acknowledgement signal and STOP signal. The **SDA** bus line may only be changed while **SCL** is low. The data on the **SDA** bus line is valid on the high-to-low transition of **SCL**.

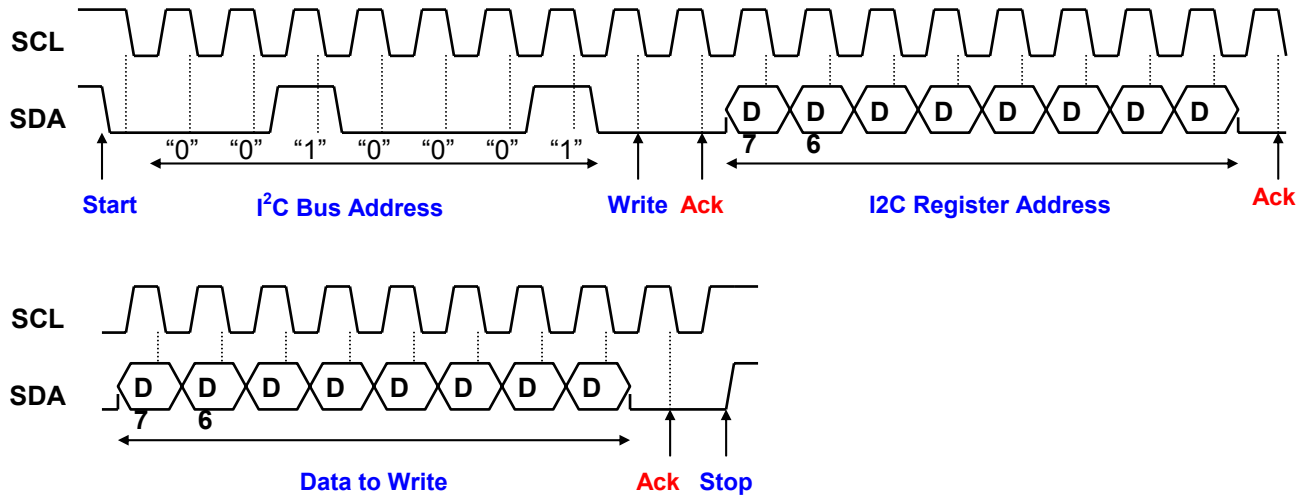


Figure 7. I²C Bus Write Cycle

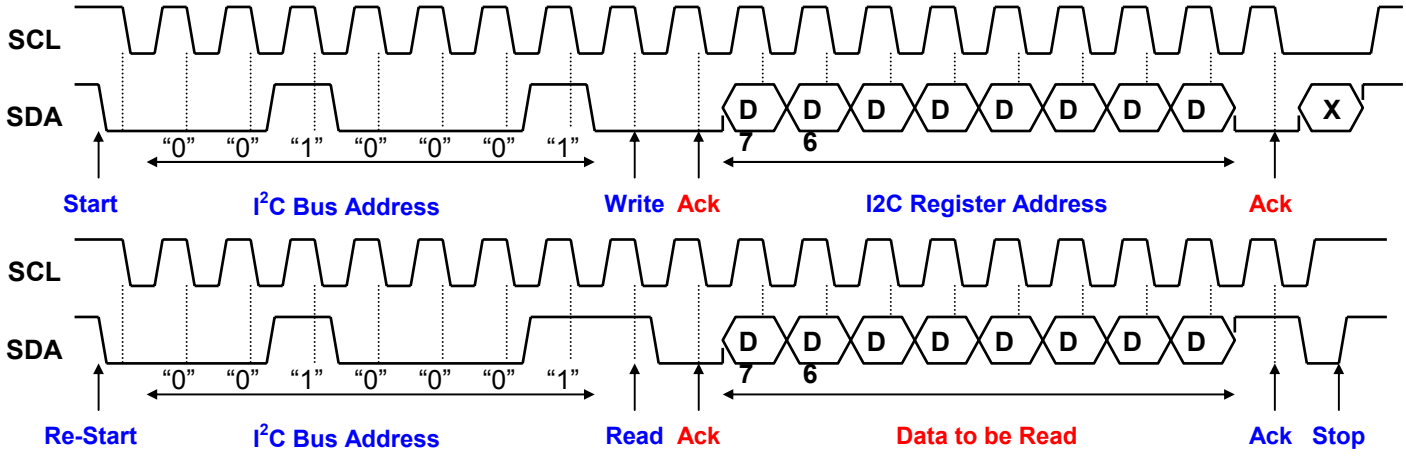


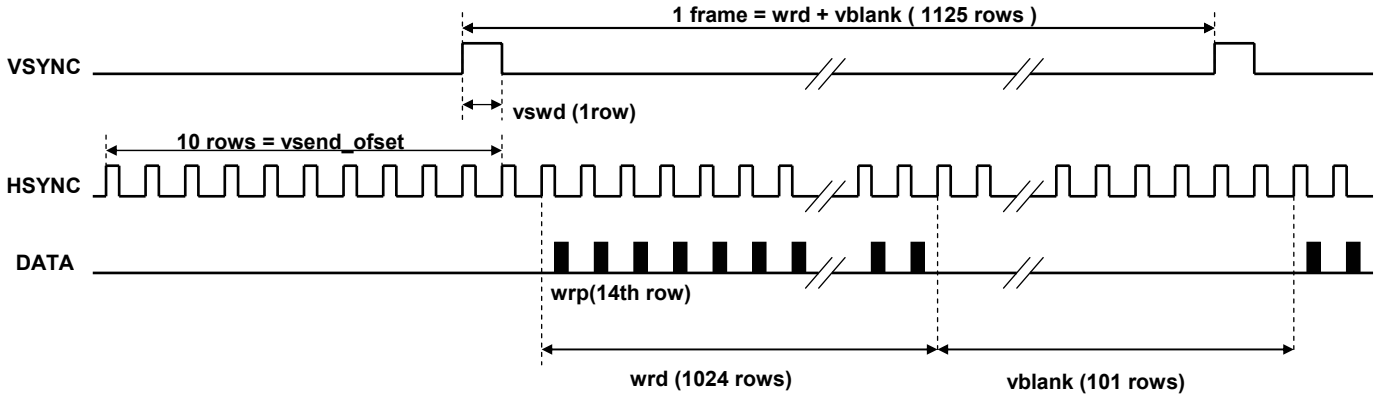
Figure 8. I²C Bus Read Cycle

TIMING CHART

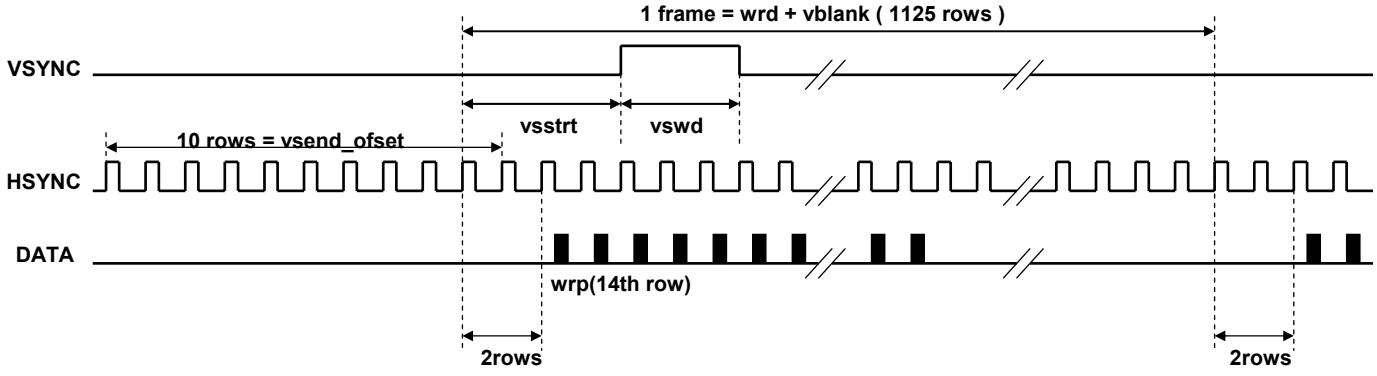
VERTICAL TIMING DIAGRAM

Continuous Frame Capture Mode

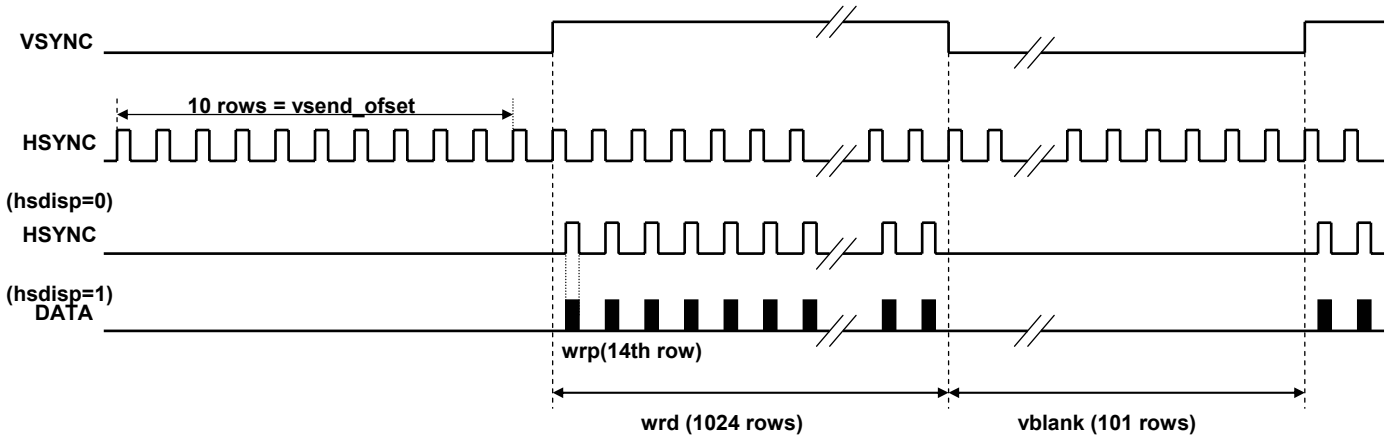
(Default Case)



(Delayed Vertical Sync Case)

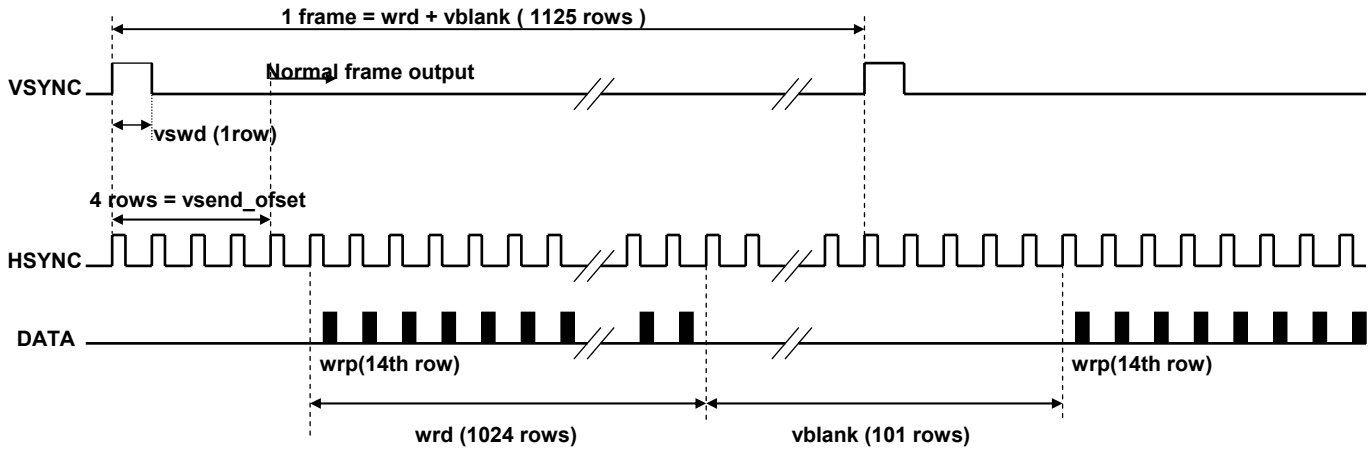


(Vertical Data Valid Mode Case) vsdisp=1

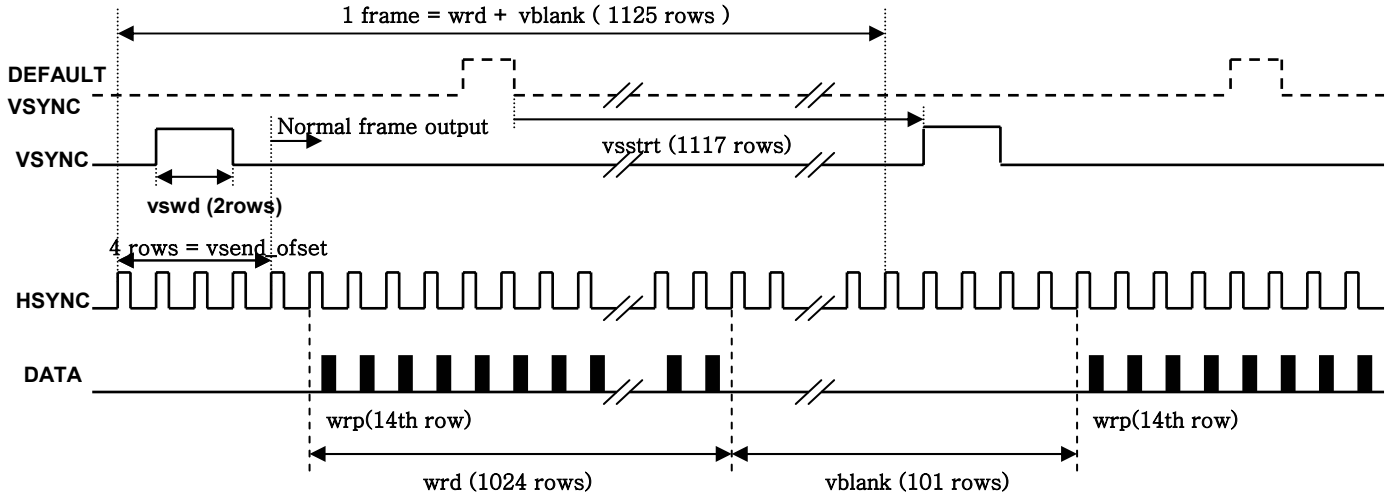


VERTICAL TIMING DIAGRAM (continued)

(Short OB Line & Fixed Vertical Sync mode) isp_sel = 1& fix_vs = 1



(Short OB Line & Normal Sync mode) isp_sel = 1, vsstrt = 1117d, vswd = 2d



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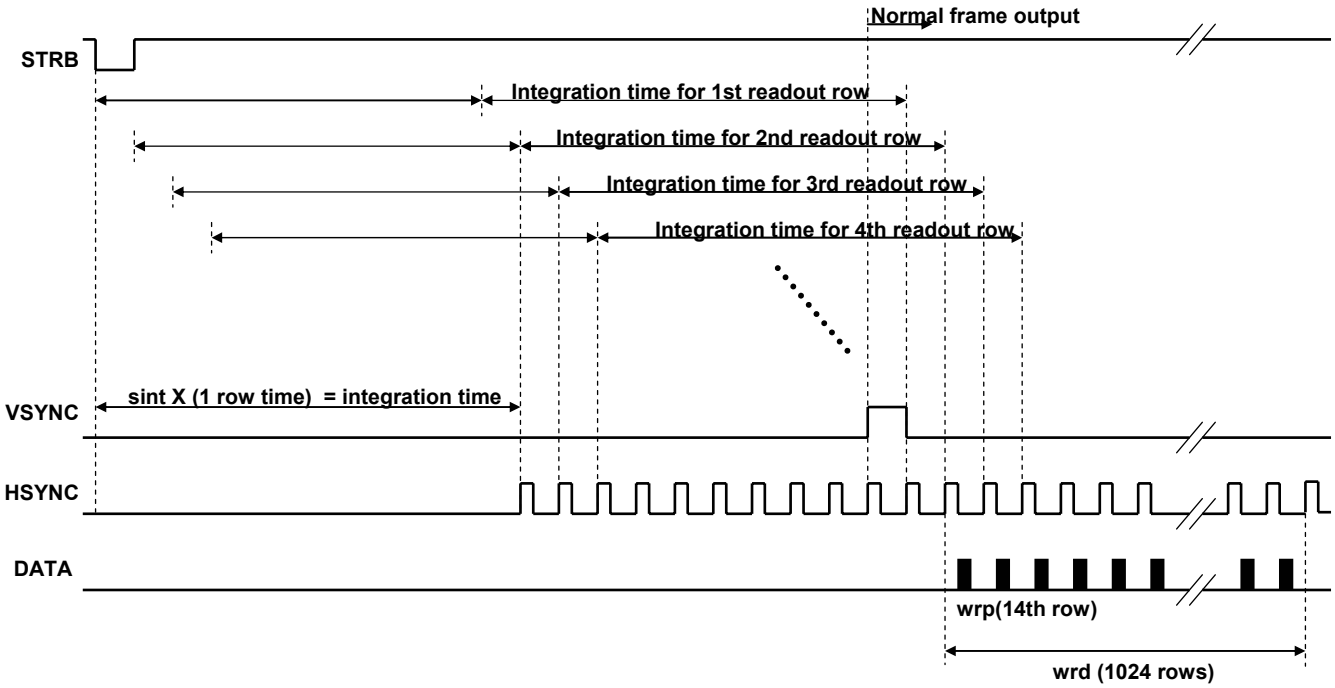
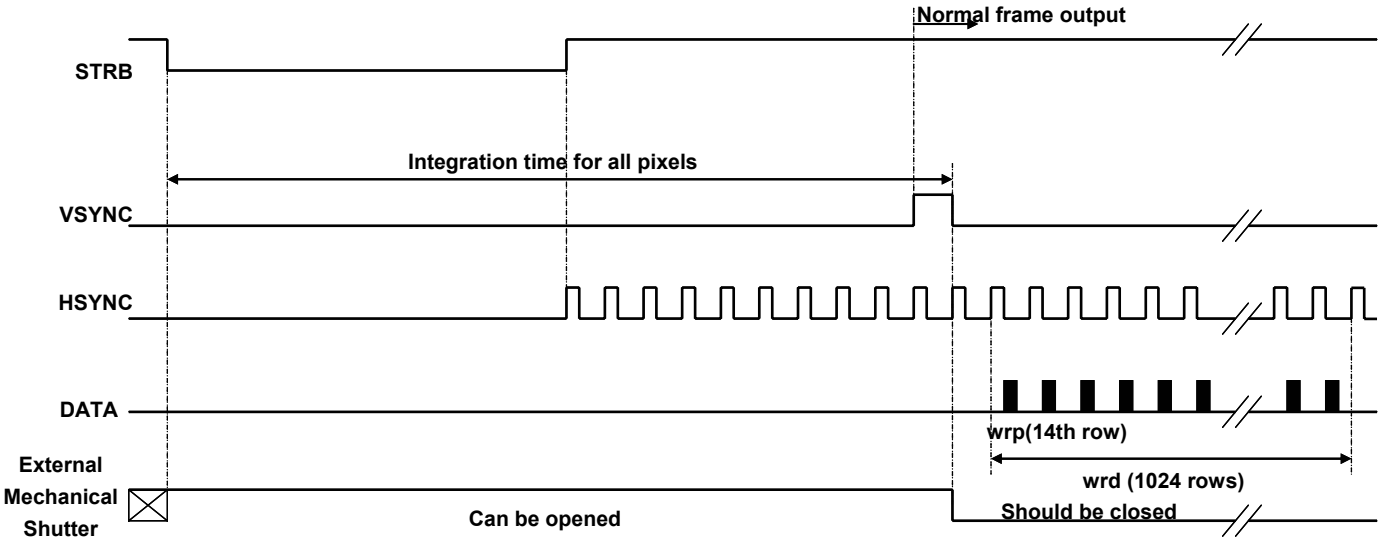
VERTICAL TIMING DIAGRAM (continued)

Single Frame Capture Mode

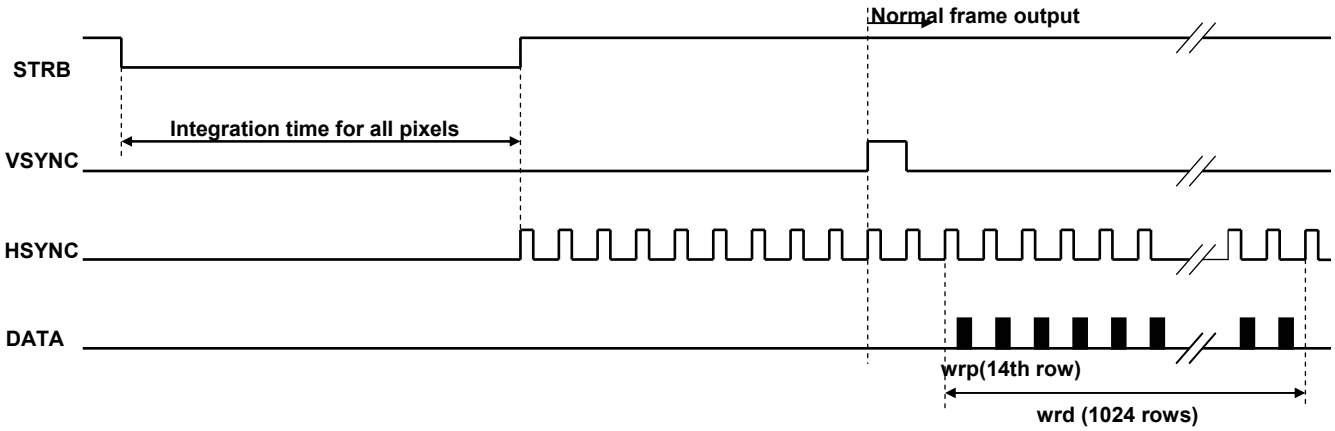
(Rolling Shutter Case, sfcen = 1 & roll_mod = 1)



(Mechanical Shutter Case, sfcen=1 & mech_mod = 1)

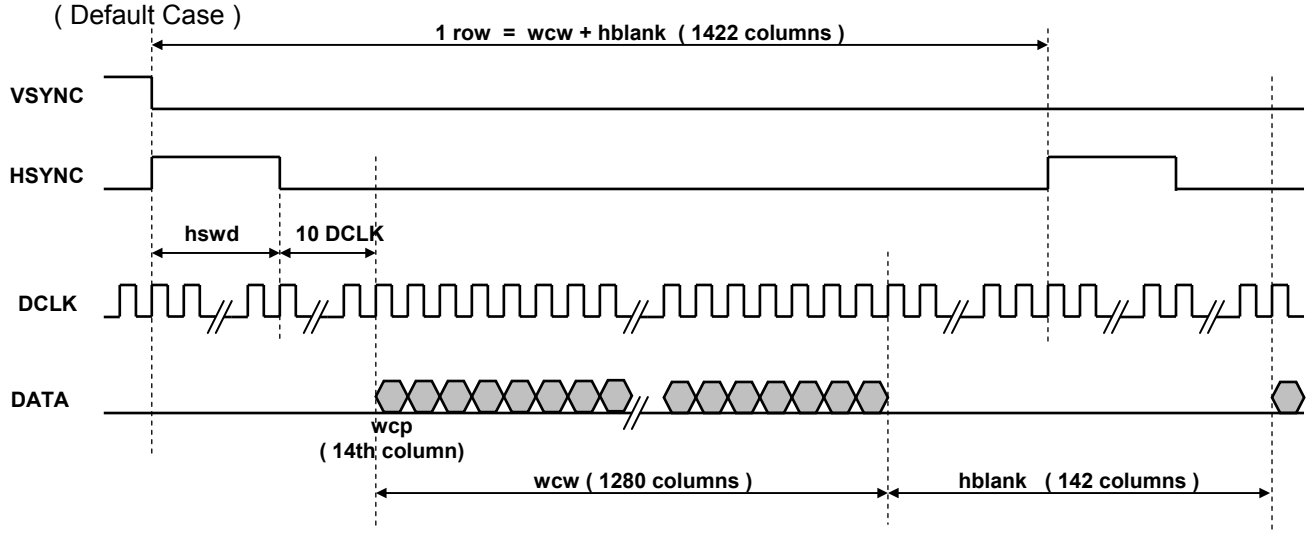


(Global Shutter Case, sfcen=1 & global_mod = 1)

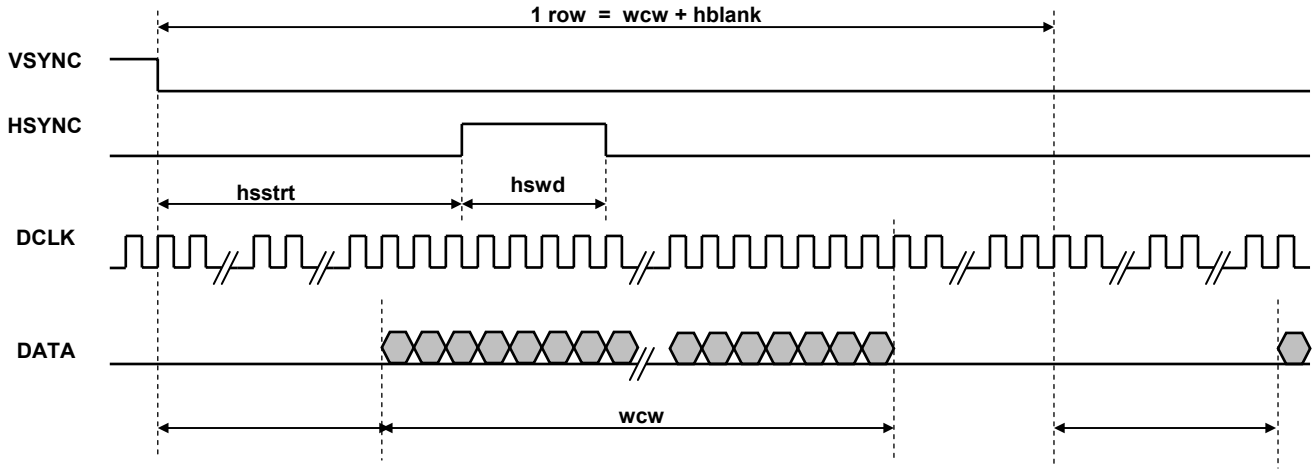


HORIZONTAL TIMING DIAGRAM

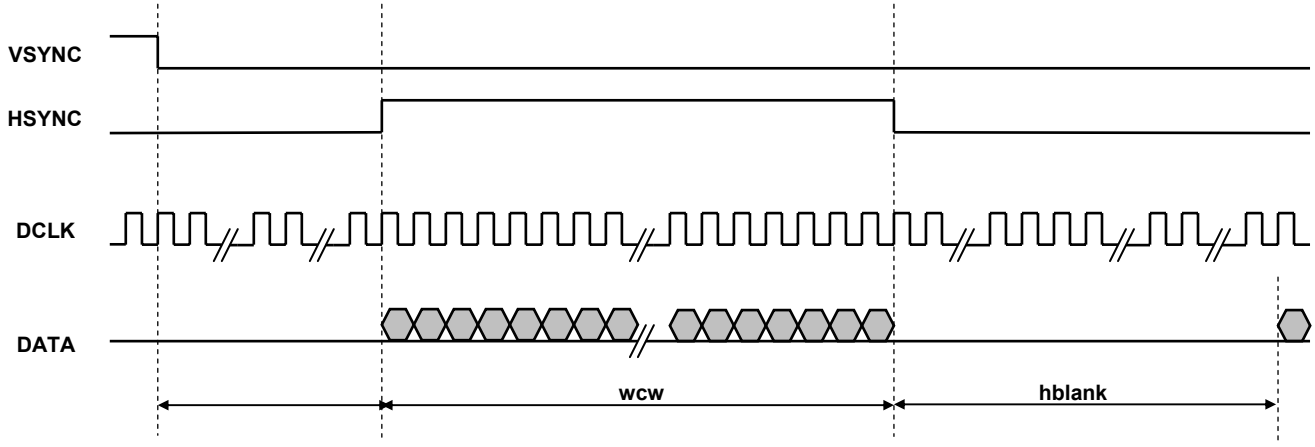
(Default Case)



(Delayed Horizontal Sync Case)



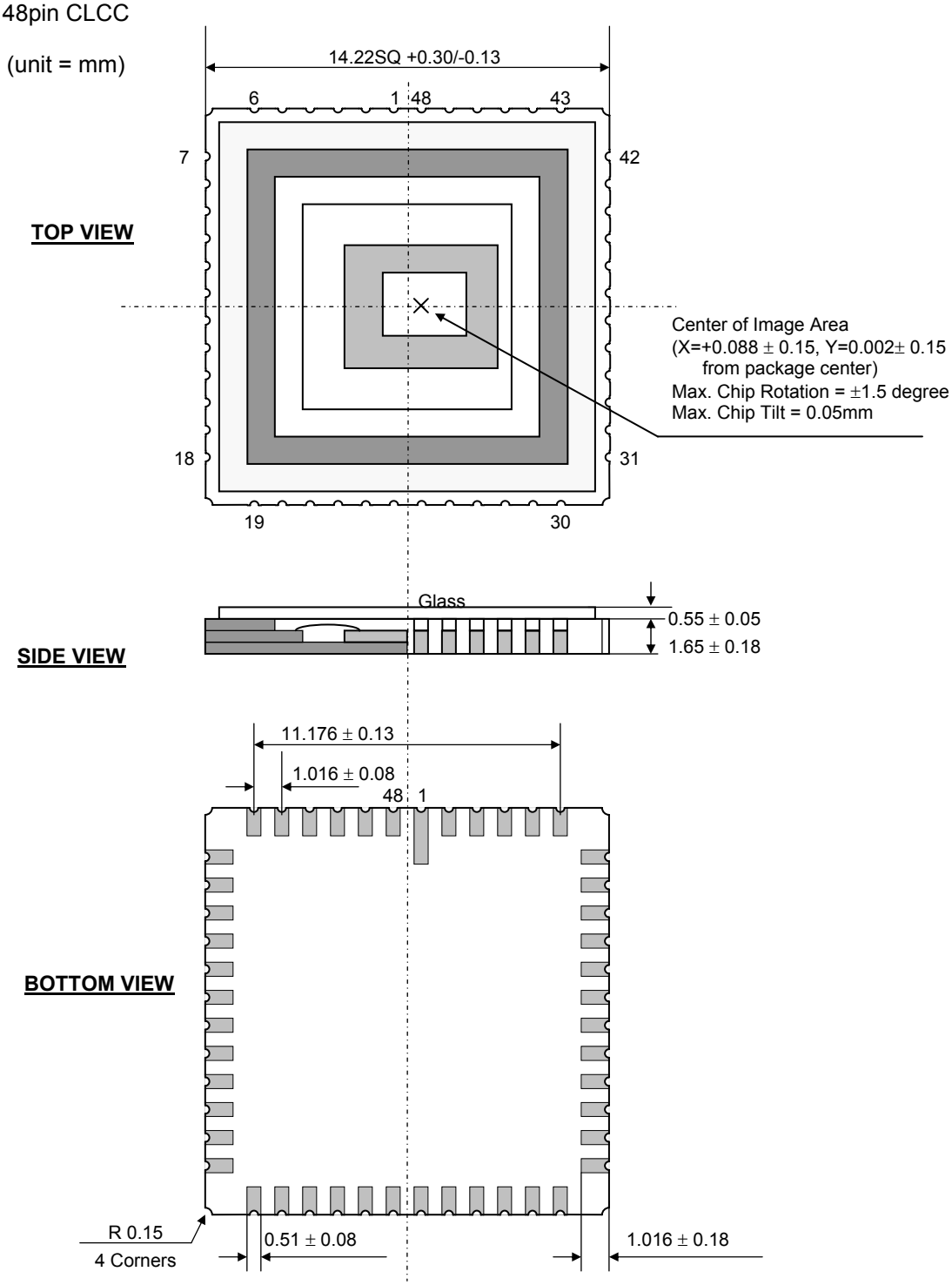
(Horizontal Data Valid Mode Case) hsdisp=1



PACKAGE DIMENSION

48pin CLCC

(unit = mm)



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