The Features of S3C6410

S3C6400 vs. S3C6410

OCT 30, 2007

REV 0.2

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S3C6410 32-Bit Risc Microcontroller

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Revision History

Revision No	Description of Change	Refer to	Author(s)	Date
0.1	- Initial Release for review	-		AUG 01, 2007
0.2	-Added SYSCON & GPIO			OCT 30, 2007

1. OVERVIEW (A POINT OF DIFFERENCE)

	S3C6400	S3C6410 (Added IP & function)	S/W change
DMC		Improved pipeline stages Deep Power Down support Variable number of auto-refresh requests before priority change. Improved write termination Auto self refresh entry	1.bank_bits is fixed for 4 banks 2. except 1, new controls are implemented in reserved addresses and bits
OneNANDC	Lowest 2 bit of address bit is ignored when accessed with AHB memory channel.	Lowest 4 bit of address bit is ignored when accessed with AHB memory channel.	Address map for accessing OneNAND memory contents is different.
	Maximum burst length of four is supported when accessing through AHB memory access channel.	Maximum burst length of eight is supported when accessing through AHB memory access channel.	
	OneNAND controller has a separate clock domain other than AHB clock domain.	OneNAND controller shares AHB clock domain with other memory controllers.	
NFCON	4KB Stepping Stone 1/4bit HW ECC 512B/2KB page read	8KB Stepping Stone 1/4/8-bit HW ECC 512B/2K/4KB page read	6400 Compatible Spare ECC generation (8-bit)
CFCON	CFCON 4.0	CFCON 4.01 HREADY Bug Fix	6400 Compatible
DMAC	MODEM_IF DMA operation not supported	Support MODEM_IF DMA (Mem-to-Mem)	New SFRs added
VIC	Interrupt source	Interrupt source	
Display CON	FIMD 4.0	FIMD 4.2.1 ITU BT.601/656 interface FIMC local interface sync clock addition	6400 Compatible
2D	FIMG-2D 1.23	FIMG-2D 2.0 AXI Master Enhanced Performance	Not Compatible 6400
CAMIF	FIMC 3.0	FIMC 3.2 Preview Path Line Buffer for D1 Support Interlace input FIMC local interface sync clock addition	
MODE IF	DMA operation not supported	DMA operation supported	New SFRs added
USB OTG	Power Save mode supported	Power Save mode not supported OTG block power down supported	S/W compatible

HSMMC	HSMMC(Ver3.1) (support SD Host Controller spec Ver1.0)	HSMMC (Ver4.0) (support SD Host Controller spec Ver2.0)	New SFRs added
IIC	1ch	2ch	
UART	4ch	4ch (3Mbps)	
RTC	Tick clock source is 32768Hz Tick counter is 16bit	Tick clock source (32768/16384/8192/4096/2048/1024/512/256/128/64/32/16/8/4/2/1)	S/W compatible.
IIS	16bit I2S 2ea	24bit Stereo I2S 2ea + 24bit Multi-Channel(up to 5.1) I2S 1ea	Bit length setting / Multi-Channel I2S transmission setting
TSADC	10bit 8channel	12bit 8channel	S/W compatible.
3D		New	

Note)

1. S/W change: User must change the software in S3C6410 even though user wants to use the same function of S3C6400 (refer to respective chapter in detail)

2. If user would like to use new IP or function, it is necessary to change software

3. There is no software change except above items

2. MEMORY MAP

2.1 Address region changes for newly introduced IPs in S3C6410.

2.1.1 S3C6400

Address		Description	Note
0x7200_0000	0x72FF_FFFF	Reserved	
0x7E00_3000	0x7E00_3FFF	Reserved	
0x7E00_8000	0x7E00_8FFF	Reserved	
0x7E00_9000	0x7E00_9FFF	Reserved	
0x7F00_D000	0x7F00_DFFF	Reserved	
0x7F00_E000	0x7F00_EFFF	Reserved	
0x7F00_F000	0x7F00_FFFF	Reserved	

2.1.2 S3C6410

Address		Description	Note
0x7200_0000	0x72FF_FFFF	3D Graphic Accelerator	
0x7E00_3000	0x7E00_3FFF	QoS control registers for AXI SPINE	
0x7E00_8000	0x7E00_8FFF	QoS control registers for AXI PERI	
0x7E00_9000	0x7E00_9FFF	QoS control registers for AXI SFR	
0x7F00_D000	0x7F00_DFFF	I2S version 4.0	
0x7F00_F000	0x7F00_FFFF	I2C	

2.2 Behavior for accessing reserved address regions

2.2.1 S3C6400

Accesses to reserve address region returns OKAY response.

2.2.2 S3C6410

Accesses to reserve address region returns ERROR response.

(IP Based reserved region,)

3. SYSTEM CONTROLLER

3.1 Difference summary

3.1.1 New functionality

Added Clock Gating SFRs (3D, I2S_V40, MEM0)

Added Clock Source Select SFRS(I2S_V40)

Extended ARM Divider Ratio (Max. Divider Value 8 -> 16)

Added clock divider value for Camera I/F

Added DMA select register for Modem I/F.

Added SROMC address expand register between DMC0 and SROMC.

Additional Power Domain SFRs (3D)

Added Operating Mode. (Synchronous mode)

Added DEEP_STOP Wake-up status register.

3.2 Register comparison

PLL Control Registers (Added Field)

EPLL_CON1	BIT	DESCRIPTION	RESET VALUE
RESERVED	[30:18]	RESERVED	0x0
ICP	[17:16]	EPLL ICP (Charge Pump Current Control)	0x0
KDIV	[15:0]	PLL K divide value	0x9111

Clock source control register (Added New SFR)

CLK_SRC2	BI	DESCRIPTION	RESET VALUE
RESERVED	[31:4]	RESERVED	0x0
AUDIO2_SEL	[2:0]	Control MUX_{AUDIO2}, which is the source clock of IIS_V40 (000:$MOUT_{EPLL}$, 001: $DOUT_{MPLL}$, 010:FIN_{EPLL}, 011: IIS_V40_CDCLK, 10x: PCMCDCLK[1])	0x0

Clock divider control register (Modified)

CLK_DIV0	BIT	DESCRIPTION	RESET VALUE
MFC_RATIO	[31:28]	MFC clock divider ratio *CLKMFC = $CLKMFC_{IN}$ / (MFC_RATIO + 1)*	0x0
JPEG_RATIO	[27:24]	JPEG clock divider ratio, which must be odd value. In other words, S3C6410 supports only even divider ratio. *CLKJPEG = HCLKX2 / (JPEG_RATIO + 1)*	0x1
CAM_RATIO	[23:20]	CAM clock divider ratio *CLKCAM = HCLKX2 / (CAM_RATIO + 1)*	0x0
SECUR_RATIO	[19:18]	Security clock divider ratio, which must be 0x1 or 0x3. *CLKSECUR = HCLKX2 / (SECUR_RATIO + 1)*	0x1
PCLK_RATIO	[15:12]	PCLK clock divider ratio, which must be odd value. In other words, S3C6410 supports only even divider ratio. *PCLK = HCLKX2 / (PCLK_RATIO + 1)*	0x1
HCLKX2_RATIO	[11:9]	HCLKX2 clock divider ratio *HCLKX2 = $HCLKX2_{IN}$ / (HCLKX2_RATIO + 1)*	0x0
HCLK_RATIO	[8]	HCLK clock divider ratio *HCLK = HCLKX2 / (HCLK_RATIO + 1)*	0
RESERVED	[7:5]	RESERVED	0x0
MPLL_RATIO	[4]	DIV_{MPLL} clock divider ratio *$DOUT_{MPLL}$ = $MOUT_{MPLL}$ / (MPLL_RATIO + 1)*	0
ARM_RATIO	[3:0]	DIV_{ARM} clock divider ratio *ARMCLK = $DOUT_{APLL}$ / (ARM_RATIO + 1)*	0x0

CLK_DIV1	BIT	DESCRIPTION	RESET VALUE
RESERVED	[31:28]	RESERVED	0x0
FIMC_RATIO	[27:24]	FIMC clock divider ratio *CLKFIMC = HCLKX2 / (FIMC_RATIO + 1)*	0x0
UHOST_RATIO	[23:20]	USB host clock divider ratio	0x0

		CLKUHOST = $CLKUHOST_{IN}$ / (UHOST_RATIO + 1)	
SCALER_RATIO	[19:16]	TV Scaler clock divider ratio *CLKSCALER = $CLKSCALER_{IN}$ / (SCALER_RATIO + 1)*	0x0
LCD_RATIO	[15:12]	LCD clock divider ratio *CLKLCD = $CLKLCD_{IN}$ / (LCD_RATIO + 1)*	0x0
MMC2_RATIO	[11:8]	MMC2 clock divider ratio *CLKMMC2 = $CLKMMC2_{IN}$ / (MMC2_RATIO + 1)*	0x0
MMC1_RATIO	[7:4]	MMC1 clock divider ratio *CLKMMC1 = $CLKMMC1_{IN}$ / (MMC1_RATIO + 1)*	0x0
MMC0_RATIO	[3:0]	MMC0 clock divider ratio *CLKMMC0 = $CLKMMC0_{IN}$ / (MMC0_RATIO + 1)*	0x0

CLK_DIV2	BIT	DESCRIPTION	RESET VALUE
RESERVED	[31:28]	RESERVED	0x0
AUDIO2_RATIO	[27:24]	AUDIO2 clock divider ratio *CLKAUDIO2 = $CLKAUDIO2_{IN}$ / (AUDIO2_RATIO + 1)*	0x0
IRDA_RATIO	[23:20]	IRDA clock divider ratio *CLKIRDA = $CLKIRDA_{IN}$ / (IRDA_RATIO + 1)*	0x0
UART_RATIO	[19:16]	UART clock divider ratio *CLKUART = $CLKUART_{IN}$ / (UART_RATIO + 1)*	0x0
AUDIO1_RATIO	[15:12]	AUDIO1 clock divider ratio *CLKAUDIO1 = $CLKAUDIO1_{IN}$ / (AUDIO1_RATIO + 1)*	0x0
AUDIO0_RATIO	[11:8]	AUDIO0 clock divider ratio *CLKAUDIO0 = $CLKAUDIO0_{IN}$ / (AUDIO0_RATIO + 1)*	0x0
SPI1_RATIO	[7:4]	SPI1 clock divider ratio *CLKSPI1 = $CLKSPI1_{IN}$ / (SPI1_RATIO + 1)*	0x0
SPI0_RATIO	[3:0]	SPI0 clock divider ratio *CLKSPI0 = $CLKSPI0_{IN}$ / (SPI0_RATIO + 1)*	0x0

PLL Control Registers (Added Field & Added SFRs)

HCLK_GATE	BIT	DESCRIPTION	RESET VALUE
HCLK_3DSE	[31]	Gating HCLK for 3D (0: mask, 1: pass)	1
RESERVED	[30]	RESERVED	1
HCLK_UHOST	[29]	Gating HCLK for UHOST (0: mask, 1: pass)	1
HCLK_SECUR	[28]	Gating HCLK for security sub-system (0: mask, 1: pass)	1
HCLK_SDMA1	[27]	Gating HCLK for SDMA1 (0: mask, 1: pass)	1
HCLK_SDMA0	[26]	Gating HCLK for SDMA0 (0: mask, 1: pass)	1

HCLK_IROM	[25]	Gating HCLK for IROM (0: mask, 1: pass)	1
HCLK_DDR1	[24]	Gating HCLK for DDR1 (0: mask, 1: pass)	1
HCLK_DDR0	[23]	Gating HCLK for DDR0 (0: mask, 1: pass)	1
HCLK_MEM1	[22]	Gating HCLK for DMC1 (0: mask, 1: pass)	1
HCLK_MEM0	[21]	Gating HCLK for DMC0, SROM, OneNAND, NFCON, CFCON (0: mask, 1: pass)	1
HCLK_USB	[20]	Gating HCLK for USB OTG (0: mask, 1: pass)	1
HCLK_HSMMC2	[19]	Gating HCLK for HSMMC2 (0: mask, 1: pass)	1
HCLK_HSMMC1	[18]	Gating HCLK for HSMMC1 (0: mask, 1: pass)	1
HCLK_HSMMC0	[17]	Gating HCLK for HSMMC0 (0: mask, 1: pass)	1
HCLK_MDP	[16]	Gating HCLK for MDP (0: mask, 1: pass)	1
HCLK_DHOST	[15]	Gating HCLK for direct HOST interface (0: mask, 1: pass)	1
HCLK_IHOST	[14]	Gating HCLK for indirect HOST interface (0: mask, 1: pass)	1
HCLK_DMA1	[13]	Gating HCLK for DMA1 (0: mask, 1: pass)	1
HCLK_DMA0	[12]	Gating HCLK for DMA0 (0: mask, 1: pass)	1
HCLK_JPEG	[11]	Gating HCLK for JPEG (0: mask, 1: pass)	1
HCLK_CAMIF	[10]	Gating HCLK for camera interface (0: mask, 1: pass)	1
HCLK_SCALER	[9]	Gating HCLK for scaler (0: mask, 1: pass)	1
HCLK_2D	[8]	Gating HCLK for 2D (0: mask, 1: pass)	1
HCLK_TV	[7]	Gating HCLK for TV encoder (0: mask, 1: pass)	1
RESERVED	[6]	RESERVED	1
HCLK_POST0	[5]	Gating HCLK for POST0 (0: mask, 1: pass)	1
HCLK_ROT	[4]	Gating HCLK for rotator (0: mask, 1: pass)	1
HCLK_LCD	[3]	Gating HCLK for LCD controller (0: mask, 1: pass)	1
HCLK_TZIC	[2]	Gating HCLK for trust interrupt controller (0: mask, 1: pass)	1
HCLK_INTC	[1]	Gating HCLK for vectored interrupt controller (0: mask, 1: pass)	1
HCLK_MFC	[0]	Gating HCLK for MFC (0: mask, 1: pass)	1

PCLK_GATE	BIT	DESCRIPTION	RESET VALUE
RESERVED	[31:28]	RESERVED	0x1F
PCLK_IIC1	[27]	Gating PCLK for IIC1 (0: mask, 1: pass)	1
PCLK_IIS2	[26]	Gating PCLK for IIS2 (0: mask, 1: pass)	1
RESERVED	[25]	RESERVED	1
PCLK_SKEY	[24]	Gating PCLK for security key (0: mask, 1: pass)	1
PCLK_CHIPID	[23]	Gating PCLK for chip ID (0: mask, 1: pass)	1
PCLK_SPI1	[22]	Gating PCLK for SPI1 (0: mask, 1: pass)	1

PCLK_SPI0	[21]	Gating PCLK for SPI0 (0: mask, 1: pass)	1
PCLK_HSIRX	[20]	Gating PCLK for HSI receiver (0: mask, 1: pass)	1
PCLK_HSITX	[19]	Gating PCLK for HSI transmitter (0: mask, 1: pass)	1
PCLK_GPIO	[18]	Gating PCLK for GPIO (0: mask, 1: pass)	1
PCLK_IIC0	[17]	Gating PCLK for IIC0 (0: mask, 1: pass)	1
PCLK_IIS1	[16]	Gating PCLK for IIS1 (0: mask, 1: pass)	1
PCLK_IIS0	[15]	Gating PCLK for IIS0 (0: mask, 1: pass)	1
PCLK_AC97	[14]	Gating PCLK for AC97 (0: mask, 1: pass)	1
PCLK_TZPC	[13]	Gating PCLK for TZPC (0: mask, 1: pass)	1
PCLK_TSADC	[12]	Gating PCLK for touch screen ADC (0: mask, 1: pass)	1
PCLK_KEYPAD	[11]	Gating PCLK for Key PAD (0: mask, 1: pass)	1
PCLK_IRDA	[10]	Gating PCLK for IRDA (0: mask, 1: pass)	1
PCLK_PCM1	[9]	Gating PCLK for PCM1 (0: mask, 1: pass)	1
PCLK_PCM0	[8]	Gating PCLK for PCM0 (0: mask, 1: pass)	1
PCLK_PWM	[7]	Gating PCLK for PWM (0: mask, 1: pass)	1
PCLK_RTC	[6]	Gating PCLK for RTC (0: mask, 1: pass)	1
PCLK_WDT	[5]	Gating PCLK for watch dog timer (0: mask, 1: pass)	1
PCLK_UART3	[4]	Gating PCLK for UART3 (0: mask, 1: pass)	1
PCLK_UART2	[3]	Gating PCLK for UART2 (0: mask, 1: pass)	1
PCLK_UART1	[2]	Gating PCLK for UART1 (0: mask, 1: pass)	1
PCLK_UART0	[1]	Gating PCLK for UART0 (0: mask, 1: pass)	1
PCLK_MFC	[0]	Gating PCLK for MFC (0: mask, 1: pass)	1

SCLK_GATE	BIT	DESCRIPTION	RESET VALUE
RESERVED	[31]	RESERVED	1
SCLK_UHOST	[30]	Gating special clock for USB-HOST (0: mask, 1: pass)	1
SCLK_MMC2_48	[29]	Gating special clock for MMC2 (0: mask, 1: pass)	1
SCLK_MMC1_48	[28]	Gating special clock for MMC1 (0: mask, 1: pass)	1
SCLK_MMC0_48	[27]	Gating special clock for MMC0 (0: mask, 1: pass)	1
SCLK_MMC2	[26]	Gating special clock for MMC2 (0: mask, 1: pass)	1
SCLK_MMC1	[25]	Gating special clock for MMC1 (0: mask, 1: pass)	1
SCLK_MMC0	[24]	Gating special clock for MMC0 (0: mask, 1: pass)	1
SCLK_SPI1_48	[23]	Gating special clock for SPI (0: mask, 1: pass)	1
SCLK_SPI0_48	[22]	Gating special clock for SPI (0: mask, 1: pass)	1
SCLK_SPI1	[21]	Gating special clock for SPI (0: mask, 1: pass)	1
SCLK_SPI0	[20]	Gating special clock for SPI (0: mask, 1: pass)	1
SCLK_DAC27	[19]	Gating special clock for DAC (0: mask, 1: pass)	1

SCLK_TV27	[18]	Gating special clock for TV encoder (0: mask, 1: pass)	1
SCLK_SCALER27	[17]	Gating special clock for scaler27 (0: mask, 1: pass)	1
SCLK_SCALER	[16]	Gating special clock for scaler (0: mask, 1: pass)	1
SCLK_LCD27	[15]	Gating special clock for LCD controller (0: mask, 1: pass)	1
SCLK_LCD	[14]	Gating special clock for LCD controller (0: mask, 1: pass)	1
SCLK_FIMC	[13]	Gating special clock for camera & LCD (0: mask, 1: pass)	1
SCLK_POST0_27	[12]	Gating special clock for POST0 (0: mask, 1: pass)	1
SCLK_AUDIO2	[11]	Gating special clock for PCM2, IIS2, AC97 2(0: mask, 1: pass)	1
SCLK_POST0	[10]	Gating special clock for POST0 (0: mask, 1: pass)	1
SCLK_AUDIO1	[9]	Gating special clock for PCM1, IIS1, AC97 1(0: mask, 1: pass)	1
SCLK_AUDIO0	[8]	Gating special clock for PCM0, IIS0, and AC97 0 (0: mask, 1: pass)	1
SCLK_SECUR	[7]	Gating special clock for security block (0: mask, 1: pass)	1
SCLK_IRDA	[6]	Gating special clock for IRDA (0: mask, 1: pass)	1
SCLK_UART	[5]	Gating special clock for UART0~3 (0: mask, 1: pass)	1
SCLK_MFC	[3]	Gating special clock for MFC (0: mask, 1: pass)	1
SCLK_CAM	[2]	Gating special clock for camera interface (0: mask, 1: pass)	1
SCLK_JPEG	[1]	Gating special clock for JPEG (0: mask, 1: pass)	1
RESERVED	[0]	RESERVED	1

MEM0_CLK_GATE	BIT	DESCRIPTION	RESET VALUE
RESERVED	[31:6]	RESERVED	0x3ff_ffff
HCLK_CFCON	[5]	Gating special clock for CFCON (0: mask, 1: pass)	1
HCLK_OneNAND1	[4]	Gating special clock for OneNAND1 (0: mask, 1: pass)	1
HCLK_OneNAND0	[3]	Gating special clock for OneNAND0 (0: mask, 1: pass)	1
HCLK_NFCON	[2]	Gating special clock for NFCON (0: mask, 1: pass)	1
HCLK_SROM	[1]	Gating special clock for SROM (0: mask, 1: pass)	1
HCLK_DMC0	[0]	Gating special clock for DMC0 (0: mask, 1: pass)	1

Software reset control register (Added Field)

SW_RST	BIT	DESCRIPTION	RESET VALUE
RESERVED	[31:18]	RESERVED	0x0
RESERVED	[17]	RESERVED	0x0
RESERVED	[16]	RESERVED	0x0
SWRESET	[15:0]	Generate software reset when the value is 0x6410	0x0000

System Others register (Added SFRs)

SYS_OTHERS	BIT	DESCRIPTION	RESET VALUE
RESERVED	[31:4]	RESERVED	0
MODEM_RX1_SDMA_SEL	[3]	DMA selection for MODEM RX1 (0: SDMA0, 1: DMA0)	0
MODEM_RX0_SDMA_SEL	[2]	DMA selection for MODEM RX0 (0: SDMA0, 1: DMA0)	0
MODEM_TX1_SDMA_SEL	[1]	DMA selection for MODEM TX1 (0: SDMA0, 1: DMA0)	0
MODEM_TX0_SDMA_SEL	[0]	DMA selection for MODEM TX0 (0: SDMA0, 1: DMA0)	0

Memory Controller Status register (Added Fields)

MEM_SYS_CFG	BI	DESCRIPTION	RESET VALUE
RESERVED	[31:15]	RESERVED	0x0000_0
INDEP_CF	[14]	Use CF interface independently. 0 = Use memory port 0 shared by EBI. 1 = Use independent CF interface.	0
nCFG_ADDR_EXPAND (nCFG_SROM_ADDR_EXPAND_To_DRAM0)	[13]	Set whether DRAM control pins are used for SROMC address field or not. Note: Active low. 0 = Xm0RAS, CAS, AP, WE pins are used for SROMC address [19:16]. 1 = Xm0RAS, CAS, AP, WE pins are used for DRAM0.	0
BUS_WIDTH	[12]	Select initial state of SROMC CS0 memory bus width. 0 = 8-bit data width. 1 = 16-bit data width. If NOR booting (OM[4:1] = 0101) is selected, this setting is ignored and 16-bit data width is selected. Even this bit is set to 0 or 1, this selects only reset value of DataWidth0 of SROM_BW SFR in SROMC. Bus width of CS0 for SROMC follows DataWidth0 setting.	0
EBI_PRI	[11]	Set EBI priority scheme.	0

<table>
<tr><td></td><td></td><td>0 = Fixed priority scheme.
1 = Circular priority scheme.</td><td></td></tr>
<tr><td>EBI_FIX_PRI</td><td>[10:8]</td><td>Set EBI fixed priority setting.
<table>
<tr><td></td><td>Highest <-> Lowest</td></tr>
<tr><td>0,6,7</td><td>DMC0 – SROMC - OneNANDC CS0 - OneNANDC CS1 – NFCON – CFCON</td></tr>
<tr><td>1</td><td>DMC0 – OneNANDC CS0 – OneNANDC CS1 – SROMC – NFCON – CFCON</td></tr>
<tr><td>2</td><td>DMC0 - OneNANDC CS1 – NFCON – SROMC - OneNANDC CS0 – CFCON</td></tr>
<tr><td>3</td><td>DMC0 – NFCON – SROMC - OneNANDC CS0 - OneNANDC CS1 – CFCON</td></tr>
<tr><td>4</td><td>DMC0 – CFCON – SROMC - OneNANDC CS0 - OneNANDC CS1 – NFCON</td></tr>
<tr><td>5</td><td>SROMC - DMC0 - OneNANDC CS0 - OneNANDC CS1 – NFCON – CFCON</td></tr>
</table></td><td>000</td></tr>
<tr><td>ADDR_EXPAND (CFG_SROM_ADDR_EXPAND_To_DRAM1</td><td>[7]</td><td>Set usage of Xm1DATA[31:16] pins.
0 = Xm1DATA[31:16] pins are used for DMC1 upper halfword data field, data[31:16].
1 = Xm1DATA[31:16] pins are used for SROMC upper 10-bit address field, address[25:16].</td><td>1</td></tr>
<tr><td>ENDIAN</td><td>[6]</td><td>Set endian control for SROMC, NFCON, and internal ROM.
0 = Little-endian memory system.
1 = Big-endian byte-invariant memory system.</td><td>0</td></tr>
<tr><td>MP0_CS_SEL</td><td>[5:0]</td><td>Set static memory chip selection multiplexing of memory port 0.
Setting for MP0_CS_SEL[0] and MP0_CS_SEL[2] are ignored. Distinguishing OneNANDC and NFCON is done by XSELNAND pin value instead of MP0_CS_SEL[0] and MP0_CS_SEL[2]. When XSELNAND is 0, OneNANDC is selected. When XSELNAND is 1, NFCON is selected.
When NAND booting (OM[4:3] = 00) is selected, the setting values of MP0_CS_SEL[1] and MP0_CS_SEL[3] as well as XSELNAND setting are ignored and Xm0CSn[2] and Xm0CSn[3] are used as NFCON CS0 and NFCON CS1. In this case, XSELNAND should be set to 1.
When OneNAND booting (OM[4:1] = 0110) is selected, the setting values of MP0_CS_SEL[1] and MP0_CS_SEL[3] are ignored and Xm0CSn[2] and Xm0CSn[3] are used as OneNANDC CS0 and OneNANDC CS1. In this case, XSELNAND should be set to 0.
<table>
<tr><td rowspan="2"></td><td colspan="6">MP0_CS_SEL</td><td rowspan="2"></td></tr>
<tr><td>[5]</td><td>[4]</td><td>[3]</td><td>[2]</td><td>[1]</td><td>[0]</td></tr>
<tr><td>Xm0CSn[0]</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>SROMC CS0</td></tr>
</table></td><td>0x00</td></tr>
</table>

		Xm0CSn[1]	-	-	-	-	-	-	SROMC CS1		
		Xm0CSn[2]	-	-	-	-	1	-	SROMC CS2		
			-	-	-	-	0	-	OneNANDC CS0		
			-	-	-	-	0	-	NFCON CS0		
		Xm0CSn[3]	-	-	1	-	-	-	SROMC CS3		
			-	-	0	-	-	-	OneNANDC CS1		
			-	-	0	-	-	-	NFCON CS1		
		Xm0CSn[4]	-	0	-	-	-	-	SROMC CS4		
			-	1	-	-	-	-	CFCON CS0		
		Xm0CSn[5]	0	-	-	-	-	-	SROMC CS5		
			1	-	-	-	-	-	CFCON CS1		

NORMAL Configuration Register (Added Fields)

NORMAL_CFG	BI	DESCRIPTION	RESET VALUE
RESERVED	[31]	DO NOT CHANGE	1
IROM	[30]	0: LP mode(OFF), 1: active mode(ON)	1
RESERVED	[29:17]	DO NOT CHANGE	0x1FFF
DOMAIN_ETM	[16]	0: LP mode(OFF), 1: active mode(ON)	1
DOMAIN_S	[15]	0: LP mode(OFF), 1: active mode(ON)	1
DOMAIN_F	[14]	0: LP mode(OFF), 1: active mode(ON)	1
DOMAIN_P	[13]	0: LP mode(OFF), 1: active mode(ON)	1
DOMAIN_I	[12]	0: LP mode(OFF), 1: active mode(ON)	1
RESERVED	[11]	RESERVED	0x1
DOMAIN_G	[10]	0: LP mode(OFF), 1: active mode(ON)	0x1
DOMAIN_V	[9]	0: LP mode(OFF), 1: active mode(ON)	1
RESERVED	[8:0]	DO NOT CHANGE	0x100

Others Register (Added Fields)

OTHERS	BIT	DESCRIPTION	RESET VALUE
RESERVED	[31:24]	RESERVED	0x0000
STABLE COUNTER SCALE	[23]	Indicate OSC_STABLE, PWR_STABLE counter scale 0 : Exponential Scale, 1 : Linear Scale	0
RESERVED	[22:17]	RESERVED	0x0000
USB_SIG_MASK	[16]	USB signal mask to prevent unwanted leakage.	0

		(This bit must set before USB PHY is used.)	
RESERVED	[14]	DO NOT CHANGE	0
CLEAR_DBGACK	[13]	Clear DBGACK signal when this field has 1. ARM1176 asserts DBGACK signal to indicate the system has entered Debug state. If DBGACK is asserted, this state is store in SYSCON until software clear it using this field.	0
CLEAR_BATF_INT	[12]	Clear interrupt caused by battery fault when this bit is set.	0
RESERVED	[11:8]	DO NOT CHANGE	0x00
SYNCMODE	[7]	SYNCMODEREQ to ARM 0: Asynchronous mode, 1: Synchronous mode	0
SYNCMUXSEL	[6]	SYS CLOCK SELECT IN CMU 0: Asynchronous mode, 1: Synchronous mode	0
RESEVED	[5:3]	DO NOT CHANGE	0x3
SPNIDEN	[2]	Secure privileged non-invasive debug enable. This field enables and disables non-invasive debug in the secure world of ARM1176. If it is '1', non-invasive debug is permitted in all non-secure mode. Otherwise, non-invasive debug is not permitted in all secure privileged mode. Non-invasive debug is permitted in Secure use mode according to the SUNIDEN bit of ARM1176.	1
SPIDEN	[1]	Secure privileged invasive debug enable. This field enables and disables invasive debug in the secure world of ARM1176. If it is '1', invasive debug is permitted in all secure mode. Otherwise, invasive debus is not permitted in any secure privileged mode. Invasive debug is permitted in Secure use mode according to the SUNIDEN bit of ARM1176.	1
CP15DISABLE	[0]	Disables write asses to some system control processor registers of ARM1176. (0: enable, 1: disable)	0

Reset Status register (Added Fields)

RST_STAT	BIT	DESCRIPTION	RESET VALUE
RESERVED	[31:7]	RESERVED	0x0000_000
DEEP_STOP_WAKEUP	[6]	Reset by DEEP_STOP mode wake-up	0
SW_RESET	[5]	Software reset by SWRESET	0
RESERVED	[4]	RESERVED	0
SLEEP_WAKEUP	[3]	Reset by SLEEP mode wake-up	0
WDT_RESET	[2]	Watch dog timer reset by WDTRST	0
WARM_RESET	[1]	Warm reset by XnWRESET. This field is not set when the wakeup source of SLEEP mode is XnWRESET.	0

HW_RESET	[0]	External reset by XnRESET	1

4.MEMORY SUBSYSTEM

4.1 Behavior for accessing reserved address regions

4.1.1 S3C6400

Accesses to reserve address region returns OKAY response.

4.1.2 S3C6410

Accesses to reserve address region returns ERROR response.

(IP Based reserved region,)

4.2 Clock domain for OneNAND controller

4.2.1 S3C6400

OneNAND controller has a separate clock domain other than AHB clock domain.

4.2.2 S3C6410

OneNAND controller shares AHB clock domain with other memory controllers.

5. DRAM CONTROLLER

5.1 Difference summary

5.1.1 New programmable options

DPD support

Variable number of auto-refresh requests before priority change.

5.1.2 New functionality

Improved pipeline stages

Improved write termination

Auto self refresh entry

5.2 Register comparison

5.2.1 DRAM Controller Status Register (MODIFIED)

Register	Address	R/W	Description	Reset Value
P0MEMSTAT	0x9E000000	R	16-bit DRAM controller status register	0xAB0
P1MEMSTAT	0x9E001000	R	32-bit DRAM controller status register	0xAB4

S3C6400

PnMEMSTAT	Bit	Description	Initial State
Reserved	[31:14]	Read undefined.	
Memory banks	[13:12]	The maximum number of banks that DRAM controller supports on each chip. 00 = 4 banks	00
Exclusive monitors	[11:10]	The number of exclusive access monitor resources 10 = 2 monitors	10
Reserved	[9]	Read always zero.	0

Memory chips	[8:7]	The maximum number of different chip selects that DRAM controller can supports: 11 = 4 chips However, S3C6400X uses only two chip select signals per DRAM controller.	11
Memory type	[6:4]	The type of SDRAM that DRAM controller supports: 100 = Support SDR SDRAM (normal or mobile) and DDR SDRAM (normal or mobile)	100
Memory width	[3:2]	The width of the external memory 00 = 16-bit 01 = 32-bit 10 = 64-bit 11 = reserved	00 / 01
Controller status	[1:0]	The status of the DRAM controller 00 = Config. 01 = Ready 10 = Paused 11 = Low-Power	00

S3C6410

PnMEMSTAT	Bit	Description	Initial State
Reserved	[31:14]	Read undefined.	
Memory banks	[13:12]	The maximum number of banks that DRAM controller supports on each chip. 00 = 4 banks	00
Exclusive monitors	[11:10]	The number of exclusive access monitor resources 10 = 2 monitors	10
Reserved	[9]	Read always zero.	0
Memory chips	[8:7]	The maximum number of different chip selects that DRAM controller can supports: 00 = 1chip, 01 = 2 chips, 10 = 3 chips, 11 = 4 chips	11
Memory type	[6:4]	The type of SDRAM that DRAM controller supports: 000 = SDR SDRAM, 001 = DDR SDRAM 011 = Mobile DDR SDRAM, 010 = eDRAM 1xx = Reserved. If Mobile DDR SDRAM or SDR SDRAM or an eDRAM is supported, the cas_half_cycle bit at address offset 0x14 is ignored.	000/001
Memory width	[3:2]	The width of the external memory 00 = 16-bit 01 = 32-bit 10 = 64-bit 11 = reserved	00 / 01
Controller status	[1:0]	The status of the DRAM controller 00 = Config. 01 = Ready 10 = Paused 11 = Low-Power	00

5.2.2 Direct Command Register

Register	Address	R/W	Description	Reset Value
P0DIRECTCMD	0x9E000008	W	16-bit DRAM controller direct command register	
P1 DIRECTCMD	0x9E001008	W	32-bit DRAM controller direct command register	

r0p0_AP

PnDIRECTCMD	Bit	Description	Initial State
Reserved	[31:22]	Undefined. Write as Zero	
Chip number	[21:20]	Bits mapped to external memory chip address bits.	
Memory command	[19:18]	Determine the command required 00 = Prechargeall 01 = Autorefresh 10 = MRS or EMRS 11 = NOP.	
Bank address	[17:16]	Bits mapped to external memory bank address bits when command is MRS or EMRS access.	
Reserved	[15:14]	Undefined. Write as Zero	
Address_13_to_0	[13:0]	Bits mapped to external memory address bits [13:0] when command is MRS or EMRS access.	

S3C6410

PnDIRECTCMD	Bit	Description	Initial State
Reserved	[31:23]	Undefined. Write as Zero	
Extended Memory command	[22]	Extended memory command, see note after the table If this bit is set and Memory command is Prechargeall, direct command is DPD.	
Chip number	[21:20]	Bits mapped to external memory chip address bits.	
Memory command	[19:18]	Determine the command required 00 = Prechargeall 01 = Autorefresh 10 = MRS or EMRS 11 = NOP.	
Bank address	[17:16]	Bits mapped to external memory bank address bits when command is MRS or EMRS access.	

Reserved	[15:14]	Undefined. Write as Zero	
Address_13_to_0	[13:0]	Bits mapped to external memory address bits [13:0] when command is MRS or EMRS access.	

5.2.3 Memory Configuration 2 Register (MODIFIED)

Register	Address	R/W	Description	Reset Value
P0MEMCFG2	0x9E00004C	R/W	16-bit DRAM controller configuration register	0x0B00
P1MEMCFG2	0x9E00104C	R/W	32-bit DRAM controller configuration register	0x0B40

r0p0_AP

PnMEMCFG2	Bit	Description	Initial State
Reserved	[31:13]	Read undefined. Write as Zero.	
Read delay	[12:11]	Encodes the delay used when reading from the pad interface to allow for de-skew of incoming read data 00 = Read delay 0 cycle (usually for SDR SDRAM) 01 = Read delay 1 cycle (usually for DDR SDRAM and mobile DDR SDRAM) 10, 11 = Read delay 2 cycle	01
Memory type	[10:8]	The type of SDRAM that is attached to DRAM controller: 000 = SDR SDRAM 001 = DDR SDRAM 011 = mobile DDR SDRAM 010 = Embedded SDRAM 1xx = reserved	011
Memory width	[7:6]	The width of the external memory 00 = 16-bit 01 = 32-bit 10 = 64-bit 11 = 128-bit	00 / 01
Bank bits	[5:4]	Encodes the number of bit of the AXI address that comprise the bank address. 00 = 2 bits 01 = 1 bit 10 = 0 bit 11 = reserved	00
Reserved	[3]	Read as Zero. Write as Zero.	0
DQM init	[2]	State of DQM when memory reset is de-asserted.	1

Clock config	[1:0]	The clock scheme supports: 00 = AXI clock and memory clock are asynchronous. 01 = AXI clock and memory clock are synchronous, and AXI clock is the same frequency or slower than memory clock. S3C6400X supports synchronous configuration. If this value is set to asynchronous, S3C6400X should endure performance degradation. 10~11 = reserved	00

r2p0_AP

PnMEMCFG2	Bit	Description	Initial State
Reserved	[31:13]	Read undefined. Write as Zero.	
Read delay	[12:11]	Encodes the delay used when reading from the pad interface to allow for de-skew of incoming read data 00 = Read delay 0 cycle (usually for SDR SDRAM) 01 = Read delay 1 cycle (usually for DDR SDRAM and mobile DDR SDRAM) 10, 11 = Read delay 2 cycle	01
Memory type	[10:8]	The type of SDRAM that is attached to DRAM controller: 000 = SDR SDRAM 001 = DDR SDRAM 011 = mobile DDR SDRAM 010 = Embedded SDRAM 1xx = reserved	011
Memory width	[7:6]	The width of the external memory 00 = 16-bit 01 = 32-bit 10 = 64-bit 11 = 128-bit	00 / 01
Reserved	[5:4]	Read undefined. Write as Zero.[1]	00
Cke Init	[3]	Sets the level for the cke outputs after reset.	0
DQM init	[2]	State of DQM when memory reset is de-asserted.	1
A_gt_m_sync	[1]	Requires to be set HIGH when running the aclk and mclk synchronously but with aclk running faster than mclk.	00
sync	[0]	Set high when aclk and mclk are synchronous.	

[1] bank_bits is not programmable in S3C6410

5.2.4 Memory Configuration 3 Register (NEW)

Register	Address	R/W	Description	Reset Value
P0MEMCFG3	0x9E000050	R/W	16-bit DRAM controller configuration register	0x0B00
P1MEMCFG3	0x9E001050	R/W	32-bit DRAM controller configuration register	0x0B40

r2p0_AP

PnMEMCFG3	Bit	Description	Initial State
sr_enable	[31]	Auto self-entry enable. Only if configured else read is undefined write as zero.	0
Reserved	[30:12]	Read undefined. Write as Zero.	
Prescale	[11:3]	Prescalar counter value.	
max_outs_refs	[2:0]	Maximum number of outstanding refresh commands.	

6. SROM CONTROLLER

6.1 Difference summary

There in no change

7. ONENAND CONTROLLER

7.1 Address regions

7.1.1 S3C6400

dev_id size field	Density	# of Blocks	Page Size	MAP location	MEM_ADDR Field					
					Reserved	DFS_DBS	FBA	FPA	FSA	Reserved
0000	128Mb	256	1KB	[23:22]	[21:17]	N/A	[16:9]	[8:3]	[2]	[1:0]
0001	256Mb	512	1KB	[23:22]	[21:18]	N/A	[17:9]	[8:3]	[2]	[1:0]
0010	512Mb	512	2KB	[23:22]	[21:19]	N/A	[18:10]	[9:4]	[3:2]	[1:0]
0011	1Gb Dual Die	1024	2KB	[23:22]	[21:20]	[19]	[18:10]	[9:4]	[3:2]	[1:0]
0011	1Gb	1024	2KB	[23:22]	[21]	N/A	[19:10]	[9:4]	[3:2]	[1:0]
0100	2Gb Dual Die	2048	2KB	[23:22]	[21]	[20]	[19:10]	[9:4]	[3:2]	[1:0]
0100	2Gb	2048	2KB	[23:22]	N/A	N/A	[20:10]	[9:4]	[3:2]	[1:0]
0101	4Gb Dual Die	4096	2KB	[23:22]	N/A	[21]	[20:10]	[9:4]	[3:2]	[1:0]
0101	4Gb	4096	2KB	[23:22]	N/A	N/A	[21:10]	[9:4]	[3:2]	[1:0]

7.1.2 S3C6410

dev_id size field	Density	# of Blocks	Page Size	MAP location	MEM_ADDR Field					
					Reserved	DFS_DBS	FBA	FPA	FSA	Reserved
0000	128Mb	256	1KB	[25:24]	[23:20]	N/A	[19:12]	[11:6]	[4][1]	[3:0]
0001	256Mb	512	1KB	[25:24]	[23:21]	N/A	[20:12]	[11:6]	[4][2]	[3:0]

[1] In case of dev_id of 0000, MEM_ADDR[5] is not used.
[2] In case of dev_id of 0001, MEM_ADDR[6] is not used.

0010	512Mb	512	2KB	[25:24]	[23:21]	N/A	[20:12]	[11:6]	[5:4]	[3:0]
0011	1Gb Dual Die	1024	2KB	[25:24]	[23:22]	[21]	[20:12]	[11:6]	[5:4]	[3:0]
0011	1Gb	1024	2KB	[25:24]	[23]	N/A	[21:12]	[11:6]	[5:4]	[3:0]
0100	2Gb Dual Die	2048	2KB	[25:24]	[23]	[22]	[21:12]	[11:6]	[5:4]	[3:0]
0100	2Gb	2048	2KB	[25:24]	N/A	N/A	[22:12]	[11:6]	[5:4]	[3:0]
0101	4Gb Dual Die	4096	2KB	[25:24]	N/A	[23]	[22:12]	[11:6]	[5:4]	[3:0]
0101	4Gb	4096	2KB	[25:24]	N/A	N/A	[23:12]	[11:6]	[5:4]	[3:0]

7.2 AHB transaction supported

7.2.1 S3C6400

OneNAND controller supports burst length up to four.

7.2.2 S3C6410

OneNAND controller supports burst length up to eight.

7.3 Clock domain for OneNAND controller

7.3.1 S3C6400

OneNAND controller has a separate clock domain other than AHB clock domain.

7.3.2 S3C6410

OneNAND controller shares AHB clock domain with other memory controllers.

8. NAND FLASH CONTROLLER

8.1 NAND controller compare

Difference	S3C6400	S3C6410
Nand booting	8-bit Only (after booting, 16-bit access is possible in software mode) 512B / 2KB page	8-bit Only (after booting, 16-bit access is possible in software mode) 512B / 2KB / 4KB page
MLC	Support	Support
ECC	1-bit / 4-bit ECC	1-bit / 4-bit / 8-bit ECC
Stepping stone	4KB	8KB

8.2 NAND ECC Encoding & Decoding

8.2.1 S3C6410 4bit ECC Programming guide (Encoding)

1) To use 4bit ECC in software mode, set the MsgLength to 0(512-byte message length) and set the ECCType to “10”(enable 4bit ECC). ECC module generates ECC parity code for 512-byte write data. So, you have to reset ECC value by writing the InitMECC (NFCONT[5]) bit as ‘1’ and have to clear the MainECCLock (NFCONT[7]) bit to ‘0’(Unlock) before write data.
MainECCLock (NFCONT[7]) bit controls whether ECC Parity code is generated or not.

2) Whenever data is written, the 4bit ECC module generates ECC parity code internally.

3) After you finish writing 512-byte data (not include spare area data), the parity codes are automatically updated to NFMECC0, NFMECC1 register. If you use 512-byte NAND flash memory, you can program these values to spare area. However, if you use NAND flash memory more than 512-byte page, you can’t program immediately. In this case, you have to copy these parity codes to other memory like DRAM. After writing all main data, you can write the copied ECC values to spare area.
The parity codes have self-correctable information include parity code itself.

4) To generate spare area ECC parity code, set the MsgLength to 1(24-byte message length), and set the ECCType to “10”(enable 4bit ECC). ECC module generates ECC parity code for 24-byte write data. So you have to reset ECC value by writing the InitMECC (NFCONT[5]) bit as ‘1’ and have to clear the MainECCLock (NFCONT[7]) bit to ‘0’(Unlock) before write data.
MainECCLock (NFCONT[7]) bit controls whether ECC Parity code is generated or not.

5) Whenever data is written, the 4bit ECC module generates ECC parity code internally.

6) When you finish writing 24-byte meta or extra data, the parity codes are automatically updated to

NFMECC0, NFMECC1 register. You can program these parity codes to spare area.
The parity codes have self-correctable information include parity code itself.

8.2.2 S3C6410 4bit ECC Programming guide (dEcoding)

1) To use 4bit ECC in software mode, set the MsgLength to 0(512-byte message length) and set the ECCType to “10”(enable 4bit ECC). ECC module generates ECC parity code for 512-byte read data. So, you have to reset ECC value by writing the InitMECC (NFCONT[5]) bit as ‘1’ and have to clear the MainECCLock (NFCONT[7]) bit to ‘0’(Unlock) before read data.
MainECCLock (NFCONT[7]) bit controls whether ECC Parity code is generated or not.

2) Whenever data is read, the 4bit ECC module generates ECC parity code internally.

3) After you complete read 512-byte (does not include spare area data), you have to read parity codes. MLC ECC module needs parity codes to detect whether error bits are or not. So you have to read ECC parity code right after read 512-byte. Once ECC parity code is read, 4bit ECC engine start to search any error internally. 4bit ECC error searching engine need minimum 155 cycles to find any error. During this time, you can continue read main data from external NAND flash memory. ECCDecDone(NFSTAT[6]) can be used to check whether ECC decoding is completed or not.

4) When ECCDecDone (NFSTAT[6]) is set (‘1’), NFECCERR0 indicates whether error bit exist or not. If any error exists, you can fix it by referencing NFECCERR0/1 and NFMLCBITPT register.

5) If you have more main data to read, continue to step 1.

6) For meta data error check, set the MsgLength to 1(24-byte message length) and set the ECCType to ‘1’(enable 4bit ECC). ECC module generates ECC parity code for 512-byte read data. So you have to reset ECC value by writing the InitMECC (NFCONT[5]) bit as ‘1’ and have to clear the MainECCLock (NFCONT[7]) bit to ‘0’(Unlock) before read data.
MainECCLock (NFCONT[7]) bit controls whether ECC Parity code is generated or not.

7) Whenever data is read, the 4bit ECC module generates ECC parity code internally.

8) After you complete read 512-byte (not include spare area data), you have to read parity codes. 4bit ECC module needs parity codes to detect whether error bits are or not. So you have to read ECC parity codes right after read 512-byte. Once ECC parity code is read, 4bit ECC engine start to search any error internally. 4bit ECC error searching engine need minimum 155 cycles to find any error. During this time, you can continue read main data from external NAND flash memory. ECCDecDone(NFSTAT[6]) can be used to check whether ECC decoding is completed or not.

9) When ECCDecDone (NFSTAT[6]) is set (‘1’), NFECCERR0 indicates whether error bit exist or not. If any error exists, you can fix it by referencing NFECCERR0/1 and NFMLCBITPT register.

8.2.3 S3C6410 8Bit ECC Programming guide (Encoding)

1) To use 8bit ECC in software mode, set the MsgLength to 0(512-byte message length) and set the ECCType to “01”(enable 8bit ECC). ECC module generates ECC parity code for 512-byte write data. So, you have to reset ECC value by writing the InitMECC (NFCONT[5]) bit as ‘1’ after clearing the MainECCLock (NFCONT[7]) bit to ‘0’(Unlock) .
MainECCLock (NFCONT[7]) bit controls whether ECC Parity code is generated or not.

   Note. In 8bit ECC, MainECCLock should be cleared before InitMECC.

2) Whenever data is written, the 8bit ECC module generates ECC parity code internally.

3) After you finish writing 512-byte data (not include spare area data), the parity codes are automatically updated to NF8MECC0, NFMECC1, NF8MECC2, NF8MECC3 register. If you use 512-byte NAND flash memory, you can program these values to spare area. However, if you use NAND flash memory more than 512-byte page, you can’t program immediately. In this case, you have to copy these parity codes to other memory like DRAM. After writing all main data, you can write the copied ECC values to spare area. The parity codes have self-correctable information include parity code itself.

4) To generate spare area ECC parity code, set the MsgLength to 1(24-byte message length), and set the ECCType to “01”(enable 8bit ECC). ECC module generates ECC parity code for 24-byte write data. So you have to reset ECC value by writing the InitMECC (NFCONT[5]) bit as ‘1’ after clearing the MainECCLock (NFCONT[7]) bit to ‘0’(Unlock.
MainECCLock (NFCONT[7]) bit controls whether ECC Parity code is generated or not.

   Note. In 8bit ECC, MainECCLock should be cleared before InitMECC.

5) Whenever data is written, the 8bit ECC module generates ECC parity code internally.

6) When you finish writing 24-byte meta or extra data, the parity codes are automatically updated to NF8MECC0, NFMECC1, NF8MECC2, NF8MECC3 register. You can program these parity codes to spare area.The parity codes have self-correctable information include parity code itself.

8.2.4 S3C6410 8bit ECC Programming guide (dEcoding)

1) To use 8bit ECC in software mode, set the MsgLength to 0(512-byte message length) and set the ECCType to “01”(enable 8bit ECC). ECC module generates ECC parity code for 512-byte read data. So, you have to reset ECC value by writing the InitMECC (NFCONT[5]) bit as ‘1’ after clearing the MainECCLock (NFCONT[7]) bit to ‘0’(Unlock.
MainECCLock (NFCONT[7]) bit controls whether ECC Parity code is generated or not.

   Note. In 8bit ECC, MainECCLock should be cleared before InitMECC

2) Whenever data is read, the MLC ECC module generates ECC parity code internally.

3) After you complete read 512-byte (does not include spare area data), you must set the MainECCLock (NFCONT[7]) bit to ‘1’(Lock) and have to read parity codes. 8bit ECC module needs parity codes to detect whether error bits are or not. So you have to read ECC parity code right after read 512-byte. Once ECC parity code is read, MLC ECC engine start to search any error internally. 8bit ECC error searching

engine need minimum 372 cycles to find any error. During this time, you can continue read main data from external NAND flash memory. ECCDecDone(NFSTAT[6]) can be used to check whether ECC decoding is completed or not.

4) When ECCDecDone (NFSTAT[6]) is set ('1'), NF8ECCERR0 indicates whether error bit exist or not. If any error exists, you can fix it by referencing NF8ECCERR0/1/2 and NFMLC8BITPT0/1 register.

5) If you have more main data to read, continue to step 1.

6) For meta data error check, set the MsgLength to 1(24-byte message length) and set the ECCType to "01"(enable 8bit ECC). ECC module generates ECC parity code for 512-byte read data. So you have to reset ECC value by writing the InitMECC (NFCONT[5]) bit as '1' after clearing the MainECCLock (NFCONT[7]) bit to '0'(Unlock).
MainECCLock (NFCONT[7]) bit controls whether ECC Parity code is generated or not.

7) Whenever data is read, the 8bit ECC module generates ECC parity code internally.

8) After you complete read 512-byte (not include spare area data), you must set the MainECCLock (NFCONT[7]) bit to '1'(Lock) and read parity codes. MLC ECC module needs parity codes to detect whether error bits are or not. So you have to read ECC parity codes right after read 512-byte. Once ECC parity code is read, 8bit ECC engine start to search any error internally. 8bit ECC error searching engine need minimum 372 cycles to find any error. During this time, you can continue read main data from external NAND flash memory. ECCDecDone(NFSTAT[6]) can be used to check whether ECC decoding is completed or not.

9) When ECCDecDone (NFSTAT[6]) is set ('1'), NF8ECCERR0 indicates whether error bit exist or not. If any error exists, you can fix it by referencing NF8ECCERR0/1/2 and NF8MLCBITPT register.

8.3 Register comparison

NAND FLASH CONFIGURATION REGISTER

Register	Address	R/W	Description	Reset Value
NFCONF	0x70200000	R/W	NAND Flash Configuration register	0x0000100X

S3C6400

NFCONF	Bit	Description	Initial State
NANDBoot	[31]	Read Only. Shows whether NAND boot or not 1=NAND Flash memory boot	0
ECCClkCon	[30]	Clock control for 4-bit ECC engine.(Hidden Spec.) 0: Recommended when system clock is more than 66MHz. 1: Recommended when system clock is less than 66MHz	0
Reserved	[29:26]	Reserved	0000

MsgLength	[25]	Message(Data) length for 4-bit ECC(for MLC NAND) 0 : 512-byte for main data area 1: 24-byte for meta data	0
ECCType	[24]	ECC type selection 0: SLC (1-bit correction) ECC 1:MLC (4-bit correction) ECC	0
Reserved	[15]	Reserved	0
TACLS	[14:12]	CLE & ALE duration setting value (0~7) Duration = HCLK x TACLS	001
Reserved	[11]	Reserved	0
TWRPH0	[10:8]	TWRPH0 duration setting value (0~7) Duration = HCLK x (TWRPH0 + 1)	000
Reserved	[7]	Reserved	0
TWRPH1	[6:4]	TWRPH1 duration setting value (0~7) Duration = HCLK x (TWRPH1 + 1)	000
AdvFlash	[3]	Advance NAND flash memory for auto-booting 0: Support 512 byte/page NAND flash memory 1: Support 2048 byte/page NAND flash memory This bit is determined by OM[2] pin status during reset and wake-up from sleep mode. This bit can be changed by software.	H/W Set
Reserved	[2]	Reserved. Must be written 1.	1
AddrCycle	[1]	NAND flash memory Address cycle for auto-booting AdvFlash AddrCycle When AdvFlash is 0, 0: 3 address cycle 1: 4 address cycle When AdvFlash is 1, 0: 4 address cycle 1: 5 address cycle This bit is determined by OM[1] pin status during reset and wake-up from sleep mode. This bit can be changed by software.	H/W Set
Reserved	[0]	Reserved. Must be written 0.	0

S3C6410

NFCONF	Bit	Description	Initial State
CfgEnbNFCON	[31]	This bit indicates whether NAND boot or not 1=NAND Flash memory boot	H/W Set * When OM[4:2] is 000, then 1.

			The other case 0.
MLCClkCtrl	[30]	Clock control for 4-bit ECC & 8-bit ECC engine.(Hidden Spec.) 0: Recommended when system clock is more than 66MHz. 1: Recommended when system clock is less than 66MHz	0
Reserved	[29:27]	Reserved	000
EnbMECC	[26]	00 : 512 byte Message Length 01 : 24 byte Message Length	0
EnbSECC	[25]		0
ECCType	**[24:23]**	This bit indicates what kind of ECC should be used. **00: 1-bit ECC** **10: 4-bit ECC** **01 : 8-bit ECC** **Note. Don't confuse the value of 4-bit ECC and 8-bit ECC.**	H/W Set (CfgBootEcc)
Reserved	[22:15]	Reserved	000000000
TACLS	[14:12]	CLE & ALE duration setting value (0~7) Duration = HCLK x TACLS	**001**
Reserved	[11]	Reserved	0
TWRPH0	[10:8]	TWRPH0 duration setting value (0~7) Duration = HCLK x (TWRPH0 + 1)	000
Reserved	[7]	Reserved	0
TWRPH1	[6:4]	TWRPH1 duration setting value (0~7) Duration = HCLK x (TWRPH1 + 1)	000
MLCFlash	[3]	This bit indicated what kind of NAND Flash memory is used. **0: SLC NAND Flash** **1: MLC NAND Flash** This bit is determined by RSMCLK pin on reset and wake-up time from sleep mode. This bit can be changed by software later.	H/W Set (CfgAdvFlash)
PageSize	[2]	This bit indicates the page size of NAND Flash Memory, which is used for auto-booting mode. When MLCFlash is 0, the value of PageSize means following: **0: 2048 Bytes/page, 1: 512 Bytes/page** When MLCFlash is 1, the value of PageSize measns following: **0: 4096 Bytes/page, 1: 2048 Bytes/page**	H/W Set (CfgPageSize)

		This bit is determined by OM[1] pin status on reset and wake-up time from sleep mode. This bit can be changed by software later.	
AddrCycle	[1]	This bit indicates the number of Address cycle of NAND Flash memory. When Page Size is 512 Bytes, 0: 3 address cycle 1: 4 address cycle When page size is 2K or 4K, 0: 4 address cycle 1: 5 address cycle This bit is determined by RSMVAD pin on reset and wake-up time from sleep mode. This bit can be changed by software later.	H/W Set (CfgAddrCycle)
BusWidth	[0]	This bit indicates the I/O bus width of NAND Flash Memory. The value of BusWidth means the followings. 0: 8-bit bus 1: 16-bit bus This bit has no meaning in NAND-boot Mode, when the I/O bus width is only 8-bit. BusWidth has effects on normal access. This bit is determined by a GPIO(Not-determined yet) pin on reset and wake-up time from sleep mode. This bit can be changed by software.	H/W Set (CfgBusWidth)

CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
NFCONT	0x70200004	R/W	NAND Flash control register	0x0384

S3C6400

NFCONT	Bit	Description	Initial State
Reserved	[31:19]	Reserved	0
ECC Direction	[18]	4-bit ECC encoding / decoding control 0: Decoding 4-bit ECC, It is used for page read 1: Encoding 4-bit ECC, It is used for page program	0
Lock-tight	[17]	Lock-tight configuration 0: Disable lock-tight 1: Enable lock-tight, Once this bit is set to 1, you cannot clear. Only reset or wake up from sleep mode can make this bit disable (cannot cleared by software). When it is set to 1, the area setting in NFSBLK	0

		(0x70200020) to NFEBLK (0x70200024)-1 is unlocked, and except this area, write or erase command will be invalid and only read command is valid. When you try to write or erase locked area, the illegal access will be occurred (NFSTAT [5] bit will be set). If the NFSBLK and NFEBLK are same, entire area will be locked.	
Soft Lock	[16]	Soft Lock configuration 0: Disable lock 1: Enable lock Soft lock area can be modified at any time by software. When it is set to 1, the area setting in NFSBLK (0x70200020) to NFEBLK (0x70200024)-1 is unlocked, and except this area, write or erase command will be invalid and only read command is valid. When you try to write or erase locked area, the illegal access will be occurred (NFSTAT [5] bit will be set). If the NFSBLK and NFEBLK are same, entire area will be locked.	1
Reserved	[15:13]	Reserved. Should be written to 0.	000
EnbECCDecINT	[12]	4-bit ECC decoding completion interrupt control 0: Disable interrupt 1: Enable interrupt	0
Reserved	[11]	Reserved	0
EnbIllegalAccINT	[10]	**Illegal access interrupt control** 0: Disable interrupt 1: Enable interrupt Illegal access interrupt will occurs when CPU tries to program or erase locking area (the area setting in NFSBLK (0x70200020) to NFEBLK (0x70200024)- 1).	0
EnbRnBINT	[9]	RnB status input signal transition interrupt control 0: Disable RnB interrupt 1: Enable RnB interrupt	0
RnB_TransMode	[8]	RnB transition detection configuration 0: Detect rising edge 1: Detect falling edge	0
MainECCLock	[7]	Lock Main area ECC generation 0: Unlock Main area ECC 1: Lock Main area ECC Main area ECC status register is NFMECC0/1(0x70200034/38),	1
SpareECCLock	[6]	Lock Spare area ECC generation. 0: Unlock Spare ECC 1: Lock Spare ECC Spare area ECC status register is NFSECC(0x7020003C),	1
InitMECC	[5]	1: Initialize main area ECC decoder/encoder (write-only)	0
InitSECC	[4]	1: Initialize spare area ECC decoder/encoder (write-only)	0

Reserved	[3]	Reserved (HW_nCE)	0
Reg_nCE1	**[2]**	NAND Flash Memory nGCS[3] signal control 0: Force nGCS[3] to low(Enable chip select) 1: Force nGCS[3] to High(Disable chip select) **Note**: Even Reg_nCE1 and Reg_nCE0 are set to zero simultaneously, only one of them is asserted.	1
Reg_nCE0	**[1]**	NAND Flash Memory nGCS[2] signal control 0: Force nGCS[2] to low(Enable chip select) 1: Force nGCS[2] to High(Disable chip select) **Note**: During boot time, it is controlled automatically. This value is only valid while MODE bit is 1	1
MODE	[0]	**NAND Flash controller operating mode** 0: NAND Flash Controller Disable (Don't work) 1: NAND Flash Controller Enable	0

S3C6410

NFCONT	Bit	Description	Initial State
Reserved	[31:19]	Reserved	0
MLCEccDirection	[18]	4-bit, 8-bitECC encoding / decoding control 0: Decoding 4-bit, 8bit ECC, It is used for page read 1: Encoding 4-bit, 8-bit ECC, It is be used for page program	0
LockTight	[17]	Lock-tight configuration 0: Disable lock-tight 1: Enable lock-tight, Once this bit is set to 1, you cannot clear this bit. Only when reset or wake up from sleep mode can this bit be cleared. (It is impossible to clear LockTight by software). When it is set to 1, the location excluding the area between NFSBLK (0x8020_0020) and NFEBLK (0x8020_0024)-1 is locked, write or erase to the area will be invalid and only read access is possible. When you try to write or erase locked area, the illegal access will be occur (NFSTAT [3] bit will be set). If the NFSBLK and NFEBLK are same, entire area will be locked.	0
LOCK	[16]	Soft Lock configuration 0: Disable lock 1: Enable lock Soft lock area can be modified at any time by software. When it is set to 1, the location excluding the area between NFSBLK (0x8020_0020) and NFEBLK (0x8020_0024)-1 is	1

		locked, write or erase to the area will be invalid and only read access is possible. When you try to write or erase locked area, the illegal access will be occur (NFSTAT [3] bit will be set). If the NFSBLK and NFEBLK are same, entire area will be locked.	
Reserved	[15:14]	Reserved	00
EnbMLCEncInt	[13]	4-bit, 8-bit ECC encoding completion interrupt control 0: Disable interrupt 1: Enable interrupt	0
EnbMLCDecInt	[12]	4-bit, 8-bit ECC decoding completion interrupt control 0: Disable interrupt 1: Enable interrupt	0
MLCStop	[11]	8-bit ECC encoding/decoding operation initialization	0
EnbIllegalAccINT	[10]	**Illegal access interrupt control** 0: Disable interrupt 1: Enable interrupt Illegal access interrupt is occurs when CPU tries to program or erase locking area (the area setting in NFSBLK (0x8020_0020) to NFEBLK (0x8020_0024)-1.	0
EnbRnBINT	[9]	RnB status input signal transition interrupt control 0: Disable RnB interrupt 1: Enable RnB interrupt	0
RnB_TransMode	[8]	RnB transition detection configuration 0: Detect rising edge 1: Detect falling edge	0
MECCLock	[7]	Lock Main area ECC generation 0: Unlock Main area ECC 1: Lock Main area ECC Main area ECC status register is NFMECC0/NFMECC1(0x8020_0034/0x8020_0038),	1
SECCLock	[6]	Lock Spare area ECC generation. 0: Unlock Spare ECC 1: Lock Spare ECC Spare area ECC status register is NFSECC(0x8020_003C),	1
InitMECC	[5]	1: Initialize main area ECC decoder/encoder (write-only)	0
InitSECC	[4]	1: Initialize spare area ECC decoder/encoder (write-only)	0
HW_nCE	[3]	Reserved (HW_nCE)	0
Reg_nCE1	**[2]**	NAND Flash Memory nRCS[3] signal control	1
Reg_nCE0	**[1]**	NAND Flash Memory nRCS[0],nRCS[2] signal control 0: Force nRCS[0],nRCS[2] to low(Enable chip select) 1: Force nRCS[0],nRCS[2] to High(Disable chip select) **Note**: During boot time, it is controlled automatically. This value is only valid while MODE bit is 1	1
MODE	[0]	**NAND Flash controller operating mode** 0: NAND Flash Controller Disable (Don't work)	0

		1: NAND Flash Controller Enable	

some registers are added for 8-bit ECC

ECC0/1/2 FOR 8BIT ECC STATUS REGISTER

Register	Address	R/W	Description	Reset Value
NF8ECCERR0	0x7020_0044	R	NAND Flash ECC Error Status register 0	0x4000_0000
NF8ECCERR1	0x7020_0048	R	NAND Flash ECC Error Status register 1	0x0000_0000
NF8ECCERR2	0x7020_004C	R	NAND Flash ECC Error Status register 2	0x0000_0000

NFECCERR0	Bit	Description	Initial State
MLC8ECCBusy	[31]	Indicates the 8-bit ECC decoding engine is searching whether a error exists or not 0: Idle 1: Busy	b'0
MLC8ECCReady	[30]	ECC Ready bit	b'1
MLC8FreePage	[29]	Inidicates the page data read from NAND flash has all 'FF' value.	b'0
MLC8ECCError	[28:25]	8-bit ECC decoding result 0000: No error 0001: 1-bit error 0010: 2-bit error 0011: 3-bit error 0100: 4-bit error 0101: 5-bit error 0110: 6-bit error 0111: 7-bit error 1000: 8-bit error 1001: Uncorrectable 1010 ~1111: reserved	b'0000
MLC8ErrLocation2	[24:15]	Error byte location of 2nd bit error	0x000
Reserved	[14:10]	Reserved	0x00
MLC8ErrLocation1	[9:0]	Error byte location of 1st bit error	0x000

Note : These values are updated when ECCDecodeDone (NFSTAT[6]) is set ('1').

NFECCERR1	Bit	Description	Initial State
MLCErrLocation5	[31:22]	Error byte location of 5th bit error	0x000
Reserved	[21]	Reserved	b'0
MLCErrLocation4	[20:11]	Error byte location of 4th bit error	0x000
Reserved	[10]	Reserved	b'0

MLCErrLocation3	[9:0]	Error byte location of 3rd bit error	0x000

Note : These values are updated when ECCDecodeDone (NFSTAT[6]) is set ('1').

NFECCERR2	Bit	Description	Initial State
MLCErrLocation8	[31:22]	Error byte location of 8th bit error	0x000
Reserved	[21]	Reserved	b'0
MLCErrLocation7	[20:11]	Error byte location of 7th bit error	0x000
Reserved	[10]	Reserved	b'0
MLCErrLocation6	[9:0]	Error byte location of 6th bit error	0x000

Note : These values are updated when ECCDecodeDone (NFSTAT[6]) is set ('1').

MAIN DATA AREA ECC0 STATUS REGISTER

Register	Address	R/W	Description	Reset Value
NFM8ECC0	0x7020_0050	R	8bit ECC status register	0x0000_0000
NFM8ECC1	0x7020_0054	R	8bit ECC status register	0x0000_0000
NFM8ECC2	0x7020_0058	R	8bit ECC status register	0x0000_0000
NFM8ECC3	0x7020_005C	R	8bit ECC status register	0xXXXXXX

NFM8ECC0	Bit	Description	Initial State
4th Parity	[31:24]	4th Check Parity generated from main area (512-byte)	0x00
3rd Parity	[23:16]	3rd Check Parity generated from main area (512-byte)	0x00
2nd Parity	[15:8]	2nd Check Parity generated from main area (512-byte)	0x00
1st Parity	[7:0]	1st Check Parity generated from main area (512-byte)	0x00

NFM8ECC1	Bit	Description	Initial State
8th Parity	[31:24]	8th Check Parity generated from main area (512-byte)	0x00
7th Parity	[23:16]	7th Check Parity generated from main area (512-byte)	0x00
6th Parity	[15:8]	6th Check Parity generated from main area (512-byte)	0x00
5th Parity	[7:0]	5th Check Parity generated from main area (512-byte)	0x00

NFM8ECC2	Bit	Description	Initial State
12th Parity	[31:24]	12th Check Parity generated from main area (512-byte)	0x00
11th Parity	[23:16]	11th Check Parity generated from main area (512-byte)	0x00
10th Parity	[15:8]	10th Check Parity generated from main area (512-byte)	0x00
9th Parity	[7:0]	9th Check Parity generated from main area (512-byte)	0x00

NFM8ECC3	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0x000000

13th Parity	[7:0]	13th Check Parity generated from main area (512-byte)	0x00

Note: The NAND flash controller generate these ECC parity codes when write main area data while the MainECCLock (NFCON[7]) bit is '0'(unlock).

MLC 8-BIT ECC ERROR PATTEN REGISTER

Register	Address	R/W	Description	Reset Value
NFMLC8BITPT0	0x7020_0060	R	NAND Flash 8-bit ECC Error Pattern register0 for data[7:0]	0x0000_0000
NFMLC8BITPT1	0x7020_0064	R	NAND Flash 8-bit ECC Error Pattern register1 for data[7:0]	0x0000_0000

NFMLC8BITPT0	Bit	Description	Initial State
4th Error bit pattern	[31:24]	4th Error bit pattern	0x00
3rd Error bit pattern	[23:16]	3rd Error bit pattern	0x00
2nd Error bit pattern	[15:8]	2nd Error bit pattern	0x00
1st Error bit pattern	[7:0]	1st Error bit pattern	0x00

NFMLC8BITPT1	Bit	Description	Initial State
8th Error bit pattern	[31:24]	8th Error bit pattern	0x00
7th Error bit pattern	[23:16]	7th Error bit pattern	0x00
6th Error bit pattern	[15:8]	6th Error bit pattern	0x00
5th Error bit pattern	[7:0]	5th Error bit pattern	0x00

9. CFCON

9.1 Difference summary

There in no change

10. GPIO

10.1 Difference summary

Additional I2C Interface are muxed with GPB[3:2]

I2S 5.1CH interface are muxed with GPC7, GPC[5:4], GPH[9:6]

Additional ATA Control signals are muxed with GPL

Additional Memory Port0 Address[19:16]

10.2 Register comparison

GPBCON	Bit	Description		Initial State
GPB0	[3:0]	0000 = Input 0010 = UART RXD[2] 0100 = IrDA RXD 0110 = Reserved	0001 = Output 0011 = Ext. DMA Request 0101 = ADDR_CF[0] 0111 = External Interrupt Group 1[8]	0000
GPB1	[7:4]	0000 = Input 0010 = UART TXD[2] 0100 = IrDA TXD 0110 = Reserved	0001 = Output 0011 = Ext. DMA Ack 0101 = ADDR_CF[1] 0111 = External Interrupt Group 1[9]	0000
GPB2	[11:8]	0000 = Input 0010 = UART RXD[3] 0100 = Ext. DMA Req 0110 = I2C SCL[1]	0001 = Output 0011 = IrDA RXD 0101 = ADDR_CF[2] 0111 = External Interrupt Group 1[10]	0000
GPB3	[15:12]	0000 = Input 0010 = UART TXD[3] 0100 = Ext. DMA Ack 0110 = I2C SDA[1]	0001 = Output 0011 = Irda TXD 0101 = Reserved 0111 = External Interrupt Group 1[11]	0000
GPB4	[19:16]	0000 = Input 0010 = IrDA SDBW 0100 = CF Data DIR 0110 = Reserved	0001 = Output 0011 = CAM FIELD 0101 = Reserved 0111 = External Interrupt Group 1[12]	0000
GPB5	[23:20]	0000 = Input 0010 = I2C SCL[0] 0100 = Reseved 0110 = Reserved	0001 = Output 0011 = reserved 0101 = Reserved 0111 = External Interrupt Group 1[13]	0000
GPB6	[27:24]	0000 = Input 0010 = I2C SDA[0] 0100 = Reseved 0110 = Reserved	0001 = Output 0011 = reserved 0101 = Reserved 0111 = External Interrupt Group 1[14]	0000

GPCCON	Bit	Description	
GPC0	[3:0]	0000 = Input 0010 = SPI MISO[0] 0100 = Reserved 0110 = Reserved	0001 = Output 0011 = reserved 0101 = ADDR_CF[0] 0111 = External Interrupt Group 2[0]
GPC1	[7:4]	0000 = Input 0010 = SPI CLK[0] 0100 = Reserved 0110 = Reserved	0001 = Output 0011 = reserved 0101 = ADDR_CF[1] 0111 = External Interrupt Group 2[1]
GPC2	[11:8]	0000 = Input 0010 = SPI MOSI[0] 0100 = Reserved 0110 = Reserved	0001 = Output 0011 = reserved 0101 = ADDR_CF[2] 0111 = External Interrupt Group 2[2]
GPC3	[15:12]	0000 = Input 0010 = SPI CSn[0] 0100 = Reserved 0110 = Reserved	0001 = Output 0011 = reserved 0101 = Reserved 0111 = External Interrupt Group 2[3]
GPC4	[19:16]	0000 = Input 0010 = SPI MISO[1] 0100 = Reserved 0110 = Reserved	0001 = Output 0011 = MMC CMD2 0101 = I2S_V40 DO[0] 0111 = External Interrupt Group 2[4]
GPC5	[23:20]	0000 = Input 0010 = SPI CLK[1] 0100 = Reserved 0110 = Reserved	0001 = Output 0011 = MMC CLK2 0101 = I2S_V40 DO[1] 0111 = External Interrupt Group 2[5]
GPC6	[27:24]	0000 = Input 0010 = SPI MOSI[1] 0100 = Reserved 0110 = Reserved	0001 = Output 0011 = reserved 0101 = Reserved 0111 = External Interrupt Group 2[6]
GPC7	[31:28]	0000 = Input 0010 = SPI CSn[1] 0100 = Reserved 0110 = Reserved	0001 = Output 0011 = reserved 0101 = I2S_V40 DO[2] 0111 = External Interrupt Group 2[7]

GPHCON0	Bit	Description		Initial State
GPH0	[3:0]	0000 = Input 0010 = MMC CLK1 0100 = Key pad COL[0] 0110 = Reserved	0001 = Output 0011 = reserved 0101 = ADDR_CF[0] 0111 = External Interrupt Group 6[0]	0000
GPH1	[7:4]	0000 = Input 0010 = MMC CMD1 0100 = Key pad COL[1] 0110 = Reserved	0001 = Output 0011 = reserved 0101 = ADDR_CF[1] 0111 = External Interrupt Group 6[1]	0000
GPH2	[11:8]	0000 = Input 0010 = MMC DATA1[0] 0100 = Key pad COL[2]	0001 = Output 0011 = reserved 0101 = ADDR_CF[2]	0000

		0110 = Reserved 0111 = External Interrupt Group 6[2]	
GPH3	[15:12]	0000 = Input 0001 = Output 0010 = MMC DATA1[1] 0011 = reserved 0100 = Key pad COL[3] 0101 = Reserved 0110 = Reserved 0111 = External Interrupt Group 6[3]	0000
GPH4	[19:16]	0000 = Input 0001 = Output 0010 = MMC DATA1[2] 0011 = reserved 0100 = Key pad COL[4] 0101 = Reserved 0110 = Reserved 0111 = External Interrupt Group 6[4]	0000
GPH5	[23:20]	0000 = Input 0001 = Output 0010 = MMC DATA1[3] 0011 = reserved 0100 = Key pad COL[5] 0101 = Reserved 0110 = Reserved 0111 = External Interrupt Group 6[5]	0000
GPH6	[27:24]	0000 = Input 0001 = Output 0010 = MMC DATA1[4] 0011 = MMC DATA2[0] 0100 = Key pad COL[6] 0101 = I2S_V40 BCLK 0110 = ADDR_CF[0] 0111 = External Interrupt Group 6[6]	0000
GPH7	[31:28]	0000 = Input 0001 = Output 0010 = MMC DATA1[5] 0011 = MMC DATA2[1] 0100 = Key pad COL[7] 0101 = I2S_V40 CDCLK 0110 = ADDR_CF[1] 0111 = External Interrupt Group 6[7]	0000

GPHCON1	Bit	Description	Initial State
GPH8	[3:0]	0000 = Input 0001 = Output 0010 = MMC DATA1[6] 0011 = MMC DATA2[2] 0100 = Reserved 0101 = I2S_V40 LRCLK 0110 = ADDR_CF[2] 0111 = External Interrupt Group 6[8]	0000
GPH9	[7:4]	0000 = Input 0001 = Output 0010 = MMC DATA1[7] 0011 = MMC DATA2[3] 0100 = Reserved 0101 = I2S_V40 DI 0110 = Reserved 0111 = External Interrupt Group 6[9]	0000

GPLCON0	Bit	Description	Initial State
GPL0	[3:0]	0000 = Input 0001 = Output 0010 = Host I/F ADDR[0] 0011 = Key pad COL[0] 0100 = Reserved 0101 = Reserved 0110 = ADDR_CF[0] 0111 = OTG ULPI DATA[0]	0010
GPL1	[7:4]	0000 = Input 0001 = Output 0010 = Host I/F ADDR[1] 0011 = Key pad COL[1] 0100 = Reserved 0101 = Reserved 0110 = ADDR_CF[1] 0111 = OTG ULPI DATA[1]	0010
GPL2	[11:8]	0000 = Input 0001 = Output 0010 = Host I/F ADDR[2] 0011 = Key pad COL[2] 0100 = Reserved 0101 = Reserved 0110 = ADDR_CF[2] 0111 = OTG ULPI DATA[2]	0010
GPL3	[15:12]	0000 = Input 0001 = Output	0010

		0010 = Host I/F ADDR[3] 0100 = Reserved 0110 = MEM0_INTata	0011 = Key pad COL[3] 0101 = Reserved 0111 = OTG ULPI DATA[3]	
GPL4	[19:16]	0000 = Input 0010 = Host I/F ADDR[4] 0100 = Reserved 0110 = MEM0_RESETata	0001 = Output 0011 = Key pad COL[4] 0101 = Reserved 0111 = OTG ULPI DATA[4]	0010
GPL5	[23:20]	0000 = Input 0010 = Host I/F ADDR[5] 0100 = Reserved 0110 = MEM0_INPACKata	0001 = Output 0011 = Key pad COL[5] 0101 = Reserved 0111 = OTG ULPI DATA[5]	0010
GPL6	[27:24]	0000 = Input 0010 = Host I/F ADDR[6] 0100 = Reserved 0110 = MEM0_REGata	0001 = Output 0011 = Key pad COL[6] 0101 = Reserved 0111 = OTG ULPI DATA[6]	0010
GPL7	[31:28]	0000 = Input 0010 = Host I/F ADDR[7] 0100 = Reserved 0110 = MEM0_CData	0001 = Output 0011 = Key pad COL[7] 0101 = Reserved 0111 = OTG ULPI DATA[7]	0010

GPLCON1	Bit	Description		Initial State
GPL8	[3:0]	0000 = Input 0010 = Host I/F ADDR[8] 0100 = Reserved 0110 = Reserved	0001 = Output 0011 = Ext. Interrupt[16] 0101 = CE_CF[0] 0111 = OTG ULPI STP	0010
GPL9	[7:4]	0000 = Input 0010 = Host I/F ADDR[9] 0100 = Reserved 0110 = Reserved	0001 = Output 0011 = Ext. Interrupt [17] 0101 = CE_CF[1] 0111 = OTG ULPI CLK	0010
GPL10	[11:8]	0000 = Input 0010 = Host I/F ADDR[10] 0100 = Reserved 0110 = Reserved	0001 = Output 0011 = Ext. Interrupt [18] 0101 = IORD_CF 0111 = OTG ULPI NXT	0010
GPL11	[15:12]	0000 = Input 0010 = Host I/F ADDR[11] 0100 = Reserved 0110 = Reserved	0001 = Output 0011 = Ext. Interrupt [19] 0101 = IOWR_CF 0111 = OTG ULPI DIR	0010
GPL12	[19:16]	0000 = Input 0010 = Host I/F ADDR[12] 0100 = Reserved 0110 = Reserved	0001 = Output 0011 = Ext. Interrupt [20] 0101 = IORDY_CF 0111 = Reserved	0010
GPL13	[23:20]	0000 = Input 0010 = Host I/F DATA[16] 0100 = Reserved 0110 = Reserved	0001 = Output 0011 = Ext. Interrupt [21] 0101 = DATA_CF[8] 0111 = Reserved	0010
GPL14	[27:24]	0000 = Input	0001 = Output	0010

		0010 = Host I/F DATA[17] 0011 = Ext. Interrupt [22] 0100 = Reserved 0101 = DATA_CF[9] 0110 = Reserved 0111 = Reserved	

GPQCON	Bit	Description	Initial State
GPQ0	[1:0]	00 = Input 01 = Output 10 = MEM0_ADDR18_RAS 11 = Ext. Interrupt Group9[0]	10
GPQ1	[3:2]	00 = Input 01 = Output 10 = MEM0_ADDR19_CAS 11 = Ext. Interrupt Group9[1]	10
GPQ2	[5:4]	00 = Input 01 = Output 10 = MEM0_SCLK 11 = Ext. Interrupt Group9 [2]	10
GPQ3	[7:6]	00 = Input 01 = Output 10 = MEM0_SCLKn 11 = Ext. Interrupt Group9 [3]	10
GPQ4	[9:8]	00 = Input 01 = Output 10 = MEM0_SCKE 11 = Ext. Interrupt Group9 [4]	10
GPQ5	[11:10]	00 = Input 01 = Output 10 = MEM0_DQS[0] 11 = Ext. Interrupt Group9 [5]	10
GPQ6	[13:12]	00 = Input 01 = Output 10 = MEM0_DQS[1] 11 = Ext. Interrupt Group9 [6]	10
GPQ7	[15:14]	00 = Input 01 = Output 10 = MEM0_ADDR17_WEndmc 11 = Ext. Interrupt Group9 [7]	10
GPQ8	[17:16]	00 = Input 01 = Output 10 = MEM0_ADDR16_APdmc 11 = Ext. Interrupt Group9 [8]	10

11. DMAC

11.1 Request Source

S3C6400 DMA REQUEST SOURCE

DMA sources for each channel are as follows

Bit	Source	Bit	Source	Bit	Source	Bit	Source
0	UART_0[0]	8	PCM0 TX	16	PCM1 TX	24	AC_MICIN
1	UART_0[1]	9	PCM0 RX	17	PCM1 RX	25	PWM
2	UART_1[0]	10	I2S0 TX	18	I2S1 TX	26	IrDA
3	UART_1[1]	11	I2S0 RX	19	I2S1 RX	27	External
4	UART_2[0]	12	SPI0_TX	20	SPI1_TX	28	Reserved
5	UART_2[1]	13	SPI0_RX	21	SPI1_RX	29	Reserved
6	UART_3[0]	14	MIPI_HSI_TX	22	ACPCM_OUT	30	Security RX
7	UART_3[1]	15	MIPI_HSI_RX	23	ACPCM_IN	31	Security TX

S3C6410 DMA REQUEST SOURCE

DMA sources for each channel are as follows

Bit	Source	Bit	Source	Bit	Source	Bit	Source
0	UART_0[0]	8	PCM0 TX	16	PCM1 TX	24	AC_MICIN
1	UART_0[1]	9	PCM0 RX	17	PCM1 RX	25	PWM
2	UART_1[0]	10	I2S0 TX	18	I2S1 TX	26	IrDA
3	UART_1[1]	11	I2S0 RX	19	I2S1 RX	27	External
4	UART_2[0]	12	SPI0_TX	20	SPI1_TX	28	RESERVED
5	UART_2[1]	13	SPI0_RX	21	SPI1_RX	29	Reserved
6	UART_3[0]	14	I2S_V40 TX	22	ACPCM_OUT	30	Security RX
7	UART_3[1]	15	I2S_V40 RX	23	ACPCM_IN	31	Security TX

11.2 Register comparison

DMACCxConfiguration

@S3C6400

Reserved (OneNandModeDst)	[10]	R/W	For channel 3, this bit is used to support page-write features for OneNAND Controller. If this bit is set to 1 and the destination address points the address field of OneNAND Controller, destination address increment setting can support 01 command of OneNAND Controller. When this bit is set, following fields in DMACCxControl0 should be set as follows DBSize : greater than or equal to 3'b001 SWidth : should be 3'b010 DWidth : should be 3'b010 DI : should be 1 For other channels, this bit is reserved and must be written as zero, masked on read.
Reserved **(OneNandModeSrc)**	**[5]**	**R/W**	For channel 3, this bit is used to support page-read features for OneNAND Controller. If this bit is set to 1 and the source address points the address field of OneNAND Controller, source address increment setting can support 01 command of OneNAND Controller. When this bit is set, following fields in DMACCxControl0 should be set as follows SBSize : greater than or equal to 3'b001 SWidth : should be 3'b010 DWidth : should be 3'b010 SI : should be 1 For channel 7, this bit is used to support bypass HGRANT operation Enable bit to enhance bus performance . For other channels, this bit is reserved and must be written as zero, masked on read.

@S3C6410

OneNandModeDst	[10]	R/W	This bit is used to support page-write features for OneNAND Controller. If this bit is set to 1 and the destination address points the address field of OneNAND Controller, destination address increment setting can support 01 command of OneNAND Controller. When this bit is set, following fields in DMACCxControl0 should be set as follows DBSize : greater than or equal to 3'b001 SWidth : should be 3'b010 DWidth : should be 3'b010 DI : should be 1

OneNandModeSrc	**[5]**	**R/W**	This bit is used to support page-read features for OneNAND Controller. If this bit is set to 1 and the source address points the address field of OneNAND Controller, source address increment setting can support 01 command of OneNAND Controller. When this bit is set, following fields in DMACCxControl0 should be set as follows SBSize : greater than or equal to 3'b001 SWidth : should be 3'b010 DWidth : should be 3'b010 SI : should be 1

New SFR @S3C6410

Channel configuration expansion register, DMACCxConfigurationExp

The eight DMACCxConfigurationExp registers are read/write and are used to configure the DMA channel additionally.

Table 11-25 shows the bit assignment of a DMACCxConfigurationExp register.

Table 11-25. Bit Assignment of DMACCxConfigurationExp register

DMACCxConfiguration Exp	Bits	Type	Function
PeriReqSel	[2:1]	R/W	Peripheral DMA Request for Mem-to-Mem Access Selection : 00 = MODEM_IF TX 0 Request 01 = MODEM_IF TX 1 Request 10 = MODEM_IF RX 0 Request 11 = MODEM_IF RX 1 Request
EnPeriReq	[0]	R/W	Enable for Peripheral DMA Request: 0 = Disable 1 = Enable This value can be used in Peripheral for Mem-to-Mem access not Peri-to-Mem access.

12. VECTORED INTERRUPT CONTROLLER(VIC)

12. Difference summary

S3C6410 supports 60 Interrupt Source

Differences with others(S3C6400, S3C6410)

Function	S3C6400	S3C6410
Interrupt Source	60	64

12.1 Register compare bit by bit

S3C6410 has 2 Vectored Interrupt Controllers

S3C6400 INTERRUPT REQUEST SOURCE

Interrupt sources for each channel are as follows

Int. No.	Sources	Description	Group
63	INT_ADC	ADC EOC interrupt	TZIC1, VIC1
62	INT_PENDN	ADC Pen down interrupt	TZIC1, VIC1
61	INT_SEC	Security interrupt	TZIC1, VIC1
60	INT_RTC_ALARM	RTC alarm interrupt	TZIC1, VIC1
59	INT_IrDA	IrDA interrupt	TZIC1, VIC1
58	INT_OTG	USB OTG interrupt	TZIC1, VIC1
57	INT_HSMMC1	HSMMC1 interrupt	TZIC1, VIC1
56	INT_HSMMC0	HSMMC0 interrupt	TZIC1, VIC1
55	INT_HOSTIF	Host Interface interrupt	TZIC1, VIC1
54	INT_MSM	MSM modem I/F interrupt	TZIC1, VIC1
53	INT_EINT4	External interrupt Group 1 ~ Group 9	TZIC1, VIC1
52	INT_HSIrx	HSI Rx interrupt	TZIC1, VIC1
51	INT_HSItx	HSI Tx interrupt	TZIC1, VIC1
50	INT_I2C	I2C interrupt	TZIC1, VIC1
49	INT_SPI1	SPI1 interrupt or HSMMC2 interrupt	TZIC1, VIC1
48	INT_SPI0	SPI0 interrupt	TZIC1, VIC1
47	INT_UHOST	USB Host interrupt	TZIC1, VIC1
46	INT_CFC	CFCON interrupt	TZIC1, VIC1
45	INT_NFC	NFCON interrupt	TZIC1, VIC1

44	INT_ONENAND1	OneNAND interrupt from bank 1	TZIC1, VIC1
43	INT_ONENAND0	OneNAND interrupt from bank 0	TZIC1, VIC1
42	INT_DMA1	DMA1 interrupt	TZIC1, VIC1
41	INT_DMA0	DMA0 interrupt	TZIC1, VIC1
40	INT_UART3	UART3 interrupt	TZIC1, VIC1
39	INT_UART2	UART2 interrupt	TZIC1, VIC1
38	INT_UART1	UART1 interrupt	TZIC1, VIC1
37	INT_UART0	UART0 interrupt	TZIC1, VIC1
36	INT_AC97	AC97 interrupt	TZIC1, VIC1
35	INT_PCM1	PCM1 interrupt	TZIC1, VIC1
34	INT_PCM0	PCM0 interrupt	TZIC1, VIC1
33	INT_EINT3	External interrupt 20 ~ 27	TZIC1, VIC1
32	INT_EINT2	External interrupt 12 ~ 19	TZIC1, VIC1
31	INT_LCD[2]	LCD interrupt System I/F done	TZIC0, VIC0
30	INT_LCD[1]	LCD interrupt VSYNC interrupt	TZIC0, VIC0
29	INT_LCD[0]	LCD interrupt FIFO underrun	TZIC0, VIC0
28	INT_TIMER4	Timer 4 interrupt	TZIC0, VIC0
27	INT_TIMER3	Timer 3 interrupt	TZIC0, VIC0
26	INT_WDT	Watchdog timer interrupt	TZIC0, VIC0
25	INT_TIMER2	Timer 2 interrupt	TZIC0, VIC0
24	INT_TIMER1	Timer 1 interrupt	TZIC0, VIC0
23	INT_TIMER0	Timer 0 interrupt	TZIC0, VIC0
22	INT_KEYPAD	Keypad interrupt	TZIC0, VIC0
21	INT_ARM_DMAS	ARM DMAS interrupt	TZIC0, VIC0
20	INT_ARM_DMA	ARM DMA interrupt	TZIC0, VIC0
19	INT_ARM_DMAERR	ARM DMA Error interrupt	TZIC0, VIC0
18	INT_SDMA1	Secure DMA1 interrupt	TZIC0, VIC0
17	INT_SDMA0	Secure DMA0 interrupt	TZIC0, VIC0
16	INT_MFC	MFC interrupt	TZIC0, VIC0
15	INT_JPEG	JPEG interrupt	TZIC0, VIC0
14	INT_BATF	Battery fault interrupt	TZIC0, VIC0
13	INT_SCALAR	TV Scalar interrupt	TZIC0, VIC0
12	INT_TVENC	TV Encoder interrupt	TZIC0, VIC0
11	INT_2D	2D interrupt	TZIC0, VIC0
10	INT_ROTATOR	Rotator interrupt	TZIC0, VIC0
9	INT_POST0	Post processor interrupt	TZIC0, VIC0
8	Reserved	-	TZIC0, VIC0

7	Reserved	-	TZIC0, VIC0
6	Reserved	-	TZIC0, VIC0
5	Reserved	-	TZIC0, VIC0
4	INT_CAMIF_P	Camera interface interrupt	TZIC0, VIC0
3	INT_CAMIF_C	Camera interface interrupt	TZIC0, VIC0
2	INT_RTC_TIC	RTC TIC interrupt	TZIC0, VIC0
1	INT_EINT1	External interrupt 4 ~ 11	TZIC0, VIC0
0	INT_EINT0	External interrupt 0 ~ 3	TZIC0, VIC0

S3C6410 INTERRUPT REQUEST SOURCE

Interrupt sources for each channel are as follows

Int. No.	Sources	Description	Group
63	INT_ADC	ADC EOC interrupt	TZIC1, VIC1
62	INT_PENDN	ADC Pen down interrupt	TZIC1, VIC1
61	INT_SEC	Security interrupt	TZIC1, VIC1
60	INT_RTC_ALARM	RTC alarm interrupt	TZIC1, VIC1
59	INT_IrDA	IrDA interrupt	TZIC1, VIC1
58	INT_OTG	USB OTG interrupt	TZIC1, VIC1
57	INT_HSMMC1	HSMMC1 interrupt	TZIC1, VIC1
56	INT_HSMMC0	HSMMC0 interrupt	TZIC1, VIC1
55	INT_HOSTIF	Host Interface interrupt	TZIC1, VIC1
54	INT_MSM	MSM modem I/F interrupt	TZIC1, VIC1
53	INT_EINT4	External interrupt Group 1 ~ Group 9	TZIC1, VIC1
52	INT_HSIrx	HSI Rx interrupt	TZIC1, VIC1
51	INT_HSItx	HSI Tx interrupt	TZIC1, VIC1
50	INT_I2C0	I2C0 interrupt	TZIC1, VIC1
49	INT_SPI1	SPI1 interrupt or HSMMC2 interrupt	TZIC1, VIC1
48	INT_SPI0	SPI0 interrupt	TZIC1, VIC1
47	INT_UHOST	USB Host interrupt	TZIC1, VIC1
46	INT_CFC	CFCON interrupt	TZIC1, VIC1
45	INT_NFC	NFCON interrupt	TZIC1, VIC1
44	INT_ONENAND1	OneNAND interrupt from bank 1	TZIC1, VIC1
43	INT_ONENAND0	OneNAND interrupt from bank 0	TZIC1, VIC1
42	INT_DMA1	DMA1 interrupt	TZIC1, VIC1
41	INT_DMA0	DMA0 interrupt	TZIC1, VIC1
40	INT_UART3	UART3 interrupt	TZIC1, VIC1

39	INT_UART2	UART2 interrupt	TZIC1, VIC1
38	INT_UART1	UART1 interrupt	TZIC1, VIC1
37	INT_UART0	UART0 interrupt	TZIC1, VIC1
36	INT_AC97	AC97 interrupt	TZIC1, VIC1
35	INT_PCM1	PCM1 interrupt	TZIC1, VIC1
34	INT_PCM0	PCM0 interrupt	TZIC1, VIC1
33	INT_EINT3	External interrupt 20 ~ 27	TZIC1, VIC1
32	INT_EINT2	External interrupt 12 ~ 19	TZIC1, VIC1
31	INT_LCD[2]	LCD interrupt System I/F done	TZIC0, VIC0
30	INT_LCD[1]	LCD interrupt VSYNC interrupt	TZIC0, VIC0
29	INT_LCD[0]	LCD interrupt FIFO underrun	TZIC0, VIC0
28	INT_TIMER4	Timer 4 interrupt	TZIC0, VIC0
27	INT_TIMER3	Timer 3 interrupt	TZIC0, VIC0
26	INT_WDT	Watchdog timer interrupt	TZIC0, VIC0
25	INT_TIMER2	Timer 2 interrupt	TZIC0, VIC0
24	INT_TIMER1	Timer 1 interrupt	TZIC0, VIC0
23	INT_TIMER0	Timer 0 interrupt	TZIC0, VIC0
22	INT_KEYPAD	Keypad interrupt	TZIC0, VIC0
21	INT_ARM_DMAS	ARM DMAS interrupt	TZIC0, VIC0
20	INT_ARM_DMA	ARM DMA interrupt	TZIC0, VIC0
19	INT_ARM_DMAERR	ARM DMA Error interrupt	TZIC0, VIC0
18	INT_SDMA1	Secure DMA1 interrupt	TZIC0, VIC0
17	INT_SDMA0	Secure DMA0 interrupt	TZIC0, VIC0
16	INT_MFC	MFC interrupt	TZIC0, VIC0
15	INT_JPEG	JPEG interrupt	TZIC0, VIC0
14	INT_BATF	Battery fault interrupt	TZIC0, VIC0
13	INT_SCALAR	TV Scalar interrupt	TZIC0, VIC0
12	INT_TVENC	TV Encoder interrupt	TZIC0, VIC0
11	INT_2D	2D interrupt	TZIC0, VIC0
10	INT_ROTATOR	Rotator interrupt	TZIC0, VIC0
9	INT_POST0	Post processor interrupt	TZIC0, VIC0
8	INT_3D	FIMG_3D interrupt	TZIC0, VIC0
7	RESERVED	RESERVED	TZIC0, VIC0
6	INT_I2S_V40	I2S_V40 interrupt	TZIC0, VIC0
5	INT_I2C1	I2C1 interrupt	TZIC0, VIC0
4	INT_CAMIF_P	Camera interface interrupt	TZIC0, VIC0
3	INT_CAMIF_C	Camera interface interrupt	TZIC0, VIC0

2	INT_RTC_TIC	RTC TIC interrupt	TZIC0, VIC0
1	INT_EINT1	External interrupt 4 ~ 11	TZIC0, VIC0
0	INT_EINT0	External interrupt 0 ~ 3	TZIC0, VIC0

13. SECURITY SUBSYSTEM

13.1 Difference summary

There in no change

14. DISPLAY CONTROLLER

14.1 Difference summary

ITU BT.601/656 interface

CSC function (precision 향상)

VCLK freerun Mode support

Bug fix related FRM signal

Addition of the synchronous clock for the local interface to CAMIF.

14.1.1 IP version

FIMC 4.2.1

14.2 ITU-R BT.601/656 interface spec

Name	Type	Source/Destination	Description
V601_CLK	Output	Pad	ITU 601 data clock
*VEN_HREF	Output	Pad	DATA Enable
**VEN_VSYNC	Output	Pad	Vertical Sync Signal
VEN_HSYNC	Output	Pad	Horizontal Sync Signal
**VEN_FIELD	Output	Pad	FIELD Signal (option)
VEN_DATA[7:0]	Output	Pad	ITU601 YUV422 format data output
V656_CLK	Output	Pad	ITU 656 data clock
V656_DATA[7:0]	Output	Pad	ITU656 YUV422 format data output

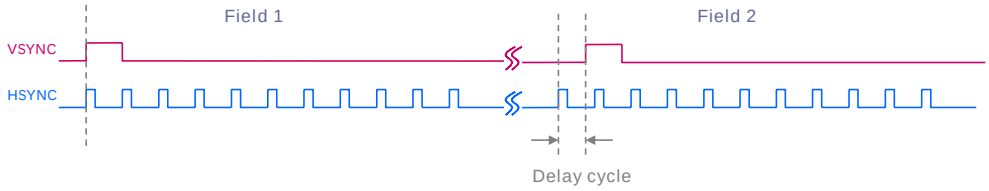
Table .1. Indirect I80 Interface Pin Description

* VEN_HREF : DATA Blank (when I601HREF[0] = 1)

DATA Enable (when I601HREF[0] = 0)

** VEN_VSYNC, VEN_FIELD (field information in interlace mode)

When SELVSYNC[0] = 1, Delay Cycle = DLYVSYNC[7:0] + 1



When SELVSYNC[0] = 0,

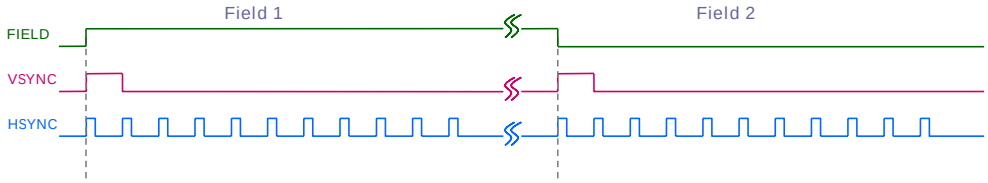


Figure 1. ITU-R BT.601 Controllable Vsync

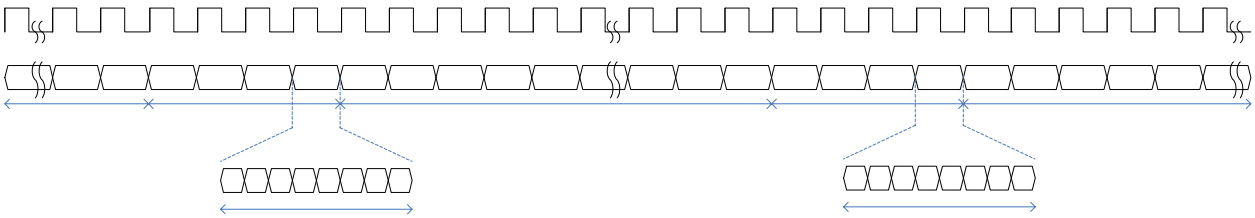


Figure 2. ITU-R BT.656 interface Timing

bit		
[7]	1	
[6]	F	0 : during Field 1 1 : during Field 2
[5]	V	0 : elsewhere 1 : during field blanking
[4]	H	0 : in SAV 1 : in EAV
[3]	P3	V ^ H

CLK

V656_DATA FF 00 00 XY Y Cb Y Cr Y

1 F V H P3 P2 P1 P0

[2]	P2	F ^ H
[1]	P1	F ^ V
[0]	P0	F ^ V ^ H

Table 2. Timing Reference Code (XY definition)

14.3 LCD DATA PIN MAP

	Parallel RGB			Serial RGB		I80 CPU I/F		601/656
	24BPP (888)	18BPP (666)	16BPP (565)	24BPP (888)	16BPP (666)	18BPP (666)	16BPP (565)	
VD[23]	R[7]	R[5]	R[4]	D[7]	D[5]	-	-	
VD[22]	R[6]	R[4]	R[3]	D[6]	D[4]	-	-	
VD[21]	R[5]	R[3]	R[2]	D[5]	D[3]	-	-	
VD[20]	R[4]	R[2]	R[1]	D[4]	D[2]	-	-	
VD[19]	R[3]	R[1]	R[0]	D[3]	D[1]	-	-	
VD[18]	R[2]	R[0]	-	D[2]	D[0]	-	-	
VD[17]	R[1]	-	-	D[1]	-	R[5]	-	
VD[16]	R[0]	-	-	D[0]	-	R[4]	-	
VD[15]	G[7]	G[5]	G[5]	-	-	R[3]	R[4]	V656_DATA[7]
VD[14]	G[6]	G[4]	G[4]	-	-	R[2]	R[3]	V656_DATA[6]
VD[13]	G[5]	G[3]	G[3]	-	-	R[1]	R[2]	V656_DATA[5]

VD[12]	G[4]	G[2]	G[2]	-	-	R[0]	R[1]	V656_DATA[4]
VD[11]	G[3]	G[1]	G[1]	-	-	G[5]	R[0]	V656_DATA[3]
VD[10]	G[2]	G[0]	G[0]	-	-	G[4]	G[5]	V656_DATA[2]
VD[9]	G[1]	-	-	-	-	G[3]	G[4]	V656_DATA[1]
VD[8]	G[0]	-	-	-	-	G[2]	G[3]	V656_DATA[0]
VD[7]	B[7]	B[5]	B[4]	-	-	G[1]	G[2]	VEN_DATA[7]
VD[6]	B[6]	B[4]	B[3]	-	-	G[0]	G[1]	VEN_DATA[6]
VD[5]	B[5]	B[3]	B[2]	-	-	B[5]	G[0]	VEN_DATA[5]
VD[4]	B[4]	B[2]	B[1]	-	-	B[4]	B[4]	VEN_DATA[4]
VD[3]	B[3]	B[1]	B[0]	-	-	B[3]	B[3]	VEN_DATA[3]
VD[2]	B[2]	B[0]	-	-	-	B[2]	B[2]	VEN_DATA[2]
VD[1]	B[1]	-	-	-		B[1]	B[1]	VEN_DATA[1]
VD[0]	B[0]	-	-	-	-	B[0]	B[0]	VEN_DATA[0]

14.4 Register comparison

14.4.1 Video Main Control 0 Register

Register	Address	R/W	Description	Reset Value
VIDCON0	0x77100000	R/W	Video control 0 register	0x0000_0000

6400

VIDCON0	Bit	Description	Initial State
-	[31:30]	Reserved	0
INTERLACE_F	[29]	Interlace or Progressive 0 : Progressive 1: Interlace	0
-	[28]	Reserved (Should be zero)	0
VIDOUT	[27:26]	It determines the output format of Video Controller 00: RGB I/F 01: TV Encoder Interface 10: I80 CPU I/F for LDI0 11: I80 CPU I/F for LDI1	00
L1_DATA16	[25:23]	Select the mode of output data format of I80 CPU I/F (LDI1.) (Only when, VIDOUT[1:0] == 2'b11) 000 = 16 bit mode (16 BPP) 001 = 16 + 2 bit mode (18 BPP) 010 = 9 + 9 bit mode (18 BPP) 011 = 16 + 8 bit mode (24 BPP) 100 = 18 bit mode (18BPP) 101 = 8 + 8 bit mode (16BPP)	000
L0_DATA16	[22:20]	Select the mode of output data format of I80 CPU I/F (LDI0.) (Only when, VIDOUT[1:0] == 2'b10) 000 = 16 bit mode (16 BPP) 001 = 16 + 2 bit mode (18 BPP) 010 = 9 + 9 bit mode (18 BPP) 011 = 16 + 8 bit mode (24 BPP) 100 = 18 bit mode (18BPP) 101 = 8 + 8 bit mode (16BPP)	000

-	[19]	Reserved	0
PNRMODE	[18:17]	Select the display mode. (Where, VIDOUT[1:0] == 2'b00) 00 = RGB Parallel format (RGB) 01 = RGB Parallel format (BGR) 10 = Serial Format (R->G->B) 11 = Serial Format (B->G->R) Select the display mode. (Where, VIDOUT[1:0] == 2'b1x) 00 = RGB Parallel format (RGB)	00
CLKVALUP	[16]	Select CLKVAL_F update timing control 0 = always 1 = start of a frame (only once per frame)	0
-	[15:14]	Reserved	
CLKVAL_F	[13:6]	Determine the rates of VCLK and CLKVAL[7:0] VCLK = Video Clock Source / (CLKVAL+1) where CLKVAL >= 1 Note. 1. The maximum frequency of VCLK is 66MHz. 2. Video Clock Source is selected by CLKSEL_F register	0
-	[5]	Reserved	0
CLKDIR	[4]	Select the clock source as direct or divide using CLKVAL_F register 0 = Direct clock (frequency of VCLK = frequency of Clock source) 1 = Divided by CLKVAL_F	0x0
CLKSEL_F	[3:2]	Select the Video Clock source 00 = HCLK 01 = LCD video Clock (from SYSCON) 10 = reserved 11 = 27MHz Ext Clock input	0
ENVID	[1]	Video output and the logic immediately enable/disable. 0 = Disable the video output and the Display control signal. 1 = Enable the video output and the Display control signal.	0
ENVID_F	[0]	Video output and the logic enable/disable at current frame end. 0 = Disable the video output and the Display control signal. 1 = Enable the video output and the Display control signal. * If set on and off this bit, then you will read "H" and video controller enable until the end of current frame.	0

6410

VIDCON0	Bit	Description	Initial State

-	[31:30]	Reserved	0
INTERLACE_F	[29]	Interlace or Progressive 0 : Progressive 1: Interlace	0
-	[28]	Reserved (Should be zero)	0
VIDOUT	[27:26]	It determines the output format of Video Controller 00: RGB I/F 01: TV Interface (Encoder or ITU601/656) 10: I80 CPU I/F for LDI0 11: I80 CPU I/F for LDI1	00
L1_DATA16	[25:23]	Select the mode of output data format of I80 CPU I/F (LDI1.) (Only when, VIDOUT[1:0] == 2'b11) 000 = 16 bit mode (16 BPP) 001 = 16 + 2 bit mode (18 BPP) 010 = 9 + 9 bit mode (18 BPP) 011 = 16 + 8 bit mode (24 BPP) 100 = 18 bit mode (18BPP) 101 = 8 + 8 bit mode (16BPP)	000
L0_DATA16	[22:20]	Select the mode of output data format of I80 CPU I/F (LDI0.) (Only when, VIDOUT[1:0] == 2'b10) 000 = 16 bit mode (16 BPP) 001 = 16 + 2 bit mode (18 BPP) 010 = 9 + 9 bit mode (18 BPP) 011 = 16 + 8 bit mode (24 BPP) 100 = 18 bit mode (18BPP) 101 = 8 + 8 bit mode (16BPP)	000
-	[19]	Reserved	0
PNRMODE	[18:17]	Select the display mode. (Where, VIDOUT[1:0] == 2'b00) 00 = RGB Parallel format (RGB) 01 = RGB Parallel format (BGR) 10 = Serial Format (R->G->B) 11 = Serial Format (B->G->R) Select the display mode. (Where, VIDOUT[1:0] == 2'b1x) 00 = RGB Parallel format (RGB)	00
CLKVALUP	[16]	Select CLKVAL_F update timing control 0 = always	0

		1 = start of a frame (only once per frame)	
-	[15:14]	Reserved	
CLKVAL_F	[13:6]	Determine the rates of VCLK and CLKVAL[7:0] VCLK = Video Clock Source / (CLKVAL+1) where CLKVAL >= 1 Note. 1. The maximum frequency of VCLK is 66MHz. 2. Video Clock Source is selected by CLKSEL_F register	0
VCLKFREE	[5]	VCLK Free run control (Only valid at the RGB IF mode) 0 = Normal mode (control by ENVID) 1 = Free-run mode	0
CLKDIR	[4]	Select the clock source as direct or divide using CLKVAL_F register 0 = Direct clock (frequency of VCLK = frequency of Clock source) 1 = Divided by CLKVAL_F	0x0
CLKSEL_F	[3:2]	Select the Video Clock source 00 = HCLK 01 = LCD video Clock (from SYSCON) 10 = reserved 11 = 27MHz Ext Clock input	0
ENVID	[1]	Video output and the logic immediately enable/disable. 0 = Disable the video output and the Display control signal. 1 = Enable the video output and the Display control signal.	0
ENVID_F	[0]	Video output and the logic enable/disable at current frame end. 0 = Disable the video output and the Display control signal. 1 = Enable the video output and the Display control signal. * If set on and off this bit, then you will read “H” and video controller enable until the end of current frame.	0

14.4.2 Video Main Control 2 Register

Register	Address	R/W	Description	Reset Value
VIDCON2	0x77100008	R/W	Video control 2 register	0x0000_0000

6400

Hidden Register

6410

VIDCON2	Bit	Description	Initial state
-	[31:24]	Reserved	0

EN601	[23]	Control ITU601 output enable 0 = Disable 1 = Enable	0
EN656	[22]	Control ITU656 output enable. 0 = Disable 1 = Enable	0
-	[21:13]	Reserved	0
TVFORMATSEL0	[14]	This bit indicates method of YUV data format selection. 0 = Hardware 1 = Software (use TVFORMATSEL1[1:0] bits)	0
TVFORMATSEL1	[13:12]	This bit indicates output format of YUV data. 00 = RGB 01 = YUV422 1x = YUV444	0
-	[11:9]	Reserved	0
OrgYCbCr	[8]	This bit indicates order of YUV data. 0 = Y - CbCr 1 = CbCr – Y	0
YUVOrd	[7]	This bit indicates order of Chroma data. 0 = Cb - Cr 1 = Cr – Cb	0
-	[6:0]	Reserved	0

14.4.3 ITU Interface Control 0 Register

Register	Address	R	Description	Reset Value
ITUIFCON0	0x001A8	R/W	ITU (BT.601/656) Interface control	0x0

6400

Doesn't exist

6410

I80IFCONAx	Bit	Description	Initial State
-	[26:25]	Reserved	0
SELVSYNC	[24]	Select the Vsync mode 0 : equal leading edge with Hsync 1 : Delayed Vsync (standard)	0
DLYVSYNC	[23:16]	Numbers of clock cycles for delay of the VSYNC signal (Only when SELVSYNC is '1') DLYVSYNC+1 * over 64cycles (standard)	0
-	[15:10]	Reserved	0
I656FIELD	[9]	The polarity of the F value (in timing reference code) 0: normal 1: inverted	0
I656CLK	[8]	The polarity of the V656_CLK active edge. 0: normal 1: inverted	0

-	[7]	Reserved	0
I601HREF	[6]	The polarity of the VEN_HREF Signal 0: normal 1: inverted	0
I601VSYNC	[5]	The polarity of the VEN_VSYNC Signal 0: normal 1: inverted	0
I601HSYNC	[4]	The polarity of the VEN_HSYNC Signal 0: normal 1: inverted	0
I601FIELD	[3]	The polarity of the VEN_FIELD Signal 0: normal 1: inverted	0
I601CLK	[2]	The polarity of the V601_CLK active edge 0: normal 1: inverted	0
-	[1:0]	Reserved	0

14.4.4 VIDEO Time Control Register

Register	Address	R/W	Description	Reset Value
VIDTCON 3	**0x0001C**	**R/W**	**Video time control 3 register**	**0x0000_0000**

6400

Hidden Register

6410

VIDTCON3	Bit	Description	Initial State
VSYNCEN	[31]	Control VSYNC Signal Output Enable 0 = Disable 1 = Enable VBPD(VFPD, VSPW) + 1 < LINEVAL (when VSYNCEN =1)	0
-	[30]	Reserved **(should be 0)**	0
FRMEN	[29]	Control the FRM signal output enable 0 = Disable 1 = Enable	0

INVFRM	[28]	Control the polarity of the FRM pulse. 0 = Active HIGH 1 = Active LOW	0
FRMVRATE	[27:24]	Control the FRM issue rate. Max rate up to 1:16	0x00
-	[23:16]	Reserved	0x00
FRMVFPD	[15:8]	Number of line between data active and FRM signal	0x00
FRMVSPW	[7:0]	Number of line of FRM signal width (FRMVFPD + 1) + (FRMVSPW + 1) < LINEVAL + 1 (in RGB) ??	0x00

15. PORT PROCESSOR

15.1 Difference summary

There in no change

16. TV SCALER

16.1 Difference summary

There in no change

17. TV ENCODER

17.1 Difference summary

There in no change

18. GRAPHIC2D

18.1 Difference summary

Enhanced Performance
AXI Master Bus

18.1.1 IP version

: FIMG-2D 2.0

18.2 SFR

Base address : 0x7610_0000				
Register	**Offset**	**R/W**	**Description**	**Reset Value**
General Registers				
CONTROL_REG	0x0000	W	Control register.	0x0000_0000
INTEN_REG	0x0004	R/W	Interrupt Enable register.	0x0000_0000
FIFO_INTC_REG	0x0008	R/W	Interrupt Control register.	0x0000_0018
INTC_PEND_REG	0x000C	R/W	Interrupt Control Pending register.	0x0000_0000
FIFO_STAT_REG	0x0010	R	Command FIFO Status register.	-
Command Registers				
CMD0_REG	0x0100	W	Command register for Line/Point drawing.	-
CMD1_REG	0x0104	W	Command register for BitBLT.	-
CMD2_REG	0x0108	W	Command register for Host to Screen Bitblt transfer start.	-
CMD3_REG	0x010C	W	Command register for Host to Screen Bitblt transfer continue.	-
CMD4_REG	0x0110	W	Command register for Color Expansion. (Host to Screen, Font Start)	-
CMD5_REG	0x0114	W	Command register for Color Expansion. (Host to Screen, Font Continue)	-
CMD6_REG	0x0118	W	Reserved	-
CMD7_REG	0x011C	W	Command register for Color Expansion. (Memory to Screen)	-
Parameter Setting Registers				

Resolution				
SRC_ RES_REG	0x0200	W	Source Image Resolution	0x0000_0000
SRC_HORI_RES_REG	0x0204	W	Source Image Horizontal Resolution	0x0000_0000
SRC_VERT_RES_REG	0x0208	W	Source Image Vertical Resolution	0x0000_0000
SC_RES_REG	0x0210	R/W	Screen Resolution	0x0000_0000
SC_HORI_RES _REG	0x0214	W	Screen Horizontal Resolution	0x0000_0000
SC_VERT_RES _REG	0x0218	W	Screen Vertical Resolution	0x0000_0000
Clipping Window				
CW_LT_REG	0x0220	R/W	LeftTop coordinates of Clip Window.	0x0000_0000
CW_LT_X_REG	0x0224	W	Left X coordinate of Clip Window.	0x0000_0000
CW_LT_Y_REG	0x0228	W	Top Y coordinate of Clip Window.	0x0000_0000
CW_RB_REG	0x0230	R/W	RightBottom coordinate of Clip Window.	0x0000_0000
CW_RB_X_REG	0x0234	W	Right X coordinate of Clip Window.	0x0000_0000
CW_RB_Y_REG	0x0238	W	Bottom Y coordinate of Clip Window.	0x0000_0000
Coordinates				
COORD0_REG	0x0300	R/W	Coordinates 0 register.	0x0000_0000
COORD0_X_REG	0x0304	W	X coordinate of Coordinates 0.	0x0000_0000
COORD0_Y_REG	0x0308	W	Y coordinate of Coordinates 0.	0x0000_0000
COORD1_REG	0x0310	R/W	Coordinates 1 register.	0x0000_0000
COORD1_X_REG	0x0314	W	X coordinate of Coordinates 1.	0x0000_0000
COORD1_Y_REG	0x0318	W	Y coordinate of Coordinates 1.	0x0000_0000
COORD2_REG	0x0320	R/W	Coordinates 2 register.	0x0000_0000
COORD2_X_REG	0x0324	W	X coordinate of Coordinates 2.	0x0000_0000
COORD2_Y_REG	0x0328	W	Y coordinate of Coordinates 2.	0x0000_0000
COORD3_REG	0x0330	R/W	Coordinates 3 register.	0x0000_0000
COORD3_X_REG	0x0334	W	X coordinate of Coordinates 3.	0x0000_0000
COORD3_Y_REG	0x0338	W	Y coordinate of Coordinates 3.	0x0000_0000
Rotation				
ROT_OC_REG	0x0340	R/W	Rotation Origin Coordinates.	0x0000_0000
ROT_OC_X_REG	0x0344	W	X coordinate of Rotation Origin Coordinates.	0x0000_0000
ROT_OC_Y_REG	0x0348	W	Y coorindate of Rotation Origin Coordinates.	0x0000_0000
ROTATE_REG	0x034C	R/W	Rotation Mode register.	0x0000_0001
Data Format				
ENDIAN	0x0350	R/W	Big&little ENDIAN select	0x0000_0000
X,Y Increment Setting				
X_INCR_REG	0x0400	R/W	X Increment register.	0x0000_0000
Y_INCR_REG	0x0404	R/W	Y Increment register.	0x0000_0000

ROP & Alpha Setting				
ROP_REG	0x0410	R/W	Raster Operation register.	0x0000_0000
ALPHA_REG	0x0420	R/W	Alpha value, Fading offset.	0x0000_0000
Color				
FG_COLOR_REG	0x0500	R/W	Foreground Color / Alpha register.	0x0000_0000
BG_COLOR_REG	0x0504	R/W	Background Color register	0x0000_0000
BS_COLOR_REG	0x0508	R/W	Blue Screen Color register	0x0000_0000
SRC_COLOR_MODE_REG	0x0510	R/W	Src Image Color Mode register.	0x0000_0000
DEST_COLOR_MODE_REG	0x0514	R/W	Dest Image Color Mode register	0x0000_0000
Pattern				
PATTERN_REG[0:31]	0x0600 ~0x067C	R/W	Pattern memory.	0x0000_0000
PATOFF_REG	0x0700	R/W	Pattern Offset XY register.	0x0000_0000
PATOFF_X_REG	0x0704	W	Pattern Offset X register.	0x0000_0000
PATOFF_Y_REG	0x0708	W	Pattern Offset Y register.	0x0000_0000
Stencil Test				
STENCIL_CNTL_REG	0x0720	W	Stencil control register	0x0000_0000
STENCIL_DR_MIN_REG	0x0724	W	Stencil decision reference MIN register	0x0000_0000
STENCIL_DR_MAX_REG	0x0728	W	Stencil decision reference MAX register	0xFFFF_FFFF
Image Base Address				
SRC_BASE_ADDR_REG	0x0730	R/W	Source Image Base Address register	0x0000_0000
DEST_BASE_ADDR_REG	0x0734	R/W	Dest Image Base Address register (in most cases, frame buffer address)	0x0000_0000

18.2.1 General Registers

Control Register (CONTROL_REG)

Offset=0x0000, W, Reset Value=0x0000_0000

Field	Bit	Description	Initial State
Reserved	[31:1]		0x0
R	[0]	Software Reset, Automatic Clear.	0x0

Interrupt Enable REGISTER (INTEN_REG)

Offset=0x0004, R/W, Reset Value=0x0000_0000

Field	Bit	Description	Initial State
Reserved	[31:11]		0x0
DF	[10]	Drawing Engine Finished Interrupt Enable.	0x0
F	[9]	All command Finished Interrupt Enable.	0x0
OV	[8]	Overflow Interrupt Enable.	0x0
Reserved	[7:1]		0x0
E	[0]	Interrupt Enable. ; If E bit is set to 1, when FIFO_INT_LEVEL is same with FIFO_USED, Graphics Engine makes INTREQ signal high.	0x0

FIFO Interrupt Control REGISTER (FIFO_INTC_REG)

Offset=0x0008, R/W, Reset Value=0x0000_0018

Field	Bit	Description	Initial State
Reserved	[31:6]		0x0
FIFO_INT_LEVEL	[5:0]	Graphics Engine requests interrupt when the number of FIFO used is FIFO_INT_LEVEL and Interrupt Enable bit is set to 1.	0x18

Interrupt Pending REGISTER (INTC_PEND_REG)

Offset=0x000C, R/W, Reset Value=0x0000_0000

Field	Bit	Description	Initial State

CLRSEL	[31]	Level interrupt & pulse interrupt mode select. 1 : level interrupt mode select(interrupt clear enable) 0: pulse interrupt mode select	0x0
Reserved	[30:11]		-
INTP_DE_FIN	[10]	Graphics Drawing Engine finished.	-
INTP_FINISH_ALL	[9]	Graphics Engine IDLE state.	-
INTP_OVERFLOW	[8]	Overflow Interrupt.	-
Reserved	[7:1]		-
INTP_FIFO_LEVEL	[0]	When FIFO_INT_LEVEL is same with FIFO_USED, Graphics Engine makes INTP_FIFO_LEVEL signal high.	-

FIFO status REGISTER (FIFO_STAT_REG)

Offset=0x0010, R

Field	Bit	Description	Initial State
Reserved	[31:11]		-
DE_FIN	[10]	Current command finished	-
ALL_FIN	[9]	All commands finished	-
FIFO_OVERFLOW	[8]	The command fifo is full, no more commands can be handled	-
Reserved	[7]		-
FIFO_USED	[6:1]	The number of FIFO entry used.	-
FIFO_LEVEL_INT	[0]	The number of entries in the command FIFO reaches the number specified by the user (FIFO_INT_LEVEL)	-

COMMAND REGISTERS

Line Drawing REGISTER (CMD0_REG)

Offset=0x0100, W

Field	Bit	Description	Initial State
Reserved	[31:10]		-
D	[9]	0 : Draw Last Point 1 : Do-not-Draw Last Point.	-
M	[8]	0 : Major axis is Y. 1 : Major axis is X.	-
Reserved	[7:2]		-
L	[1]	0 : Nothing. 1 : Line Drawing.	-
P	[0]	0 : Nothing. 1 : Point Drawing.	-

BitBLT REGISTER (CMD1_REG)

Offset=0x0104, W

Field	Bit	Description	Initial State
Reserved	[31:2]		-
S	[1]	0 : Nothing 1 : Stretch BitBLT	-
N	[0]	0 : Nothing 1 : Normal BitBLT	-

Host to Screen Start BitBLT REGISTER (CMD2_REG)

Offset=0x0108, W

Field	Bit	Description	Initial State
Data	[31:0]	BitBLT data (Start)	-

Host to Screen Continue BitBLT REGISTER (CMD3_REG)

Offset=0x010C, W

Field	Bit	Description	Initial State

Data	[31:0]	BitBLT data (Continue)	-

Host to Screen Start Color Expansion REGISTER (CMD4_REG)

Offset=0x0110, W

Field	Bit	Description	Initial State
Data	[31:0]	Packed format bitmap data (Start)	-

Host to Screen Continue Color Expansion REGISTER (CMD5_REG)

Offset=0x0114, W

Field	Bit	Description	Initial State
Data	[31:0]	Packed format bitmap data (Continue)	-

Memory to Screen Color Expansion REGISTER (CMD7_REG)

Offset=0x011C, W

Field	Bit	Description	Initial State
Memory Address	[31:0]	Bitmap data base address (used in memory-to-screen mode, should be word-aligned).	-

18.2.3 Parameter Setting Registers

Resolution

Source Image Resolution (SRC_RES_REG)

Offset=0x0200, R/W, Reset Value=0x0000_0000

Field	Bit	Description	Initial State
Reserved	[31:27]		0x0
VertRes	[26:16]	Vertical Resolution of Source Image	0x0
Reserved	[15:11]		0x0
HoriRes	[10:0]	Horizontal Resolution of Source Image	0x0

Source Image Horizontal Resolution (SRC_HORI_RES_REG)

Offset=0x0204, W, Reset Value=0x0000_0000

Field	Bit	Description	Initial State
Reserved	[31:1]		0x0
HoriRes	[10:0]	Horizontal Resolution of Source Image	0x0

Source Image Vertical Resolution (SRC_VERT_RES_REG)

Offset=0x0208, W, Reset Value=0x0000_0000

Field	Bit	Description	Initial State
Reserved	[31:1]		0x0
VertRes	[10:0]	Vertical Resolution of Source Image	0x0

Screen Resolution (SC_RES_REG)

Offset=0x0210, R/W, Reset Value=0x0000_0000

Field	Bit	Description	Initial State
Reserved	[31:27]		0x0
VertRes	[26:16]	Vertical Resolution	0x0
Reserved	[15:11]		0x0
HoriRes	[10:0]	Horizontal Resolution	0x0

Screen Horizontal Resolution (SC_HORI_RES_REG)

Offset=0x0214, W, Reset Value=0x0000_0000

Field	Bit	Description	Initial State
Reserved	[31:11]		0x0
HoriRes	[10:0]	Horizontal Resolution	0x0

Screen Vertical Resolution (SC_VERI_RES_REG)

Offset=0x0218, W, Reset Value=0x0000_0000

Field	Bit	Description	Initial State
Reserved	[31:1]		0x0
VeriRes	[10:0]	Vertical Resolution	0x0

19. ROTATOR

19.1 Difference summary

There is no change

20. CAMIF

20.1 Difference summary

	6400	6410
LCD direct path	Dual-path & LCD direct path always use HCLK	Add the New input clock port (DCLK) Select DCLK or HCLK for LCD direct path output data
Scaler mem. size	Preview : sram_320x16/20 Codec : sram_1024x16/20	Preview : sram_368x16/20 Codec : sram_1024x16/20
Scaler image max. size (horizontal)	Preview : 640, Codec : 2048	Preview : 720 , Codec : 2048
Rotator mem. size	Preview : sram_1280x32	Preview : sram_2944x32
One2One register add	none	For no interpolation when 1:1 scaling Refer to the document SFR (One2One)
CSC precision enhancement	-	No relationship verification software. Just CSC algorithm enhancement (C model + RTL updated)
Hardware trigger	Don't care (should be set software trigger)	Don't care (should be set software trigger)
Interlace Input	Not support	Support

20.1.1 IP version

FIMC 3.2

20.2 Interlace Mode Support

* Rules

- Starting point : First Even Field

Odd (Ignored) → Even (Start) → Odd

Even (Start) → Odd

- Frame buffer start address

  1st or 3rd buffer : Even Field address

  2nd or 4th buffer : Odd Field address

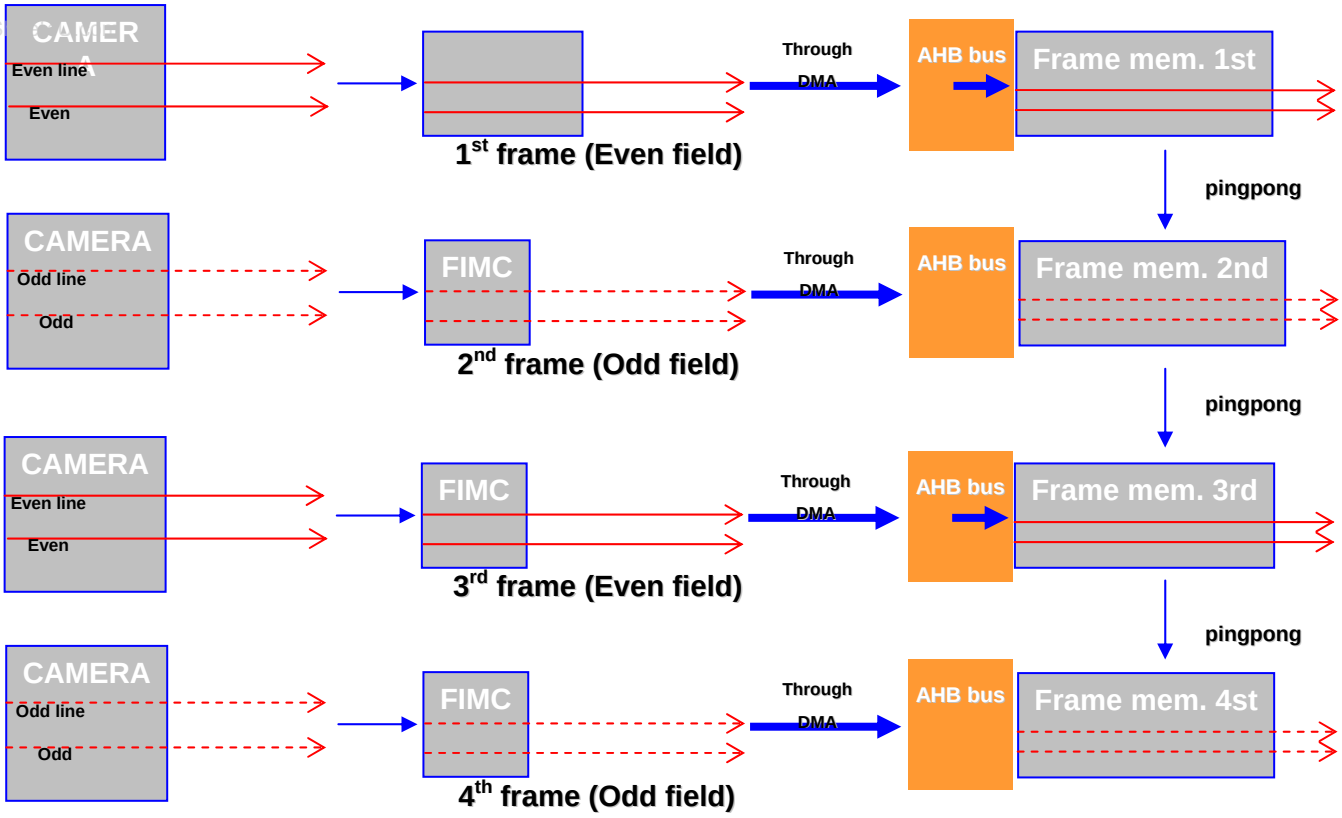
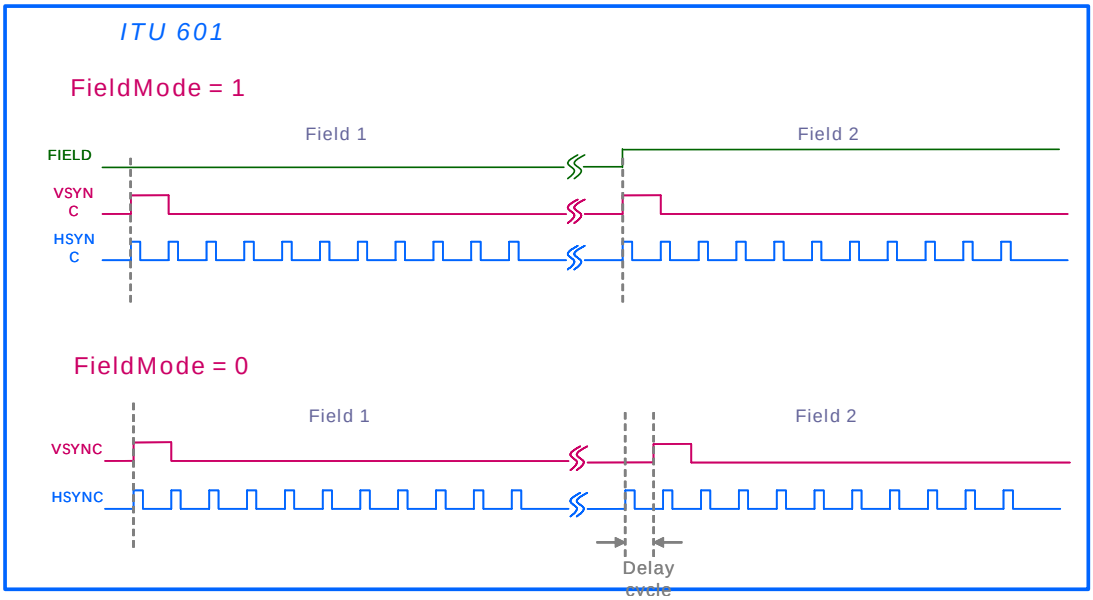


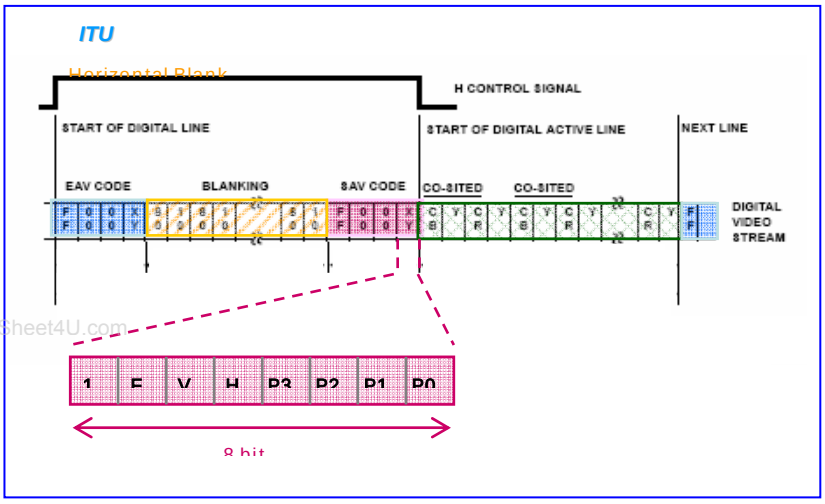
Figure 1. Frame buffer Control



Control Register

Name	Description
FieldMode	ITU 601 Interlace Field mode 1 : Need field port 0 : Need not field port
InvField	Inverse polarity Field <Note> FIMC handles Field 1(Low level) equals Even field

Figure 2. Frame Capture Control (1)



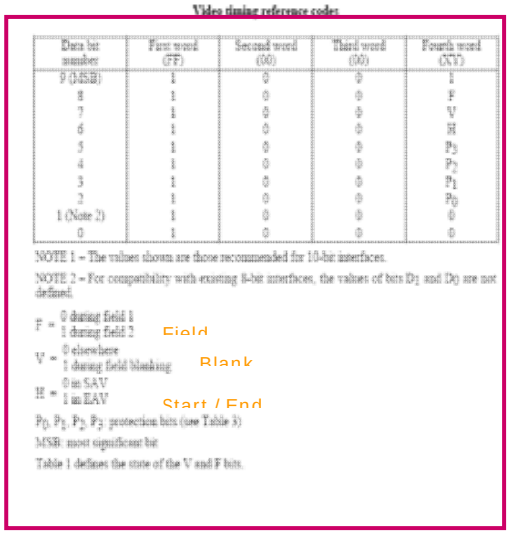


Figure 3. Frame Capture Control (2)

20.3 SFR

20.3.1 CODEC MAIN-SCALER CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
CICOSCCTRL	0x78000058	RW	Codec main-scaler control	0x18000000

6400

CICOSCCTRL	Bit	Description	Initial State	M	L
ScalerBypass_Co	[31]	Codec scaler bypass. In this case, ImgCptEn_CoSC must be 0, but ImgCptEn must be 1. Generally this mode uses large image size upper scaler maximum size. Therefore it is not recommended to capturing preview image. (Recommend, ImgCptEn_PrSC must be 0). This mode is intended to capture JPEG input image for DSC application). In this case, input pixel buffering depends on only input FIFOs, so system bus must not be busy in this mode. ScalerBypass has some restriction. it is not allowed size scaling, color space conversion, rotator and MSDMA memory input image. so, Input / output format is allowed YCbCr non-interleave 4:2:0,4:2:2 & interleave 4:2:2	0	O	O

ScaleUp_H_Co	[30]	Horizontal scale up/down flag for codec scaler (In 1:1 scale ratio, this bit must be “1”) 1: up, 0:down	0	O	O
ScaleUp_V_Co	[29]	Vertical scale up/down flag for codec scaler (In 1:1 scale ratio, this bit must be “1”) 1: up, 0:down	0	O	O
CSCR2Y_c	[28]	YCbCr Data Dynamic Range Selection for the Color Space Conversion RGB to YCbCr (Codec path) 1 : Wide => Y/Cb/Cr (0 ~ 255) : Wide default 0 : Narrow => Y (16 ~ 235), Cb/Cr (16 ~ 240) ※ Recommend CSC range setting CSCR2Y_c = CSCY2R_c (Wide=Wide or Narrow=Narrow)	1	O	O
CSCY2R_c	[27]	YCbCr Data Dynamic Range Selection for the Color Space Conversion YCbCr to RGB (Codec path) 1 : Wide => Y/Cb/Cr (0 ~ 255) : Wide default 0 : Narrow => Y (16 ~ 235), Cb/Cr (16 ~ 240)	1	O	O
LCDPathEn_Co	[26]	FIFO Mode Enable. 1 for FIFO mode and 0 for DMA mode FIFO mode output format is YCbCr4:4:4 or RGB24bit. its selection depends on OutFormat register. OutFormat_Co = RGB → RGB24bit , otherwise YCbCr4:4:4	0	O	O
Interlace_Co	[25]	Output scan method selection register only when FIFO mode (LCDPathEn =1). 1 for Interlace scan and 0 for progressive scan. In DMA mode (LCDPathEn = 0), progressive scan is applied whatever this value has. This mode is not allowed when Input image data is from Camera processor.	0	O	O
MainHorRatio_Co	[24:16]	Horizontal scale ratio for codec main-scaler	0	O	O
CoScalerStart	[15]	Codec scaler start 1 : scaler start 0 : scaler stop	0	O	O
InRGB_FMT_Co	[14:13]	Input RGB format MSDMA for codec path dedicated 00 : RGB565 , 01 : RGB666 , 10 : RGB888 , 11 : Reserved	0	O	O
OutRGB_FMT_Co	[12:11]	Output RGB format for Codec write DMA 00 : RGB565 , 01 : RGB666 , 10 : RGB888 , 11 : Reserved	0	O	O
Ext_RGB_Co	[10]	Input RGB data extension enable bit for the conversion of RGB565/666 mode into RGB888 mode for codec path. 1 : Extension , 0 : normal i) Input R = 5bit in RGB565 mode *10100* -> 10100*101* (Extension) 10100 -> 10100000 (normal) ii) Input R = 6bit in RGB666 mode *101100* -> 10110*10* (Extension) 101100 -> 10110000 (normal)	0	O	O

Reserved	[9]		0	O	O
MainVerRatio_Co	[8:0]	Vertical scale ratio for codec main-scaler	0	O	O

6410

CICOSCCTRL	Bit	Description	Initial State	M	L
ScalerBypass_Co	[31]	Codec scaler bypass. In this case, ImgCptEn_CoSC must be 0, but ImgCptEn must be 1. Generally this mode uses large image size upper scaler maximum size. Therefore it is not recommended to capturing preview image. (Recommend, ImgCptEn_PrSC must be 0). This mode is intended to capture JPEG input image for DSC application). In this case, input pixel buffering depends on only input FIFOs, so system bus must not be busy in this mode. ScalerBypass has some restriction. it is not allowed size scaling, color space conversion, rotator and MSDMA memory input image. so, Input / output format is allowed YCbCr non-interleave 4:2:0,4:2:2 & interleave 4:2:2	0	O	O
ScaleUp_H_Co	[30]	Horizontal scale up/down flag for codec scaler (In 1:1 scale ratio, this bit must be “1”) 1: up, 0:down	0	O	O
ScaleUp_V_Co	[29]	Vertical scale up/down flag for codec scaler (In 1:1 scale ratio, this bit must be “1”) 1: up, 0:down	0	O	O
CSCR2Y_c	[28]	YCbCr Data Dynamic Range Selection for the Color Space Conversion RGB to YCbCr (Codec path) 1 : Wide => Y/Cb/Cr (0 ~ 255) : Wide default 0 : Narrow => Y (16 ~ 235), Cb/Cr (16 ~ 240) ※ Recommend CSC range setting CSCR2Y_c = CSCY2R_c (Wide=Wide or Narrow=Narrow)	1	O	O
CSCY2R_c	[27]	YCbCr Data Dynamic Range Selection for the Color Space Conversion YCbCr to RGB (Codec path) 1 : Wide => Y/Cb/Cr (0 ~ 255) : Wide default 0 : Narrow => Y (16 ~ 235), Cb/Cr (16 ~ 240)	1	O	O
LCDPathEn_Co	[26]	FIFO Mode Enable. 1 for FIFO mode and 0 for DMA mode FIFO mode output format is YCbCr4:4:4 or RGB24bit. its selection depends on OutFormat register. OutFormat_Co = RGB → RGB24bit , otherwise YCbCr4:4:4	0	O	O

Interlace_Co	[25]	Output scan method selection register only when FIFO mode (LCDPathEn =1). 1 for Interlace scan and 0 for progressive scan. In DMA mode (LCDPathEn = 0), progressive scan is applied whatever this value has. This mode is not allowed when Input image data is from Camera processor.	0	O	O
MainHorRatio_Co	[24:16]	Horizontal scale ratio for codec main-scaler	0	O	O
CoScalerStart	[15]	Codec scaler start 1 : scaler start 0 : scaler stop	0	O	O
InRGB_FMT_Co	[14:13]	Input RGB format MSDMA for codec path dedicated 00 : RGB565 , 01 : RGB666 , 10 : RGB888 , 11 : Reserved	0	O	O
OutRGB_FMT_Co	[12:11]	Output RGB format for Codec write DMA 00 : RGB565 , 01 : RGB666 , 10 : RGB888 , 11 : Reserved	0	O	O
Ext_RGB_Co	[10]	Input RGB data extension enable bit for the conversion of RGB565/666 mode into RGB888 mode for codec path. 1 : Extension , 0 : normal i) Input R = 5bit in RGB565 mode *101*00 -> 10100*101* (Extension) 10100 -> 10100000 (normal) ii) Input R = 6bit in RGB666 mode *10*1100 -> 10110*10* (Extension) 101100 -> 10110000 (normal)	0	O	O
One2One_Co	[9]	Non-interpolation data copy. (Caution : this register should be set at 1:1 scaler size for same in-out format and Image effect cannot support RGB format & One2One mode.) Ex) input YCbCr4:2:0 (VGA) -> output YCbCr4:2:0 (VGA)	0	O	O
MainVerRatio_Co	[8:0]	Vertical scale ratio for codec main-scaler	0	O	O

20.3.2 CODEC MAIN-SCALER CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
CIPRSCCTRL	0x780000AC	RW	Preview main-scaler control	0x18000000

6400

CIPRSCCTRL	Bit	Description	Initial State	M	L

ScalerBypass_Pr	[31]	Preview scaler bypass. In this case, ImgCptEn_PrSC must be 0, but ImgCptEn must be 1. Generally this mode uses large image size than preview scaler maximum size. ScalerBypass has some restriction. It is not allowed size scaling, color space conversion and rotator. Therefore, Input / output format is allowed YCbCr non-interleave 4:2:0,4:2:2 & interleave 4:2:2	0	O	O
ScaleUp_H_Pr	[30]	Horizontal scale up/down flag for preview scaler (In 1:1 scale ratio, this bit must be “1”) 1: up, 0:down	0	O	O
ScaleUp_V_Pr	[29]	Vertical scale up/down flag for preview scaler (In 1:1 scale ratio, this bit must be “1”) 1: up, 0:down	0	O	O
CSCR2Y_Pr	[28]	YCbCr Data Dynamic Range Selection for the Color Space Conversion RGB to YCbCr (Preview path) 1 : Wide => Y/Cb/Cr (0 ~ 255) : Wide default 0 : Narrow => Y (16 ~ 235), Cb/Cr (16 ~ 240) ※ Recommend CSC range setting CSCR2Y = CSCY2R (Wide=Wide or Narrow=Narrow)	1	O	O
CSCY2R_Pr	[27]	YCbCr Data Dynamic Range Selection for the Color Space Conversion YCbCr to RGB (Preview path) 1 : Wide => Y/Cb/Cr (0 ~ 255) : Wide default 0 : Narrow => Y (16 ~ 235), Cb/Cr (16 ~ 240)	1	O	O
LCDPathEn_Pr	[26]	FIFO Mode Enable. 1 for FIFO mode and 0 for DMA mode FIFO mode output format is YCbCr4:4:4 or RGB24bit. its selection depends on OutFormat register. OutFormat_Pr = RGB → RGB24bit , otherwise YCbCr4:4:4	0	O	O
Interlace_Pr	[25]	Output scan method selection register only when FIFO mode (LCDPathEn =1). 1 for Interlace scan and 0 for progressive scan. In DMA mode (LCDPathEn = 0), progressive scan is applied whatever this value has.Interlace mode is allowed when MSDMA input data & is not allowed when Camera processor input data	0	O	O
MainHorRatio_Pr	[24:16]	Horizontal scale ratio for preview main-scaler	0	O	O
PrScalerStart	[15]	Preview scaler start. This bit must be zero in preview scaler-bypass mode. 1 : scaler start 0 : scaler stop	0	O	O
InRGB_FMT_Pr	[14:13]	Input RGB format MSDMA for preview path dedicated 00 : RGB565 , 01 : RGB666 , 10 : RGB888 , 11 : Forbidden	0	O	O
OutRGB_FMT_Pr	[12:11]	Output RGB format for Preview write DMA 00 : RGB565 , 01 : RGB666 , 10 : RGB888 , 11 : Forbidden	0	O	O

Ext_RGB_Pr	[10]	Input RGB data extension enable bit for the conversion of RGB565/666 mode into RGB888 mode for preview path 1 : Extension , 0 : normal i) Input R = 5bit in RGB565 mode *10100* -> 10100*101* (Extension) 10100 -> 10100000 (normal) ii) Input R = 6bit in RGB666 mode *101*100 -> 10110*10* (Extension) 101100 -> 10110000 (normal)	0	O	O
Reserved	[9]		0	O	O
MainVerRatio_Pr	[8:0]	Vertical scale ratio for preview main-scaler	0	O	O

6410

CIPRSCCTRL	Bit	Description	Initial State	M	L
ScalerBypass_Pr	[31]	Preview scaler bypass. In this case, ImgCptEn_PrSC must be 0, but ImgCptEn must be 1. Generally this mode uses large image size than preview scaler maximum size. ScalerBypass has some restriction. It is not allowed size scaling, color space conversion and rotator. Therefore, Input / output format is allowed YCbCr non-interleave 4:2:0,4:2:2 & interleave 4:2:2	0	O	O
ScaleUp_H_Pr	[30]	Horizontal scale up/down flag for preview scaler (In 1:1 scale ratio, this bit must be “1”) 1: up, 0:down	0	O	O
ScaleUp_V_Pr	[29]	Vertical scale up/down flag for preview scaler (In 1:1 scale ratio, this bit must be “1”) 1: up, 0:down	0	O	O
CSCR2Y_Pr	[28]	YCbCr Data Dynamic Range Selection for the Color Space Conversion RGB to YCbCr (Preview path) 1 : Wide => Y/Cb/Cr (0 ~ 255) : Wide default 0 : Narrow => Y (16 ~ 235), Cb/Cr (16 ~ 240) ※ Recommend CSC range setting CSCR2Y = CSCY2R (Wide=Wide or Narrow=Narrow)	1	O	O
CSCY2R_Pr	[27]	YCbCr Data Dynamic Range Selection for the Color Space Conversion YCbCr to RGB (Preview path) 1 : Wide => Y/Cb/Cr (0 ~ 255) : Wide default 0 : Narrow => Y (16 ~ 235), Cb/Cr (16 ~ 240)	1	O	O
LCDPathEn_Pr	[26]	FIFO Mode Enable. 1 for FIFO mode and 0 for DMA mode FIFO mode output format is YCbCr4:4:4 or RGB24bit. its selection depends on OutFormat register. OutFormat_Pr = RGB → RGB24bit , otherwise YCbCr4:4:4	0	O	O

Interlace_Pr	[25]	Output scan method selection register only when FIFO mode (LCDPathEn =1). 1 for Interlace scan and 0 for progressive scan. In DMA mode (LCDPathEn = 0), progressive scan is applied whatever this value has.Interlace mode is allowed when MSDMA input data & is not allowed when Camera processor input data	0	O	O
MainHorRatio_Pr	[24:16]	Horizontal scale ratio for preview main-scaler	0	O	O
PrScalerStart	[15]	Preview scaler start. This bit must be zero in preview scaler-bypass mode. 1 : scaler start 0 : scaler stop	0	O	O
InRGB_FMT_Pr	[14:13]	Input RGB format MSDMA for preview path dedicated 00 : RGB565 , 01 : RGB666 , 10 : RGB888 , 11 : Forbidden	0	O	O
OutRGB_FMT_Pr	[12:11]	Output RGB format for Preview write DMA 00 : RGB565 , 01 : RGB666 , 10 : RGB888 , 11 : Forbidden	0	O	O
Ext_RGB_Pr	[10]	Input RGB data extension enable bit for the conversion of RGB565/666 mode into RGB888 mode for preview path 1 : Extension , 0 : normal i) Input R = 5bit in RGB565 mode *101*00 -> 10100*101* (Extension) 10100 -> 10100000 (normal) ii) Input R = 6bit in RGB666 mode *10*1100 -> 10110*10* (Extension) 101100 -> 10110000 (normal)	0	O	O
One2One_Pr	[9]	Non-interpolation data copy. (Caution : this register should be set at 1:1 scaler size for same in-out format and Image effect cannot support RGB format & One2One mode.) Ex) input YCbCr4:2:0 (VGA) -> output YCbCr4:2:0 (VGA)	0	O	O
MainVerRatio_Pr	[8:0]	Vertical scale ratio for preview main-scaler	0	O	O

21. MFC

21.1 Difference summary

There in no change

22. JPEG

22.1 Difference summary

There in no change

23. MODEM INTERFACE

23.1 Difference summary

S3C6410 supports DMA operation

23.2 Register compare bit by bit

There are new added SFR fields.

Modem Interface Control Register (MIFCON)

MIFCON	Bit	DESCRIPTION	INITIAL STATE
DMARXREQEN_1	[19]	MSM Write DMA Request (RX 1) to AP(DMA Controller) Enable	0
DMARXREQEN_0	[18]	MSM Write DMA Request (RX 0) to AP(DMA Controller) Enable	0
DMATXREQEN_1	[17]	MSM Read DMA Request (TX 1) to AP(DMA Controller) Enable	0
DMATXREQEN_0	[16]	MSM Read DMA Request (TX 0) to AP(DMA Controller) Enable	0

DMA Request TX Address Register (DMAREQ_TX_ADR)

Register	address	R/W	Description	Reset Value
DMA_TX_ADR	0x74108014	R/W	DMA TX request Address register	0x07FE03FE

INT2AP	Bit	Description	Initial State
Reserved	[31:29]	Reserved	0
DMA_TX_ADR_1	[28:16]	Modem interface requests the DMA to AP(DMA Controller) when modem chip **reads** this address. Source : DMA_MSM_Req[1]	07FE
Reserved	[15:13]	Reserved	0
DMA_TX_ADR_0	[12:0]	Modem interface requests the DMA to AP(DMA Controller) when modem chip **reads** this address. Source : DMA_MSM_Req[0]	03FE

DMA Request RX Address Register (DMAREQ_RX_ADR)

Register	address	R/W	Description	Reset Value
DMA_RX_ADR	0x74108018	R/W	DMA RX request Address register	0x0FFE0BFE

INT2AP	Bit	Description	Initial State
Reserved	[31:29]	Reserved	0
DMA_RX_ADR_1	[28:16]	Modem interface requests the DMA to AP(DMA Controller) when modem chip **writes** this address. Source : DMA_MSM_Req[3]	0FFE
Reserved	[15:13]	Reserved	0
DMA_RX_ADR_0	[12:0]	Modem interface requests the DMA to AP(DMA Controller) when modem chip **writes** this address. Source : DMA_MSM_Req[2]	0BFE

24. HOST INTERFACE

24.1 Difference summary

There in no change

25. USB HOST CONTROLLER

25.1 Difference summary

There in no change

26. USB 2.0 HS OTG

26.1 Difference summary

26.1.1 New functionality

- OTG Block Disable
; This controller signal power down the OTG Block, including the VBUS Valid comparator. If the application does not use OTG functionality, you can set this input high to save power

26.1.2 Not support

- XO block power down mode
- Power Save mode : The digital logic uses 48MHz Clock, PLL power down ,
(This mode is valid for full-speed and low-speed operation in a host application, and only full-speed operation in a device application)
- Force XO Block On During a Suspend

26.2 Register compare bit by bit

26.2.1 OTG PHY POWER CONTROL REGISTER(OPHYPWR)

Register	Address	R/W	Description	Reset Value
OPHYPWR	0x7C10_0000	R/W	OTG PHY Power Control Register	32 bits

6400

OPHYPWR	Bit	R/W	Description	Initial State
	[31:4]		Reserved	28'h0
analog_powerdown	[3]	R_W	Analog block power down in PHY2.0 · 1'b0 : Analog block power up (Normal Operation) · 1'b1 : Analog block power down	1'b1
xo_powerdown	[2]	R_W	XO block power down in PHY2.0 · 1'b0 : XO block power up (PLL reference is XO block output) · 1'b1 : XO block power down (PLL reference is clk_core input) Note : clk_sel[1:0] bus must be set to 2'b00	1'b1
pll_powerdown	[1]	R_W	PLL power down in PHY2.0	1'b1

			· 1'b0 : PLL power up. The digital logic uses a 480 MHz clock. · 1'b1 : PLL power down. The digital logic uses a 48-MHz clock. This mode is valid for full-speed and low-speed operation in a host application, and only full-speed operation in a device application. The clk_sel[1:0] bus must be set to 2'b00 (48MHz) when pll_powerdown is asserted high. PLL power down mode is not supported with 12/24 MHz reference clock inputs.	
force_suspend	[0]	R_W	Apply Suspend signal for power save · 1'b0 : disable (Normal Operation) · 1'b1 : enable	1'b1

6410

OPHYPWR	Bit	R/W	Description	Initial State
	[31:5]		Reserved	
otg_disable	[4]	R_W	OTG block power down down in PHY 2.0 0 = OTG block power up 1 = OTG block power down	1'b1
analog_powerdown	[3]	R_W	Analog block power down in PHY2.0 · 1'b0 : Analog block power up (Normal Operation) · 1'b1 : Analog block power down	1'b1
	[2:1]		Reserved	2'b0
force_suspend	[0]	R_W	Apply Suspend signal for power save · 1'b0 : disable (Normal Operation) · 1'b1 : enable	1'b1

26.2.2 OTG PHY Clock Control Register (OPHYCLK)

Register	Address	R/W	Description	Reset Value
OPHYCLK	0x7C10_0004	R/W	OTG PHY Control Register	32 bits

6400

OPHYCLK	Bit	R/W	Description	Initial State
	[31:7]		Reserved	25'h0
serial_mode	[6]	R_W	UTMI/Serial Interface Select When this register is asserted, USB traffic flows through the serial interface. · 1'b0 : Data on the D+ and D- lines is transmitted	1'b0

			and received through the UTMI. · 1'b1 : Data on the D+ and D- lines is transmitted and received through the USB1.1 Serial Interface.	
xo_ext_clk_enb	[5]	R_W	Reference Clock Select for XO Block · 1'b0 : external crystal · 1'b1 : external clock/oscillator Note : clk_sel[1:0] bus must be set to 2'b00	1'b0
common_on_n	[4]	R_W	Force XO, Bias, Bandgap, and PLL to Remain Powered During a Suspend This bit controls the power-down signals of sub-blocks in the Common block when the USB 2.0 OTG PHY is suspended. · 1'b0 : 48MHz clock on clk48m_ohci is available at all times, except in Suspend mode. · 1'b1 : 48MHz clock on clk48m_ohci is available at all times, even in Suspend mode.	1'b0
xo_on_n	[3]	R_W	Force XO Block On During a Suspend · 1'b0 : If all ports are suspended, the XO block is powered up, and the clk_ref_ohci(48MHz clock source for other IPs) signal is available. · 1'b1 : XO block is powered down when all ports are suspended.	1'b0
id_pullup	[2]	R_W	Analog ID Input Sample Enable · 1'b0 : id_dig disable. · 1'b1 : id_dig enable. (The id_dig output is valid, and within 20ms, id_dig must indicate which type of plug is connected.)	1'b0
clk_sel	[1:0]	R_W	Reference Clock Frequency Select for PLL · 2'b00 : 48MHz · 2'b01 : Reserved · 2'b10 : 12MHz · 2'b11 : 24MHz	2'b00

6410

OPHYCLK	Bit	R/W	Description	Initial State
	[31:7]		Reserved	25'h0
serial_mode	[6]	R_W	UTMI/Serial Interface Select When this register is asserted, USB traffic flows through the serial interface. · 1'b0 : Data on the D+ and D- lines is transmitted and received through the UTMI. · 1'b1 : Data on the D+ and D- lines is transmitted and received through the USB1.1 Serial Interface.	1'b0

ref_clk_sel	[5]	R_W	Reference Clock select for XO Block · 1'b0 : external crystal · 1'b1 : external clock/oscillator	2'b00
common_on_n	[4]	R_W	Force XO, Bias, Bandgap, and PLL to Remain Powered During a Suspend This bit controls the power-down signals of sub-blocks in the Common block when the USB 2.0 OTG PHY is suspended. · 1'b0 : 48MHz clock on clk48m_ohci is available at all times, except in Suspend mode. · 1'b1 : 48MHz clock on clk48m_ohci is available at all times, even in Suspend mode.	1'b0
	[3]		Reserved	1'b0
id_pullup	[2]	R_W	Analog ID Input Sample Enable · 1'b0 : id_dig disable. · 1'b1 : id_dig enable. (The id_dig output is valid, and within 20ms, id_dig must indicate which type of plug is connected.)	1'b0
clk_sel	[1:0]	R_W	Reference Clock Frequency Select for PLL · 2'b00 : 48MHz · 2'b01 : Reserved · 2'b10 : 12MHz · 2'b11 : 24MHz	2'b00

27. HSMMC

27.1 Difference summary

S3C6410 HSMMC Controller supports new feature : SD Standard Host Spec(ver 2.0) compatible

27.2 New added Register fields

There are new added SFR fields.

HOST CONTROL REGISTER

	[4:3]	**DMA Select** One of supported DMA modes can be selected. The host driver shall check support of DMA modes by referring the *Capabilities* register. Use of selected DMA is determined by **DMA Enable** of the *Transfer Mode* register. 00 = SDMA is selected 01 = Reserved 10 = 32-bit Address ADMA2 is selected 11 = 64-bit Address ADMA2 is selected (Not supported)	0

ERROR INTERRUPT STATUS REGISTER

	[9]	**ADMA Error** This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the *ADMA Error Status* Register, In addition, the Host Controller generates this Interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state. **ADMA Error State** in the *ADMA Error Status* indicates that an error occurs in ST_FDS state. The Host Driver may find that Valid bit is not set at the error descriptor. '1' = Error '0' = No Error	0

Error Interrupt Status Enable Register

	[9]	**ADMA Error Status Enable** '1' = Enabled '0' = Masked	0

ERROR INTERRUPT SIGNAL ENABLE REGISTER

	[9]	**ADMA Error Signal Enable** '1' = Enabled '0' = Masked	0

FORCE EVENT REGISTER FOR ERROR INTERRUPT STATUS

Register	Address	R/W	Description	Reset Value
FEERR0	0x4A800052	WO	Force Event Error Interrupt Register Error Interrupt (Channel 0)	0x0000
FEERR1	0x4A900052	WO	Force Event Error Interrupt Register Error Interrupt (Channel 1)	0x0000

The *Force Event* Register is not a physically implemented register. Rather, it is an address at which the *Error Interrupt Status* register can be written. The effect of a write to this address will be reflected in the *Error Interrupt Status* Register if the corresponding bit of the *Error Interrupt Status Enable* Register is set.
Writing 1 : set each bit of the *Error Interrupt Status* Register
Writing 0 : no effect
Note: By setting this register, the Error Interrupt can be set in the *Error Interrupt Status* register. In order to generate interrupt signal, both the *Error Interrupt Status Enable* and **Error Interrupt Signal Enable** shall be set.

Name	Bit	Description	Initial Value
	[15:12]	**Force Event for Vendor Specific Error Status** Additional status bits can be defined in this register by the vendor. 1=Interrupt is generated 0=No Interrupt	0x0
	[11:10]		
	[9]	**Force Event for ADMA Error** 1=Interrupt is generated 0=No Interrupt	0
	[8]	**Force Event for Auto CMD12 Error** 1=Interrupt is generated 0=No Interrupt	0
	[7]	**Force Event for Current Limit Error** 1=Interrupt is generated 0=No Interrupt	0
	[6]	**Force Event for Data End Bit Error** 1=Interrupt is generated 0=No Interrupt	0
	[5]	**Force Event for Data CRC Error**	0

		1=Interrupt is generated 0=No Interrupt	
	[4]	**Force Event for Data Timeout Error** 1=Interrupt is generated 0=No Interrupt	0
	[3]	**Force Event for Command Index Error** 1=Interrupt is generated 0=No Interrupt	0
	[2]	**Force Event for Command End Bit Error** 1=Interrupt is generated 0=No Interrupt	0
	[1]	**Force Event for Command CRC Error** 1=Interrupt is generated 0=No Interrupt	0
	[0]	**Force Event for Command Timeout Error** 1=Interrupt is generated 0=No Interrupt	0

FORCE EVENT REGISTER FOR AUTO CMD12 ERROR STATUS

Register	Address	R/W	Description	Reset Value
FEAER0	0x4A800050	WO	Force Event Auto CMD12 Error Interrupt Register Error Interrupt (Channel 0)	0x0000
FEAER1	0x4A900050	WO	Force Event Auto CMD12 Error Interrupt Register Error Interrupt (Channel 1)	0x0000

The Force Event Register is not a physically implemented register. Rather, it is an address at which the Auto CMD12 Error Status Register can be written.
Writing 1 : set each bit of the Auto CMD12 Error Status Register
Writing 0 : no effect

Name	Bit	Description	Initial Value
	[15:8]	-	0x0
	[7]	**Force Event for Command Not Issued By Auto CMD12 Error** 1=Interrupt is generated 0=No Interrupt	0
	[6:5]	-	0
	[4]	**Force Event for Auto CMD12 Index Error** 1=Interrupt is generated 0=No Interrupt	0
	[3]	**Force Event for Auto CMD12 End Bit Error** 1=Interrupt is generated	0

		0=No Interrupt	
	[2]	**Force Event for Auto CMD12 CRC Error** 1=Interrupt is generated 0=No Interrupt	0
	[1]	**Force Event for Auto CMD12 Timeout Error** 1=Interrupt is generated 0=No Interrupt	0
	[0]	**Force Event for Auto CMD12 Not Executed** 1=Interrupt is generated 0=No Interrupt	0

ADMA ERROR STATUS REGISTER

When **ADMA Error** Interrupt is occurred, the **ADMA Error States** field in this register holds the ADMA state and the *ADMA System Address* Register holds the address around the error descriptor. For recovering the error, the Host Driver requires the ADMA state to identify the error descriptor address as follows:

ST_STOP: Previous location set in the ADMA System Address register is the error descriptor address
ST_FDS: Current location set in the ADMA System Address register is the error descriptor address
ST_CADR: This sate is never set because do not generate ADMA error in this state.
ST_TFR: Previous location set in the ADMA System Address register is the error descriptor address

In case of write operation, the Host Driver should use ACMD22 to get the number of written block rather than using this information, since unwritten data may exist in the Host Controller.
The Host Controller generates the **ADMA Error** Interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state. In this case, ADMA Error State indicates that an error occurs at ST_FDS state. The Host Driver may find that the Valid bit is not set in the error descriptor.

Register	Address	R/W	Description	Reset Value
ADMAERR0	0x4A800054	R/W	ADMA Error Status Register (Channel 0)	0x00
ADMAERR1	0x4A900054	R/W	ADMA Error Status Register (Channel 1)	0x00

Name	Bit	Description	Initial Value
	[7:3]	Reserved	0x04
	[2]	**ADMA Length Mismatch Error** This error occurs in the following 2 cases. (1) While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. (2) Total data length can not be divided by the block length. '0' = No Error '1'= Error	00
	[1:0]	**ADMA Error State** This field indicates the state of ADMA when error is occurred during	0

		ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. D01 – D00 ADMA Error State when error is occurred Contents of SYS_SDR register '00' = ST_STOP (Stop DMA) Points next of the error descriptor '01' = ST_FDS (Fetch Descriptor) Points the error descriptor '10' = Never set this state (Not used) '11' = ST_TFR (Transfer Data) Points the next of the error descriptor	

ADMA System Address Register

This register contains the physical Descriptor address used for ADMA data transfer.

Register	Address	R/W	Description	Reset Value
ADMASYSADDR0	0x4A800058	R/W	ADMA System Address Register (Channel 0)	0x00
ADMASYSADDR1	0x4A900058	R/W	ADMA System Address Register (Channel 1)	0x00

Name	Bit	Description	Initial Value
	[31:0]	**ADMA System Address** This register holds byte address of executing command of the Descriptor table. 32-bit Address Descriptor uses lower 32-bit of this register. At the start of ADMA, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold valid Descriptor address depending on the ADMA state. The Host Driver shall program Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. ADMA2 ignores lower 2-bit of this register and assumes it to be 00b. 32-bit Address ADMA Register Value 32-bit System Address xxxxxxxx 00000000h 00000000h xxxxxxxx 00000004h 00000004h xxxxxxxx 00000008h 00000008h xxxxxxxx 0000000Ch 0000000Ch …… …… xxxxxxxx FFFFFFFCh FFFFFFFCh	00

10.3 Register fields compared bit-by-bit

S3C6400

HOST CONTROLLER VERSION REGISTER

This register contains the SD Command Argument.

Register	Address	R/W	Description	Reset Value
HCVER0	0x7C2000FE	HWInit	Host Controller Version Register (Channel 0)	0x1300
HCVER1	0x7C3000FE	HWInit	Host Controller Version Register (Channel 1)	0x1300
HCVER2	0x7C4000FE	HWInit	Host Controller Version Register (Channel 2)	0x1300

Name	Bit	Description	Initial Value
	[15:8]	**Vendor Version Number** This status is reserved for the vendor version number. The Host Driver must not use this status. 0x3 : SDMMC3.0 Host Controller	0x13
	[7:0]	**Specification Version Number** This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version. '00' = SD Host Specification Version 1.0 Ohters = Reserved	0x00

S3C6410

HOST CONTROLLER VERSION REGISTER

Register	Address	R/W	Description	Reset Value
HCVER0	0x7C2000FE	HWInit	Host Controller Version Register (Channel 0)	0x0400
HCVER1	0x7C3000FE	HWInit	Host Controller Version Register (Channel 1)	0x0400
HCVER2	0x7C4000FE	HWInit	Host Controller Version Register (Channel 2)	0x0400

Name	Bit	Description	Initial Value
	[15:8]	**Vendor Version Number** This status is reserved for the vendor version number. The Host Driver should not use this status. 0x04 : SDMMC4.0 Host Controller	0x04
	[7:0]	**Specification Version Number** This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version '00' = SD Host Specification Version 1.0	0x01

		'01' = SD Host Specification Version 2.00 Including the feature of the ADMA and Test Register Others = Reserved	

28. MIPI HIS

28.1 Difference summary

There in no change

29. SPI

29.1 Difference summary

There in no change

30. IIC

30.1 Difference summary

S3C6410 supports 2 channels.

30.1.1 Differences with others (S3C6400)

Function	S3C6400	**S3C6410**
# Channel	1 Channel	2 channel

31. UART

31.1 Difference summary

S3C6410 supports 3Mbps Baud Rate.

31.1.1 Differences with others(S3C6400, S3C6410)

Function	S3C6400	S3C6410
Max. Baud Rate	921.6Kbps	3Mbps

32. PWM

32.1 Difference summary

There in no change

33. RTC

33.1 Difference summary

Tick resolution extended to 16 kinds of resolution from 1 kinds of resolution by having more Tick clock sources and Tick counter bits are changed 16bits to 32bits.
Clock range extended to 61.034usec ~ 4,294,967,296 sec

33.1.1 Differences with others(S3C6400)

Function	S3C6400	S3C6410
Tick resolution	1/32768	1/1, **1/2, 1/4, 1/8, 1/16, 1/32, 1/64**, 1/128, **1/256, 1/512, 1/1024**, 1/2048, 1/4096, 1/8192, **1/16384,** 1/32768
Tick counter	16-bit counter (TICNT 16bit)	**32 bit counter (TICNT 32bit)**
Tick read path	rTICKCNT	rTICKCNT
Interrupt Sources	Alarm & TICK	Alarm & TICK
Idle/ Stop/Sleep Wakeup	Alarm & TICK	Alarm & Tick
Idle/Stop/Sleep Interrupt pending after waking up	Alarm : Idle/Stop Tick : Idle/Stop	Alarm : Idle/Stop Tick : Idle/**Stop**
OP. Volt	2.25V ~ 2.75V	2.5V ~ 3.6V
Changed Register		**rTICNT, rRTCCON**
Tick Time Calculation	Period = (n+1) * Tick resolution - Tick resolution : 32768 - n: 16bits	Period = (n+1) * Tick resolution - Tick resolution : 32768 - n:32bits

33.2 Register comparison

33.2.1 6400

Register Name	Address	R/W	Function	Reset Value
RTCCON	0x7E00_5040	R/W	RTC control	0x00
TICNT	0x7E00_5044	R/W	Tick time count register	0x00

33.2.2 6410

Register Name	Address	R/W	Function	Reset Value
RTCCON	0x7E00_5040	R/W	RTC control	0x0
TICNT	0x7E00_5044	R/W	Tick time count register	0x00

33.3 Tick counter clock sources selection

33.3.1 6400

Tick clock source frequency : 32768Hz

Clock range : 0~2 sec

Resolution : 0.03 ms

33.3.2 6410

RTCCON[7:4]	Tick clock source frequency(Hz)	Clock range (s)	Resolution (ms)
4'b0000	32768 (2^15)	0 ~ 2^{17}	0.03
4'b0001	16384 (2^14)	0 ~ 2^{18}	0.06
4'b0010	8192 (2^13)	0 ~ 2^{19}	0.12
4'b0011	4096 (2^12)	0 ~2^{20}	0.24
4'b0100	2048 (2^11)	0 ~ 2^{21}	0.49
4'b0101	1024 (2^10)	0 ~ 2^{22}	0.97
4'b0110	512 (2^9)	0 ~ 2^{23}	1.95
4'b0111	256 (2^8)	0 ~ 2^{24}	3.90
4'b1000	128 (2^7)	0 ~ 2^{25}	7.81
4'b1001	64 (2^6)	0 ~ 2^{26}	15.62
4'b1010	32 (2^5)	0 ~ 2^{27}	31.25
4'b1011	16 (2^4)	0 ~ 2^{28}	62.50
4'b1100	8 (2^3)	0 ~ 2^{29}	125
4'b1101	4 (2^2)	0 ~ 2^{30}	250
4'b1110	2	0 ~2^{31}	500

4’b1111	1	0 ~2^{32}	1000

33.5 Register compare bit by bit

33.5.1 6400

RTCCON	Bit	Description	Initial State
Reserved	[7:4]	Reserved	0

TICNT	Bit	Description	Initial State
Reserved	[31:16]	Reserved	
TICNT	[15:0]	Internal tick counter. 0 ~ 32767	0

33.5.4 6410

RTCCON	Bit	Description	Initial State
TICCKSEL	[7:4]	Tick timer sub clock selection. 4’b0000 = 32768 hz 4’b0001 = 16384 hz 4’b0010 = 8192 hz 4’b0011 = 4096 hz 4’b0100 = 2048 hz 4’b0101 =1024 hz 4’b0110 =512 hz 4’b0111 =256 hz 4’b1000 =128 hz 4’b1001 =64 hz 4’b1010 =32 hz 4’b1011 =16 hz 4’b1100 =8 hz 4’b1101 =4 hz 4’b1110 =2 hz 4’b1111 =1 hz	4’b0000

TICNT	Bit	Description	Initial State
TICCNT	[31:0]	32 bit tick time count value	32’b0

34. WATCH DOG

34.1 Difference summary

There in no change

35. AC97

35.1 Difference summary

There in no change

36. IIS BUS INTERFACE

36.1 Difference summary

S3C6410X support 1ea of 24bit/5.1Ch and 2ea of 24bit/Stereo . This is first to support 24bit and multi channel audio in Samsung AP.

36.1.1 IP version

: I2S V3.21(24bit/Stereo) , I2S V4.0(24bit/Multi-channel)

36.1.2 Difference with S3C6400

Function	S3C6400	S3C6410
Occurrence	16bit/Stereo I2S 2EA	**24bit/Stereo I2S 2EA** **+** **24bit/Multi-Channel(up to 5.1) I2S 1EA**
Sound channel	Only Stereo sound	**Stereo & 5.1ch** sound (6 channel - front left, front right, front center, low frequency, back left, back right)
Data bus type	Serial, 8/16bit per channel data transfers	Serial, 8/16/**24** bit per channel data transfers
Number of controller	2 port	**3 port** (2 port : stereo, 1 port : 5.1ch sound)
Using interrupt	DMA done(INT_DMA)	DMA done(INT_DMA), FIFO underrun(INT_IIS)
Signals	BCLK, LRCLK, CDCLK, SDI, SDO	Two data signals are added from SDO to **SDO[2:0]** in port 1 only
Registers	IISCON, IISMOD, IISFIC, IISPSR, IISTXD, IISRXD	IISCON, IISMOD, IISFIC are updated for supporting 5.1ch sounds in port 1 only IISCON, IISMOD are updated for supporting under-run interrupt and 24bit data in all ports

36.2 Signal summary

Data name and location are added

6400 IIS Pad Name	Location	Functions
I2SLRCK[1:0]	IO	IIS-bus channel select clock
I2SSCLK[1:0]	IO	IIS-bus serial clock
I2SCDCLK[1:0]	O	CODEC system clock
I2SSDI[1:0]	I	IIS-bus serial data input
I2SSDO[1:0]	O	IIS-bus serial data output

6410 IIS Pad Name	Location	Functions
I2SLRCK[1:0]	IO	IIS-bus channel select clock
I2SSCLK[1:0]	IO	IIS-bus serial clock
I2SCDCLK[1:0]	O	CODEC system clock
I2SSDI[1:0]	I	IIS-bus serial data input
I2SSDO[1:0]	O	IIS-bus serial data outputs for stereo sound
I2SLRCK_V40	IO	IIS-bus channel select clock
I2SSCLK_V40	IO	IIS-bus serial clock
I2SCDCLK_V40	O	CODEC system clock
I2SSDI1	I	IIS-bus serial data input
I2SSDO1[2:0]	O	IIS-bus serial data outputs for 5.1 channel sound

36.3 Register comparison

36.3.1 S3C6400 registers

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read / Write	Function
IIS					
IISCON	0x7F002000 0x7F003000		W	R/W	IIS control
IISMOD	0x7F002004 0x7F003004				IIS mode
IISFIC	0x7F002008 0x7F003008				IIS interface FIFO control register
IISPSR	0x7F00200C 0x7F00300C				IIS interface clock divider control register
IISTXD	0x7F002010 0x7F003010			W	IIS interface transmit data register
IISRXD	0x7F002014 0x7F003014			R	IIS interface receive data register

36.3.2 S3C6410 registers

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read / Write	Function
IIS					
IISCON	0x7F002000 0x7F003000		W	R/W	IIS control
IISMOD	0x7F002004 0x7F003004				IIS mode
IISFIC	0x7F002008 0x7F003008				IIS interface FIFO control register

IISPSR	0x7F00200C 0x7F00300C				IIS interface clock divider control register
IISTXD	0x7F002010 0x7F003010			W	IIS interface transmit data register
IISRXD	0x7F002014 0x7F003014			R	IIS interface receive data register
IISCON_V40	0x7F00D000		W	R/W	IIS control
IISMOD_V40	0x7F00D004				IIS mode
IISFIC_V40	0x7F00D008				IIS interface FIFO control register
IISPSR_V40	0x7F00D00C				IIS interface clock divider control register
IISTXD_V40	0x7F00D010			W	IIS interface transmit data register
IISRXD_V40	0x7F00D014			R	IiS interface receive data register

36.4 Register compare bit by bit

S3C6410 has 2 IIS interfaces including added functions, so there is additional register description by bit. It's compared with S3C6400 IIS interface as follows.

36.4.1 S3C6400 registers (stereo 1 port)

IIS CONTROL REGISTER (I2SCON)

Register	Address	R/W	Description	Reset Value
I2SCON	0x7F002000 0x7F003000	R/W	IIS interface control register	0xE00

I2SCON	Bit	R/W	Description	Initial State
Reserved	[31:12]	R/W	Reserved. Program to zero.	0

IIS MODE REGISTER (I2SMOD)

Register	Address	R/W	Description	Reset Value
I2SMOD	0x7F002004 0x7F003004	R/W	IIS interface mode register	0x0

I2SMOD	Bit	R/W	Description	Initial State
Reserved	[31:13]	R/W	Reserved. Program to zero.	0
IMS	[11:10]	R/W	I2S master or slave mode select. 00: Master mode (use PCLK for generating CODECLK) 01: Master mode (use CODECLKI for generating CODECLK) 1x: Slave mode (Please refer Figure 25-2)	0
BLC	[0]	R/W	Bit length per channel. 0: 16-bit, 1: 8-bit	0

36.4.2 S3C6410 registers

36.4.2.1 IIS port 0 (Stereo)

IIS CONTROL REGISTER (IISCON0)

Register	Address	R/W	Description	Reset Value
IISCON	0x7F002000 0x7F003000	R/W	IIS interface control register	0xE00

I2SCON	Bit	R/W	Description	Initial State
Reserved	[31:18]	R/W	Reserved. Program to zero.	0
FTXURSTATUS	[17]	R/W	TX FIFO under-run interrupt status. And this is used by interrupt clear bit. When this is high, you can do interrupt clear by writing '1'. 0 : Interrupt didn't be occurred. 1 : Interrupt was occurred.	0
FTXURINTEN	[16]	R/W	TX FIFO Under-run Interrupt Enable 0: TXFIFO Under-run INT disable 1: TXFIFO Under-run INT enable	0
Reserved	[15:12]	R/W	Reserved. Program to zero.	0

IIS MODE REGISTER (IISMOD0)

Register	Address	R/W	Description	Reset Value
IISMOD	0x7F002004 0x7F003004	R/W	IIS interface control register	0x0

IISMOD	Bit	R/W	Description	Initial State
	[31:15]	R/W	Reserved. Program to zero.	0
BLC	[14:13]	R/W	Bit Length Control Bit Which decides transmission of 8/16 bits per audio channel 00:16 Bits per channel 01:8 Bits Per Channel 10:24 Bits Per Channel 11:Reserved	0
IMS	[11:10]	R/W	IIS master (internal/external) or slave mode select. 00: Master mode (divide mode, using PCLK) 01: Master mode (bypass mode, using I2SCLK) 10: Slave mode (divide mode, using PCLK) 11: Slave mode (bypass mode, using I2SCLK) (Refer to Figure 28-2)	0
	[0]	R/W	Reserved. Program to zero.	0

36.4.2.2 IIS port 1 (5.1 channel)

IIS CONTROL REGISTER (IISCON1)

Register	Address	Description	Reset Value
IISCON_V40	0x7F00D000	IIS interface control register	0xE00

IISCON1	Bit	R/W	Description
FTXURSTATUS	[17]	R/W	TX FIFO under-run interrupt status. And this is used by interrupt clear bit. When this is high, you can do interrupt clear by writing '1'. 0 : Interrupt didn't be occurred. 1 : Interrupt was occurred.
FTXURINTEN	[16]	R/W	TX FIFO Under-run Interrupt Enable 0: TXFIFO Under-run INT disable 1: TXFIFO Under-run INT enable
FTX2EMPT	[15]	R	TX FIFO2 empty Status Indication 0:TX FIFO2 is not empty(Ready to transmit Data) 1:TX FIFO2 is empty (Not Ready to transmit Data)
FTX1EMPT	[14]	R	TX FIFO1 empty Status Indication 0:TX FIFO1 is not empty(Ready to transmit Data) 1:TX FIFO1 is empty (Not Ready to transmit Data)
FTX2FULL	[13]	R	TX FIFO2 full Status Indication 0:TX FIFO2 is not full 1:TX FIFO2 is full

FTX1FULL	[12]	R	TX FIFO1 full Status Indication 0:TX FIFO1 is not full 1:TX FIFO1 is full

IIS MODE REGISTER (IISMOD1)

Register	Address	Description	Reset Value
IISMOD_V40	0x7F00D004	IIS interface mode register	0x0

IISMOD	Bit	R/W	Description
	[31:22]	R/W	Reserved. Program to zero.
CDD2	[21:20]	R/W	Channel-2 Data Discard. Discard means zero padding. It only supports 8/16 bit mode. 00 : No Discard 01 : I2STXD[15:0] Discard 10 : I2STXD[31:16] Discard 11 : Reserved
CDD1	[19:18]	R/W	Channel-1 Data Discard. Discard means zero padding. It only supports 8/16 bit mode. 00 : No Discard 01 : I2STXD[15:0] Discard 10 : I2STXD[31:16] Discard 11 : Reserved
DCE	[17:16]	R/W	Data Channel Enable. [17] : SD2 channel enable [16] : SD1 channel enable
	[15]	R/W	Reserved, Program to Zero
BLC	[14:13]	R/W	Bit Length Control Bit Which decides transmission of 8/16 bits per audio channel 00:16 Bits per channel 01:8 Bits Per Channel 10:24 Bits Per Channel 11:Reserved
IMS	[11:10]	R/W	IIS master (internal/external) or slave mode select. 00: Master mode (divide mode, using PCLK) 01: Master mode (bypass mode, using I2SCLK) 10: Slave mode (divide mode, using PCLK) 11: Slave mode (bypass mode, using I2SCLK) (Refer to Figure 28-2)
	[0]	R/W	Reserved. Program to zero.

IIS FIFO CONTROL REGISTER (IISFIC1)

Register	Address	Description	Reset Value
IISFIC_V40	0x7F00D008	IIS interface FIFO control register	0x0

IISFIC1	Bit	R/W	Description
	[31:29]	R/W	Reserved. Program to zero.
FTX2CNT	[28:24]	R	TX FIFO2 data count. FIFO has 16 depth, so value ranges from 0 to 15. N: Data count N of FIFO
	[23:21]	R/W	Reserved. Program to zero.
FTX1CNT	[20:16]	R	TX FIFO1 data count. FIFO has 16 depth, so value ranges from 0 to 15. N: Data count N of FIFO

36.5 Software modification points

If user want to use similarly as S3C6400, sentences of bold character should be implemented, but other points are compatible with S3C6400.

	S3C6410
Control setting	1) It's added under-run interrupt enable bit and status bits of FIFO1, FIFO2 in IISCON, and data channel setting bits in IISMOD. If user want to use similarly as S3C6400, those bits should be set '0' 2) It's modified BLC setting bits from IISMOD[0] to IISMOD[14:13] for supporting 24bit sound data. **If user want to use similarly as S3C6400, IISMOD[14:13] bits should be set same as S3C6400 BLC setting value.**
Using interrupt	If user want to use similarly as S3C6400, under-run interrupt enabe bit should be set '0'. Otherwise, if user want to use under-run interrupt, you will add an ISR for under-run interrupt.
Data transmit	If user want to use similarly as S3C6400, data channel enabe bits should be set '0'. Otherwise, if user want to use added data channel, it should be set enable data channel and added data handling codes for supporting 5.1 channel sound.

37. PCM AUDIO

37.1 Difference summary

There in no change

38. IRDA

38.1 Difference summary

There in no change

39. ADC&TOUCH SCREEN INTERFACE

39.1 Difference summary

39.1.1 Differences with others(S3C6400, S3C6410)

S3C6410 12bit 8channel.

Function	S3C6400	S3C6410
Analog input	8 channel	8channel
Resolution	10bit	12bit

39.2 Register comparison

39.2.1 6400

Register	Address	R/W	Description	Reset Value
ADCCON	0x7E00B000	R/W	ADC Control Register	0x3FC4

Register	Address	R/W	Description	Reset Value
ADCDAT0	0x7E00B00C	R	ADC Conversion Data Register	-

Register	Address	R/W	Description	Reset Value
ADCDAT1	0x7E00B010	R	ADC Conversion Data Register	-

39.2.2 6410

Register	Address	R/W	Description	Reset Value
ADCCON	0x7E00B000	R/W	ADC Control Register	0x3FC4

Register	Address	R/W	Description	Reset Value

ADCDAT0	0x7E00B00C	R	ADC Conversion Data Register	-

Register	Address	R/W	Description	Reset Value
ADCDAT1	0x7E00B010	R	ADC Conversion Data Register	-

39.3 Register compare bit by bit

39.3.1 6400

ADCCON	Bit	Description	Initial State
Reserved	[16]	Reserved	0
ECFLG	[15]	End of conversion flag(Read only) 0 = A/D conversion in process 1 = End of A/D conversion	0
PRSCEN	[14]	A/D converter prescaler enable 0 = Disable 1 = Enable	0
PRSCVL	[13:6]	A/D converter prescaler value Data value: 5 ~ 255 (This A/D converter was designed to operate at maximum 2.5MHz clock)	0xFF
SEL_MUX	[5:3]	Analog input channel select 000 = AIN 0 001 = AIN 1 010 = AIN 2 011 = AIN 3 100 = YM 101 = YP 110 = XM 111 = XP	0
STDBM	[2]	Standby mode select 0 = Normal operation mode 1 = Standby mode	1
READ_ START	[1]	A/D conversion start by read 0 = Disable start by read operation 1 = Enable start by read operation	0
ENABLE_START	[0]	A/D conversion starts by enable. If READ_START is enabled, this value is not valid.	0

		0 = No operation 1 = A/D conversion starts and this bit is cleared after the start-up.	

ADCDAT0	Bit	Description	Initial State
UPDOWN	[15]	Up or Down state of Stylus at Waiting for Interrupt Mode. 0 = Stylus down state. 1 = Stylus up state.	-
AUTO_PST	[14]	Automatic sequencing conversion of X-Position and Y-Position 0 = Normal ADC conversion. 1 = Sequencing measurement of X-position, Y-position.	-
XY_PST	[13:12]	Manually measurement of X-Position or Y-Position. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	-
Reserved	[11:10]	Reserved	
XPDATA (Normal ADC)	[9:0]	X-Position Conversion data value (include Normal ADC Conversion data value) Data value : 0 ~ 3FF	-

ADCDAT1	Bit	Description	Initial State
UPDOWN	[15]	Up or Down state of Stylus at Waiting for Interrupt Mode. 0 = Stylus down state. 1 = No stylus down state.	-
AUTO_PST	[14]	Automatically sequencing conversion of X-Position and Y-Position 0 = Normal ADC conversion. 1 = Sequencing measurement of X-position, Y-position.	-
XY_PST	[13:12]	Manually measurement of X-Position or Y-Position. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	-
Reserved	[11:10]	Reserved	
YPDATA	[9:0]	Y-Position Conversion data value Data value : 0 ~ 3FF	-

39.3.2 6410

ADCCON	Bit	Description	Initial State
RESSEL	[16]	A/D converter resolution selection 0 = 10 bit A/D conversion 1 = 12 bit A/D conversion	0
ECFLG	[15]	End of conversion flag(Read only) 0 = A/D conversion in process 1 = End of A/D conversion	0
PRSCEN	[14]	A/D converter prescaler enable 0 = Disable 1 = Enable	0
PRSCVL	[13:6]	A/D converter prescaler value Data value: 5 ~ 255 (This A/D converter was designed to operate at maximum 2.5MHz clock)	0xFF
SEL_MUX	[5:3]	Analog input channel select 000 = AIN 0 001 = AIN 1 010 = AIN 2 011 = AIN 3 100 = YM 101 = YP 110 = XM 111 = XP	0
STDBM	[2]	Standby mode select 0 = Normal operation mode 1 = Standby mode	1

READ_ START	[1]	A/D conversion start by read 0 = Disable start by read operation 1 = Enable start by read operation	0
ENABLE_STA RT	[0]	A/D conversion starts by enable. If READ_START is enabled, this value is not valid. 0 = No operation 1 = A/D conversion starts and this bit is cleared after the start-up.	0

ADCDAT0	Bit	Description	Initial State
UPDOWN	[15]	Up or Down state of Stylus at Waiting for Interrupt Mode. 0 = Stylus down state. 1 = Stylus up state.	-
AUTO_PST	[14]	Automatic sequencing conversion of X-Position and Y-Position 0 = Normal ADC conversion. 1 = Sequencing measurement of X-position, Y-position.	-
XY_PST	[13:12]	Manually measurement of X-Position or Y-Position. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	-
XPDATA_12	[11:10]	When A/D resolution is 12bit X-position conversion data[11:0] value	
XPDATA (Normal ADC)	[9:0]	X-Position Conversion data value (include Normal ADC Conversion data value) Data value : 0 ~ 3FF	-

ADCDAT1	Bit	Description	Initial State
UPDOWN	[15]	Up or Down state of Stylus at Waiting for Interrupt Mode. 0 = Stylus down state. 1 = No stylus down state.	-
AUTO_PST	[14]	Automatically sequencing conversion of X-Position and Y-Position 0 = Normal ADC conversion. 1 = Sequencing measurement of X-position, Y-position.	-
XY_PST	[13:12]	Manually measurement of X-Position or Y-Position. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	-

YPDATA_12	[11:10]	When A/D resolution is 12bit Y-position conversion data[11:0] value	
YPDATA	[9:0]	Y-Position Conversion data value Data value : 0 ~ 3FF	-

40. KEY INTERFACE

40.1 Difference summary

There in no change

41. GRAPHIC3D(NEW)

Features

- 4M triangles/s @133MHz (Transform Only)
- 75.8M pixels/s fill-rates @133MHz (shaded pixels)
- Programmable Shader Model 3.0 support
- 128-bit (32-bit x 4) Floating-point Vertex Shader
  - Geometry-texture cache support
- 128-bit (32-bit x 4) Floating-point two Fragment Shaders
- Max. 4K x 4K frame-buffer (16/32-bpp)
- 32-bit depth buffer (8-bit stencil/24-bit Z)
- Texture format: 1/2/4/8/16/32-bpp RGB, YUV 422, S3TC Compressed
- Support max. 8 surfaces (max. 8 user-defined textures)
- API Support: OpenGL ES 1.1 & 2.0, D3D Mobile
- Intelligent Host Interface
  - 15 input data-types, Vertex Buffer & Vertex Cache
- H/W Clipping (Near & Far)
- 8-stage five-threaded Shader architecture
- Primitive assembly & hard-wired triangle setup engine
- One pixels/cycle hard-wired rasterizer
- One texturing engine (one bilinear-filtered texel/cycle each)
  - Nearest/bilinear/trilinear filtering
  - 8-layered multi-texturing support
- Fragment processing: Alpha/Stencil/Z/Dither/Mask/ROP
- Memory bandwidth optimization through hierarchical caching
  - L1/L2 Texture-caches, Z/Color caches
- System bus interface
  - Host interface: 32-bit AHB (AMBA 2.0)
  - Memory Interface: two 64-bit AXI (AMBA 3.0) channels