SAMSUNG ELECTRONICS

S3C2450/51/16 Routing Guide

S3C2450/51/16

RISC Microprocessor

August 26, 2008

REV 0.00

Important Notice

The information in this publication has been carefully checked and is believed to be entirely accurate at the time of publication. Samsung assumes no responsibility, however, for possible errors or omissions, or for any consequences resulting from the use of the information contained herein.

Samsung reserves the right to make changes in its products or product specifications with the intent to improve function or design at any time and without notice and is not required to update this documentation to reflect such changes.

This publication does not convey to a purchaser of semiconductor devices described herein any license under the patent rights of Samsung or others.

Samsung makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Samsung assume any liability arising out of the application or use of any product or circuit and specifically disclaims any and all liability, including without limitation any consequential or incidental damages.

"Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by the customer's technical experts.

Samsung products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, for other applications intended to support or sustain life, or for any other application in which the failure of the Samsung product could create a situation where personal injury or death may occur.

Should the Buyer purchase or use a Samsung product for any such unintended or unauthorized application, the Buyer shall indemnify and hold Samsung and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that Samsung was negligent regarding the design or manufacture of said product

.

S3C2450/16X RISC Microprocessor
Routing Guide, Revision 0.00

Samsung Electronics Co., Ltd.
San #24 Nongseo-Dong, Giheung-Gu
Yongin-City Gyeonggi-Do, Korea
446-711

Home Page: http://www.samsungsemi.com/

E-Mail: mobilesol.cs@samsung.com

Printed in the Republic of Korea

Revision History

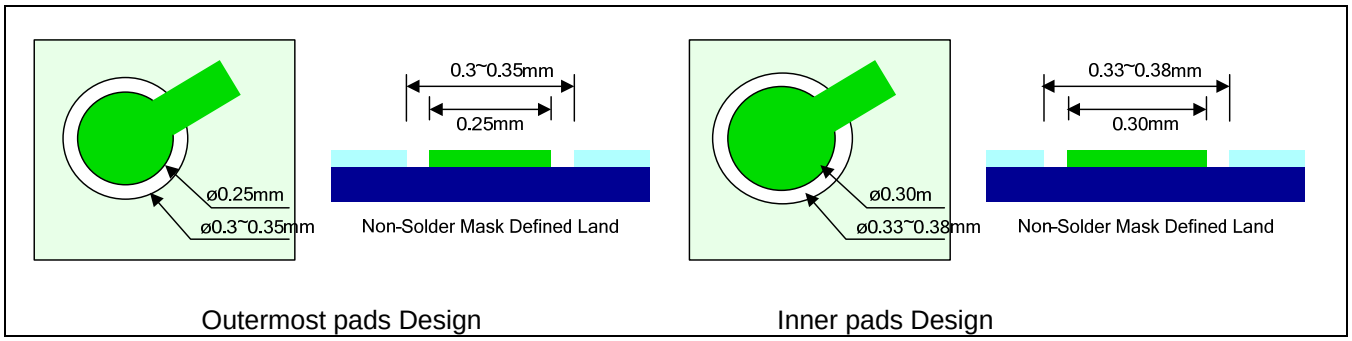
Revision No	Description of Change	Refer to	Author(s)	Date
0.00	- Initial Release for review	-		August 26, 2008
	-			

Table of Contents

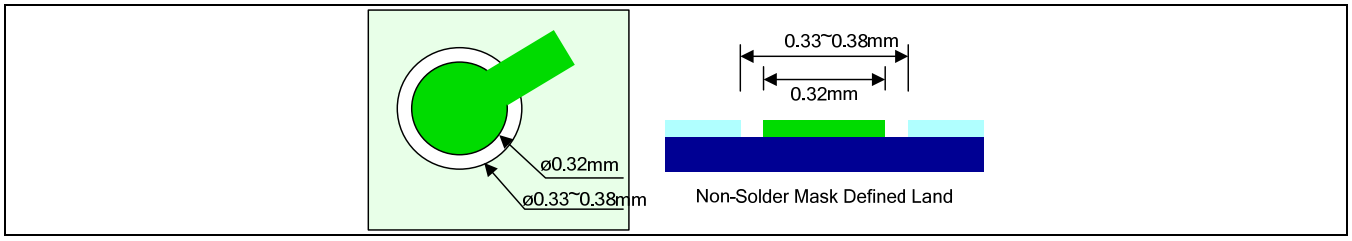
1. LAND SIZE

It is of great importance to properly design the PCB land pad of FBGA package in terms of productivity of mass-produced board. It is better to match the size of PCB land pad with that of FBGA package. There are two methods for forming the land in PCB.

Land size is made smaller than the solder mask to form the land. The Land size is determined according to etching time generated in the course of producing PCB. This method is a little better for routing because of small area of copperplate, compared to the SMD method.



S3C2450 Land Size



S3C2451 & S3C2416 Land Size

Note:
Values on this material are just recommended values and can be changed from PCB manufacture and assembly capability.

2. VIA HOLE

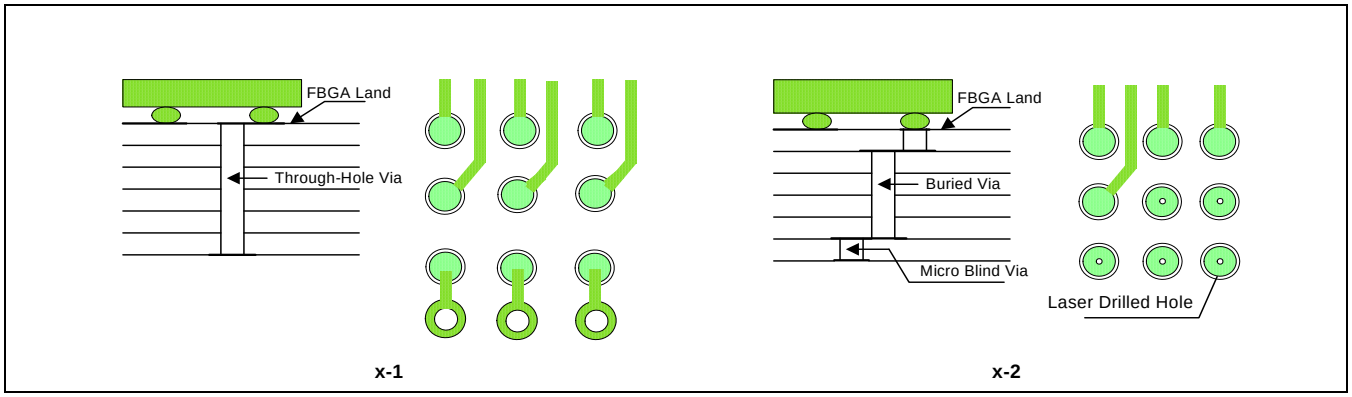
In multi-layered PCB, via is the only method to enable electrical connection of signals between layers. Using via properly facilitates the layout of parts. In case of highly integrated board, via size becomes more important. It is because the small-sized via allows more routing space and the increased insertion rate of parts.

The through-hole via is the most frequently used type of via. However, it is not suitable for PCB routing and component layout since it occupies much area of PCB. In particular, if the through-hole via is used for FBGA package, via hole matrix is formed on the opposite side of PCB, causing restriction in the layout of trace and component. (See Figure x-1)

If you want to facilitate routing on Board and increase the area of insertion for parts, it is more useful to use the following two via techniques.

- **Micro Blind Via**
  Possible to minimize the size of via by forming 'via' using very small-sized laser-drill (usually 4um). However, it is possible to connect one side of PCB only to the neighboring layer. When using the FBGA package, the user can get much space for routing, if the combination of PCB and via is used (See Figure x-2). In addition, it facilitates both-side insertion because via does not appear on the opposite side of PCB.

- **Buried Via**
  Via technique allowing connection from inner layer to inner layer of PCB, which is buried under the external surface of PCB. It is also used to interconnect Micro blind vias. (See Figure x-2)



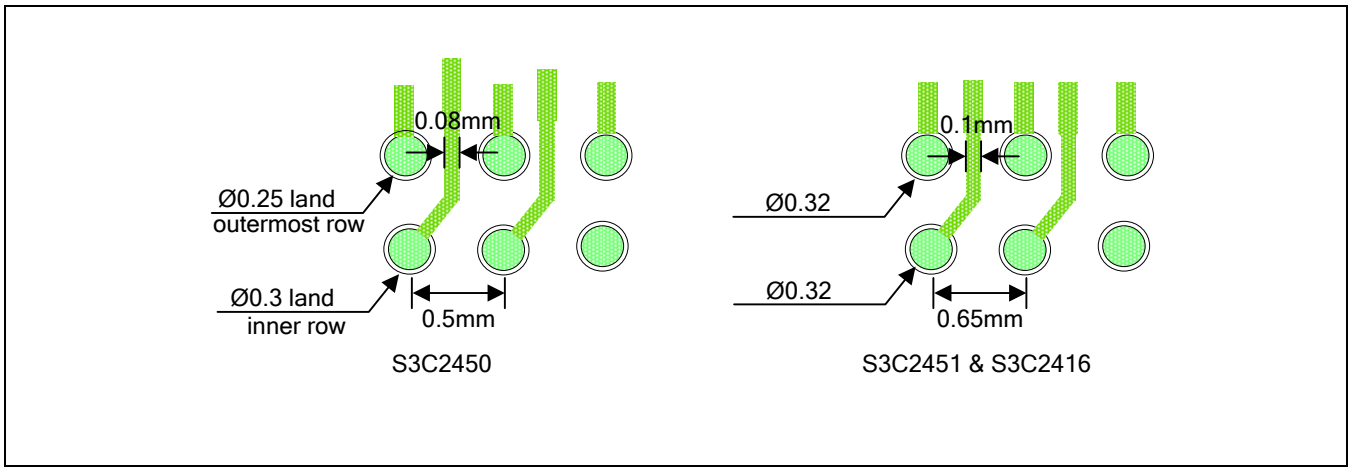
x-1 x-2

3. ROUTING GUIDE

3.1. Trace Width & Clearance

This section describes how to perform routing while properly maintaining the width and interval of trace in FBGA package land.

It is required to extract many signal traces from narrow space and it is not easy for each trace to maintain desired characteristic impedance. Using too narrow trace might cause a problem in PCB manufacture and increase the costs of PCB manufacture. The following figure illustrates the width and interval of trace the user can observe when using the land pad as explained in the previous chapter.



Note:
Values on this material are just recommended values and can be changed from PCB manufacture and assembly capability.

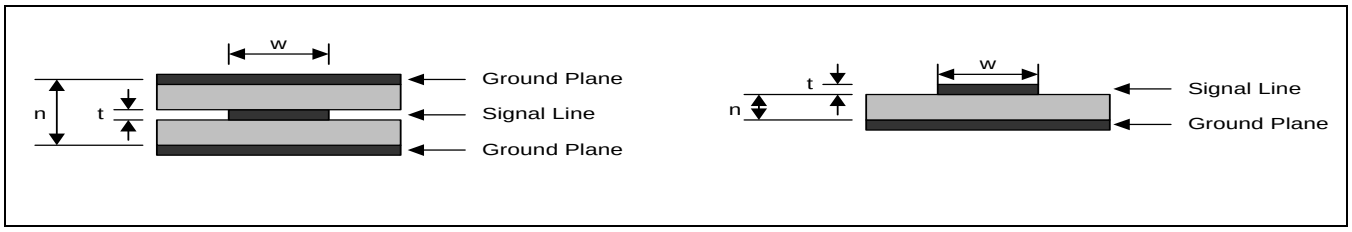
3.2. Transmission Line Impedance

This section describes two-transmission line impedance's that can be implemented on the PCB.

- **Strip line**
  The signal line is inserted between upper and lower layer power planes in order to implement transmission line. It is advantageous in that clean signals can be transmitted because the power plane has shield effects on both sides, but it must pass the via in order to connect to the element.

- **Microstrip line**
  The signal line is placed on the outer layer and ground plane is placed at the next neighboring layer. This is easier to implement than the Strip line.

The following example illustrates characteristic impedance of the two transmission lines.



Transmission line capacitance, Inductance, Z0 and TPD can be calculated with PCB size and material dielectric constant.

For Stripline

$$Z_0 = \frac{60}{\sqrt{\varepsilon_R}} \ln \frac{4h}{0.67\pi w\,(0.8 + \frac{t}{w})}\ \Omega$$

$$t_{PD} = 1.017\sqrt{\varepsilon_R}\ ns/ft$$

$$C_0 = 1000\,\frac{t_{PD}}{Z_0}\ pF/ft$$

$$L_0 = Z_0^2 C_0\ pH/ft$$

For Microstrip

$$Z_0 = \frac{87}{\sqrt{\varepsilon_R + 1.41}} \ln \frac{5.98h}{0.8w + t}\ \Omega$$

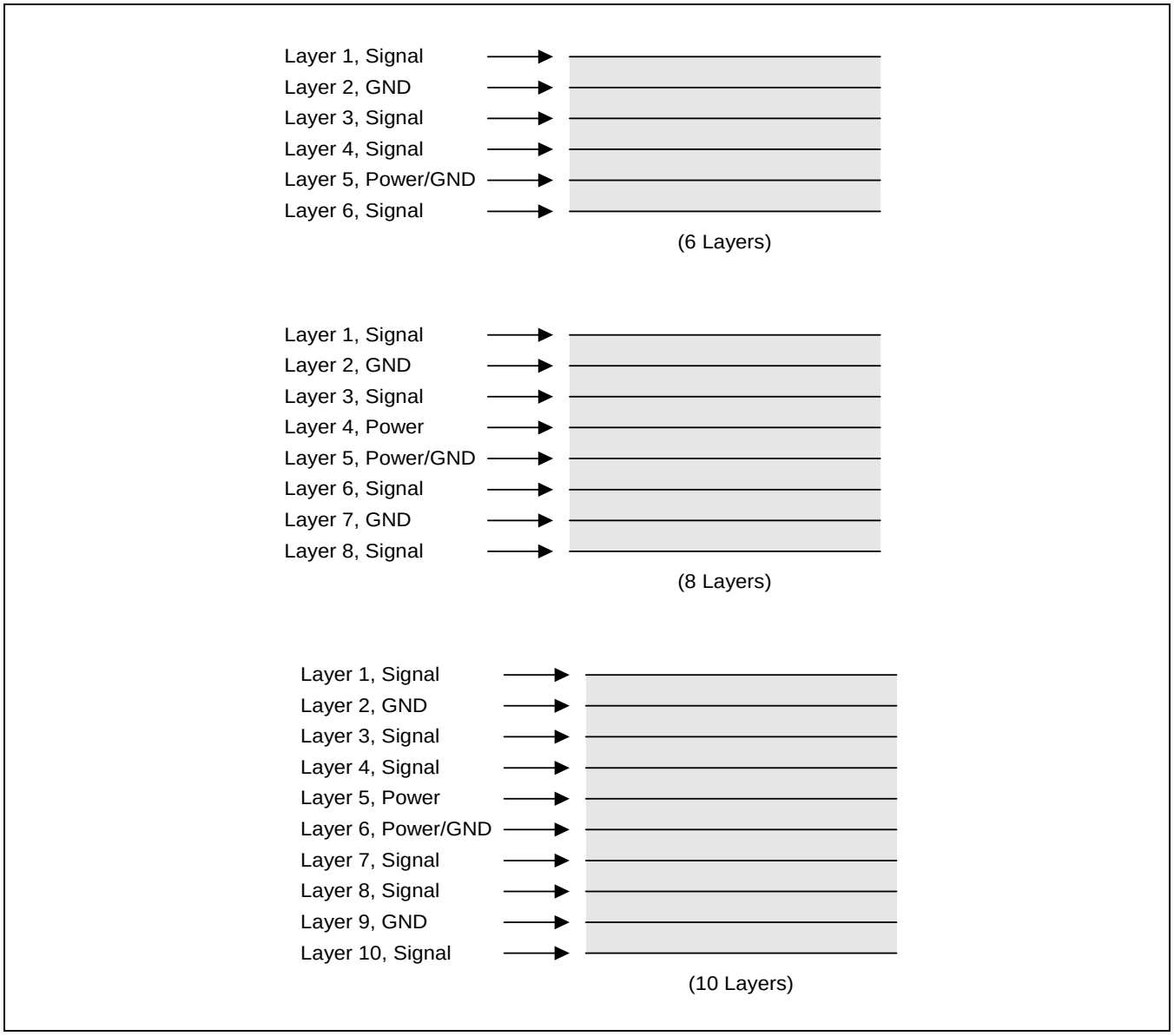
$$t_{PD} = 1.017\ \sqrt{0.457\varepsilon_R + 0.67}\ ns/ft$$

$$C_0 = 1000\,\frac{t_{PD}}{Z_0}\ pF/ft$$

$$L_0 = Z_0^2 C_0\ pH/ft$$

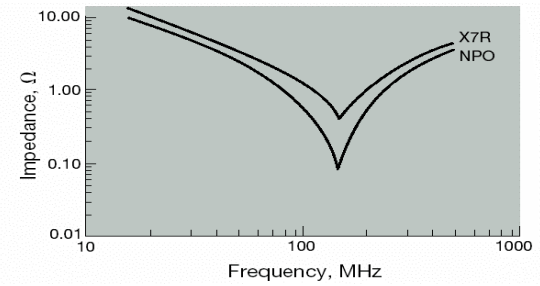
4. LAYER STACK-UP

To easily implement the impedance line, the PWR or GND plane must be placed in the layer adjacent to the signal line. The following examples illustrate the proper use of layers.



5. DECOUPLING CAP AND VIA HOLE LAYOUT

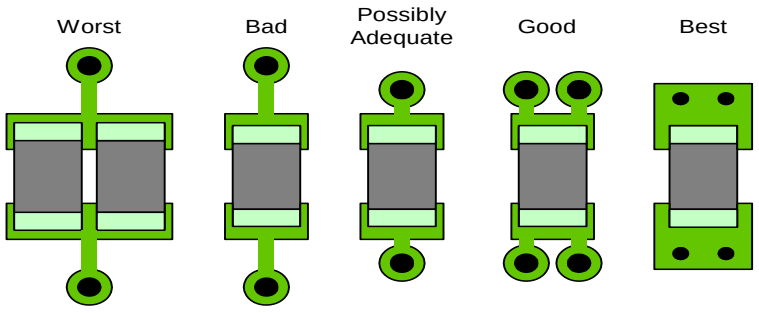
The decoupling capacitor of sufficient capacity must be placed in the high frequency switching device, for the supply of necessary power in the shortest distance. If dcap lacks capacity or supplied path impedance is too high, switching noise is generated and it becomes the source of radiation. Dcap must use a proper capacitor type according to the frequency. Since Dcap impedance is x= sqrt (r2+…) and parasitic inductance value can be dominant according to the frequency, be sure to use it in consideration of frequency bandwidth that acts as capacitor.



F = 1/(2×pi×sqrt (LC))

The Dcap must have enough capacity to supply power during the signal transition.

If possible, the decoupling capacitor must be basically placed closer to the power pin of a desired device. When using PCB pad, in addition, do not connect more than 2 decoupling capacitors to one via. The PWR/GND read trace used for decoupling capacitor installation must be routed short, if possible.

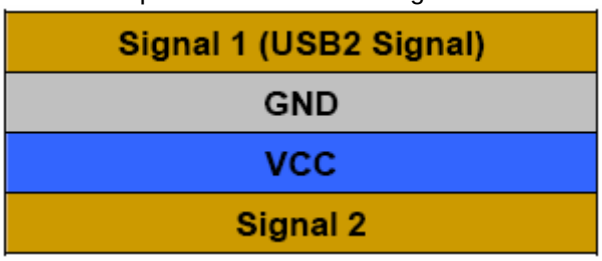


6. SIGNAL ROUTING

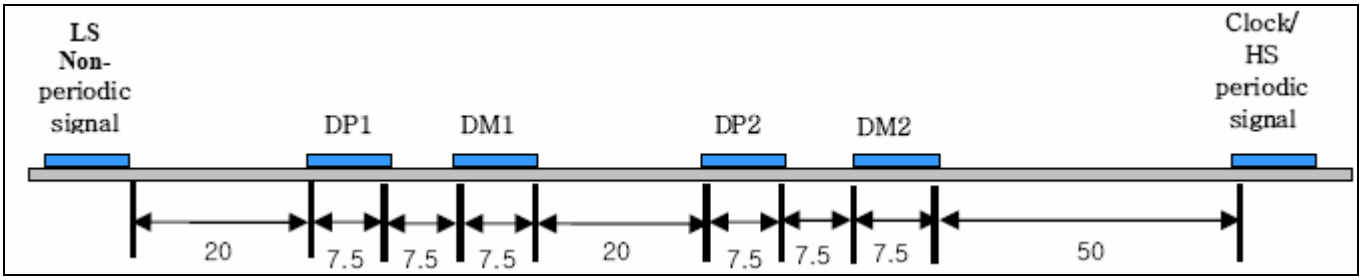
6.1. USB Signal

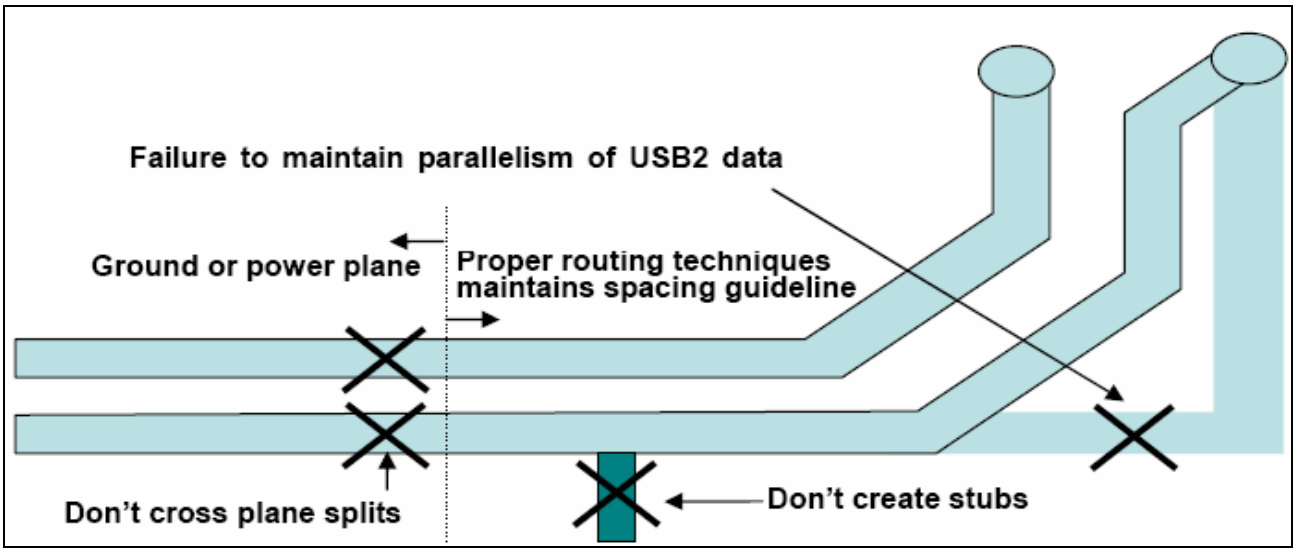
This document conducts a guide to integrate a discrete high speed USB device onto a four layer PCB. The board design guidelines handle trace separation, termination placement requirements and overall trace length guidelines.
When an engineer lays out a new design, the excellent signal quality and minimized EMI problem must be required. That is based on four layer board. The first layer is for signal layer. The second layer is for ground. The third layer is for power and the fourth layer is for signal layer again. We should basically consider the following instruction.

- HS signals should be placed on top shown in the below figure.



- HS clock and HS USB different pairs should be first routed with minimum trace length.
- Route high-speed USB signals not using Vias and stubs with using two 45 degree turns or an arc instead of making a single 90 degree turn. This reduces signal reflections and impedance changes that affect signal quality.
- Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- Route all traces over continuous planes (VCC and GND), with no interruptions. Avoid crossing over anti-etch if at all possible.
- Their parallelism between USB differential signals with the trace spacing should be maintained. The deviation should be minimized.
- The minimized length of high speed clock and periodic signal traces is highly recommended. The suggested spacing to clock signal is 50mils (1mils = 0.0254mm)
- To prevent crosstalk, you should 20-mil minimum spacing between HS USB signal pairs. For example,
- Max trace length mismatch between HS USB signal pairs such as DM and DP should be under 150mils.





Note:
X: Poor routing mistake

6.2. Guidance notes for mSDR/mDDR/DDR2 signal routing

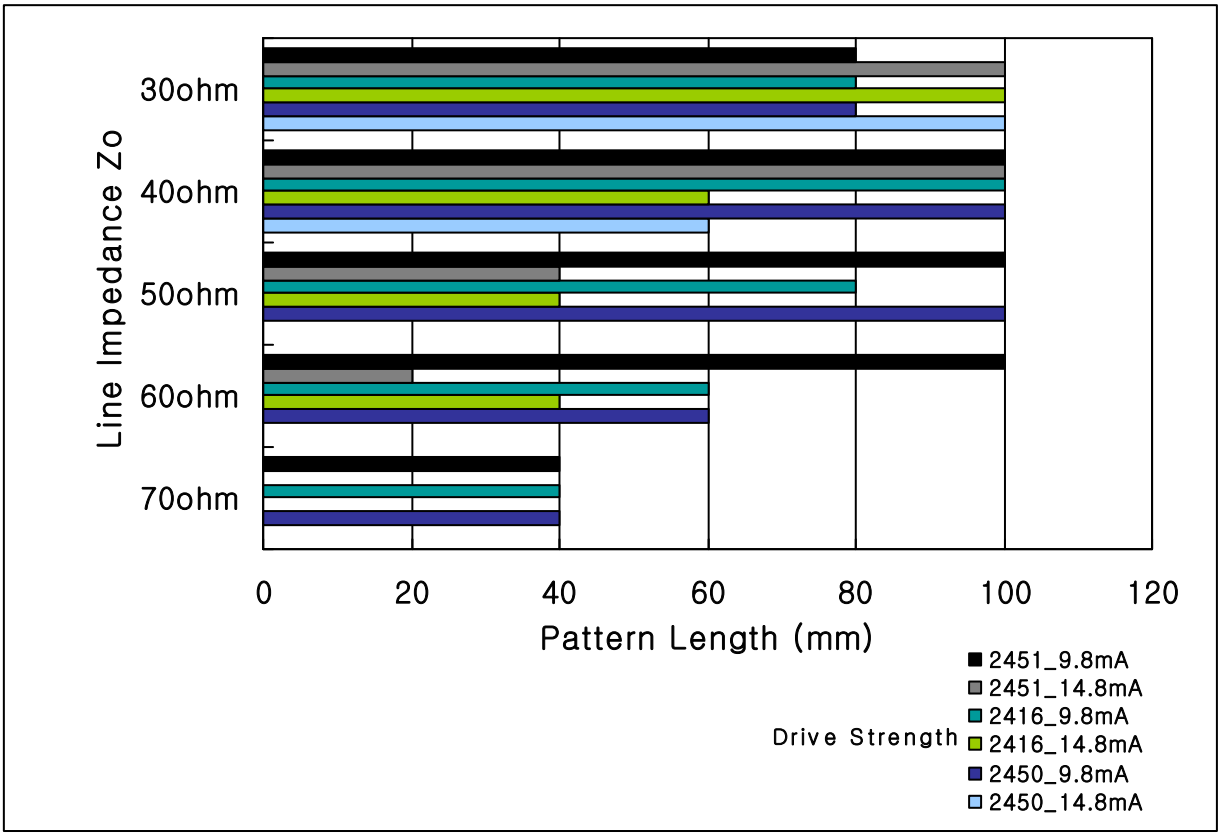
- Common design guidelines
  - All signals are simulated load capacitance at 15pF@133MHz. So, all capacitance including the board parasitic must be smaller than 15pF.
  - Line impedance same for all signal layers.
  - Minimize the branch length.
  - Signal net have reference is VSS plane.
  - Route most segments in inner layer.
  - Power signal must be reinforced as soon as possible. Also, the bypass capacitor has to be nearest to the power pads.
  - Place 2 more decoupling capacitors for power net per a DRAM.
  - Use solid VDD/VSS plane for DRAM.

- Design guidelines for DATA, DQS and DQM net
  - Lengths of DATA, DQS and DQM in a byte are in target range. (Target length -/+ 1.0mm)
  - Space between DATA signals is recommended to 3*WIDTH.
  - Use same number of vias in DATA net or compensate length.

- Design guidelines for SCLK and SCLKn
  - Star topology is recommenced.
  - Route as same length in same layer.
  - Recommended differential impedance is 100 ohm.
  - Spacing from clock net to other net are more than 3*WIDTH.

- Design guidelines for control signals
  - T-branch topology is recommenced for Command, Address and Control net. (CKE, CSn[1:0], ADDR[`5:0], RASn, CASn, WEn)
  - Do not route near high speed signals (SCLK, SCLKn, DATA net) or have enough spacing over 3*WIDTH.

- Pattern Length guidelines
  - According to line impedance and drive strength, pattern length is put in the range of value described as below.
  - This value is available in the case of using mDDR/DDR2 @ ~133MHz. (VDD and VDDQ=1.7V)



6.3. Guidance notes for Power signal routing

This table shows the mainly effective pin number for each power domain. Please route first these pin when power signals are routed.

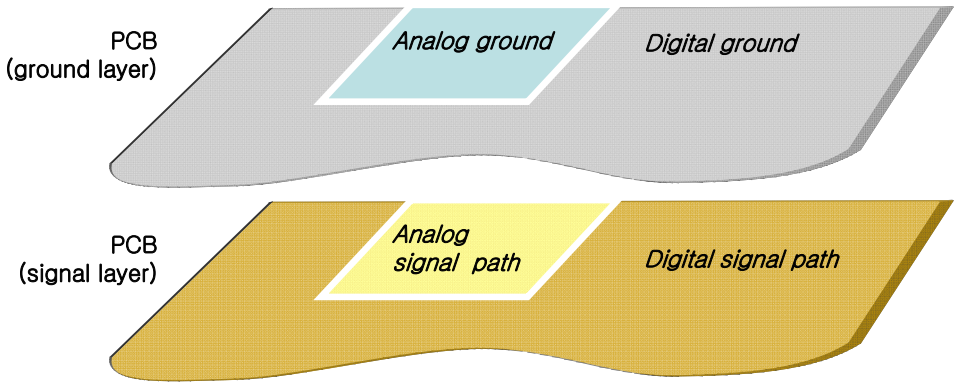
Net Name	S3C2450 Pin Number	S3C2451	S3C2416 Pin Number
VDD_SDRAM	C13, D13, G17, H20, C15	C12, D16, C17, F18, E19	A12, C16, H14
VDD ARM	P4, T4, U4, V4, Y6, AB11	L4, M3, N4, T4, V5, V8, V9	J2, K2, N3, V5, W8, W9
VSS	A18, D22, J14, Y10, Y7, Y8, N2, N4, D16, L4, Y13, N17, D7	D7, D9, E18, D19, L2, G18, N19, T18, W12, W9, W8, V6, P3, M4, K4, L13	B11, C15, K3, L3, P3, U7, U8, U9,H13, J3, L6

6.4. Layout guide for Audio codec & signal

1. For general layout guide, please refer the Codec chip manual.

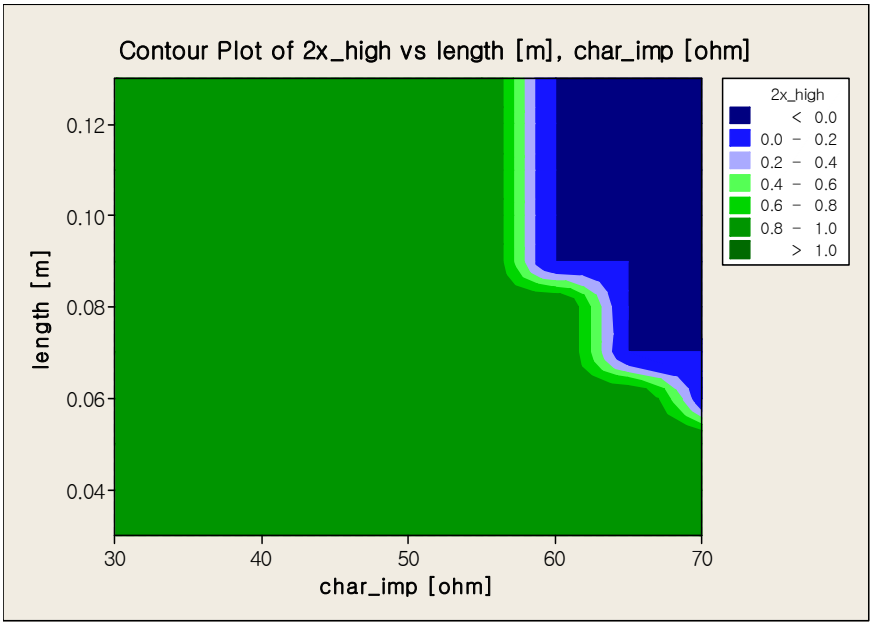
2. Separate analog and digital ground at ground PCB layer with isolation area(white bold line)

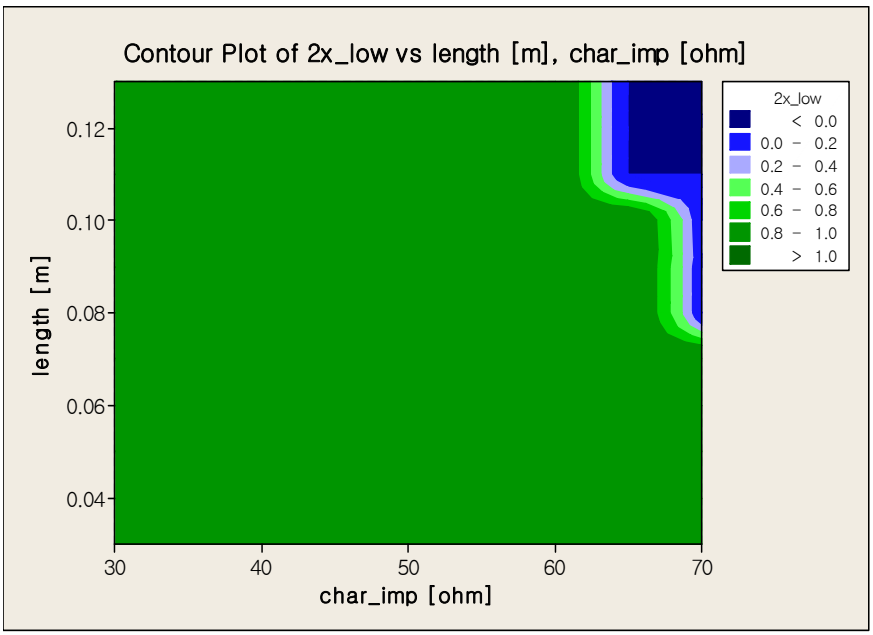
3. Analog signal at signal layer should pass over/under analog ground, also Digital signal should pass over/under digital ground.



6.5. Layout guide for HS-SPI signal routing

Next pictures show the signal reflection related with trace length and characteristic impedance.
The physical HS-SPI traces should be in green range in the picture.





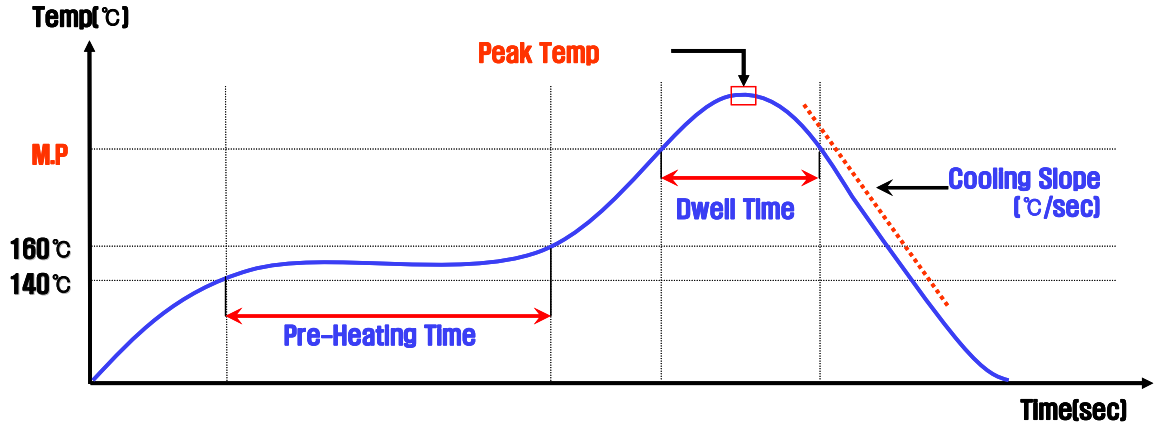
7. REFLOW PROFILE

➢ IR Reflow Condition in the Preconditioning Test

Reflow Profile

Machine No.	Pre-Heating Time	Dwell Time	Peak Temp.	Cooling Slope
Spec	60 ~ 100sec	30 ~ 50sec	230 ~ 240℃	-5 ~ -1 ℃/sec
S3C2451&S3C2416	79 sec	43 sec	234 ℃	-4.88 ℃/sec
S3C2450	84 sec	37 sec	233 ℃	-1.50 ℃/sec

※Conventional Profile (RSS)



➢ Storage and using condition for the BGA package

Items	Specification
Storage condition after unpacking the MBB (Moisture Barrier Bag)	30℃ / 60% RH
Using condition after unpacking the MBB	Within 168hours after opening the MBB
Re-bake condition	Minimum 4 hours at 125℃ when more than 7 days has passed after unpacking the MBB

8. EMI REDUCTION

- Close coupling between conductors of a pair not only reduces EMI, but it helps to ensure noise coupled onto the conductors will do so equally as common mode noise which will then be rejected by the receiver.
- Imbalance minimization is the other important factor in reducing EMI.
- The basic rule to follow is: if any discontinuity must be introduced in proximity to differential lines, it should be introduced equally to both members of the pair.