S3C2413X

32-BIT RISC
MICROPROCESSOR
USER'S MANUAL

Revision 1.07

SAMSUNG ELECTRONICS

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1 PRODUCT OVERVIEW

INTRODUCTION

This manual describes SAMSUNG's S3C2413X 16/32-bit RISC microprocessor. This product is designed to provide hand-held devices and general applications with cost-effective, low-power, and high-performance micro-controller solution in small die size. To reduce total system cost, the S3C2413X includes the following components separate 8KB Instruction and 8KB Data Cache, MMU to handle virtual memory management, LCD Controller (65K CSTN & TFT), NAND Flash Boot Loader, OneNAND Controller, System Manager (chip select logic and SDRAM/DDR Controller), 3-ch UART, 4-ch DMA, 4-ch Timers with PWM, I/O Ports, RTC, 8-ch 10-bit ADC and Touch Screen Interface, IIC-BUS Interface, IIS-BUS Interface, USB Host, USB Device, SD Host & Multi-Media Card Interface, 2-ch SPI and PLL for clock generation.

The S3C2413X was developed using an ARM926EJ-S core, 0.13um CMOS standard cells and a memory complier. Its low-power, simple, elegant and fully static design is particularly suitable for cost- and power-sensitive applications. It adopts a new bus architecture called Advanced Microcontroller Bus Architecture (AMBA).

The S3C2413X offers outstanding features with its CPU core, a 16/32-bit ARM926EJ-S RISC processor designed by Advanced RISC Machines, Ltd. The ARM926EJ-S implements MMU, AMBA BUS, and Harvard cache architecture with separate 8KB instruction and 8KB data caches, each with an 8-word line length.

By providing a complete set of common system peripherals, the S3C2413X minimizes overall system costs and eliminates the need to configure additional components. The integrated on-chip functions that are described in this document include:

- 1.4V arm, 1.25V internal, 1.8V/2.5V/3.3V memory, 2.5V/2.8V/3.3V external I/O microprocessor with 8KB I-Cache/8KB D-Cache/MMU
- External memory controller (SDRAM/DDR Control and Chip Select logic)
- LCD controller (up to 65K color STN and 16M color TFT) with 1-ch LCD-dedicated DMA
- 4-ch DMAs with external request pins
- 3-ch UART (IrDA1.0, 64-Byte Tx FIFO, and 64-Byte Rx FIFO) / 2-ch SPI
- 1-ch multi-master IIC-BUS/1-ch IIS-BUS controller
- SD Host interface version 1.0 & Multi-Media Card Protocol version 2.11 compatible
- 2-port USB Host /1- port USB Device (ver 1.1)
- 4-ch PWM timers & 1-ch internal timer
- Watch Dog Timer
- 129-bit general purpose I/O ports / 24-ch external interrupt source
- Camera interface (Max. 1600 x 1200 pixels input support. 1600 x 1200 pixel input support for scaling)
- Power control: Normal, Idle, stop and Sleep mode
- 8-ch 10-bit ADC and Touch screen interface
- RTC with calendar function
- On-chip clock generator with PLL

FEATURES

Architecture

- Integrated system for hand-held devices and general embedded applications
- 16/32-Bit RISC architecture and powerful instruction set with ARM926EJ-S CPU core
- ARM's Jazelle Java technology enhanced ARM architecture MMU to support WinCE, Symbian and Linux
- Instruction cache, data cache, write buffer and Physical address TAG RAM to reduce the effect of main memory bandwidth and latency on performance
- ARM926EJ-S CPU core supports the ARM debug architecture.
- Internal Advanced Microcontroller Bus Architecture (AMBA) (AMBA2.0, AHB/APB)

System Manager

- Little/Big Endian support
- Address space: 128M bytes for each bank (total 1G bytes)
- Supports programmable 8/16/32-bit data bus width for each bank
- Fixed bank start address from bank 0 to bank 6
- Programmable bank start address and bank size for bank 7
- Eight memory banks:
  - Six memory banks for ROM, SRAM, and others.
  - Two memory banks for ROM/SRAM Synchronous DRAM/DDR
- Fully Programmable access cycles for all memory banks
- Supports external wait signals to expend the bus cycle
- Supports self-refresh mode in SDRAM for power-down
- Supports various types of ROM for booting (NOR/NAND Flash, EEPROM, and others)

NAND Flash Boot Loader

- Supports booting from NAND flash memory
- 4KB internal buffer for booting
- Supports storage memory for NAND flash memory after booting

Cache Memory

- 4-way set-associative cache with I-Cache (8KB) and D-Cache (8KB)
- 8-words length per line with one valid bit and two dirty bits per line
- Pseudo random or round robin replacement algorithm
- Write-through or write-back cache operation to update the main memory
- The write buffer can hold 16 words of data and four addresses.

Clock & Power Manager

- On-chip MPLL and UPLL:
  UPLL generates the clock to operate USB Host/Device.
  MPLL generates the clock to operate MCU at maximum 266MHz @ 1.4V
- Clock can be fed selectively to each function block by software.
- Power mode: Normal, Idle, Stop, and Sleep mode
  Normal mode: Normal operating mode
  Idle mode: The clock for only CPU is stopped.
  Stop mode: All clocks are stopped.
  Sleep mode: The Core power including all peripherals is shut down.
- Woken up by EINT[15:0] or RTC alarm interrupt from Sleep mode

FEATURES (Continued)

Interrupt Controller

- 55 Interrupt sources (One Watch dog timer, 5 timers, 9 UARTs, 24 external interrupts, 4 DMA, 2 RTC, 2 ADC, 1 IIC, 2 SPI, 1 SDI, 2 USB, 1 LCD, and 1 Battery Fault)
- Level/Edge mode on external interrupt source
- Programmable polarity of edge and level
- Supports Fast Interrupt request (FIQ) for very urgent interrupt request

Timer with Pulse Width Modulation (PWM)

- 4-ch 16-bit Timer with PWM / 1-ch 16-bit internal timer with DMA-based or interrupt-based operation
- Programmable duty cycle, frequency, and polarity
- Dead-zone generation
- Supports external clock sources

RTC (Real Time Clock)

- Full clock feature: second, minute, hour, date, day, month, and year
- 32.768 KHz operation
- Alarm interrupt
- Time tick interrupt

General Purpose Input/Output Ports

- 24 external interrupt ports
- multiplexed input/output ports

UART

- 3-channel UART with DMA-based or interrupt-based operation
- Supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/receive (Tx/Rx)
- Supports external clocks for the UART operation (UEXTCLK)
- Programmable baud rate
- Supports IrDA 1.0
- Loopback mode for testing
- Each channel has internal 64-byte Tx FIFO and 64-byte Rx FIFO.

DMA Controller

- 4-ch DMA controller
- Supports memory to memory, IO to memory, memory to IO, and IO to IO transfers
- Burst transfer mode to enhance the transfer rate

A/D Converter & Touch Screen Interface

- 8-ch multiplexed ADC
- Max. 500KSPS and 10-bit Resolution
- Internal FET for direct Touch screen Interface

LCD Controller STN LCD Displays Feature

- Supports 3 types of STN LCD panels: 4-bit dual scan, 4-bit single scan, 8-bit single scan display type
- Supports monochrome mode, 4 gray levels, 16 gray levels
- Supports up to 65k colors for color STN LCD panel
- Supports multiple screen size
- Typical actual screen size: 640x480, 320x240, 160x160, and others
- Maximum virtual screen size is 4 Mbytes.
- Maximum virtual screen size in 256 color mode: 4096x1024, 2048x2048, 1024x4096, and others

TFT (Thin Film Transistor) Color Displays Feature

- Supports 1, 2, 4 or 8 bpp (bit-per-pixel) palette color displays for color TFT
- Supports 16, 24 bpp non-palette true-color displays for color TFT
- Supports maximum 16M color TFT at 24 bpp mode
- LPC3600 Timing controller embedded for LTS350Q1-PD1/2(SAMSUNG 3.5” Portrait / 256K-color/ Reflective a-Si TFT LCD)
- LCC3600 Timing controller embedded for LTS350Q1-PE1/2(SAMSUNG 3.5” Portrait / 256K-color/ Transflective a-Si TFT LCD)
- Supports multiple screen size
- Typical actual screen size: 640x480, 320x240, 160x160, and others
- Maximum virtual screen size is 4Mbytes.
- Maximum virtual screen size in 64K color mode: 2048 x 1024, and others

Watchdog Timer

- 16-bit Watchdog Timer
- Interrupt request or system reset at time-out

IIC-Bus Interface

- 1-ch Multi-Master IIC-Bus
- Serial, 8-bit oriented and bi-directional data transfers can be made at up to 100 Kbit/s in Standard mode or up to 400 Kbit/s in Fast mode.

IIS-Bus Interface

- 1-ch IIS-bus for audio interface with DMA-based operation
- Serial, 8-/16-bit per channel data transfers
- 128 Bytes (64-Byte + 64-Byte) FIFO for Tx/Rx
- Supports IIS format, MSB-justified and LSB-justified data format
- Full Duplex supported

USB Host

- 2-port USB Host
- Complies with OHCI Rev. 1.0
- Compatible with USB Specification version 1.1

USB Device

- 1-port USB Device
- 5 Endpoints for USB Device
- Compatible with USB Specification version 1.1
- SD Host Interface
- Normal, Interrupt and DMA data transfer mode (byte, halfword, word transfer)
- DMA burst4 access support (only word transfer)
- Compatible with SD Memory Card Protocol version 1.0
- Compatible with SDIO Card Protocol version 1.0
- 64 Bytes FIFO for Tx/Rx
- Compatible with Multimedia Card Protocol version 2.11

SPI Interface

- Compatible with 2-ch Serial Peripheral Interface Protocol version 2.11
- 2 x 16bytes FIFO for Tx/Rx
- DMA-based or interrupt-based operation

Camera Interface

- ITU-R BT 601/656 8-bit mode support
- DZI (Digital Zoom In) capability
- Programmable polarity of video sync signals
- Max. 1600 x 1200 pixels input support with scaling
- Image mirror and rotation (X-axis mirror, Y-axis mirror, and 180° rotation)
- Camera output format (RGB 16/24-bit and YCbCr 4:2:0/4:2:2 format)
- Scan line offset support
- YCbCr 4:2:2 codec image format interleave support

Operating Voltage Range

- ARM : 1.4V
- Internal : 1.25V
- Memory: 1.8V/2.5V/3.3V
- IO: 2.5V/2.8V/3.3V

Operating Frequency

- Up to 266MHz

Package

- 289-FBGA

PIN ASSIGNMENTS

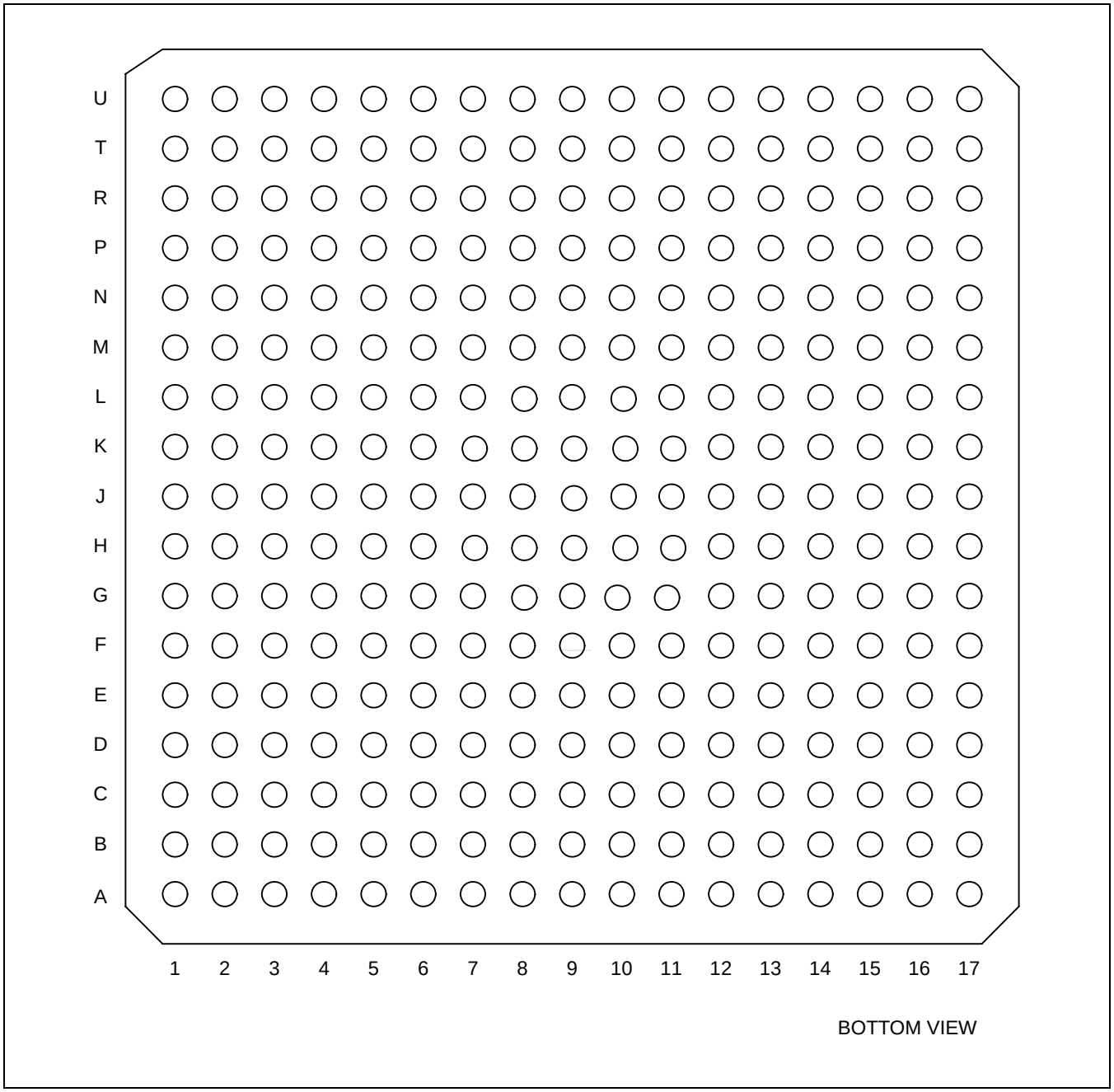


Figure 1-2. S3C2413X Pin Assignments (289-FBGA)

Table 1-1. 289-Pin FBGA Pin Assignments – Pin Number Order

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A1	VSSMOP8	B14	DATA8	D10	ADDR22/GPA7
A2	VSSI6	B15	DATA9	D11	ADDR26/GPA11
A3	NWE	B16	DATA14	D12	DATA5
A4	NBE0/nWBE0/DQM0	B17	VDDMOP2	D13	DATA16
A5	VSSMOP7	C1	CLE/GPA17	D14	DATA12
A6	VDDI7	C2	NGCS5/GPA16	D15	DATA15
A7	VSSMOP6	C3	NGCS3/GPA14	D16	DATA18
A8	ADDR10	C4	NGCS0	D17	VSSI3
A9	VDDMOP5	C5	SCLK	E1	VDDI1
A10	VDDI6	C6	NBE1/nWBE1/DQM1	E2	NFWE/GPA19
A11	VSSMOP5	C7	ADDR0/GPA0	E3	NWAIT
A12	VSSI4	C8	ADDR8	E4	NGCS1/GPA12
A13	DATA2	C9	ADDR14	E5	NSRAS
A14	VDDMOP3	C10	ADDR20/GPA5	E6	ADDR1
A15	VSSMOP3	C11	ADDR25/GPA10	E7	ADDR4
A16	VDDI4	C12	DATA4	E8	ADDR7
A17	DATA11	C13	DATA7	E9	ADDR17/GPA2
B1	VDDMOP7	C14	DATA10	E10	ADDR23/GPA8
B2	NGCS4/GPA15	C15	DATA13	E11	DATA1
B3	SCKE	C16	DATA17	E12	DATA3
B4	NSCLK	C17	VSSMOP2	E13	DATA25
B5	NOE	D1	VSSMOP9	E14	DATA23
B6	VDDMOP6	D2	NGCS6	E15	DATA19
B7	ADDR2	D3	NGCS7	E16	DATA21
B8	ADDR9	D4	NGCS2/GPA13	E17	VSSMOP1
B9	ADDR13	D5	NBE2/nWBE2/DQM2	F1	VSSOP1
B10	VSSI5	D6	NBE3/nWBE3/DQM3	F2	VSSI1
B11	VDDI5	D7	ADDR3	F3	RNB
B12	VDDMOP4	D8	ADDR6	F4	NFRE/GPA20
B13	DATA6	D9	ADDR15	F5	NSCAS

Table 1-1. 289-Pin FBGA Pin Assignments – Pin Number Order (Continued)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
F6	ADDR5	H2	TOUT1/GPB1	J15	TMS
F7	ADDR11	H3	TOUT0/GPB0	J16	RTCK
F8	ADDR19/GPA4	H4	TOUT2/GPB2	J17	VDDALIVE2
F9	ADDR21/GPA6	H5	GPB5	K1	VSSIARM2
F10	ADDR24/GPA9	H6	NXDREQ1/GPB8	K2	NXDACK0/GPB9
F11	DATA0	H7	CAMDATA1/GPJ1	K3	NXDREQ0/GPB10
F12	DATA24	H8	CAMHREF/GPJ10	K4	VCLK/GPC1
F13	DATA20	H9	CAMPCLK/GPJ8	K5	LCDVF0/GPC5
F14	DATA27	H10	SMCLK	K6	SPIMOSI0/GPE12
F15	DATA22	H11	SMAVD	K7	CAMRESET/GPJ12
F16	VDDI3	H12	NRESET	K8	CAMPCLKOUT/GPJ11
F17	VDDMOP1	H13	DATA31	K9	CAMDATA6/GPJ6
G1	VSSIARM1	H14	EXTCLK	K10	CAMDATA5/GPJ5
G2	VDDALIVE1	H15	nTRST	K11	CAMDATA3/GPJ3
G3	SMBSTWAIT	H16	PWREN	K12	TXD2/nRTS1/GPH6
G4	ALE/GPA18	H17	VSSOP5	K13	TXD0/GPH2
G5	ADDR12	J1	VDDIARM1	K14	NCTS0/GPH0
G6	ADDR16/GPA1	J2	TCLK0/GPB4	K15	RXD1/GPH5
G7	ADDR18/GPA3	J3	TOUT3/GPB3	K16	RXD0/GPH3
G8	DQS[1]	J4	GPB6	K17	RXD2/nCTS1/GPH7
G9	VSSMOP4	J5	NXDACK1/GPB7	L1	VDDIARM2
G10	DQS[0]	J6	VLINE/GPC2	L2	VM/GPC4
G11	VSSI2	J7	CLKOUT1/GPH10	L3	VFRAME/GPC3
G12	DATA29	J8	CAMDATA2/GPJ2	L4	VD0/GPC8
G13	DATA26	J9	CAMDATA0/GPJ0	L5	LCDVF2/GPC7
G14	DATA28	J10	CAMVSYNC/GPJ9	L6	SDDAT0/GPE7
G15	DATA30	J11	BATT_FLT	L7	IICSDA/GPE15
G16	XTOPLL	J12	TDI	L8	CAMDATA7/GPJ7
G17	XTIPLL	J13	TDO	L9	EINT14/SPIMOSI1/GPG6
H1	VDDOP1	J14	TCK	L10	CAMDATA4/GPJ4

Table 1-1. 289-Pin FBGA Pin Assignments – Pin Number Order (Continued)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
L11	TXD1/GPH4	N8	IICSCL/GPE14	R5	VD18/GPD10/SPICLK1
L12	EINT7/GPF7	N9	EINT10/nSS0/GPG2	R6	VD21/GPD13
L13	EINT2/GPF2	N10	EINT19/TCLK1/GPG11	R7	CDCLK/GPE2
L14	EINT5/GPF5	N11	EINT23/GPG15	R8	SPIMISO0/GPE11
L15	EINT3/GPF3	N12	DN1/PDN0	R9	EINT9/ATA_NRESET/GPG 1
L16	UCLK/GPH8	N13	NRSTOUT/GPA21	R10	EINT15/SPICLK1/GPG7
L17	NRTS0/GPH1	N14	DP0	R11	EINT22/GPG14
M1	LCDVF1GPC6	N15	MPLLCAP	R12	OM4
M2	VD2/GPC10	N16	XTORTC	R13	OM0
M3	VD3/GPC11	N17	XTIRTC	R14	AIN0
M4	VD1/GPC9	P1	VSSIARM3	R15	AIN3
M5	I2SLRCLK/GPE0	P2	VD8/GPD0	R16	AIN6/TSXM
M6	I2SSDI/nSS0/GPE3	P3	VD9/GPD1	R17	VSSI_UPLL
M7	SDDAT2/GPE9	P4	VD15/GPD7	T1	VDDIARM3
M8	CLKOUT0/GPH9	P5	VD16/GPD8/SPIMISO1	T2	VD11/GPD3
M9	EINT12/GPG4	P6	VD22/nSS1/GPD14	T3	VDDOP2
M10	EINT21/GPG13	P7	SDCMD/GPE6	T4	VD17/GPD9/SPIMOSI1
M11	EINT6/GPF6	P8	SDDAT3/GPE10	T5	VD20/GPD12
M12	EINT4/GPF4	P9	EINT11/NSS1/GPG3	T6	I2SSCLK/GPE1
M13	RTCVDD	P10	EINT13/SPIMISO1/ GPG5	T7	I2SSDO/I2SSDI/ GPE4
M14	UPLLCAP	P11	EINT20/GPG12	T8	SPICLK0/GPE13
M15	EINT0/GPF0	P12	DP1/PDP0	T9	EINT8/ATA_INTRQ/GPG0
M16	EINT1/GPF1	P13	OM1	T10	EINT16/GPG8
M17	VDDOP4	P14	AIN7/TSXP	T11	EINT18/GPG10/nCTS1
N1	VSSOP2	P15	VDDA_ADC	T12	DN0
N2	VD5/GPC13	P16	VDDI_MPLL	T13	OM2
N3	VD7/GPC15	P17	VDDI_UPLL	T14	VSSA_ADC
N4	VD4/GPC12	R1	VD6/GPC14	T15	AIN2
N5	VD19/GPD11	R2	VD10/GPD2	T16	AIN4/TSYM
N6	VD23/NSS0/GPD1 5	R3	VD12/GPD4	T17	VSSI_MPLL
N7	SDCLK//GPE5	R4	VD14/GPD6	U1	VSSIARM4

Table 1-1. 289-Pin FBGA Pin Assignments – Pin Number Order (Continued)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
U2	VD13/GPD5	U8	VSSOP3	U14	VSSOP4
U3	VDDIARM4	U9	VSSIARM6	U15	VREF
U4	VSSIARM5	U10	VDDI2	U16	AIN1
U5	VDDIARM5	U11	EINT17/GPG9/nRTS1	U17	AIN5/TSYP
U6	SDDAT1/GPE8	U12	VDDOP3	-	-
U7	VDDIARM6	U13	OM3	-	-

Table 1-2. S3C2413X 289-Pin FBGA Pin Assignments (Sheet 1 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
C7	ADDR0/GPA0	ADDR0	Hi-z/–	–	O(L)	t12s
E6	ADDR1	ADDR1	Hi-z	–	O(L)	t12s
B7	ADDR2	ADDR2	Hi-z	–	O(L)	t12s
D7	ADDR3	ADDR3	Hi-z	–	O(L)	t12s
E7	ADDR4	ADDR4	Hi-z	–	O(L)	t12s
F6	ADDR5	ADDR5	Hi-z	–	O(L)	t12s
D8	ADDR6	ADDR6	Hi-z	–	O(L)	t12s
E8	ADDR7	ADDR7	Hi-z	–	O(L)	t12s
C8	ADDR8	ADDR8	Hi-z	–	O(L)	t12s
B8	ADDR9	ADDR9	Hi-z	–	O(L)	t12s
A8	ADDR10	ADDR10	Hi-z	–	O(L)	t12s
F7	ADDR11	ADDR11	Hi-z	–	O(L)	t12s
G5	ADDR12	ADDR12	Hi-z	–	O(L)	t12s
B9	ADDR13	ADDR13	Hi-z	–	O(L)	t12s
C9	ADDR14	ADDR14	Hi-z	–	O(L)	t12s
D9	ADDR15	ADDR15	Hi-z	–	O(L)	t12s
G6	ADDR16/GPA1	ADDR16	Hi-z/–	–	O(L)	t12s
E9	ADDR17/GPA2	ADDR17	Hi-z/–	–	O(L)	t12s
G7	ADDR18/GPA3	ADDR18	Hi-z/–	–	O(L)	t12s
F8	ADDR19/GPA4	ADDR19	Hi-z/–	–	O(L)	t12s
C10	ADDR20/GPA5	ADDR20	Hi-z/–	–	O(L)	t12s
F9	ADDR21/GPA6	ADDR21	Hi-z/–	–	O(L)	t12s
D10	ADDR22/GPA7	ADDR22	Hi-z/–	–	O(L)	t12s
E10	ADDR23/GPA8	ADDR23	Hi-z/–	–	O(L)	t12s
F10	ADDR24/GPA9	ADDR24	Hi-z/–	–	O(L)	t12s
C11	ADDR25/GPA10	ADDR25	Hi-z/–	–	O(L)	t12s
D11	ADDR26/GPA11	ADDR26	Hi-z/–	–	O(L)	t12s
R14	AIN0	AIN0	–	–	AI	r10
U16	AIN1	AIN1	–	–	AI	r10
T15	AIN2	AIN2	–	–	AI	r10
R15	AIN3	AIN3	–	–	AI	r10
T16	YM/AIN4	AIN4	–/–	–/–	AI	r10

Table 1-2. S3C2413X 289-Pin FBGA Pin Assignments (Sheet 2 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
U17	YP/AIN5	YP	–/–	–/–	AI	r10
R16	XM/AIN6	AIN6	–/–	–/–	AI	r10
P14	XP/AIN7	XP	–/–	–/–	AI	r10
J9	CAMDATA0/GPJ0	GPJ0	–/–	–	I	t8
H7	CAMDATA1/GPJ1	GPJ1	–/–	–	I	t8
J8	CAMDATA2/GPJ2	GPJ2	–/–	–	I	t8
K11	CAMDATA3/GPJ3	GPJ3	–/–	–	I	t8
L10	CAMDATA4/GPJ4	GPJ4	–/–	–	I	t8
K10	CAMDATA5/GPJ5	GPJ5	–/–	–	I	t8
K9	CAMDATA6/GPJ6	GPJ6	–/–	–	I	t8
L8	CAMDATA7/GPJ7	GPJ7	–/–	–	I	t8
H9	CAMPCLK/GPJ8	GPJ8	–/–	–	I	t8
J10	CAMVSYNC/GPJ9	GPJ9	–/–	–	I	t8
H8	CAMHREF/GPJ10	GPJ10	–/–	–	I	t8
K8	CAMCLKOUT/GPJ11	GPJ11	–/–	–	I	t8
K7	CAMRESET/GPJ12	GPJ12	–/–	–	I	t8
F11	DATA0	DATA0	Hi-z	–	I	b12s
E11	DATA1	DATA1	Hi-z	–	I	b12s
A13	DATA2	DATA2	Hi-z	–	I	b12s
E12	DATA3	DATA3	Hi-z	–	I	b12s
C12	DATA4	DATA4	Hi-z	–	I	b12s
D12	DATA5	DATA5	Hi-z	–	I	b12s
B13	DATA6	DATA6	Hi-z	–	I	b12s
C13	DATA7	DATA7	Hi-z	–	I	b12s
B14	DATA8	DATA8	Hi-z	–	I	b12s
B15	DATA9	DATA9	Hi-z	–	I	b12s
C14	DATA10	DATA10	Hi-z	–	I	b12s
A17	DATA11	DATA11	Hi-z	–	I	b12s
D14	DATA12	DATA12	Hi-z	–	I	b12s
C15	DATA13	DATA13	Hi-z	–	I	b12s
B16	DATA14	DATA14	Hi-z	–	I	b12s
D15	DATA15	DATA15	Hi-z	–	I	b12s

Table 1-2. S3C2413X 289-Pin FBGA Pin Assignments (Sheet 3 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
D13	DATA16	DATA16	Hi-z	–	I	b12s
C16	DATA17	DATA17	Hi-z	–	I	b12s
D16	DATA18	DATA18	Hi-z	–	I	b12s
E15	DATA19	DATA19	Hi-z	–	I	b12s
F13	DATA20	DATA20	Hi-z	–	I	b12s
E16	DATA21	DATA21	Hi-z	–	I	b12s
F15	DATA22	DATA22	Hi-z	–	I	b12s
E14	DATA23	DATA23	Hi-z	–	I	b12s
F12	DATA24	DATA24	Hi-z	–	I	b12s
E13	DATA25	DATA25	Hi-z	–	I	b12s
G13	DATA26	DATA26	Hi-z	–	I	b12s
F14	DATA27	DATA27	Hi-z	–	I	b12s
G14	DATA28	DATA28	Hi-z	–	I	b12s
G12	DATA29	DATA29	Hi-z	–	I	b12s
G15	DATA30	DATA30	Hi-z	–	I	b12s
H13	DATA31	DATA31	Hi-z	–	I	b12s
T12	DN0	DN0	–	–	AI	us
N14	DP0	DP0	–	–	AI	us
N12	DN1/PDN0	DN1	–/–	–	AI	us
P12	DP1/PDP0	DP1	–/–	–	AI	us
M15	EINT0/GPF0	GPF0	–/–	Hi-z/–	I	t8
M16	EINT1/GPF1	GPF1	–/–	Hi-z/–	I	t8
L13	EINT2/GPF2	GPF2	–/–	Hi-z/–	I	t8
L15	EINT3/GPF3	GPF3	–/–	Hi-z/–	I	t8
M12	EINT4/GPF4	GPF4	–/–	Hi-z/–	I	t8
L14	EINT5/GPF5	GPF5	–/–	Hi-z/–	I	t8
M11	EINT6/GPF6	GPF6	–/–	Hi-z/–	I	t8
L12	EINT7/GPF7	GPF7	–/–	Hi-z/–	I	t8
T9	EINT8/ATA_INTRQ/GPG0	GPG0	–/–/–	–	I	t8
R9	EINT9/ATA_nRESET/GPG1	GPG1	–/–/–	–	I	t8
N9	EINT10/nSS0/GPG2	GPG2	–/–/–	–	I	t8
P9	EINT11/nSS1/GPG3	GPG3	–/–/–	–	I	t8

Table 1-2. S3C2413X 289-Pin FBGA Pin Assignments (Sheet 4 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
M9	EINT12/GPG4	GPG4	–/–	–	I	t8
P10	EINT13/SPIMISO1/GPG5	GPG5	–/–/–	–	I	t8
L9	EINT14/SPIMOSI1/GPG6	GPG6	–/–/–	–	I	t8
R10	EINT15/SPICLK1/GPG7	GPG7	–/–/–	–	I	t8
T10	EINT16/GPG8	GPG8	–/–	–	I	t8
U11	EINT17/nRTS1/GPG9	GPG9	–/–/–	–	I	t8
T11	EINT18/nCTS1/GPG10	GPG10	–/–/–	–	I	t8
N10	EINT19/TCLK1/GPG11	GPG11	–/–/–	–	I	t12
P11	EINT20/GPG12	GPG12	–/–	–	I	t12
M10	EINT21/GPG13	GPG13	–/–	–	I	t12
R11	EINT22/GPG14	GPG14	–/–	–	I	t12
N11	EINT23/GPG15	GPG15	–/–	–	I	t12
H14	EXTCLK	EXTCLK	–	–	AI	is
H12	nRESET	nRESET	–	–	I	is
M14	UPLLCAP	UPLLCAP	–	–	AI	r50
N15	MPLLCAP	MPLLCAP	–	–	AI	r50
J11	nBATT_FLT	nBATT_FLT	–	–	I	is
A4	nBE0/nWBE0/DQM0	nBE0	Hi-z	–	O(H)	t12s
C6	nBE1/nWBE1/DQM1	nBE1	Hi-z	–	O(H)	t12s
D5	nBE2/nWBE2/DQM2	nBE2	Hi-z	–	O(H)	t12s
D6	nBE3/nWBE3/DQM3	nBE3	Hi-z	–	O(H)	t12s
F3	FRnB	FRnB	–	Hi-z,O(L)	I	d2s
E3	nWAIT	nWAIT	–	Hi-z,O(L)	I	d2s
G3	SMBSTWAIT	SMBSTWAIT	–	Hi-z,O(L)	I	d2s
B5	nOE	nOE	Hi-z	–	O(H)	t12s
A3	nWE	nWE	Hi-z	–	O(H)	t12s
C1	CLE/GPA17	GPA17	O(L)/–	–	O(L)	t12s
G4	ALE/GPA18	GPA18	O(L)/–	–	O(L)	t12s
E2	nFWE/GPA19	GPA19	O(H)/–	–	O(H)	t12s
F4	nFRE/GPA20	GPA20	O(H)/–	–	O(H)	t12s
N13	nRSTOUT/GPA21	GPA21	–/–	–	O(L)	b8
C4	nGCS0	nGCS0	Hi-z	–	O(H)	t12s

Table 1-2. S3C2413X 289-Pin FBGA Pin Assignments (Sheet 5 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
E4	nGCS1/GPA12	GPA12	Hi-z/–	–	O(H)	t12s
D4	nGCS2/GPA13	GPA13	Hi-z/–	–	O(H)	t12s
C3	nGCS3/GPA14	GPA14	Hi-z/–	–	O(H)	t12s
B2	nGCS4/GPA15	GPA15	Hi-z/–	–	O(H)	t12s
C2	nGCS5/GPA16	GPA16	Hi-z/–	–	O(H)	t12s
D2	nGCS6	nGCS6	Hi-z	–	O(H)	t12s
D3	nGCS7	nGCS7	Hi-z	–	O(H)	t12s
F5	nSCAS	nSCAS	Hi-z	–	O(H)	t12s
E5	nSRAS	nSRAS	Hi-z	–	O(H)	t12s
B4	nSCLK	nSCLK	Hi-z	–	O(H)	t12s
B3	SCKE	SCKE	Hi-z	–	O(H)	t12s
C5	SCLK	SCLK	Hi-z	–		b12s
H10	SMCLK	SMCLK	Hi-z	–		b12s
H11	SMAVD/GPA22			–		t12s
G10	DQS0			–		b12s
G8	DQS1			–		b12s
H15	nTRST	nTRST	I	–	I	is
H3	TOUT0/GPB0	GPB0	–/–	–	I	t8
H2	TOUT1/GPB1	GPB1	–/–	–	I	t8
H4	TOUT2/GPB2	GPB2	–/–	–	I	t8
J3	TOUT3/GPB3	GPB3	–/–	–	I	t8
J2	TCLK0/GPB4	GPB4	–/–	–	I	t8
H5	GPB5	GPB5	–/–	–	I	t8
J4	GPB6	GPB6	–/–	–	I	t8
J5	nXDACK1/GPB7	GPB7	–/–	–	I	t8
H6	nXDREQ1/GPB8	GPB8	–/–	–	I	t8
K2	nXDACK0/GPB9	GPB9	–/–	–	I	t8
K3	nXDREQ0/GPB10	GPB10	–/–	–	I	t8
R13	OM0	OM0	–	–	I	is
P13	OM1	OM1	–	–	I	is
T13	OM2	OM2	–	–	I	is
U13	OM3	OM3	–	–	I	is

Table 1-2. S3C2413X 289-Pin FBGA Pin Assignments (Sheet 6 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
R12	OM4	OM4	–	–	I	is
H16	PWREN	PWREN	O(H)	O(L)	O(H)	b8
K14	nCTS0/GPH0	GPH0	–/–	–	I	t8
L17	nRTS0/GPH1	GPH1	–/–	–	I	t8
K13	TXD0/GPH2	GPH2	–/–	–	I	t8
K16	RXD0/GPH3	GPH3	–/–	–	I	t8
L11	TXD1/GPH4	GPH4	–/–	–	I	t8
K15	RXD1/GPH5	GPH5	–/–	–	I	t8
K12	TXD2/nRTS1/GPH6	GPH6	–/–/–	–	I	t8
K17	RXD2/nCTS1/GPH7	GPH7	–/–/–	–	I	t8
L16	UCLK/GPH8	GPH8	–/–	–	I	t8
M8	CLKOUT0/GPH9	GPH9	–/–	–	I	t12
J7	CLKOUT1/GPH10	GPH10	–/–	–	I	t12
M5	I2SLRCLK/GPE0	GPE0	–/–	–	I	t8
T6	I2SSCLK/GPE1	GPE1	–/–	–	I	t8
R7	CDCLK/GPE2	GPE2	–/–	–	I	t8
M6	I2SSDI/nSS0/GPE3	GPE3	–/–/–	–	I	t8
T7	I2SSDO/I2SSDI/GPE4	GPE4	–/–/–	–	I	t8
N7	SDCLK/GPE5	GPE5	–/–	–	I	t8
P7	SDCMD/GPE6	GPE6	–/–	–	I	t8
L6	SDDAT0/GPE7	GPE7	–/–	–	I	t8
U6	SDDAT1/GPE8	GPE8	–/–	–	I	t8
M7	SDDAT2/GPE9	GPE9	–/–	–	I	t8
P8	SDDAT3/GPE10	GPE10	–/–	–	I	t8
R8	SPIMISO0/GPE11	GPE11	–/–	–	I	t8
K6	SPIMOSI0/GPE12	GPE12	–/–	–	I	t8
T8	SPICLK0/GPE13	GPE13	–/–	–	I	t8
N8	IICSCL/GPE14	GPE14	–/–	–	I	d8
L7	IICSDA/GPE15	GPE15	–/–	–	I	d8
J14	TCK	TCK	I	–	I	is
J12	TDI	TDI	I	–	I	is
J13	TDO	TDO	O	O	O	ot

Table 1-2. S3C2413X 289-Pin FBGA Pin Assignments (Sheet 7 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
J15	TMS	TMS	I	–	I	is
J16	RTCK	RTCK	O	O	O	o12s
K4	VCLK/GPC1	GPC1	–/–	–	I	t8
J6	VLINE/GPC2	GPC2	–/–	–	I	t8
L3	VFRAME/GPC3	GPC3	–/–	–	I	t8
L2	VM/GPC4	GPC4	–/–	–	I	t8
c	LCDVF0/GPC5	GPC5	–/–	–	I	t8
M1	LCDVF1/GPC6	GPC6	–/–	–	I	t8
L5	LCDVF2/GPC7	GPC7	–/–	–	I	t8
L4	VD0/GPC8	GPC8	–/–	–	I	t8
M4	VD1/GPC9	GPC9	–/–	–	I	t8
M2	VD2/GPC10	GPC10	–/–	–	I	t8
M3	VD3/GPC11	GPC11	–/–	–	I	t8
N4	VD4/GPC12	GPC12	–/–	–	I	t8
N2	VD5/GPC13	GPC13	–/–	–	I	t8
R1	VD6/GPC14	GPC14	–/–	–	I	t8
N3	VD7/GPC15	GPC15	–/–	–	I	t8
P2	VD8/GPD0	GPD0	–/–	–	I	t8
P3	VD9/GPD1	GPD1	–/–	–	I	t8
R2	VD10/GPD2	GPD2	–/–	–	I	t8
T2	VD11/GPD3	GPD3	–/–	–	I	t8
R3	VD12/GPD4	GPD4	–/–	–	I	t8
U2	VD13/ GPD5	GPD5	–/–/–	–	I	t8
R4	VD14/GPD6	GPD6	–/–/–	–	I	t8
P4	VD15/GPD7	GPD7	–/–/–	–	I	t8
P5	VD16/SPIMISO1/GPD8	GPD8	–/–/–	–	I	t8
T4	VD17/SPIMOSI1/GPD9	GPD9	–/–/–	–	I	t8
R5	VD18/SPICLK1/GPD10	GPD10	–/–/–	–	I	t8
N5	VD19/GPD11	GPD11	–/–/–	–	I	t8
T5	VD20/ GPD12	GPD12	–/–/–	–	I	t8
R6	VD21/ GPD13	GPD13	–/–/–	–	I	t8
P6	VD22/nSS1/GPD14	GPD14	–/–/–	–	I	t8

Table 1-2. S3C2413X 289-Pin FBGA Pin Assignments (Sheet 8 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
N6	VD23/nSS0/GPD15	GPD15	–/–/–	–	I	t8
U15	Vref	Vref	–	–	AI	ia
G17	XTIpll	XTIpll	–	–	AI	m26
N17	Xtirtc	Xtirtc	–	–	AI	mrtc
G16	XTOpll	XTOpll	–	–	AO	M26
N16	Xtortc	Xtortc	–	–	AO	mrtc
M13	RTCVDD	VDD_RTC	P	P	P	drtc
P15	VDDA_ADC	VDDA_ADC	P	P	P	d33th
P16	VDDI_MPLL	VDDA_MPLL	P	P	P	d12t
P17	VDDI_UPLL	VDDA_UPLL	P	P	P	d12t
G2	VDDalive	VDDalive	P	P	P	d12i
J17	VDDalive	VDDalive	P	P	P	d12i
E1	VDDi	VDDi	P	P	P	d12c
U10	VDDi	VDDi	P	P	P	d12c
F16	VDDi	VDDi	P	P	P	d12c
A16	VDDi	VDDi	P	P	P	d12c
B11	VDDi	VDDi	P	P	P	d12c
A10	VDDi	VDDi	P	P	P	d12c
A6	VDDi	VDDi	P	P	P	d12c
J1	VDDiarm	VDDiarm	P	P	P	d12c
L1	VDDiarm	VDDiarm	P	P	P	d12c
T1	VDDiarm	VDDiarm	P	P	P	d12c
U3	VDDiarm	VDDiarm	P	P	P	d12c
U5	VDDiarm	VDDiarm	P	P	P	d12c
U7	VDDiarm	VDDiarm	P	P	P	d12c
F17	VDDMOP	VDDMOP	P	P	P	d18o
B17	VDDMOP	VDDMOP	P	P	P	d18o
A14	VDDMOP	VDDMOP	P	P	P	d18o
B12	VDDMOP	VDDMOP	P	P	P	d18o
A9	VDDMOP	VDDMOP	P	P	P	d18o
B6	VDDMOP	VDDMOP	P	P	P	d18o
B1	VDDMOP	VDDMOP	P	P	P	d18o

Table 1-2. S3C2413X 289-Pin FBGA Pin Assignments (Sheet 9 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
H1	VDDOP	VDDOP	P	P	P	d33o
T3	VDDOP	VDDOP	P	P	P	d33o
U12	VDDOP	VDDOP	P	P	P	d33o
M17	VDDOP	VDDOP	P	P	P	d33o
T14	VSSA_ADC	VSSA_ADC	P	P	P	sth
T17	VSSI_MPLL	VSSA_MPLL	P	P	P	st
R17	VSSI_UPLL	VSSA_UPLL	P	P	P	st
F2	VSSi	VSSi	P	P	P	si
G11	VSSi	VSSi	P	P	P	si
D17	VSSi	VSSi	P	P	P	si
A12	VSSi	VSSi	P	P	P	si
B10	VSSi	VSSi	P	P	P	si
A2	VSSi	VSSi	P	P	P	si
G1	VSSiarm	VDDiarm	P	P	P	si
K1	VSSiarm	VDDiarm	P	P	P	si
P1	VSSiarm	VDDiarm	P	P	P	si
U1	VSSiarm	VDDiarm	P	P	P	si
U4	VSSiarm	VDDiarm	P	P	P	si
U9	VSSiarm	VDDiarm	P	P	P	si
E17	VSSMOP	VSSMOP	P	P	P	s18
C17	VSSMOP	VSSMOP	P	P	P	s18
A15	VSSMOP	VSSMOP	P	P	P	s18
G9	VSSMOP	VSSMOP	P	P	P	s18
A11	VSSMOP	VSSMOP	P	P	P	s18
A7	VSSMOP	VSSMOP	P	P	P	s18
A5	VSSMOP	VSSMOP	P	P	P	s18
A1	VSSMOP	VSSMOP	P	P	P	s18
D1	VSSMOP	VSSMOP	P	P	P	s18
F1	VSSOP	VSSOP	P	P	P	so
N1	VSSOP	VSSOP	P	P	P	so
U8	VSSOP	VSSOP	P	P	P	so
U14	VSSOP	VSSOP	P	P	P	so
H17	VSSOP	VSSOP	P	P	P	so

THE TABLE BELOW SHOWS I/O TYPES AND DESCRIPTIONS.

Input (I)/Output (O) Type	Descriptions
d12i(vdd12ih_45p)	1.2V Vdd for alive power
d12c(vdd12ih_core_45p), si(vssiph_45p)	1.2V Vdd/Vss for internal logic
d18o(vdd18op_ddr), s18(vsso_ddr)	1.8V Vdd/Vss for external logic
d33o(vdd33oph), so(vssoh)	3.3V Vdd/Vss for external logic
d33th(vdd33th_abb, vddi33ih_abb), sth(vssbbh_abb, vssih_abb)	3.3V Vdd/Vss for analog circuitry
d12t(vdd12t_abb), st(vssbb_abb)	1.2V Vdd/Vss for analog circuitry
drtc(vdd30th_rtc)	3.0V Vdd for RTC power
t8(phbsd100ct8sm)	Bi-directional pad, LVCMOS schmitt-trigger,100Kohm pull-down resistor with control, tri-state, Io=8mA
t12 (phbsd100ct12sm)	Bi-directional pad,LVCMOS schmitt-trigger,100Kohm pull-down resistor with control, tri-state, Io=12mA
is(phis)	Input pad, LVCMOS schmitt-trigger level
us(pbusb0)	USB pad
ot(phot8)	Output pad, tri-state, Io=8mA
b8(phob8)	Output pad, Io=8mA
o12s(phob12sm)	Output pad with medium slew-rate, Io=12mA
r10(phiar10_abb)	Analog input pad with 10-ohm resistor
ia(phia_abb)	Analog input pad
m26(phsoscm26)	Oscillator cell with enable and feedback resistor
mrtc(rtc_osc)	RTC oscillator cell
d8(phbsd8sm)	Bi-directional pad, LVCMOS schmitt-trigger, Open Drain, Io=8mA
b12s(phnbsud100ct12cd_ddr)	Bi-directional pad, LVCMOS schmitt-trigger, 100Kohm pull-up resistor with control, tri -state,output drive strenth control, Io=6,8,10,12mA
d2s(phbsd2)	Bi-directional pad, LVCMOS schmitt-trigger, open-drain, output drive strenth ignore,
r50(poar50_pll_abb)	Analog Output pad, 50Kohm resistor, Separated bulk-bias
t12s(phnot12cd_ddr)	output pad, LVCMOS , tri -state, output drive strenth control, Io=6,8,10,12mA
nc(phnc)	No connection pad

SIGNAL DESCRIPTIONS

Table 1-3. S3C2413X Signal Descriptions

Signal	I/O	Power	Descriptions
System Controller			
OM [0:4]	I	VDDOP3	OM [0:4] sets operation mode of S3C2413X . OM[4] sets clock source 0 : oscillator clock, 1 : EXTCLK OM[0:2] sets boot mode 0xx : Nand-boot 100:NOR-boot 101: OneNAND-boot 11x:Test mode
nRESET	ST	VDDOP4	nRESET suspends any operation in progress and places S3C2413X into a known reset state. For a reset, nRESET must be held to L level for at least 5 cycle(source clock) after the processor power has been stabilized.
nRSTOUT	O	VDDOP3	For external device reset control (nRSTOUT = nRESET & nWDTRST & SW_RESET)
PWREN	O	VDDOP4	1.2V core power on-off control signal
nBATT_FLT	I	VDDOP4	Probe for battery state (Does not wake up at Sleep mode in case of low battery state). If it isn't used, it has to be High (3.3V).
EXTCLK	I	VDDOP4	External clock source. When OM [4] = 1'b1, EXTCLK is used for MPLL CLK source. If it isn't used, it has to be High (3.3V).
XTIpll	AI	VDDOP4	Crystal Input for internal osc circuit. When OM [4] = 1'b0, XTIpll is used for MPLL CLK source. If it isn't used, XTIpll has to be High (3.3V).
XTOpll	AO	VDDOP4	Crystal Output for internal osc circuit. When OM [4] = 1'b0, XTIpll is used for MPLL CLK source. If it isn't used, it has to be a floating pin.
MPLLCAP	AI	VDDI_MPLL	Loop filter capacitor for MPLL.
UPLLCAP	AI	VDDI_UPLL	Loop filter capacitor for UPLL.
XTIrtc	AI	RTCVDD	32.768 kHz crystal input for RTC. If it isn't used, it has to be in High (RTCVDD = 3.3V).
XTOrtc	AO	RTCVDD	32.768 kHz crystal output for RTC. If it isn't used, it has to be Float.
CLKOUT [1:0]	O	VDDOP3	Clock output signal. The CLKSEL of MISCCR register configures the clock output mode among the Source Clock, MPLL CLK, UPLL CLK, ARMCLK, RTCCLK, HCLK and PCLK.

Table 1-3. S3C2413X Signal Descriptions (Continued)

Signal	I/O	Power	Descriptions
Memory Interface			
ADDR [26:0]	O	VDDMOP	ADDR [26:0] (Address Bus) outputs the memory address of the corresponding bank.
DATA [31:0]	IO	VDDMOP	DATA [31:0] (Data Bus) inputs data during memory read and outputs data during memory write. The bus width is programmable among 8/16/32-bit.
nGCS [7:0]	O	VDDMOP	nGCS [7:0] (General Chip Select) are activated when the address of a memory is within the address region of each bank. The number of access cycles and the bank size can be programmed.
nWE	O	VDDMOP	nWE (Write Enable) indicates that the current bus cycle is a write cycle.
nOE	O	VDDMOP	nOE (Output Enable) indicates that the current bus cycle is a read cycle.
nWAIT	I	VDDMOP	nWAIT requests to prolong a current bus cycle. As long as nWAIT is L, the current bus cycle cannot be completed. If nWAIT signal isn't used in your system, nWAIT signal must be tied on pull-up resistor.
SDRAM/mSDRAM/SRAM/DDR/mDDR			
nSRAS	O	VDDMOP	SDRAM Row Address Strobe
nSCAS	O	VDDMOP	SDRAM Column Address Strobe
DQM [3:0]	O	VDDMOP	SDRAM Data Mask
NGCS[7:6]	O	VDDMOP	SDRAM chip select
nBE [3:0]	O	VDDMOP	Upper Byte/Lower Byte Enable (In case of 16-bit SRAM)
nWBE [3:0]	O	VDDMOP	Write Byte Enable
SCLK	I/O	VDDMOP	SDRAM Clock
nSCLK	O	VDDMOP	SDRAM Conversion Clock
SCKE	O	VDDMOP	SDRAM Clock Enable
DQS[1:0]	I/O	VDDMOP	DDR data strobe
NAND Flash			
CLE	O	VDDMOP	Command Latch Enable
ALE	O	VDDMOP	Address Latch Enable
nFRE	O	VDDMOP	NAND Flash Read Enable
nFWE	O	VDDMOP	NAND Flash Write Enable
R/nB	I	VDDMOP	NAND Flash Ready/Busy. If NAND Flash Controller isn't used, it has to be tied on pull-up resistor.
SSMC/OneNAND			
SMCLK	I/O	VDDMOP	SSMC Clock
nBE[3:0]	O	VDDMOP	SSMC Byte line enable
SMAVD	O	VDDMOP	SSMC Address Valid
SMBSTWAIT	O	VDDMOP	SSMC Burst wait

Table 1-3. S3C2413X Signal Descriptions (Continued)

Signal	I/O	POWER	Descriptions
ATA			
ATA_INTRQ	I	VDDOP3	ATA interrupt request
ATA_NRESET	O	VDDOP3	ATA nRESET
LCD Control Unit			
VD [23:0]	O	VDDOP2	**STN/TFT/SEC TFT:** LCD Data Bus
VCLK	O	VDDOP2	**STN/TFT:** LCD clock signal
VFRAME	O	VDDOP2	**STN:** LCD Frame signal
VLINE	O	VDDOP2	**STN:** LCD line signal
VM	O	VDDOP2	**STN:** VM alternates the polarity of the row and column voltage
VSYNC	O	VDDOP2	**TFT:** Vertical synchronous signal
HSYNC	O	VDDOP2	**TFT:** Horizontal synchronous signal
VDEN	O	VDDOP2	**TFT:** Data enable signal
STV	O	VDDOP2	**SEC TFT:** SEC (Samsung Electronics Company) TFT LCD panel control signal
CPV	O	VDDOP2	**SEC TFT:** SEC (Samsung Electronics Company) TFT LCD panel control signal
LCD_HCLK	O	VDDOP2	**SEC TFT:** SEC (Samsung Electronics Company) TFT LCD panel control signal
TP	O	VDDOP2	**SEC TFT:** SEC (Samsung Electronics Company) TFT LCD panel control signal
STH	O	VDDOP2	**SEC TFT:** SEC (Samsung Electronics Company) TFT LCD panel control signal
LCDVF [2:0]	O	VDDOP2	**SEC TFT:** Timing control signal for specific TFT LCD (OE/REV/REVB)
Interrupt Control Unit			
EINT [7:0]	I	VDDOP4	External Interrupt request
EINT [23:8]	I	VDDOP3	External Interrupt request
EXTERNAL Interface			
nXDREQ [1:0]	I	VDDOP1	External DMA request
nXDACK [1:0]	O	VDDOP1	External DMA acknowledge
CAMERA Interface			
CAMPCLK	I	VDDOP1	Camera interface Pixel Clock
CAMVSYNC	I	VDDOP1	Camera interface Frame Sync.
CAMHREF	I	VDDOP1	Camera interface Horizontal Sync.
CAMDATA[7:0]	I	VDDOP1	Camera interface Data
CAMPCLKOUT	O	VDDOP1	Camera interface Master Clock
CAMRESET	O	VDDOP1	Camera interface reset

Table 1-3. S3C2413X Signal Descriptions (Continued)

Signal	I/O	POWER	Descriptions
UART			
RxD [2:0]	I	VDDOP4	UART receives data input
TxD [2:0]	O	VDDOP4	UART transmits data output
nCTS [1:0]	I	VDDOP4	UART clear to send input signal
nRTS [1:0]	O	VDDOP4	UART request to send output signal
UCLK	I	VDDOP4	UART clock signal
ADC			
AIN [7:0]	AI	VDDA_ADC	ADC input [7:0]. If it isn't used pin, it has to be in Ground.
Vref	AI	VDDA_ADC	ADC Vref
IIC-Bus			
IICSDA	IO	VDDOP3	IIC-bus data
IICSCL	IO	VDDOP3	IIC-bus clock
IIS-Bus			
I2SLRCLK	IO	VDDOP3	IIS-bus channel select clock
I2SSDO	O	VDDOP3	IIS-bus serial data output
I2SSDI	I	VDDOP3	IIS-bus serial data input
I2SSCLK	IO	VDDOP3	IIS-bus serial clock
CDCLK	O	VDDOP3	CODEC system clock
USB Host			
DN [1:0]	IO	VDDOP3	DATA (–) from USB host. (15Kohm pull-down)
DP [1:0]	IO	VDDOP3	DATA (+) from USB host. (15Kohm pull-down)
USB Device			
PDN0	IO	VDDOP3	DATA (–) for USB peripheral. (470Kohm pull-down)
PDP0	IO	VDDOP3	DATA (+) for USB peripheral. (1.5Kohm pull-up)
SPI			
SPIMISO [1:0]	IO	VDDOP3 VDDOP2	SPIMISO is the master data input line, when SPI is configured as a master. When SPI is configured as a slave, these pins reverse its role.
SPIMOSI [1:0]	IO	VDDOP3 VDDOP2	SPIMOSI is the master data output line, when SPI is configured as a master. When SPI is configured as a slave, these pins reverse its role.
SPICLK [1:0]	IO	VDDOP3 VDDOP2	SPI clock
nSS [1:0]	I	VDDOP3 VDDOP2	SPI chip select (only for slave mode)

Table 1-3. S3C2413X Signal Descriptions (Continued)

Signal	I/O	POWER	Descriptions
SD			
SDDAT [3:0]	IO	VDDOP3	SD receive/transmit data
SDCMD	IO	VDDOP3	SD receive response/ transmit command
SDCLK	O	VDDOP3	SD clock
TIMMER/PWM			
TOUT [3:0]	O	VDDOP1	Timer Output [3:0]
TCLK [0]	I	VDDOP1	External timer clock input
TCLK [1]	I	VDDOP3	External timer clock input
General Port			
GPA [20:0]	IO	VDDMOP	General input/output ports (some ports are output only)
GPA [21]	IO	VDDOP3	General input/output ports (some ports are output only)
GPA [22]	IO	VDDMOP	General input/output ports (some ports are output only)
GPB [10:0]	IO	VDDOP1	General input/output ports (some ports are output only)
GPC [15:1]	IO	VDDOP2	General input/output ports (some ports are output only)
GPD [15:0]	IO	VDDOP2	General input/output ports (some ports are output only)
GPE [15:0]	IO	VDDOP3	General input/output ports (some ports are output only)
GPF [7:0]	IO	VDDOP4	General input/output ports (some ports are output only)
GPG [15:0]	IO	VDDOP3	General input/output ports (some ports are output only)
GPH [8:0]	IO	VDDOP4	General input/output ports (some ports are output only)
GPH [10:9]	IO	VDDOP3	General input/output ports (some ports are output only)
GPJ [12:0]	IO	VDDOP1	General input/output ports (some ports are output only)
JTAG TEST LOGIC			
NTRST	I	VDDOP4	nTRST (TAP Controller Reset) resets the TAP controller at start. If debugger is used, A 10K pull-up resistor has to be connected. If debugger (black ICE) is not used, nTRST pin must be issued by a low active pulse (Typically connected to nRESET).
TMS	I	VDDOP4	TMS (TAP Controller Mode Select) controls the sequence of the TAP controller's states. A 10K pull-up resistor has to be connected to TMS pin.
TCK	I	VDDOP4	TCK (TAP Controller Clock) provides the clock input for the JTAG logic. A 10K pull-up resistor must be connected to TCK pin.
TDI	I	VDDOP4	TDI (TAP Controller Data Input) is the serial input for test instructions and data. A 10K pull-up resistor must be connected to TDI pin.
TDO	O	VDDOP4	TDO (TAP Controller Data Output) is the serial output for test instructions and data.
RTCK	O	VDDOP4	TAP Controller Returned Clock

Table 1-3. S3C2413X Signal Descriptions (Continued)

Signal	I/O	Descriptions
Power		
VDDALIVE	P	S3C2413X reset block and port status register VDD (1.25V). It should be always supplied whether in normal mode or in sleep mode.
VDDI/VDDIARM	P	S3C2413X core logic VDD (1.4V) for CPU.
VSSI/VSSIARM	P	S3C2413X core logic VSS
VDDI_MPLL	P	S3C2413X MPLL analog and digital VDD (1.25V).
VSSI_MPLL	P	S3C2413X MPLL analog and digital VSS.
VDDI_UPLL	P	S3C2413X UPLL analog and digital VDD (1.25V)
VSSI_UPLL	P	S3C2413X UPLL analog and digital VSS
VDDOP1,2	P	S3C2413X I/O port VDD (2.5/2.8/3.3V)
VDDOP3,4	P	S3C2413X I/O port VDD (3.3V)
VSSOP	P	S3C2413X I/O port VSS
VDDMOP	P	S3C2413X Memory I/O VDD 1.8V / 2.5V / 3.0V: SCLK up to 133MHz
VSSMOP	P	S3C2413X Memory I/O VSS
RTCVDD	P	RTC VDD (3.3V) (This pin must be connected to power properly if RTC isn't used)
VDDA_ADC	P	S3C2413X ADC VDD (3.3V)
VSSA_ADC	P	S3C2413X ADC VSS

NOTES:
1. I/O means input/output.
2. AI/AO means analog input/analog output.
3. ST means schmitt-trigger.
4. P means power.

S3C2413X SPECIAL REGISTERS

Table 1-4. S3C2413X Special Registers (Sheet 1 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
Memory Controller					
BANKCFG	0x48000000	←	W	R/W	DRAM/SDRAM configuration
BANKCON1	0x48000004				BANK1 Control
BANKCON2	0x48000008				BANK2 Control
BANKCON3	0x4800000C				BANK3 Control
REFRESH	0x48000010				DRAM/SDRAM Refresh Control
TIMEOUT	0x48000014				Write buffer time out control
EBI					
EBIPR	0x48800000	←	W	R/W	Bus priority decision
BANK_CFG	0x48800004				Bank configuration

Table 1-4. S3C2413X Special Registers (Sheet 2 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
USB Host Controller					
HcRevision	0x49000000	←	W		Control and Status Group
HcControl	0x49000004				
HcCommonStatus	0x49000008				
HcInterruptStatus	0x4900000C				
HcInterruptEnable	0x49000010				
HcInterruptDisable	0x49000014				
HcHCCA	0x49000018				Memory Pointer Group
HcPeriodCuttentED	0x4900001C				
HcControlHeadED	0x49000020				
HcControlCurrentED	0x49000024				
HcBulkHeadED	0x49000028				
HcBulkCurrentED	0x4900002C				
HcDoneHead	0x49000030				
HcRmInterval	0x49000034				Frame Counter Group
HcFmRemaining	0x49000038				
HcFmNumber	0x4900003C				
HcPeriodicStart	0x49000040				
HcLSThreshold	0x49000044				
HcRhDescriptorA	0x49000048				Root Hub Group
HcRhDescriptorB	0x4900004C				
HcRhStatus	0x49000050				
HcRhPortStatus1	0x49000054				
HcRhPortStatus2	0x49000058				
Interrupt Controller					
SRCPND	0X4A000000	←	W	R/W	Interrupt Request Status
INTMOD	0X4A000004			W	Interrupt Mode Control
INTMSK	0X4A000008			R/W	Interrupt Mask Control
PRIORITY	0X4A00000C			W	IRQ Priority Control
INTPND	0X4A000010			R/W	Interrupt Request Status
INTOFFSET	0X4A000014			R	Interrupt request source offset
SUBSRCPND	0X4A000018			R/W	Sub source pending
INTSUBMSK	0X4A00001C			R/W	Interrupt sub mask

Table 1-4. S3C2413X Special Registers (Sheet 3 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
DMA					
DISRC0	0x4B000000	←	W	R/W	DMA 0 Initial Source
DISRCC0	0x4B000004				DMA 0 Initial Source Control
DIDST0	0x4B000008				DMA 0 Initial Destination
DIDSTC0	0x4B00000C				DMA 0 Initial Destination Control
DCON0	0x4B000010				DMA 0 Control
DSTAT0	0x4B000014			R	DMA 0 Count
DCSRC0	0x4B000018				DMA 0 Current Source
DCDST0	0x4B00001C				DMA 0 Current Destination
DMASKTRIG0	0x4B000020			R/W	DMA 0 Mask Trigger
DMAREQSEL0	0x4B000024				DMA 0 Request Selection Register
DISRC1	0x4B000040				DMA 1 Initial Source
DISRCC1	0x4B000044				DMA 1 Initial Source Control
DIDST1	0x4B000048				DMA 1 Initial Destination
DIDSTC1	0x4B00004C				DMA 1 Initial Destination Control
DCON1	0x4B000050				DMA 1 Control
DSTAT1	0x4B000054			R	DMA 1 Count
DCSRC1	0x4B000058				DMA 1 Current Source
DCDST1	0x4B00005C				DMA 1 Current Destination
DMASKTRIG1	0x4B000060			R/W	DMA 1 Mask Trigger
DMAREQSEL1	0x4B000064				DMA 1 Request Selection Register
DISRC2	0x4B000080				DMA 2 Initial Source
DISRCC2	0x4B000084				DMA 2 Initial Source Control
DIDST2	0x4B000088				DMA 2 Initial Destination
DIDSTC2	0x4B00008C				DMA 2 Initial Destination Control
DCON2	0x4B000090				DMA 2 Control
DSTAT2	0x4B000094			R	DMA 2 Count
DCSRC2	0x4B000098				DMA 2 Current Source
DCDST2	0x4B00009C				DMA 2 Current Destination
DMASKTRIG2	0x4B0000A0			R/W	DMA 2 Mask Trigger
DMAREQSEL2	0x4B0000A4				DMA 2 Request Selection Register

DISRC3	0x4B0000C0	←	W	R/W	DMA 3 Initial Source
DISRCC3	0x4B0000C4				DMA 3 Initial Source Control
DIDST3	0x4B0000C8				DMA 3 Initial Destination
DIDSTC3	0x4B0000CC				DMA 3 Initial Destination Control
DCON3	0x4B0000D0				DMA 3 Control
DSTAT3	0x4B0000D4			R	DMA 3 Count

Table 1-4. S3C2413X Special Registers (Sheet 4 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
DMA(continue)					
DCSRC3	0x4B0000D8	←	W	R	DMA 3 Current Source
DCDST3	0x4B0000DC				DMA 3 Current Destination
DMASKTRIG3	0x4B0000E0			R/W	DMA 3 Mask Trigger
DMAREQSEL3	0x4B0000E4				DMA 3 Request Selection Register
ATA Controller					
ATA_CONTROL	0x4B800000	←	W	R/W	ATA control
ATA_STATUS	0x4B800004			R	ATA status
ATA_COMMAND	0x4B800008			R/W	ATA command
ATA_SWRST	0x4B80000C				ATA S/W reset
ATA_IRQ	0x4B800010				ATA IRQ
ATA_IRQ_MASK	0x4B800014				ATA IRQ MASK
ATA_CFG	0x4B800018				ATA configuration
ATA_PIO_TIME	0x4B80002C				ATA PIO time
ATA_XFR_NUM	0x4B800034				ATA data transfer number
ATA_XFR_CNT	0x4B800038				ATA data transfer count
ATA_TBUF_START	0x4B80003C				ATA tract buffer start adress
ATA_TBUF_SIZE	0x4B800040				ATA tract buffer size
ATA_SBUF_START	0x4B800044				ATA source buffer start adress
ATA_SBUF_SIZE	0x4B800048				ATA source buffer size
ATA_CADDR_TBUR	0x4B80004C				ATA tract buffer current address
ATA_CADDR_SBUR	0x4B800050				ATA source buffer current address
ATA_PIO_DTR	0x4B800054				ATA PIO 16 bit data
ATA_PIO_FED	0x4B800058				ATA PIO feature/error
ATA_PIO_SCR	0x4B80005C				ATA PIO sector count
ATA_PIO_LLR	0x4B800060				ATA PIO LBA low
ATA_PIO_LMR	0x4B800064				ATA PIO LBA middle
ATA_PIO_LHR	0x4B800068				ATA PIO LBA high
ATA_PIO_DVR	0x4B80006C				ATA PIO device
ATA_PIO_CSD	0x4B800070				ATA PIO command/status
ATA_PIO_DAD	0x4B800074				ATA PIO control/alternate status
ATA_PIO_READY	0x4B800078			R	ATA PIO READY
ATA_PIO_RDATA	0x4B80007C			R/W	ATA read data
BUS_FIFO_STATUS	0x4B800090			R	Bus FIFO status
ATA_FIFO_STATUS	0x4B800094				ATA FIFO status

Table 1-4. S3C2413X Special Registers (Sheet 5 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
Clock & Power Management					
LOCKTIME	0x4C000000	←	W	R/W	PLL Lock Time Counter
MPLLCON	0x4C000004				MPLL Control
UPLLCON	0x4C000008				UPLL Control
CLKCON	0x4C00000C				Clock Generator Control
CLKDIVN	0x4C000014				Clock divider Control
OSCSET	0x4C000018				Oscillator stabilization time counter
CLKSRC	0x4C00001C				Clock source Control
PWRMODECON	0x4C000020				Power management mode setting
PWRCFG	0x4C000024				Power management Configuration
ENDIAN	0x4C00002C				System endian control
SWRSTCON	0x4C000030				S/W reset control register
RSTCON	0x4C000034				Reset control
INFORM0	0x4C000070				User Defined information 0
INFORM1	0x4C000074				User Defined information 1
INFORM2	0x4C000078				User Defined information 2
INFORM3	0x4C00007C				User Defined information 3

Table 1-4. S3C2413X Special Registers (Sheet 6 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
LCD Controller					
LCDCON1	0X4D000000	←	W	R/W	LCD Control 1
LCDCON2	0X4D000004				LCD Control 2
LCDCON3	0X4D000008				LCD Control 3
LCDCON4	0X4D00000C				LCD Control 4
LCDCON5	0X4D000010				LCD Control 5
LCDSADDR1	0X4D000014				STN/TFT: Frame Buffer Start Address1
LCDSADDR2	0X4D000018				STN/TFT: Frame Buffer Start Address2
LCDSADDR3	0X4D00001C				STN/TFT: Virtual Screen Address Set
TPAL	0X4D000020				TFT: Temporary palette
LCDINTPND	0X4D000024				LCD Interrupt Pending
LCDSRCPND	0X4D000028				LCD Interrupt Source
LCDINTMSK	0X4D00002C				LCD Interrupt Mask
TCONSEL	0X4D000030				TCON(LPC3600/LCC3600) Control
LCDCON6	0X4D000034				LCD Control 6
LCDCON7	0X4D000038				LCD Control 7
LCDCON8	0X4D00003C				LCD Control 8
LCDCON9	0X4D000040				LCD Control 9
REDLUT0	0X4D000044				Red Lookup table[31:0]
REDLUT1	0X4D000048				Red Lookup table[63:32]
REDLUT2	0X4D00004C				Red Lookup table[95:64]
REDLUT3	0X4D000050				Red Lookup table[127:96]
REDLUT4	0X4D000054				Red Lookup table[159:128]
REDLUT5	0X4D000058				Red Lookup table[191:160]
REDLUT6	0X4D00005C				Red Lookup table[223:192]

Table 1-4. S3C2413X Special Registers (Sheet 7 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
LCD Controller(continue)					
GREENLUT0	0X4D000060	←	W	R/W	GREEN Lookup table[31:0]
GREENLUT1	0X4D000064				GREEN Lookup table[63:32]
GREENLUT2	0X4D000068				GREEN Lookup table[95:64]
GREENLUT3	0X4D00006C				GREEN Lookup table[127:96]
GREENLUT4	0X4D000070				GREEN Lookup table[159:128]
GREENLUT5	0X4D000074				GREEN Lookup table[191:160]
GREENLUT6	0X4D000078				GREEN Lookup table[223:192]
GREENLUT7	0X4D00007C				GREEN Lookup table[255:224]
GREENLUT8	0X4D000080				GREEN Lookup table[287:256]
GREENLUT9	0X4D000084				GREEN Lookup table[319:288]
GREENLUT10	0X4D000088				GREEN Lookup table[351:320]
GREENLUT11	0X4D00008C				GREEN Lookup table[383:352]
GREENLUT12	0X4D000090				GREEN Lookup table[415:384]
GREENLUT13	0X4D000094				GREEN Lookup table[447:416]
BLUELUT0	0X4D000098				BLUE Lookup table[31:0]
BLUELUT1	0X4D00009C				BLUE Lookup table[63:32]
BLUELUT2	0X4D0000A0				BLUE Lookup table[95:64]
BLUELUT3	0X4D0000A4				BLUE Lookup table[127:96]
BLUELUT4	0X4D0000A8				BLUE Lookup table[159:128]
BLUELUT5	0X4D0000AC				BLUE Lookup table[191:160]
BLUELUT6	0X4D0000B0				BLUE Lookup table[223:192]

Table 1-4. S3C2413X Special Registers (Sheet 8 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
LCD Controller(continue)					
FRCPAT0	0X4D0000B4	←	W	R/W	FRC Pattern Register
FRCPAT1	0X4D0000B8				FRC Pattern Register
FRCPAT2	0X4D0000BC				FRC Pattern Register
FRCPAT3	0X4D0000C0				FRC Pattern Register
FRCPAT4	0X4D0000C4				FRC Pattern Register
FRCPAT5	0X4D0000C8				FRC Pattern Register
FRCPAT6	0X4D0000CC				FRC Pattern Register
FRCPAT7	0X4D0000D0				FRC Pattern Register
FRCPAT8	0X4D0000D4				FRC Pattern Register
FRCPAT9	0X4D0000D8				FRC Pattern Register
FRCPAT10	0X4D0000DC				FRC Pattern Register
FRCPAT11	0X4D0000E0				FRC Pattern Register
FRCPAT12	0X4D0000E4				FRC Pattern Register
FRCPAT13	0X4D0000E8				FRC Pattern Register
FRCPAT14	0X4D0000EC				FRC Pattern Register
FRCPAT15	0X4D0000F0				FRC Pattern Register
FRCPAT16	0X4D0000F4				FRC Pattern Register
FRCPAT17	0X4D0000F8				FRC Pattern Register
FRCPAT18	0X4D0000FC				FRC Pattern Register
FRCPAT19	0X4D000100				FRC Pattern Register
FRCPAT20	0X4D000104				FRC Pattern Register
FRCPAT21	0X4D000108				FRC Pattern Register
FRCPAT22	0X4D00010C				FRC Pattern Register
FRCPAT23	0X4D000110				FRC Pattern Register
FRCPAT24	0X4D000114				FRC Pattern Register
FRCPAT25	0X4D000118				FRC Pattern Register
FRCPAT26	0X4D00011C				FRC Pattern Register
FRCPAT27	0X4D000120				FRC Pattern Register
FRCPAT28	0X4D000124				FRC Pattern Register
FRCPAT29	0X4D000128				FRC Pattern Register
FRCPAT30	0X4D00012C				FRC Pattern Register

Table 1-4. S3C2413X Special Registers (Sheet 9 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
LCD Controller(continue)					
FRCPAT31	0X4D000130	←	W	R/W	FRC Pattern Register
FRCPAT32	0X4D000134				FRC Pattern Register
FRCPAT33	0X4D000138				FRC Pattern Register
FRCPAT34	0X4D00013C				FRC Pattern Register
FRCPAT35	0X4D000140				FRC Pattern Register
FRCPAT36	0X4D000144				FRC Pattern Register
FRCPAT37	0X4D000148				FRC Pattern Register
FRCPAT38	0X4D00014C				FRC Pattern Register
FRCPAT39	0X4D000150				FRC Pattern Register
FRCPAT40	0X4D000154				FRC Pattern Register
FRCPAT41	0X4D000158				FRC Pattern Register
FRCPAT42	0X4D00015C				FRC Pattern Register
FRCPAT43	0X4D000160				FRC Pattern Register
FRCPAT44	0X4D000164				FRC Pattern Register
FRCPAT45	0X4D000168				FRC Pattern Register
FRCPAT46	0X4D00016C				FRC Pattern Register
FRCPAT47	0X4D000170				FRC Pattern Register
FRCPAT48	0X4D000174				FRC Pattern Register
FRCPAT49	0X4D000178				FRC Pattern Register
FRCPAT50	0X4D00017C				FRC Pattern Register
FRCPAT51	0X4D000180				FRC Pattern Register
FRCPAT52	0X4D000184				FRC Pattern Register
FRCPAT53	0X4D000188				FRC Pattern Register
FRCPAT54	0X4D00018C				FRC Pattern Register
FRCPAT55	0X4D000190				FRC Pattern Register
FRCPAT56	0X4D000194				FRC Pattern Register
FRCPAT57	0X4D000198				FRC Pattern Register
FRCPAT58	0X4D00019C				FRC Pattern Register
FRCPAT59	0X4D0001A0				FRC Pattern Register
FRCPAT60	0X4D0001A4				FRC Pattern Register
FRCPAT61	0X4D0001A8				FRC Pattern Register
FRCPAT62	0X4D0001AC				FRC Pattern Register
FRCPAT63	0X4D0001B0				FRC Pattern Register

Table 1-4. S3C2413X Special Registers (Sheet 10 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
Camera Interface					
CISRCFMT	0x4D800000	←	W	RW	Input Source Format
CIWDOFST	0x4D800004				Window offset register
CIGCTRL	0x4D800008				Global control register
CIDOWSFT2	0x4D800014				Window option register 2
CICOYSA1	0x4D800018				Y 1st frame start address for codec DMA
CICOYSA2	0x4D80001C				Y 2nd frame start address for codec DMA
CICOYSA3	0x4D800020				Y 3rd frame start address for codec DMA
CICOYSA4	0x4D800024				Y 4th frame start address for codec DMA
CICOCBSA1	0x4D800028				Cb 1st frame start address for codec DMA
CICOCBSA2	0x4D80002C				Cb 2nd frame start address for codec DMA
CICOCBSA3	0x4D800030				Cb 3rd frame start address for codec DMA
CICOCBSA4	0x4D800034				Cb 4th frame start address for codec DMA
CICOCRSA1	0x4D800038				Cr 1st frame start address for codec DMA
CICOCRSA2	0x4D80003C				Cr 2nd frame start address for codec DMA
CICOCRSA3	0x4D800040				Cr 3rd frame start address for codec DMA
CICOCRSA4	0x4D800044				Cr 4th frame start address for codec DMA
CICOTRGFMT	0x4D800048				Target image format of codec DMA
CICOCTRL	0x4D80004C				Codec DMA control related
CICOSCPRERATIO	0x4D800050				Codec pre-scaler ratio control
CICOSCPREDST	0x4D800054				Codec pre-scaler destination format
CICOSCCTRL	0x4D800058				Codec main-scaler control
CICOTAREA	0x4D80005C				Codec scaler target area
CICOSTATUS	0x4D800064				Codec path status
CIIMGCPT	0x4D8000A0				Image capture enable command
CICOCPTSEQ	0x4D8000A4				Codec dma capture sequence related
COCOSCOS	0x4D8000A8				Codec scan line offset related
CIIMGEFF	0x4D8000B0				Image Effects related

Table 1-4. S3C2413X Special Registers (Sheet 11 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
NAND Flash					
NFCONF	0x4E000000	←	W	R/W	NAND Flash Configuration
NFCONT	0x4E000004				NAND Flash Control
NFCMMD	0x4E000008				NAND Flash Command
NFADDR	0x4E00000C				NAND Flash Address
NFDATA	0x4E000010				NAND Flash Data
NFMECCD0	0x4E000014				NAND Flash Main area ECC0/1
NFMECCD1	0x4E000018				NAND Flash Main area ECC2/3
NFSECCD	0x4E00001C				NAND Flash Spare area ECC
NFSBLK	0x4E000020				NAND Flash start block address
NFEBLK	0x4E000024				NAND Flash end block address
NFSTAT	0x4E000028				NAND Flash Operation Status
NFECCERR0	0x4E00002C			R	NAND Flash ECC error Status 0
NFECCERR1	0x4E000030				NAND Flash ECC error Status 1
NFMECC0	0x4E000034				NAND Flash Main area ECC0 status
NFMECC1	0x4E000038				NAND Flash Main Area ECC1 status
NFSECC	0x4E00003C				NAND Flash Spare Area ECC status
NFMLCBITPT	0x4E000040				4-bit ECC error bit pattern

Table 1-4. S3C2413X Special Registers (Sheet 12 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
SSMC					
SMBIDCYR0	0x4F000000	←	W	R/W	BANK0 idle cycle control
SMBWSTRDR0	0x4F000004				BANK0 read wait state control
SMBWSTWRR0	0x4F000008				BANK0 write wait state control
SMBWSTOENR0	0x4F00000C				BANK0 output enable assertion delay control
SMBWSTWENR0	0x4F000010				BANK0 write enable assertion delay control
SMBCR0	0x4F000014				BANK0 control
SMBSR0	0x4F000018				BANK0 status
SMBWSTBRDR0	0x4F00001C				BANK0 burst read wait delay control
SMBIDCYR1	0x4F000020				BANK1 idle cycle control
SMBWSTRDR1	0x4F000024				BANK1 read wait state control
SMBWSTWRR1	0x4F000028				BANK1 write wait state control
SMBWSTOENR1	0x4F00002C				BANK1 output enable assertion delay control
SMBWSTWENR1	0x4F000030				BANK1 write enable assertion delay control
SMBCR1	0x4F000034				BANK1 control
SMBSR1	0x4F000038				BANK1 status
SMBWSTBRDR1	0x4F00003C				BANK1 burst read wait delay control
SMBIDCYR2	0x4F000040				BANK2 idle cycle control
SMBWSTRDR2	0x4F000044				BANK2 read wait state control
SMBWSTWRR2	0x4F000048				BANK2 write wait state control
SMBWSTOENR2	0x4F00004C				BANK2 output enable assertion delay control
SMBWSTWENR2	0x4F000050				BANK2 write enable assertion delay control
SMBCR2	0x4F000054				BANK2 control
SMBSR2	0x4F000058				BANK2 status
SMBWSTBRDR2	0x4F00005C				BANK2 burst read wait delay control

Table 1-4. S3C2413X Special Registers (Sheet 13 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
SSMC(continue)					
SMBIDCYR3	0x4F000060	←	W	R/W	BANK3 idle cycle control
SMBWSTRDR3	0x4F000064				BANK3 read wait state control
SMBWSTWRR3	0x4F000068				BANK3 write wait state control
SMBWSTOENR3	0x4F00006C				BANK3 output enable assertion delay control
SMBWSTWENR3	0x4F000070				BANK3 write enable assertion delay control
SMBCR3	0x4F000074				BANK3 control
SMBSR3	0x4F000078				BANK3 status
SMBWSTBRDR3	0x4F00007C				BANK3 burst read wait delay control
SMBIDCYR4	0x4F000080				BANK4 idle cycle control
SMBWSTRDR4	0x4F000084				BANK4 read wait state control
SMBWSTWRR4	0x4F000088				BANK4 write wait state control
SMBWSTOENR4	0x4F00008C				BANK4 output enable assertion delay control
SMBWSTWENR4	0x4F000090				BANK4 write enable assertion delay control
SMBCR4	0x4F000094				BANK4 control
SMBSR4	0x4F000098				BANK4 status
SMBWSTBRDR4	0x4F00009C				BANK4 burst read wait delay control
SMBIDCYR5	0x4F0000A0				BANK5 idle cycle control
SMBWSTRDR5	0x4F0000A4				BANK5 read wait state control
SMBWSTWRR5	0x4F0000A8				BANK5 write wait state control
SMBWSTOENR5	0x4F0000AC				BANK5 output enable assertion delay control
SMBWSTWENR5	0x4F0000B0				BANK5 write enable assertion delay control
SMBCR5	0x4F0000B4				BANK5 control
SMBSR5	0x4F0000B8				BANK5 status
SMBWSTBRDR5	0x4F0000BC				BANK5 burst read wait delay control

Table 1-4. S3C2413X Special Registers (Sheet 14 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
SSMC(continue)					
SMBIDCYR6	0x4F0000C0	←	W	R/W	BANK6 idle cycle control
SMBWSTRDR6	0x4F0000C4				BANK6 read wait state control
SMBWSTWRR6	0x4F0000C8				BANK6 write wait state control
SMBWSTOENR6	0x4F0000CC				BANK6 output enable assertion delay control
SMBWSTWENR6	0x4F0000D0				BANK6 write enable assertion delay control
SMBCR6	0x4F0000D4				BANK6 control
SMBSR6	0x4F0000D8				BANK6 status
SMBWSTBRDR6	0x4F0000DC				BANK6 burst read wait delay control
SMBIDCYR7	0x4F0000E0				BANK7 idle cycle control
SMBWSTRDR7	0x4F0000E4				BANK7 read wait state control
SMBWSTWRR7	0x4F0000E8				BANK7 write wait state control
SMBWSTOENR7	0x4F0000EC				BANK7 output enable assertion delay control
SMBWSTWENR7	0x4F0000F0				BANK7 write enable assertion delay control
SMBCR7	0x4F0000F4				BANK7 control
SMBSR7	0x4F0000F8				BANK7 status
SMBWSTBRDR7	0x4F0000FC				BANK7 burst read wait delay control
SSMCSR	0x4F000200			R	SROMC status
SSMCCR	0x4F000204			R/W	SROMC control

Table 1-4. S3C2413X Special Registers (Sheet 15 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
UART					
ULCON0	0x50000000	←	W	R/W	UART 0 Line Control
UCON0	0x50000004				UART 0 Control
UFCON0	0x50000008				UART 0 FIFO Control
UMCON0	0x5000000C				UART 0 Modem Control
UTRSTAT0	0x50000010			R	UART 0 Tx/Rx Status
UERSTAT0	0x50000014				UART 0 Rx Error Status
UFSTAT0	0x50000018				UART 0 FIFO Status
UMSTAT0	0x5000001C				UART 0 Modem Status
UTXH0	0x50000023	0x50000020	B	W	UART 0 Transmission Hold
URXH0	0x50000027	0x50000024		R	UART 0 Receive Buffer
UBRDIV0	0x50000028	←	W	R/W	UART 0 Baud Rate Divisor
UDIVSLOT0	0x5000002C				Baud rate division
ULCON1	0x50004000				UART 1 Line Control
UCON1	0x50004004				UART 1 Control
UFCON1	0x50004008				UART 1 FIFO Control
UMCON1	0x5000400C				UART 1 Modem Control
UTRSTAT1	0x50004010			R	UART 1 Tx/Rx Status
UERSTAT1	0x50004014				UART 1 Rx Error Status
UFSTAT1	0x50004018				UART 1 FIFO Status
UMSTAT1	0x5000401C				UART 1 Modem Status
UTXH1	0x50004023	0x50004020	B	W	UART 1 Transmission Hold
URXH1	0x50004027	0x50004024		R	UART 1 Receive Buffer
UBRDIV1	0x50004028	←	W	R/W	UART 1 Baud Rate Divisor
UDIVSLOT0	0x5000402C				Baud rate division
ULCON2	0x50008000				UART 2 Line Control
UCON2	0x50008004				UART 2 Control
UFCON2	0x50008008				UART 2 FIFO Control
UTRSTAT2	0x50008010			R	UART 2 Tx/Rx Status
UERSTAT2	0x50008014				UART 2 Rx Error Status
UFSTAT2	0x50008018				UART 2 FIFO Status

UTXH2	0x50008023	0x50008020	B	W	UART 2 Transmission Hold
URXH2	0x50008027	0x50008024		R	UART 2 Receive Buffer
UBRDIV2	0x50008028	←	W	R/W	UART 2 Baud Rate Divisor
UDIVSLOT0	0x5000802C				Baud rate division

Table 1-4. S3C2413X Special Registers (Sheet 16 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
PWM Timer					
TCFG0	0x51000000	←	W	R/W	Timer Configuration
TCFG1	0x51000004				Timer Configuration
TCON	0x51000008				Timer Control
TCNTB0	0x5100000C				Timer Count Buffer 0
TCMPB0	0x51000010				Timer Compare Buffer 0
TCNTO0	0x51000014			R	Timer Count Observation 0
TCNTB1	0x51000018			R/W	Timer Count Buffer 1
TCMPB1	0x5100001C				Timer Compare Buffer 1
TCNTO1	0x51000020			R	Timer Count Observation 1
TCNTB2	0x51000024			R/W	Timer Count Buffer 2
TCMPB2	0x51000028				Timer Compare Buffer 2
TCNTO2	0x5100002C			R	Timer Count Observation 2
TCNTB3	0x51000030			R/W	Timer Count Buffer 3
TCMPB3	0x51000034				Timer Compare Buffer 3
TCNTO3	0x51000038			R	Timer Count Observation 3
TCNTB4	0x5100003C			R/W	Timer Count Buffer 4
TCNTO4	0x51000040			R	Timer Count Observation 4

Table 1-4. S3C2413X Special Registers (Sheet 17 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
USB Device					
FUNC_ADDR_REG	0x52000143	0x52000140	B	R/W	Function Address
PWR_REG	0x52000147	0x52000144			Power Management
EP_INT_REG	0x5200014B	0x52000148			EP Interrupt Pending and Clear
USB_INT_REG	0x5200015B	0x52000158			USB Interrupt Pending and Clear
EP_INT_EN_REG	0x5200015F	0x5200015C			Interrupt Enable
USB_INT_EN_REG	0x5200016F	0x5200016C			Interrupt Enable
FRAME_NUM1_REG	0x52000173	0x52000170		R	Frame Number Lower Byte
FRAME_NUM2_REG	0x52000177	0x52000174			Frame Number Higher Byte
INDEX_REG	0x5200017B	0x52000178		R/W	Register Index
MAXP_REG	0x52000183	0x52000180			Endpoint MAX packet register
EP0_CSR	0x52000187	0x52000184			Endpoint 0 Status
IN_CSR1_REG	0x52000187	0x52000184			In Endpoint Control Status
IN_CSR2_REG	0x5200018B	0x52000188			In Endpoint Control Status
MAXP_REG	0x52000183	0x52000180			Endpoint Max Packet
OUT_CSR1_REG	0x52000193	0x52000190			Out Endpoint Control Status
OUT_CSR2_REG	0x52000197	0x52000194			Out Endpoint Control Status
OUT_FIFO_CNT1_REG	0x5200019B	0x52000198		R	Endpoint Out Write Count
OUT_FIFO_CNT2_REG	0x5200019F	0x5200019C			Endpoint Out Write Count
EP0_FIFO	0x520001C3	0x520001C0		R/W	Endpoint 0 FIFO
EP1_FIFO	0x520001C7	0x520001C4			Endpoint 1 FIFO
EP2_FIFO	0x520001CB	0x520001C8			Endpoint 2 FIFO
EP3_FIFO	0x520001CF	0x520001CC			Endpoint 3 FIFO
EP4_FIFO	0x520001D3	0x520001D0			Endpoint 4 FIFO
EP1_DMA_CON	0x52000203	0x52000200			EP1 DMA Interface Control
EP1_DMA_UNIT	0x52000207	0x52000204			EP1 DMA Tx Unit Counter
EP1_DMA_FIFO	0x5200020B	0x52000208			EP1 DMA Tx FIFO Counter
EP1_DMA_TTC_L	0x5200020F	0x5200020C			EP1 DMA Total Tx Counter
EP1_DMA_TTC_M	0x52000213	0x52000210			EP1 DMA Total Tx Counter
EP1_DMA_TTC_H	0x52000217	0x52000214			EP1 DMA Total Tx Counter
EP2_DMA_CON	0x5200021B	0x52000218			EP2 DMA Interface Control
EP2_DMA_UNIT	0x5200021F	0x5200021C			EP2 DMA Tx Unit Counter
EP2_DMA_FIFO	0x52000223	0x52000220			EP2 DMA Tx FIFO Counter

Table 1-4. S3C2413X Special Registers (Sheet 18 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/Write	Function
USB Device (Continued)					
EP2_DMA_TTC_L	0x52000227	0x52000224	B	R/W	EP2 DMA Total Tx Counter
EP2_DMA_TTC_M	0x5200022B	0x52000228			EP2 DMA Total Tx Counter
EP2_DMA_TTC_H	0x5200022F	0x5200022C			EP2 DMA Total Tx Counter
EP3_DMA_CON	0x52000243	0x52000240			EP3 DMA Interface Control
EP3_DMA_UNIT	0x52000247	0x52000244			EP3 DMA Tx Unit Counter
EP3_DMA_FIFO	0x5200024B	0x52000248			EP3 DMA Tx FIFO Counter
EP3_DMA_TTC_L	0x5200024F	0x5200024C			EP3 DMA Total Tx Counter
EP3_DMA_TTC_M	0x52000253	0x52000250			EP3 DMA Total Tx Counter
EP3_DMA_TTC_H	0x52000257	0x52000254			EP3 DMA Total Tx Counter
EP4_DMA_CON	0x5200025B	0x52000258			EP4 DMA Interface Control
EP4_DMA_UNIT	0x5200025F	0x5200025C			EP4 DMA Tx Unit Counter
EP4_DMA_FIFO	0x52000263	0x52000260			EP4 DMA Tx FIFO Counter
EP4_DMA_TTC_L	0x52000267	0x52000264			EP4 DMA Total Tx Counter
EP4_DMA_TTC_M	0x5200026B	0x52000268			EP4 DMA Total Tx Counter
EP4_DMA_TTC_H	0x5200026F	0x5200026C			EP4 DMA Total Tx Counter
Watchdog Timer					
WTCON	0x53000000	←	W	R/W	Watchdog Timer Mode
WTDAT	0x53000004				Watchdog Timer Data
WTCNT	0x53000008				Watchdog Timer Count
IIC					
IICCON	0x54000000	←	W	R/W	IIC Control
IICSTAT	0x54000004				IIC Status
IICADD	0x54000008				IIC Address
IICDS	0x5400000C				IIC Data Shift
IICLC	0x54000010				IIC multi-master line control
IIS					
I2SCON	0x55000000	←	W	R/W	IIS Control
I2SMOD	0x55000004				IIS Mode
I2SFIC	0x55000008				IIS FIFO control
I2SPSR	0x5500000C				IIS Prescaler
I2STXD	0x55000010			W	IIS transmit date
I2SRXD	0x55000014			R	IIS receive data

Table 1-4. S3C2413X Special Registers (Sheet 19 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
I/O port					
GPACON	0x56000000	←	W	R/W	Port A Control
GPADAT	0x56000004				Port A Data
GPBCON	0x56000010				Port B Control
GPBDAT	0x56000014				Port B Data
GPBDN	0x56000018				Pull-down Control B
GPBSLPCON	0x5600001C				Port B sleep mode configuration
GPCCON	0x56000020				Port C Control
GPCDAT	0x56000024				Port C Data
GPCDN	0x56000028				Pull-down Control C
GPCSLPCON	0x5600002C				Port C sleep mode configuration
GPDCON	0x56000030				Port D Control
GPDDA1T	0x56000034				Port D Data
GPDDN	0x56000038				Pull-down Control D
GPDSLPCON	0x5600003C				Port D sleep mode configuration
GPECON	0x56000040				Port E Control
GPEDAT	0x56000044				Port E Data
GPEDN	0x56000048				Pull-down Control E
GPESLPCON	0x5600004C				Port E sleep mode configuration
GPFCON	0x56000050				Port F Control
GPFDAT	0x56000054				Port F Data
GPFDN	0x56000058				Pull-down Control F
GPGCON	0x56000060				Port G Control
GPGDAT	0x56000064				Port G Data
GPGDN	0x56000068				Pull-down Control G
GPGSLPCON	0x5600006C				Port G sleep mode configuration
GPHCON	0x56000070				Port H Control
GPHDAT	0x56000074				Port H Data
GPHDN	0x56000078				Pull-down Control H
GPHSLPCON	0x5600007C				Port H sleep mode configuration
GPJCON	0x56000080				Port J Control
GPJDAT	0x56000084				Port J Data
GPJDN	0x56000088				Pull-down Control J
GPJSLPCON	0x5600008C				Port J sleep mode configuration
MISCCR	0x56000090				Miscellaneous Control
DCLKCON	0x56000094				DCLK0/1 Control

Table 1-4. S3C2413X Special Registers (Sheet 20 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
I/O port (Continued)					
EXTINT0	0x56000098	←	W	R/W	External Interrupt Control Register 0
EXTINT1	0x5600009C				External Interrupt Control Register 1
EXTINT2	0x560000A0				External Interrupt Control Register 2
EINTFLT0	0x560000A4				Reserved
EINTFLT1	0x560000A8				Reserved
EINTFLT2	0x560000AC				External Interrupt Filter Control Register 2
EINTFLT3	0x560000B0				External Interrupt Filter Control Register 3
EINTMASK	0x560000B4				External Interrupt Mask
EINTPEND	0x560000B8				External Interrupt Pending
GSTATUS0	0x560000BC			R	External Pin Status
GSTATUS1	0x560000C0				Chip ID
GSTATUS2	0x560000C4			R/W	Reset Status
GSTATUS3	0x560000C8				Inform Register
GSTATUS4	0x560000CC				Inform Register
GSTATUS5	0x560000D0				Inform Register
MSTCON	0x560000D4				Memory port Stop control
MSLCON	0x560000D8				Memory port Sleep control
DSC0	0x560000DC				Strength control 0
DSC1	0x560000E0				Strength control 0

Table 1-4. S3C2413X Special Registers (Sheet 21 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
RTC					
RTCCON	0x57000043	0x57000040	B	R/W	RTC Control
TICNT0	0x57000047	0x57000044			Tick time count 0
TICNT1	0x5700004F	0x5700004C			Tick time count 1
RTCALM	0x57000053	0x57000050			RTC Alarm Control
ALMSEC	0x57000057	0x57000054			Alarm Second
ALMMIN	0x5700005B	0x57000058			Alarm Minute
ALMHOUR	0x5700005F	0x5700005C			Alarm Hour
ALMDATE	0x57000063	0x57000060			Alarm Day
ALMMON	0x57000067	0x57000064			Alarm Month
ALMYEAR	0x5700006B	0x57000068			Alarm Year
BCDSEC	0x57000073	0x57000070			BCD Second
BCDMIN	0x57000077	0x57000074			BCD Minute
BCDHOUR	0x5700007B	0x57000078			BCD Hour
BCDDATE	0x5700007F	0x5700007C			BCD Day
BCDDAY	0x57000083	0x57000080			BCD Date
BCDMON	0x57000087	0x57000084			BCD Month
BCDYEAR	0x5700008B	0x57000088			BCD Year

Table 1-4. S3C2413X Special Registers (Sheet 22 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
A/D converter					
ADCCON	0x58000000	←	W	R/W	ADC Control
ADCTSC	0x58000004				ADC Touch Screen Control
ADCDLY	0x58000008				ADC Start or Interval Delay
ADCDAT0	0x5800000C			R	ADC Conversion Data
ADCDAT1	0x58000010				ADC Conversion Data
SPI					
SPCON0,1	0x59000000,100	←	W	R/W	SPI Control
SPSTA0,1	0x59000004,104			R	SPI Status
SPPIN0,1	0x59000008,108			R/W	SPI Pin Control
SPPRE0,1	0x5900000C,10C				SPI Baud Rate Prescaler
SPTDAT0,1	0x59000010,110				SPI Tx Data
SPRDAT0,1	0x59000014,114			R	SPI Rx Data
SPTXFIFO0,1	0x59000018,118			W	SPI Tx FIFO
SPRXFIFO0,1	0x5900001C,11C			R	SPI Rx FIFO
SPRDATB0,1	0x59000020,120				SPI Rx Data
SPFIC0,1	0x59000024,124			R/W	SPI FIFO interrupt and DMA control

Table 1-4. S3C2413X Special Registers (Sheet 23 of 23)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
SD interface					
SDICON	0x5A000000	←	W	R/W	SDI Control
SDIPRE	0x5A000004				SDI Baud Rate Prescaler
SDICARG	0x5A000008				SDI Command Argument
SDICCON	0x5A00000C				SDI Command Control
SDICSTA	0x5A000010			R/(C)	SDI Command Status
SDIRSP0	0x5A000014			R	SDI Response
SDIRSP1	0x5A000018				SDI Response
SDIRSP2	0x5A00001C				SDI Response
SDIRSP3	0x5A000020				SDI Response
SDIDTIMER	0x5A000024			R/W	SDI Data / Busy Timer
SDIBSIZE	0x5A000028				SDI Block Size
SDIDCON	0x5A00002C				SDI Data control
SDIDCNT	0x5A000030			R	SDI Data Remain Counter
SDIDSTA	0x5A000034			R/(C)	SDI Data Status
SDIFSTA	0x5A000038				SDI FIFO Status
SDIIMSK	0x5A00003C	←	W	R/W	SDI Interrupt Mask
SDIDAT	0x5A000043	0x5A000040	B		SDI Data

Cautions on S3C2413X Special Registers

1. In the little endian mode ‘L’, endian address must be used. In the big endian mode ‘B’ endian address must be used.
2. The special registers have to be accessed for each recommended access unit.
3. All registers except ADC registers, RTC registers and UART registers must be read/write in word unit (32bit) in little/big endian.
4. Make sure that the ADC registers, RTC registers and UART registers be read/write by the specified access unit and the specified address. Moreover, one must carefully consider which endian mode is used.
5. W : 32-bit register, which must be accessed by LDR/STR or int type pointer(int *).
   HW : 16-bit register, which must be accessed by LDRH/STRH or short int type pointer(short int *).
   B : 8-bit register, which must be accessed by LDRB/STRB or char type pointer(char int *).

2 EBI

INTRODUCTION

S3C2413X EBI (External Bus Interface) features are as follows

- EBI is the bus multiplexer supporting the share of pad interface used by 4 memory controllers (SROMC, DRAMC, NAND flash and CF).
- Pad interface ownership is determined by the priority that can be changed.
- The handshaking between the EBI and the memory controller consists of s a three-wire interface, EBIREG, EBIGNT, and EBIBACKOFF, all active HIGH:

  EBIREG signals are asserted by memory controllers to indicate that they require external bus access.

  the respective arbitrated EBIGNT is issued to the highest priority memory controller.

  EBIBACKOFF is output by the EBI to signal that the memory controller must complete the current transfer and release the bus.
- The EBI arbitration scheme keeps track of the memory controller that is currently granted and waits for the transaction from that memory controller to finish (EBIREQ taken LOW by the memory controller) before it grants the next memory controller. If a higher priority memory controller requests the bus then EBIBACKOFF signal tells the currently granted memory controller to terminate the current transfer as soon as possible.

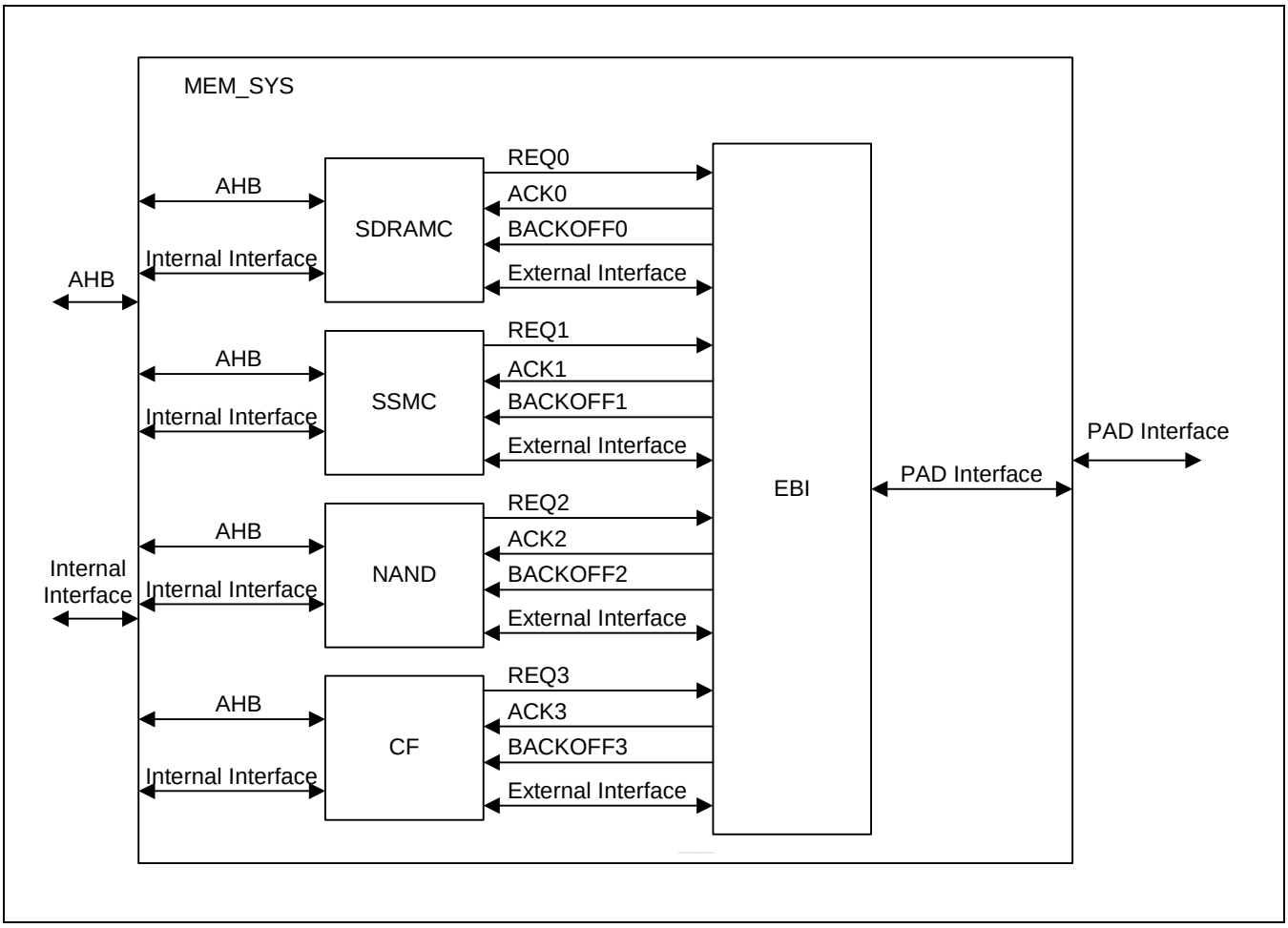


Figure 2-1. Memory interface through EBI

FUNCTIONAL DESCRIPTION

The EBI, as a peripheral, relies on the memory controllers to release their external requests for the external bus when they are idle, because it has no other knowledge of when a transfer starts or completes.

Figure 2-2. shows a simple handshake example. In this example, a device requests the external bus and is immediately granted because no other devices are requesting the bus.

If a higher priority device requests the bus, when a lower priority device is in control of the external bus then the EBIBACKOFF signal tells the lower priority device to release the bus as soon as possible. Figure 2-3. shows a an example of this.

In Figure 2-3., a higher priority device requests the bus, shortly after a device has been granted the bus. The EBIBACKOFF signal tells the device to end the access early. Device 1 is granted the bus and completes its transfer. When the transfer is complete then device 2 is granted the bus and completes the transfer that was interrupted. The EBIREQ2 signal must be LOW for at least one clock cycle and after this, you can reassert it.

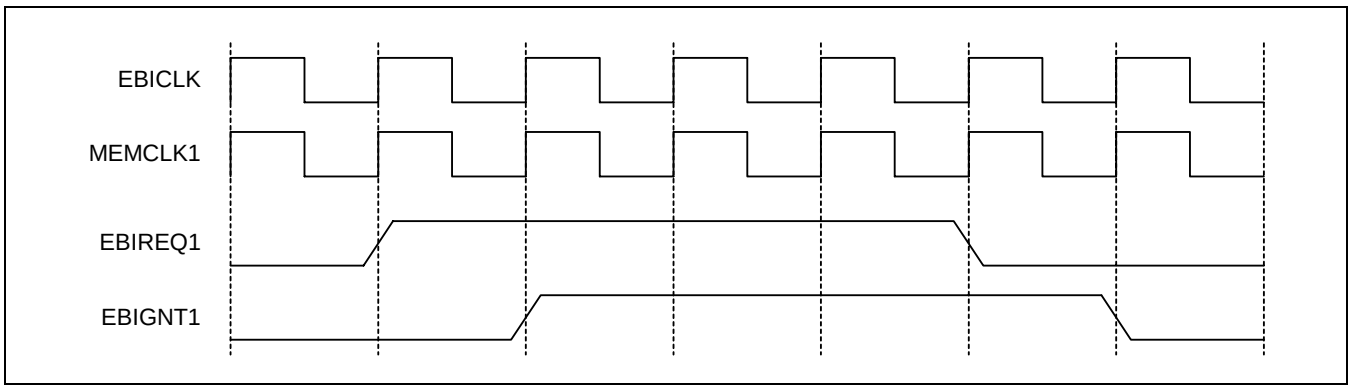


Figure 2-2. EBIREQ, EBIGANT signals

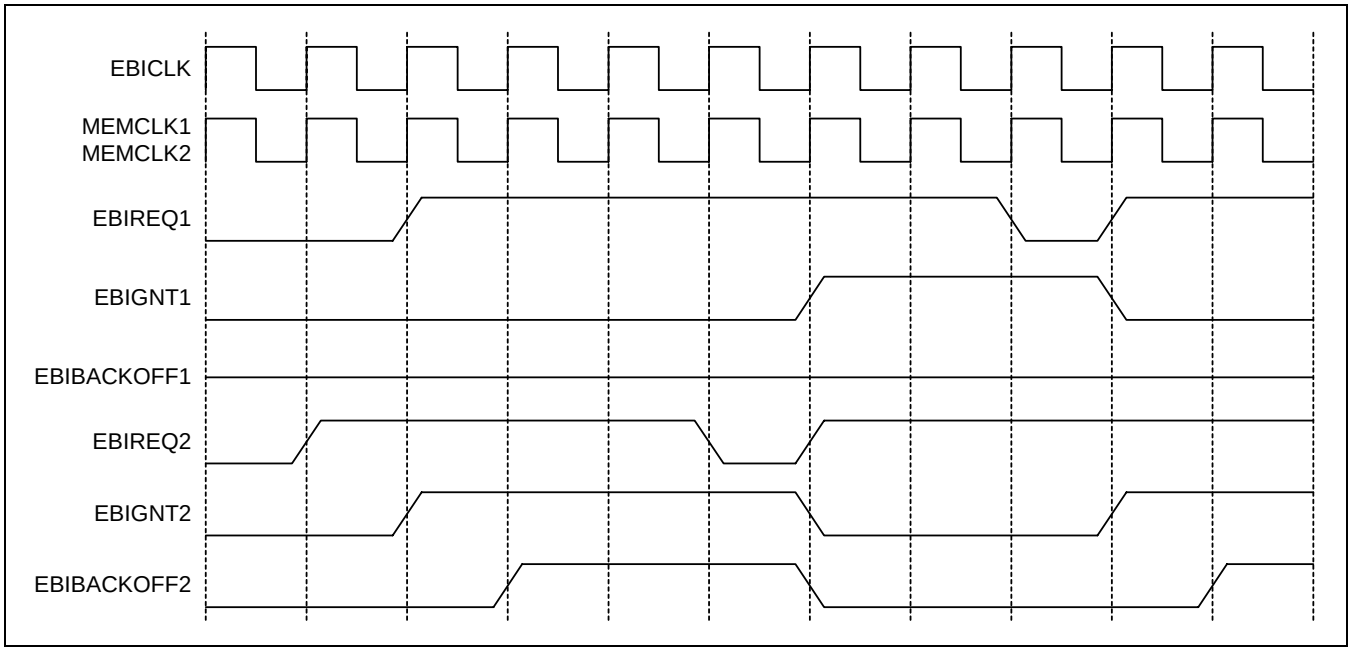


Figure 2-3. EBIBACKOFF signal

EBI SPECIAL REGISTERS

BUS PRIORITY DECISION REGISTER

Register	Address	R/W	Description	Reset Value
EBIPR	0x4880000	R/W	Bus priority decision	0x0000_0000

EBIPR	Bit	Description							Initial State
Reserved	[31:3]	Reserved							0x0000_000
EBIPR	[2:0]	bit value priority order	000	001	010	011	100	101	0x0
		1	One	One	NAND	CF	NAND	CF	
		2	NAND	CF	One	One	CF	NAND	
		3	CF	NAND	CF	NAND	One	One	

BANK CONFIGURATION REGISTER

Register	Address	R/W	Description	Reset Value
BANK_CFG	0x4880004	R/W	Bank Configuration register	0x0000_0000

EBIPR	Bit	Description	Initial State
Reserved	**[31:8]**	Reserved	0x0000_00
	[7]	BANK 7 conf. 0 : one NAND/SRAM 1: SDRAM	0b
	[6]	BANK 6 conf. 0 : one NAND/SRAM 1: SDRAM	0b
	[5]	BANK 5 conf. 0 : one NAND/SRAM 1 : CF	0b
	[4]	BANK 4 conf. 0 : one NAND/SRAM 1 : CF	0b
	[3]	BANK 3 conf. 0 : one NAND/SRAM 1: NANDFlash	0b
	[2]	BANK 2 conf. 0 : one NAND/SRAM 1: NANDFlash	0b
	[1:0]	Reserved	0b

3 DRAM CONTROLLER

OVERVIEW

The S3C2413 DRAM Controller supports two kinds of memory interface. One is for SDRAM/Mobile SDRAM and the other is for DDR/mobile DDR memory interface. DRAM controller provides 2 chip select signals (2 memory banks), these are used for up to 2 SDRAM/mobile SDRAM banks or 2 DDR/mobile DDR banks. DRAM controller can't support 2 kinds of memory interface simultaneous, for example one bank for SDRAM/mobile SDRAM and one bank for DDR/mobile DDR

- DRAM controller has the following features:
  - DDR/mobile DDR SDRAM and SDRAM/Mobile SDRAM
  - Supports 16/32-bit data bus interface for SDRAM/mobile SDRAM
  - Supports 16-bit data bus interface for DDR/mobile DDR
  - Supports up to 1Gbit memory per bank
  - Supports 2 banks: 2-nCS (chip selection)
  - 16-bit Refresh Timer
  - Self Refresh Mode support (controlled by power management)
  - Programmable CAS Latency
  - Provide Write buffer: 8-word size
  - Provide pre-charge and active power down mode
  - Provide power save mode
  - Support EMRS (Extended MRS) for mobile DRAM
    - DS, TSCR, PASR

BLOCK DIAGRAM

Follow figure 3-1 shows the block diagram of DRAM Controller

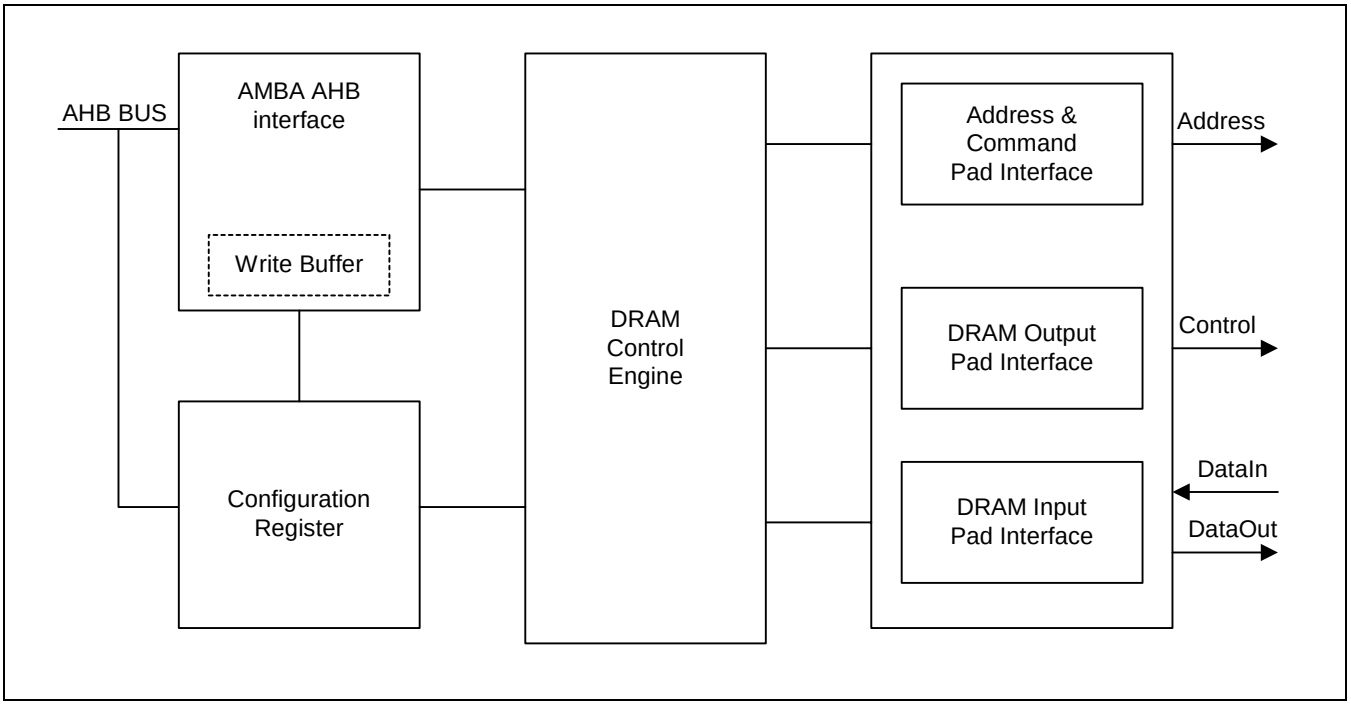


Figure 3-1. DRAM Controller Block Diagram

DRAM INITIALIZATION SEQUENCE

On power-on reset, software must initialize the memory controller and the DRAM connected to the controller. Refer to the DRAM(SDRAM or DDR) data sheet for the start up procedure, and example sequences are given below:

DRAM (SDRAM OR DDR) initialization sequence

1. Wait 200us to allow DRAM power and clock stabilize.
2. Setting the Configuration Register0. This is for MRS and EMRS command to DRAM.
3. Program the configuration register1, and 3 to their normal operation values
4. Program the INIT[1:0] to '01b'. This automatically issues a PALL(pre-charge all) cammand to the DRAM.
5. Write '0xff' into the refresh timer register. This provides a refresh cycle every 255-clock cycles.
6. Wait minimum 2 auto-refresh cycle; DRAM requires minimun 2 auto-refresh cycle.
7. Program the INIT[1:0] of Control Register1 to '10b'. This automatically issues a MRS command to the DRAM
8. Program the normal operational value(auto-refresh ducy cycle) into the refresh timer.
9. Program the INIT[1:0] of Control Register1 to '11b'. This automatically issues a EMRS command to the Mobile DRAM, It's only needed for Mobile DRAM.
10. Program the INIT[1:0] to '00b'. The controller enters the normal mode.
11. The external DRAM is now ready for normal operation.

Note.

In sleep mode wakeup sequence, general reset of system is deasserted after system power stable. in this case, time A generate between reset and power stable. At time A, SDRAM release self-fresh mode. For keep SDRAM data, you must do first self-refresh of SDRAM.

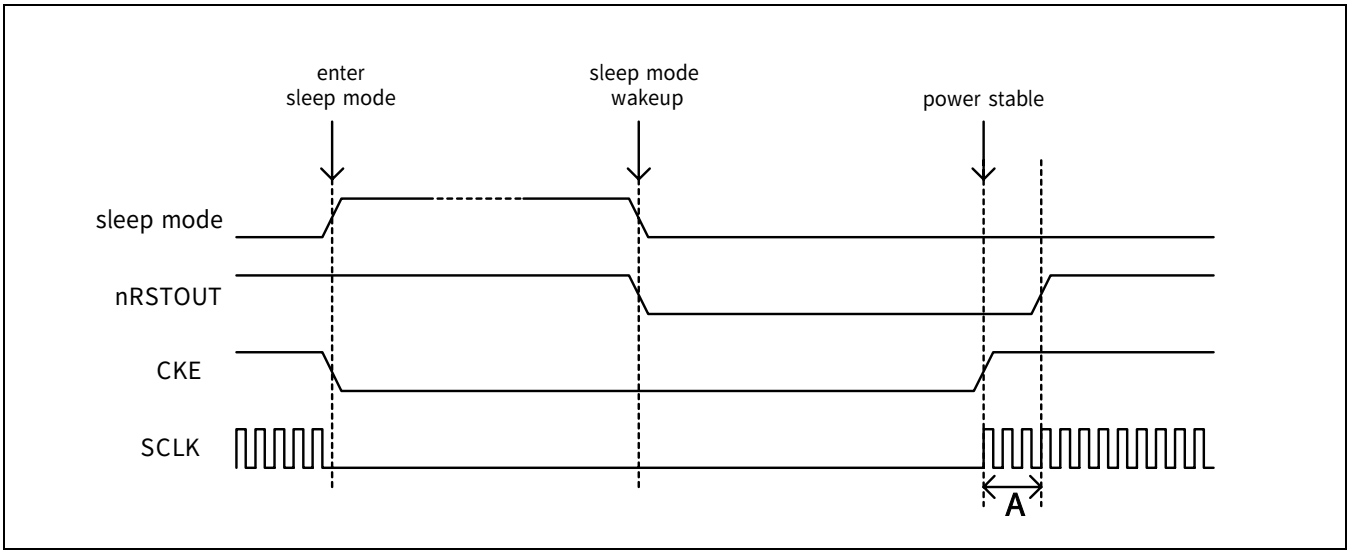


Figure 3-2. Sleep mode wakeup sequence

Table 1 Sleep-mode wake-up time(time A of Figure 3-2)

Boot Mode	Wake-up time
NOR/SROM Memory Boot	70 cycles
NAND Flash Memory Boot (Normal NAND, it has 512Byte/page)	5us(tRST) + 10us(tR)*8(page #) + 8414 cycles For example, the wake time is 9264 cycles, if you use 10MHz clock.
NAND Flash Memory Boot (Advanced NAND, it has 2Kbyte/page)	5us(tRST) + 25us(tR)*2(page #) + 8242 cycles For example, the wake time is 8792 cycles, if you use 10MHz clock.

* Note: refer to NAND flash memory data sheet for more detail about tRST and tR description. tRST and tR can be different according to memory part.

- tRST: Device resetting time

- tR: Data transfer from cell to register

SDRAM/Mobile SDRAM Memory Interface Examples

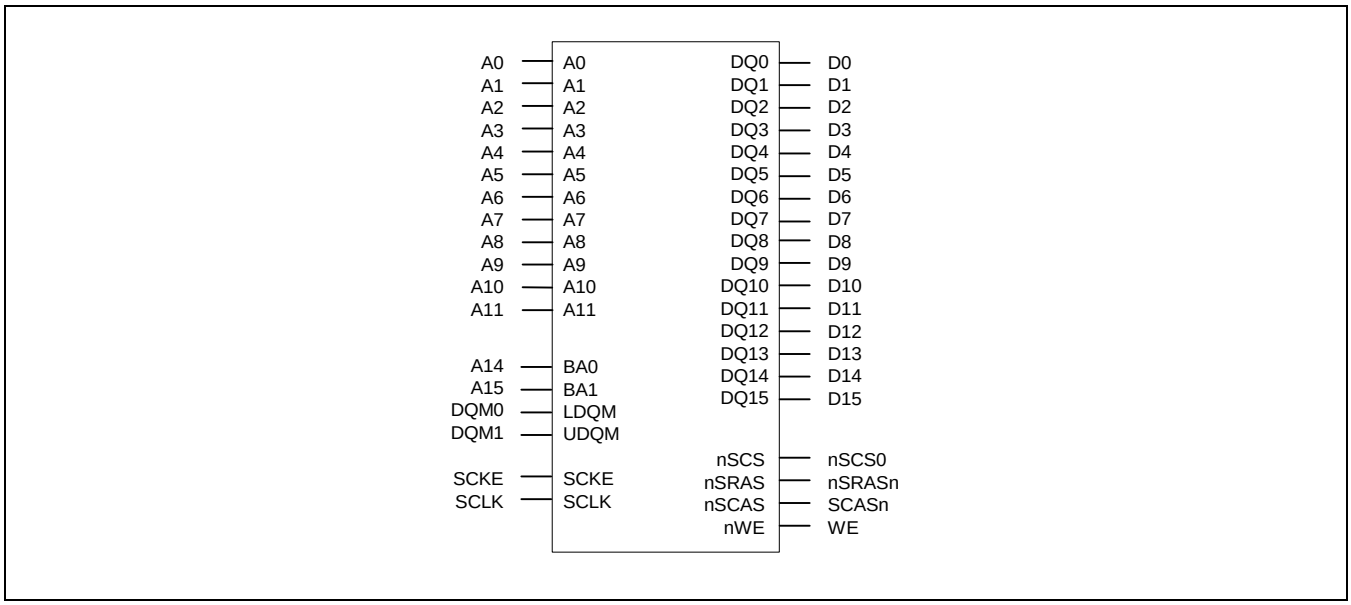


Figure 3-3. Memory Interface with 16-bit SDRAM (4Mx16, 4banks)

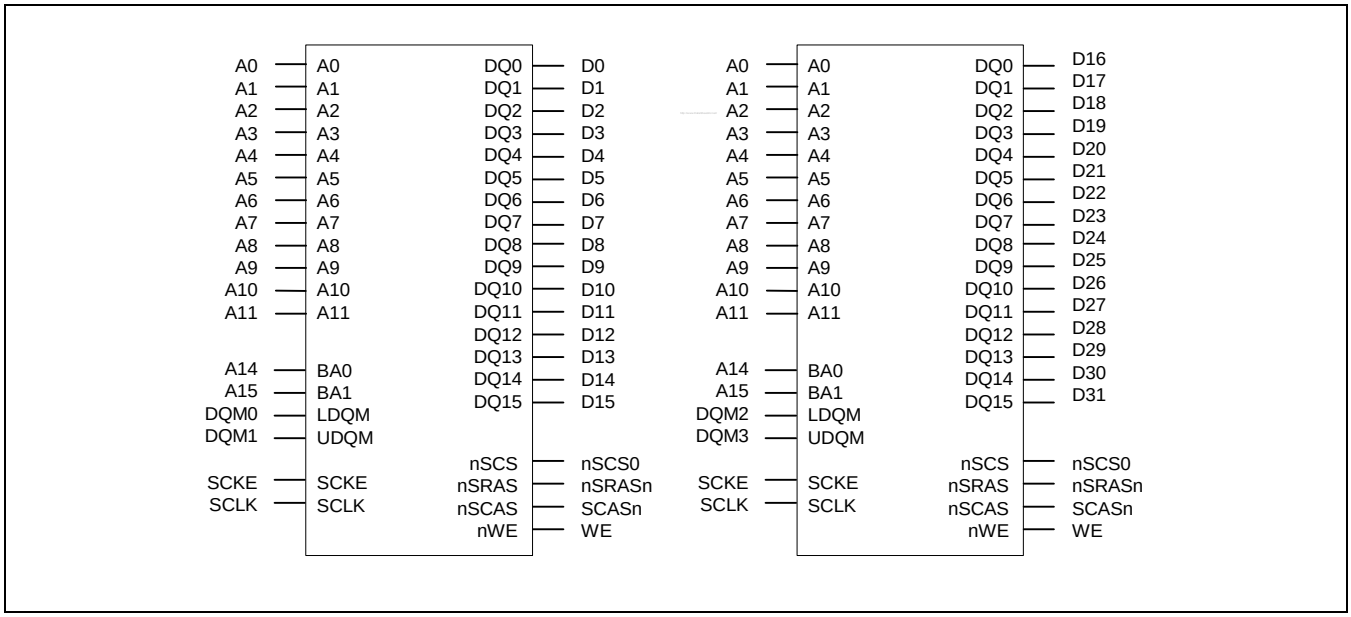


Figure 3-4. Memory Interface with 32-bit SDRAM (4Mx16 * 2ea, 4banks)

DDR/Mobile DDR Memory Interface Examples

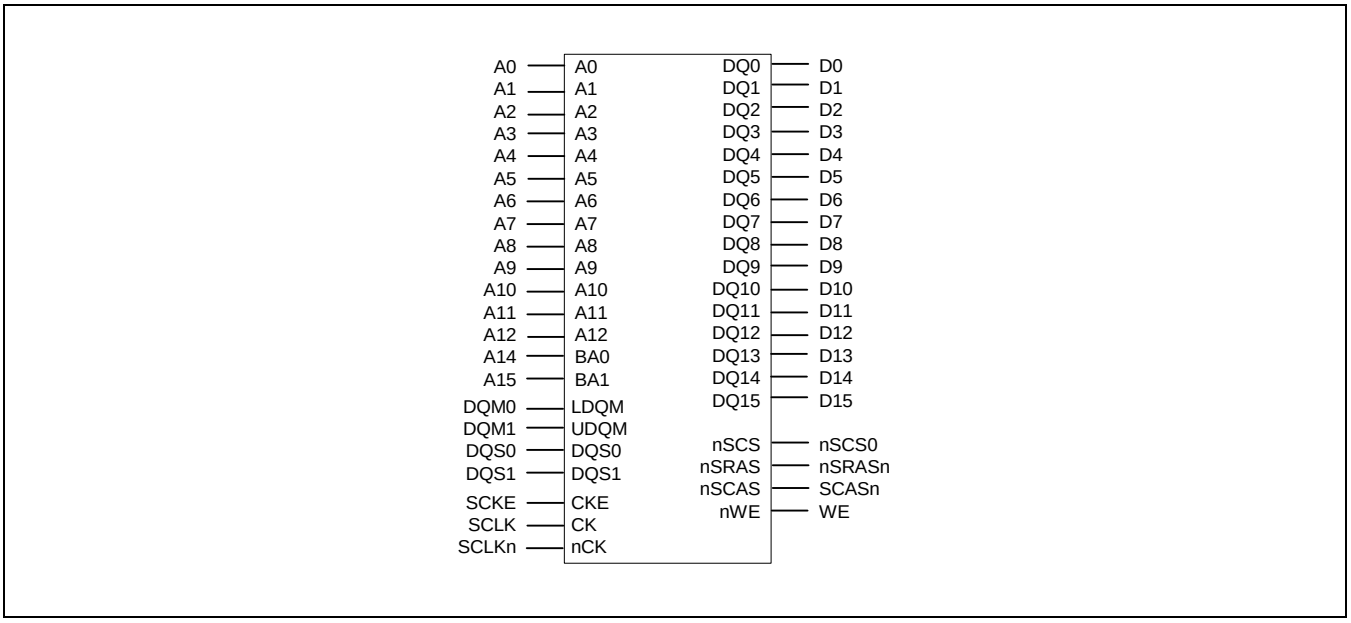


Figure 3-5. Memory Interface with 16-bit DDR/Mobile DDR

Note: DRAM controller supports only 16-bit DDR/Mobile DDR memory device. Specially DQS[1:0] must be connected to between DRAM controller and external memory. In case of 16-bit normal DDR, sometimes it has only 1-bit DQS signal. DRAM controller can't support these kinds of memory.

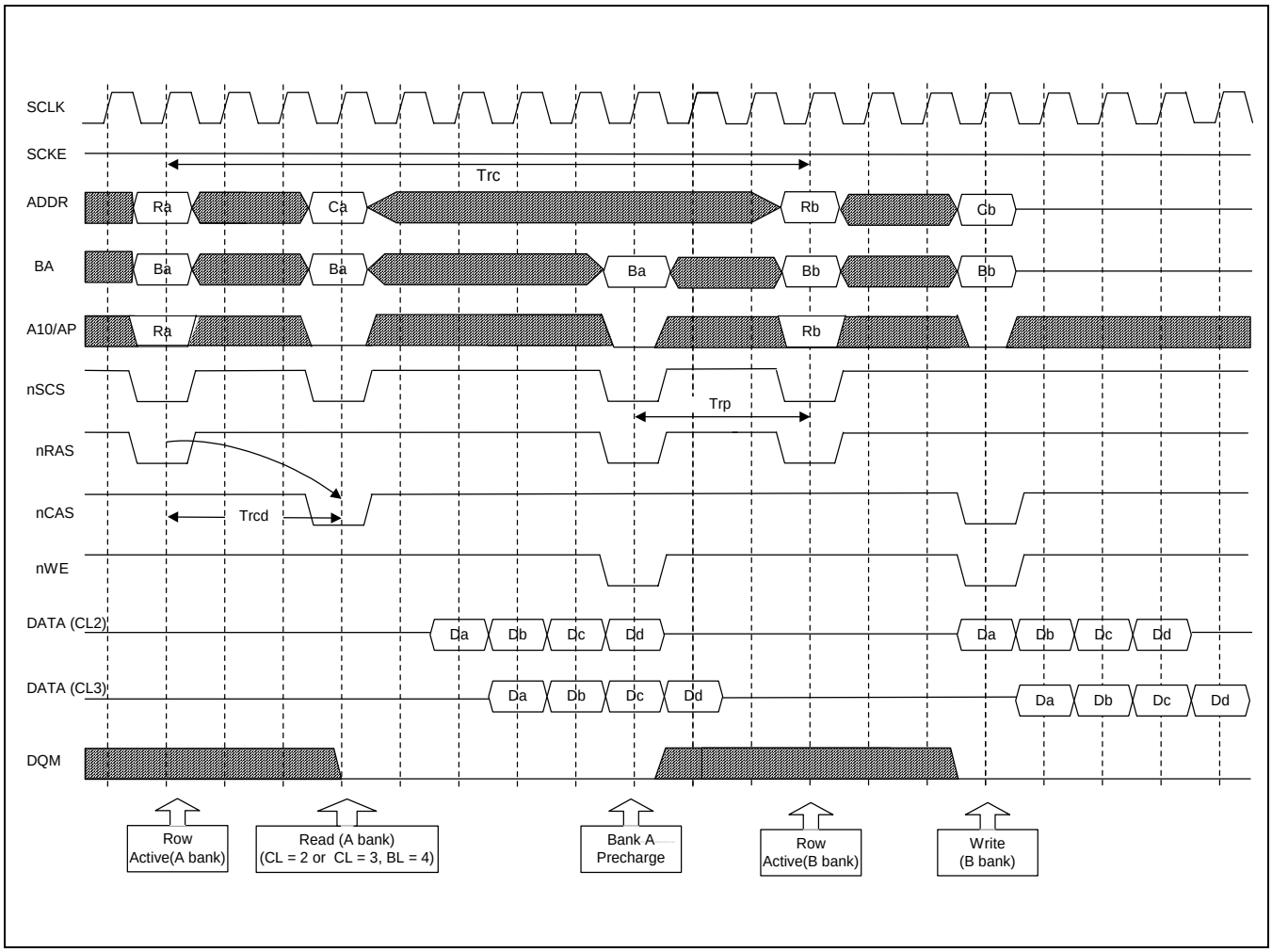


Figure 3-6. SDRAM Timing Diagram

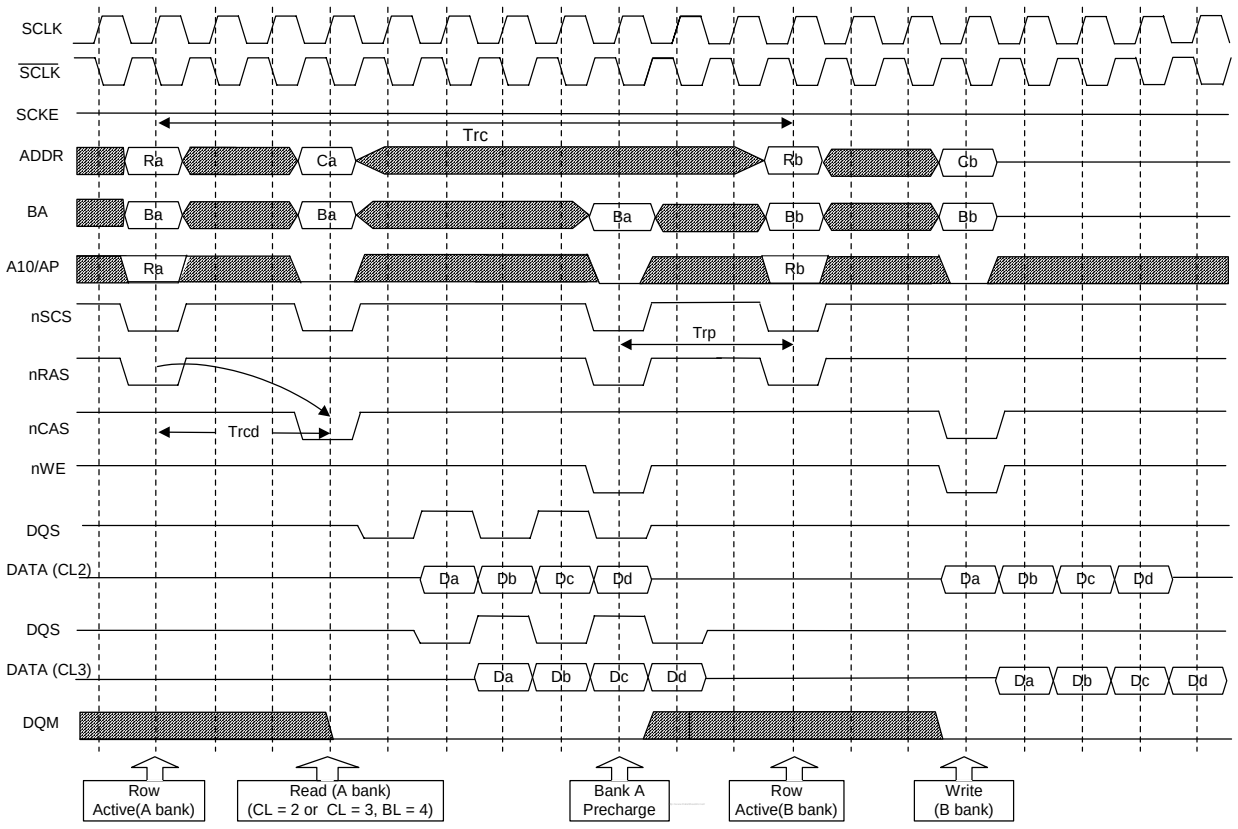


Figure 3-7. DDR/Mobile DDR Timing Diagram

SPECIAL FUNCTION REGISTER

DRAM CONFIGURATION REGISTER

Register	Address	R/W	Description	Reset Value
BANKCFG	0x48000000	R/W	DRAM configuration register	0x0000_000C

BANKCFG	Bit	Description	Initial State
Reserved	[31:19]	Reserved	0x0000
RASBW0	[18:17]	The bit width of RAS (row) address of bank 0 00 = 11-bit 01 = 12-bit 10 = 13-bit 11 = 14-bit	00
Reserved	[16]	Reserved	0
RASBW1	[15:14]	The bit width of RAS (row) address of bank 1 00 = 11-bit 01 = 12-bit 10 = 13-bit 11 = 14-bit	00
Reserved	[13]	Reserved	0
CASBW0	[12:11]	The bit width of CAS (column) address of bank 0 00 = 8-bit 01 = 9-bit 10 = 10-bit 11 = 11-bit	00
Reserved	[10]	Reserved	0
CASBW1	[9:8]	The bit width of CAS (column) address of bank 1 00 = 8-bit 01 = 9-bit 10 = 10-bit 11 = 11-bit	00
ADDRCFG0	[7:6]	Memory address configuration of 00 = {BA, RAS, CAS} 01 = {RAS, BA, CAS} Note: “01” is better that “00” when the memory access is executed consecutively.	0
ADDRCFG1	[5:4]	Memory address configuration 00 = {BA, RAS, CAS} 01 = {RAS, BA, CAS} Note: “01” is better that “00” when the memory access is executed consecutively.	0
MEMCFG	[3:2]	External memory configuration 00 = SDR 01 = MSDR 1x = DDR/Mobile DDR	11
Reserved	[1]	Reserved	0
BW	[0]	Determine external memory data bus width 0 = 32-bit 1 = 16-bit Note: DDR/Mobile DDR interface is supported 16-bit only.	0

NOTE: BANKCFG register should not be written when the DRAM controller is busy. The controller status bit, BUSY in BANKCON register, can be used to check if the controller is idle.

DRAM CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
BANKCON1	0x48000004	R/W	DRAM control register	0x4400_0040

BANKCON1	Bit	Description	Initial State
BUSY	[31]	DRAM controller status bit (read only) 0 = IDLE 1 = BUSY	0
Reserved	[30:28]	Should be set “000”(note)	100
Reserved	[27:26]	Should be “01”	01
Reserved	[25:8]	Reserved	0
BurstStop	[7]	Burst stop control (Only used in DDR interface) 0 = Disable 1 = Enable	0
WBUF	[6]	Write buffer control 0 = Disable 1 = Enable **note:** Disabling the write buffer will flush any stored values to the external DRAM memory. Recommend to set value ‘1’	1
AP	[5]	Auto pre-charge control 0 = Enable auto pre-charge 1 = Disable auto pre-charge Note: If PWRDN is enabled, then AP=0 provides active power down and AP=1 provides pre-charge power down. Note: ‘1’ is better that ‘0’ when the memory access is executed consecutively.	0
PWRDN	[4]	DRAM power down control 0 = Do not use DRAM power down feature 1 = Use DRAM power down feature	0
Reserved	[3:2]	Reserved	00
INIT	[1:0]	DRAM initialization control 00 = Normal operation 01 = Issue PALL command 10 = Issue MRS command 11 = Issue EMRS command	00

Note: There are difference between reset value and recommendation value. Please keep in mind to adopt recommendation value for this field.

DRAM TIMMING CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
BANKCON2	0x48000008	R/W	DRAM timing control register	0x0099_003f

BANKCON2	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
tRAS	[23:20]	Row active time 0000 = 1-clock 0001 = 2-clock 0010 = 3-clock 0011 = 4-clock 0100 = 5-clock 0101 = 6-clock 0110 = 7-clock 0111 = 8-clock 1000 = 9-clock 1001 = 10-clock 1010 = 11-clock 1011 = 12-clock 1100 = 13-clock 1101 = 14-clock 1110 = 15-clock 1111 = 16-clock	1001
tRC	[19:16]	Row cycle time 0000 = 1-clock 0001 = 2-clock 0010 = 3-clock 0011 = 4-clock 0100 = 5-clock 0101 = 6-clock 0110 = 7-clock 0111 = 8-clock 1000 = 9-clock 1001 = 10-clock 1010 = 11-clock 1011 = 12-clock 1100 = 13-clock 1101 = 14-clock 1110 = 15-clock 1111 = 16-clock	1001
Reserved	[15:4]	Reserved	0x000
CAS Latency	[5:4]	CAS Latency Control 00 = Reserved 01 = 1-clock 10 = 2-clock 11 = 3-clock	011
tRCD	[3:2]	RAS to CAS delay 00 = 1-clock 01 = 2-clock 10 = 3-clock 11 = 4-clock	11
tRP	[1:0]	Row pre-charge time 00 = 1-clock 01 = 2-clock 10 = 3-clock 11 = 4-clock	11

DRAM (EXTENDED) MODE REGITER SET REGISTER

Register	Address	R/W	Description	Reset Value
BANKCON3	0x4800000C	R/W	DRAM (E)MRS Register	0x8000_0003

BANKCON3	Bit	Description	Initial State
BA	[31:30]	Bank address for EMRS	10
Reserved	[29:16]	Reserved for EMRS	0x0000
DS	[22:21]	DS(Drive Strength) for EMRS	00
Reserved	[20:19]	Reserved for EMRS	00
PASR	[18:16]	PASR(Partial Array Self Refresh) for EMRS	00
BA	[15:14]	Bank address for MRS	00
Reserved	[13:7]	Reserved for MRS	0x00
CAS Latency	[6:4]	CAS Latency for MRS 00 = Reserved 01 = 1-clock 10 = 2-clock 11 = 3-clock	000
Burst Type	[3]	DRAM Burst Type (Read Only) Only support sequential burst type.	0
Burst Length	[2:0]	DRAM Burst Length (Read Only) This value is determined internally.	011

NOTE: Bit[15:0] is used for MRS command cycle, and Bit[31:16] is for EMRS command cycle. You can program this register as memory type you are using. Each 16-bit exactly map the (E)MRS register bit location. Refer to memory data sheet.

DRAM REFRESH CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
REFRESH	0x48000010	R/W	DRAM refresh control register	0x0000_0020

REFRESH	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0000
REFCYC	[15:0]	DRAM refresh cycle. **Example:** Refresh period is 15.6us, and HCLK is 66MHz. The value of REFCYC is as follows: REFCYC = $15.6 \times 10^{-6} \times 66 \times 10^{6} = 1029$	0x0020

DRAM WRITE BUFFER TIME OUT REGISTER

A write to a enabling write buffer loads the value in the timeout register into timeout down counter of the buffer. When the timeout counter reached 0 the contents of write buffer is flushed to the external DRAM. The down counter is clocked HCLK. Writing a value of 0 in the TIMEOUT register disables the write buffer timeout function.

Register	Address	R/W	Description	Reset Value
TIMEOUT	0x48000014	R/W	Write Buffer Time out control register	0x0000_0000

TIMEOUT	Bit	Description	Initial State
Reserved	[31:16]	Reserved	0x0000
TIMEOUT	[15:0]	Write buffer time-out delay time Recommend to set value 0x0	0x0000

NOTES

4 SSMC

INTRODUCTION

SSMC can support SRAM, OneNAND and Flash devices from BANK 0 to BANK 7.

FEATURE

- Supports asynchronous static memory-mapped devices including RAM, ROM, OneNAND and flash
- Supports synchronous static memory-mapped devices including synchronous burst flash
- Supports asynchronous page mode read operation in non-clocked memory subsystems
- Supports asynchronous burst mode read access to burst mode ROM and flash devices
- Supports synchronous burst mode read, write access to burst mode ROM and flash devices
- Supports 8, 16 and 32-bit data bus
- Address space: Up to 128MB per Bank
- Fixed memory bank start address
- External wait to extend the bus cycle
- Support byte, half-word and word access for external memory
- Programmable wait states, up to 31
- Programmable bus turnaround cycles, up to 15
- Programmable output enable and write enable delays, up to 15
- Configurable size at reset for boot memory bank using external control pins
- Support for interfacing to another memory controller using an External Bus Interface (EBI)
- Multiple memory clock frequencies available, HCLK and HCLK/2
- Eight words, 32-bit, wrapping reads from 16-bit or 32-bit memory
- SMBSTWAIT is synchronous burst wait input that the external device uses to delay a synchronous burst transfer for bank 0. When this signal is not used, it shall be driven to high.
- nWAIT is wait mode input from external memory controller. Active HIGH or active LOW, as programmed in the SSMC Control Registers for each bank.

SPECIAL REGISTERS

BANK IDLE CYCLE CONTROL REGISTERS 0-7

Register	Address	R/W	Description	Reset Value
SMBIDCYR0	0x4F000000	R/W	Bank0 idle cycle control register	0x0000_000F
SMBIDCYR1	0x4F000020	R/W	Bank1 idle cycle control register	0x0000_000F
SMBIDCYR2	0x4F000040	R/W	Bank2 idle cycle control register	0x0000_000F
SMBIDCYR3	0x4F000060	R/W	Bank3 idle cycle control register	0x0000_000F
SMBIDCYR4	0x4F000080	R/W	Bank4 idle cycle control register	0x0000_000F
SMBIDCYR5	0x4F0000A0	R/W	Bank5 idle cycle control register	0x0000_000F
SMBIDCYR6	0x4F0000C0	R/W	Bank6 idle cycle control register	0x0000_000F
SMBIDCYR7	0x4F0000E0	R/W	Bank7 idle cycle control register	0x0000_000F

	Bit	Description	Initial State
	[31:4]	Read undefined. Write as zero.	0x0000_000
IDCY	**[3:0]**	Idle or turnaround cycles. Default to 1111 at reset. This field controls the number of bus turnaround cycles added between read and write accesses to prevent bus contention on the external memory data bus. Turnaround time = IDCY x SMMEMCLK period	0xF

*note : SMMEMCLK is internal Memory Clock for SSMC.

BANK READ WAIT STATE CONTROL REGISTERS 0-7

Register	Address	R/W	Description	Reset Value
SMBWSTRDR0	0x4F000004	R/W	Bank0 read wait state control register	0x0000_001F
SMBWSTRDR1	0x4F000024	R/W	Bank1 read wait state control register	0x0000_001F
SMBWSTRDR2	0x4F000044	R/W	Bank2 read wait state control register	0x0000_001F
SMBWSTRDR3	0x4F000064	R/W	Bank3 read wait state control register	0x0000_001F
SMBWSTRDR4	0x4F000084	R/W	Bank4 read wait state control register	0x0000_001F
SMBWSTRDR5	0x4F0000A4	R/W	Bank5 read wait state control register	0x0000_001F
SMBWSTRDR6	0x4F0000C4	R/W	Bank6 read wait state control register	0x0000_001F
SMBWSTRDR7	0x4F0000E4	R/W	Bank7 read wait state control register	0x0000_001F

	Bit	Description	Initial State
	[31:5]	Read undefined. Write as zero.	0x0000_000
WSTRD	[4:0]	Read wait state. Defaults to 11111 at reset. For SRAM and ROM, the WSTRD field controls the number of wait states for read accesses, and the external wait assertion timing for reads. For burst ROM, the WSTRD field controls the number of wait states for the first read access only. Wait state time = WSTRD x SMMEMCLK period	0x1F

BANK WRITE WAIT STATE CONTROL REGISTERS 0-7

Register	Address	R/W	Description	Reset Value
SMBWSTWRR0	0x4F000008	R/W	Bank0 write wait state control register	0x0000_001F
SMBWSTWRR1	0x4F000028	R/W	Bank1 write wait state control register	0x0000_001F
SMBWSTWRR2	0x4F000048	R/W	Bank2 write wait state control register	0x0000_001F
SMBWSTWRR3	0x4F000068	R/W	Bank3 write wait state control register	0x0000_001F
SMBWSTWRR4	0x4F000088	R/W	Bank4 write wait state control register	0x0000_001F
SMBWSTWRR5	0x4F0000A8	R/W	Bank5 write wait state control register	0x0000_001F
SMBWSTWRR6	0x4F0000C8	R/W	Bank6 write wait state control register	0x0000_001F
SMBWSTWRR7	0x4F0000E8	R/W	Bank7 write wait state control register	0x0000_001F

	Bit	Description	Initial State
	[31:5]	Read undefined. Write as zero.	0x0000_000
WSTWR	[4:0]	Write wait state. Defaults to 11111 at reset. For SRAM , the WSTWR field controls the number of wait states for write accesses, and the external wait assertion timing for writes. Wait state time = WSTWR x SMMEMCLK period WSTWR does not apply to read-only devices such as ROM.	0x1F

BANK OUTPUT ENABLE ASSERTION DELAY CONTROL REGISTERS 0-7

Register	Address	R/W	Description	Reset Value
SMBWSTOENR0	0x4F00000C	R/W	Bank0 output enable assertion delay control register	0x0000_0000
SMBWSTOENR1	0x4F00002C	R/W	Bank1 output enable assertion delay control register	0x0000_0000
SMBWSTOENR2	0x4F00004C	R/W	Bank2 output enable assertion delay control register	0x0000_0000
SMBWSTOENR3	0x4F00006C	R/W	Bank3 output enable assertion delay control register	0x0000_0000
SMBWSTOENR4	0x4F00008C	R/W	Bank4 output enable assertion delay control register	0x0000_0000
SMBWSTOENR5	0x4F0000AC	R/W	Bank5 output enable assertion delay control register	0x0000_0000
SMBWSTOENR6	0x4F0000CC	R/W	Bank6 output enable assertion delay control register	0x0000_0000
SMBWSTOENR7	0x4F0000EC	R/W	Bank7 output enable assertion delay control register	0x0000_0000

	Bit	Description	Initial State
	[31:4]	Read undefined. Write as zero.	0x0000_000
WSTOEN	[3:0]	Output enable assertion delay from chip select assertion. Default to 0000 at reset	0x0

BANK WRITE ENABLE ASSERTION DELAY CONTROL REGISTERS 0-7

Register	Address	R/W	Description	Reset Value
SMBWSTWENR0	0x4F000010	R/W	Bank0 write enable assertion delay control register	0x0000_0001
SMBWSTWENR1	0x4F000030	R/W	Bank1 write enable assertion delay control register	0x0000_0001
SMBWSTWENR2	0x4F000050	R/W	Bank2 write enable assertion delay control register	0x0000_0001
SMBWSTWENR3	0x4F000070	R/W	Bank3 write enable assertion delay control register	0x0000_0001
SMBWSTWENR4	0x4F000090	R/W	Bank4 write enable assertion delay control register	0x0000_0001
SMBWSTWENR5	0x4F0000B0	R/W	Bank5 write enable assertion delay control register	0x0000_0001
SMBWSTWENR6	0x4F0000D0	R/W	Bank6 write enable assertion delay control register	0x0000_0001
SMBWSTWENR7	0x4F0000F0	R/W	Bank7 write enable assertion delay control register	0x0000_0001

	Bit	Description	Initial State
	[31:4]	Read undefined. Write as zero.	0x0000_000
WSTWEN	[3:0]	Write enable assertion delay from chip select assertion. Default to 0001 at reset	0x1

BANK CONTROL REGISTERS 0-7

Register	Address	R/W	Description	Reset Value
SMBCR0	0x4F000014	R/W	Bank0 control register	0x0030_3020
SMBCR1	0x4F000034	R/W	Bank1 control register	0x0030_3000
SMBCR2	0x4F000054	R/W	Bank2 control register	0x0030_3010
SMBCR3	0x4F000074	R/W	Bank3 control register	0x0030_3000
SMBCR4	0x4F000094	R/W	Bank4 control register	0x0030_3020
SMBCR5	0x4F0000B4	R/W	Bank5 control register	0x0030_3020
SMBCR6	0x4F0000D4	R/W	Bank6 control register	0x0030_3010
SMBCR7	0x4F0000F4	R/W	Bank7 control register	0x0030_3000

	Bit	Description	Initial State
	[31:22]	Read undefined. Write as zero.	0x000
	[21]	not available(should be high)	0x1
AddrValidWriteEn	[20]	Controls the behavior of the signal **SMAVD** during write operations: 0 Signal always HIGH 1 Signal active for asynchronous and synchronous write accesses (default).	0x1
BurstLenWrite	[19:18]	Burst transfer length. Sets the number of sequential transfers that the burst device supports for a write: 00 4-transfer burst (default) 01 8-transfer burst 10 Reserved 11 Continuous burst (synchronous only).	0x0
SyncWriteDev	[17]	Synchronous access capable device connected. Access the device using synchronous accesses for writes: 0 Asynchronous device (default). 1 Synchronous device.	0x0
BMWrite	[16]	Burst mode write: 0 Nonburst writes to memory devices (default at reset) 1 Burst mode writes to memory devices.	0x0
DRnOWE	[15]	0 Get the delay between nCS signal and nOE/nWE signal. nOE : 1.5 cycle, nWE : 2 cycle of SMMEMCLK. (default) 1 No delay Note: The only use for Bank1, Bank3. and if DRnCS is set “1”, it must be set “1”.	0x0
WrapRead	[14]	Enables the wrapping burst feature from external memory. This is to support eight word wrapping bursts only. Only valid for burst 16 from 16-bit external memory and burst 8 from 32-bit external memory. 0 Disabled (default). 1 Enabled. Note The SSMC supports wrapping reads, but does not support wrapping writes.	0x0

	[13]	not available (should be high)	0x1
AddrValidReadEn	[12]	Controls the behavior of the signal SMAVD during read operations: 0 Signal always HIGH. 1 Signal active for asynchronous and synchronous read accesses (default).	0x1
BurstLenRead	[11:10]	Burst transfer length. Sets the number of sequential transfers that the burst device supports for a read: 00 4-transfer burst. 01 8-transfer burst. 10 16-transfer burst. 11 Continuous burst (synchronous only).	0x0
SyncReadDev	[9]	Synchronous access capable device connected. Access the device using synchronous accesses for reads: 0 Asynchronous device (default). 1 Synchronous device.	0x0
BMRead	[8]	Burst mode read and asynchronous page mode: 0 Nonburst reads from memory devices (default at reset). 1 Burst mode reads from memory devices.	0x0
DRnCS	[7]	0 Get the 1 SMMEMCLK cycle delay between ADDR signal and nCS signal.(default) 1 No delay Note: The only use for Bank1, Bank3.	0x0
SMBLSPOL	[6]	Polarity of signal nBE: 0 Signal is active LOW (default). 1 Signal is active HIGH. Note: The value of Bank0 always remains 0	0x0
MW	[5:4]	Memory width: 00 8-bit. 01 16-bit. 10 32-bit. 11 Reserved. Defaults to different values at reset for each bank This value of Bank0 changes by OM configuration.	0x1

	Bit	Description	Initial State
WP	[3]	Write protect: 0 No write protection, for example, SRAM or write enabled Flash (default at reset). 1 Device is write protected, for example, ROM, burst ROM, read-only Flash, or SRAM.	0x0
WaitEn	[2]	External memory controller wait signal enable: 0 The SSMC is not controlled by the external wait signal (default at reset). 1 The SSMC looks for the external wait input signal, nWAIT.	0x0
WaitPol	[1]	Polarity of the external wait input for activation: 0 The nWAIT signal is active LOW (default at reset). 1 The nWAIT signal is active HIGH.	0x0
RBLE	[0]	Read byte lane enable: 0 nBE[3:0] all deasserted HIGH during system reads from external memory. This is for 8-bit devices where the byte lane enable is connected to the write enable pin so you must deassert it during a read (default at reset). The nBE signals act as write enables in this configuration. 1 nBE[3:0] all asserted LOW during system reads from external memory. This is for 16 or 32-bit devices where you use the separate write enable signal, and you must hold the byte lane selects asserted during a read. The nWE signal acts as the write enable in this configuration.	0x0

BANK STATUS REGISTERS 0-7

Register	Address	R/W	Description	Reset Value
SMBSR0	0x4F000018	R/W	Bank0 status register	0x0000_0000
SMBSR1	0x4F000038	R/W	Bank1 status register	0x0000_0000
SMBSR2	0x4F000058	R/W	Bank2 status register	0x0000_0000
SMBSR3	0x4F000078	R/W	Bank3 status register	0x0000_0000
SMBSR4	0x4F000098	R/W	Bank4 status register	0x0000_0000
SMBSR5	0x4F0000B8	R/W	Bank5 status register	0x0000_0000
SMBSR6	0x4F0000D8	R/W	Bank6 status register	0x0000_0000
SMBSR7	0x4F0000F8	R/W	Bank7 status register	0x0000_0000

	Bit	Description	Initial State
	[31:1]	Read undefined. Write as zero.	0x0000_000
WaitToutErr	[0]	External wait timeout error flag. Reading this bit: 0 No Error (default at reset). 1 External wait timeout error. Writing this bit: 0 Has no effect. 1 Clears the write protect error status flag.	0x0

BANK BURST READ WAIT DELAY CONTROL REGISTERS 0-7

Register	Address	R/W	Description	Reset Value
SMBWSTBRDR0	0x4F00001C	R/W	Bank0 burst read wait delay control register	0x0000_001F
SMBWSTBRDR1	0x4F00003C	R/W	Bank1 burst read wait delay control register	0x0000_001F
SMBWSTBRDR2	0x4F00005C	R/W	Bank2 burst read wait delay control register	0x0000_001F
SMBWSTBRDR3	0x4F00007C	R/W	Bank3 burst read wait delay control register	0x0000_001F
SMBWSTBRDR4	0x4F00009C	R/W	Bank4 burst read wait delay control register	0x0000_001F
SMBWSTBRDR5	0x4F0000BC	R/W	Bank5 burst read wait delay control register	0x0000_001F
SMBWSTBRDR6	0x4F0000DC	R/W	Bank6 burst read wait delay control register	0x0000_001F
SMBWSTBRDR7	0x4F0000FC	R/W	Bank7 burst read wait delay control register	0x0000_001F

	Bit	Description	Initial State
	[31:5]	Read undefined. Write as zero.	0x0000_00
WSTBRD	[4:0]	Burst read wait state. Defaults to 1111 at reset. For burst devices, the WSTBRD field controls the number of wait states for the burst read accesses after the first read. Wait state time = WSTBRD x SMMEMCLK period WSTBRD does not apply to nonburst devices.	0x1F

SSMC STATUS REGISTER

Register	Address	R/W	Description	Reset Value
SSMCSR	0x4F000200	R	SSMC status register	0x0000_0000

	Bit	Description	Initial State
	[31:1]	Read undefined.	0x0000_000
WaitStatus	[0]	External wait status, read: 0 nWAIT deasserted. 1 nWAIT asserted. After an externally waited transfer that was terminated early, this bit value can detect when nWAIT is deasserted. At all other times, this bit reads zero.	0x0

SSMCC CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
SSMCCR	0x4F000204	R/W	SSMC control register	0x0000_0003

	Bit	Description	Initial State
	[31:3]	Read undefined. Write as zero.	0x0000_000
MemClkRatio	[2:1]	Defines the ratio of SMMEMCLK to HCLK: 00 SMMEMCLK = HCLK . 01 SMMEMCLK = HCLK/2.(default) 10 Reserved(should be zero) 11 Reserved.	0x1
SMClockEn	[0]	SMCLK enable: 0 Clock only active during memory accesses. 1 Clock always running. Clock stopping saves power by stopping SMCLK when it is not required. If clock stopping is enabled before the memory access, SSMC controller stops SMCLK on the following conditions: • asynchronous read access to asynchronous memory • asynchronous write access to asynchronous memory • asynchronous read access to synchronous memory • asynchronous write access to synchronous memory	0x1

ASYNCHRONOUS READ

The delay between the assertion of the chip select and the output enable is programmable from 0-15 cycles using the WSTOEN bits of the Bank Control Registers. In the External Wait enabled mode, the timing of the transfer(controlled by nWAIT) is not known, so nOEN is asserted along with nGCS and the WSTOEN delay value is not used.

Figure 4-1 shows an external memory read transfer with two output enable delay states, WSTOEN = 2, and two wait states, WSTRD = 2. Four AHB wait states are inserted during the transfer, two for the standard read, and additional two because of the programmed wait states added.

The SMAVD signal might be required for synchronous static memory devices when you use it in asynchronous mode. You can disable this using the AddrValidReadEn bit in the SMBCRx register. This bit defaults to being set(enable) to enable a system to boot from synchronous memory. You can then clear it if you do not require it. When disabled, the signal is driven HIGH continuously.

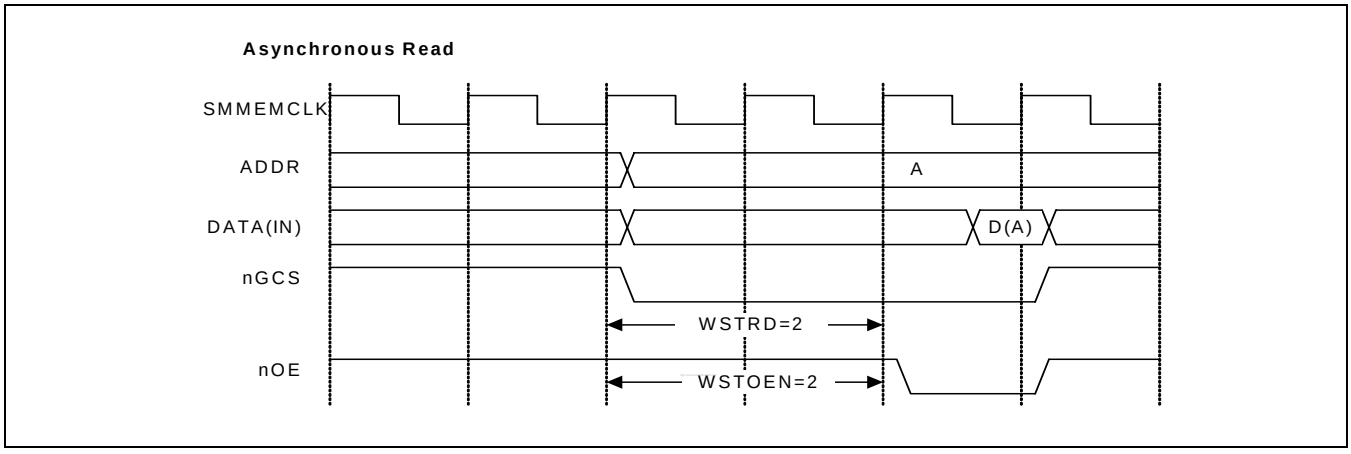


Figure 4-1. External memory two output enable delay state read

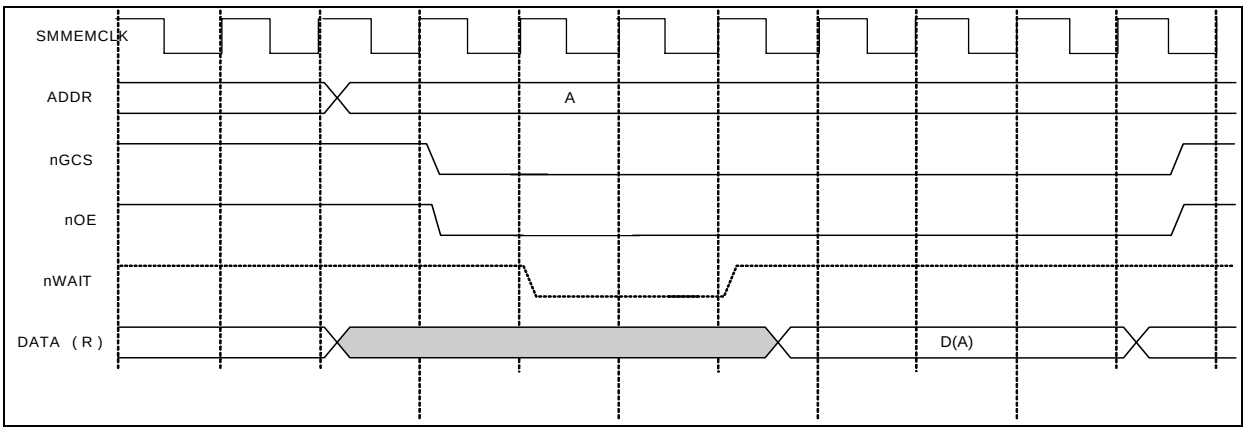


Figure 4-2. Read Timing diagram (DRnCS = 0, DRnOWE = 1)

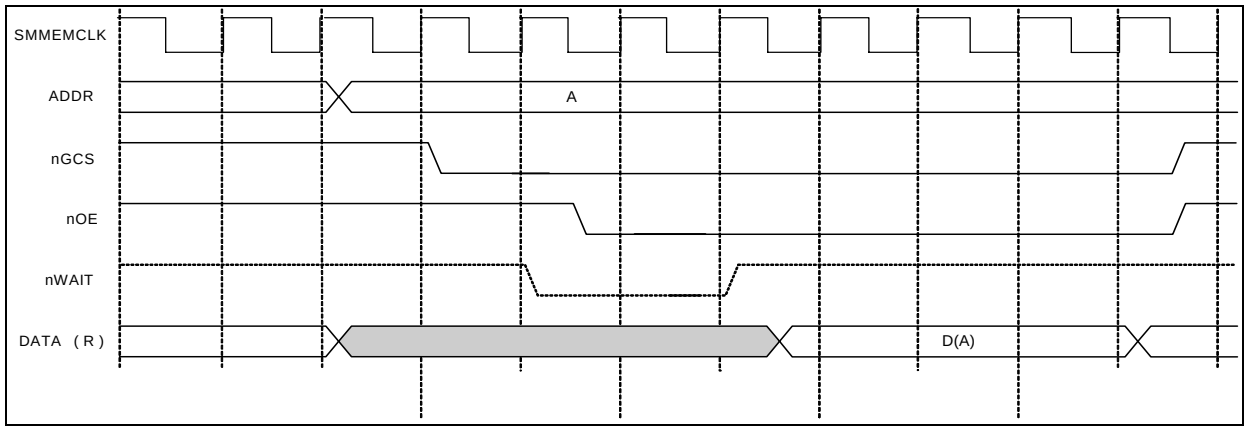


Figure 4-3. Read Timing diagram (DRnCS = 0, DRnOWE = 0)

ASYNCHRONOUS BURST READ

The SSMC supports sequential access asynchronous burst reads to four or eight consecutive locations in 8, 16, or 32-bit memories, as set using the BurstLenRead bits of the Control Register SMBCRx. Burst mode is enabled by setting the Burst Mode bits, BMRead or BMWrite, in the Control register. This feature supports burst mode devices and increases the bandwidth by using a reduced access time(that you can configure) for the sequential reads, WSTBRD, following the first read, WSTRD. The chip select and output enable lines are held during the burst, and only the address changes between subsequent accesses. At the end of the burst the chip select and output enable lines are deasserted together.

Asynchronous page mode read operation is supported. This is enabled by setting the BMRead bit and by setting the burst length using BurstLenRead in the SMBCRx register. Sequential bursts of up to four or eight beats are the only type of access supported for page mode operation.

Figure 4-4 shows an external memory burst read transfer with two initial wait states, and one sequential wait state. The first read has four AHB wait states inserted, and all additional sequential transfers have only one AHB wait state.

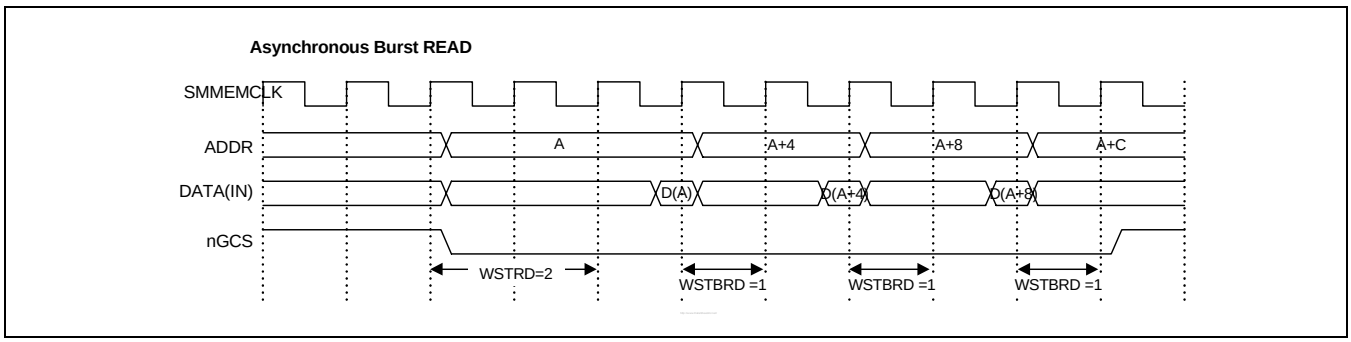


Figure 4-4. External burst ROM with WSTRD=2 and WSTBRD=1 fixed length burst read

SYNCHRONOUS READ/SYNCHRONOUS BURST READ

Single synchronous read operations have the same control signal timing as an asynchronous read operation, but with different timing requirements for setup and hold relative to the clock. Because the output signals of the SSMC are generated internally from clocked logic, the timing for single synchronous reads is the same as for asynchronous reads.

Synchronous burst read transfers are performed differently to asynchronous burst reads, because of the internal address incrementing performed by synchronous burst devices. The ADDR outputs are held with the initial address value, and the SMAVD output is asserted during the transfer to indicate that the address is valid.

Four, eight, or continuous synchronous burst lengths are supported, and are controlled by the BurstLenRead bits in the Bank Control Register SMBCRx when the SyncEnRead and BMRead bits indicate that the device supports synchronous bursts.

Figure shows continuous burst read transfers, where WSTRD = 3 and WSTBRD = 0.

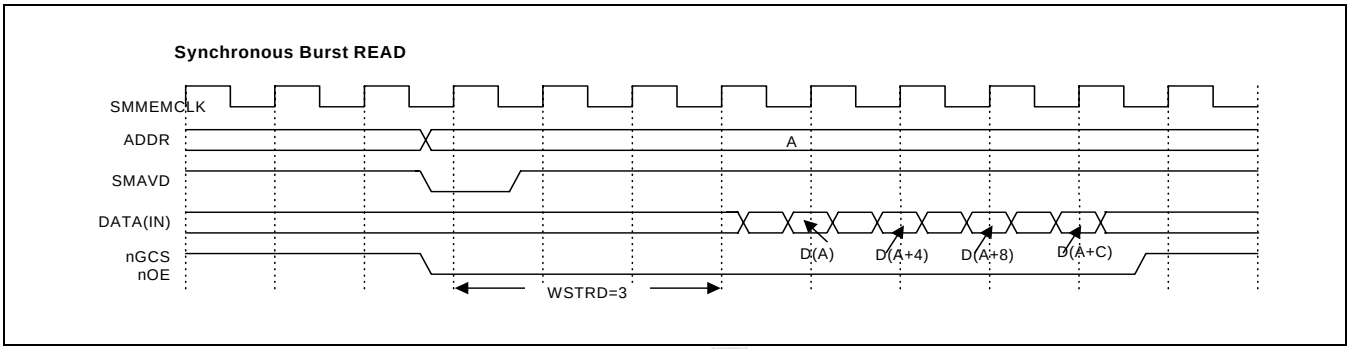


Figure 4-5. External synchronous fixed length four transfer burst read

ASYNCHRONOUS WRITE

You can program the delay between the assertion of the chip select and the write enable from 0-15 cycles using the WSTWEN bits of the Bank Write Enable Assertion Delay Control Register, SMBWSTWENRx. This reduces the power consumption for memories. The write enable is asserted on the falling edge of SMMEMCLK, half a clock after the assertion of chip select.

For most asynchronous memory devices an SMMEMCLK cycle is required before the assertion of nWE otherwise there is the hazard that nCS changes after nWE. You can add extra cycles before nWE is asserted using the WSTWEN bits in the Bank Write Enable Assertion Delay Control Registers. For example, setting WSTWR=WSTWEN=1 extends the transfer by one cycle and delays the assertion of nWE by one cycle.

The Write enable is always deasserted half a cycle before the chip select, at the end of the transfer. nBE has the same timing as nWE for writes to 8-bit devices that use the byte lane selects instead of the write enables.

The WSTWEN programmed value must be equal to , or less than the WSTWR programmed value otherwise an invalid access sequence is generated. The access is timed by the WSTWR value and not by the WSTWEN value.

You might require the SMAVD signal for synchronous static memory devices when you use it in asynchronous mode. You can disable it using the AddrValidWriteEn bit in the SMBCRx Register. This bit defaults to being set(enable). You can then clear it if you do not require it. When you disable it, the signal is driven HIGH continuously.

Figure 4-6 shows a single external memory write transfer with two write enable delay states, WSTEN=2, and two wait states, WSTWR=2. A single AHB wait state is inserted.

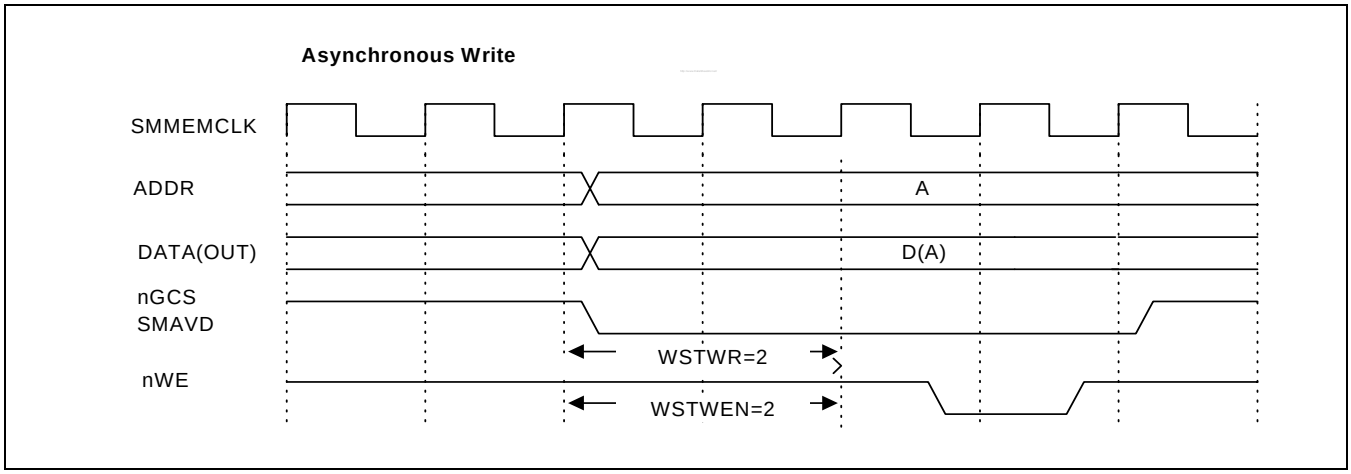


Figure 4-6. External memory two write enable delay state write

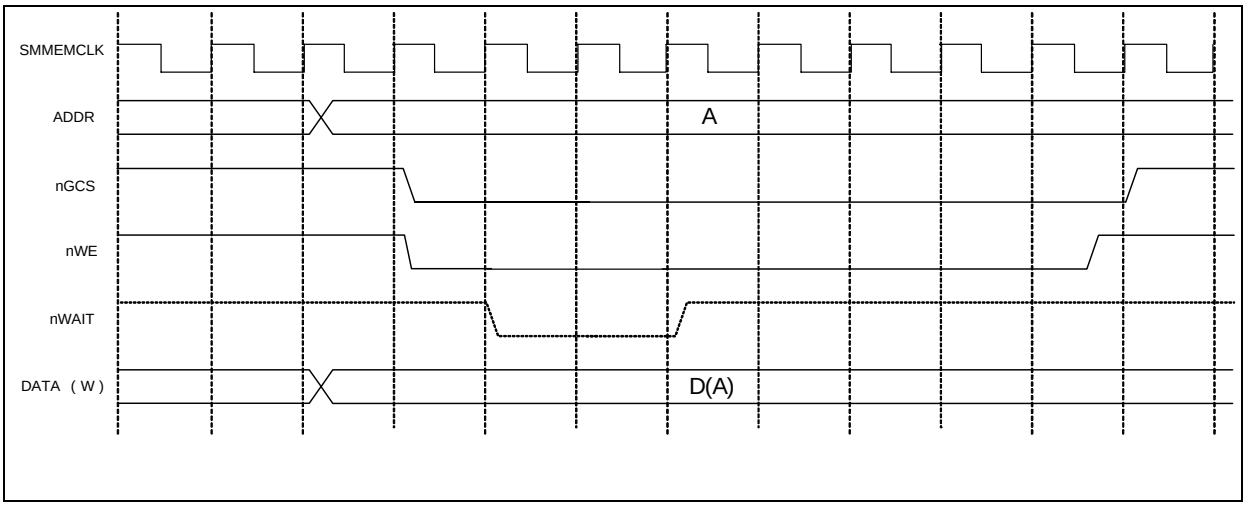


Figure 4-7. Write Timing diagram (DRnCS = 0, DRnOWE = 1)

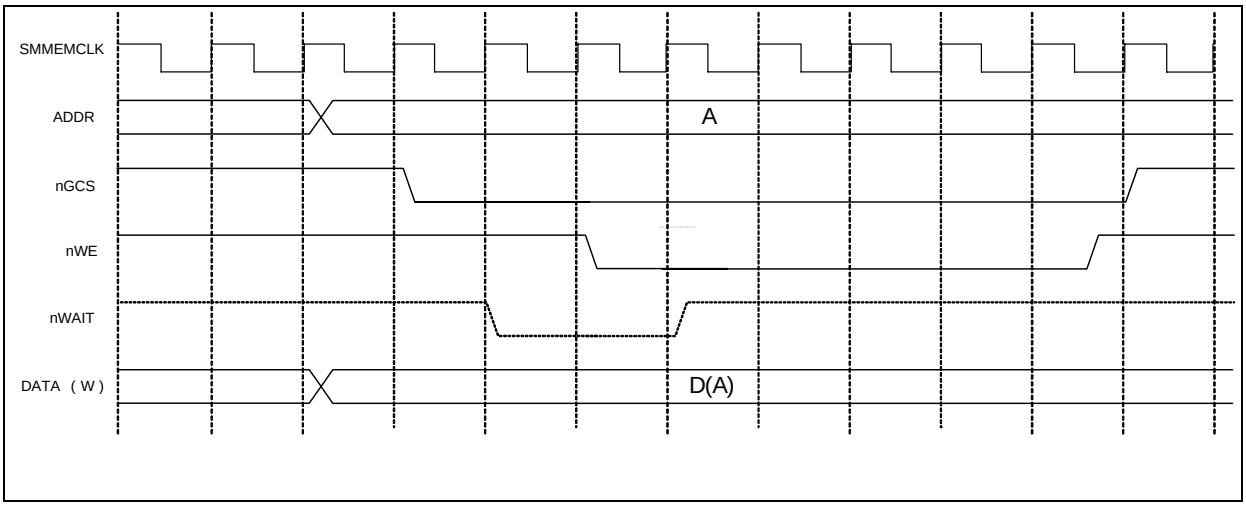


Figure 4-8. Write Timing diagram (DRnCS = 0, DRnOWE = 0)

SYNCHRONOUS WRITE/ SYNCHRONOUS BURST WRITE

Figure 4-9 shows an example synchronous write operation. In this example the signal SMAVD provides a one-cycle pulse. This behavior is enabled by setting the SyncWriteDev bit in the SMBCRx register. You must also set the AddrValidWriteEn bit for synchronous write.

The signal nWE is only active for one cycle. This is active at the start of the transfer unless it is delayed using the control bits WSTWEN to delay it.

Synchronous burst writes are supported by the SSMC. There is no write buffer so you must delay the AHB transfer to enable the data to be output onto the DATA bus. You can control the write in the same way as reads using the bits AddrValidWriteEn, BurstLenWrite, SyncEnWrite, and BMWrite contained in the Bank Control Register, SMCRx.

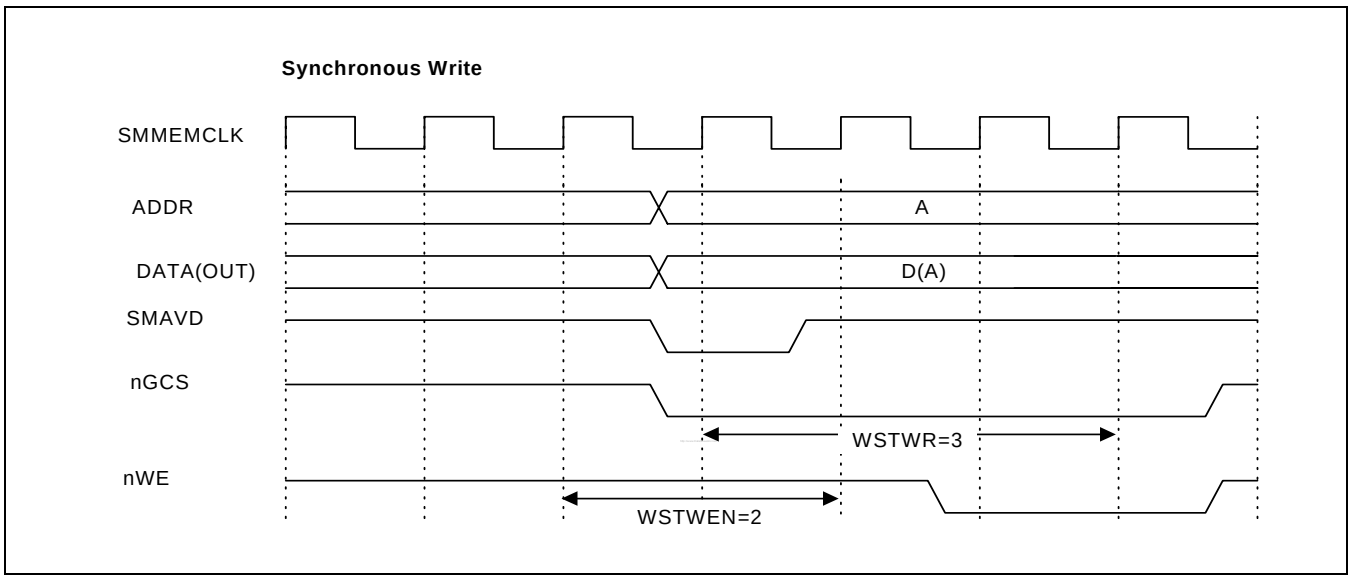


Figure 4-9. Synchronous two wait state write

BUS TURNAROUND

You can configure the SSMC for each memory bank to use external bus turnaround cycles between read and write memory accesses. You can program the IDCY field for up to 15 bus turnaround wait states. This avoids bus contention on the external memory data bus. Bus turnaround cycles are generated between external bus transfers as follows:

read-to-read, to different memory banks

read-to-write to the same memory banks

read-to-write to different memory banks

Figure 4-10 shows a zero wait asynchronous read followed by two zero wait asynchronous writes with two turnaround cycles added. The standard minimum of two AHB wait states are added to the read transfer, one is added to the first write, as for any read-write transfer sequence, and three are added to the second write because of insertion of the two turnaround cycles that are only generated after the first write transfer has been detected, and the standard one wait state added when a write transfer is buffered.

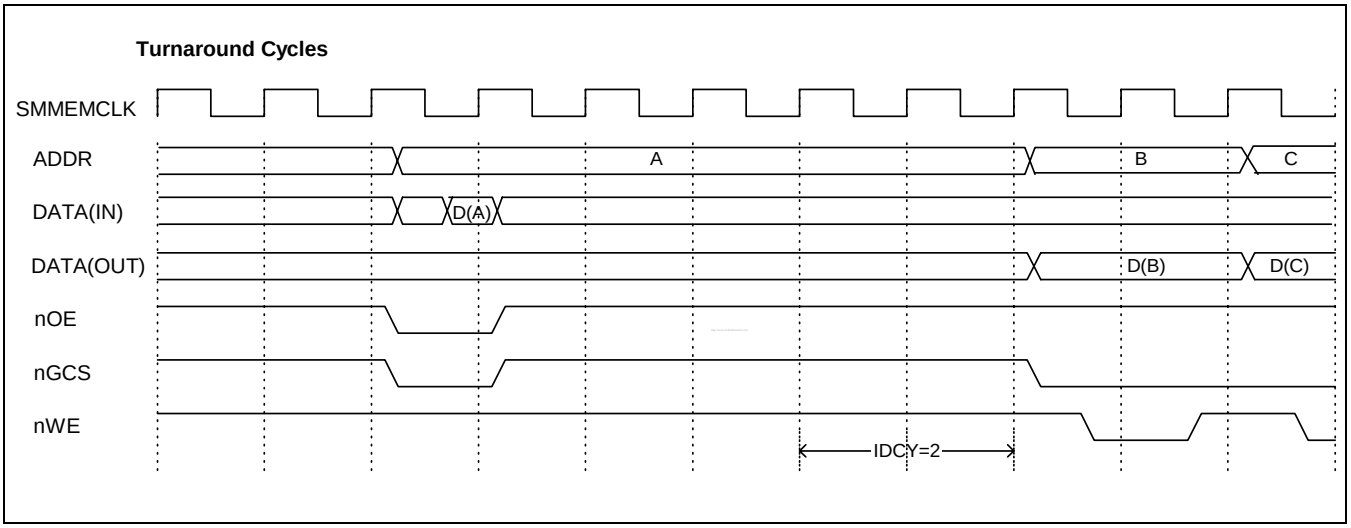


Figure 4-10. Read, then writes (WSTRD=WSTWR=0), two turnaround cycles (IDCY=2)

NOTES

5 NAND FLASH CONTROLLER

OVERVIEW

In recent times, NOR flash memory gets high in price while an SDRAM and a NAND flash memory get moderate, motivating some users to execute the boot code on a NAND flash and execute the main code on an SDRAM.

S3C2413X boot code can be executed on an external NAND flash memory. In order to support NAND flash boot loader, the S3C2413X is equipped with an internal SRAM buffer called 'Steppingstone'. When booting, the first 4 KBytes of the NAND flash memory will be loaded into Steppingstone and the boot code loaded into Steppingstone will be executed.

Generally, the boot code will copy NAND flash content to SDRAM. Using hardware ECC, the NAND flash data validity will be checked. Upon the completion of the copy, the main program will be executed on the SDRAM.

FEATURES

1. Auto boot: The boot code is transferred into 4-kbytes Steppingstone during reset. After the transfer, the boot code will be executed on the Steppingstone.
2. NAND Flash memory I/F: Support 256Words, 512Bytes, 1KWords and 2KBytes Page.
3. Software mode: User can directly access NAND flash memory, *for example this feature can be used in read/erase/program NAND flash memory*.
4. Interface: 8 / 16-bit NAND flash memory interface bus.
5. Hardware ECC generation, detection and indication (Software correction).
6. Support both SLC and MLC NAND flash memory : 1-bit ECC for SLC and 4-bit ECC for MLC NAND flash.
7. SFR I/F: Support Little Endian Mode, Byte/half word/word access to Data and ECC Data register, and Word access to other registers
8. SteppingStone I/F: Support Little/Big Endian, Byte/half word/word access.
9. The Steppingstone 4-KB internal SRAM buffer can be used for another purpose after NAND flash booting.

BLOCK DIAGRAM

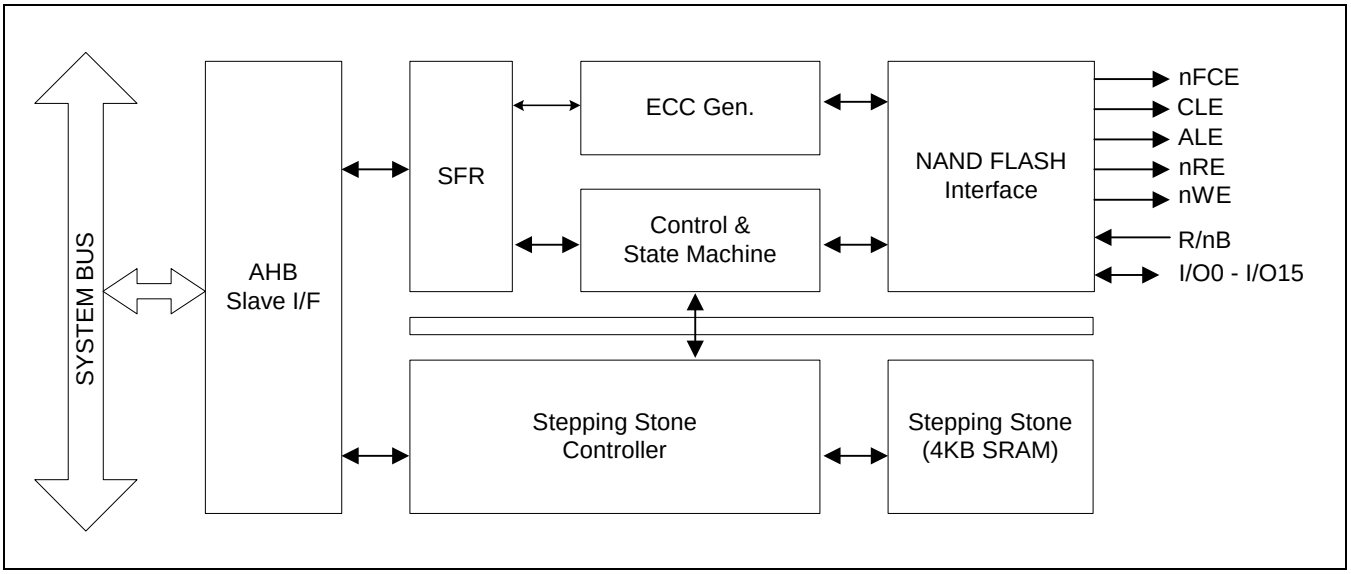


Figure 5-1. NAND Flash Controller Block Diagram

BOOT LOADER FUNCTION

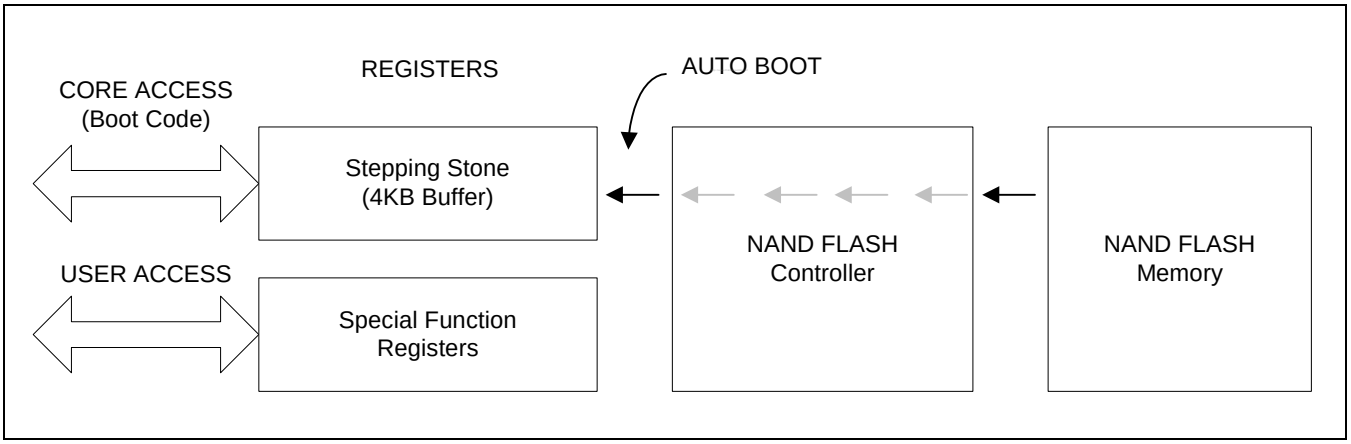


Figure 5-2. NAND Flash Controller Boot Loader Block Diagram

During reset, Nand flash controller will get information about connected NAND flash through Pin status of XOM – refer to **PIN CONFIGURATION**), After power-on or system reset is occurred, the NAND Flash controller load automatically the 4-KBytes boot loader codes. After loading the boot loader codes, the boot loader code in steppingstone is executed.

NOTE:

During the auto boot, the ECC is not checked. So, the first 4-KB of NAND flash should have no bit error.

PIN CONFIGURATION TABLE

OM[3:0	AdvFlash	PageSize	AddrCycle	BusWidth
0b0100	0: Normal NAND	1: 512 byte	0: 3 cycle	0: 8-bit data bus
0b1100	0: Normal NAND	1: 512 byte	1: 4 cycle	0: 8-bit data bus
0b0110	1: Advance NAND	1: 2-Kbyte	0: 4 cycle	0: 8-bit data bus
0b1110	1: Advance NAND	1: 2-Kbyte	1: 5 cycle	0: 8-bit data bus

Example) NAND flash configuration setting example.

Parts	Page size/Total size	OM[3]	OM[2]	OM[1]	OM[0]
K9S1208V0M-xxxx	512Byte / 512Mbit	1	1	0	0
K9K2G08U0M-xxxx	1KW / 2Gbit	1	0	1	0

NAND FLASH MEMORY TIMING

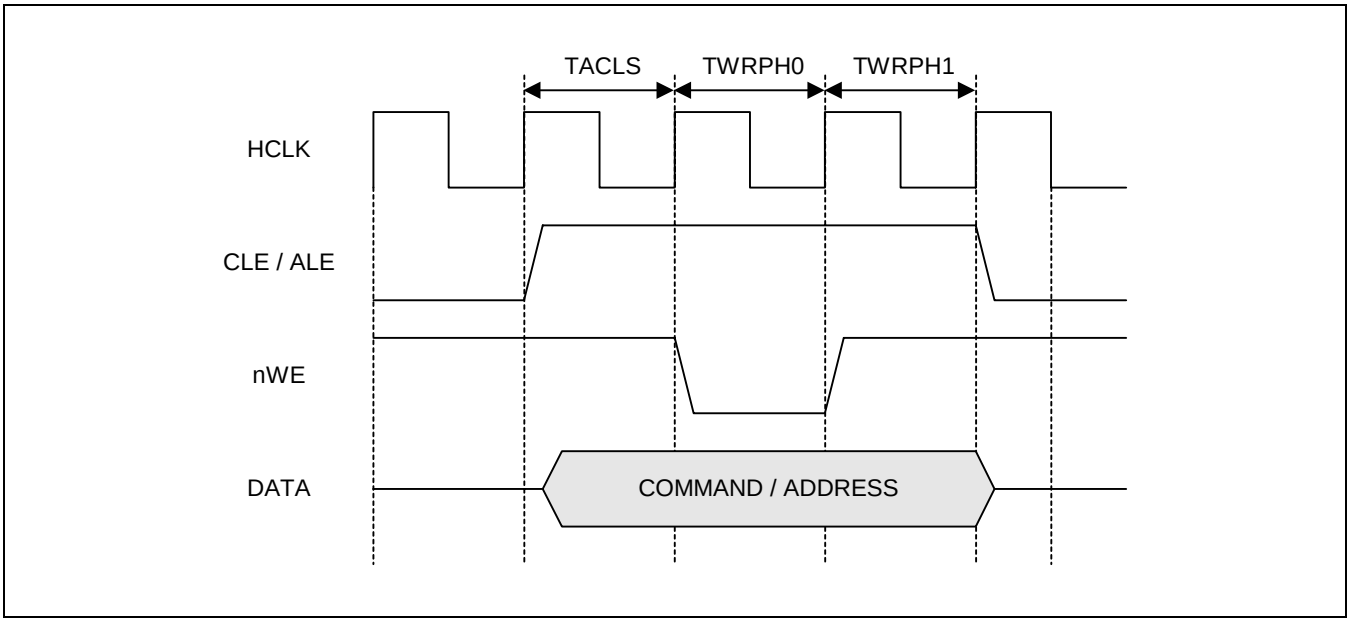


Figure 5-3. CLE & ALE Timing (TACLS = 1, TWRPH0 = 0, TWRPH1 = 0)

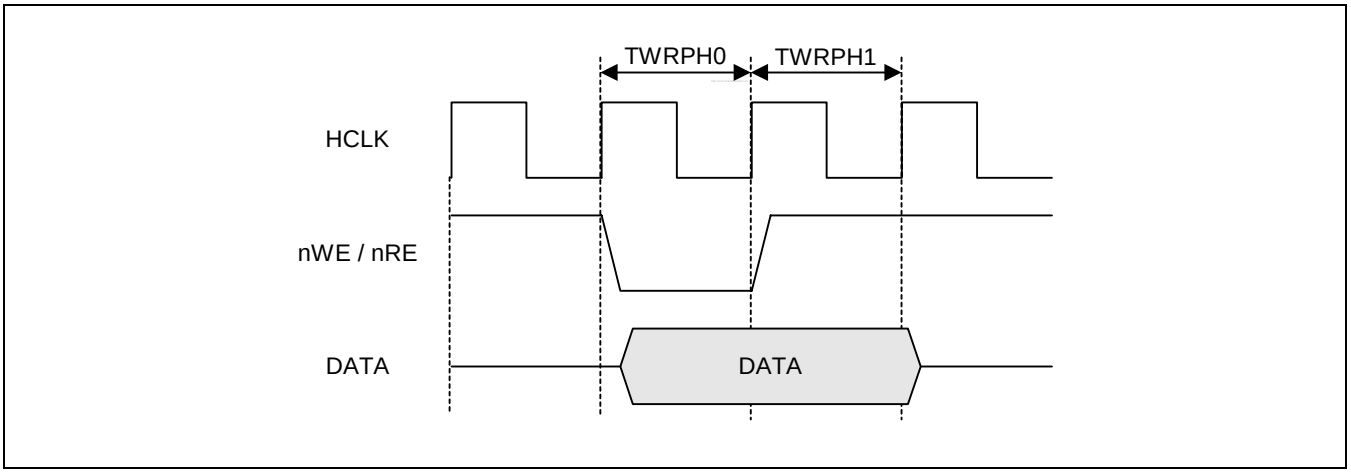


Figure 5-4. nWE & nRE Timing (TWRPH0 = 0, TWRPH1 = 0)

SOFTWARE MODE

S3C2413X only supports software mode access. Using this mode, you can completely access the NAND flash memory. The NAND Flash Controller supports direct access interface with the NAND flash memory.

1. Writing to the command register = the NAND Flash Memory command cycle
2. Writing to the address register = the NAND Flash Memory address cycle
3. Writing to the data register = write data to the NAND Flash Memory (write cycle)
4. Reading from the data register = read data from the NAND Flash Memory (read cycle)
5. Reading main ECC registers and Spare ECC registers = read data from the NAND Flash Memory

NOTE:

In the software mode, you have to check the RnB status input pin by using polling or interrupt.

Data Register Configuration

1. 16-bit NAND Flash Memory Interface

A. Word Access

Register	Endian	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFDATA	Little	2nd I/O[15:8]	2nd I/O[7:0]	1st I/O[15:8]	1st I/O[7:0]
NFDATA	Big	1st I/O[15:8]	1st I/O[7:0]	2nd I/O[15:8]	2nd I/O[7:0]

B. Half-word Access

Register	Endian	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFDATA	Little/Big	Invalid value	Invalid value	1st I/O[15:8]	1st I/O[7:0]

2. 8-bit NAND Flash Memory Interface

A. Word Access

Register	Endian	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFDATA	Little	4th I/O[7:0]	3rd I/O[7:0]	2nd I/O[7:0]	1st I/O[7:0]
NFDATA	Big	1st I/O[7:0]	2nd I/O[7:0]	3rd I/O[7:0]	4th I/O[7:0]

B. Half-word Access

Register	Endian	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFDATA	Little	Invalid value	Invalid value	2nd I/O[7:0]	1st I/O[7:0]
NFDATA	Big	Invalid value	Invalid value	1st I/O[7:0]	2nd I/O[7:0]

C. Byte Access

Register	Endian	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFDATA	Little/Big	Invalid value	Invalid value	Invalid value	1st I/O[7:0]

STEPPINGSTONE (4K-Byte SRAM)

The NAND Flash controller uses Steppingstone as the buffer on booting and also you can use this area for another purpose.

SLC / MLC ECC (Error Correction Code)

NAND flash controller has four ECC (Error Correction Code) modules for SLC NAND flash memory. And has one ECC module for MLC NAND flash memory.

For SLC NAND flash memory interface, NAND flash controller has 4 ECC modules. The two SLC ECC modules (one for data [7:0] and the other for data [15:8]) can be used for (up to) 2048 bytes ECC parity code generation, and the others (one for data[7:0] and the other for data[15:8]) can be used for (up to) 3 bytes ECC Parity code generation.

For MLC NAND flash memory interface, NAND flash controller has one ECC module. This can be used only 512 bytes ECC parity code generation. For 8-bit memory interface, MLC ECC module generate parity code for each 512 byte. And for 16-bit memory interface, MLC ECC module generate parity code for each 256 words(512 bytes). But SLC ECC modules generate parity code per byte lane separately.

Following ECC parity code and two tables are SLC ECC.

28-bit ECC Parity Code = 22bit Line parity + 6bit Column Parity

14-bit ECC Parity Code = 2 bit Line parity + 6bit Column Parity

2048 BYTE SLC ECC PARITY CODE ASSIGNMENT TABLE

	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
MECCn_0	~P64	~P64’	~P32	~P32’	~P16	~P16’	~P8	~P8’
MECCn_1	~P1024	~P1024’	~P512	~P512’	~P256	~P256’	~P128	~P128’
MECCn_2	~P4	~P4’	~P2	~P2’	~P1	~P1’	~P2048	~P2048’
MECCn_3	1	1	1	1	~P8192	~P8192’	~P4096	~P4096’

16 BYTE ECC SLC PARITY CODE ASSIGNMENT TABLE

	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
SECCn_0	~P2	~P2’	~P1	~P1’	~P16	~P16’	~P8	~P8’
SECCn_1	0	0	0	0	0	0	~P4	~P4’

ECC MODULE FEATURES

ECC generation is controlled by the ECC Lock (MainECCLock, SpareECCLock) bit of the Control register. When ECCLock is Low, ECC codes are generated by the H/W ECC modules.

SLC ECC Register Configuration (Little / Big Endian)

Following tables shows the configuration of SLC ECC value read from spare area of external NAND flash memory. For comparing to ECC parity code generated by the H/W modules, the format of ECC read from memory is important.

Note: MLC ECC decoding scheme is different to SLC ECC.

1. 16-bit NAND Flash Memory Interface

Register	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFMECCD0	2nd ECC for I/O[15:8]	2nd ECC for I/O[7:0]	1st ECC for I/O[15:8]	1st ECC for I/O[7:0]
NFMECCD1	4th ECC for I/O[15:8]	4th ECC for I/O[7:0]	3rd ECC for I/O[15:8]	3rd ECC for I/O[7:0]

Register	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFSECCD	2nd ECC for I/O[15:8]	2nd ECC for I/O[7:0]	1st ECC for I/O[15:8]	1st ECC for I/O[7:0]

2. 8-bit NAND Flash Memory Interface

Register	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFMECCD0		2nd ECC for I/O[7:0]		1st ECC for I/O[7:0]
NFMECCD1		4th ECC for I/O[7:0]		3rd ECC for I/O[7:0]

Register	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
NFSECCD	Not used		2nd ECC for I/O[7:0]	1st ECC for I/O[7:0]

SLC ECC PROGRAMMING GUIDE

1. To use SLC ECC in software mode, reset the ECCType to '0'(enable SLC ECC)'. ECC module generates ECC parity code for all read/write data when MainECCLock (NFCON[7]) and SpareECCLock (NFCON[6]) are unlocked('0'). So you have to reset ECC value by writing the InitMECC (NFCONT[5]) and InitSECC (NFCON[4]) bit as '1' and have to clear the MainECCLock (NFCONT[7]) bit to '0'(Unlock) before read or write data.
   MainECCLock (NFCONT[7]) and SpareECCLock(NFCONT[6]) bit controls whether ECC Parity code is generated or not.
2. Whenever data is read or written, the ECC module generates ECC parity code on register NFMECC0/1.
3. After you complete read or write one page (not include spare area data), Set the MainECCLock bit to '1'(Lock). ECC Parity code is locked and the value of the ECC status register will not be changed.
4. To generate spare area ECC parity code, Clear as '0'(Unlock) SpareECCLock(NFCONT[6]) bit.
5. Whenever data is read or written, the spare area ECC module generates ECC parity code on register NFSECC.
6. After you complete read or write spare area, set the SpareECCLock bit to '1'(Lock). ECC Parity code is locked and the value of the ECC status register will not be changed.
7. From now, you can use these values to record to the spare area or check the bit error.
8. For example, to check the bit error of main data area on page read operation, after generating of ECC codes for main data area, you have to move the ECC parity codes (is stored to spare area) to NFMECCD0 and NFMECCD1. From this time, the NFECCERR0 and NFECCERR1 have the valid error status values.

NOTE: NFSECCD is for ECC in the spare area (Usually, the user will write the ECC value generated from main data area to Spare area, which value will be the same as NFMECC0/1) and which is generated from the main data area.

MLC ECC PROGRAMMING GUIDE (ENCODING)

1. To use MLC ECC in software mode, set the ECCType to '1'(enable MLC ECC). ECC module generates ECC parity code for all write data. So you have to reset ECC value by writing the InitMECC (NFCONT[5]) and InitSECC (NFCON[4]) bit as '1' and have to clear the MainECCLock (NFCONT[7]) bit to '0'(Unlock) before write data.
   MainECCLock (NFCONT[7]) and SpareECCLock(NFCONT[6]) bit controls whether ECC Parity code is generated or not.
2. Whenever data is written, the MLC ECC module generates ECC parity code internally.
3. After you complete write 512-byte or 256-words (16-bit I/O) (not include spare area data), Set the MainECCLock bit to '1'(Lock). ECC Parity code generation is locked and the values are updated to NFMECC0, NFMECC1 register when NFSTAT[7] (ECCEncDone) is set('1'). If you use 512-byte or 256-word (16-bit I/O) NAND flash memory, you can program these values to spare area. But if you use NAND flash memory more than 512-byte or 256-word (16-bit I/O) page, you can't program right now. In this case, you have to copy these parity codes to other memory like DRAM. After writing all main data, you can write the copied ECC values to spare area.

MLC ECC PROGRAMMING GUIDE (DECODING)

1. To use MLC ECC in software mode, set the ECCType to ‘1’(enable MLC ECC). ECC module generates ECC parity code for all read data. So you have to reset ECC value by writing the InitMECC (NFCONT[5]) and InitSECC (NFCON[4]) bit as ‘1’ and have to clear the MainECCLock (NFCONT[7]) bit to ‘0’(Unlock) before read data.
   MainECCLock (NFCONT[7]) and SpareECCLock(NFCONT[6]) bit controls whether ECC Parity code is generated or not.
2. Whenever data is read, the MLC ECC module generates ECC parity code internally.
3. After you complete read 512-byte or 256-words (16-bit I/O) (not include spare area data), Set the MainECCLock bit to ‘1’(Lock). ECC Parity code generation is locked. MLC ECC module needs parity codes to detect whether error bits are or not. So you have to read ECC parity code right after read 512-byte or 256-word (in 16-bit I/O). Once ECC parity code is read, MLC ECC engine start to search any error internally. MLC ECC error searching engine need minimum 155 cycles to find any error. During this time, you can continue read main data from external NAND flash memory. NFSTAT[6] can be used to check whether ECC decoding is completed or not.
4. When ECCDecDone (NFSTAT[7]) is set (‘1’), NFESTAT0 indicates whether error bit exist or not. If any error exist, you can fix it by referencing NFSTAT0/1 and NFMLCBITPT register.
5. MLC ECC parity code scheme is used only for main data area to find up to 4-bit error.

NAND FLASH MEMORY MAPPING

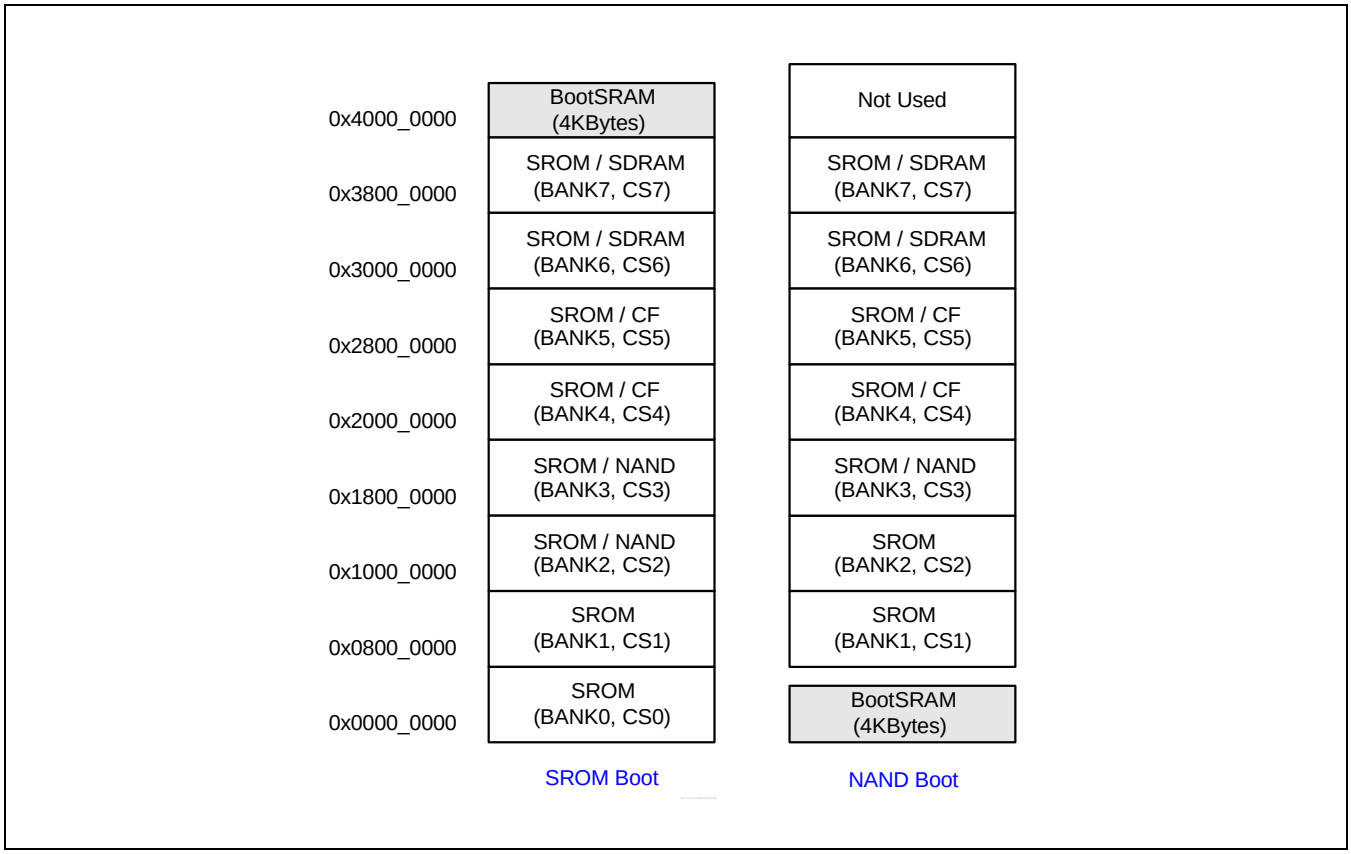


Figure 5-5. NAND Flash Memory Mapping

NOTE:

SROM means ROM or SRAM type memory

NAND FLASH MEMORY CONFIGURATION

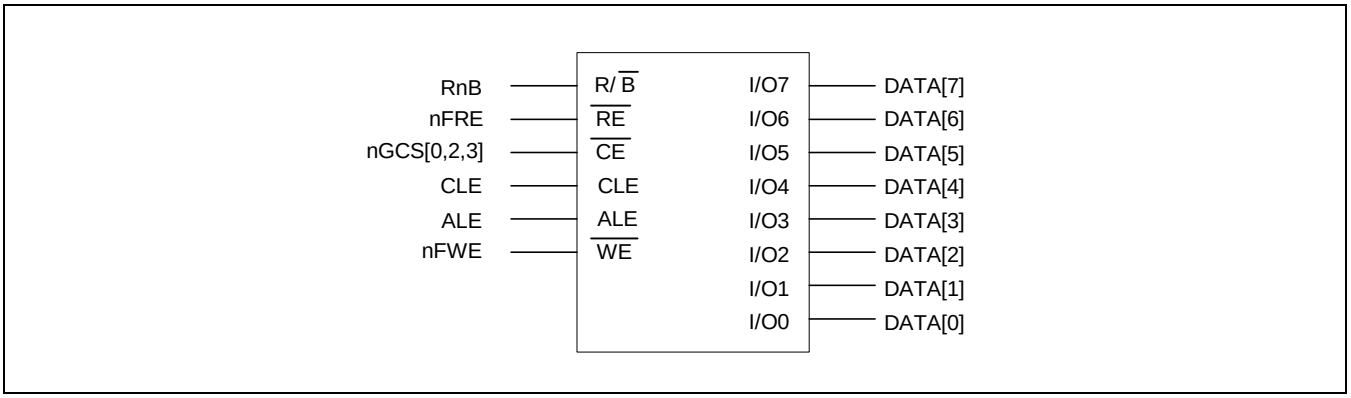


Figure 5-6. A 8-bit NAND Flash Memory Interface

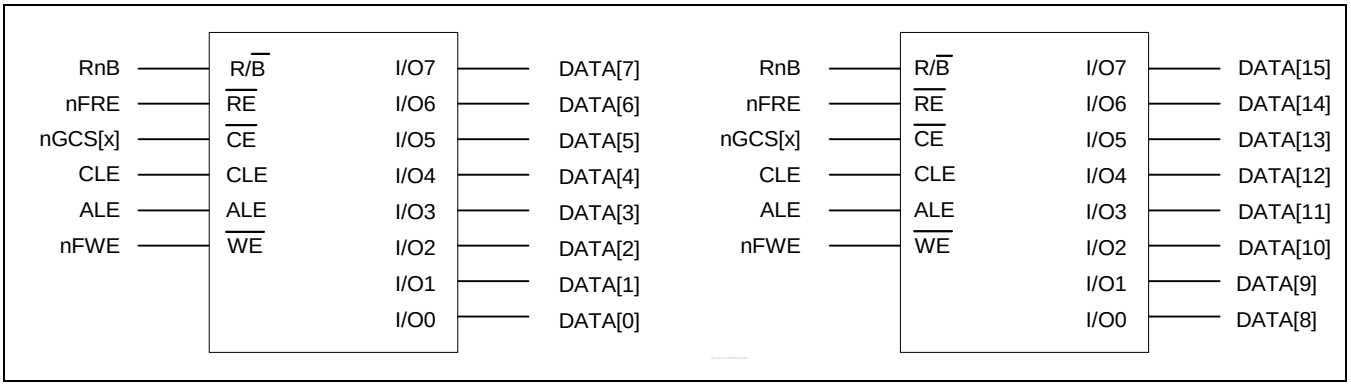


Figure 5-7. Two 8-bit NAND Flash Memory Interface

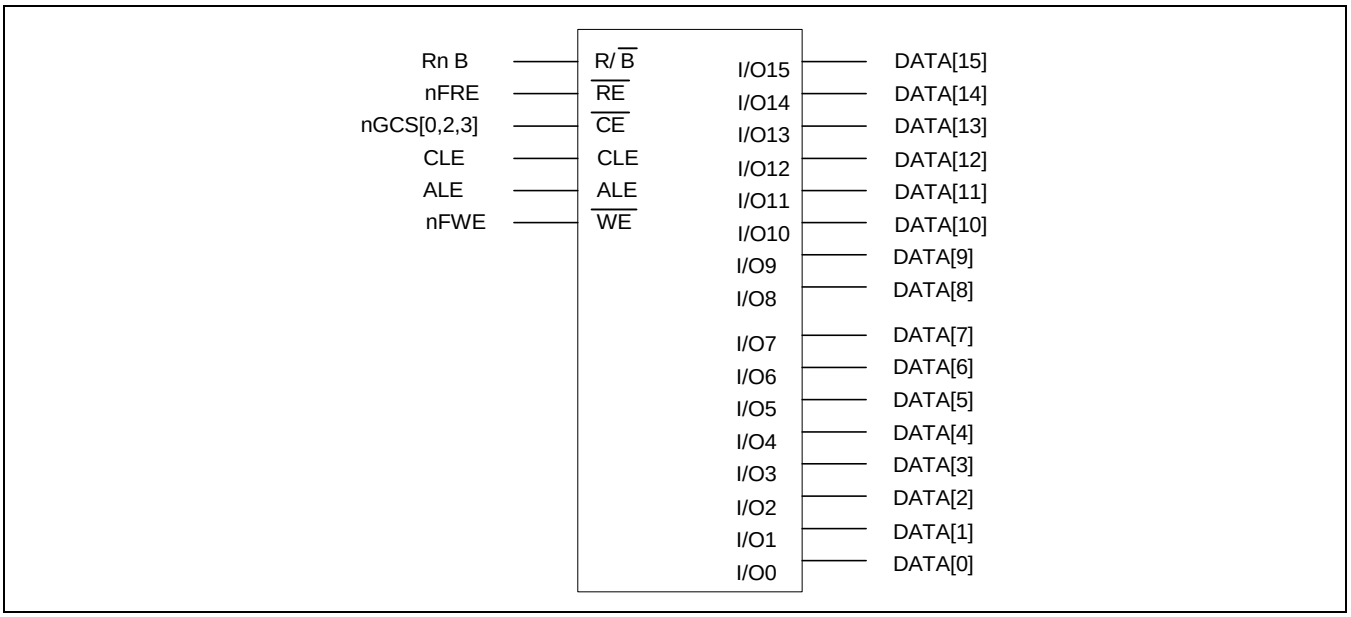


Figure 5-8 A 16-bit NAND Flash Memory Interface

NOTE: NAND CONTROLLER can support to control two nand flash memories .

	NAND BOOT	ROOM BOOT
Reg_nCE0	nGCS0	nGCS2
Reg_nCE1	nGCS3	nGCS3

If you want NAND BOOT, nGCS0 should be using for boot. Optionally you can use nGCS3 for storage.

Or if you want ROOM BOOT, you could use nGCS2 and nGCS3.

NAND FLASH CONTROLLER SPECIAL REGISTERS

NAND FLASH CONTROLLER REGISTER MAP

Address	R/W	Reset value	Name	Description
Base + 0x00	R/W	0x0000_100X	NFCONF	Configuration register
Base + 0x04	R/W	0x0001_00C6	NFCONT	Control register
Base + 0x08	R/W	0x0000_0000	NFCMMD	Command register
Base + 0x0c	R/W	0x0000_0000	NFADDR	Address register
Base + 0x10	R/W	0xXXXX_XXXX	NFDATA	Data register
Base + 0x14	R/W	0x0000_0000	NFMECCD0	1st and 2nd main ECC data register
Base + 0x18	R/W	0x0000_0000	NFMECCD1	3rd and 4th main ECC data register
Base + 0x1c	R/W	0x0000_0000	NFSECCD	Spare ECC read register
Base + 0x20	R/W	0x0000_0000	NFSBLK	Programmable start block address register
Base + 0x24	R/W	0x0000_0000	NFEBLK	Programmable end block address register
Base + 0x28	R/W	0x0080_000D	NFSTAT	NAND status registet
Base + 0x2C	R	0x007F_FFFA	NFECCERR0	ECC error status0 register
Base + 0x30	R	0x007F_FFFA	NFECCERR1	ECC error status1 register
Base + 0x34	R	0xXXXX_XXXX	NFMECC0	Generated ECC status0 register
Base + 0x38	R	0xXXXX_XXXX	NFMECC1	Generated ECC status1 register
Base + 0x3C	R	0xXXXX_XXXX	NFSECC	Generated Spare area ECC status register
Base + 0x40	R	0x0000_0000	NFMLCBITPT	4-bit ECC error bit pattern register
* Base = 0x4E00_0000				

NAND FLASH CONFIGURATION REGISTER

Register	Address	R/W	Description	Reset Value
NFCONF	0x4E000000	R/W	NAND Flash Configuration register	0x0000_100X

NFCONF	Bit	Description	Initial State
NANDBoot	[31]	Shows whether NAND boot or not 1=NAND Flash memory boot	000000
Reserved	[30:25]	Reserved	000000
ECCType	[24]	ECC type selection 0: SLC (1-bit correction) ECC 1:MLC (4-bit correction) ECC	0
Reserved	[23:15]	Reserved	0
TACLS	[14:12]	CLE & ALE duration setting value (0~7) Duration = HCLK x TACLS	001
Reserved	[11]	Reserved	0
TWRPH0	[10:8]	TWRPH0 duration setting value (0~7) Duration = HCLK x (TWRPH0 + 1)	000
Reserved	[7]	Reserved	0
TWRPH1	[6:4]	TWRPH1 duration setting value (0~7) Duration = HCLK x (TWRPH1 + 1)	000
AdvFlash (Read only)	[3]	Advance NAND flash memory for auto-booting 0: Support 256 or 512 byte/page NAND flash memory 1: Support 1024 or 2048 byte/page NAND flash memory This bit is determined by NCON0 pin status during reset and wake-up from sleep mode.	H/W Set
PageSize (R/W)	[2]	NAND flash memory page size for auto-booting AdvFlash PageSize When AdvFlash is 0, 0: 256 Bytes/page, 1: 512 Bytes/page When AdvFlash is 1, 0: 1024 Bytes/page, 1: 2048 Bytes/page This bit is determined by OM[3:0] pin status during reset and wake-up from sleep mode.	H/W Set
AddrCycle (Read only)	[1]	NAND flash memory Address cycle for auto-booting AdvFlash AddrCycle When AdvFlash is 0, 0: 3 address cycle 1: 4 address cycle When AdvFlash is 1, 0: 4 address cycle 1: 5 address cycle This bit is determined by OM[3:0] pin status during reset and wake-up from sleep mode.	H/W Set
BusWidth (R/W)	[0]	NAND Flash Memory I/O bus width for auto-booting and general access. 0: 8-bit bus 1: 16-bit bus This bit is determined by OM[3] pin status during reset and wake-up from sleep mode. This bit can be changed by software.	H/W Set

CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
NFCONT	0x4E000004	R/W	NAND Flash control register	0x0001_00C6

NFCONT	Bit	Description	Initial State
Reserved	[31:19]	Reserved	0x000
ECC Direction	[18]	4-bit ECC encoding / decoding control 0: Decoding 4-bit ECC, It is used for page read 1: Encoding 4-bit ECC, It is be used for page program	0
Lock-tight	[17]	Lock-tight configuration 0: Disable lock-tight 1: Enable lock-tight, Once this bit is set to 1, you cannot clear. Only reset or wake up from sleep mode can make this bit disable (can not cleared by software). When it is set to 1, the area setting in NFSBLK (0x4E000038) to NFEBLK (0x4E00003C)-1 is unlocked, and except this area, write or erase command will be invalid and only read command is valid. When you try to write or erase locked area, the illegal access will be occur (NFSTAT [3] bit will be set). If the NFSBLK and NFEBLK are same, entire area will be locked.	0
Soft Lock	[16]	Soft Lock configuration 0: Disable lock 1: Enable lock Soft lock area can be modified at any time by software. When it is set to 1, the area setting in NFSBLK (0x4E000038) to NFEBLK (0x4E00003C)-1 is unlocked, and except this area, write or erase command will be invalid and only read command is valid. When you try to write or erase locked area, the illegal access will be occur (NFSTAT [3] bit will be set). If the NFSBLK and NFEBLK are same, entire area will be locked.	1
Reserved	[14]	Reserved	0
EnbECCEncINT	[13]	4-bit ECC encoding completion interrupt control 0: Disable interrupt 1: Enable interrupt	0
EnbECCDecINT	[12]	4-bit ECC decoding completion interrupt control 0: Disable interrupt 1: Enable interrupt	0
Reserved	[11]	Reserved	0

NFCONT	Bit	Description	Initial State
EnbIllegalAccINT	[10]	Illegal access interrupt control 0: Disable interrupt 1: Enable interrupt Illegal access interrupt is occurs when CPU tries to program or erase locking area (the area setting in NFSBLK (0x4E000038) to NFEBLK (0x4E00003C)-1).	0
EnbRnBINT	[9]	RnB status input signal transition interrupt control 0: Disable RnB interrupt 1: Enable RnB interrupt	0
RnB_TransMode	[8]	RnB transition detection configuration 0: Detect rising edge 1: Detect falling edge	0
MainECCLock	[7]	Lock Main area ECC generation 0: Unlock Main area ECC 1: Lock Main area ECC Main area ECC status register is NFMECC0/1(0x4E00002C/30),	1
SpareECCLock	[6]	Lock Spare area ECC generation. 0: Unlock Spare ECC 1: Lock Spare ECC Spare area ECC status register is NFSECC(0x4E000034),	1
InitMECC	[5]	1: Initialize main area ECC decoder/encoder (write-only)	0
InitSECC	[4]	1: Initialize spare area ECC decoder/encoder (write-only)	0
Reserved	[3]	Reserved (HW_nCE)	0
Reg_nCE1	[2]	NAND Flash Memory nGCS[3] signal control	1
Reg_nCE0	[1]	NAND Flash Memory nGCS[0],nGCS[2] signal control 0: Force nGCS[0],nGCS[2] to low(Enable chip select) 1: Force nGCS[0],nGCS[2] to High(Disable chip select) Note: During boot time, it is controlled automatically. This value is only valid while MODE bit is 1	1
MODE	[0]	NAND Flash controller operating mode 0: NAND Flash Controller Disable (Don't work) 1: NAND Flash Controller Enable	0

COMMAND REGISTER

Register	Address	R/W	Description	Reset Value
NFCMMD	0x4E000008	R/W	NAND Flash command set register	0x0000_0000

NFCMMD	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0x0000_00
NFCMMD	[7:0]	NAND Flash memory command value	0x00

ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
NFADDR	0x4E00000C	R/W	NAND Flash address set register	0x0000_0000

REG_ADDR	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0x0000_00
NFADDR	[7:0]	NAND Flash memory address value	0x00

DATA REGISTER

Register	Address	R/W	Description	Reset Value
NFDATA	0x4E000010	R/W	NAND Flash data register	0xXXXX_XXXX

NFDATA	Bit	Description	Initial State
NFDATA	[31:0]	NAND Flash read/program data value for I/O (Note) Refer to **DATA REGISTER CONFIGURATION** in p6-5.	0xXXXX_XXXX

MAIN DATA AREA ECC REGISTER

Register	Address	R/W	Description	Reset Value
NFMECCD0	0x4E000014	R/W	NAND Flash ECC 1st and 2nd register for main data read (Note) Refer to **ECC MODULE FEATURES** in p6-8.	0x0000_0000
NFMECCD1	0x4E000018	R/W	NAND Flash ECC 3rd 4th register for main data read (Note) Refer to **ECC MODULE FEATURES** in p6-8.	0x0000_0000

When 16-bit NAND flash is used.

NFMECCD0	Bit	Description	Initial State
ECCData1_1	[31:24]	2nd ECC for I/O[15:8]	0x00
ECCData1_0	[23:16]	2nd ECC for I/O[7:0] Note : In Software mode, Read this register when you need to read 2nd ECC value from NAND flash memory	0x00
ECCData0_1	[15:8]	1st ECC for I/O[15:8]	0x00
ECCData0_0	[7:0]	1st ECC for I/O[7:0] Note : In Software mode, Read this register when you need to read 1st ECC value from NAND flash memory. This register has same read function of NFDATA.	0x00

NOTE: Only word access is valid.

NFMECCD1	Bit	Description	Initial State
ECCData3_1	[31:24]	4th ECC for I/O[15:8]	0x00
ECCData3_0	[23:16]	4th ECC for I/O[7:0] Note : In Software mode, Read this register when you need to read 4th ECC value from NAND flash memory	0x00
ECCData2_1	[15:8]	3rd ECC for I/O[15:8]	0x00
ECCData2_0	[7:0]	3rd ECC for I/O[7:0] Note: In Software mode, Read this register when you need to read 3rd ECC value from NAND flash memory. This register has same read function of NFDATA.	0x00

NOTE: Only word access is valid.

When 8-bit interface NAND flash is use.

NFMECCD0	Bit	Description	Initial State
	[31:24]	-	0x00
ECCData1	[23:16]	ECC1 for I/O[7:0]	0x00
	[15:8]	-	0x00
ECCData0	[7:0]	ECC0 for I/O[7:0]	0x00

NOTE: Only word access is valid.

NFMECCD1	Bit	Description	Initial State
	[31:24]	-	0x00
ECCData3	[23:16]	ECC3 for I/O[7:0]	0x00
	[15:8]	-	0x00
ECCData2	[7:0]	ECC2 for I/O[7:0]	0x00

SPARE AREA ECC REGISTER

Register	Address	R/W	Description	Reset Value
NFSECCD	0x4E00001C	R/W	NAND Flash ECC(Error Correction Code) register for spare area data read	0x0000_0000

When 16-bit NAND flash is used.

NFSECCD	Bit	Description	Initial State
ECCData1_1	[31:24]	2nd ECC for I/O[15:8]	0x00
ECCData1_0	[23:16]	2nd ECC for I/O[7:0] Note: In Software mode, Read this register when you need to read 2nd ECC value from NAND flash memory	0x00
ECCData0_1	[15:8]	1st ECC for I/O[15:8]	0x00
ECCData0_0	[7:0]	1st ECC for I/O[7:0] Note: In Software mode, Read this register when you need to read 1st ECC value from NAND flash memory. This register has same read function of NFDATA.	0x00

NOTE: Only word access is valid.

When 8-bit NAND flash is used.

NFSECCD	Bit	Description	Initial State
Reserved	[31:16]	Not used	0x00
Reserved	[23:16]	Not used	0x00
SECCData1	[15:8]	2nd Spare area ECC for I/O[7:0]	0x00
SECCData0	[7:0]	1st Spare area ECC for I/O[7:0]	0x00

NOTE: Only word or half word access is valid.

PROGRMMABLE BLOCK ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
NFSBLK	0x4E000020	R/W	NAND Flash programmable start block address	0x0000_0000
NFEBLK	0x4E000024	R/W	NAND Flash programmable end block address Nand Flash can be programmed between start and end address. When the Soft lock or Lock-tight is enabled and the Start and End address has same value, Entire area of NAND flash will be locked.	0x0000_0000

NFSBLK	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
SBLK_ADDR2	[23:16]	The 3rd block address of the block erase operation	0x00
SBLK_ADDR1	[15:8]	The 2nd block address of the block erase operation	0x00
SBLK_ADDR0	[7:0]	The 1st block address of the block erase operation (Only bit [7:5] are valid)	0x00

NOTE: Advance Flash's block Address start from 3-address cycle. So block address register only needs 3-bytes.

NFEBLK	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
EBLK_ADDR2	[23:16]	The 3rd block address of the block erase operation	0x00
EBLK_ADDR1	[15:8]	The 2nd block address of the block erase operation	0x00
EBLK_ADDR0	[7:0]	The 1st block address of the block erase operation (Only bit [7:5] are valid)	0x00

NOTE: Advance Flash's block Address start from 3-address cycle. So block address register only needs 3-bytes.

The NFSLK and NFEBLK can be changed while Soft lock bit(NFCONT[12]) is enabled. But cannot be changed when Lock-tight bit(NFCONT[13]) is set.

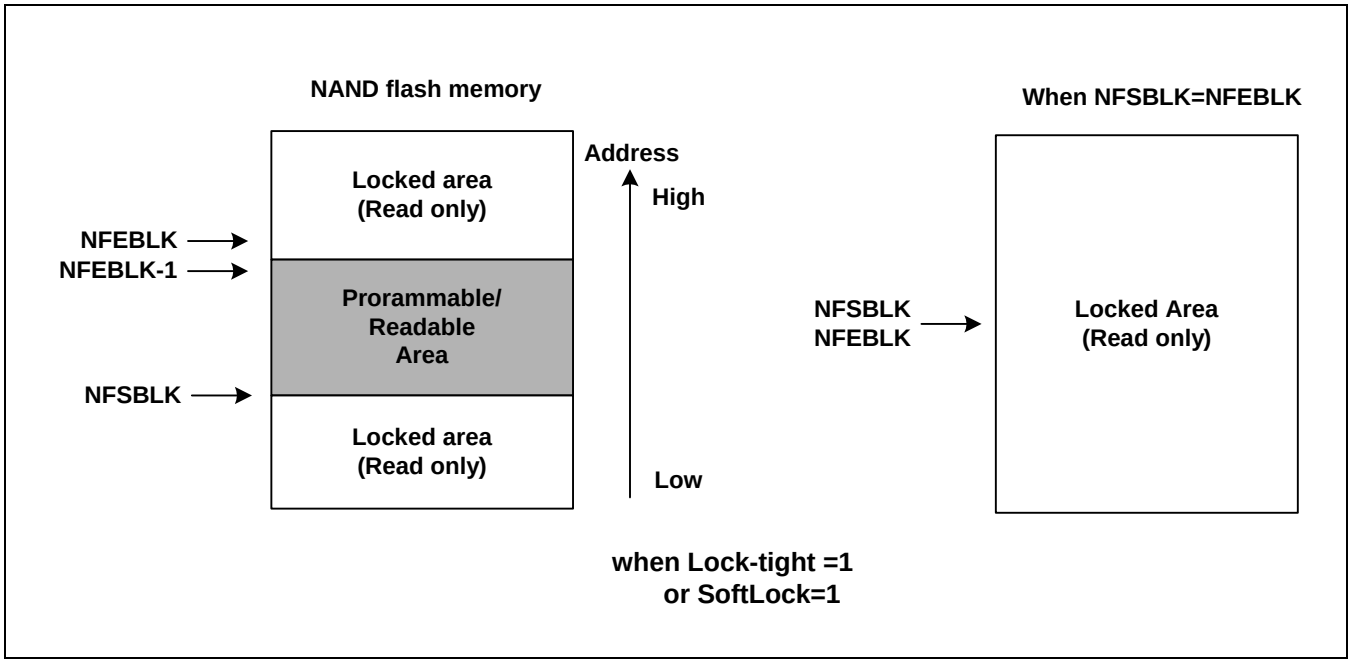


Figure 5-9..

NFCON STATUS REGISTER

Register	Address	R/W	Description	Reset Value
NFSTAT	0x4E000028	R/W	NAND Flash operation status register	0x0080_000D

NFSTAT	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0x0080_00
ECCEncDone	[7]	When 4-bit ECC encodng is finished, this value set and issue interrupt if enabled. The NFMLCECC0 and NFMLCECC1 have valid values. To clear this write to '1' 1: 4-bit ECC encoding is completed	0
ECCDecDone	[6]	When 4-bit ECC decoding is finished, this value set and issue interrupt if enabled. The NFMLCBITPT, NFMLCL0 and NFMLCEL1 have valid values., .To clear this write to '1' 1: 4-bit ECC decoding is completed	0
IllegalAccess	[5]	Once Soft Lock or Lock-tight is enabled, The illegal access (program, erase) to the memory makes this bit set. 0: illegal access is not detected 1: illegal access is detected	0
RnB_TransDetect	[4]	When RnB low to high transition is occurred, this value set and issue interrupt if enabled. To clear this write '1'. 0: RnB transition is not detected 1: RnB transition is detected Transition configuration is set in RnB_TransMode(NFCONT[8]).	0
NCE[1] (Read-only)	[3]	The status of nCE[1] output pin	1
NCE[0] (Read-only)	[2]	The status of nCE[0] output pin	1
Reserved	[1]	Reserved	0
RnB (Read-only)	[0]	The status of RnB input pin. 0: NAND Flash memory busy 1: NAND Flash memory ready to operate	1

ECC0/1 STATUS REGISTER

Register	Address	R/W	Description	Reset Value
NFECCERR0	0x4E00002C	R	NAND Flash ECC Error Status register for I/O [7:0]	0x007F_FFFA
NFECCERR1	0x4E000030	R	NAND Flash ECC Error Status register for I/O [15:8]	0x007F_FFFA

When ECCType is SLC.

NFECCERR0	Bit	Description	Initial State
Reserved	[31:25]	Reserved	0x00
SErrorDataNo	[24:21]	In spare area, Indicates which number data is error	0011
SErrorBitNo	[20:18]	In spare area, Indicates which bit is error	111
MErrorDataNo	[17:7]	In main data area, Indicates which number data is error	0x7FF
MErrorBitNo	[6:4]	In main data area, Indicates which bit is error	111
SpareError	[3:2]	Indicates whether spare area bit fail error occurred 00: No Error 01: 1-bit error(correctable) 10: Multiple error 11: ECC area error	10
MainError	[1:0]	Indicates whether main data area bit fail error occurred 00: No Error 01: 1-bit error(correctable) 10: Multiple error 11: ECC area error	10

NOTE: The above values are only valid when both ECC register and ECC status register have valid value.

NFECCERR1	Bit	Description	Initial State
Reserved	[31:25]	Reserved	0x00
SErrorDataNo	[24:21]	In spare area, Indicates which number data is error	0011
SErrorBitNo	[20:18]	In spare area, Indicates which bit is error	111
MErrorDataNo	[17:7]	In main data area, Indicates which number data is error	0x7FF
MErrorBitNo	[6:4]	In main data area, Indicates which bit is error	111
SpareError	[3:2]	Indicates whether spare area bit fail error occurred 00: No Error 01: 1-bit error(correctable) 10: Multiple error 11: ECC area error	10
MainError	[1:0]	Indicates whether main data area bit fail error occurred 00: No Error 01: 1-bit error(correctable) 10: Multiple error 11: ECC area error	10

NOTE: The above values are only valid when both ECC register and ECC status register have valid value.

When ECCType is MLC.

NFECCERR0	Bit	Description	Initial State
ECC Busy	[31]	Indicates the 4-bit ECC decoding engine is searching whether a error exists or not 0: Idle 1: Busy	0
ECC Ready	[30]	ECC Ready bit	1
Free Page	[29]	Inidicates the page data red from NAND flash has all 'FF' value.	0
MLC MECC Error	[28:26]	4-bit ECC decoding result 000: No error 001: 1-bit error 010: 2-bit error 011: 3-bit error 100: 4-bit error 101: Uncorrectable 11x: reserved	000
2nd Bit Error Location	[25:16]	Error byte location of 2nd bit error	0x00
Reserved	[15:10]	Reserved	0x0
1st Bit Error Location	[9:0]	Error byte location of 1st bit error	0x00

NOTE: These values are updated when ECCDecDone (NFSTAT[6]) is set ('1').

NFECCERR1	Bit	Description	Initial State
Reserved	[31:26]	Reserved	0x00
4th Bit Error Location	[25:16]	Error byte location of 4th bit error	0x00
Reserved	[15:10]	Reserved	0x0
3rd Bit Error Location	[9:0]	Error byte location of 3rd bit error	0x00

NOTE: These values are updated when ECCDecDone (NFSTAT[6]) is set ('1').

MAIN DATA AREA ECC0 STATUS REGISTER

Register	Address	R/W	Description	Reset Value
NFMECC0	0x4E000034	R	SLC or MLC NAND Flash ECC status register	0xXXXX_XXXX
NFMECC1	0x4E000038	R	SLC or MLC NAND Flash ECC status register	0xXXXX_XXXX

When ECCType is SLC

NFMECC0	Bit	Description	Initial State
MECC0_3	[31:24]	ECC3 for data[7:0]	0xXX
MECC0_2	[23:16]	ECC2 for data[7:0]	0xXX
MECC0_1	[15:8]	ECC1 for data[7:0]	0xXX
MECC0_0	[7:0]	ECC0 for data[7:0]	0xXX

NFMECC1	Bit	Description	Initial State
MECC1_3	[31:24]	ECC3 data[15:8]	0xXX
MECC1_2	[23:16]	ECC2 data[15:8]	0xXX
MECC1_1	[15:8]	ECC1 data[15:8]	0xXX
MECC1_0	[7:0]	ECC0 data[15:8]	0xXX

NOTE: The NAND flash controller generate NFMECC0/1 when read or write main area data while the MainECCLock(NFCONT[7]) bit is '0'(Unlock).

When ECCType is MLC.

NFMECC0	Bit	Description	Initial State
4th Parity	[31:24]	4th Check Parity generated from main area (512-byte)	0x00
3rd Parity	[23:16]	3rd Check Parity generated from main area (512-byte)	0x00
2nd Parity	[15:8]	2nd Check Parity generated from main area (512-byte)	0x00
1st Parity	[7:0]	1st Check Parity generated from main area (512-byte)	0x00

NFMECC1	Bit	Description	Initial State
Reserved	[31:24]	Reserved	0x00
7th Parity	[23:16]	7th Check Parity generated from main area (512-byte)	0x00
6th Parity	[15:8]	6th Check Parity generated from main area (512-byte)	0x00
5th Parity	[7:0]	5th Check Parity generated from main area (512-byte)	0x00

NOTE: The NAND flash controller generate these ECC parity codes when write main area data while the MainECCLock (NFCON[7]) bit is '0'(unlock).

SPARE AREA ECC STATUS REGISTER

Register	Address	R/W	Description	Reset Value
NFSECC	0x4E00003C	R	NAND Flash ECC register for I/O [15:0]	0xXXXX_XXXX

NFSECC	Bit	Description	Initial State
SECC1_1	[31:24]	Spare area ECC1 Status for I/O[15:8]	0xXX
SECC1_0	[23:16]	Spare area ECC0 Status for I/O[15:8]	0xXX
SECC0_1	[15:8]	Spare area ECC1 Status for I/O[7:0]	0xXX
SECC0_0	[7:0]	Spare area ECC0 Status for I/O[7:0]	0xXX

NOTE: The NAND flash controller generate NFSECC when read or write spare area data while the SpareECCLock(NFCONT[6]) bit is '0'(Unlock).

MLC 4-BIT ECC ERROR PATTEN REGISTER

Register	Address	R/W	Description	Reset Value
NFMLCBITPT	0x4E000040	R	NAND Flash 4-bit ECC Error Pattern register for data[7:0]	0x0000_0000

NFMLCBITPT	Bit	Description	Initial State
4th Error bit pattern	[31:24]	4th Error bit pattern	0x00
3rd Error bit pattern	[23:16]	3rd Error bit pattern	0x00
2nd Error bit pattern	[15:8]	2nd Error bit pattern	0x00
1st Error bit pattern	[7:0]	1st Error bit pattern	0x00

6 SYSTEM CONTROLLER

OVERVIEW

The system controller consists of three parts: clock control, reset control, and power control.

The clock control logic in S3C2413X can generate the required clock signals including ARMCLK for ARM926EJ, HCLK for the AHB bus peripherals, and PCLK for the APB bus peripherals. The S3C2413X has two Phase Locked Loops (PLLs): one for ARMCLK, HCLK, and PCLK, and the other for USB block and CAMIF block. The clock control logic can make slow clocks without PLL and connect/disconnect the clock to each peripheral block by software, which will reduce the power consumption.

For the power control logic, the S3C2413X has various power management schemes to keep minimal power dissipation for a given task. The power management block in the S3C2413X can activate four modes: NORMAL mode, IDLE mode, STOP mode, and SLEEP mode.

Normal mode: system controller supplies clocks to CPU as well as all peripherals in S3C2413X. In this mode, the performance is maximized and the power consumption will be high when all clocks of peripherals are operated. It allows the user to control the operation of peripherals by software. For example, if a timer is not needed, the user can disconnect the clock to the timer to eliminate the power consumption by the timer.

IDLE mode: the ARM operation clock, ARMCLK, will be fixed to low while the clock generator supplies the clocks for all other peripherals. The IDLE mode results in reduced power consumption due to CPU core. Any interrupt requests to CPU can be woken up from the IDLE mode.

STOP mode: all operation clocks, including ARM, all AHB peripherals, and all APB peripherals, are fixed to low. However, the operation power is supplied by the external power supplier, and the internal hardware status will be sustained. Power mode can be changed into NORMAL and SLEEP mode when there is the external reset and RTC interrupt, and external interrupts.

SLEEP mode: the internal power will be disconnected. So, there occurs no power consumption due to ARM and the internal logic except the wake-up logic in this mode. Activating the SLEEP mode requires two independent power sources. One power source supplies the power for the wake-up logic while the other supplies other internal logic including ARM. They should be controlled for power on/off. In the SLEEP mode, the second power source for the ARM and internal logic will be turned off. The wakeup from SLEEP mode can be issued by the external interrupt or by RTC alarm interrupt.

FUNCTIONAL DESCRIPTION

This section describes the functionality of the system controller, which includes the clock architecture, reset scheme, and power management modes.

Figure 6-1 shows the block diagram of the clock generation module. The main clock source comes from an external crystal (XTIpll) and external clock (EXTCLK). The clock generator consists of two PLLs (Phase Locked Loop) which generate high frequency clock signals required in S3C2413X.

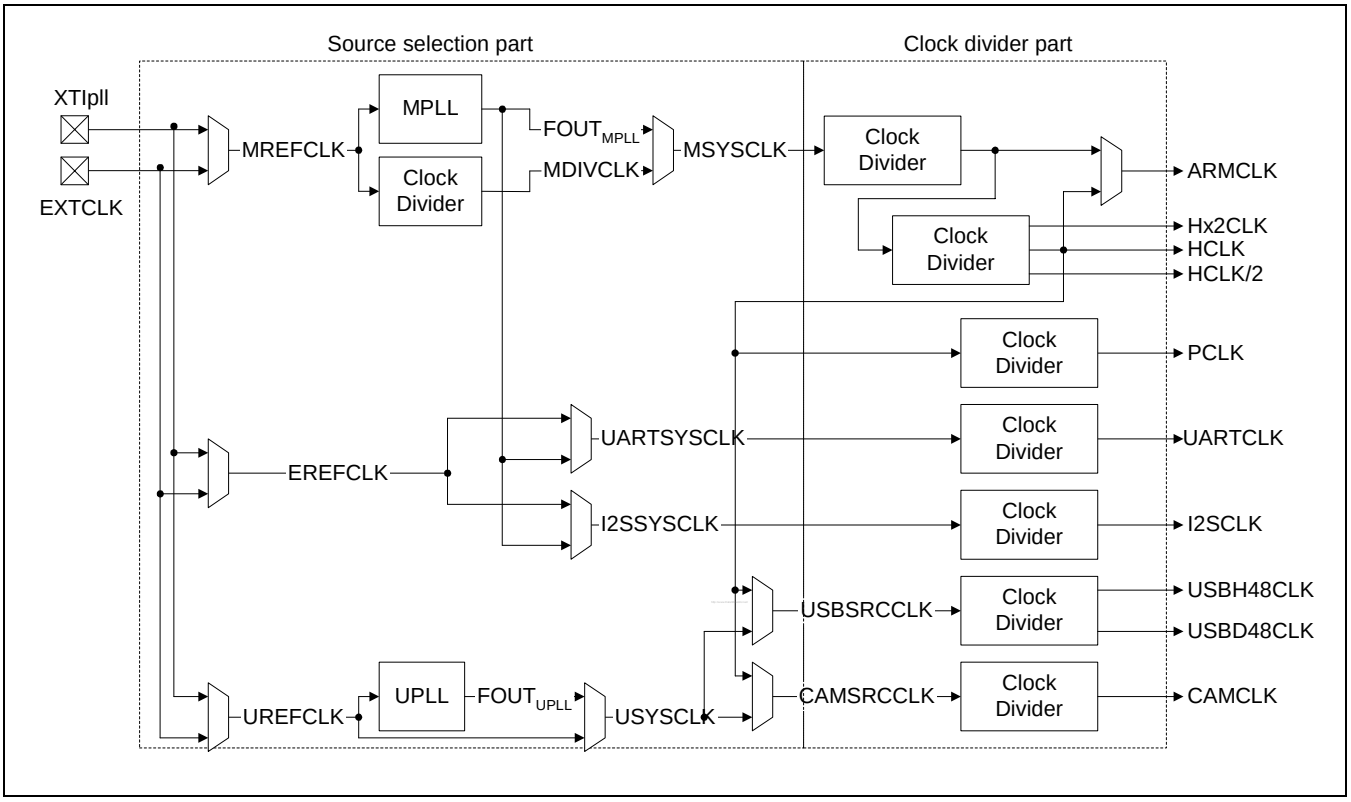


Figure 6-1. Clock Generator Block Diagram

CLOCK ARCHITECTURE

S3C2413 requires many internal clocks to support various functional blocks, which requires appropriate operating clocks. As shown in Figure 6-1, the clock generator mainly consists of two parts. The intermediate clocks, which are MSYSCLK, UARTSYSCLK, I2SSYSCLK, USYSCLK, are generated using two PLLs and several MUXs. They will be the reference clocks for all internal clocks. The clock divider logic divides the reference clocks and makes the input clocks of internal blocks.

CLOCK SOURCE SELECTION

Internal clocks will be generated using external clock source as shown in Table 6-1. The OM[0:4] pins determine the operating mode of S3C2413 when the external reset signal is applied. As shown in the table, the OM[4] selects the external clock source, i.e., if the OM[4] is low, the external crystal will be selected. Otherwise, the external clock will be the source of internal clocks. However, if the operating mode is a test mode, then the external clock source will be oscillator regardless of the OM[4].

Table 6-1. Device operating mode selection at boot-up

OM[0:4]	Boot device	Function	PLL clock source
00 10x	NAND	AdvFlash=0, PageSize=512, AddrCycle=3	XTIpll if OM[4] = 0 EXTCLK if OM[4] = 1
00 11x		AdvFlash=0, PageSize=512, AddrCycle=4	
01 10x		AdvFlash=1, PageSize=2KB, AddrCycle=4	
01 11x		AdvFlash=1, PageSize=2KB, AddrCycle=5	
10 00x	NOR	16-bit boot	
10 01x		32-bit boot	
10 10x	OneNAND	16-bit boot	
10 11x		32-bit boot	
11101	TEST	JTAG Boundary Scan	

The operating mode mainly is classified into four categories according to the boot mode. The boot code can be placed in NAND, NOR, and OneNAND, since the S3C2413 memory controller can support them as an external device. Each boot mode contains several sub-groups according to the each characteristic.

PHASE LOCKED LOOP (PLL)

The MPLL and the UPLL within the clock generator, as an analog circuit, synchronizes an output signal with a reference input signal in frequency and phase. In this application, it includes the following basic blocks as shown in Figure 6-2 The Voltage Controlled Oscillator (VCO) generates the output frequency proportional to input DC voltage. The pre-divider divides the input frequency (Fin) by P. The main divider divides the VCO output frequency by M, which is input to Phase Frequency Detector (PFD). The post scaler divides the VCO output frequency by S, which is $MPLL_{FOUT}$ (the output frequency from MPLL block)/$UPLL_{FOUT}$ (the output frequency from UPLL block). The phase difference detector calculates the phase difference and the charge pump increases/decreases the output voltage. The output clock frequencies $MPLL_{FOUT}$ and $UPLL_{FOUT}$ are related to the reference input clock frequency $MPLL_{FIN}$ and $UPLL_{FIN}$ by the following equation:

$FOUT_{MPLL} = (2m \times FIN) / (p \times 2^{S})$

where, m = (MDIV + 8), p = (PDIV + 2), s = SDIV

$FOUT_{UPLL} = (m \times FIN) / (p \times 2^{S})$

where, m = (MDIV + 8), p = (PDIV + 2), s = SDIV

The following sections describe the operation of the PLL, including the phase difference detector, the charge pump, the Voltage controlled oscillator (VCO), and the loop filter.

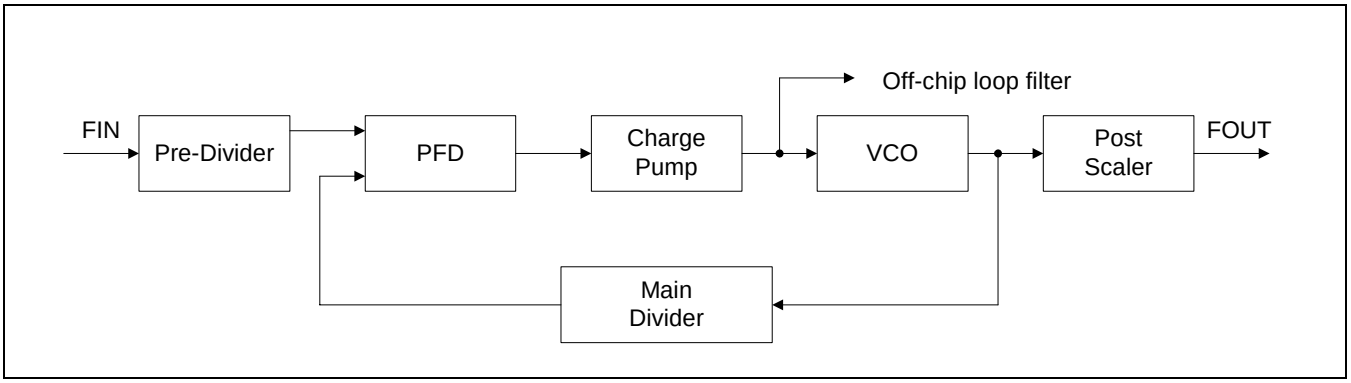


Figure 6-2. S3C2413 internal PLL block diagram

PHASE FREQUENCY DETECTOR (PFD)

The PFD monitors the phase difference between Fref and Fvco, and generates a control signal (tracking signal) when it detects a difference. The Fref means the reference frequency as shown in the Figure XXX.

CHARGE PUMP (PUMP)

The charge pump converts PFD control signals into a proportional charge in voltage across the external filter that drives the VCO.

LOOP FILTER

The control signal, which the PFD generates for the charge pump, may generate large excursions (ripples) each time the F_{VCO} is compared to the F_{REF}. To avoid overloading the VCO, a low pass filter samples and filters the high-frequency components out of the control signal. The filter is typically a single-pole RC filter with a resistor and a capacitor.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

The output voltage from the loop filter drives the VCO, causing its oscillation frequency to increase or decrease linearly as a function of variations in average voltage. When the Fvco matches Fref in terms of frequency as well as phase, the PFD stops sending control signals to the charge pump, which in turn stabilizes the input voltage to the loop filter. The VCO frequency then remains constant, and the PLL remains fixed onto the system clock.

USUAL CONDITIONS FOR PLL & CLOCK GENERATOR

PLL & Clock Generator generally uses the following conditions.

Loop filter capacitance	**MPLL : 820 pF**
	UPLL : 1500 pF
External X-tal frequency	10 – 20 MHz (note)
External capacitance used for X-tal	15 – 22 pF

NOTES:
1. The value could be changed.
2. FCLK must be more than three times X-tal or EXTCLK (FCLK ≥ 3X-tal or 3EXTCLK)

CHANGE PLL SETTINGS IN NORMAL OPERATION MODE

During the operation of the S3C2413A in NORMAL mode, the user can change the frequency by writing the PMS value and the PLL lock time will be automatically inserted for stabilizing the output frequency of the PLL. During the lock time, the clock is not supplied to the internal blocks in the S3C2413A as shown in Figure 6-3. The PLL restarts the lockup sequence toward the new frequency only after the software configures the PLL with a new frequency. The system clock can be configured as PLL output ($MPLL_{FOUT}$) immediately after lock time.

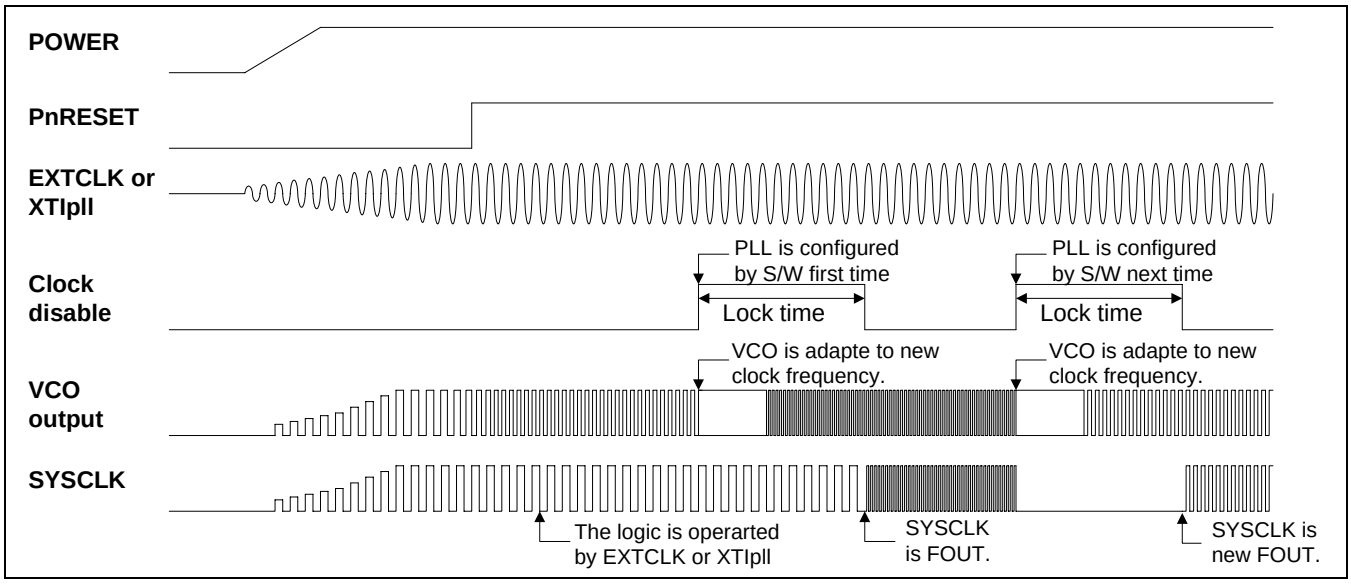


Figure 6-3. PLL lock time will be automatically inserted when MPS value is changed.

During the lock time, all reference clocks of Figure 6-1 will stop. Thus, the MPS value change can cause a problem in LCD display. In the S3C2413, the LCD screen-refresh timing is dependent on the HCLK (HCLK clock is directly dependent on the MSYSCLK of Figure 6-1.)

Although there are many combinations to generate PLL output with a certain frequency, it is not easy to find a proper PLL value to produce stable output. Thus, we strongly recommend referring to the following PLL value recommendation table.

Table 6-2. PMS recommendation table (FIN = 12MHz)

$FOUT_{MPLL}$	P	M	S	$FOUT_{UPLL}$	P	M	S
200.00	1	42 (0x2A)	1	24.00	7	64 (0x40)	2
210.00	2	62 (0x3E)	1	25.00	7	67 (0x43)	2
220.00	1	47 (0x2F)	1	30.00	6	72 (0x48)	2
230.00	4	107 (0x6B)	1	40.00	7	52 (0x34)	1
240.00	2	72 (0x48)	1	48.00	7	64 (0x40)	1
250.00	4	117 (0x75)	1	50.00	7	67 (0x43)	1
260.00	1	57 (0x39)	1	60.00	6	72 (0x48)	1
266.00	4	125 (0x7D)	1	66.00	5	69 (0x45)	1
280.00	1	62 (0x3E)	1	70.00	4	62 (0x3E)	1
288.00	2	88 (0x58)	1	80.00	7	52 (0x34)	0
300.00	1	67 (0x43)	1	90.00	6	52 (0x34)	0
320.00	4	72 (0x48)	0	96.00	7	64 (0x40)	0
336.00	2	48 (0x30)	0	100.00	7	67 (0x43)	0
340.80	3	63 (0x3F)	0	110.00	4	47 (0x2F)	0
360.00	2	52 (0x34)	0	120.00	6	72 (0x48)	0
380.00	4	87 (0x57)	0	130.00	4	57 (0x39)	0
384.00	2	56 (0x38)	0	133.00	10	125 (0x7D)	0
400.00	1	42 (0x2A)	0	140.00	4	62 (0x3E)	0
				144.00	7	100 (0x64)	0
				150.00	4	67 (0x43)	0

USB Clock Control

USB host/device interface needs 48MHz clock. In the S3C2413A, the USB dedicated PLL (UPLL) generates 48MHz for USB.

CLOCK CONTROL LOGIC

The MSYSCLK is the base clock for S3C2413 system clock, such as ARMCLK, HCLK, PCLK, HCLKx2, HCLK/2, etc. The ARMCLK is used for ARM926EJ-S core, the main CPU of the S3C2413x. The HCLK is the reference clock for internal AHB bus and peripherals such as the memory controller, the interrupt controller, the LCD controller, etc. The PCLK is used for internal APB bus and peripherals such as WDT, IIS, I2C, PWM timer, etc. The USYSCLK is the base clock for USB interface block and the camera interface block.

The clock control logic determines the clock source to be used, i.e., the PLL clock ($MPLL_{FOUT}$) or the divided external clock (XTIpll or EXTCLK). When PLL is configured to a new frequency value, the clock control logic disables the $MPLL_{FOUT}$ until the PLL output is stabilized during the PLL locking time. The clock ratio can be configured with the CLKDIVN register as shown in Table 6-3. The HCLK/2 is half frequency of the HCLK if the HALFCLK field is set.

Table 6-3. ARMCLK, HCLK, HCLKx2, HCLK/2, and PCLK clock ratio

ARMDIV	HCLKDIV	PCLKDIV	ARMCLK	HCLK	HCLKx2	HCLK/2	PCLK
0	0	0	MSYSCLK	MSYSCLK	MSYSCLK	MSYSCLK / 2	MSYSCLK
0	0	1	MSYSCLK	MSYSCLK	MSYSCLK	MSYSCLK / 2	MSYSCLK / 2
0	1	0	MSYSCLK	MSYSCLK/2	MSYSCLK	MSYSCLK / 4	MSYSCLK / 2
0	1	1	MSYSCLK	MSYSCLK/2	MSYSCLK	MSYSCLK / 4	MSYSCLK / 4
0	2	0	MSYSCLK	MSYSCLK/3	MSYSCLK	MSYSCLK / 6	MSYSCLK / 3
0	2	1	MSYSCLK	MSYSCLK/3	MSYSCLK	MSYSCLK / 6	MSYSCLK / 6
0	3	0	MSYSCLK	MSYSCLK/4	MSYSCLK/2	MSYSCLK / 8	MSYSCLK / 4
0	3	1	MSYSCLK	MSYSCLK/4	MSYSCLK/2	MSYSCLK / 8	MSYSCLK / 8
1	0	0	MSYSCLK/2	MSYSCLK/2	MSYSCLK/1	MSYSCLK / 2	MSYSCLK / 2
1	0	1	MSYSCLK/2	MSYSCLK/2	MSYSCLK/1	MSYSCLK / 4	MSYSCLK / 4
1	1	0	MSYSCLK/2	MSYSCLK/4	MSYSCLK/2	MSYSCLK / 4	MSYSCLK / 4
1	1	1	MSYSCLK/2	MSYSCLK/4	MSYSCLK/2	MSYSCLK / 8	MSYSCLK / 8
1	2	0	MSYSCLK/2	MSYSCLK/6	MSYSCLK/3	MSYSCLK / 12	MSYSCLK / 6
1	2	1	MSYSCLK/ 2	MSYSCLK/6	MSYSCLK/3	MSYSCLK / 12	MSYSCLK / 12
1	3	0	MSYSCLK/2	MSYSCLK/8	MSYSCLK/4	MSYSCLK / 16	MSYSCLK / 8
1	3	1	MSYSCLK/2	MSYSCLK/8	MSYSCLK/4	MSYSCLK / 16	MSYSCLK / 16

NOTES:

1. In (ARMDIV,HCLKDIV,PCLKDIV) = (0,0,0), (0,0,1), (0,2,0), (0,2,1) mode, external DDR is not supported.

RESET MANAGEMENT

Figure 6-3 shows the clock behavior during the power-on reset sequence. The crystal oscillator begins oscillation within several milliseconds. When nRESET is released after the stabilization of OSC (XTIpll) clock, the PLL starts to operate according to the default PLL configuration. However, PLL is commonly known to be unstable after power-on reset, so the external clock is fed directly to the system clock instead of the $MPLL_{FOUT}$ (PLL output) before the software newly configures the MPLLCON. User should clear the ONOFF field of MPLLCON register to run the MPLL.

S3C2413x has four types of resets and the reset controller in the system controller can place the system into one of four resets.

- Hardware reset: The hardware reset is generated when nRESET is asserted. It is an uncompromised, ungated, total and complete reset that is used when you do not need information in system any more.
- Watchdog reset: Reset signal by watchdog timer
- Software reset: Reset signal by setting special control register
- Wakeup reset: Reset signal generated when the system wake up from the SLEEP mode

Hardware reset

The hardware reset is invoked when the nRESET pin is asserted and all units in the system (except RTC) are reset to known states. During the hardware reset, the following actions occur:

- All internal registers and ARM926EJ-S core go to their pre-defined reset state.
- All pins get their reset state, and nBATT_FLT pin is ignored.
- nRSTOUT pin is asserted when nRESET is asserted.

The hardware reset is invoked when an external source drives the nRESET input pin low. nRESET is un-maskable and is always enabled. Upon assertion of nRESET, S3C2413 enters into reset state regardless of the previous mode. To enter hardware reset, nRESET must be held long enough to allow internal stabilization and propagation of the reset state.

Caution: Power regulator for system must be stable prior to the deassertion of nRESET. Otherwise, it damages to S3C2413x and its operation is not guaranteed.

Watchdog reset

Watchdog reset is invoked when software fails to prevent the watchdog timer from timing out. During the watchdog reset, the following actions occur:

- All units(except alive part) go to their pre-defined reset state.
- All pins get their reset state, and nBATT_FLT is ignored.
- The nRSTOUT pin is asserted during watchdog reset.

Watchdog reset can be activated in NORMAL and IDLE mode because watchdog timer can expire with clock. It is invoked when watchdog timer and reset are enabled and watchdog timer is expired. Then, the following sequence occurs:

1. Watchdog reset source asserts
2. System controller requests bus controller to finish current transactions.
3. Bus controller sends acknowledge to system controller after completed bus transactions.
4. System controller requests memory controller to enter into self-refresh mode.
5. System controller wait for self-refresh acknowledge from memory controller.
6. Internal reset signals and nRSTOUT are asserted and reset counter is activated.
7. Reset counter is expired and then internal reset signals and nRSTOUT are deasserted.

Software reset

Software reset is invoked when CPU write “0x533C_2412” to SWRSTCON register. The behavior is same to watchdog reset case.

Wakeup reset

Wakeup reset is invoked when the system is woken up from SLEEP mode by wakeup event. The details are described in the following section.

POWER MANAGEMENT

The power management block controls the system clocks by software for the reduction of power consumption in the S3C2413A. These schemes are related to PLL, clock control logics (ARMCLK, HCLK, and PCLK) and wakeup signals.

The S3C2413A has four power modes as shown in Figure 6-4. The following section describes each power management mode. The transition between the modes is not allowed freely.

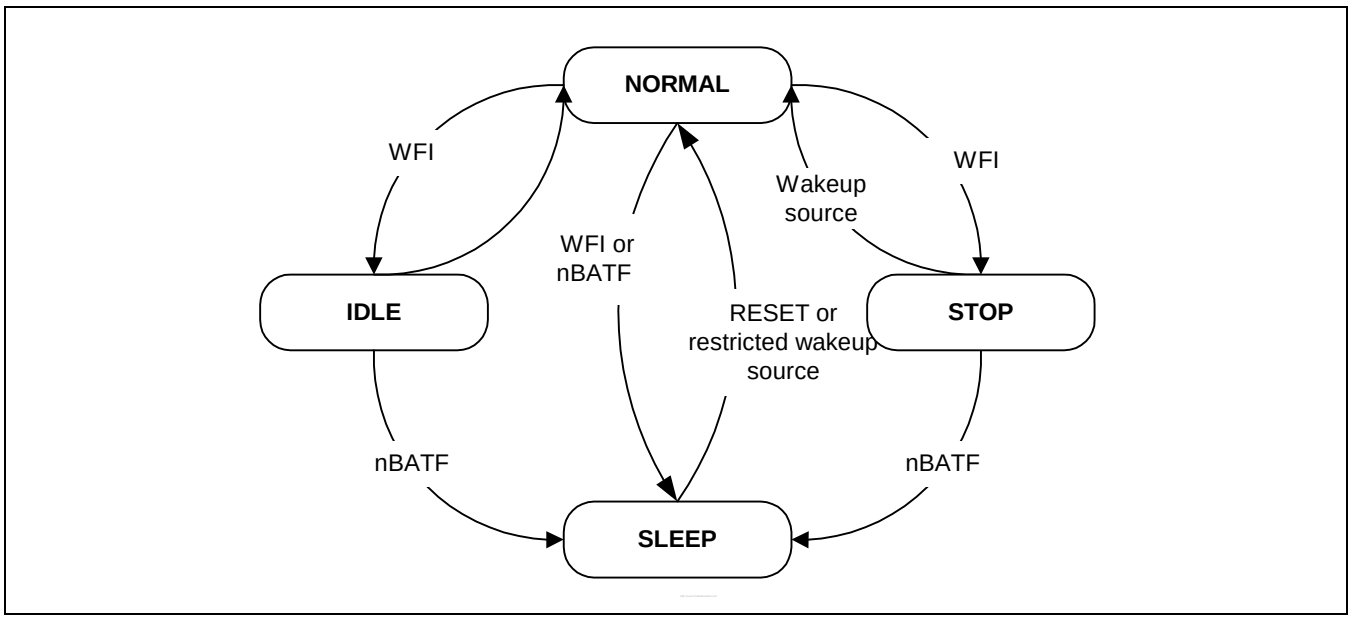


Figure 6-4. The power mode state diagram

NORMAL Mode

In normal mode, all peripherals and the basic blocks including power management block, the CPU core, the bus controller, the memory controller, the interrupt controller, DMA, and the external master may operate fully. However, the clock to each peripheral, except the basic blocks, can be stopped selectively by software to reduce the power consumption.

The ON/OFF clock gating of the individual clock source of each IP block is performed by controlling of each corresponding clock enable bit. The clock gating is applied instantly whenever the corresponding bit (or bits) is changed. (In general, these bits are set or cleared by the main CPU).

IDLE Mode

In IDLE mode, the clock to the CPU core is stopped except the bus controller, the memory controller, the interrupt controller, and the power management block. To exit the IDLE mode, EINT[23:0], or RTC alarm interrupt, or the other interrupts should be activated. (EINT is not available until GPIO block is turned on).

STOP Mode

In STOP mode, all clocks are stopped for minimum power consumption. Therefore, the PLL and oscillator circuit are also stopped. The STOP mode is activated after the execution of the STORE instruction that enables the STOP mode bit. The STOP mode entering sequence is as follows:

1. Software program sets the STOP mode bit (in general by the main CPU) or generate STANDBYWFI signal by using special command.

   MCR p15, 0, Rd, c7, c0, 4
2. The system controller requests bus controller to finish current bus transaction.
3. The bus controller sends acknowledge to the system controller after the current bus transaction is completed.
4. The system controller requests memory controller to ender into self-refresh mode, since the contents in the external SDRAM must be preserved during the STOP mode.
5. The memory controller sends self-refresh acknowledge to the system controller.
6. The system controller disables system clocks, and changes MSYSCLK's source to MPLL reference clock.
7. The system controller disables PLLs and the crystal oscillator (XTIpll).

To exit from the STOP mode, external interrupt, RTC alarm, nRESET must be activated. During the wake-up sequence from the STOP mode, the crystal oscillator and PLL may begin to operate according to the previous configuration. The crystal oscillator settle-down time and the PLL locking-time are required to provide stabilized MSYSCLK. Those time-waits are automatically inserted by the hardware of the S3C2413x. During these time-waits, the clock is not supplied to the internal logic. The STOP mode exiting sequence is as follows:

1. Enable crystal oscillator if it is used, and wait the OSC settle-down (around 1ms)
2. After the oscillator settle-down, the oscillator clock is fed using the PLL input clock and also enables the PLLs and waits the PLL locking time.
3. Change the clock source if the PLL is the clock source of the system clock.

SLEEP Mode

In the SLEEP mode, all the clock sources are off and the internal logic-power is not supplied except for the wake-up logic circuitry. In this mode, the static power dissipation of internal logic can be minimized. The SLEEP mode entering sequence is as follows:

1. The system software or hardware signal (nBATT_FLT) activates the SLEEP mode entering events.
2. The system controller requests bus controller to finish current bus transaction.
3. The bus controller sends acknowledge to the system controller after the current bus transaction is completed.
4. The system controller requests memory controller to ender into self-refresh mode, since the contents in the external SDRAM must be preserved during the STOP mode.
5. The memory controller sends self-refresh acknowledge to the system controller.
6. The system controller disables system clocks, and changes MSYSCLK's source to MPLL reference clock.
7. The system controller disables PLLs and the crystal oscillator (XTIpll).
8. Finally, the system controller disables the external power source for the internal logic by asserting the PWREN signal to the low state. The PWREN signal is the regulator-disable control signal for the internal-logic power-source.

The SLEEP mode exiting sequence is as follows:

1. Enable external power source by deactivation of the PWREN signal and wait power settle-down time (around 6ms, it is programmable by a register in the GPIO block).
2. Release the system reset (synchronously, relatively to the system clock) after the power supply is stabilized. (see the GPIO descriptions).
3. The remaining sequence is the same as the hardware reset sequence.

Wake-up events

The initial state of the S3C2413x after wake-up from the SLEEP mode is almost the same as the power-on-reset state except for the contents of the external DRAM is preserved. In contrast, the S3C2413x automatically recovers the previous working state after wake-up from the STOP mode.

The table 6-4 shows that the entering and exiting condition to change power management mode. In general, the entering conditions are set by the main CPU.

Power mode	Enter	Exit
IDLE	STANDBYWFI	All interrupt sources RTC alarm RTC TICK nRESET
STOP	STANDBYWFI	External interrupt (EINT[15:0]) RTC alarm RTC TICK nRESET
SLEEP	STANDBYWFI	External interrupt (EINT[15:0]) RTC alarm RTC TICK nRESET

Note) After wake-up from SLEEP mode by RTC alarm and RTC TICK, the corresponding source pending bits of SRCPND register are not set.

SYSTEM CONTROLLER SPECIAL REGISTERS

System controller block contains 19 special function registers. They control the output frequencies of the system controller and changes power mode to reduce the operating power. Their address map and information are summarized as follows:

Address	Register	R/W	Reset Value	Meaning
0x4C00_0000	LOCKTIME (note1)	R/W	0xFFFF_FFFF	MPLL/UPLL lock time counter register
0x4C00_0004	MPLLCON	R/W	0x0012_A011	MPLL configuration register
0x4C00_0008	UPLLCON	R/W	0x0014_0071	UPLL configuration register
0x4C00_000C	CLKCON	R/W	0x1FFF_FFFF	Clock generator control register
0x4C00_0010	RESERVED			
0x4C00_0014	CLKDIVN	R/W	0x0000_0024	Clock divider control register
0x4C00_0018	OSCSET (note1)	R/W	0x0000_8000	Oscillator stabilization time counter register
0x4C00_001C	CLKSRC	R/W	0x0000_0000	Clock source control register
0x4C00_0024	PWRCFG (note1)	R/W	0x0000_0000	Power management configuration register
0x4C00_002C	RESERVED			
0x4C00_0030	SWRSTCON	R/W	0x0000_0000	S/W reset control register
0x4C00_0034	RSTCON (note1)	R/W	0x0000_0101	Reset control register
0x4C00_0038~ 0x4C00_006C	RESERVED			
0x4C00_0070	INFORM0 (note1)	R/W	0x0000_0000	User defined information register
0x4C00_0074	INFORM1 (note1)	R/W	0x0000_0000	User defined information register
0x4C00_0078	INFORM2 (note1)	R/W	0x0000_0000	User defined information register
0x4C00_007C	INFORM3 (note1)	R/W	0x0000_0000	User defined information register

Note1: The value of these registers can be kept during sleep mode. In addition these can be reset by only nRESET.

LOCK TIME COUNT REGISTER (LOCKTIME)

Register	Address	R/W	Description	Reset Value
LOCKTIME	0x4C00_0000	R/W	MPLL/UPLL lock time count register	0xFFFF_FFFF

Conventional PLL requires stabilization duration after the PLL is on. The duration can be varied according to the device variation. Thus, SW must configure with an appropriate value in the LOCKTIME register whose value means the number of the external reference clock. The upper 16-bit of LOCKTIME controls UPLL and the lower 16-bit controls MPLL.

LOCKTIME	Bit	Description	Initial State
U_LTIME	[31:16]	UPLL lock time count value for UCLK. (U_LTIME > 150 usec)	0xFFFF
M_LTIME	[15:0]	MPLL lock time count value for ARMCLK, HCLK, and PCLK (M_LTIME > 150 usec)	0xFFFF

PLL CONTROL REGISTER (MPLLCON AND UPLLCON)

The output frequencies of each PLL can be calculated using the following equations:

$FOUT_{MPLL} = (2m \times FIN) / (p \times 2^{S})$

where, m = (MDIV + 8), p = (PDIV + 2), s = SDIV

$FOUT_{UPLL} = (m \times FIN) / (p \times 2^{S})$

where, m = (MDIV + 8), p = (PDIV + 2), s = SDIV

NOTE:

Although there is the equation for choosing PLL value, we recommend only the values in the PLL value recommendation table. If you have to use another value, please contact us.

Register	Address	R/W	Description	Reset Value
MPLLCON	0x4C00_0004	R/W	MPLL configuration register	0x0012_A011
UPLLCON	0x4C00_0008	R/W	UPLL configuration register	0x0014_0071

PLLCON	Bit	Description	Initial State
LOCKSTATUS	[31]	0: PLL is under LOCK Time, 1: LOCK Time is finished. This bit value is only valid after S/W set the ONOFF bit of PLLCON.	0 / 0
ONOFF	[20]	PLL on/off. 0: on, 1: off	1 / 1
MDIV	[19:12]	Main divider value	0x2A / 0x40
PDIV	[9:4]	Pre-divider value	0x01 / 0x07
SDIV	[1:0]	Post-divider value	0x1 / 0x1

CLOCK CONTROL REGISTERS (CLKCON, CLKDIVN AND CLKSRC)

Register	Address	R/W	Description	Reset Value
CLKCON	0x4C00_000C	R/W	Clock generator control register	0x1FFF_FFFF
CLKDIVN	0x4C00_0014	R/W	Clock divider control register	0x0000_0024
CLKSRC	0x4C00_001C	R/W	Clock source control register	0x0000_0000

The CLKCON register enable and disable the input clock of internal functional blocks as follows:

CLKCON	Bit	Description	Initial State
WDT	[28]	Enable/disable PCLK into watchdog timer 0 : disable 1 : enable	1
SPI	[27]	Enable/disable PCLK into SPI block 0 : disable 1 : enable	1
I2S	[26]	Enable/disable PCLK into I2S block 0 : disable 1 : enable	1
I2C	[25]	Enable/disable PCLK into I2C block 0 : disable 1 : enable	1
ADC	[24]	Enable/disable PCLK into ADC block 0 : disable 1 : enable	1
RTC	[23]	Enable/disable PCLK into RTC block 0 : disable 1 : enable	1
GPIO	[22]	Enable/disable PCLK into GPIO block 0 : disable 1 : enable	1
UART	[21:19]	Enable/disable PCLK into UART channel 0~2 0 : disable 1 : enable	0x7
SDI	[18]	Enable/disable PCLK into SDI block 0 : disable 1 : enable	1
PWM	[17]	Enable/disable PCLK into PWM timer block 0 : disable 1 : enable	1
USBD	[16]	Enable/disable PCLK into USB device interface block 0 : disable 1 : enable	1
CAMCLK	[15]	Enable/disable CAMERA clock 0 : disable 1 : enable	1
UARTCLK	[14]	Enable/disable UART clock 0 : disable 1 : enable	1
I2SCLK	[13]	Enable/disable audio CODE clock into I2S block 0 : disable 1 : enable	1
USBH48M	[12]	Enable/disable 48MHz clock into USB host interface block 0 : disable 1 : enable	1
USBD48M	[11]	Enable/disable 48MHz clock into USB device interface block 0 : disable 1 : enable	1
HCLKx1_2	[10]	Enable/disable HCLK / 2 clock into memory controller block	1

		0 : disable 1 : enable	
HCLKx2	[9]	Enable/disable HCLK x 2 clock into memory controller block 0 : disable 1 : enable	1
SDRAM	[8]	Enable/disable HCLK into memory controller block 0 : disable 1 : enable	1
USBH	[6]	Enable/disable HCLK into USB host interface block 0 : disable 1 : enable	1
LCDC	[5]	Enable/disable HCLK into LCD controller block 0 : disable 1 : enable	1
NFC	[4]	Enable/disable HCLK into NAND flash controller block 0 : disable 1 : enable	1
DMA	[3:0]	Enable/disable HCLK into DMA channel 0~3 0 : disable 1 : enable	0xF

Note. Before entering Stop / Sleep Mode, must be enable UARTCLK , I2SCLK HCLKx1_2, HCLKx2 and SDRAM.

The CLKDIVN register controls the output frequency of clock generator. Some blocks in the devices require several operating frequencies, i.e., 48MHz and 24MHz for USB interface block. Thus, the output frequencies can control using the CLKDIVN values. The operating speed of ARM can be slow to reduce the overall power dissipation, if a software does not require to utilize the processor performance. In this case, the power dissipation due to ARM processor can be reduced if the DVS field is on. This makes that the operating frequency of ARM is the same as system operating clock (HCLK).

CLKDIVN	Bit	Description	Initial State
CAMCLKDIV	[19:16]	CAM clock divider ratio. ratio = (CAMCLKDIV + 1)	0x0
I2SCLKDIV	[15:12]	I2S clock divider ratio. ratio = (I2SCLKDIV + 1)	0x0
UARTCLKDIV	[11:8]	UART clock divider ratio. ratio = (UARTCLKDIV + 1)	0x0
USB48DIV	[6]	48MHz clock divider ratio. (input clock for USB host/device block) 0 = (48MHz clock source), 1 = (48MHz clock source / 2)	0
HALFHCLK	[5]	HCLK clock divider for SSMC, 0 = HCLK, 1 = HCLK / 2	1
DVS	[4]	Enable/disable DVS (Dynamic Voltage Scaling) feature. 0 = disable 1 = enable (ARMCLK = HCLK)	0
ARMDIV	[3]	ARM clock divider ratio 0 = (system clock source), 1 = (system clock source / 2)	0
PCLKDIV	[2]	PCLK clock divider ratio. 0 = HCLK, 1 = HCLK / 2	1
HCLKDIV	[1:0]	HCLK clock divider ratio. ratio = (ARMDIV + 1) * (HCLKDIV + 1)	0x0

CLKSRC	Bit	Description	Initial State
SELEREF	[15:14]	EREFCLK selection 00 = OM[4], 10 = external oscillator, 11 = external clock	0x0
SELUREF	[13:12]	UREFCLK source selection 00 = OM[4], 10 = external oscillator, 11 = external clock	0x0
SELCAM	[11]	CAMSRCCLK source selection 0 = USYSCLK, 1= HCLK	0
SELUSB	[10]	USBSRCCLK source selection 0 = USYSCLK, 1 = HCLK	0
SELI2S	[9]	I2SSYSCLK source selection 0 = EREFCLK, 1 = $FOUT_{MPLL}$	0
SELUART	[8]	UARTSYSCLK source selection 0 = EREFCLK, 1 = $FOUT_{MPLL}$	0
SELUPLL	[5]	USYSCLK selection 0 = FIN_{UPLL}(=UREFCLK), 1 = $FOUT_{UPLL}$	0
SELMPLL	[4]	MSYSCLK selection 0 = MDIVCLK, 1 = $FOUT_{MPLL}$	0
SELEXTDIV	[3]	MDIVCLK selection 0 = MREFCLK, 1 = Divided clock by EXTCLKDIV ratio	0
EXTCLKDIV	[2:0]	External clock divider ratio. ratio = 2*EXTCLKDIV	0x0

NOTE: All clock names of CLKSRC register are denoted in Figure 6-1.

OSCILLATOR STABILIZATION CONTROL REGISTER (OSCSET)

Register	Address	R/W	Description	Reset Value
OSCSET	0x4C00_0018	R/W	Oscillator stabilization control register	0x0000_8000

Conventional oscillator requires stabilization duration after power is on. This register specify the duration based on the reference clock.

OSCSET	Bit	Description	Initial State
XTALWAIT	[15:0]	Crystal oscillator settle-down wait time	0x8000

POWER MANAGEMENT REGISTERS (PWRCFG)

Register	Address	R/W	Description	Reset Value
PWRCFG	0x4C00_0024	R/W	Power management configuration register	0x0000_0000

S3C2413 consists of three power-down modes, which are IDLE, STOP, and SLEEP.The PWRCFG register controls the source of power mode transition.

PWRCFG	Bit	Description	Initial State
EINT_WAKE_ MASK	[31:16]	Configure external interrupt wake-up mask. 0: after nBATT_FLT goes high, wakeup signal is generated. 1: mask external interrupt wakeup event during battery fault.	0x0000
RESERVED	[15]	RESERVED	0
NFRESET_CFG	[9]	Reset configuration when internal reset is generated. 0: reset NAND flash controller when software reset occurs. 1: do not reset NAND flash controller when software reset, watch dog reset occurs.	0
RTC_CFG	[8]	Configure RTC alarm and TICK interrupt wakeup mask 0: wakeup signal event is generated when RTC alarm occurs. 1: mask RTC alarm interrupt	0
STANDBYWFI	[7:6]	Configure the signal, STANDBYWFI of ARM. 00: ignore, 01: go IDLE mode 10: go STOP mode, 11: go SLEEP mode	0x0
BATF_CFG	[1:0]	Configure nBATT_FLT operation 00: Reserved 01: Generate Interrupt 10: Ignore 11: The system enters into SLEEP mode when nBATT_FLT is asserted.	0x0

RESET CONTROL REGISTERS (SWRSTCON AND RSTCON)

Register	Address	R/W	Description	Reset Value
SWRSTCON	0x4C00_0030	R/W	Software reset control register	0x0000_0000
RSTCON	0x4C00_0034	R/W	Reset control register	0x0000_0101

When a software write the predefined value, 0x533C2412, into SWRSTCON register, then the system controller asserts internal reset signal. The 0x533C2412 means the device family name, S3C2413 (S3C2411, S3C2412), since ‘S’ character has 0x53 in ASCII.

SWRSTCON	Bit	Description	Initial State
SWRST	[31:0]	If this field has 0x533C2412, then the system will restart. The pattern, “0x533C2412”, means the device family name.	0x0000_0000

RSTCON register controls the duration of the system reset signal.

RSTCON	Bit	Description	Initial State
RSTCNT	[15:8]	Force internal reset and nRSTOUT signal active until counter reaches to this bit value (EXTCLKxRSTCON[15:8])when software and watchdog reset is intiated.	0x01
PWRSETCNT	[7:0]	Force internal reset and nRSTOUT signal active until counter reaches to this bit value (EXTCLKx2048xRSTCON[7:0]) when waking-up from sleep mode	0x01

MISCELLANEOUS REGISTERS (INFORM0~3)

Register	Address	R/W	Description	Reset Value
INFORM0	0x4C00_0070	R/W	User defined information register 0	0x0000_0000
INFORM1	0x4C00_0074	R/W	User defined information register 1	0x0000_0000
INFORM2	0x4C00_0078	R/W	User defined information register 2	0x0000_0000
INFORM3	0x4C00_007C	R/W	User defined information register 3	0x0000_0000

ARM processor supports two endian schemes, which are the little-endian and the big-endian. Endian mode can be selected using CP15, control register r1. Refer to ARM926EJ-S TRM.

In some application program, several important data need to be reserved during SLEEP mode. S3C2413 supports four-word register to meet this requirement. The values of INFORM0~3 are reserved during SLEEP mode.

INFORM 0~3	Bit	Description	Initial State
DATA	[31:0]	This field contains a user specific word data and sustains the contents during SLEEP mode.	0

7 DMA CONTROLLER

OVERVIEW

S3C2413X supports four-channel DMA (Bridge DMA or peripheral DMA) controller that is located between the system bus and the peripheral bus. Each channel of DMA controller can perform data movements between devices in the system bus and/or peripheral bus with no restrictions. In other words, each channel can handle the following four cases: 1) both source and destination are in the system bus, 2) source is in the system bus while destination is in the peripheral bus, 3) source is in the peripheral bus while destination is in the system bus, 4) both source and destination are in the peripheral bus.

The main advantage of DMA is that it can transfer the data without CPU intervention. The operation of DMA can be initiated by S/W, or the request from internal peripherals, or the external request pins.

DMA REQUEST SOURCES

Each channel of DMA controller can select one source among twenty-five DMA sources if H/W DMA request mode is selected by REQSEL register. (Note that if S/W request mode is selected, this DMA request sources have no meaning at all.) The twenty-five DMA sources for each channel are as follows.

Table 7-1. DMA request sources for each channel

Bit	Source	Bit	Source	Bit	Source	Bit	Source
0	SPI_0_TX	8	Reserved	16	USB device EP4	24	UART_2[1]*
1	SPI_0_RX	9	PWM Timer	17	nXDREQ0	25	Reserved
2	SPI_1_TX	10	SDMMC	18	nXDREQ1	26	Reserved
3	SPI_1_RX	11	Reserved	19	UART_0[0]*	27	Reserved
4	I2S TX	12	Reserved	20	UART_0[1]*	28	Reserved
5	I2S RX	13	USB device EP1	21	UART_1[0]*	29	Reserved
6	Reserved	14	USB device EP2	22	UART_1[1]*	30	Reserved
7	Reserved	15	USB device EP3	23	UART_2[0]*	31	Reserved

Here, nXDREQ0 and nXDREQ1 represent two external sources (External Devices).

Note(*): See the page 10-12 for additional information.

DMA OPERATION

The details of DMA operation can be explained using three-state FSM(finite state machine) as follows:

State-1. As an initial state, it waits for the DMA request. If it comes, go to state-2. At this state, DMA ACK and INT REQ are 0.

State-2. In this state, DMA ACK becomes 1 and the counter(CURR_TC) is loaded from DCON[19:0] register. Note that DMA ACK becomes 1 and remains 1 until it is cleared later.

State-3. In this state, sub-FSM handling the atomic operation of DMA is initiated. The sub-FSM reads the data from the source address and then writes it to destination address. In this operation, data size and transfer size (single or burst) are considered. This operation is repeated until the counter(CURR_TC) becomes 0 in the whole service mode, while performed only once in a single service mode. The main FSM (this FSM) counts down the CURR_TC when the sub-FSM finishes each of atomic operation. In addition, this main FSM asserts the INT REQ signal when CURR_TC becomes 0 and the interrupt setting of DCON [28] register is set to 1. In addition, it clears DMA ACK if one of the following conditions is met.
1) CURR_TC becomes 0 in the whole service mode
2) atomic operation finishes in the single service mode.

Note that in the single service mode, these three states of main FSM are performed and then stops, and wait for another DMA REQ. And if DMA REQ comes in all three states are repeated. Therefore, DMA ACK is asserted and then de-asserted for each atomic transfer. In contrast, in the whole service mode, main FSM waits at state-3 until CURR_TC becomes 0. Therefore, DMA ACK is asserted during all the transfers and then de-asserted when TC reaches 0.

However, INT REQ is asserted only if CURR_TC becomes 0 regardless of the service mode (single service mode or whole service mode).

EXTERNAL DMA DREQ/DACK PROTOCOL

There are four types of external DMA request/acknowledge protocols. Each type defines how the signals like DMA request and acknowledge are related to these protocols.

Basic DMA Timing

The DMA service means paired Reads and Writes cycles during DMA operation, which is one DMA operation. The Fig. 7-1 shows the basic Timing in the DMA operation of the S3C2413X.

- The setup time and the delay time of XnXDREQ and XnXDACK are same in all the modes.
- If the completion of XnXDREQ meets its setup time, it is synchronized twice and then XnXDACK is asserted.
- After assertion of XnXDACK, DMA requests the bus and if it gets the bus it performs its operations. XnXDACK is deasserted when DMA operation finishes.

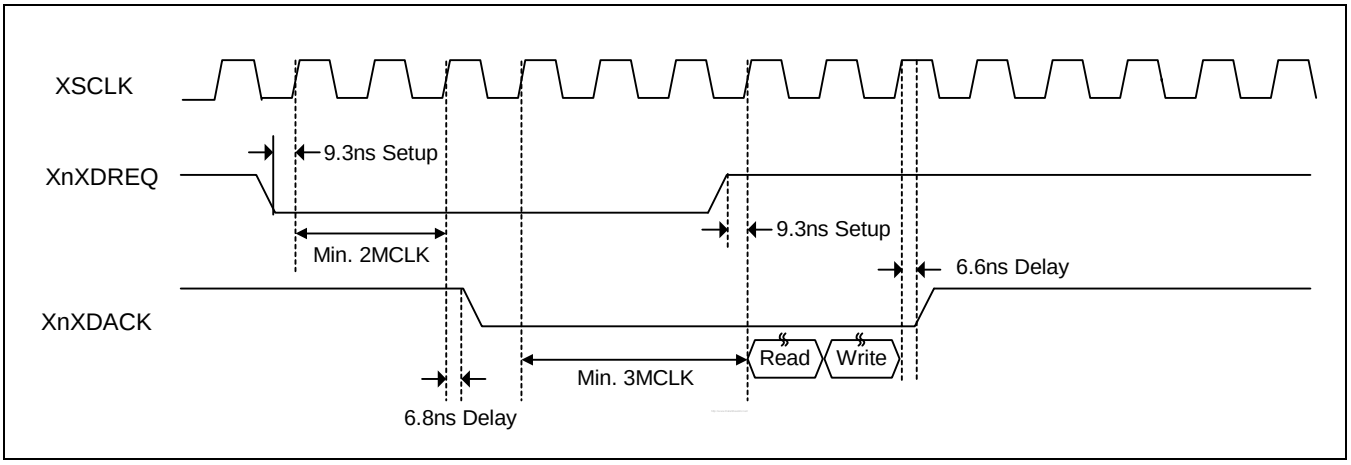


Figure 7-1. Basic DMA Timing Diagram

Demand/Handshake Mode Comparison – Related to the Protocol between XnXDREQ and XnXDACK

These are two different modes related to the protocol between XnXDREQ and XnXDACK. Fig. 7-2 shows the differences between these two modes i.e., Demand and Handshake modes.

At the end of one transfer (Single/Burst transfer), DMA checks the state of double-synched XnXDREQ.

Demand mode

- If XnXDREQ remains asserted, the next transfer starts immediately. Otherwise it waits for XnXDREQ to be asserted.

Handshake mode

- If XnXDREQ is deasserted, DMA deasserts XnXDACK in 2cycles. Otherwise it waits until XnXDREQ is deasserted.

  Caution: XnXDREQ has to be asserted (low) only after the deassertion(high) of XnXDACK.

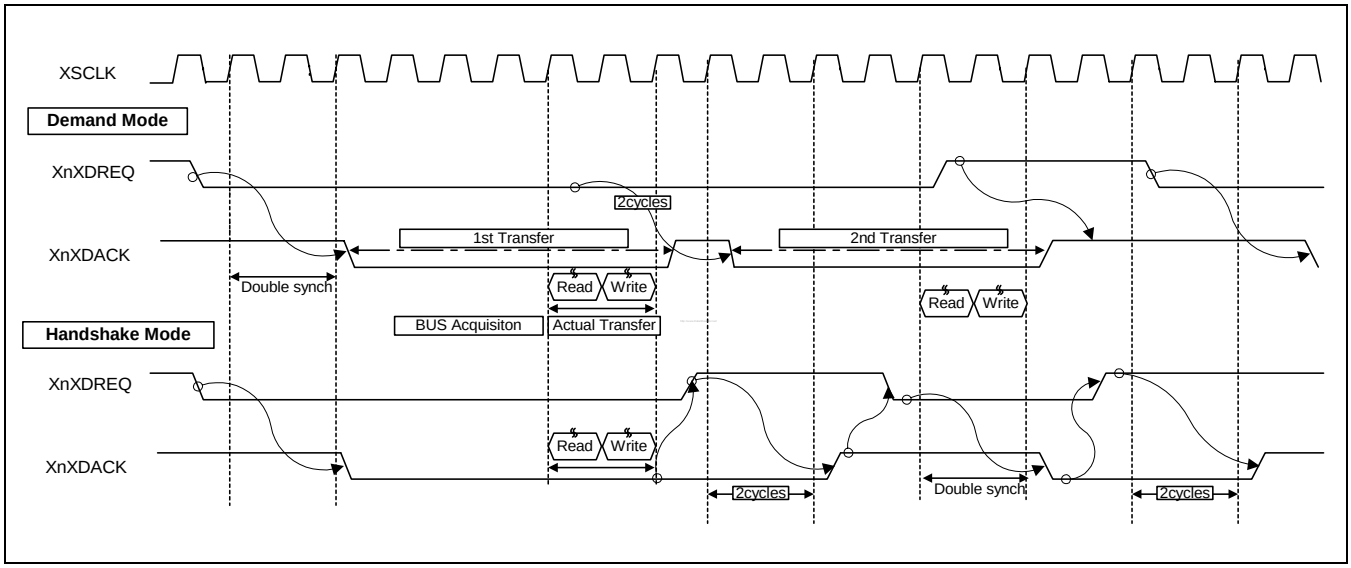


Figure 7-2. Demand/Handshake Mode Comparison

TRANSFER SIZE

- There are two different transfer sizes; single and Burst 4.
- DMA holds the bus firmly during the transfer of these chunk of data, thus other bus masters can not get the bus.

Burst 4 Transfer Size

4 sequential Reads and 4 sequential Writes are performed in the Burst 4 Transfer.

* NOTE: Single Transfer size: One read and one write are performed.

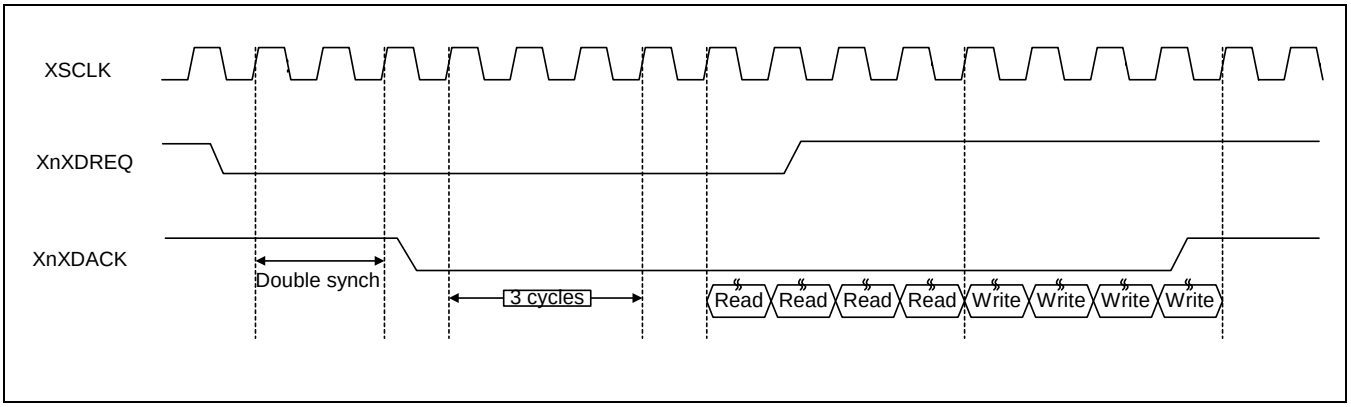


Figure 7-3. Burst 4 Transfer size

EXAMPLES OF POSSIBLE CASES

Single service, Demand Mode, Single Transfer Size

The assertion of XnXDREQ is need for every unit transfer (Single service mode), the operation continues while the XnXDREQ is asserted(Demand mode), and one pair of Read and Write(Single transfer size) is performed.

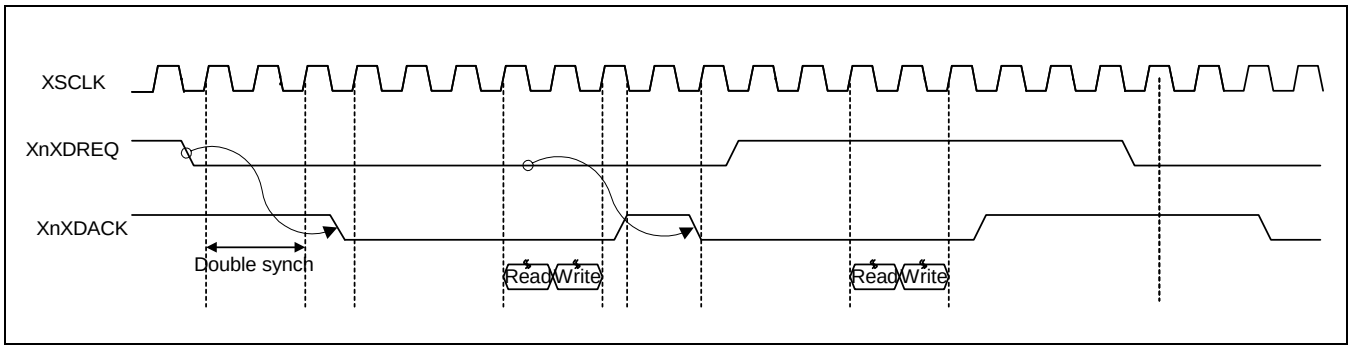


Figure 7-4. Single service, Demand Mode, Single Transfer Size

Single service/Handshake Mode, Single Transfer Size

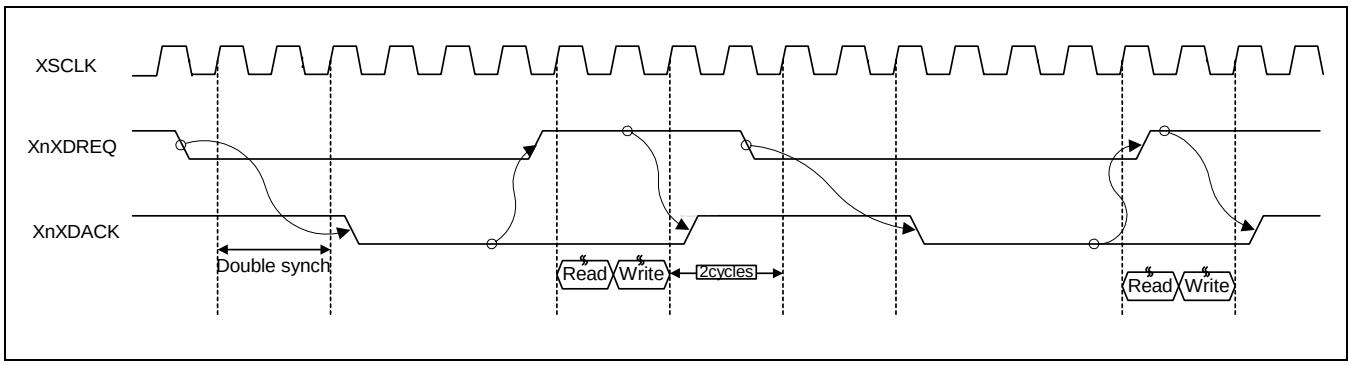


Figure 7-5. Single service, Handshake Mode, Single Transfer Size

Whole service/Handshake Mode, Single Transfer Size

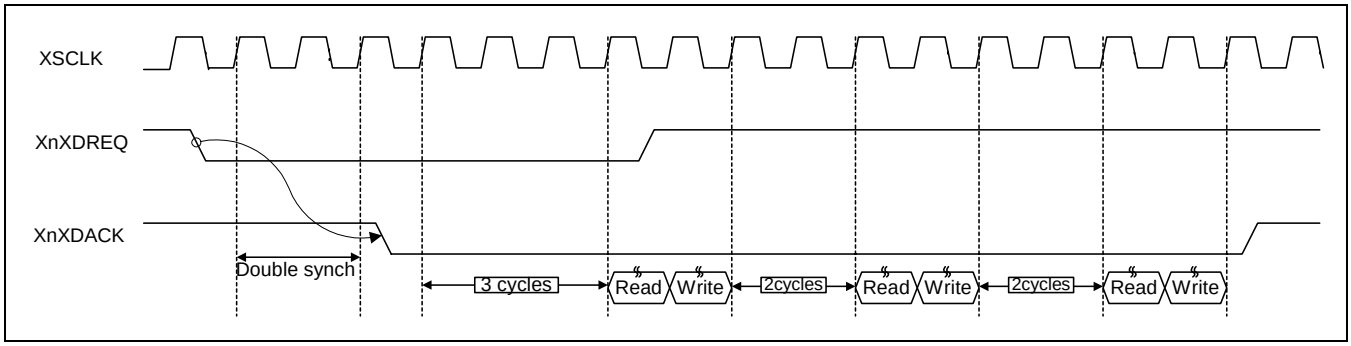


Figure 7-6. Whole service, Handshake Mode, Single Transfer Size

DMA SPECIAL REGISTERS

There are seven control registers for each DMA channel. (Since there are four channels, the total number of control registers is 28.) Four of them are to control the DMA transfer, and other three are to see the status of DMA controller. The details of those registers are as follows.

DMA INITIAL SOURCE REGISTER (DISRC)

Register	Address	R/W	Description	Reset Value
DISRC0	0x4B000000	R/W	DMA0 Initial Source Register	0x00000000
DISRC1	0x4B000040	R/W	DMA1 Initial Source Register	0x00000000
DISRC2	0x4B000080	R/W	DMA2 Initial Source Register	0x00000000
DISRC3	0x4B0000C0	R/W	DMA3 Initial Source Register	0x00000000

DISRCn	Bit	Description	Initial State
S_ADDR	[30:0]	These bits are the base address (start address) of source data to transfer. This value will be loaded into CURR_SRC only if the CURR_SRC is 0 and the DMA ACK is 1.	0x00000000

DMA INITIAL SOURCE CONTROL REGISTER (DISRCC)

Register	Address	R/W	Description	Reset Value
DISRCC0	0x4B000004	R/W	DMA0 Initial Source Control Register	0x00000000
DISRCC1	0x4B000044	R/W	DMA1 Initial Source Control Register	0x00000000
DISRCC2	0x4B000084	R/W	DMA2 Initial Source Control Register	0x00000000
DISRCC3	0x4B0000C4	R/W	DMA3 Initial Source Control Register	0x00000000

DISRCn	Bit	Description	Initial State
LOC	[1]	Bit 1 is used to select the location of source. 0: the source is in the system bus (AHB), 1: the source is in the peripheral bus (APB)	0
INC	[0]	Bit 0 is used to select the address increment. 0 = Increment 1= Fixed If it is 0, the address is increased by its data size after each transfer in burst and single transfer mode. If it is 1, the address is not changed after the transfer (In the burst mode, address is increased during the burst transfer, but the address is recovered to its first value after the transfer).	0

DMA INITIAL DESTINATION REGISTER (DIDST)

Register	Address	R/W	Description	Reset Value
DIDST0	0x4B000008	R/W	DMA0 Initial Destination Register	0x00000000
DIDST1	0x4B000048	R/W	DMA1 Initial Destination Register	0x00000000
DIDST2	0x4B000088	R/W	DMA2 Initial Destination Register	0x00000000
DIDST3	0x4B0000C0	R/W	DMA3 Initial Destination Register	0x00000000

DIDSTn	Bit	Description	Initial State
D_ADDR	[30:0]	These bits are the base address (start address) of destination for the transfer. This value will be loaded into CURR_DST only if the CURR_DST is 0 and the DMA ACK is 1.	0x00000000

DMA INITIAL DESTINATION CONTROL REGISTER (DIDSTC)

Register	Address	R/W	Description	Reset Value
DIDSTC0	0x4B00000C	R/W	DMA0 Initial Destination Control Register	0x00000000
DIDSTC1	0x4B00004C	R/W	DMA1 Initial Destination Control Register	0x00000000
DIDSTC2	0x4B00008C	R/W	DMA2 Initial Destination Control Register	0x00000000
DIDSTC3	0x4B0000CC	R/W	DMA3 Initial Destination Control Register	0x00000000

DIDSTn	Bit	Description	Initial State
CHK_INT	[2]	Select interrupt occurrence time when auto-reload is setting. 0: Interrupt will occur when TC reaches 0. 1: Interrupt will occur after auto-reload is performed. **Note** In case of H/W request mode, interrupt can occur when TC reaches 0 or after auto-reload is complete according to CHK_INT setting value. But, S/W request mode supports interrupt occurrence only when TC reaches 0. So, DIDSTCn[2] should be '0' in the S/W request mode.	0
LOC	[1]	Bit 1 is used to select the location of destination. 0: the destination is in the system bus (AHB). 1: the destination is in the peripheral bus (APB).	0
INC	[0]	Bit 0 is used to select the address increment. 0 = Increment 1= Fixed If it is 0, the address is increased by its data size after each transfer in burst and single transfer mode. If it is 1, the address is not changed after the transfer (In the burst mode, address is increased during the burst transfer, but the address is recovered to its first value after the transfer).	0

DMA CONTROL REGISTER (DCON)

Register	Address	R/W	Description	Reset Value
DCON0	0x4B000010	R/W	DMA0 Control Register	0x00000000
DCON1	0x4B000050	R/W	DMA1 Control Register	0x00000000
DCON2	0x4B000090	R/W	DMA2 Control Register	0x00000000
DCON3	0x4B0000D0	R/W	DMA3 Control Register	0x00000000

DCONn	Bit	Description	Initial State
DMD_HS	[31]	Select one between demand mode and handshake mode. 0 : demand mode is selected 1 : handshake mode is selected. In both modes, DMA controller starts its transfer and asserts DACK for a given asserted DREQ. The difference between two modes is whether it waits for the de-asserted DACK or not. In handshake mode, DMA controller waits for the de-asserted DREQ before starting a new transfer. If it sees the de-asserted DREQ, it de-asserts DACK and waits for another asserted DREQ. In contrast, in the demand mode, DMA controller does not wait until the DREQ is de-asserted. It just de-asserts DACK and then starts another transfer if DREQ is asserted. We recommend using handshake mode for external DMA request sources to prevent unintended starts of new transfers.	0
SYNC	[30]	Select DREQ/DACK synchronization. 0: DREQ and DACK are synchronized to PCLK (APB clock). 1: DREQ and DACK are synchronized to HCLK (AHB clock). Therefore, devices attached to AHB system bus, this bit has to be set to 1, while those attached to APB system, it should be set to 0. For the devices attached to external system, user should select this bit depending on whether the external system is synchronized with AHB system or APB system.	0
INT	[29]	Enable/Disable the interrupt setting for CURR_TC(terminal count) 0: CURR_TC interrupt is disabled. user has to look the transfer count in the status register. (i.e., polling) 1: interrupt request is generated when all the transfer is done (i.e., CURR_TC becomes 0).	0
TSZ	[28]	Select the transfer size of an atomic transfer (i.e., transfer performed at each time DMA owns the bus before releasing the bus). 0: a unit transfer is performed. 1: a burst transfer of length four is performed.	0

DCONn	Bit	Description	Initial State
SERVMODE	[27]	Select the service mode between single service mode and whole service mode. 0: single service mode is selected in which after each atomic transfer (single or burst of length four) DMA stops and waits for another DMA request. 1: whole service mode is selected in which one request gets atomic transfers to be repeated until the transfer count reaches to 0. In this mode, additional request is not required. Here, note that even in the whole service mode, DMA releases the bus after each atomic transfer and then tries to re-get the bus to prevent starving of other bus masters.	0
Reserved	[26:25]	Reserved for future use	0000
PADDRFIX	[24]	Select the APB address not increment when burst 4 mode 0 : increment APB address out when burst 4 mode 1 : fixed APB address out when burst 4 mode	0
Reserved	[23]	Reserved for future use	0
RELOAD	[22]	Set the reload on/off option. 0: auto reload is performed when a current value of transfer count becomes 0 (i.e., all the required transfers are performed). 1: DMA channel (DMA REQ) is turned off when a current value of transfer count becomes 0. The channel on/off bit(DMASKTRIGn[1]) is set to 0(DREQ off) to prevent unintended further start of new DMA operation	0
DSZ	[21:20]	Data size to be transferred. 00 = Byte 01 = Half word 10 = Word 11 = reserved	00
TC	[19:0]	Initial transfer count (or transfer beat). Note that the actual number of bytes that are transferred is computed by the following equation: DSZ x TSZ x TC, where DSZ, TSZ, and TC represent data size (DCONn[21:20]), transfer size (DCONn[28]), and initial transfer count, respectively. This value will be loaded into CURR_TC only if the CURR_TC is 0 and the DMA ACK is 1.	00000

DMA STATUS REGISTER (DSTAT)

Register	Address	R/W	Description	Reset Value
DSTAT0	0x4B000014	R	DMA0 Count Register	000000h
DSTAT1	0x4B000054	R	DMA1 Count Register	000000h
DSTAT2	0x4B000094	R	DMA2 Count Register	000000h
DSTAT3	0x4B0000D4	R	DMA3 Count Register	000000h

DSTATn	Bit	Description	Initial State
STAT	[21:20]	Status of this DMA controller. 00: It indicates that DMA controller is ready for another DMA request. 01: It indicates that DMA controller is busy for transfers.	00b
CURR_TC	[19:0]	Current value of transfer count. Note that transfer count is initially set to the value of DCONn[19:0] register and decreased by one at the end of every atomic transfer.	00000h

DMA CURRENT SOURCE REGISTER (DCSRC)

Register	Address	R/W	Description	Reset Value
DCSRC0	0x4B000018	R	DMA0 Current Source Register	0x00000000
DCSRC1	0x4B000058	R	DMA1 Current Source Register	0x00000000
DCSRC2	0x4B000098	R	DMA2 Current Source Register	0x00000000
DCSRC3	0x4B0000D8	R	DMA3 Current Source Register	0x00000000

DCSRCn	Bit	Description	Initial State
CURR_SRC	[30:0]	Current source address for DMAn.	0x00000000

CURRENT DESTINATION REGISTER (DCDST)

Register	Address	R/W	Description	Reset Value
DCDST0	0x4B00001c	R	DMA0 Current Destination Register	0x00000000
DCDST1	0x4B00005c	R	DMA1 Current Destination Register	0x00000000
DCDST2	0x4B00009c	R	DMA2 Current Destination Register	0x00000000
DCDST3	0x4B0000Dc	R	DMA3 Current Destination Register	0x00000000

DCDSTn	Bit	Description	Initial State
CURR_DST	[30:0]	Current destination address for DMAn.	0x00000000

DMA MASK TRIGGER REGISTER (DMASKTRIG)

Register	Address	R/W	Description	Reset Value
DMASKTRIG0	0x4B000020	R/W	DMA0 Mask Trigger Register	000
DMASKTRIG1	0x4B000060	R/W	DMA1 Mask Trigger Register	000
DMASKTRIG2	0x4B0000A0	R/W	DMA2 Mask Trigger Register	000
DMASKTRIG3	0x4B0000E0	R/W	DMA3 Mask Trigger Register	000

DMASKTRIGn	Bit	Description	Initial State
STOP	[2]	Stop the DMA operation. 1: DMA stops as soon as the current atomic transfer ends. If there is no current running atomic transfer, DMA stops immediately. The CURR_TC, CURR_SRC, CURR_DST will be 0. NOTE: Due to possible current atomic transfer, “stop” may take several cycles. The finish of “stopping” operation (i.e., actual stop time) can be detected by waiting until the channel on/off bit (DMASKTRIGn[1]) is set to off. This stop is “actual stop”.	0
ON_OFF	[1]	DMA channel on/off bit. 0: DMA channel is turned off. (DMA request to this channel is ignored.) 1: DMA channel is turned on and the DMA request is handled. This bit is automatically set to off if we set the DCONn[22] bit to “no auto reload” and/or STOP bit of DMASKTRIGn to “stop”. Note that when DCON [22] bit is "no auto reload", this bit becomes 0 when CURR_TC reaches 0. If the STOP bit is 1, this bit becomes 0 as soon as the current atomic transfer finishes. NOTE. This bit should not be changed manually during DMA operations (i.e., this has to be changed only by using DCON [22] or STOP bit.)	0
SW_TRIG	[0]	Trigger the DMA channel in S/W request mode. 1: it requests a DMA operation to this controller. However, note that for this trigger to have effects S/W request mode has to be selected (DMAREQSELn[0]) and channel ON_OFF bit has to be set to 1 (channel on). When DMA operation starts, this bit is cleared automatically.	0

NOTE: You can freely change the values of DISRC register, DIDST registers, and TC field of DCON register. Those changes take effect only after the finish of current transfer (i.e., when CURR_TC becomes 0). On the other hand, any change made to other registers and/or fields takes immediate effect. Therefore, be careful in changing those registers and fields.

DMA REQUESET SELECTION REGISTER (DMAREQSEL)

Register	Address	R/W	Description	Reset Value
DMAREQSEL0	0x4B000024	R/W	DMA0 Request Selection Register	000
DMAREQSEL1	0x4B000064	R/W	DMA1 Request Selection Register	000
DMAREQSEL2	0x4B0000A4	R/W	DMA2 Request Selection Register	000
DMAREQSEL3	0x4B0000E4	R/W	DMA3 Request Selection Register	000

DMAREQSELn	Bit	Description	Initial State
HWSRCSEL	[5:1]	Select DMA request source for each DMA. → Refer to the Table 7-1 on 7-2. This bits control the 8-1 MUX to select the DMA request source of each DMA. These bits have meanings if and only if H/W request mode is selected by DMAREQSELn[0].	00000
SWHW_SEL	[0]	Select the DMA source between software (S/W request mode) and hardware (H/W request mode). 0: S/W request mode is selected and DMA is triggered by setting SW_TRIG bit of DMASKTRIG control register. 1: DMA source selected by bit [5:1] is used to trigger the DMA operation.	0

NOTES

8 I/O PORTS

OVERVIEW

The S3C2413X has 129 multi-functional input/output port pins. The ports are:

- Port A (GPA): 23-output port
- Port B (GPB): 11-input/output port
- Port C (GPC): 15-input/output port
- Port D (GPD): 16-input/output port
- Port E (GPE): 16-input/output port
- Port F (GPF): 8-input/output port
- Port G (GPG): 16-input/output port
- Port H (GPH): 11-input/output port
- Port J (GPJ): 13-input/output port

Each port can be easily configured by software to meet various system configurations and design requirements. You have to define which function of each pin is used before starting the main program. If a pin is not used for multiplexed functions, the pin can be configured as I/O ports.

Initial pin states are configured seamlessly to avoid problems.

Table 8-1. S3C2413X Port Configuration

Port A	Selectable Pin Functions			
GPA22	Output only	SMAVD	–	–
GPA21	Output only	nRSTOUT	–	–
GPA20	Output only	nFRE	–	–
GPA19	Output only	nFWE	–	–
GPA18	Output only	ALE	–	–
GPA17	Output only	CLE	–	–
GPA16	Output only	nGCS5	–	–
GPA15	Output only	nGCS4	–	–
GPA14	Output only	nGCS3	–	–
GPA13	Output only	nGCS2	–	–
GPA12	Output only	nGCS1	–	–
GPA11	Output only	ADDR26	–	–
GPA10	Output only	ADDR25	–	–
GPA9	Output only	ADDR24	–	–
GPA8	Output only	ADDR23	–	–
GPA7	Output only	ADDR22	–	–
GPA6	Output only	ADDR21	–	–
GPA5	Output only	ADDR20	–	–
GPA4	Output only	ADDR19	–	–
GPA3	Output only	ADDR18	–	–
GPA2	Output only	ADDR17	–	–
GPA1	Output only	ADDR16	–	–
GPA0	Output only	ADDR0	–	–

Table 8-1. S3C2413X Port Configuration (Continued)

Port B	Selectable Pin Functions			
GPB10	Input/output	nXDREQ0	–	–
GPB9	Input/output	nXDACK0	–	–
GPB8	Input/output	nXDREQ1	–	–
GPB7	Input/output	nXDACK1	–	–
GPB6	Input/output	–	–	–
GPB5	Input/output	–	–	–
GPB4	Input/output	TCLK0	–	–
GPB3	Input/output	TOUT3	–	–
GPB2	Input/output	TOUT2	–	–
GPB1	Input/output	TOUT1	–	–
GPB0	Input/output	TOUT0	–	–

Port C	Selectable Pin Functions			
GPC15	Input/output	VD7	–	–
GPC14	Input/output	VD6	–	–
GPC13	Input/output	VD5	–	–
GPC12	Input/output	VD4	–	–
GPC11	Input/output	VD3	–	–
GPC10	Input/output	VD2	–	–
GPC9	Input/output	VD1	–	–
GPC8	Input/output	VD0	–	–
GPC7	Input/output	LCDVF2	–	–
GPC6	Input/output	LCDVF1	–	–
GPC5	Input/output	LCDVF0	–	–
GPC4	Input/output	VM	–	–
GPC3	Input/output	VFRAME	–	–
GPC2	Input/output	VLINE	–	–
GPC1	Input/output	VCLK	–	–
GPC0	–	–	–	–

Table 8-1. S3C2413X Port Configuration (Continued)

Port D	Selectable Pin Functions			
GPD15	Input/output	VD23	nSS0	–
GPD14	Input/output	VD22	nSS1	–
GPD13	Input/output	VD21	–	–
GPD12	Input/output	VD20	–	–
GPD11	Input/output	VD19	–	–
GPD10	Input/output	VD18	SPICLK1	–
GPD9	Input/output	VD17	SPIMOSI1	–
GPD8	Input/output	VD16	SPIMISO1	–
GPD7	Input/output	VD15	–	–
GPD6	Input/output	VD14	–	–
GPD5	Input/output	VD13	–	–
GPD4	Input/output	VD12	–	–
GPD3	Input/output	VD11	–	–
GPD2	Input/output	VD10	–	–
GPD1	Input/output	VD9	–	–
GPD0	Input/output	VD8	–	–

Port E	Selectable Pin Functions			
GPE15	Input	IICSDA	–	–
GPE14	Input	IICSCL	–	–
GPE13	Input/output	SPICLK0	–	–
GPE12	Input/output	SPIMOSI0	–	–
GPE11	Input/output	SPIMISO0	–	–
GPE10	Input/output	SDDAT3	–	–
GPE9	Input/output	SDDAT2	–	–
GPE8	Input/output	SDDAT1	–	–
GPE7	Input/output	SDDAT0	–	–
GPE6	Input/output	SDCMD	–	–
GPE5	Input/output	SDCLK	–	–
GPE4	Input/output	I2SSDO	I2SSDI	–
GPE3	Input/output	I2SSDI	nSS0	–
GPE2	Input/output	CDCLK	–	–
GPE1	Input/output	I2SSCLK	–	–
GPE0	Input/output	I2SLRCK	–	–

Table 8-1. S3C2413X Port Configuration (Continued)

Port F	Selectable Pin Functions			
GPF7	Input/output	EINT7	–	–
GPF6	Input/output	EINT6	–	–
GPF5	Input/output	EINT5	–	–
GPF4	Input/output	EINT4	–	–
GPF3	Input/output	EINT3	–	–
GPF2	Input/output	EINT2		
GPF1	Input/output	EINT1		
GPF0	Input/output	EINT0		

Port G	Selectable Pin Functions			
GPG15	Input/output	EINT23	–	–
GPG14	Input/output	EINT22	–	–
GPG13	Input/output	EINT21	–	–
GPG12	Input/output	EINT20	–	–
GPG11	Input/output	EINT19	TCLK1	–
GPG10	Input/output	EINT18	nCTS1	–
GPG9	Input/output	EINT17	nRTS1	–
GPG8	Input/output	EINT16	–	–
GPG7	Input/output	EINT15	SPICLK1	–
GPG6	Input/output	EINT14	SPIMOSI1	–
GPG5	Input/output	EINT13	SPIMISO1	–
GPG4	Input/output	EINT12	–	–
GPG3	Input/output	EINT11	nSS1	–
GPG2	Input/output	EINT10	nSS0	–
GPG1	Input/output	EINT9	ATA_NRESET	–
GPG0	Input/output	EINT8	ATA_INTRQ	–

Table 8-1. S3C2413X Port Configuration (Continued)

Port H	Selectable Pin Functions			
GPH10	Input/output	CLKOUT1	–	–
GPH9	Input/output	CLKOUT0	–	–
GPH8	Input/output	UEXTCLK	–	–
GPH7	Input/output	RXD2	nCTS1	–
GPH6	Input/output	TXD2	nRTS1	–
GPH5	Input/output	RXD1	–	–
GPH4	Input/output	TXD1	–	–
GPH3	Input/output	RXD0	–	–
GPH2	Input/output	TXD0	–	–
GPH1	Input/output	nRTS0	–	–
GPH0	Input/output	nCTS0	–	–

Port J	Selectable Pin Functions			
GPJ12	Input/output	CAMRESET	–	–
GPJ11	Input/output	CAMCLKOUT	–	–
GPJ10	Input/output	CAMHREF	–	–
GPJ9	Input/output	CAMVSYNC	–	–
GPJ8	Input/output	CAMPCLK	–	–
GPJ7	Input/output	CAMDATA7	–	–
GPJ6	Input/output	CAMDATA6	–	–
GPJ5	Input/output	CAMDATA5	–	–
GPJ4	Input/output	CAMDATA4	–	–
GPJ3	Input/output	CAMDATA3	–	–
GPJ2	Input/output	CAMDATA2	–	–
GPJ1	Input/output	CAMDATA1	–	–
GPJ0	Input/output	CAMDATA0	–	–

PORT CONTROL DESCRIPTIONS

PORT CONFIGURATION REGISTER (GPACON-GPJCON)

In the S3C2413X, most pins are multiplexed. So, It is require to determine which function is selected for each pin. port control register (PnCON) determines the function of each pin.

If GPF0 – GPF7 and GPG0 – GPG7 are used for wakeup signals in Power-OFF mode, these ports must be configured in Interrupt mode.

PORT DATA REGISTER (GPADAT-GPJDAT)

If ports are configured as output ports, data can be written to the corresponding bit of the PnDAT. If ports are configured as input ports, the data can be read from the corresponding bit of the PnDAT.

PORT PULL-DOWN REGISTER (GPBDN-GPJDN)

The port pull-down register controls the pull-down resister enable/disable of each port group. When the corresponding bit is 0, the pull-down resister of the pin is enabled. When 1, the pull-down resister is disabled.

If the port pull-down register is enabled, the pull-down resisters work without pin's functional setting (input, output, DATAn, EINTn, etc).

PORT SLEEP MODE CONTROL REGISTER (GPBSLPCON-GPJSLPCON)

MISCELLANEOUS CONTROL REGISTER

This register controls DATA port pull-up resister, hi-z state, USB pad, and CLKOUT selection.

EXTERNAL INTERRUPT CONTROL REGISTER (extintn)

The 24 external interrupts are requested by various signaling methods. The EXTINTn register configures the signaling method among the low level trigger, high level trigger, falling edge trigger, rising edge trigger, and both edge trigger for the external interrupt request.

Because each external interrupt pin has a digital filter, the interrupt controller can recognize the request signal that is longer than 3 clocks.

Only 16 EINT pins (EINT [15:0]) are used for wakeup sources.

I/O PORT CONTROL REGISTER

PORT A CONTROL REGISTERS (GPACON/GPADAT)

Register	Address	R/W	Description	Reset Value
GPACON	0x56000000	R/W	Configure the pins of port A	0x7FFFFF
GPADAT	0x56000004	R/W	The data register for port A	Undefined
Reserved	0x56000008	–	Reserved	Undefined
Reserved	0x5600000C	–	Reserved	Undefined

GPACON	Bit	Description	
GPA22	[22]	0 = Output	1 = SMAVD
GPA21	[21]	0 = Output	1 = nRSTOUT
GPA20	[20]	0 = Output	1 = nFRE
GPA19	[19]	0 = Output	1 = nFWE
GPA18	[18]	0 = Output	1 = ALE
GPA17	[17]	0 = Output	1 = CLE
GPA16	[16]	0 = Output	1 = nGCS5
GPA15	[15]	0 = Output	1 = nGCS4
GPA14	[14]	0 = Output	1 = nGCS3
GPA13	[13]	0 = Output	1 = nGCS2
GPA12	[12]	0 = Output	1 = nGCS1
GPA11	[11]	0 = Output	1 = ADDR26
GPA10	[10]	0 = Output	1 = ADDR25
GPA9	[9]	0 = Output	1 = ADDR24
GPA8	[8]	0 = Output	1 = ADDR23
GPA7	[7]	0 = Output	1 = ADDR22
GPA6	[6]	0 = Output	1 = ADDR21
GPA5	[5]	0 = Output	1 = ADDR20
GPA4	[4]	0 = Output	1 = ADDR19
GPA3	[3]	0 = Output	1 = ADDR18
GPA2	[2]	0 = Output	1 = ADDR17
GPA1	[1]	0 = Output	1 = ADDR16
GPA0	[0]	0 = Output	1 = ADDR0

NOTE: The GPA21 Power is depend on VDDOP, the other pads(GPA0~20, GPA22~24) are all on VDDMOP.

GPADAT	Bit	Description
GPA[22:0]	[22:0]	When the port is configured as output port, the pin state is the same as the that of the corresponding bit. When the port is configured as functional pin, undefined value will be read.

NOTE: nRSTOUT = HRESETn (nRESET | wakeup system bus reset | software reset | watchdog reset)

PORT B CONTROL REGISTERS (GPBCON, GPBDAT, and GPBDN)

Register	Address	R/W	Description	Reset Value
GPBCON	0x56000010	R/W	Configure the pins of port B	0x0
GPBDAT	0x56000014	R/W	The data register for port B	Undefined
GPBDN	0x56000018	R/W	Pull-down disable register for port B	0x0
GPBSLPCON	0x5600001C	R/W	Sleep mode configuration register for port B	0x0

GPBCON	Bit	Description
GPB10	[21:20]	00 = Input 01 = Output 10 = nXDREQ0 11 = reserved
GPB9	[19:18]	00 = Input 01 = Output 10 = nXDACK0 11 = reserved
GPB8	[17:16]	00 = Input 01 = Output 10 = nXDREQ1 11 = reserved
GPB7	[15:14]	00 = Input 01 = Output 10 = nXDACK1 11 = reserved
GPB6	[13:12]	00 = Input 01 = Output 10 = reserved 11 = reserved
GPB5	[11:10]	00 = Input 01 = Output 10 = reserved 11 = reserved
GPB4	[9:8]	00 = Input 01 = Output 10 = TCLK0 11 = reserved
GPB3	[7:6]	00 = Input 01 = Output 10 = TOUT3 11 = reserved
GPB2	[5:4]	00 = Input 01 = Output 10 = TOUT2 11 = reserved
GPB1	[3:2]	00 = Input 01 = Output 10 = TOUT1 11 = reserved
GPB0	[1:0]	00 = Input 01 = Output 10 = TOUT0 11 = reserved

GPBDAT	Bit	Description
GPB[10:0]	[10:0]	When the port is configured as input port, data from external sources can be read to the corresponding pin. When the port is configured as output port, data written in this register can be sent to the corresponding pin. When the port is configured as functional pin, undefined value will be read.

GPBDN	Bit	Description
GPB[10:0]	[10:0]	0: The pull-down function attached to to the corresponding port pin is enabled. 1: The pull-down function is disabled.

GPBSLPCON	Bit	Description	
GPB10	[21:20]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPB9	[19:18]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPB8	[17:16]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPB7	[15:14]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPB6	[13:12]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPB5	[11:10]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPB4	[9:8]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPB3	[7:6]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPB2	[5:4]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPB1	[3:2]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPB0	[1:0]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable

PORT C CONTROL REGISTERS (GPCCON, GPCDAT, AND GPCDN)

Register	Address	R/W	Description	Reset Value
GPCCON	0x56000020	R/W	Configure the pins of port C	0x0
GPCDAT	0x56000024	R/W	The data register for port C	Undefined
GPCDN	0x56000028	R/W	Pull-down disable register for port C	0x0
GPCSLPCON	0x5600002C	R/W	Sleep mode configuration register for port C	0x0

GPCCON	Bit	Description
GPC15	[31:30]	00 = Input 01 = Output 10 = VD[7] 11 = Reserved
GPC14	[29:28]	00 = Input 01 = Output 10 = VD[6] 11 = Reserved
GPC13	[27:26]	00 = Input 01 = Output 10 = VD[5] 11 = Reserved
GPC12	[25:24]	00 = Input 01 = Output 10 = VD[4] 11 = Reserved
GPC11	[23:22]	00 = Input 01 = Output 10 = VD[3] 11 = Reserved
GPC10	[21:20]	00 = Input 01 = Output 10 = VD[2] 11 = Reserved
GPC9	[19:18]	00 = Input 01 = Output 10 = VD[1] 11 = Reserved
GPC8	[17:16]	00 = Input 01 = Output 10 = VD[0] 11 = Reserved
GPC7	[15:14]	00 = Input 01 = Output 10 = LCDVF2 11 = Reserved
GPC6	[13:12]	00 = Input 01 = Output 10 = LCDVF1 11 = Reserved
GPC5	[11:10]	00 = Input 01 = Output 10 = LCDVF0 11 = Reserved
GPC4	[9:8]	00 = Input 01 = Output 10 = VM 11 = Reserved
GPC3	[7:6]	00 = Input 01 = Output 10 = VFRAME 11 = Reserved
GPC2	[5:4]	00 = Input 01 = Output 10 = VLINE 11 = Reserved
GPC1	[3:2]	00 = Input 01 = Output 10 = VCLK 11 = Reserved
Reserved	[1:0]	Reserved

GPCDAT	Bit	Description
GPC[15:0]	[15:0]	When the port is configured as input port, data from external sources can be read to the corresponding pin. When the port is configured as output port, data written in this register can be sent to the corresponding pin. When the port is configured as functional pin, undefined value will be read.

GPCDN	Bit	Description
GPC[15:0]	[15:0]	0: The pull-down function attached to to the corresponding port pin is enabled. 1: The pull-down function is disabled.

GPCSLPCON	Bit	Description	
GPC15	[31:30]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPC14	[29:28]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPC13	[27:26]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPC12	[25:24]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPC11	[23:22]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPC10	[21:20]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPC9	[19:18]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPC8	[17:16]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPC7	[15:14]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPC6	[13:12]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPC5	[11:10]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPC4	[9:8]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPC3	[7:6]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPC2	[5:4]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPC1	[3:2]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
Reserved	[1:0]	Reserved	

PORT D CONTROL REGISTERS (GPDCON, GPDDAT, and GPDDN)

Register	Address	R/W	Description	Reset Value
GPDCON	0x56000030	R/W	Configure the pins of port D	0x0
GPDDAT	0x56000034	R/W	The data register for port D	Undefined
GPDDN	0x56000038	R/W	Pull-down disable register for port D	0x0
GPDSLPCON	0x5600003C	R/W	Sleep mode configuration register for port D	0x0

GPDCON	Bit	Description
GPD15	[31:30]	00 = Input 01 = Output 10 = VD23 11 = nSS0
GPD14	[29:28]	00 = Input 01 = Output 10 = VD22 11 = nSS1
GPD13	[27:26]	00 = Input 01 = Output 10 = VD21 11 = Reserved
GPD12	[25:24]	00 = Input 01 = Output 10 = VD20 11 = Reserved
GPD11	[23:22]	00 = Input 01 = Output 10 = VD19 11 = Reserved
GPD10	[21:20]	00 = Input 01 = Output 10 = VD18 11 = SPICLK1
GPD9	[19:18]	00 = Input 01 = Output 10 = VD17 11 = SPIMOSI1
GPD8	[17:16]	00 = Input 01 = Output 10 = VD16 11 = SPIMISO1
GPD7	[15:14]	00 = Input 01 = Output 10 = VD15 11 = Reserved
GPD6	[13:12]	00 = Input 01 = Output 10 = VD14 11 = Reserved
GPD5	[11:10]	00 = Input 01 = Output 10 = VD13 11 = Reserved
GPD4	[9:8]	00 = Input 01 = Output 10 = VD12 11 = Reserved
GPD3	[7:6]	00 = Input 01 = Output 10 = VD11 11 = Reserved
GPD2	[5:4]	00 = Input 01 = Output 10 = VD10 11 = Reserved
GPD1	[3:2]	00 = Input 01 = Output 10 = VD9 11 = Reserved
GPD0	[1:0]	00 = Input 01 = Output 10 = VD8 11 = Reserved

GPDDAT	Bit	Description
GPD[15:0]	[15:0]	When the port is configured as input port, data from external sources can be read to the corresponding pin. When the port is configured as output port, data written in this register can be sent to the corresponding pin. When the port is configured as functional pin, undefined value will be read.

GPDDN	Bit	Description
GPD[15:0]	[15:0]	0: The pull-down function attached to to the corresponding port pin is enabled. 1: The pull-down function is disabled.

GPDSLPCON	Bit	Description	
GPD15	[31:30]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD14	[29:28]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD13	[27:26]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD12	[25:24]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD11	[23:22]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD10	[21:20]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD9	[19:18]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD8	[17:16]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD7	[15:14]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD6	[13:12]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD5	[11:10]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD4	[9:8]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD3	[7:6]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD2	[5:4]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD1	[3:2]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPD0	[1:0]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable

PORT E CONTROL REGISTERS (GPECON, GPEDAT, and GPEDN)

Register	Address	R/W	Description	Reset Value
GPECON	0x56000040	R/W	Configure the pins of port E	0x0
GPEDAT	0x56000044	R/W	The data register for port E	Undefined
GPEDN	0x56000048	R/W	pull-down disable register for port E	0x0
GPESLPCON	0x5600004C	R/W	Sleep mode configuration register for port E	0x0

GPECON	Bit	Description
GPE15	[31:30]	00 = Input 10 = IICSDA 11 = Reserved
GPE14	[29:28]	00 = Input 10 = IICSCL 11 = Reserved
GPE13	[27:26]	00 = Input 01 = Output 10 = SPICLK0 11 = Reserved
GPE12	[25:24]	00 = Input 01 = Output 10 = SPIMOSI0 11 = Reserved
GPE11	[23:22]	00 = Input 01 = Output 10 = SPIMISO0 11 = Reserved
GPE10	[21:20]	00 = Input 01 = Output 10 = SDDAT3 11 = Reserved
GPE9	[19:18]	00 = Input 01 = Output 10 = SDDAT2 11 = Reserved
GPE8	[17:16]	00 = Input 01 = Output 10 = SDDAT1 11 = Reserved
GPE7	[15:14]	00 = Input 01 = Output 10 = SDDAT0 11 = Reserved
GPE6	[13:12]	00 = Input 01 = Output 10 = SDCMD 11 = Reserved
GPE5	[11:10]	00 = Input 01 = Output 10 = SDCLK 11 = Reserved
GPE4	[9:8]	00 = Input 01 = Output 10 = I2SSDO 11 = I2SSDI
GPE3	[7:6]	00 = Input 01 = Output 10 = I2SSDI 11 = nSS0
GPE2	[5:4]	00 = Input 01 = Output 10 = CDCLK 11 = Reserved
GPE1	[3:2]	00 = Input 01 = Output 10 = I2SSCLK 11 = Reserved
GPE0	[1:0]	00 = Input 01 = Output 10 = I2SLRCK 11 = Reserved

GPEDAT	Bit	Description
GPE[15:0]	[13:0]	When the port is configured as input port, data from external sources can be read to the corresponding pin. When the port is configured as output port, data written in this register can be sent to the corresponding pin. When the port is configured as a functional pin, undefined value will be read.

GPEDN	Bit	Description
GPE[15:0]	[13:0]	0: The pull-down function attached to to the corresponding port pin is enabled. 1: The pull-down function is disabled.

GPESLPCON	Bit	Description	
GPE15	[31:30]	0x: output ‘0’	1x:input(no pull-down)
GPE14	[29:28]	0x: output ‘0’	1x:input(no pull-down)
GPE13	[27:26]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPE12	[25:24]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPE11	[23:22]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPE10	[21:20]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPE9	[19:18]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPE8	[17:16]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPE7	[15:14]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPE6	[13:12]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPE5	[11:10]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPE4	[9:8]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPE3	[7:6]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPE2	[5:4]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPE1	[3:2]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPE0	[1:0]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable

PORT F CONTROL REGISTERS (GPFCON, GPFDAT, and GPFDN)

If GPF0 - GPF7 are used for wakeup signals in Power_OFF mode, the ports must be configured as external interrupt (set in Interrupt mode).

Register	Address	R/W	Description	Reset Value
GPFCON	0x56000050	R/W	Configure the pins of port F	0x0
GPFDAT	0x56000054	R/W	The data register for port F	Undefined
GPFDN	0x56000058	R/W	Pull-down disable register for port F	0x0
Reserved	0x5600005c	-	-	

GPFCON	Bit	Description
GPF7	[15:14]	00 = Input 01 = Output 10 = EINT7 11 = Reserved
GPF6	[13:12]	00 = Input 01 = Output 10 = EINT6 11 = Reserved
GPF5	[11:10]	00 = Input 01 = Output 10 = EINT5 11 = Reserved
GPF4	[9:8]	00 = Input 01 = Output 10 = EINT4 11 = Reserved
GPF3	[7:6]	00 = Input 01 = Output 10 = EINT3 11 = Reserved
GPF2	[5:4]	00 = Input 01 = Output 10 = EINT2 11 = Reserved
GPF1	[3:2]	00 = Input 01 = Output 10 = EINT1 11 = Reserved
GPF0	[1:0]	00 = Input 01 = Output 10 = EINT0 11 = Reserved

GPFDAT	Bit	Description
GPF[7:0]	[7:0]	When the port is configured as input port, data from external sources can be read to the corresponding pin. When the port is configured as output port, data written in this register can be sent to the corresponding pin. When the port is configured as functional pin, undefined value will be read.

GPFDN	Bit	Description
GPF[7:0]	[7:0]	0: The pull-down function attached to to the corresponding port pin is enabled. 1: The pull-down function is disabled.

PORT G CONTROL REGISTERS (GPGCON, GPGDAT, AND GPGDN)

If GPG [7:0] are used for wakeup signals in Power_OFF mode, the ports must be configured as external interrupt (set in Interrupt mode).

Register	Address	R/W	Description	Reset Value
GPGCON	0x56000060	R/W	Configure the pins of port G	0x0
GPGDAT	0x56000064	R/W	The data register for port G	Undefined
GPGDN	0x56000068	R/W	Pull-down disable register for port G	0x0
GPGSLPCON	0x5600006C	R/W	Sleep mode configuration register for port G	0x0

GPGCON	Bit	Description
GPG15	[31:30]	00 = Input 01 = Output 10 = EINT23 11 = Reserved
GPG14	[29:28]	00 = Input 01 = Output 10 = EINT22 11 = Reserved
GPG13	[27:26]	00 = Input 01 = Output 10 = EINT21 11 = Reserved
GPG12	[25:24]	00 = Input 01 = Output 10 = EINT20 11 = Reserved
GPG11	[23:22]	00 = Input 01 = Output 10 = EINT19 11 = TCLK1
GPG10	[21:20]	00 = Input 01 = Output 10 = EINT18 11 = nCTS1
GPG9	[19:18]	00 = Input 01 = Output 10 = EINT17 11 = nRTS1
GPG8	[17:16]	00 = Input 01 = Output 10 = EINT16 11 = Reserved
GPG7	[15:14]	00 = Input 01 = Output 10 = EINT15 11 = SPICLK1
GPG6	[13:12]	00 = Input 01 = Output 10 = EINT14 11 = SPIMOSI1
GPG5	[11:10]	00 = Input 01 = Output 10 = EINT13 11 = SPIMISO1
GPG4	[9:8]	00 = Input 01 = Output 10 = EINT12 11 = Reserved
GPG3	[7:6]	00 = Input 01 = Output 10 = EINT11 11 = nSS1
GPG2	[5:4]	00 = Input 01 = Output 10 = EINT10 11 = nSS0
GPG1	[3:2]	00 = Input 01 = Output 10 = EINT9 11 = ATA_NRESET
GPG0	[1:0]	00 = Input 01 = Output 10 = EINT8 11 = ATA_INTRQ

GPGDAT	Bit	Description
GPG[15:0]	[15:0]	When the port is configured as input port, data from external sources can be read to the corresponding pin. When the port is configured as output port, data written in this register can be sent to the corresponding pin. When the port is configured as functional pin, undefined value will be read.

GPGDN	Bit	Description
GPG[15:0]	[15:0]	0: The pull-down function attached to to the corresponding port pin is enabled. 1: The pull-down function is disabled.

GPGSLPCON	Bit	Description
GPG15	[31:30]	0x: output ‘0’ 10:input, pull-down disable 11: input, pull-down enable
GPG14	[29:28]	0x: output ‘0’ 10:input, pull-down disable 11: input, pull-down enable
GPG13	[27:26]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPG12	[25:24]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPG11	[23:22]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPG10	[21:20]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPG9	[19:18]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPG8	[17:16]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPG7	[15:14]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPG6	[13:12]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPG5	[11:10]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPG4	[9:8]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPG3	[7:6]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPG2	[5:4]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPG1	[3:2]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPG0	[1:0]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable

PORT H CONTROL REGISTERS (GPHCON, GPHDAT, AND GPHDN)

Register	Address	R/W	Description	Reset Value
GPHCON	0x56000070	R/W	Configure the pins of port H	0x0
GPHDAT	0x56000074	R/W	The data register for port H	Undefined
GPHDN	0x56000078	R/W	Pull-down disable register for port H	0x0
GPHSLPCON	0x5600007C	R/W	Sleep mode configuration register for port H	0x0

GPHCON	Bit	Description
GPH10	[21:20]	00 = Input 01 = Output 10 = CLKOUT1 11 = Reserved
GPH9	[19:18]	00 = Input 01 = Output 10 = CLKOUT0 11 = Reserved
GPH8	[17:16]	00 = Input 01 = Output 10 = UEXTCLK 11 = Reserved
GPH7	[15:14]	00 = Input 01 = Output 10 = RXD2 11 = nCTS1
GPH6	[13:12]	00 = Input 01 = Output 10 = TXD2 11 = nRTS1
GPH5	[11:10]	00 = Input 01 = Output 10 = RXD1 11 = Reserved
GPH4	[9:8]	00 = Input 01 = Output 10 = TXD1 11 = Reserved
GPH3	[7:6]	00 = Input 01 = Output 10 = RXD0 11 = reserved
GPH2	[5:4]	00 = Input 01 = Output 10 = TXD0 11 = Reserved
GPH1	[3:2]	00 = Input 01 = Output 10 = nRTS0 11 = Reserved
GPH0	[1:0]	00 = Input 01 = Output 10 = nCTS0 11 = Reserved

GPHDAT	Bit	Description
GPH[10:0]	[10:0]	When the port is configured as input port, data from external sources can be read to the corresponding pin. When the port is configured as output port, data written in this register can be sent to the corresponding pin. When the port is configured as functional pin, undefined value will be read.

GPHDN	Bit	Description
GPH[10:0]	[10:0]	0: The pull-down function attached to to the corresponding port pin is enabled. 1: The pull-down function is disabled.

GPHSLPCON	Bit	Description	
GPH10	[21:20]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPH9	[19:18]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPH8	[17:16]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPH7	[15:14]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPH6	[13:12]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPH5	[11:10]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPH4	[9:8]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPH3	[7:6]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPH2	[5:4]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPH1	[3:2]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable
GPH0	[1:0]	00: output ‘0’ 10:input, pull-down disable	01: output ‘1’ 11: input, pull-down enable

PORT J CONTROL REGISTERS(GPJCON, GPJDAT)

Register	Address	R/W	Description	Reset Value
GPJCON	0x56000080	R/W	Configures the pins of port J	0x0
GPJDAT	0x56000084	R/W	The data register for port J	Undef.
GPJDN	0x56000088	R/W	pull-down disable register for port J	0x0000
GPJSLPCON	0x5600008C	R/W	Sleep mode configuration register for port J	0x0

GPJCON	Bit	Description
GPJ12	[25:24]	00 = Input 01 = Output 10 = CAMRESET 11 = Reserved
GPJ11	[23:22]	00 = Input 01 = Output 10 = CAMCLKOUT 11 = Reserved
GPJ10	[21:20]	00 = Input 01 = Output 10 = CAMHREF 11 = Reserved
GPJ9	[19:18]	00 = Input 01 = Output 10 = CAMVSYNC 11 = Reserved
GPJ8	[17:16]	00 = Input 01 = Output 10 = CAMPCLK 11 = Reserved
GPJ7	[15:14]	00 = Input 01 = Output 10 = CAMDATA[7] 11 = Reserved
GPJ6	[13:12]	00 = Input 01 = Output 10 = CAMDATA[6] 11 = Reserved
GPJ5	[11:10]	00 = Input 01 = Output 10 = CAMDATA[5] 11 = Reserved
GPJ4	[9:8]	00 = Input 01 = Output 10 = CAMDATA[4] 11 = Reserved
GPJ3	[7:6]	00 = Input 01 = Output 10 = CAMDATA[3] 11 = Reserved
GPJ2	[5:4]	00 = Input 01 = Output 10 = CAMDATA[2] 11 = Reserved
GPJ1	[3:2]	00 = Input 01 = Output 10 = CAMDATA[1] 11 = Reserved
GPJ0	[1:0]	00 = Input 01 = Output 10 = CAMDATA[0] 11 = Reserved

GPJDAT	Bit	Description
GPJ[12:0]	[12:0]	When the port is configured as input port, data from external sources can be read to the corresponding pin. When the port is configured as output port, data written in this register can be sent to the corresponding pin. When the port is configured as functional pin, undefined value will be read.

GPJDN	Bit	Description
GPJ[12:0]	[12:0]	0: The pull-down function attached to to the corresponding port pin is enabled. 1: The pull-down function is disabled.

GPJSLPCON	Bit	Description
GPJ12	[25:24]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPJ11	[23:22]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPJ10	[21:20]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPJ9	[19:18]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPJ8	[17:16]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPJ7	[15:14]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPJ6	[13:12]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPJ5	[11:10]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPJ4	[9:8]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPJ3	[7:6]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPJ2	[5:4]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPJ1	[3:2]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable
GPJ0	[1:0]	00: output ‘0’ 01: output ‘1’ 10:input, pull-down disable 11: input, pull-down enable

MISCELLANEOUS CONTROL REGISTER (MISCCR)

Pads related USB are controlled by this register for USB host, or for USB device.

Register	Address	R/W	Description	Reset Value
MISCCR	0x56000090	R/W	Miscellaneous control register	0x330

MISCCR	Bit	Description
Reserved	[21:20]	Reserved
Reserved	[19:17]	Should be zero
Reserved	[16:14]	Reserved
USBSUSPND1	[13]	[13] USB Port 1 mode 0 = Normal 1= Suspend
USBSUSPND0	[12]	[12] USB Port 0 mode 0 = Normal 1= Suspend
Reserved	[11]	Reserved
CLKSEL1	[10:8]	CLKOUT1 output singnal source 000 = CLK source 001 = UPLL CLK 010 = FCLK 011 = HCLK 100 = PCLK 101 = DCLK1 11x = Reserved
Reserved	[7]	0
CLKSEL0	[6:4]	CLKOUT0 output singnal source 000 = MPLL CLK 001 = UPLL CLK 010 = RTC clock 011 = HCLK 100 = PCLK 101 = DCLK0 11x = Reserved
USBPAD	[3]	0 = Use pads related USB for USB device 1 = Use pads related USB for USB host
SPUCR2	[2]	DQS[1:0] port pull-up resister 0 = Enabled 1 = Disabled
SPUCR_H	[1]	DATA[31:16] port pull-up resister 0 = Enabled 1 = Disabled
SPUCR_L	[0]	DATA[15:0] port pull-up resister 0 = Enabled 1 = Disabled

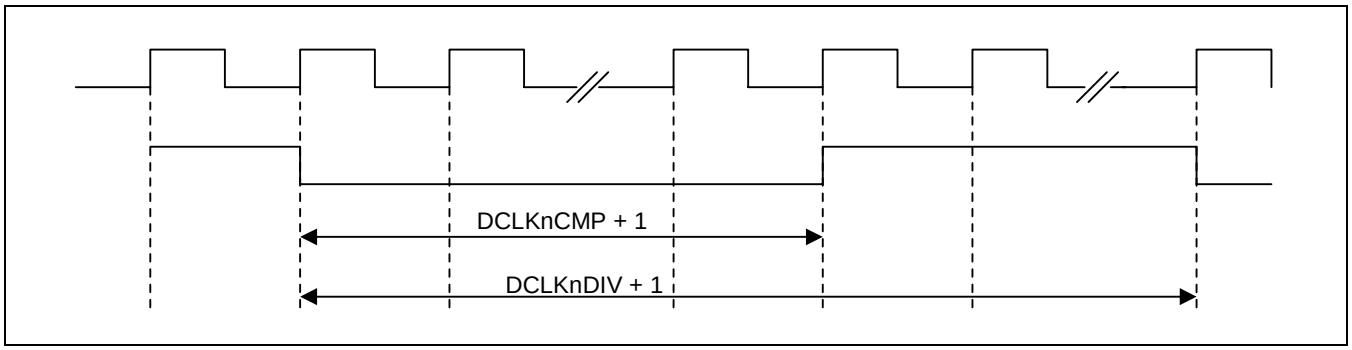
NOTE: CLKOUT is prepared only for monitoring an internal clock situation (On/Off status or frequency).

DCLK CONTROL REGISTERS (DCLKCON)

This register defines DCLKn signals, which work as clocks for external sources. See the following figure for how to make the DCLKn signals. The DCLKCON can actually operate only when CLKOUT [1:0] is set to send the DCLKn signals.

Register	Address	R/W	Description	Reset Value
DCLKCON	0x56000094	R/W	DCLK0/1 control register	0x0

DCLKCON	Bit	Description
DCLK1CMP	[27:24]	DCLK1 Compare value clock toggle value. (< DCLK1DIV) If the DCLK1CMP is n, Low level duration is (n + 1). High level duration is ((DCLK1DIV + 1) – (n +1)).
DCLK1DIV	[23:20]	DCLK1 Divide value DCLK1 frequency = source clock / (DCLK1DIV + 1)
Reserved	[19:18]	00b
DCLK1SelCK	[17]	Select DCLK1 source clock 0 = PCLK 1 = UCLK (USB)
DCLK1EN	[16]	DCLK1 Enable 0 = Disable 1 = Enable
Reserved	[15:12]	0000b
DCLK0CMP	[11:8]	DCLK0 Compare value clock toggle value. (< DCLK0DIV) If the DCLK0CMP is n, Low level duration is (n + 1). High level duration is ((DCLK0DIV + 1) – (n +1)).
DCLK0DIV	[7:4]	DCLK0 Divide value. DCLK0 frequency = source clock / (DCLK0DIV + 1)
Reserved	[3:2]	00b
DCLK0SelCK	[1]	Select DCLK0 source clock 0 = PCLK 1 = UCLK (USB)
DCLK0EN	[0]	DCLK0 Enable 0 = Disable 1 = Enable



EXTERNAL INTERRUPT CONTROL REGISTER (EXTINTn)

The 24 external interrupts can be requested by various signaling methods. The EXTINTn configures the signaling method between the level trigger and edge trigger for the external interrupt request, and also configures the signal polarity.

To recognize the level interrupt, the valid logic level on EXTINTn pin must be retained at least for 40ns because of the noise filter (EINT[15:0]).

Register	Address	R/W	Description	Reset Value
EXTINT0	0x56000098	R/W	External interrupt control register 0	0x0
EXTINT1	0x5600009C	R/W	External interrupt control register 1	0x0
EXTINT2	0x560000A0	R/W	External interrupt control register 2	0x0

EXTINT0	Bit	Description
FLTEN7	[31]	Filter Enable for EINT7 0 = Disable 1= Enable
EINT7	[30:28]	Set the signaling method of the EINT7. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN6	[27]	Filter Enable for EINT6 0 = Disable 1= Enable
EINT6	[26:24]	Set the signaling method of the EINT6. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN5	[23]	Filter Enable for EINT5 0 = Disable 1= Enable
EINT5	[22:20]	Set the signaling method of the EINT5. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN4	[19]	Filter Enable for EINT4 0 = Disable 1= Enable
EINT4	[18:16]	Set the signaling method of the EINT4. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN3	[15]	Filter Enable for EINT3 0 = Disable 1= Enable
EINT3	[14:12]	Set the signaling method of the EINT3. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN2	[11]	Filter Enable for EINT2 0 = Disable 1= Enable
EINT2	[10:8]	Set the signaling method of the EINT2. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN1	[7]	Filter Enable for EINT1 0 = Disable 1= Enable
EINT1	[6:4]	Set the signaling method of the EINT1. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN0	[3]	Filter Enable for EINT0 0 = Disable 1= Enable
EINT0	[2:0]	Set the signaling method of the EINT0. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered

NOTE: The noise filter guarantee max. 17ns.

EXTINT1	Bit	Description
FLTEN15	[31]	Filter Enable for EINT15 0 = Disable 1= Enable
EINT15	[30:28]	Set the signaling method of the EINT15. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN14	[27]	Filter Enable for EINT14 0 = Disable 1= Enable
EINT14	[26:24]	Set the signaling method of the EINT14. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN13	[23]	Filter Enable for EINT13 0 = Disable 1= Enable
EINT13	[22:20]	Set the signaling method of the EINT13. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN12	[19]	Filter Enable for EINT12 0 = Disable 1= Enable
EINT12	[18:16]	Set the signaling method of the EINT12. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN11	[15]	Filter Enable for EINT11 0 = Disable 1= Enable
EINT11	[14:12]	Set the signaling method of the EINT11. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN10	[11]	Filter Enable for EINT10 0 = Disable 1= Enable
EINT10	[10:8]	Set the signaling method of the EINT10. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN9	[7]	Filter Enable for EINT9 0 = Disable 1= Enable
EINT9	[6:4]	Set the signaling method of the EINT9. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN8	[3]	Filter Enable for EINT8 0 = Disable 1= Enable

NOTE: The noise filter guarantee max. 17ns.

EXTINT2	Bit	Description
FLTEN23	[31]	Filter Enable for EINT23 0 = Disable 1= Enable
EINT23	[30:28]	Set the signaling method of the EINT23. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN22	[27]	Filter Enable for EINT22 0 = Disable 1= Enable
EINT22	[26:24]	Set the signaling method of the EINT22. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN21	[23]	Filter Enable for EINT21 0 = Disable 1= Enable
EINT21	[22:20]	Set the signaling method of the EINT21. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN20	[19]	Filter Enable for EINT20 0 = Disable 1= Enable
EINT20	[18:16]	Set the signaling method of the EINT20. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN19	[15]	Filter Enable for EINT19 0 = Disable 1= Enable
EINT19	[14:12]	Set the signaling method of the EINT19. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN18	[11]	Filter Enable for EINT18 0 = Disable 1= Enable
EINT18	[10:8]	Set the signaling method of the EINT18. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN17	[7]	Filter Enable for EINT17 0 = Disable 1= Enable
EINT17	[6:4]	Set the signaling method of the EINT17. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN16	[3]	Filter Enable for EINT16 0 = Disable 1= Enable
EINT16	[2:0]	Set the signaling method of the EINT16. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered

EXTERNAL INTERRUPT FILTER REGISTER (EINTFLTn)

The EINTFLTn controls the length of filter for 8 external interrupts (EINT[23:16]).

Register	Address	R/W	Description	Reset Value
EINTFLT0	0x560000A4	R/W	Reserved	
EINTFLT1	0x560000A8	R/W	Reserved	
EINTFLT2	0x560000AC	R/W	External interrupt control register 2	0x0
EINTFLT3	0x4C6000B0	R/W	External interrupt control register 3	0x0

EINTFLT2	Bit	Description
FLTCLK19	[31]	Filter clock of EINT19 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT19	[30:24]	Filter width of EINT19
FLTCLK18	[23]	Filter clock of EINT18 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT18	[22:16]	Filter width of EINT18
FLTCLK17	[15]	Filter clock of EINT17 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT17	[14:8]	Filter width of EINT17
FLTCLK16	[7]	Filter clock of EINT16 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT16	[6:0]	Filter width of EINT16

EINTFLT3	Bit	Description
FLTCLK23	[31]	Filter clock of EINT23 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT23	[30:24]	Filter width of EINT23
FLTCLK22	[23]	Filter clock of EINT22 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT22	[22:16]	Filter width of EINT22
FLTCLK21	[15]	Filter clock of EINT21 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT21	[14:8]	Filter width of EINT21
FLTCLK20	[7]	Filter clock of EINT20 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT20	[6:0]	Filter width of EINT20

EXTERNAL INTERRUPT MASK REGISTER (EINTMASK)

Interrupt mask register for 20 external interrupts (EINT [23:4]).

Register	Address	R/W	Description	Reset Value
EINTMASK	0x560000B4	R/W	External interupt mask register	0x00FFFFF0

EINTMASK	Bit	Description
EINT23	[23]	0 = Enable Interrupt 1= Masked
EINT22	[22]	0 = Enable Interrupt 1= Masked
EINT21	[21]	0 = Enable Interrupt 1= Masked
EINT20	[20]	0 = Enable Interrupt 1= Masked
EINT19	[19]	0 = Enable Interrupt 1= Masked
EINT18	[18]	0 = Enable Interrupt 1= Masked
EINT17	[17]	0 = Enable Interrupt 1= Masked
EINT16	[16]	0 = Enable Interrupt 1= Masked
EINT15	[15]	0 = Enable Interrupt 1= Masked
EINT14	[14]	0 = Enable Interrupt 1= Masked
EINT13	[13]	0 = Enable Interrupt 1= Masked
EINT12	[12]	0 = Enable Interrupt 1= Masked
EINT11	[11]	0 = Enable Interrupt 1= Masked
EINT10	[10]	0 = Enable Interrupt 1= Masked
EINT9	[9]	0 = Enable Interrupt 1= Masked
EINT8	[8]	0 = Enable Interrupt 1= Masked
EINT7	[7]	0 = Enable Interrupt 1= Masked
EINT6	[6]	0 = Enable Interrupt 1= Masked
EINT5	[5]	0 = Enable Interrupt 1= Masked
EINT4	[4]	0 = Enable Interrupt 1= Masked
EINT3	[3]	0 = Enable Interrupt 1= Masked
EINT2	[2]	0 = Enable Interrupt 1= Masked
EINT1	[1]	0 = Enable Interrupt 1= Masked
EINT0	[0]	0 = Enable Interrupt 1= Masked

EXTERNAL INTERRUPT PENDING REGISTER (EINTPENDn)

Interrupt pending register for 20 external interrupts (EINT [23:4]). You can clear a specific bit of the ENITPEND register by writing "1" on the corresponding bit of this register.

Register	Address	R/W	Description	Reset Value
EINTPEND	0x560000B8	R/W	External interupt pending register	0x0

EINTPEND	Bit	Description
EINT23	[23]	0 = Not requested 1= Requested
EINT22	[22]	0 = Not requested 1= Requested
EINT21	[21]	0 = Not requested 1= Requested
EINT20	[20]	0 = Not requested 1= Requested
EINT19	[19]	0 = Not requested 1= Requested
EINT18	[18]	0 = Not requested 1= Requested
EINT17	[17]	0 = Not requested 1= Requested
EINT16	[16]	0 = Not requested 1= Requested
EINT15	[15]	0 = Not requested 1= Requested
EINT14	[14]	0 = Not requested 1= Requested
EINT13	[13]	0 = Not requested 1= Requested
EINT12	[12]	0 = Not requested 1= Requested
EINT11	[11]	0 = Not requested 1= Requested
EINT10	[10]	0 = Not requested 1= Requested
EINT9	[9]	0 = Not requested 1= Requested
EINT8	[8]	0 = Not requested 1= Requested
EINT7	[7]	0 = Not requested 1= Requested
EINT6	[6]	0 = Not requested 1= Requested
EINT5	[5]	0 = Not requested 1= Requested
EINT4	[4]	0 = Not requested 1= Requested
EINT3	[3]	0 = Not requested 1= Requested
EINT2	[2]	0 = Not requested 1= Requested
EINT1	[1]	0 = Not requested 1= Requested
EINT0	[0]	0 = Not requested 1= Requested

GENERAL STATUS REGISTER (GSTATUSn)

Register	Address	R/W	Description	Reset Value
GSTATUS0	0x560000BC	R	External pin status	Undefined
GSTATUS1	0x560000C0	R	Chip ID	0x32412003
GSTATUS2	0x560000C4	R/W	Infrom register	0x0
GSTATUS3	0x560000C8	R/W	Infrom register	0x0
GSTATUS4	0x560000CC	R/W	Infrom register	0x0
GSTATUS5	0x560000D0	R/W	Infrom register	0x0

GSTATUS0	Bit	Description
nWAIT	[3]	Status of nWAIT pin
Reserved	[2]	Reserved
RnB	[1]	Status of R/nB pin
nBATT_FLT	[0]	Status of nBATT_FLT pin

GSTATUS1	Bit	Description
CHIP ID	[31:0]	ID register = 0x32412003

GSTATUS2	Bit	Description
inform	[31:0]	Inform register. This register is cleared by nRESET or watchdog timer. Otherwise, preserve data value.

GSTATUS3	Bit	Description
inform	[31:0]	Inform register. This register is cleared by nRESET or watchdog timer. Otherwise, preserve data value.

GSTATUS4	Bit	Description
inform	[31:0]	Inform register. This register is cleared by nRESET or watchdog timer. Otherwise, preserve data value.

GSTATUS5	Bit	Description
inform	[31:0]	Inform register. This register is cleared by nRESET or watchdog timer. Otherwise, preserve data value.

MSTCON (Memory Stop Control Register)

Select memory interface status when in STOP mode.

Register	Address	R/W	Description	Reset Value
MSTCON	0x560000D4	R/W	Memory Stop Control Register	0x0

MSLCON	Bit	Description	Reset Value
MST_SCKE	[19]	SCKE pin status in Stop mode. 0: Previous State 1: Hi-Z	0
MST_nSCK	[18]	nSCK pin status in Stop mode. 0: Previous State 1: Hi-Z	0
MST_SCK	[17]	SCK pin status in Stop mode. 0: Previous State 1: Hi-Z	0
MST_SMCLK	[16]	SMCLK pin status in Stop mode. 0: Previous State 1: Hi-Z	0
MST_SMAVD	[15]	SMAVD pin status in Stop mode. 0: Previous State 1: Hi-Z	0
MST_nRSTOUT	[14]	nRSTOUT pin status in Stop mode. 0: Previous State 1: Hi-Z	0
MST_ SMBSTWAIT	[13]	SMBSTWAIT pin status in Stop mode. 0: Previous State 1: Output”0”	0
MST_WAIT	[12]	nWAIT pin status in Stop mode. 0: Previous State 1: Output”0”	0
MST_RnB	[11]	RnB pin status in Stop mode. 0: Previous State 1: Output “0”	0
MST_NFC	[10]	NAND Flash I/F pin status in Stop mode(nFRE,nFWE,ALE,CLE). 0: Previous State 1: Hi-Z	0
MST_nOE	[9]	nOE pin status in Stop mode. 0: Previous State 1: Hi-Z	0
MST_nWE	[8]	nWE pin status in Stop mode. 0: Previous State 1: Hi-Z	0
MST_BE	[7]	BE pin status in Stop mode. 0: Previous State 1: Hi-Z	0
MST_SDR	[6]	nSRAS, nSCAS pin status in Stop mode. 0: Previous State 1: Hi-Z	0
MST_CS	[5]	nGCS[7:0] pin status in Stop mode. 0: Previous State 1: Hi-Z	0
MST_ADDR	[4]	ADDR pin status in Stop mode. 0: Previous State 1: Hi-Z	0
MST_DQS	[3:2]	DQS[1:0] pin status in Stop mode. 00: Output”0” 00: Output”1” 01: Hi-Z 11: input pull-up enable	00
MST_DATA	[1:0]	nGCS[7] pin status in Stop mode. 00: Output”0” 01: Output”1” 10: Hi-Z 11: input pull-up enable	00

MSLCON (Memory Sleep Control Register)

Select memory interface status when in SLEEP mode.

Register	Address	R/W	Description	Reset Value
MSLCON	0x560000D8	R/W	Memory Sleep Control Register	0x0

MSLCON	Bit	Description	Reset Value
MST_SCKE	[31:30]	SCKE pin status in Sleep mode. 00 : Output"0" 01: Output "1" 1* : Hi-Z	0
MST_nSCK	[29:28]	nSCK pin status in Sleep mode. 00 : Output"0" 01: Output "1" 1* : Hi-Z	0
MST_SCK	[27:26]	SCK pin status in Sleep mode. 00 : Output"0" 01: Output "1" 10 : Hi-Z 11: input pull-up enable	0
MST_SMCLK	[25:24]	SMCLK pin status in Sleep mode. 00 : Output"0" 01: Output "1" 10 : Hi-Z 11: input pull-up enable	0
MST_SMAVD	[23:22]	SMAVD pin status in Sleep mode. 00 : Output"0" 01: Output "1" 1* : Hi-Z	0
MST_nRSTOUT	[21]	nRSTOUT pin status in Sleep mode. 0: Output"0" 1: Output "1"	0
MST_ SMBSTWAIT	[20]	SMBSTWAIT pin status in Sleep mode. 0: Input 1: Output "0"	0
MST_WAIT	[19]	nWAIT pin status in Sleep mode. 0: Input 1: Output "0"	0
MST_RnB	[18]	RnB pin status in Sleep mode. 0: Input 1: Output "0"	0
MST_NFC	[17:16]	NAND Flash Controller pin(nFWE, nFRE, ALE, CLE) status in Sleep mode. 00 : Output"0" 01: Output "1" 1* : Hi-Z	0
MST_nOE	[15:14]	nOE pin status in Sleep mode. 00 : Output"0" 01: Output "1" 1* : Hi-Z	0
MST_nWE	[13:12]	nWE pin status in Sleep mode. 00 : Output"0" 01: Output "1" 1* : Hi-Z	0
MST_BE	[11:10]	BE pin status in Sleep mode. 00 : Output"0" 01: Output "1" 1* : Hi-Z	0

MSLCON	Bit	Description	Reset Value
MST_SDR	[9:8]	nSCAS, nSRAS pin status in Sleep mode. 00 : Output"0" 01: Output "1" 1* : Hi-Z	0
MST_CS	[7:6]	nGCS pin status in Sleep mode. 00 : Output"0" 01: Output "1" 1* : Hi-Z	0
MST_ADDR	[5:4]	ADDR pin status in Sleep mode. 00 : Output"0" 01: Output "1" 1* : Hi-Z	0
MST_DQS	[3:2]	DQS pin status in Sleep mode. 00 : Output"0" 01: Output "1" 10 : Hi-Z 11: input pull-up enable	0
MST_DATA	[1:0]	DATA pin status in Sleep mode. 00 : Output"0" 01: Output "1" 10 : Hi-Z 11: input pull-up enable	0

DSCn (Drive Strength Control)

Control the Memory I/O drive strength

Register	Address	R/W	Description	Reset Value
DSC0	0x560000DC	R/W	strength control register 0	0x0
DSC1	0x560000E0	R/W	strength control register 1	0x0

DSC0	Bit	Description	Reset Value
nEN_DSC	[31]	enable Drive Strength Control 0: enable 1: Disable	0
Reserved	[30:26]	-	0
DSC_CS7	[25:24]	nGCS7 Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_CS6	[23:22]	nGCS6 Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_CS5	[21:20]	nGCS5 Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_CS4	[19:18]	nGCS4 Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_CS3	[17:16]	nGCS3 Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_CS2	[15:14]	nGCS2 Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_CS1	[13:12]	nGCS1 Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_CS0	[11:10]	nGCS0 Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_ADR	[9:8]	Address Bus Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_DATA3	[7:6]	DATA[31:24] I/O Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_DATA2	[5:4]	DATA[23:16] I/O Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_DATA1	[3:2]	DATA[15:8] I/O Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_DATA0	[1:0]	DATA[7:0] I/O Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00

DSC1	Bit	Description	Reset Value
Reserved	[30:20]	-	0
DSC_SMAVD	[19:18]	SMAVD Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_DQS	[17:16]	DQS Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_WOE	[15:14]	nWE/nOE Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_BE	[13:12]	nBE[3:0] Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_NFC	[11:10]	Nand Flash Control Drive strength(nFRE, nFWE, CLE, ALE). 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_SDR	[9:8]	nSRAS/nSCAS Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_SCKE	[7:6]	SCKE Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_SMCLK	[5:4]	SMCLK Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_nSCK	[3:2]	nSCLK Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00
DSC_SCK	[1:0]	SCLK Drive strength. 00: 12mA 01: 10mA 10: 8mA 11: 6mA	00

9 PWM TIMER

OVERVIEW

The S3C2413X has five 16-bit timers. Timer 0, 1, 2, and 3 have Pulse Width Modulation (PWM) function. Timer 4 has an internal timer only with no output pins. The timer 0 has a dead-zone generator, which is used with a large current device.

The timer 0 and 1 share an 8-bit prescaler, while the timer 2, 3 and 4 share other 8-bit prescaler. Each timer has a clock divider which 5 different divided signals (1/2, 1/4, 1/8, 1/16, and TCLK). Each timer block receives its own clock signals from the clock divider, which receives the clock from the corresponding 8-bit prescaler. The 8-bit prescaler is programmable and divides the PCLK according to the loading value, which is stored in TCFG0 and TCFG1 registers.

The timer count buffer register (TCNTBn) has an initial value which is loaded into the down-counter when the timer is enabled. The timer compare buffer register (TCMPBn) has an initial value which is loaded into the compare register to be compared with the down-counter value. This double buffering feature of TCNTBn and TCMPBn makes the timer generate a stable output when the frequency and duty ratio are changed.

Each timer has its own 16-bit down counter, which is driven by the timer clock. When the down counter reaches zero, the timer interrupt request is generated to inform the CPU that the timer operation has been completed. When the timer counter reaches zero, the value of corresponding TCNTBn is automatically loaded into the down counter to continue the next operation. However, if the timer stops, for example, by clearing the timer enable bit of TCONn during the timer running mode, the value of TCNTBn will not be reloaded into the counter.

The value of TCMPBn is used for pulse width modulation (PWM). The timer control logic changes the output level when the down-counter value matches the value of the compare register in the timer control logic. Therefore, the compare register determines the turn-on time (or turn-off time) of an PWM output.

FEATURE

- Five 16-bit timers
- Two 8-bit prescalers & Two 4-bit divider
- Programmable duty control of output waveform (PWM)
- Auto reload mode or one-shot pulse mode
- Dead-zone generator

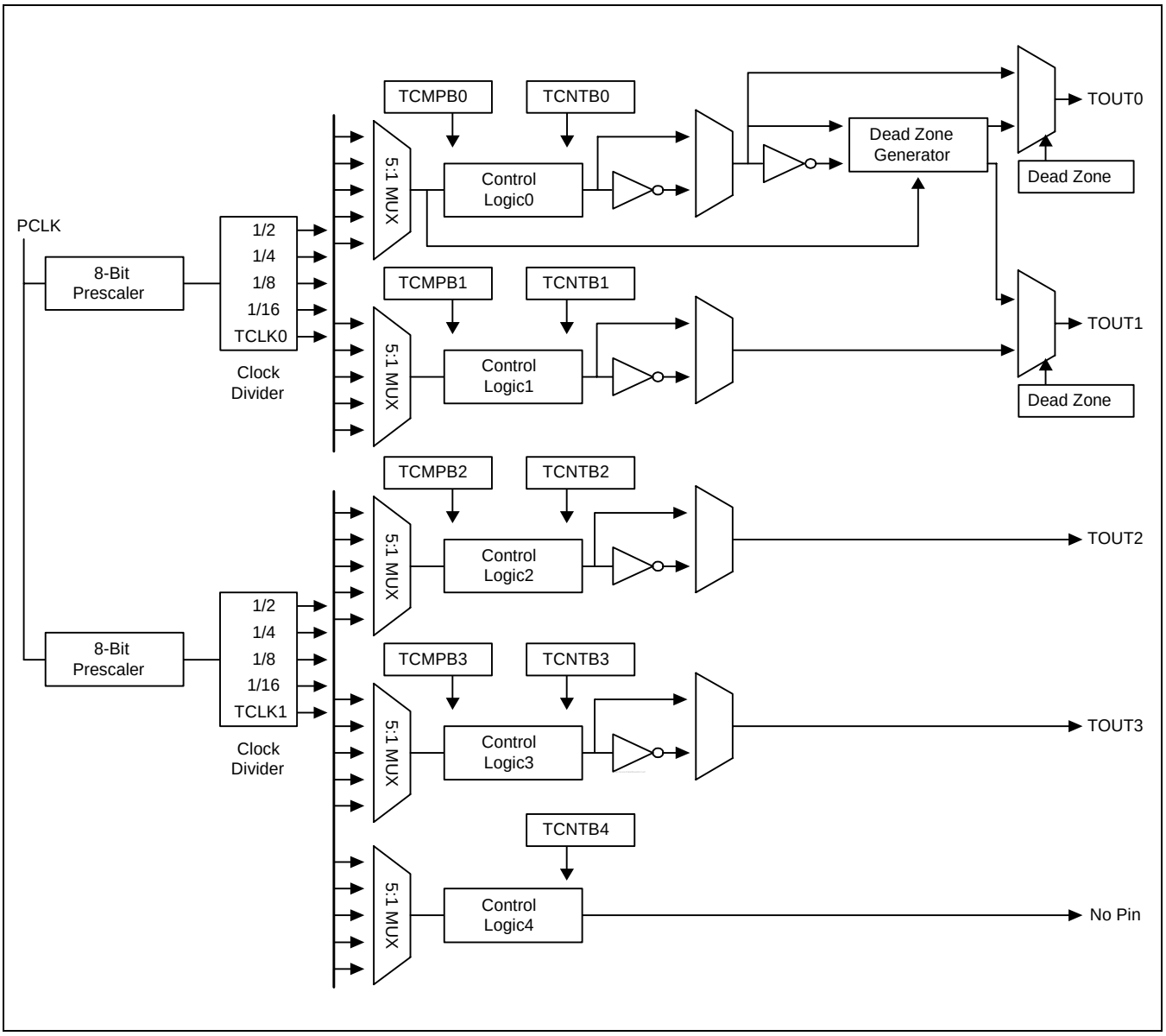


Figure 9-1. 16-bit PWM Timer Block Diagram

PWM TIMER OPERATION

PRESCALER & DIVIDER

An 8-bit prescaler and a 4-bit divider make the following output frequencies:

4-bit divider settings	Minimum resolution (prescaler = 0)	Maximum resolution (prescaler = 255)	Maximum interval (TCNTBn = 65535)
1/2 (PCLK = 66.5 MHz)	0.0300 us (33.2500 MHz)	7.6992 us (129.8828 KHz)	0.5045 sec
1/4 (PCLK = 66.5 MHz)	0.0601 us (16.6250 MHz)	15.3984 us (64.9414 KHz)	1.0091 sec
1/8 (PCLK = 66.5 MHz)	0.1203 us (8.3125 MHz)	30.7968 us (32.4707 KHz)	2.0182 sec
1/16 (PCLK = 66.5 MHz)	0.2406 us (4.1562 MHz)	61.5936 us (16.2353 KHz)	4.0365 sec

BASIC TIMER OPERATION

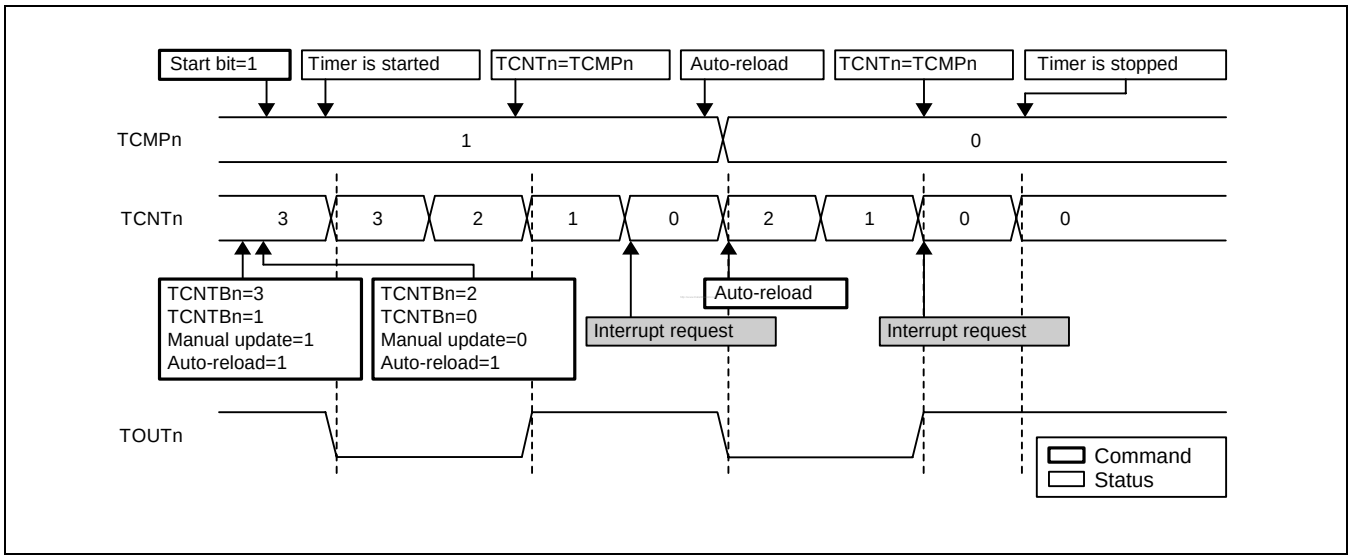


Figure 9-2. Timer Operations

A timer (except the timer ch-5) has TCNTBn, TCNTn, TCMPBn and TCMPn. (TCNTn and TCMPn are the names of the internal registers. The TCNTn register can be read from the TCNTOn register) The TCNTBn and the TCMPBn are loaded into the TCNTn and the TCMPn when the timer reaches 0. When the TCNTn reaches 0, an interrupt request will occur if the interrupt is enabled.

AUTO RELOAD & DOUBLE BUFFERING

S3C2413X PWM Timers have a double buffering function, enabling the reload value changed for the next timer operation without stopping the current timer operation. So, although the new timer value is set, a current timer operation is completed successfully.

The timer value can be written into Timer Count Buffer register (TCNTBn) and the current counter value of the timer can be read from Timer Count Observation register (TCNTOn). If the TCNTBn is read, the read value does not indicate the current state of the counter but the reload value for the next timer duration.

The auto reload operation copies the TCNTBn into TCNTn when the TCNTn reaches 0. The value, written into the TCNTBn, is loaded to the TCNTn only when the TCNTn reaches 0 and auto reload is enabled. If the TCNTn becomes 0 and the auto reload bit is 0, the TCNTn does not operate any further.

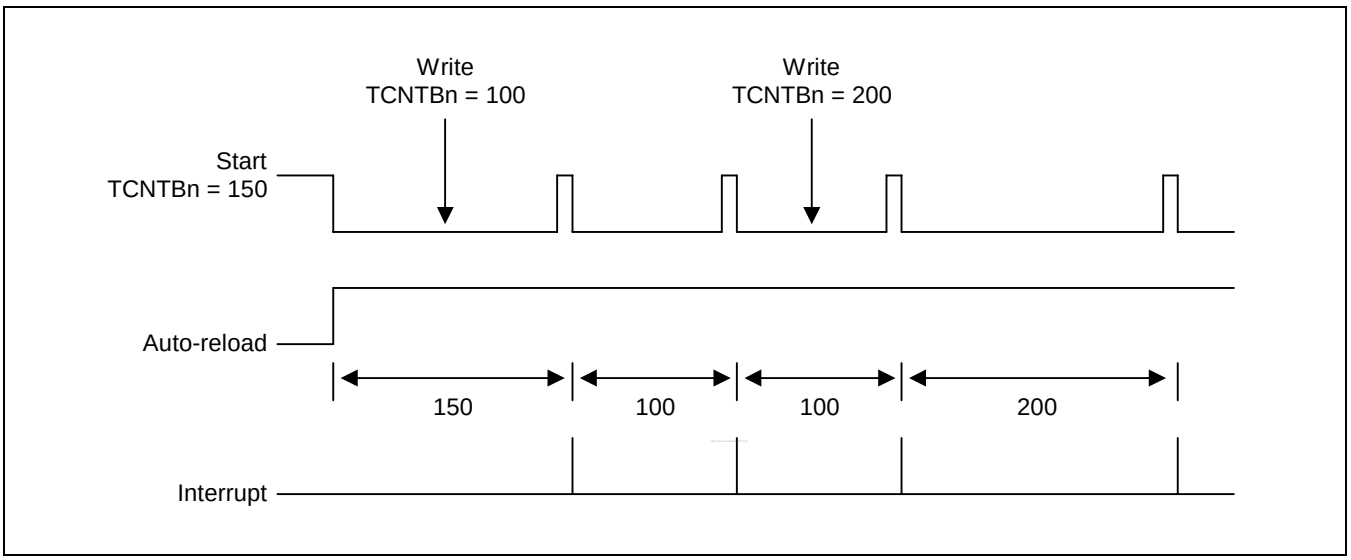


Figure 9-3. Example of Double Buffering Function

TIMER INITIALIZATION USING MANUAL UPDATE BIT AND INVERTER BIT

An auto reload operation of the timer occurs when the down counter reaches 0. So, a starting value of the TCNTn has to be defined by the user in advance. In this case, the starting value has to be loaded by the manual update bit. The following steps describe how to start a timer:

1) Write the initial value into TCNTBn and TCMPBn.
2) Set the manual update bit of the corresponding timer. It is recommended that you configure the inverter on/off bit. (whether use inverter or not).
3) Set start bit of the corresponding timer to start the timer (and clear the manual update bit).

If the timer is stopped by force, the TCNTn retains the counter value and is not reloaded from TCNTBn. If a new value has to be set, perform manual update.

NOTE

Whenever TOUT inverter on/off bit is changed, the TOUTn logic value will also be changed whether the timer runs. Therefore, it is desirable that the inverter on/off bit is configured with the manual update bit.

TIMER OPERATION

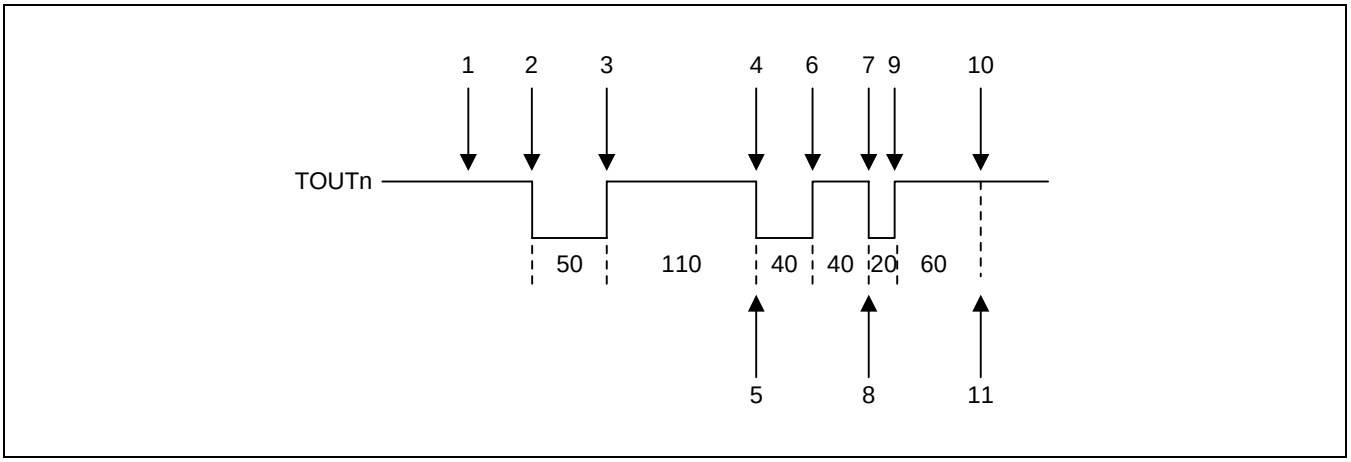


Figure 9-4. Example of a Timer Operation

Figure 9-4 shows the result of the following procedure:

1. Enable the auto reload function. Set the TCNTBn to 160 (50+110) and the TCMPBn to 110. Set the manual update bit and configure the inverter bit (on/off). The manual update bit sets TCNTn and TCMPn to the values of TCNTBn and TCMPBn, respectively.

   And then, set the TCNTBn and the TCMPBn to 80 (40+40) and 40, respectively, to determine the next reload value.
2. Set the start bit, provided that manual_update is 0 and the inverter is off and auto reload is on. The timer starts counting down after latency time within the timer resolution.
3. When the TCNTn has the same value as that of the TCMPn, the logic level of the TOUTn is changed from low to high.
4. When the TCNTn reaches 0, the interrupt request is generated and TCNTBn value is loaded into a temporary register. At the next timer tick, the TCNTn is reloaded with the temporary register value (TCNTBn).
5. In Interrupt Service Routine (ISR), the TCNTBn and the TCMPBn are set to 80 (20+60) and 60, respectively, for the next duration.
6. When the TCNTn has the same value as the TCMPn, the logic level of TOUTn is changed from low to high.
7. When the TCNTn reaches 0, the TCNTn is reloaded automatically with the TCNTBn, triggering an interrupt request.
8. In Interrupt Service Routine (ISR), auto reload and interrupt request are disabled to stop the timer.
9. When the value of the TCNTn is same as the TCMPn, the logic level of the TOUTn is changed from low to high.
10. Even when the TCNTn reaches 0, the TCNTn is not any more reloaded and the timer is stopped because auto reload has been disabled.
11. No more interrupt requests are generated.

PULSE WIDTH MODULATION (PWM)

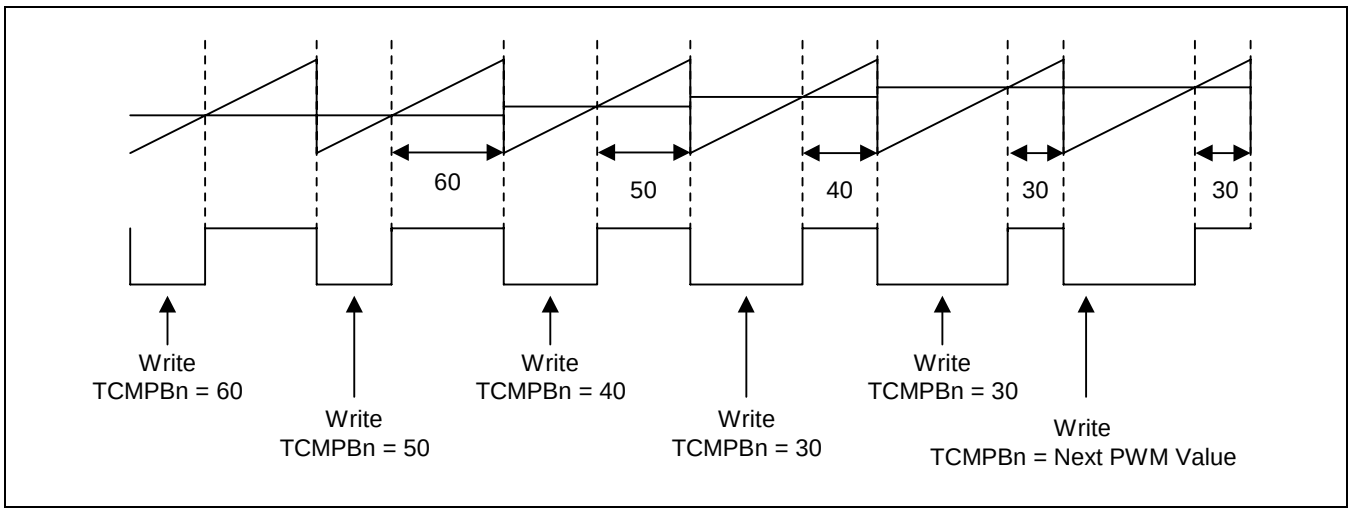


Figure 9-5. Example of PWM

PWM function can be implemented by using the TCMPBn. PWM frequency is determined by TCNTBn. Figure 9-5 shows a PWM value determined by TCMPBn.

For a higher PWM value, decrease the TCMPBn value. For a lower PWM value, increase the TCMPBn value. If an output inverter is enabled, the increment/decrement may be reversed.

The double buffering function allows the TCMPBn, for the next PWM cycle, written at any point in the current PWM cycle by ISR or other routine.

OUTPUT LEVEL CONTROL

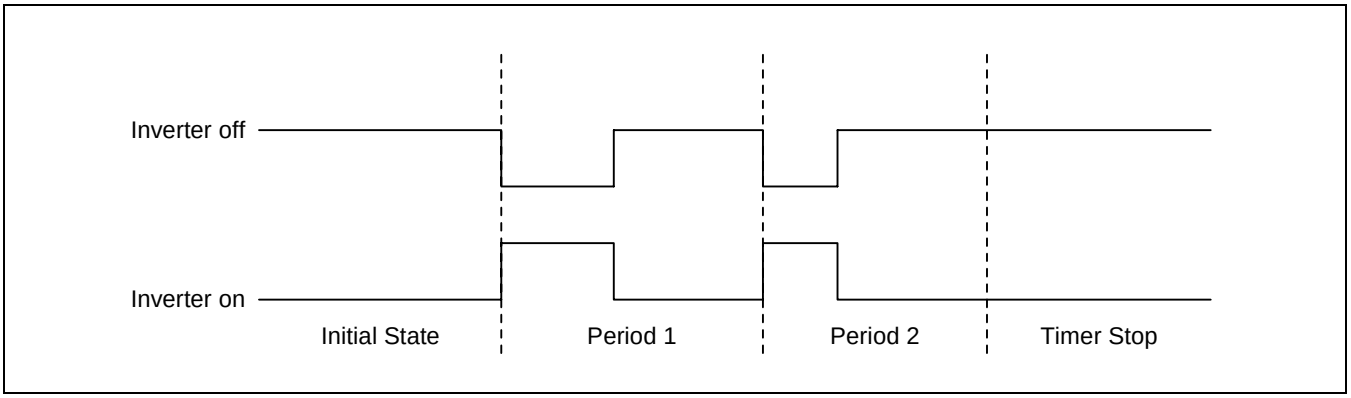


Figure 9-6. Inverter On/Off

The following procedure describes how to maintain TOUT as high or low (assume the inverter is off):

1. Turn off the auto reload bit. And then, TOUTn goes to high level and the timer is stopped after the TCNTn reaches 0 (recommended).
2. Stop the timer by clearing the timer start/stop bit to 0. If TCNTn ≤ TCMPn, the output level is high. If TCNTn >TCMPn, the output level is **low**.
3. The TOUTn can be inverted by the inverter on/off bit in TCON. The inverter removes the additional circuit to adjust the output level.

DEAD ZONE GENERATOR

The dead zone is for the PWM control in a power device. This function enables the insertion of the time gap between a turn-off of a switching device and a turn on of another switching device. This time gap prohibits the two switching devices from being turned on simultaneously, even for a very short time.

TOUT0 is the PWM output. nTOUT0 is the inversion of the TOUT0. If the dead zone is enabled, the output wave form of TOUT0 and nTOUT0 will be TOUT0_DZ and nTOUT0_DZ, respectively. nTOUT0_DZ is routed to the TOUT1 pin.

In the dead zone interval, TOUT0_DZ and nTOUT0_DZ can never be turned on simultaneously.

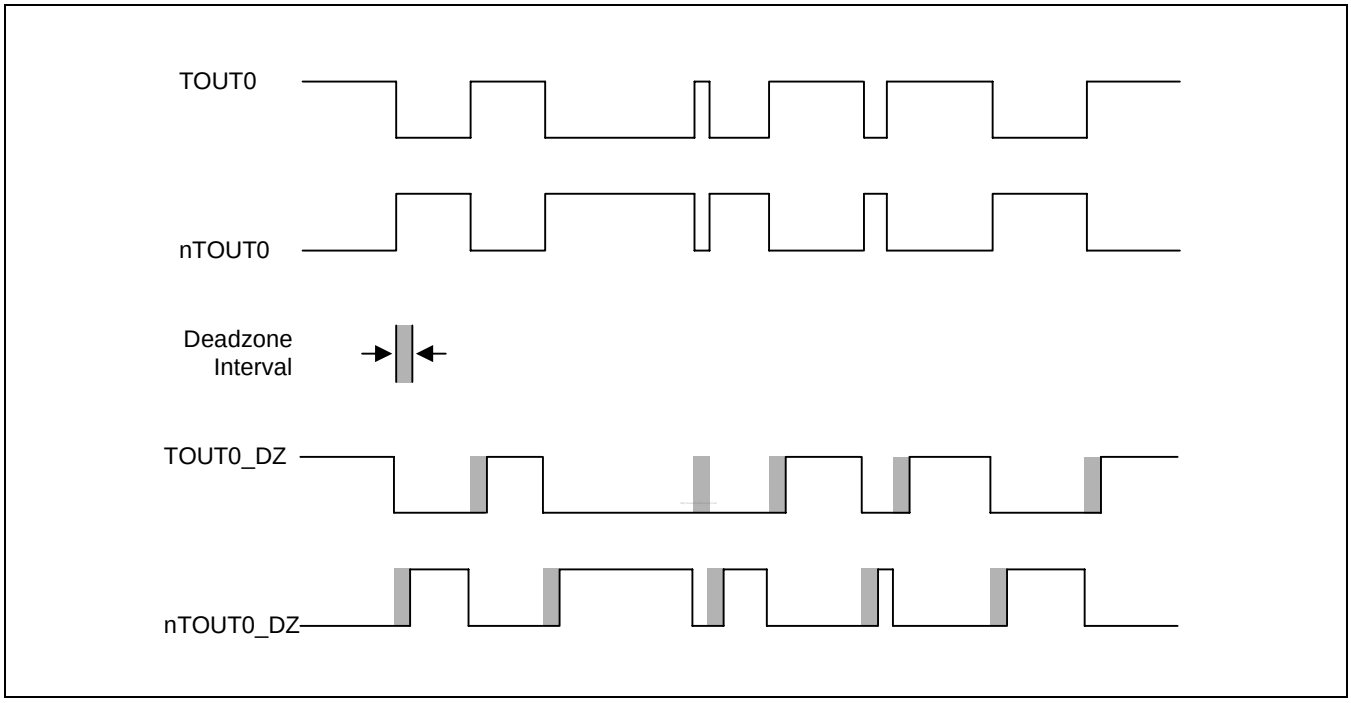


Figure 9-7. The Wave Form When a Dead Zone Feature is Enabled

DMA REQUEST MODE

The PWM timer can generate a DMA request at every specific time. The timer keeps DMA request signals (nDMA_REQ) low until the timer receives an ACK signal. When the timer receives the ACK signal, it makes the request signal inactive. The timer, which generates the DMA request, is determined by setting DMA mode bits (in TCFG1 register). If one of timers is configured as DMA request mode, that timer does not generate an interrupt request. The others can generate interrupt normally.

DMA mode configuration and DMA / interrupt operation

DMA Mode	DMA Request	Timer0 INT	Timer1 INT	Timer2 INT	Timer3 INT	Timer4 INT
0000	No select	ON	ON	ON	ON	ON
0001	Timer0	OFF	ON	ON	ON	ON
0010	Timer1	ON	OFF	ON	ON	ON
0011	Timer2	ON	ON	OFF	ON	ON
0100	Timer3	ON	ON	ON	OFF	ON
0101	Timer4	ON	ON	ON	ON	OFF
0110	No select	ON	ON	ON	ON	ON

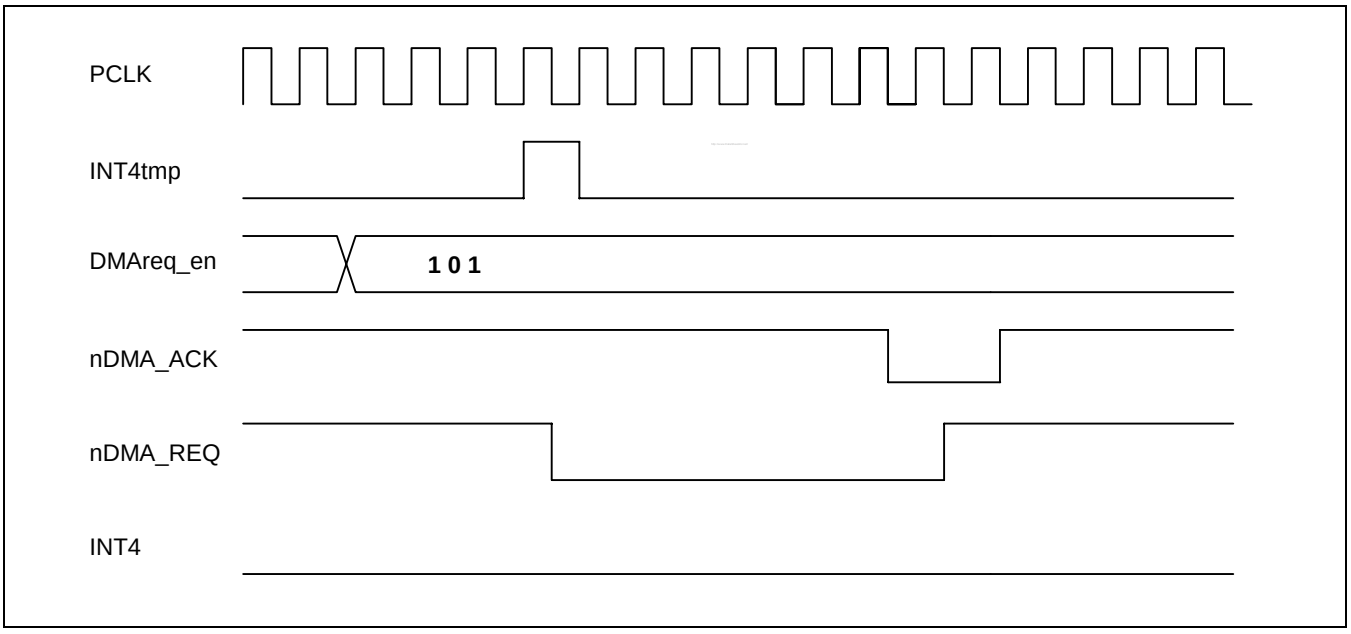


Figure 9-8. Timer4 DMA Mode Operation

PWM TIMER CONTROL REGISTERS

TIMER CONFIGURATION REGISTER0 (TCFG0)

Timer input clock Frequency = PCLK / {prescaler value+1} / {divider value}
{prescaler value} = 0~255
{divider value} = 2, 4, 8, 16

Register	Address	R/W	Description	Reset Value
TCFG0	0x51000000	R/W	Configures the two 8-bit prescalers	0x00000000

TCFG0	Bit	Description	Initial State
Reserved	[31:24]		0x00
Dead zone length	[23:16]	These 8 bits determine the dead zone length. The 1 unit time of the dead zone length is equal to that of timer 0.	0x00
Prescaler 1	[15:8]	These 8 bits determine prescaler value for Timer 2, 3 and 4.	0x00
Prescaler 0	[7:0]	These 8 bits determine prescaler value for Timer 0 and 1.	0x00

TIMER CONFIGURATION REGISTER1 (TCFG1)

Register	Address	R/W	Description	Reset Value
TCFG1	0x51000004	R/W	5-MUX & DMA mode selecton register	0x00000000

TCFG1	Bit	Description	Initial State
Reserved	[31:24]		00000000
DMA mode	[23:20]	Select DMA request channel 0000 = No select (all interrupt) 0001 = Timer0 0010 = Timer1 0011 = Timer2 0100 = Timer3 0101 = Timer4 0110 = Reserved	0000
MUX 4	[19:16]	Select MUX input for PWM Timer4. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK1	0000
MUX 3	[15:12]	Select MUX input for PWM Timer3. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK1	0000
MUX 2	[11:8]	Select MUX input for PWM Timer2. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK1	0000
MUX 1	[7:4]	Select MUX input for PWM Timer1. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK0	0000
MUX 0	[3:0]	Select MUX input for PWM Timer0. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK0	0000

TIMER CONTROL (TCON) REGISTER

Register	Address	R/W	Description	Reset Value
TCON	0x51000008	R/W	Timer control register	0x00000000

TCON	Bit	Description	Initial state
Timer 4 auto reload on/off	[22]	Determine auto reload on/off for Timer 4. 0 = One-shot 1 = Interval mode (auto reload)	0
Timer 4 manual update (note)	[21]	Determine the manual update for Timer 4. 0 = No operation 1 = Update TCNTB4	0
Timer 4 start/stop	[20]	Determine start/stop for Timer 4. 0 = Stop 1 = Start for Timer 4	0
Timer 3 auto reload on/off	[19]	Determine auto reload on/off for Timer 3. 0 = One-shot 1 = Interval mode (auto reload)	0
Timer 3 output inverter on/off	[18]	Determine output inverter on/off for Timer 3. 0 = Inverter off 1 = Inverter on for TOUT3	0
Timer 3 manual update (note)	[17]	Determine manual update for Timer 3. 0 = No operation 1 = Update TCNTB3 & TCMPB3	0
Timer 3 start/stop	[16]	Determine start/stop for Timer 3. 0 = Stop 1 = Start for Timer 3	0
Timer 2 auto reload on/off	[15]	Determine auto reload on/off for Timer 2. 0 = One-shot 1 = Interval mode (auto reload)	0
Timer 2 output inverter on/off	[14]	Determine output inverter on/off for Timer 2. 0 = Inverter off 1 = Inverter on for TOUT2	0
Timer 2 manual update (note)	[13]	Determine the manual update for Timer 2. 0 = No operation 1 = Update TCNTB2 & TCMPB2	0
Timer 2 start/stop	[12]	Determine start/stop for Timer 2. 0 = Stop 1 = Start for Timer 2	0
Timer 1 auto reload on/off	[11]	Determine the auto reload on/off for Timer1. 0 = One-shot 1 = Interval mode (auto reload)	0
Timer 1 output inverter on/off	[10]	Determine the output inverter on/off for Timer1. 0 = Inverter off 1 = Inverter on for TOUT1	0
Timer 1 manual update (note)	[9]	Determine the manual update for Timer 1. 0 = No operation 1 = Update TCNTB1 & TCMPB1	0
Timer 1 start/stop	[8]	Determine start/stop for Timer 1. 0 = Stop 1 = Start for Timer 1	0

NOTE: The bits have to be cleared at next writing.

TIMER CONTROL (TCON) REGISTER (Continued)

TCON	Bit	Description	Initial state
Reserved	[7:5]	Reserved	
Dead zone enable	[4]	Determine the dead zone operation. 0 = Disable 1 = Enable	0
Timer 0 auto reload on/off	[3]	Determine auto reload on/off for Timer 0. 0 = One-shot 1 = Interval mode(auto reload)	0
Timer 0 output inverter on/off	[2]	Determine the output inverter on/off for Timer 0. 0 = Inverter off 1 = Inverter on for TOUT0	0
Timer 0 manual update (note)	[1]	Determine the manual update for Timer 0. 0 = No operation 1 = Update TCNTB0 & TCMPB0	0
Timer 0 start/stop	[0]	Determine start/stop for Timer 0. 0 = Stop 1 = Start for Timer 0	0

NOTE: The bit have to be cleared at next writing.

TIMER 0 COUNT BUFFER REGISTER & COMPARE BUFFER REGISTER (TCNTB0/TCMPB0)

Register	Address	R/W	Description	Reset Value
TCNTB0	0x5100000C	R/W	Timer 0 count buffer register	0x00000000
TCMPB0	0x51000010	R/W	Timer 0 compare buffer register	0x00000000

TCMPB0	Bit	Description	Initial State
Timer 0 compare buffer register	[15:0]	Set compare buffer value for Timer 0	0x00000000

TCNTB0	Bit	Description	Initial State
Timer 0 count buffer register	[15:0]	Set count buffer value for Timer 0	0x00000000

TIMER 0 COUNT OBSERVATION REGISTER (TCNTO0)

Register	Address	R/W	Description	Reset Value
TCNTO0	0x51000014	R	Timer 0 count observation register	0x00000000

TCNTO0	Bit	Description	Initial State
Timer 0 observation register	[15:0]	Set count observation value for Timer 0	0x00000000

TIMER 1 COUNT BUFFER REGISTER & COMPARE BUFFER REGISTER (TCNTB1/TCMPB1)

Register	Address	R/W	Description	Reset Value
TCNTB1	0x51000018	R/W	Timer 1 count buffer register	0x00000000
TCMPB1	0x5100001C	R/W	Timer 1 compare buffer register	0x00000000

TCMPB1	Bit	Description	Initial State
Timer 1 compare buffer register	[15:0]	Set compare buffer value for Timer 1	0x00000000

TCNTB1	Bit	Description	Initial State
Timer 1 count buffer register	[15:0]	Set count buffer value for Timer 1	0x00000000

TIMER 1 COUNT OBSERVATION REGISTER (TCNTO1)

Register	Address	R/W	Description	Reset Value
TCNTO1	0x51000020	R	Timer 1 count observation register	0x00000000

TCNTO1	Bit	Description	initial state
Timer 1 observation register	[15:0]	Set count observation value for Timer 1	0x00000000

TIMER 2 COUNT BUFFER REGISTER & COMPARE BUFFER REGISTER (TCNTB2/TCMPB2)

Register	Address	R/W	Description	Reset Value
TCNTB2	0x51000024	R/W	Timer 2 count buffer register	0x00000000
TCMPB2	0x51000028	R/W	Timer 2 compare buffer register	0x00000000

TCMPB2	Bit	Description	Initial State
Timer 2 compare buffer register	[15:0]	Set compare buffer value for Timer 2	0x00000000

TCNTB2	Bit	Description	Initial State
Timer 2 count buffer register	[15:0]	Set count buffer value for Timer 2	0x00000000

TIMER 2 COUNT OBSERVATION REGISTER (TCNTO2)

Register	Address	R/W	Description	Reset Value
TCNTO2	0x5100002C	R	Timer 2 count observation register	0x00000000

TCNTO2	Bit	Description	Initial State
Timer 2 observation register	[15:0]	Set count observation value for Timer 2	0x00000000

TIMER 3 COUNT BUFFER REGISTER & COMPARE BUFFER REGISTER (TCNTB3/TCMPB3)

Register	Address	R/W	Description	Reset Value
TCNTB3	0x51000030	R/W	Timer 3 count buffer register	0x00000000
TCMPB3	0x51000034	R/W	Timer 3 compare buffer register	0x00000000

TCMPB3	Bit	Description	Initial State
Timer 3 compare buffer register	[15:0]	Set compare buffer value for Timer 3	0x00000000

TCNTB3	Bit	Description	Initial State
Timer 3 count buffer register	[15:0]	Set count buffer value for Timer 3	0x00000000

TIMER 3 COUNT OBSERVATION REGISTER (TCNTO3)

Register	Address	R/W	Description	Reset Value
TCNTO3	0x51000038	R	Timer 3 count observation register	0x00000000

TCNTO3	Bit	Description	Initial State
Timer 3 observation register	[15:0]	Set count observation value for Timer 3	0x00000000

TIMER 4 COUNT BUFFER REGISTER (TCNTB4)

Register	Address	R/W	Description	Reset Value
TCNTB4	0x5100003C	R/W	Timer 4 count buffer register	0x00000000

TCNTB4	Bit	Description	Initial State
Timer 4 count buffer register	[15:0]	Set count buffer value for Timer 4	0x00000000

TIMER 4 COUNT OBSERVATION REGISTER (TCNTO4)

Register	Address	R/W	Description	Reset Value
TCNTO4	0x51000040	R	Timer 4 count observation register	0x00000000

TCNTO4	Bit	Description	Initial State
Timer 4 observation register	[15:0]	Set count observation value for Timer 4	0x00000000

NOTES

10 UART

OVERVIEW

The S3C2413X UART (Universal Asynchronous Receiver and Transmitter) provides three independent asynchronous serial I/O (SIO) ports, each of which can operate in Interrupt-based or DMA-based mode. In other words, the UART can generate an interrupt or a DMA request to transfer data between CPU and the UART. The UART can support bit rates of up to 921.6K bps using system clock. If an external device provides the UART with UEXTCLK, then the UART can operate at higher speed. Each UART channel contains two 64-byte FIFOs for receive and transmit.

The S3C2413X UART includes programmable baud rates, infra-red (IR) transmit/receive, one or two stop bit insertion, 5-bit, 6-bit, 7-bit or 8-bit data width and parity checking.

Each UART contains a baud-rate generator, a transmitter, a receiver and a control unit, as shown in Figure10-1. The baud-rate generator can be clocked by PCLK or UEXTCLK. The transmitter and the receiver contain 64-byte FIFOs and data shifters. Data is written to FIFO and then copied to the transmit shifter before being transmitted. The data is then shifted out by the transmit data pin (TxDn). Meanwhile, received data is shifted from the receive data pin (RxDn), and then copied to FIFO from the shifter.

FEATURES

- RxD0, TxD0, RxD1, TxD1, RxD2, and TxD2 with DMA-based or interrupt-based operation
- UART Ch 0, 1, and 2 with IrDA 1.0 & 64-byte FIFO
- UART Ch 0 and 1 with nRTS0, nCTS0, nRTS1, and nCTS1
- Supports handshake transmit/receive

BLOCK DIAGRAM

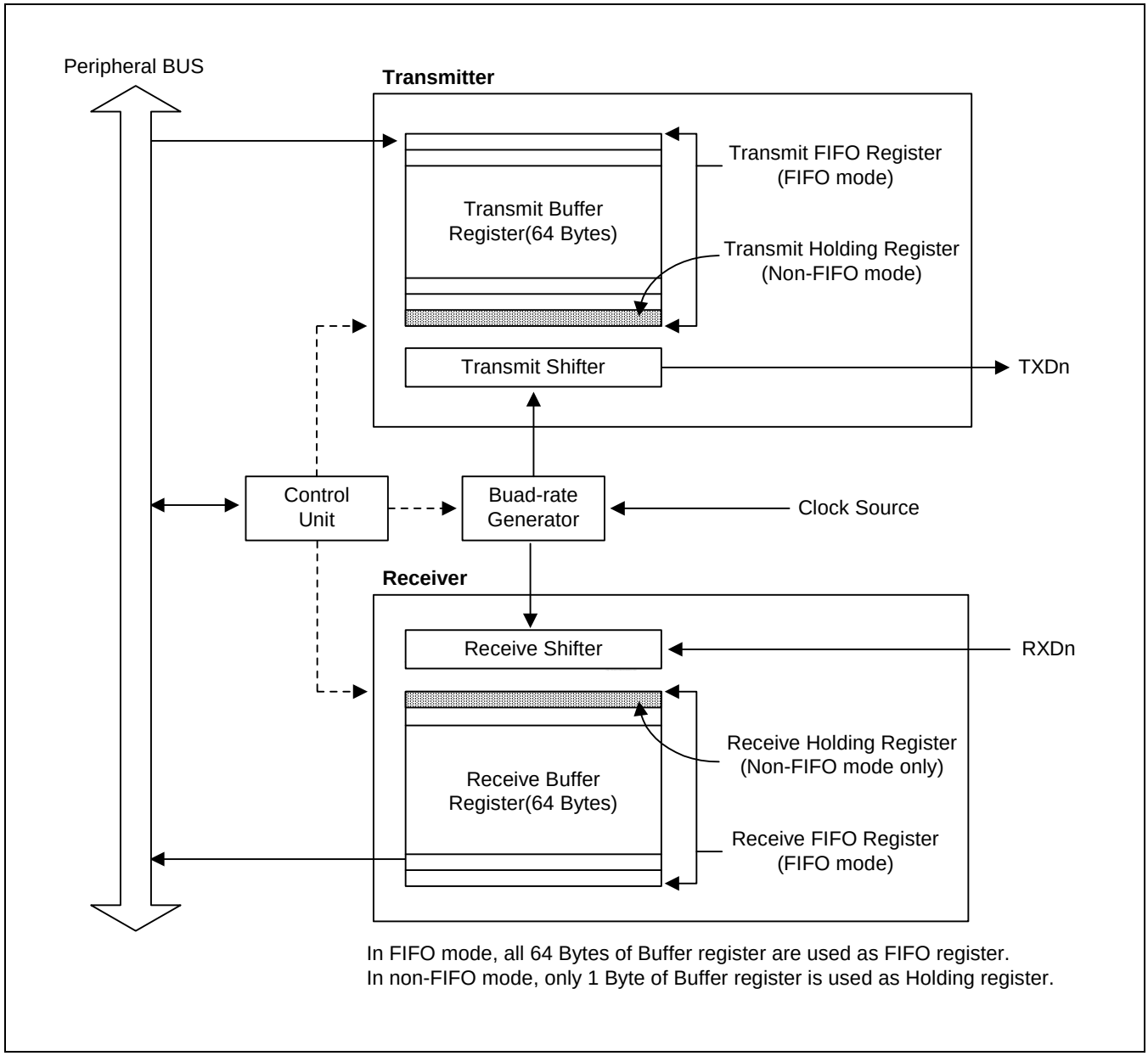


Figure 10-1. UART Block Diagram (with FIFO)

UART OPERATION

The following sections describe the UART operations that include data transmission, data reception, interrupt generation, baud-rate generation, Loopback mode, Infra-red mode, and auto flow control.

Data Transmission

The data frame for transmission is programmable. It consists of a start bit, 5 to 8 data bits, an optional parity bit and 1 to 2 stop bits, which can be specified by the line control register (ULCONn). The transmitter can also produce the break condition, which forces the serial output to logic 0 state for one frame transmission time. This block transmits break signals after the present transmission word is transmitted completely. After the break signal transmission, it continuously transmits data into the Tx FIFO (Tx holding register in the case of Non-FIFO mode).

Data Reception

Like the transmission, the data frame for reception is also programmable. It consists of a start bit, 5 to 8 data bits, an optional parity bit and 1 to 2 stop bits in the line control register (ULCONn). The receiver can detect overrun error and frame error.

- The overrun error indicates that new data has overwritten the old data before the old data has been read.
- The frame error indicates that the received data does not have a valid stop bit.

Receive time-out condition occurs when it does not receive any data during the 3 word time (this interval follows the setting of Word Length bit) and the Rx FIFO is not empty in the FIFO mode.

Auto Flow Control (AFC)

The S3C2413X's UART 0 and UART 1 support auto flow control with nRTS and nCTS signals. In case, it can be connected to external UARTs. If users want to connect a UART to a Modem, disable auto flow control bit in UMCONn register and control the signal of nRTS by software.

In AFC, nRTS depends on the condition of the receiver and nCTS signals control the operation of the transmitter. The UART's transmitter transfers the data in FIFO only when nCTS signals are activated (in AFC, nCTS means that other UART's FIFO is ready to receive data). Before the UART receives data, nRTS has to be activated when its receive FIFO has a spare more than 2-byte and has to be inactivated when its receive FIFO has a spare under 1-byte (in AFC, nRTS means that its own receive FIFO is ready to receive data).

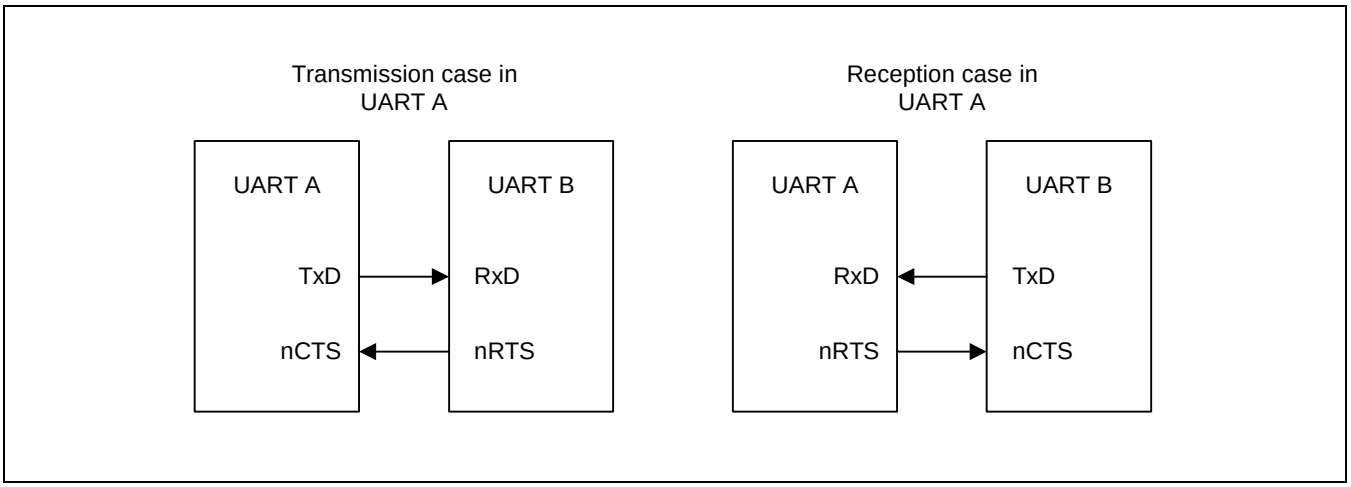


Figure 10-2. UART AFC Interface

NOTE:

UART 2 does not support AFC function, because the S3C2413X has no nRTS2 and nCTS2.

Example of Non Auto-Flow control (controlling nRTS and nCTS by software)

Rx operation with FIFO

1. Select receive mode (Interrupt or DMA mode).
2. Check the value of Rx FIFO count in UFSTATn register. If the value is less than 15, users have to set the value of UMCONn[0] to '1' (activating nRTS), and if it is equal or larger than 15 users have to set the value to '0' (inactivating nRTS).
3. Repeat the Step 2.

Tx operation with FIFO

1. Select transmit mode (Interrupt or DMA mode).
2. Check the value of UMSTATn[0]. If the value is '1' (activating nCTS), users write the data to Tx FIFO register.

RS-232C interface

If users want to connect the UART to modem interface (instead of null modem), nRTS, nCTS, nDSR, nDTR, DCD and nRI signals are needed. In this case, the users can control these signals with general I/O ports by software because the AFC does not support the RS-232C interface.

Interrupt/DMA Request Generation

Each UART of the S3C2413X has five status (Tx/Rx/Error) signals: Overrun error, Frame error, Receive buffer data ready, Transmit buffer empty, and Transmit shifter empty, all of which are indicated by the corresponding UART status register (UTRSTATn/UERSTATn).

The overrun error and frame error are referred to as the receive error status, each of which can cause the receive error status interrupt request, if the receive-error-status-interrupt-enable bit is set to one in the control register, UCONn. When a receive-error-status-interrupt-request is detected, the signal causing the request can be identified by reading the value of UERSTSTn.

When the receiver transfers the data of the receive shifter to the receive FIFO register in FIFO mode and the number of received data reaches Rx FIFO Trigger Level, Rx interrupt is generated, if Receive mode in control register (UCONn) is selected as 1 (Interrupt request or polling mode).
In the Non-FIFO mode, transferring the data of the receive shifter to the receive holding register will cause Rx interrupt under the Interrupt request and polling mode.

When the transmitter transfers data from its transmit FIFO register to its transmit shifter and the number of data left in transmit FIFO reaches Tx FIFO Trigger Level, Tx interrupt is generated, if Transmit mode in control register is selected as Interrupt request or polling mode.
In the Non-FIFO mode, transferring data from the transmit holding register to the transmit shifter will cause Tx interrupt under the Interrupt request and polling mode.

If the Receive mode and Transmit mode in control register are selected as the DMAn request mode then DMAn request occurs instead of Rx or Tx interrupt in the situation mentioned above.

Table 10-1. Interrupts in Connection with FIFO

Type	FIFO Mode	Non-FIFO Mode
Rx interrupt	Generated whenever receive data reaches the trigger level of receive FIFO. Generated when the number of data in FIFO does not reaches Rx FIFO trigger Level and does not receive any data during 3 word time (receive time out). This interval follows the setting of Word Length bit.	Generated by the receive holding register whenever receive buffer becomes full.
Tx interrupt	Generated whenever transmit data reaches the trigger level of transmit FIFO (Tx FIFO trigger Level).	Generated by the transmit holding register whenever transmit buffer becomes empty.
Error interrupt	Generated when frame error has detected. Generated when it gets to the top of the receive FIFO without reading out data in it (overrun error).	Generated by all errors. However if another error occurs at the same time, only one interrupt is generated.

UART Error Status FIFO

UART has the error status FIFO besides the Rx FIFO register. The error status FIFO indicates which data, among FIFO registers, is received with an error. The error interrupt will be issued only when the data, which has an error, is ready to read out. To clear the error status FIFO, the URXHn with an error and UERSTATn must be read out.

For example,

It is assumed that the UART Rx FIFO receives A, B, C, and D characters sequentially and the frame error occurs while receiving 'B'.

The actual UART receive error will not generate any error interrupt because the character, which was received with an error, has not been read yet. The error interrupt will occur when the character is read out.

Figure 10-3. shows the UART receiving the four characters including the one error.

Time	Sequence Flow	Error Interrupt	Note
#0	When no character is read out	–	
#1	A, B, C, and D is received	–	
#2	After A is read out	The frame error (in B) interrupt occurs.	The 'B' has to be read out.
#3	After B is read out	–	
#4	After C is read out	–	
#5	After D is read out	–	

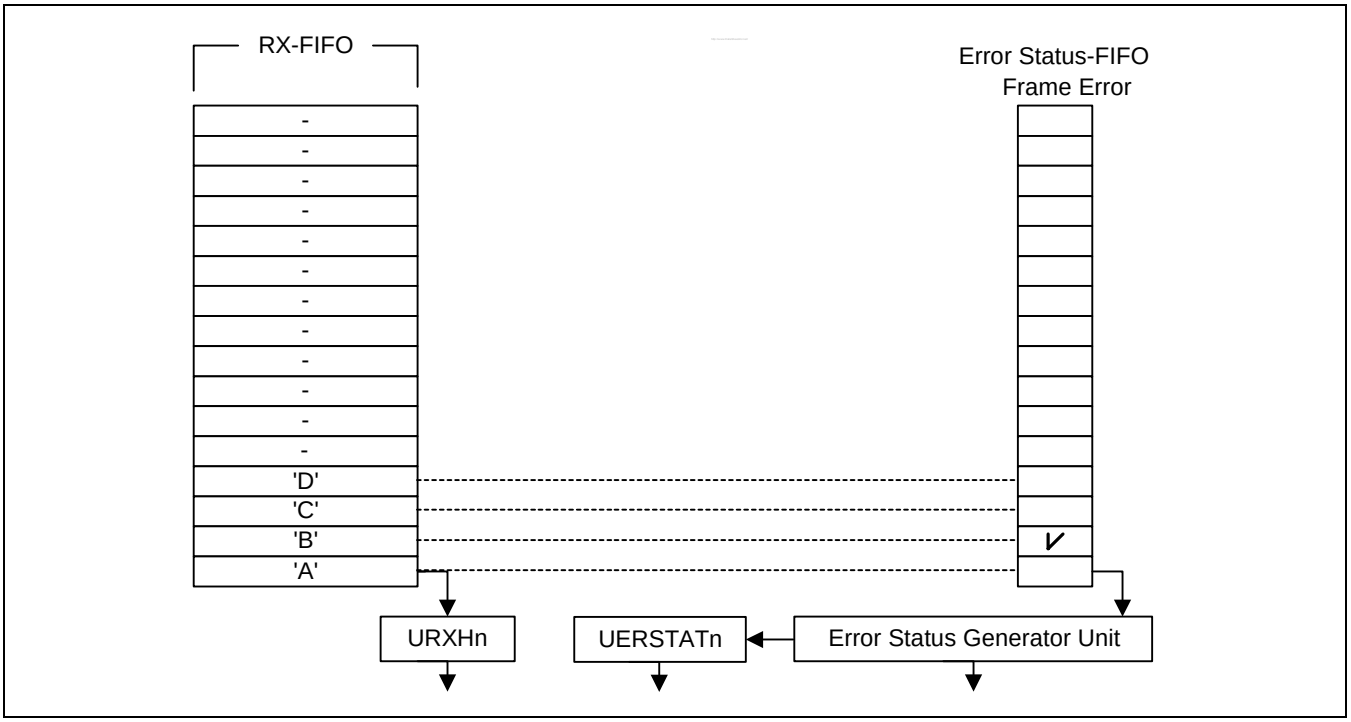


Figure 10-3. UART Receiving 4 Characters with 1 Error

Baud-Rate Generation

Each UART's baud-rate generator provides the serial clock for the transmitter and the receiver. The source clock for the baud-rate generator can be selected with the S3C2413X's internal system clock or UEXTCLK. In other words, dividend is selectable by setting Clock Selection of UCONn. The baud-rate clock is generated by dividing the source clock (PCLK or UEXTCLK) by 16 and a 16-bit divisor specified in the UART baud-rate divisor register (UBRDIVn). The UBRDIVn can be determined by the following expression:

UBRDIVn = (int)(PCLK/(bps x 16)) -1

Where, the divisor should be from 1 to (216-1).

For accurate UART operation, the S3C2413X also supports UEXTCLK as a dividend.
If the S3C2413X uses UEXTCLK, which is supplied by an external UART device or system, then the serial clock of UART is exactly synchronized with UEXTCLK. So, the user can get the more precise UART operation. The UBRDIVn can be determined:

UBRDIVn = (int)(UEXTCLK / (bps x 16)) –1

Where, the divisor should be from 1 to (2^{16}-1) and UEXTCLK should be smaller than PCLK.

For example, if the baud-rate is 115200 bps and PCLK or UEXTCLK is 40 MHz, UBRDIVn is determined:

UBRDIVn = (int)(40000000/(115200 x 16)) -1
= (int)(21.7) -1
= 21 -1 = 20

Baud-Rate Error Tolerance

UART Frame error should be less than 1.87%(3/160).

tUPCLK = (UBRDIVn + 1) x 16 x 1Frame / PCLK tUPCLK : Real UART Clock

tUEXACT = 1Frame / baud-rate tUEXACT : Ideal UART Clock

UART error = (tUPCLK – tUEXACT) / tUEXACT x 100%

NOTES:

1. 1Frame = start bit + data bit + parity bit + stop bit.
2. In specific condition, we can support baud rate up to 921.6K bps. For example, when PCLK is 60MHz,
   you can use baud rate of 921.6K bps under UART error of 1.69%.

Loopback Mode

The S3C2413X UART provides a test mode referred to as the Loopback mode, to aid in isolating faults in the communication link. This mode structurally enables the connection of RXD and TXD in the UART. In this mode, therefore, transmitted data is received to the receiver, via RXD. This feature allows the processor to verify the internal transmit and to receive the data path of each SIO channel. This mode can be selected by setting the loopback bit in the UART control register (UCONn).

Infra-Red (IR) Mode

The S3C2413X UART block supports infra-red (IR) transmission and reception, which can be selected by setting the Infra-red-mode bit in the UART line control register (ULCONn). Figure 10-4 illustrates how to implement the IR mode.

In IR transmit mode, the transmit pulse comes out at a rate of 3/16, the normal serial transmit rate (when the transmit data bit is zero); In IR receive mode, the receiver must detect the 3/16 pulsed period to recognize a zero value (see the frame timing diagrams shown in Figure 10-6 and 10-7).

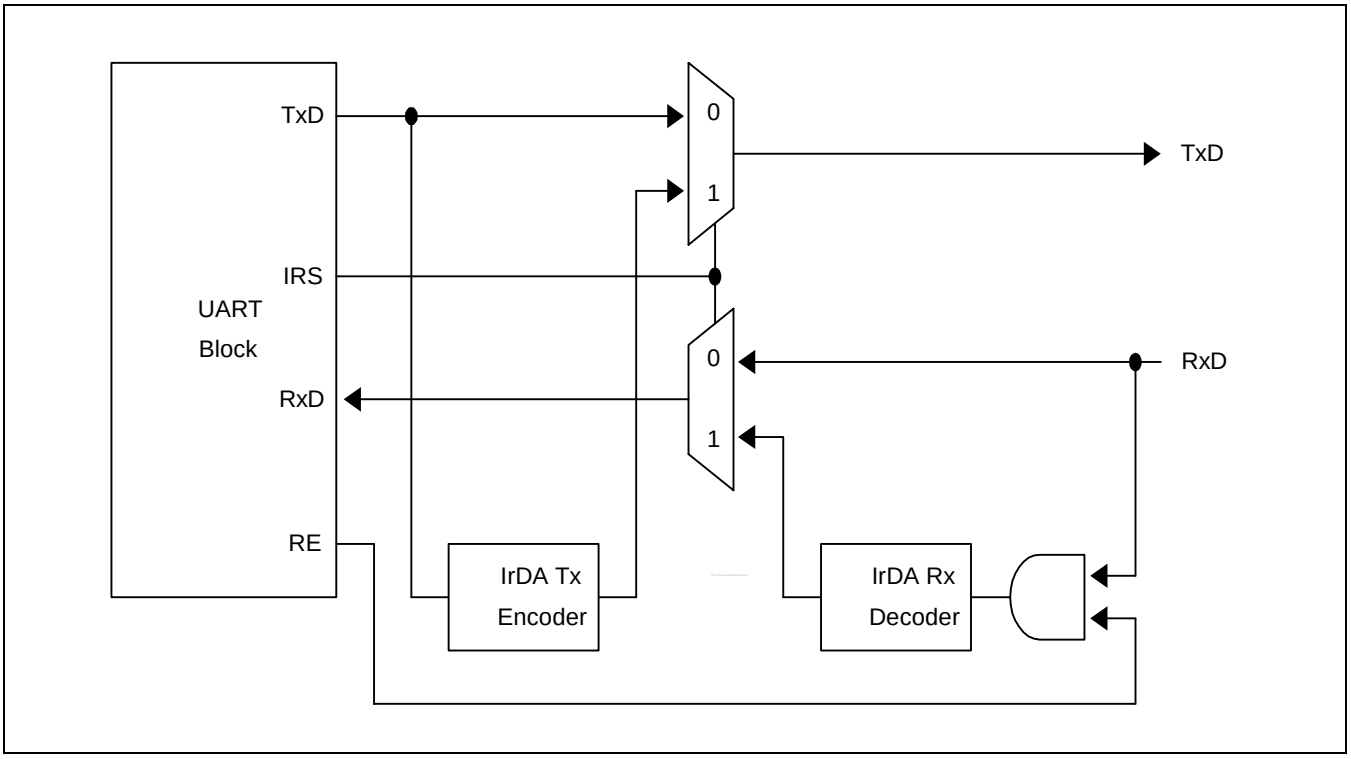


Figure 10-4. IrDA Function Block Diagram

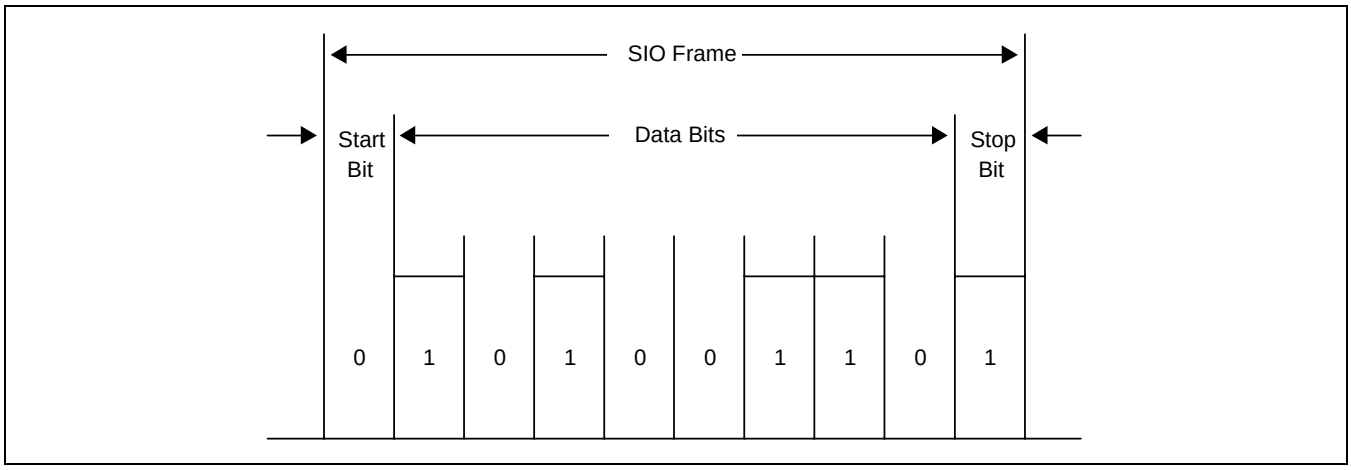


Figure 10-5. Serial I/O Frame Timing Diagram (Normal UART)

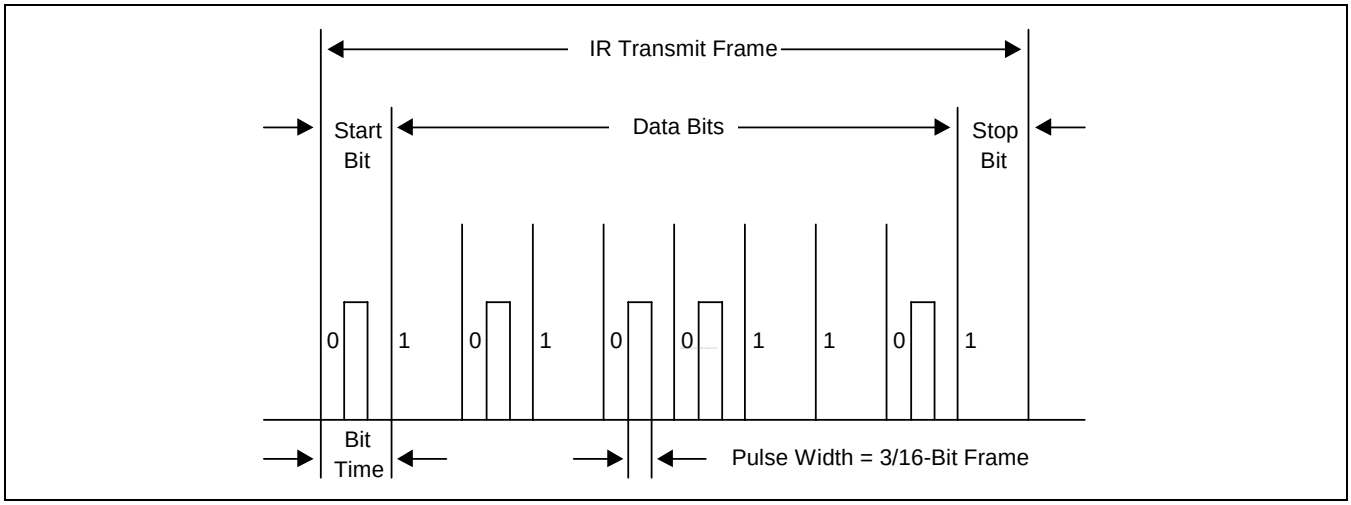


Figure 10-6. Infra-Red Transmit Mode Frame Timing Diagram

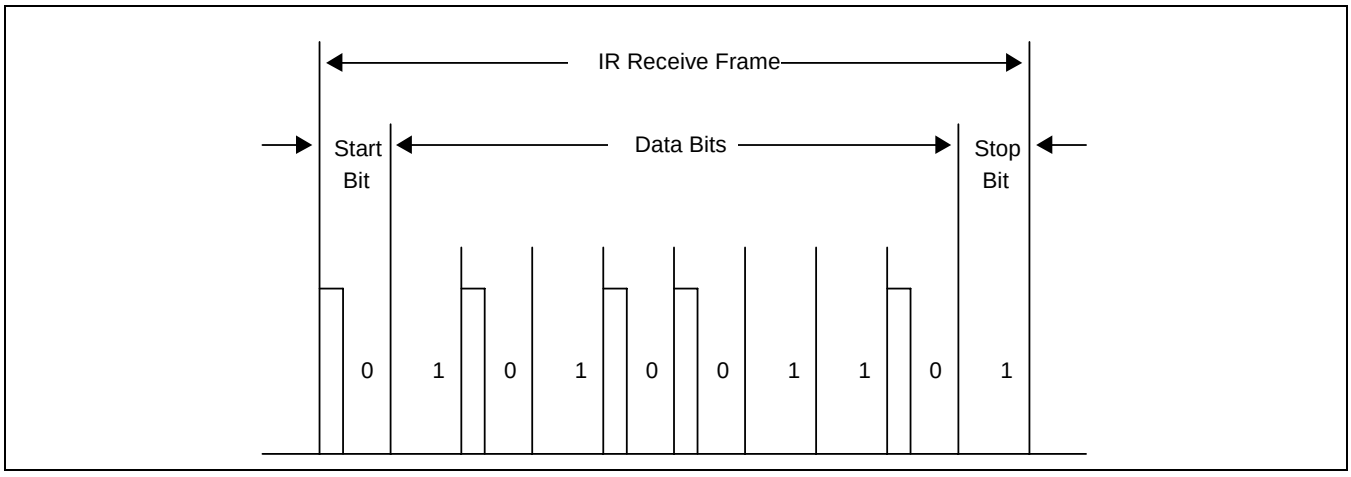


Figure 10-7. Infra-Red Receive Mode Frame Timing Diagram

UART SPECIAL REGISTERS

UART LINE CONTROL REGISTER

There are three UART line control registers including ULCON0, ULCON1, and ULCON2 in the UART block.

Register	Address	R/W	Description	Reset Value
ULCON0	0x50000000	R/W	UART channel 0 line control register	0x00
ULCON1	0x50004000	R/W	UART channel 1 line control register	0x00
ULCON2	0x50008000	R/W	UART channel 2 line control register	0x00

ULCONn	Bit	Description	Initial State
Reserved	[7]		0
Infra-Red Mode	[6]	Determine whether or not to use the Infra-Red mode. 0 = Normal mode operation 1 = Infra-Red Tx/Rx mode	0
Parity Mode	[5:3]	Specify the type of parity generation and checking during UART transmit and receive operation. 0xx = No parity 100 = Odd parity 101 = Even parity 110 = Parity forced/checked as 1 111 = Parity forced/checked as 0	000
Number of Stop Bit	[2]	Specify how many stop bits are to be used for end-of-frame signal. 0 = One stop bit per frame 1 = Two stop bit per frame	0
Word Length	[1:0]	Indicate the number of data bits to be transmitted or received per frame. 00 = 5-bit 01 = 6-bit 10 = 7-bit 11 = 8-bit	00

UART CONTROL REGISTER

There are three UART control registers including UCON0, UCON1 and UCON2 in the UART block.

Register	Address	R/W	Description	Reset Value
UCON0	0x50000004	R/W	UART channel 0 control register	0x00
UCON1	0x50004004	R/W	UART channel 1 control register	0x00
UCON2	0x50008004	R/W	UART channel 2 control register	0x00

UCONn	Bit	Description	Initial State
Clock Selection	[11:10]	Select PCLK or UEXTCLK for the UART baud rate. 10=PCLK : UBRDIVn = (int)(PCLK / (bps x 16)) -1 01=UEXTCLK(@GPH8) : UBRDIVn = (int)(UEXTCLK / (bps x 16)) -1 11=UARTCLK(from system controller) : UBRDIVn = (int)(UARTCLK / (bps x 16)) -1 Note) 00 is not used.	0
Tx Interrupt Type	[9]	Interrupt request type. 0 = Pulse (Interrupt is requested as soon as the Tx buffer becomes empty in Non-FIFO mode or reaches Tx FIFO Trigger Level in FIFO mode.) 1 = Level (Interrupt is requested while Tx buffer is empty in Non-FIFO mode or reaches Tx FIFO Trigger Level in FIFO mode.)	0
Rx Interrupt Type	[8]	Interrupt request type. 0 = Pulse (Interrupt is requested the instant Rx buffer receives the data in Non-FIFO mode or reaches Rx FIFO Trigger Level in FIFO mode.) 1 = Level (Interrupt is requested while Rx buffer is receiving data in Non-FIFO mode or reaches Rx FIFO Trigger Level in FIFO mode.)	0
Rx Time Out Enable	[7]	Enable/Disable Rx time out interrupt when UART FIFO is enabled. The interrupt is a receive interrupt. 0 = Disable 1 = Enable	0
Rx Error Status Interrupt Enable	[6]	Enable the UART to generate an interrupt upon an exception, such as a frame error, or overrun error during a receive operation. 0 = Do not generate receive error status interrupt. 1 = Generate receive error status interrupt.	0
Loopback Mode	[5]	Setting loopback bit to 1 causes the UART to enter the loopback mode. This mode is provided for test purposes only. 0 = Normal operation 1 = Loopback mode	0
Reserved	[4]	Reserved	0

UART CONTROL REGISTER (Continued)

UCONn	Bit	Description	Initial State
Transmit Mode	[3:2]	Determine which function is currently able to write Tx data to the UART transmit buffer register. (UART Tx Enable/Disable) 00 = Disable 01 = Interrupt request or polling mode 10 = DMA request (DMA Request source of UART_n[0]) 11 = DMA request (DMA Request source of UART_n[1])	00
Receive Mode	[1:0]	Determine which function is currently able to read data from UART receive buffer register. (UART Rx Enable/Disable) 00 = Disable 01 = Interrupt request or polling mode 10 = DMA request (DMA Request source of UART_n[0]), 11 = DMA request (DMA Request source of UART_n[1])	00

NOTE: When the UART does not reach the FIFO trigger level and does not receive data during 3 word time in DMA receive mode with FIFO, the Rx interrupt will be generated (receive time out), and the users should check the FIFO status and read out the rest.

UART FIFO CONTROL REGISTER

There are three UART FIFO control registers including UFCON0, UFCON1 and UFCON2 in the UART block.

Register	Address	R/W	Description	Reset Value
UFCON0	0x50000008	R/W	UART channel 0 FIFO control register	0x0
UFCON1	0x50004008	R/W	UART channel 1 FIFO control register	0x0
UFCON2	0x50008008	R/W	UART channel 2 FIFO control register	0x0

UFCONn	Bit	Description	Initial State
Tx FIFO Trigger Level	[7:6]	Determine the trigger level of transmit FIFO. 00 = Empty 01 = 16-byte 10 = 32-byte 11 = 48-byte	00
Rx FIFO Trigger Level	[5:4]	Determine the trigger level of receive FIFO. 00 = 1-byte 01 = 8-byte 10 = 16-byte 11 = 32-byte	00
Reserved	[3]		0
Tx FIFO Reset	[2]	Auto-cleared after resetting FIFO 0 = Normal 1= Tx FIFO reset	0
Rx FIFO Reset	[1]	Auto-cleared after resetting FIFO 0 = Normal 1= Rx FIFO reset	0
FIFO Enable	[0]	0 = Disable 1 = Enable	0

NOTE: When the UART does not reach the FIFO trigger level and does not receive data during 3 word time in DMA receive mode with FIFO, the Rx interrupt will be generated (receive time out), and the users should check the FIFO status and read out the rest.

UART MODEM CONTROL REGISTER

There are two UART MODEM control registers including UMCON0 and UMCON1 in the UART block.

Register	Address	R/W	Description	Reset Value
UMCON0	0x5000000C	R/W	UART channel 0 Modem control register	0x0
UMCON1	0x5000400C	R/W	UART channel 1 Modem control register	0x0
Reserved	0x5000800C	-	Reserved	Undef

UMCONn	Bit	Description	Initial State
RTS trigger Level	[7:5]	When AFC bit is enabled, these bits determine when to inactivate nRTS signal. 000 = When RX FIFO contains 63 bytes. 001 = When RX FIFO contains 56 bytes. 010 = When RX FIFO contains 48 bytes. 011 = When RX FIFO contains 40 bytes. 100 = When RX FIFO contains 32 bytes. 101 = When RX FIFO contains 24 bytes. 110 = When RX FIFO contains 16 bytes. 111 = When RX FIFO contains 8 bytes.	000
Auto Flow Control (AFC)	[4]	0 = Disable 1 = Enable	0
Reserved	[3:1]	These bits must be 0's	00
Request to Send	[0]	If AFC bit is enabled, this value will be ignored. In this case the S3C2413X will control nRTS automatically. If AFC bit is disabled, nRTS must be controlled by software. 0 = 'H' level (Inactivate nRTS) 1 = 'L' level (Activate nRTS)	0

NOTE: UART 2 does not support AFC function, because the S3C2413X has no nRTS2 and nCTS2.

UART TX/RX STATUS REGISTER

There are three UART Tx/Rx status registers including UTRSTAT0, UTRSTAT1 and UTRSTAT2 in the UART block.

Register	Address	R/W	Description	Reset Value
UTRSTAT0	0x50000010	R	UART channel 0 Tx/Rx status register	0x6
UTRSTAT1	0x50004010	R	UART channel 1 Tx/Rx status register	0x6
UTRSTAT2	0x50008010	R	UART channel 2 Tx/Rx status register	0x6

UTRSTATn	Bit	Description	Initial State
Transmitter empty	[2]	Set to 1 automatically when the transmit buffer register has no valid data to transmit and the transmit shift register is empty. 0 = Not empty 1 = Transmitter (transmit buffer & shifter register) empty	1
Transmit buffer empty	[1]	Set to 1 automatically when transmit buffer register is empty. 0 =The buffer register is not empty 1 = Empty (In Non-FIFO mode, Interrupt or DMA is requested. In FIFO mode, Interrupt or DMA is requested, when Tx FIFO Trigger Level is set to 00 (Empty)) If the UART uses the FIFO, users should check Tx FIFO Count bits and Tx FIFO Full bit in the UFSTAT register instead of this bit.	1
Receive buffer data ready	[0]	Set to 1 automatically whenever receive buffer register contains valid data, received over the RXDn port. 0 = Empty 1 = The buffer register has a received data (In Non-FIFO mode, Interrupt or DMA is requested) If the UART uses the FIFO, users should check Rx FIFO Count bits and Rx FIFO Full bit in the UFSTAT register instead of this bit.	0

UART ERROR STATUS REGISTER

There are three UART Rx error status registers including UERSTAT0, UERSTAT1 and UERSTAT2 in the UART block.

Register	Address	R/W	Description	Reset Value
UERSTAT0	0x50000014	R	UART channel 0 Rx error status register	0x0
UERSTAT1	0x50004014	R	UART channel 1 Rx error status register	0x0
UERSTAT2	0x50008014	R	UART channel 2 Rx error status register	0x0

UERSTATn	Bit	Description	Initial State
Break Detect	[3]	Set to 1 automatically to indicate that a break signal has been received. 0 = No break receive 1 = Break receive (Interrupt is requested.)	0
Frame Error	[2]	Set to 1 automatically whenever a frame error occurs during receive operation. 0 = No frame error during receive 1 = Frame error (Interrupt is requested.)	0
Parity Error	[1]	Set to 1 automatically whenever a parity error occurs during receive operation. 0 = No parity error during receive 1 = Parity error (Interrupt is requested.)	0
Overrun Error	[0]	Set to 1 automatically whenever an overrun error occurs during receive operation. 0 = No overrun error during receive 1 = Overrun error (Interrupt is requested.)	0

NOTE: These bits (UERSATn[3:0]) are automatically cleared to 0 when the UART error status register is read.

UART FIFO STATUS REGISTER

There are three UART FIFO status registers including UFSTAT0, UFSTAT1 and UFSTAT2 in the UART block.

Register	Address	R/W	Description	Reset Value
UFSTAT0	0x50000018	R	UART channel 0 FIFO status register	0x00
UFSTAT1	0x50004018	R	UART channel 1 FIFO status register	0x00
UFSTAT2	0x50008018	R	UART channel 2 FIFO status register	0x00

UFSTATn	Bit	Description	Initial State
Reserved	[15]	Reserved.	0
Tx FIFO Full	[14]	Set to 1 automatically whenever transmit FIFO is full during transmit operation 0 = 0-byte ≤ Tx FIFO data ≤ 63-byte 1 = Full	0
Tx FIFO Count	[13:8]	Number of data in Tx FIFO	0
Reserved	[7]	Reserved.	0
Rx FIFO Full	[6]	Set to 1 automatically whenever receive FIFO is full during receive operation 0 = 0-byte ≤ Rx FIFO data ≤ 63-byte 1 = Full	0
Rx FIFO Count	[5:0]	Number of data in Rx FIFO	0

UART MODEM STATUS REGISTER

There are two UART modem status registers including UMSTAT0 and UMSTAT1 in the UART block.

Register	Address	R/W	Description	Reset Value
UMSTAT0	0x5000001C	R	UART channel 0 Modem status register	0x0
UMSTAT1	0x5000401C	R	UART channel 1 Modem status register	0x0
Reserved	0x5000801C	–	Reserved	Undef

UMSTAT0	Bit	Description	Initial State
Delta CTS	[4]	Indicate that the nCTS input to the S3C2413X has changed state since the last time it was read by CPU. (Refer to Figure 10-8.) 0 = Has not changed 1 = Has changed	0
Reserved	[3:1]		0
Clear to Send	[0]	0 = CTS signal is not activated (nCTS pin is high.) 1 = CTS signal is activated (nCTS pin is low.)	0

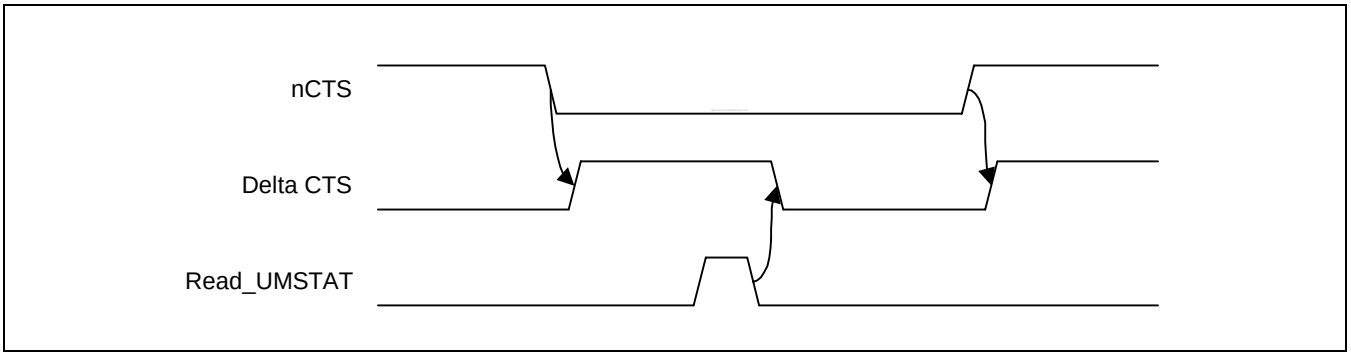


Figure 10-8. nCTS and Delta CTS Timing Diagram

UART TRANSMIT BUFFER REGISTER (HOLDING REGISTER & FIFO REGISTER)

There are three UART transmit buffer registers including UTXH0, UTXH1 and UTXH2 in the UART block. UTXHn has an 8-bit data for transmission data.

Register	Address	R/W	Description	Reset Value
UTXH0	0x50000020(L) 0x50000023(B)	W (by byte)	UART channel 0 transmit buffer register	0x00
UTXH1	0x50004020(L) 0x50004023(B)	W (by byte)	UART channel 1 transmit buffer register	0x00
UTXH2	0x50008020(L) 0x50008023(B)	W (by byte)	UART channel 2 transmit buffer register	0x00

UTXHn	Bit	Description	Initial State
TXDATAn	[7:0]	Transmit data for UARTn	0x00

NOTE: (L): The endian mode is Little endian.
(B): The endian mode is Big endian.

UART RECEIVE BUFFER REGISTER (HOLDING REGISTER & FIFO REGISTER)

There are three UART receive buffer registers including URXH0, URXH1 and URXH2 in the UART block. URXHn has an 8-bit data for received data.

Register	Address	R/W	Description	Reset Value
URXH0	0x50000024(L) 0x50000027(B)	R (by byte)	UART channel 0 receive buffer register	0x00
URXH1	0x50004024(L) 0x50004027(B)	R (by byte)	UART channel 1 receive buffer register	0x00
URXH2	0x50008024(L) 0x50008027(B)	R (by byte)	UART channel 2 receive buffer register	0x00

URXHn	Bit	Description	Initial State
RXDATAn	[7:0]	Receive data for UARTn	0x00

NOTE: When an overrun error occurs, the URXHn must be read. If not, the next received data will also make an overrun error, even though the overrun bit of UERSTATn had been cleared.

UART BAUD RATE DIVISOR REGISTER

There are three UART baud rate divisor registers including UBRDIV0, UBRDIV1 and UBRDIV2 in the UART block.
The value stored in the baud rate divisor register (UBRDIVn) and dividing slot register(UDIVSLOTn), are used to determine the serial Tx/Rx clock rate (baud rate) as follows:

DIV_VAL = UBRDIVn + (num of 1's in UDIVSLOTn)/16

DIV_VAL = (PCLK / (bps x 16)) –1

or

DIV_VAL = (UCLK / (bps x 16)) –1

Where, the divisor should be from 1 to (2^{16}-1) and UCLK should be smaller than PCLK.Using UDIVSLOT, you can make more accurate baud rate.For example, if the baud-rate is 115200 bps and PCLK or UCLK is 40 MHz, UBRDIVn and UDIVSLOTn are:

DIV_VAL = (40000000 / (115200 x 16)) -1
= 21.7 -1
= 20.7

UBRDIVn = 20 (integer part of DIV_VAL)

(num of 1's in UDIVSLOTn)/16 = 0.7

then, (num of 1's in UDIVSLOTn) = 11

so, UDIVSLOTn can be *16'b1110_1110_1110_1010* or *16'b0111_0111_0111_0101*, etc.

Register	Address	R/W	Description	Reset Value
UBRDIV0	0x50000028	R/W	Baud rate divisior register 0	0x0000
UBRDIV1	0x50004028	R/W	Baud rate divisior register 1	0x0000
UBRDIV2	0x50008028	R/W	Baud rate divisior register 2	0x0000

UBRDIVn	Bit	Description	Initial State
UBRDIV	[15:0]	Baud rate division value UBRDIVn > 0	0x0000

Register	Address	R/W	Description	Reset Value
UDIVSLOT0	0x5000002C	R/W	Baud rate divisior register 0	0x0000
UDIVSLOT1	0x5000402C	R/W	Baud rate divisior register 1	0x0000
UDIVSLOT2	0x5000802C	R/W	Baud rate divisior register 2	0x0000

UBRDIVn	Bit	Description	Initial State
UDIVSLOT	[15:0]	Select the slot where clock generator divide clock source by (UBRDIV + 2)	0x0000

11 USB HOST CONTROLLER

OVERVIEW

S3C2413X supports 2-port USB host interface as follows:

- OHCI Rev 1.0 compatible
- USB Rev1.1 compatible
- Two down stream ports
- Support for both LowSpeed and FullSpeed USB devices

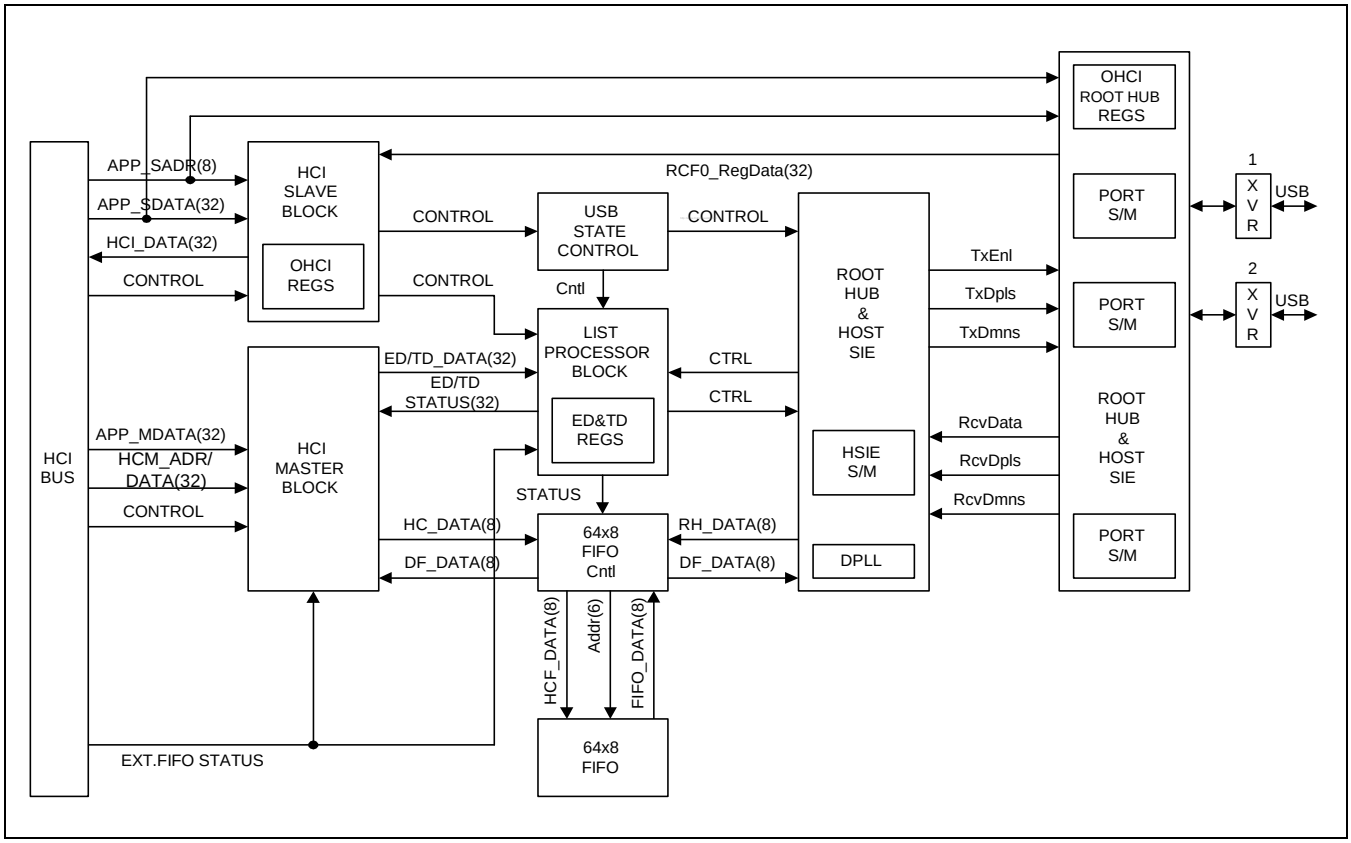


Figure 11-1. USB Host Controller Block Diagram

USB HOST CONTROLLER SPECIAL REGISTERS

The S3C2413X USB host controller complies with OHCI Rev 1.0. Refer to Open Host Controller Interface Rev 1.0 specification for detail information.

Table 11-1. OHCI Registers for USB Host Controller

Register	Base Address	R/W	Description	Reset Value
HcRevision	0x49000000	–	Control and status group	–
HcControl	0x49000004	–		–
HcCommonStatus	0x49000008	–		–
HcInterruptStatus	0x4900000C	–		–
HcInterruptEnable	0x49000010	–		–
HcInterruptDisable	0x49000014	–		–
HcHCCA	0x49000018	–	Memory pointer group	–
HcPeriodCuttentED	0x4900001C	–		–
HcControlHeadED	0x49000020	–		–
HcControlCurrentED	0x49000024	–		–
HcBulkHeadED	0x49000028	–		–
HcBulkCurrentED	0x4900002C	–		–
HcDoneHead	0x49000030	–		–
HcRmInterval	0x49000034	–	Frame counter group	–
HcFmRemaining	0x49000038	–		–
HcFmNumber	0x4900003C	–		–
HcPeriodicStart	0x49000040	–		–
HcLSThreshold	0x49000044	–		–
HcRhDescriptorA	0x49000048	–	Root hub group	–
HcRhDescriptorB	0x4900004C	–		–
HcRhStatus	0x49000050	–		–
HcRhPortStatus1	0x49000054	–		–
HcRhPortStatus2	0x49000058	–		–

12 USB DEVICE CONTROLLER

OVERVIEW

Universal Serial Bus (USB) device controller is designed to provide a high performance full speed function controller solution with DMA interface. USB device controller allows bulk transfer with DMA, interrupt transfer and control transfer.

USB device controller supports:

- Full speed USB device controller compatible with the USB specification version 1.1
- DMA interface for bulk transfer
- Five endpoints with FIFO
  EP0: 16byte (Register)
  EP1: 64byte IN/OUT FIFO (dual port asynchronous RAM): interrupt or DMA
  EP2: 64byte IN/OUT FIFO (dual port asynchronous RAM): interrupt or DMA
  EP3: 64byte IN/OUT FIFO (dual port asynchronous RAM): interrupt or DMA
  EP4: 64byte IN/OUT FIFO (dual port asynchronous RAM): interrupt or DMA
- Integrated USB Transceiver

FEATURE

- Fully compliant with USB Specification Version 1.1
- Full speed (12Mbps) device
- Integrated USB Transceiver
- Supports control, interrupt and bulk transfer
- Five endpoints with FIFO:
  One bi-directional control endpoint with 16-byte FIFO (EP0)
  Four bi-directional bulk endpoints with 64-byte FIFO (EP1, EP2, EP3, and EP4)
- Supports DMA interface for receive and transmit bulk endpoints. (EP1, EP2, EP3, and EP4)
- Independent 64byte receive and transmit FIFO to maximize throughput
- Supports suspend and remote wakeup function

NOTE:

PCLK should be more than 20MHz to use USB Device Controller stably.

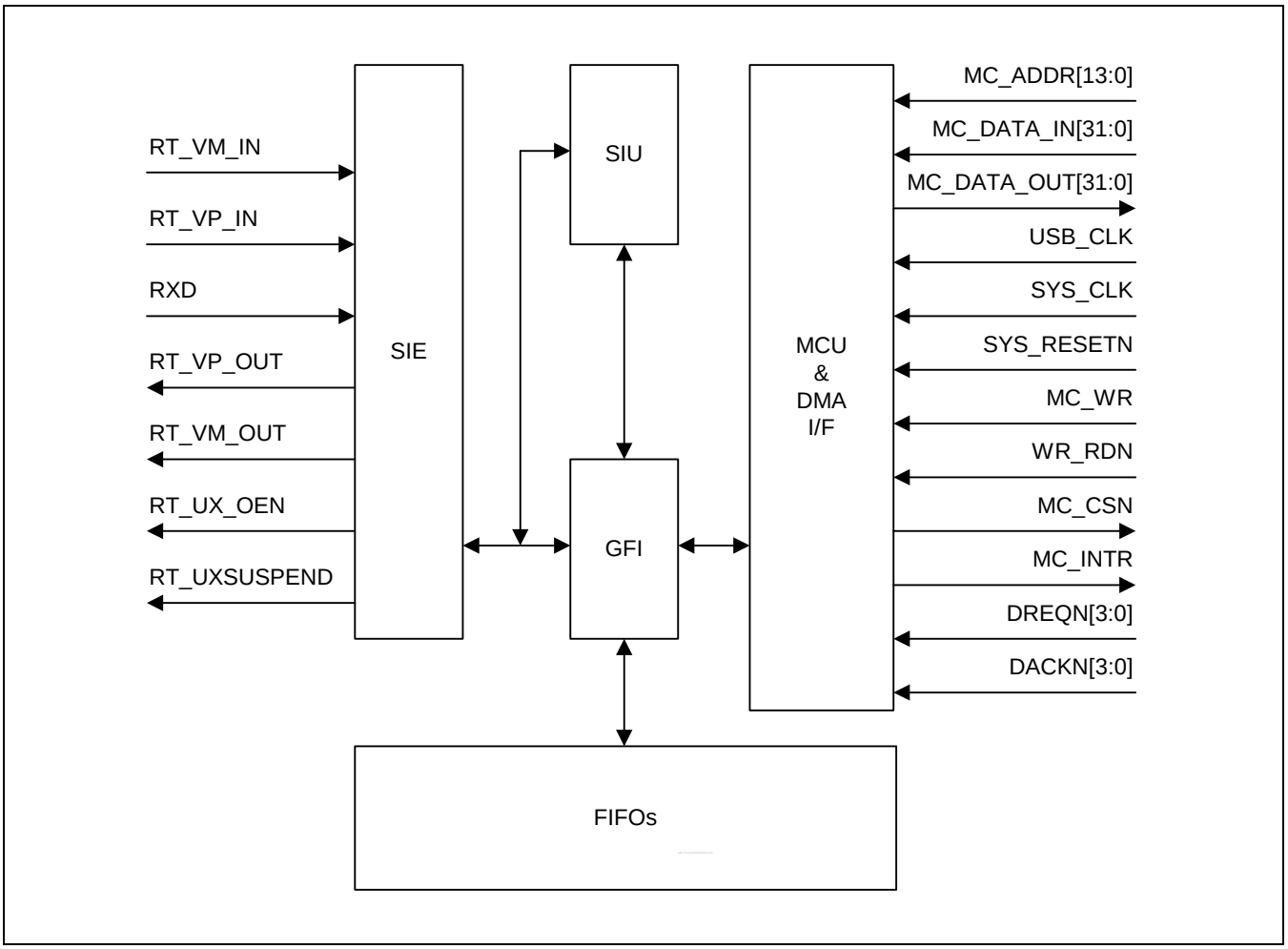


Figure 12-1. USB Device Controller Block Diagram

USB DEVICE CONTROLLER SPECIAL REGISTERS

This section describes detailed functionalities about register sets of USB device controller.
All special function register is byte-accessible or word-accessible. If you access byte mode offset-address is different in little endian and big endian. All reserved bit is zero.
Common indexed registers depend on INDEX register (INDEX_REG) (offset address: 0x178) value. For example if you want to write EP0 CSR register, you must write "0x00" on the INDEX_REG before writing IN_CSR1 register.

NOTE:

All register must be resettled after performing Host Reset Signaling.

Register Name	Description	Offset Address
NON INDEXED REGISTERS		
FUNC_ADDR_REG	Function address register	0x140(L) / 0x143(B)
PWR_REG	Power management register	0x144(L) / 0x147(B)
EP_INT_REG (EP0–EP4)	Endpoint interrupt register	0x148(L) / 0x14B(B)
USB_INT_REG	USB interrupt register	0x158(L) / 0x15B(B)
EP_INT_EN_REG (EP0–EP4)	Endpoint interrupt enable register	0x15C(L) / 0x15F(B)
USB_INT_EN_REG	USB Interrupt enable register	0x16C(L) / 0x16F(B)
FRAME_NUM1_REG	Frame number 1 register	0x170(L) / 0x173(B)
FRAME_NUM2_REG	Frame number 2 register	0x174(L) / 0x177(B)
INDEX_REG	Index register	0x178(L) / 0x17B(B)
EP0_FIFO_REG	Endpoint0 FIFO register	0x1C0(L) / 0x1C3(B)
EP1_FIFO_REG	Endpoint1 FIFO register	0x1C4(L) / 0x1C7(B)
EP2_FIFO_REG	Endpoint2 FIFO register	0x1C8(L) / 0x1CB(B)
EP3_FIFO_REG	Endpoint3 FIFO register	0x1CC(L) / 0x1CF(B)
EP4_FIFO_REG	Endpoint4 FIFO register	0x1D0(L) / 0x1D3(B)
EP1_DMA_CON	Endpoint1 DMA control register	0x200(L) / 0x203(B)
EP1_DMA_UNIT	Endpoint1 DMA unit counter register	0x204(L) / 0x207(B)
EP1_DMA_FIFO	Endpoint1 DMA FIFO counter register	0x208(L) / 0x20B(B)
EP1_DMA_TTC_L	Endpoint1 DMA transfer counter low-byte register	0x20C(L) / 0x20F(B)
EP1_DMA_TTC_M	Endpoint1 DMA transfer counter middle-byte register	0x210(L) / 0x213(B)
EP1_DMA_TTC_H	Endpoint1 DMA transfer counter high-byte register	0x214(L) / 0x217(B)
EP2_DMA_CON	Endpoint2 DMA control register	0x218(L) / 0x21B(B)
EP2_DMA_UNIT	Endpoint2 DMA unit counter register	0x21C(L) / 0x21F(B)
EP2_DMA_FIFO	Endpoint2 DMA FIFO counter register	0x220(L) / 0x223(B)
EP2_DMA_TTC_L	Endpoint2 DMA transfer counter low-byte register	0x224(L) / 0x227(B)

USB DEVICE CONTROLLER SPECIAL REGISTERS (Continued)

Register Name	Description	Offset Address
EP2_DMA_TTC_M	Endpoint2 DMA transfer counter middle-byte register	0x228(L) / 0x22B(B)
EP2_DMA_TTC_H	Endpoint2 DMA transfer counter high-byte register	0x22C(L) / 0x22F(B)
EP3_DMA_CON	Endpoint3 DMA control register	0x240(L) / 0x243(B)
EP3_DMA_UNIT	Endpoint3 DMA unit counter register	0x244(L) / 0x247(B)
EP3_DMA_FIFO	Endpoint3 DMA FIFO counter register	0x248(L) / 0x24B(B)
EP3_DMA_TTC_L	Endpoint3 DMA transfer counter low-byte register	0x24C(L) / 0x24F(B)
EP3_DMA_TTC_M	Endpoint3 DMA transfer counter middle-byte register	0x250(L) / 0x253(B)
EP3_DMA_TTC_H	Endpoint3 DMA transfer counter high-byte register	0x254(L) / 0x257(B)
EP4_DMA_CON	Endpoint4 DMA control register	0x258(L) / 0x25B(B)
EP4_DMA_UNIT	Endpoint4 DMA unit counter register	0x25C(L) / 0x25F(B)
EP4_DMA_FIFO	Endpoint4 DMA FIFO counter register	0x260(L) / 0x263(B)
EP4_DMA_TTC_L	Endpoint4 DMA transfer counter low-byte register	0x264(L) / 0x267(B)
EP4_DMA_TTC_M	Endpoint4 DMA transfer counter middle-byte register	0x268(L) / 0x26B(B)
EP4_DMA_TTC_H	Endpoint4 DMA transfer counter high-byte register	0x26C(L) / 0x26F(B)
COMMON INDEXED REGISTERS		
MAXP_REG	Endpoint MAX packet register	0x180(L) / 0x183(B)
IN INDEXED REGISTERS		
IN_CSR1_REG/EP0_CSR	EP In control status register 1/EP0 control status register	0x184(L) / 0x187(B)
IN_CSR2_REG	EP In control status register 2	0x188(L) / 0x18B(B)
OUT INDEXED REGISTERS		
OUT_CSR1_REG	EP out control status register 1	0x190(L) / 0x193(B)
OUT_CSR2_REG	EP out control status register 2	0x194(L) / 0x197(B)
OUT_FIFO_CNT1_REG	EP out write count register 1	0x198(L) / 0x19B(B)
OUT_FIFO_CNT2_REG	EP out write count register 2	0x19C(L) / 0x19F(B)

FUNCTION ADDRESS REGISTER (FUNC_ADDR_REG)

This register maintains the USB device controller address assigned by the host. The Micro Controller Unit (MCU) writes the value received through a SET_ADDRESS descriptor to this register. This address is used for the next token.

Register	Address	R/W	Description	Reset Value
FUNC_ADDR_ REG	0x52000140(L) 0x52000143(B)	R/W (byte)	Function address register	0x00

FUNC_ADDR_REG	Bit	MCU	USB	Description	Initial State
ADDR_UPDATE	[7]	R /SET	R /CLEAR	Set by the MCU whenever it updates the FUNCTION_ADDR field in this register. This bit will be cleared by USB when DATA_END bit in EP0_CSR register.	0
FUNCTION_ADDR	[6:0]	R/W	R	The MCU write the unique address, assigned by host, to this field.	00

POWER MANAGEMENT REGISTER (PWR_REG)

This register acts as a power control register in the USB block.

Register	Address	R/W	Description	Reset Value
PWR_REG	0x52000144(L) 0x52000147(B)	R/W (byte)	Power management register	0x00

PWR_ADDR	Bit	MCU	USB	Description	Initial State
Reserved	[7:4]	–	–	–	–
USB_RESET	[3]	R	SET	Set by the USB if reset signaling is received from the host. This bit remains set as long as reset signaling persists on the bus	0
MCU_RESUME	[2]	R/W	R /CLEAR	Set by the MCU for MCU Resume. The USB generates the resume signaling during 10ms, if this bit is set in suspend mode.	
SUSPEND_MODE	[1]	R	SET /CLEAR	Set by USB automatically when the device enter into suspend mode. It is cleared under the following conditions: 1) The MCU clears the MCU_RESUME bit by writing "0", in order to end remote resume signaling. 2) The resume signal form host is received.	0
SUSPEND_EN	[0]	R/W	R	Suspend mode enable control bit 0 = Disable (default). The device will not enter suspend mode. 1 = Enable suspend mode.	0

INTERRUPT REGISTER (EP_INT_REG/USB_INT_REG)

The USB core has two interrupt registers.
These registers act as status registers for the MCU when it is interrupted. The bits are cleared by writing a "1" (not "0") to each bit that was set.
Once the MCU is interrupted, MCU should read the contents of interrupt-related registers and write back to clear the contents if it is necessary.

Register	Address	R/W	Description	Reset Value
EP_INT_REG	0x52000148(L) 0x5200014B(B)	R/W (byte)	EP interrupt pending/clear register	0x00

EP_INT_REG	Bit	MCU	USB	Description	Initial State
EP1~EP4 Interrupt	[4:1]	R /CLEAR	SET	**For BULK/INTERRUPT IN endpoints:** Set by the USB under the following conditions: 1. IN_PKT_RDY bit is cleared. 2. FIFO is flushed 3. SENT_STALL set. **For BULK/INTERRUPT OUT endpoints:** Set by the USB under the following conditions: 1. Sets OUT_PKT_RDY bit 2. Sets SENT_STALL bit **NOTE:** Conditions 1 and 2 are mutually exclusive.	0
EP0 Interrupt	[0]	R /CLEAR	SET	Correspond to endpoint 0 interrupt. Set by the USB under the following conditions: 1. OUT_PKT_RDY bit is set. 2. IN_PKT_RDY bit is cleared. 3. SENT_STALL bit is set 4. SETUP_END bit is set 5. DATA_END bit is cleared (it indicates the end of control transfer).	0

INTERRUPT REGISTER (EP_INT_REG/USB_INT_REG) (Continued)

Register	Address	R/W	Description	Reset Value
USB_INT_REG	0x52000158(L) 0x5200015B(B)	R/W (byte)	USB interrupt pending/clear register	0x00

USB_INT_REG	Bit	MCU	USB	Description	Initial State
RESET Interrupt	[2]	R /CLEAR	SET	Set by the USB when it receives reset signaling.	0
RESUME Interrupt	[1]	R /CLEAR	SET	Set by the USB when it receives resume signaling, *while in Suspend mode*. If the resume occurs due to a USB reset, then the MCU is first interrupted with a RESUME interrupt. Once the clocks resume and the SE0 condition persists for 2.5us, USB RESET interrupt will be asserted.	0
SUSPEND Interrupt	[0]	R /CLEAR	SET	Set by the USB when it receives suspend signalizing. This bit is set whenever there is no activity for 3ms on the bus. Thus, if the MCU does not stop the clock after the first suspend interrupt, it will continue to be interrupted every 3ms as long as there is no activity on the USB bus. By default, this interrupt is disabled.	0

NOTE: If the RESET interrupt is occurred, all USB device registers should be re-configured.

INTERRUPT ENABLE REGISTER (EP_INT_EN_REG/USB_INT_EN_REG)

Corresponding to each interrupt register, The USB device controller also has two interrupt enable registers (except resume interrupt enable). By default, usb reset interrupt is enabled.

If bit = 0, the interrupt is disabled.
If bit = 1, the interrupt is enabled.

Register	Address	R/W	Description	Reset Value
EP_INT_EN_REG	0x5200015C(L) 0x5200015F(B)	R/W (byte)	Determine which interrupt is enabled	0xFF

EP_INT_EN_REG	Bit	MCU	USB	Description	Initial State
EP4_INT_EN	[4]	R/W	R	EP4 Interrupt Enable bit 0 = Interrupt disable 1 = Enable	1
EP3_INT_EN	[3]	R/W	R	EP3 Interrupt Enable bit 0 = Interrupt disable 1 = Enable	1
EP2_INT_EN	[2]	R/W	R	EP2 Interrupt Enable bit 0 = Interrupt disable 1 = Enable	1
EP1_INT_EN	[1]	R/W	R	EP1 Interrupt Enable bit 0 = Interrupt disable 1 = Enable	1
EP0_INT_EN	[0]	R/W	R	EP0 Interrupt Enable bit 0 = Interrupt disable 1 = Enable	1

Register	Address	R/W	Description	Reset Value
USB_INT_EN_ REG	0x5200016C(L) 0x5200016F(B)	R/W (byte)	Determine which interrupt is enabled	0x04

INT_MASK_REG	Bit	MCU	USB	Description	Initial State
RESET_INT_EN	[2]	R/W	R	Reset interrupt enable bit 0 = Interrupt disable 1 = Enable	1
Reserved	[1]	–	–	–	0
SUSPEND_INT_ EN	[0]	R/W	R	Suspend interrupt enable bit 0 = Interrupt disable 1 = Enable	0

FRAME NUMBER REGISTER (FPAME_NUM1_REG/FRAME_NUM2_REG)

When the host transfers USB packets, each Start Of Frame (SOF) packet includes a frame number. The USB device controller catches this frame number and loads it into this register automatically.

Register	Address	R/W	Description	Reset Value
FRAME_NUM1_ REG	0x52000170(L) 0x52000173(B)	R (byte)	Frame number lower byte register	0x00

FRAME_NUM_ REG	Bit	MCU	USB	Description	Initial State
FRAME_NUM1	[7:0]	R	W	Frame number lower byte value	00

Register	Address	R/W	Description	Reset Value
FRAME_NUM2_ REG	0x52000174(L) 0x52000177(B)	R (byte)	Frame number higher byte register	0x00

FRAME_NUM_ REG	Bit	MCU	USB	Description	Initial State
FRAME_NUM2	[7:0]	R	W	Frame number higher byte value	00

INDEX REGISTER (INDEX_REG)

The INDEX register is used to indicate certain endpoint registers effectively. The MCU can access the endpoint registers (MAXP_REG, IN_CSR1_REG, IN_CSR2_REG, OUT_CSR1_REG, OUT_CSR2_REG, OUT_FIFO_CNT1_REG, and OUT_FIFO_CNT2_REG) for an endpoint inside the core using the INDEX register.

Register	Address	R/W	Description	Reset Value
INDEX_REG	0x52000178(L) 0x5200017B(B)	R/W (byte)	Register index register	0x00

INDEX_REG	Bit	MCU	USB	Description	Initial State
INDEX	[7:0]	R/W	R	Indicate a certain endpoint	00

END POINT0 CONTROL STATUS REGISTER (EP0_CSR)

This register has the control and status bits for Endpoint 0. Since a control transaction is involved with both IN and OUT tokens, there is only one CSR register, mapped to the IN CSR1 register. (share IN1_CSR and can access by writing index register "0" and read/write IN1_CSR)

Register	Address	R/W	Description	Reset Value
EP0_CSR	0x52000184(L) 0x52000187(B)	R/W (byte)	Endpoint 0 status register	0x00

EP0_CSR	Bit	MCU	USB	Description	Initial State
SERVICED_ SETUP_END	[7]	W	CLEAR	The MCU should write a "1" to this bit to clear SETUP_END.	0
SERVICED_OUT_ PKT_RDY	[6]	W	CLEAR	The MCU should write a "1" to this bit to clear OUT_PKT_RDY.	0
SEND_STALL	[5]	R/W	CLEAR	MCU should write a "1" to this bit at the same time it clears OUT_PKT_RDY, if it decodes an invalid token. 0 = Finish the STALL condition 1 = The USB issues a STALL and shake to the current control transfer.	0
SETUP_END	[4]	R	SET	Set by the USB when a control transfer ends before DATA_END is set. When the USB sets this bit, an interrupt is generated to the MCU. When such a condition occurs, the USB flushes the FIFO and invalidates MCU access to the FIFO.	0
DATA_END	[3]	SET	CLEAR	Set by the MCU on the conditions below: 1. After loading the last packet of data into the FIFO, at the same time IN_PKT_RDY is set. 2. While it clears OUT_PKT_RDY after unloading the last packet of data. 3. For a zero length data phase.	0
SENT_STALL	[2]	CLEAR	SET	Set by the USB if a control transaction is stopped due to a protocol violation. An interrupt is generated when this bit is set. The MCU should write "0" to clear this bit.	0

END POINT0 CONTROL STATUS REGISTER (EP0_CSR) (Continued)

EP0_CSR	Bit	MCU	USB	Description	Initial State

IN_PKT_RDY	[1]	SET	CLEAR	Set by the MCU after writing a packet of data into EP0 FIFO. The USB clears this bit once the packet has been successfully sent to the host. An interrupt is generated when the USB clears this bit, so as the MCU to load the next packet. For a zero length data phase, the MCU sets DATA_END at the same time.	0
OUT_PKT_RDY	[0]	R	SET	Set by the USB once a valid token is written to the FIFO. An interrupt is generated when the USB sets this bit. The MCU clears this bit by writing a "1" to the SERVICED_OUT_PKT_RDY bit.	0

END POINT IN CONTROL STATUS REGISTER (IN_CSR1_REG/IN_CSR2_REG)

Register	Address	R/W	Description	Reset Value
IN_CSR1_REG	0x52000184(L) 0x52000187(B)	R/W (byte)	IN END POINT control status register1	0x00

IN_CSR1_REG	Bit	MCU	USB	Description	Initial State
Reserved	[7]	–	–	–	0
CLR_DATA_ TOGGLE	[6]	R/W	R/ CLEAR	Used in Set-up procedure. 0: There are alternation of DATA0 and DATA1 1: The data toggle bit is cleared and PID in packet will maintain DATA0	0
SENT_STALL	[5]	R/ CLEAR	SET	Set by the USB when an IN token issues a STALL handshake, after the MCU sets SEND_STALL bit to start STALL handshaking. When the USB issues a STALL handshake, IN_PKT_RDY is cleared	0
SEND_STALL	[4]	W/R	R	0: The MCU clears this bit to finish the STALL condition. 1: The MCU issues a STALL handshake to the USB.	0
FIFO_FLUSH	[3]	R/W	CLEAR	Set by the MCU if it intends to flush the packet in Input-related FIFO. This bit is cleared by the USB when the FIFO is flushed. The MCU is interrupted when this happens. If a token is in process, the USB waits until the transmission is complete before FIFO flushing. If two packets are loaded into the FIFO, only first packet (The packet is intended to be sent to the host) is flushed, and the corresponding IN_PKT_RDY bit is cleared	0
Reserved	[2:1]	–	–	–	0

END POINT IN CONTROL STATUS REGISTER (IN_CSR1_REG/IN_CSR2_REG) (CONTINUED)

IN_CSR1_REG	Bit	MCU	USB	Description	Initial State
IN_PKT_RDY	[0]	R/SET	CLEAR	Set by the MCU after writing a packet of data into the FIFO. The USB clears this bit once the packet has been successfully sent to the host. An interrupt is generated when the USB clears this bit, so the MCU can load the next packet. While this bit is set, the MCU will not be able to write to the FIFO. If the MCU sets SEND STALL bit, this bit cannot be set.	0

Register	Address	R/W	Description	Reset Value
IN_CSR2_REG	0x52000188(L) 0x5200018B(B)	R/W (byte)	IN END POINT control status register2	0x20

IN_CSR2_REG	Bit	MCU	USB	Description	Initial State
AUTO_SET	[7]	R/W	R	If set, whenever the MCU writes MAXP data, IN_PKT_RDY will automatically be set by the core without any intervention from MCU. If the MCU writes less than MAXP data, IN_PKT_RDY bit has to be set by the MCU.	0
ISO	[6]	R/W	R	*Used only for endpoints whose transfer type is programmable.* 1: Reserved 0: Configures endpoint to Bulk mode	0
MODE_IN	[5]	R/W	R	*Used only for endpoints whose direction is programmable.* 1: Configures Endpoint Direction as IN 0: Configures Endpoint Direction as OUT	1
IN_DMA_INT_EN	[4]	R/W	R	Determine whether the interrupt should be issued or not, when the IN_PKT_RDY condition happens. This is only useful for DMA mode. 0 = Interrupt enable, 1 = Interrupt Disable	0
Reserved	[3:0]	–	–	–	–

END POINT OUT CONTROL STATUS REGISTER (OUT_CSR1_REG/OUT_CSR2_REG)

Register	Address	R/W	Description	Reset Value
OUT_CSR1_REG	0x52000190(L) 0x52000193(B)	R/W (byte)	End Point out control status register1	0x00

OUT_CSR1_REG	Bit	MCU	USB	Description	Initial State
CLR_DATA_ TOGGLE	[7]	R/W	CLEAR	When the MCU writes a 1 to this bit, the data toggle sequence bit is reset to DATA0.	0
SENT_STALL	[6]	R/ CLEAR	SET	Set by the USB when an OUT token is ended with a STALL handshake. The USB issues a stall handshake to the host if it sends more than MAXP data for the OUT TOKEN.	0
SEND_STALL	[5]	R/W	R	0: The MCU clears this bit to end the STALL condition handshake, IN PKT RDY is cleared. 1: The MCU issues a STALL handshake to the USB. The MCU clears this bit to end the STALL condition handshake, IN PKT RDY is cleared.	0
FIFO_FLUSH	[4]	R/W	CLEAR	The MCU writes a 1 to flush the FIFO. This bit can be set only when OUT_PKT_RDY (D0) is set. The packet due to be unloaded by the MCU will be flushed.	0
Reserved	[3:1]	–	–	–	0
OUT_PKT_RDY	[0]	R/ CLEAR	SET	Set by the USB after it has loaded a packet of data into the FIFO. Once the MCU reads the packet from FIFO, this bit should be cleared by MCU (write a "0").	0

END POINT OUT CONTROL STATUS REGISTER (OUT_CSR1_REG/OUT_CSR2_REG) (Continued)

Register	Address	R/W	Description	Reset Value
OUT_CSR2_REG	0x52000194(L) 0x52000197(B)	R/W (byte)	End Point out control status register2	0x00

OUT_CSR2_REG	Bit	MCU	USB	Description	Initial State
AUTO_CLR	[7]	R/W	R	If the MCU is set, whenever the MCU reads data from the OUT FIFO, OUT_PKT_RDY will automatically be cleared by the logic without any intervention from the MCU.	0
ISO	[6]	R/W	R	Determine endpoint transfer type. 0: Configures endpoint to Bulk mode. 1: Reserved	0
OUT_DMA_INT_ MASK	[5]	R/W	R	Determine whether the interrupt should be issued or not. OUT_PKT_RDY condition happens. This is only useful for DMA mode 0 = Interrupt Enable 1 = Interrupt Disable	0

END POINT FIFO REGISTER (EPN_FIFO_REG)

The EPn_FIFO_REG enables the MCU to access to the EPn FIFO.

Register	Address	R/W	Description	Reset Value
EP0_FIFO	0x520001C0(L) 0x520001C3 (B)	R/W (byte)	End Point0 FIFO register	0xXX
EP1_FIFO	0x520001C4(L) 0x520001C7(B)	R/W (byte)	End Point1 FIFO register	0xXX
EP2_FIFO	0x520001C8(L) 0x520001CB(B)	R/W (byte)	End Point2 FIFO register	0xXX
EP3_FIFO	0x520001CC(L) 0x520001CF(B)	R/W (byte)	End Point3 FIFO register	0xXX
EP4_FIFO	0x520001D0(L) 0x520001D3(B)	R/W (byte)	End Point4 FIFO register	0xXX

EPn_FIFO	Bit	MCU	USB	Description	Initial State
FIFO_DATA	[7:0]	R/W	R/W	FIFO data value	0xXX

MAX PACKET REGISTER (MAXP_REG)

Register	Address	R/W	Description	Reset Value
MAXP_REG	0x52000180(L) 0x52000183(B)	R/W (byte)	End Point MAX packet register	0x01

MAXP_REG	Bit	MCU	USB	Description	Initial State
MAXP	[3:0]	R/W	R	0000: Reserved 0001: MAXP = 8 Byte0010: MAXP = 16 Byte 0100: MAXP = 32 Byte1000: MAXP = 64 Byte For EP0, MAXP=8 is recommended. For EP1~4, MAXP=32 or MAXP=64 is recommended. And, if MAXP=32, the dual packet mode will be enabled automatically.	0001

END POINT OUT WRITE COUNT REGISTER (OUT_FIFO_CNT1_REG/OUT_FIFO_CNT2_REG)

These registers maintain the number of bytes in the packet as the number is unloaded by the MCU.

Register	Address	R/W	Description	Reset Value
OUT_FIFO_CNT1_REG	0x52000198(L) 0x5200019B(B)	R (byte)	End Point out write count register1	0x00

OUT_FIFO_CNT1_REG	Bit	MCU	USB	Description	Initial State
OUT_CNT_LOW	[7:0]	R	W	Lower byte of write count	0x00

Register	Address	R/W	Description	Reset Value
OUT_FIFO_CNT2_REG	0x5200019C(L) 0x5200019F(B)	R (byte)	End Point out write count register2	0x00

OUT_FIFO_CNT2_REG	Bit	MCU	USB	Description	Initial State
OUT_CNT_HIGH	[7:0]	R	W	Higher byte of write count. The OUT_CNT_HIGH may be always 0 normally.	0x00

DMA INTERFACE CONTROL REGISTER (EPN_DMA_CON)

Register	Address	R/W	Description	Reset Value
EP1_DMA_CON	0x52000200(L) 0x52000203(B)	R/W (byte)	EP1 DMA interface control register	0x00
EP2_DMA_CON	0x52000218(L) 0x5200021B(B)	R/W (byte)	EP2 DMA interface control register	0x00
EP3_DMA_CON	0x52000240(L) 0x52000243(B)	R/W (byte)	EP3 DMA interface control register	0x00
EP4_DMA_CON	0x52000258(L) 0x5200025B(B)	R/W (byte)	EP4 DMA interface control register	0x00

EPn_DMA_CON	Bit	MCU	USB	Description	Initial State
IN_RUN_OB	[7]	R/W	W	Read) IN_DMA_Run Observation 0: DMA is stopped 1:DMA is running Write) Ignore EPn_DMA_TTC_n register 0: DMA requests will be stopped if EPn_DMA_TTC_n reaches 0. 1: DMA requests will be continued although EPn_DMA_TTC_n reaches 0.	0

STATE	[6:4]	R	W	DMA State Monitoring	0
DEMAND_MODE	[3]	R/W	R	DMA Demand mode enable bit 0: Demand mode disable 1: Demand mode enable	0
OUT_RUN_OB/ OUT_DMA_RUN	[2]	R/W	R/W	Functionally separated into write and read operation. Write operation: "0" = Stop "1" = Run Read operation: OUT DMA Run Observation	0
IN_DMA_RUN	[1]	R/W	R	Start DMA operation. 0 = Stop 1 = Run	0
DMA_MODE_EN	[0]	R/W	R/ CLEAR	Set DMA mode.If the IN_RUN_OB has been wrtten as 0 and EPn_DMA_TTC_n reaches 0, DMA_MODE_EN bit will be cleared by USB. 0 = Interrupt mode 1 = DMA mode	0

DMA UNIT COUNTER REGISTER (EPN_DMA_UNIT)

This register is valid in Demand mode. In other modes, this register value must be set to "0x01"

Register	Address	R/W	Description	Reset Value
EP1_DMA_UNIT	0x52000204(L) 0x52000207(B)	R/W (byte)	EP1 DMA transfer unit counter base register	0x00
EP2_DMA_UNIT	0x5200021C(L) 0x5200021F(B)	R/W (byte)	EP2 DMA transfer unit counter base register	0x00
EP3_DMA_UNIT	0x52000244(L) 0x52000247(B)	R/W (byte)	EP3 DMA transfer unit counter base register	0x00
EP4_DMA_UNIT	0x5200025C(L) 0x5200025F(B)	R/W (byte)	EP4 DMA transfer unit counter base register	0x00

DMA_UNIT	Bit	MCU	USB	Description	Initial State
EPn_UNIT_CNT	[7:0]	R/W	R	EP DMA transfer unit counter value	0x00

DMA FIFO COUNTER REGISTER (EPN_DMA_FIFO)

This register has values in byte size in FIFO to be transferred by DMA. In case of OUT_DMA_RUN enabled, the value in OUT FIFO Write Count Register1 will be loaded in this register automatically. In case of IN DMA mode, the MCU should set proper value by software.

Register	Address	R/W	Description	Reset Value
EP1_DMA_FIFO	0x52000208(L) 0x5200020B(B)	R/W (byte)	EP1 DMA transfer FIFO counter base register	0x00
EP2_DMA_FIFO	0x52000220(L) 0x52000223(B)	R/W (byte)	EP2 DMA transfer FIFO counter base register	0x00
EP3_DMA_FIFO	0x52000248(L) 0x5200024B(B)	R/W (byte)	EP3 DMA transfer FIFO counter base register	0x00
EP4_DMA_FIFO	0x52000260(L) 0x52000263(B)	R/W (byte)	EP4 DMA transfer FIFO counter base register	0x00

DMA_FIFO	Bit	MCU	USB	Description	Initial State
EPn_FIFO_CNT	[7:0]	R/W	R	EP DMA transfer FIFO counter value	0x00

DMA TOTAL TRANSFER COUNTER REGISTER (EPN_DMA_TTC_L, M, H)

This register should have total number of bytes to be transferred using DMA (total 20-bit counter).

Register	Address	R/W	Description	Reset Value
EP1_DMA_TTC_L	0x5200020C(L) 0x5200020F(B)	R/W (byte)	EP1 DMA total transfer counter(lower byte)	0x00
EP1_DMA_TTC_M	0x52000210(L) 0x52000213(B)	R/W (byte)	EP1 DMA total transfer counter(middle byte)	0x00
EP1_DMA_TTC_H	0x52000214(L) 0x52000217(B)	R/W (byte)	EP1 DMA total transfer counter(higher byte)	0x00
EP2_DMA_TTC_L	0x52000224(L) 0x52000227(B)	R/W (byte)	EP2 DMA total transfer counter(lower byte)	0x00
EP2_DMA_TTC_M	0x52000228(L) 0x5200022B(B)	R/W (byte)	EP2 DMA total transfer counter(middle byte)	0x00
EP2_DMA_TTC_H	0x5200022C(L) 0x5200022F(B)	R/W (byte)	EP2 DMA total transfer counter(higher byte)	0x00
EP3_DMA_TTC_L	0x5200024C(L) 0x5200024F(B)	R/W (byte)	EP3 DMA total transfer counter(lower byte)	0x00
EP3_DMA_TTC_M	0x52000250(L) 0x52000253(B)	R/W (byte)	EP3 DMA total transfer counter(middle byte)	0x00
EP3_DMA_TTC_H	0x52000254(L) 0x52000257(B)	R/W (byte)	EP3 DMA total transfer counter(higher byte)	0x00
EP4_DMA_TTC_L	0x52000264(L) 0x52000267(B)	R/W (byte)	EP4 DMA total transfer counter(lower byte)	0x00
EP4_DMA_TTC_M	0x52000268(L) 0x5200026B(B)	R/W (byte)	EP4 DMA total transfer counter(middle byte)	0x00
EP4_DMA_TTC_H	0x5200026C(L) 0x5200026F(B)	R/W (byte)	EP4 DMA total transfer counter(higher byte)	0x00

DMA_TX	Bit	MCU	USB	Description	Initial State
EPn_TTC_L	[7:0]	R/W	R	DMA total transfer count value (lower byte)	0x00
EPn_TTC_M	[7:0]	R/W	R	DMA total transfer count value (middle byte)	0x00
EPn_TTC_H	[3:0]	R/W	R	DMA total transfer count value (higher byte)	0x00

13 INTERRUPT CONTROLLER

OVERVIEW

The interrupt controller in the S3C2413X receives the request from 56 interrupt sources. These interrupt sources are provided by internal peripherals such as the DMA controller, the UART, IIC, and others. In these interrupt sources, the UARTn and EINTn interrupts are 'OR'ed to the interrupt controller.

When receiving multiple interrupt requests from internal peripherals and external interrupt request pins, the interrupt controller requests FIQ or IRQ interrupt of the ARM926EJ core after the arbitration procedure.

The arbitration procedure depends on the hardware priority logic and the result is written to the interrupt pending register, which helps users notify which interrupt is generated out of various interrupt sources.

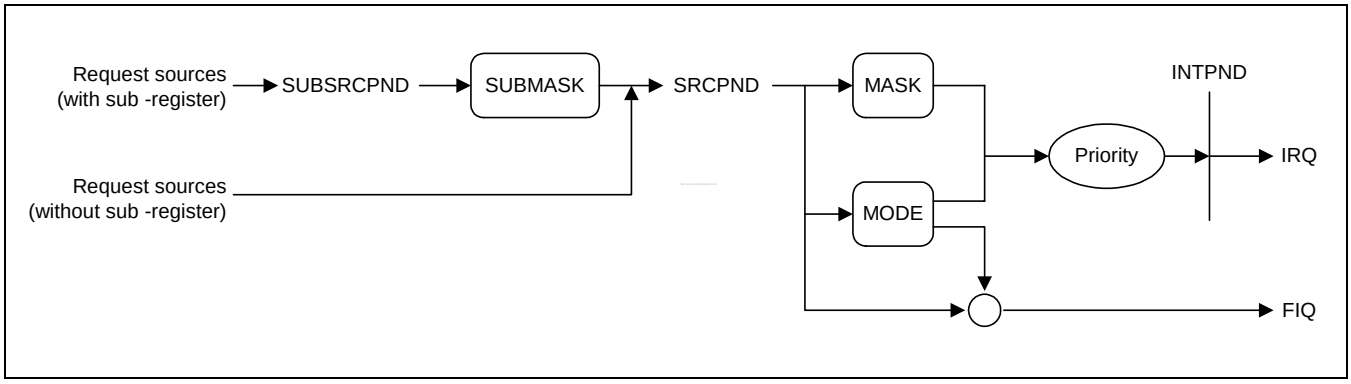


Figure 13-1. Interrupt Process Diagram

INTERRUPT CONTROLLER OPERATION

F-bit and I-bit of Program Status Register (PSR)

If the F-bit of PSR in ARM926EJ CPU is set to 1, the CPU does not accept the Fast Interrupt Request (FIQ) from the interrupt controller. Likewise, If I-bit of the PSR is set to 1, the CPU does not accept the Interrupt Request (IRQ) from the interrupt controller. So, the interrupt controller can receive interrupts by clearing F-bit or I-bit of the PSR to 0 and setting the corresponding bit of INTMSK to 0.

Interrupt Mode

The ARM926EJ has two types of Interrupt mode: FIQ or IRQ. All the interrupt sources determine which mode is used at interrupt request.

Interrupt Pending Register

The S3C2413X has two interrupt pending resisters: source pending register (SRCPND) and interrupt pending register (INTPND). These pending registers indicate whether or not an interrupt request is pending. When the interrupt sources request interrupt service, the corresponding bits of SRCPND register are set to 1, and at the same time, only one bit of the INTPND register is set to 1 automatically after arbitration procedure. If interrupts are masked, the corresponding bits of the SRCPND register are set to 1. This does not cause the bit of INTPND register changed. When a pending bit of the INTPND register is set, the interrupt service routine starts whenever the I-flag or F-flag is cleared to 0. The SRCPND and INTPND registers can be read and written, so the service routine must clear the pending condition by writing a 1 to the corresponding bit in the SRCPND register first and then clear the pending condition in the INTPND registers by using the same method.

Interrupt Mask Register

This register indicates that an interrupt has been disabled if the corresponding mask bit is set to 1. If an interrupt mask bit of INTMSK is 0, the interrupt will be serviced normally. If the corresponding mask bit is 1 and the interrupt is generated, the source pending bit will be set.

INTERRUPT SOURCES

The interrupt controller supports 56 interrupt sources as shown in the table below.

Sources	Descriptions	Arbiter Group
INT_ADC	ADC EOC and Touch interrupt (INT_ADC/INT_TC)	ARB5
INT_RTC	RTC alarm interrupt	ARB5
INT_SPI1_SPITO	SPI1 interrupt and SPI 0, 1 Timeout interrupt	ARB5
INT_UART0	UART0 Interrupt (ERR, RXD, and TXD)	ARB5
INT_IIC	IIC interrupt	ARB4
INT_USBH	USB Host interrupt	ARB4
INT_USBD	USB Device interrupt	ARB4
INT_NAND	NAND Flash Controller interrupt	ARB4
INT_UART1	UART1 Interrupt (ERR, RXD, and TXD)	ARB4
INT_SPI0	SPI0 interrupt	ARB4
INT_SDI_CF	SDI and CF interrupts	ARB 3
INT_DMA3	DMA channel 3 interrupt	ARB3
INT_DMA2	DMA channel 2 interrupt	ARB3
INT_DMA1	DMA channel 1 interrupt	ARB3
INT_DMA0	DMA channel 0 interrupt	ARB3
INT_LCD	LCD interrupt (INT_FrSyn and INT_FiCnt)	ARB3
INT_UART2	UART2 Interrupt (ERR, RXD, and TXD)	ARB2
INT_TIMER4	Timer4 interrupt	ARB2
INT_TIMER3	Timer3 interrupt	ARB2
INT_TIMER2	Timer2 interrupt	ARB2
INT_TIMER1	Timer1 interrupt	ARB 2
INT_TIMER0	Timer0 interrupt	ARB2
INT_WDT	Watch-Dog timer interrupt	ARB1
INT_TICK	RTC Time tick interrupt	ARB1
nBATT_FLT	Battery Fault interrupt	ARB1
INT_CAMIF	Camera Interface	ARB1
EINT8_23	External interrupt 8 – 23	ARB1
EINT4_7	External interrupt 4 – 7	ARB1
EINT3	External interrupt 3	ARB0
EINT2	External interrupt 2	ARB0
EINT1	External interrupt 1	ARB0
EINT0	External interrupt 0	ARB0

INTERRUPT PRIORITY GENERATING BLOCK

The priority logic for 32 interrupt requests is composed of seven rotation based arbiters: six first-level arbiters and one second-level arbiter as shown in Figure 13-2 below.

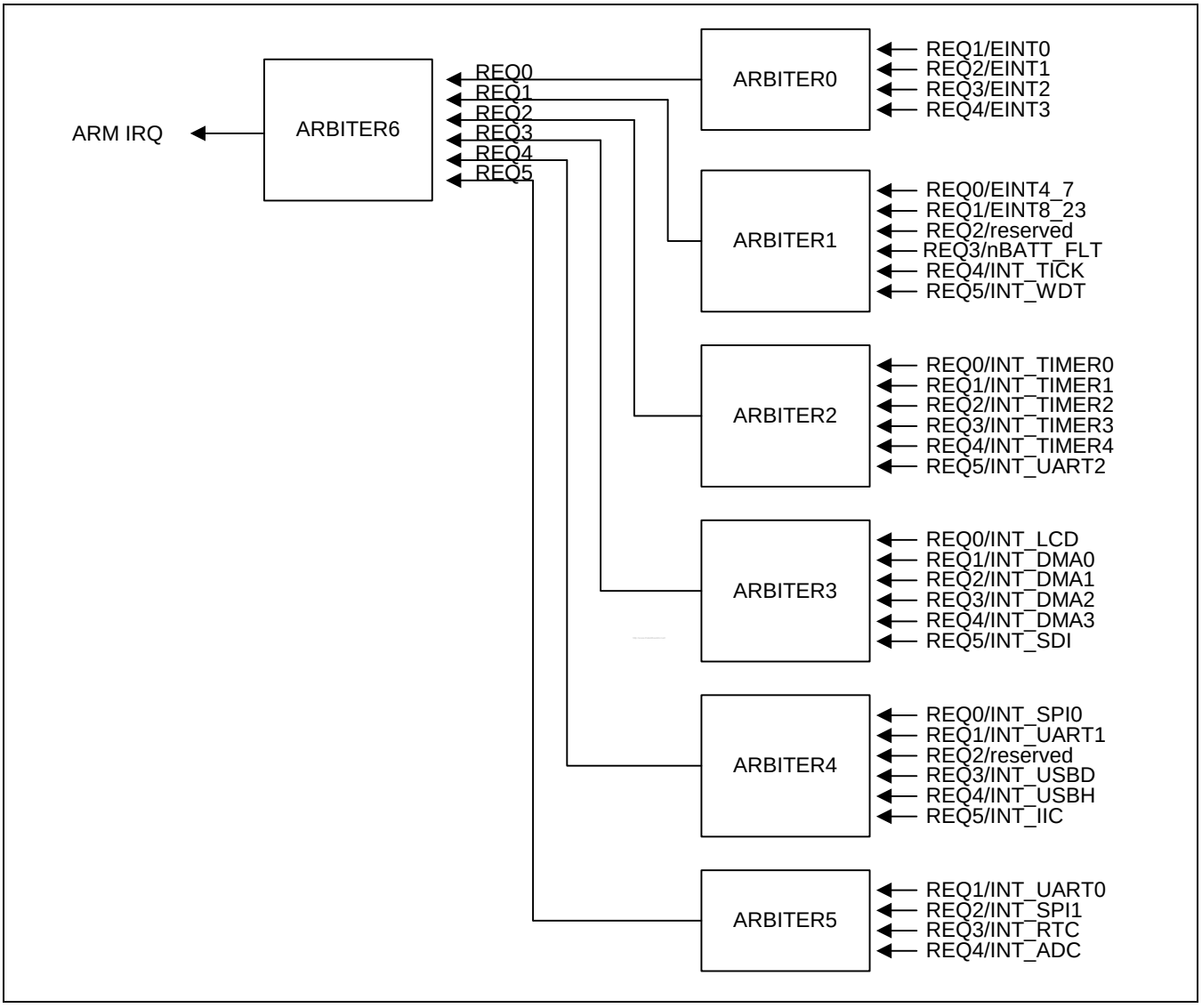


Figure 13-2. Priority Generating Block

INTERRUPT PRIORITY

Each arbiter can handle six interrupt requests based on the one bit arbiter mode control (ARB_MODE) and two bits of selection control signals (ARB_SEL) as follows:

- If ARB_SEL bits are 00b, the priority order is REQ0, REQ1, REQ2, REQ3, REQ4, and REQ5.
- If ARB_SEL bits are 01b, the priority order is REQ0, REQ2, REQ3, REQ4, REQ1, and REQ5.
- If ARB_SEL bits are 10b, the priority order is REQ0, REQ3, REQ4, REQ1, REQ2, and REQ5.
- If ARB_SEL bits are 11b, the priority order is REQ0, REQ4, REQ1, REQ2, REQ3, and REQ5.

Note that REQ0 of an arbiter always has the highest priority, and REQ5 has the lowest one. In addition, by changing the ARB_SEL bits, we can rotate the priority of REQ1 to REQ4.

Here, if ARB_MODE bit is set to 0, ARB_SEL bits are not automatically changed, making the arbiter to operate in the fixed priority mode (note that even in this mode, we can reconfigure the priority by manually changing the ARB_SEL bits). On the other hand, if ARB_MODE bit is 1, ARB_SEL bits are changed in rotation fashion, e.g., if REQ1 is serviced, ARB_SEL bits are changed to 01b automatically so as to put REQ1 into the lowest priority. The detailed rules of ARB_SEL change are as follows:

- If REQ0 or REQ5 is serviced, ARB_SEL bits are not changed at all.
- If REQ1 is serviced, ARB_SEL bits are changed to 01b.
- If REQ2 is serviced, ARB_SEL bits are changed to 10b.
- If REQ3 is serviced, ARB_SEL bits are changed to 11b.
- If REQ4 is serviced, ARB_SEL bits are changed to 00b.

INTERRUPT CONTROLLER SPECIAL REGISTERS

There are five control registers in the interrupt controller: source pending register, interrupt mode register, mask register, priority register, and interrupt pending register.

All the interrupt requests from the interrupt sources are first registered in the source pending register. They are divided into two groups including Fast Interrupt Request (FIQ) and Interrupt Request (IRQ), based on the interrupt mode register. The arbitration procedure for multiple IRQs is based on the priority register.

SOURCE PENDING (SRCPND) REGISTER

The SRCPND register is composed of 32 bits each of which is related to an interrupt source. Each bit is set to 1 if the corresponding interrupt source generates the interrupt request and waits for the interrupt to be serviced. Accordingly, this register indicates which interrupt source is waiting for the request to be serviced. Note that each bit of the SRCPND register is automatically set by the interrupt sources regardless of the masking bits in the INTMASK register. In addition, the SRCPND register is not affected by the priority logic of interrupt controller.

In the interrupt service routine for a specific interrupt source, the corresponding bit of the SRCPND register has to be cleared to get the interrupt request from the same source correctly. If you return from the ISR without clearing the bit, the interrupt controller operates as if another interrupt request came in from the same source. In other words, if a specific bit of the SRCPND register is set to 1, it is always considered as a valid interrupt request waiting to be serviced.

The time to clear the corresponding bit depends on the user's requirement. If you want to receive another valid request from the same source, you should clear the corresponding bit first, and then enable the interrupt.

You can clear a specific bit of the SRCPND register by writing a data to this register. It clears only the bit positions of the SRCPND corresponding to those set to one in the data. The bit positions corresponding to those that are set to 0 in the data remains as they are.

Register	Address	R/W	Description	Reset Value
SRCPND	0X4A000000	R/W	Indicate the interrupt request status. 0 = The interrupt has not been requested. 1 = The interrupt source has asserted the interrupt request.	0x00000000

SOURCE PENDING (SRCPND) REGISTER (Continued)

SRCPND	Bit	Description	Initial State
INT_ADC	[31]	0 = Not requested, 1 = Requested	0
INT_RTC	[30]	0 = Not requested, 1 = Requested	0
INT_SPI1_SPITO	[29]	0 = Not requested, 1 = Requested	0
INT_UART0	[28]	0 = Not requested, 1 = Requested	0
INT_IIC	[27]	0 = Not requested, 1 = Requested	0
INT_USBH	[26]	0 = Not requested, 1 = Requested	0
INT_USBD	[25]	0 = Not requested, 1 = Requested	0
INT_NAND	[24]	0 = Not requested, 1 = Requested	0
INT_UART1	[23]	0 = Not requested, 1 = Requested	0
INT_SPI0	[22]	0 = Not requested, 1 = Requested	0
INT_SDI_CF	[21]	0 = Not requested, 1 = Requested	0
INT_DMA3	[20]	0 = Not requested, 1 = Requested	0
INT_DMA2	[19]	0 = Not requested, 1 = Requested	0
INT_DMA1	[18]	0 = Not requested, 1 = Requested	0
INT_DMA0	[17]	0 = Not requested, 1 = Requested	0
INT_LCD	[16]	0 = Not requested, 1 = Requested	0
INT_UART2	[15]	0 = Not requested, 1 = Requested	0
INT_TIMER4	[14]	0 = Not requested, 1 = Requested	0
INT_TIMER3	[13]	0 = Not requested, 1 = Requested	0
INT_TIMER2	[12]	0 = Not requested, 1 = Requested	0
INT_TIMER1	[11]	0 = Not requested, 1 = Requested	0
INT_TIMER0	[10]	0 = Not requested, 1 = Requested	0
INT_WDT	[9]	0 = Not requested, 1 = Requested	0
INT_TICK	[8]	0 = Not requested, 1 = Requested	0
nBATT_FLT	[7]	0 = Not requested, 1 = Requested	0
INT_CAMIF	[6]	0 = Not requested, 1 = Requested	0
EINT8_23	[5]	0 = Not requested, 1 = Requested	0
EINT4_7	[4]	0 = Not requested, 1 = Requested	0
EINT3	[3]	0 = Not requested, 1 = Requested	0
EINT2	[2]	0 = Not requested, 1 = Requested	0
EINT1	[1]	0 = Not requested, 1 = Requested	0
EINT0	[0]	0 = Not requested, 1 = Requested	0

INTERRUPT MODE (INTMOD) REGISTER

This register is composed of 32 bits each of which is related to an interrupt source. If a specific bit is set to 1, the corresponding interrupt is processed in the FIQ (fast interrupt) mode. Otherwise, it is processed in the IRQ mode (normal interrupt).

Note that only one interrupt source can be serviced in the FIQ mode in the interrupt controller (you should use the FIQ mode only for the urgent interrupt). Thus, only one bit of INTMOD can be set to 1.

Register	Address	R/W	Description	Reset Value
INTMOD	0X4A000004	R/W	Interrupt mode regiseter. 0 = IRQ mode 1 = FIQ mode	0x00000000

NOTE: If an interrupt mode is set to FIQ mode in the INTMOD register, FIQ interrupt will not affect both INTPND and INTOFFSET registers. In this case, the two registers are valid only for IRQ mode interrupt source.

INTMOD	Bit	Description	Initial State
INT_ADC	[31]	0 = IRQ, 1 = FIQ	0
INT_RTC	[30]	0 = IRQ, 1 = FIQ	0
INT_SPI1_SPITO	[29]	0 = IRQ, 1 = FIQ	0
INT_UART0	[28]	0 = IRQ, 1 = FIQ	0
INT_IIC	[27]	0 = IRQ, 1 = FIQ	0
INT_USBH	[26]	0 = IRQ, 1 = FIQ	0
INT_USBD	[25]	0 = IRQ, 1 = FIQ	0
INT_NAND	[24]	0 = IRQ, 1 = FIQ	0
INT_UART1	[23]	0 = IRQ, 1 = FIQ	0
INT_SPI0	[22]	0 = IRQ, 1 = FIQ	0
INT_SDI_CF	[21]	0 = IRQ, 1 = FIQ	0
INT_DMA3	[20]	0 = IRQ, 1 = FIQ	0
INT_DMA2	[19]	0 = IRQ, 1 = FIQ	0
INT_DMA1	[18]	0 = IRQ, 1 = FIQ	0
INT_DMA0	[17]	0 = IRQ, 1 = FIQ	0
INT_LCD	[16]	0 = IRQ, 1 = FIQ	0
INT_UART2	[15]	0 = IRQ, 1 = FIQ	0
INT_TIMER4	[14]	0 = IRQ, 1 = FIQ	0
INT_TIMER3	[13]	0 = IRQ, 1 = FIQ	0
INT_TIMER2	[12]	0 = IRQ, 1 = FIQ	0
INT_TIMER1	[11]	0 = IRQ, 1 = FIQ	0
INT_TIMER0	[10]	0 = IRQ, 1 = FIQ	0
INT_WDT	[9]	0 = IRQ, 1 = FIQ	0
INT_TICK	[8]	0 = IRQ, 1 = FIQ	0
nBATT_FLT	[7]	0 = IRQ, 1 = FIQ	0
INT_CAMIF	[6]	0 = IRQ, 1 = FIQ	0
EINT8_23	[5]	0 = IRQ, 1 = FIQ	0
EINT4_7	[4]	0 = IRQ, 1 = FIQ	0
EINT3	[3]	0 = IRQ, 1 = FIQ	0
EINT2	[2]	0 = IRQ, 1 = FIQ	0
EINT1	[1]	0 = IRQ, 1 = FIQ	0
EINT0	[0]	0 = IRQ, 1 = FIQ	0

INTERRUPT MASK (INTMSK) REGISTER

This register also has 32 bits each of which is related to an interrupt source. If a specific bit is set to 1, the CPU does not service the interrupt request from the corresponding interrupt source (note that even in such a case, the corresponding bit of SRCPND register is set to 1). If the mask bit is 0, the interrupt request can be serviced.

Register	Address	R/W	Description	Reset Value
INTMSK	0X4A000008	R/W	Determine which interrupt source is masked. The masked interrupt source will not be serviced. 0 = Interrupt service is available. 1 = Interrupt service is masked.	0xFFFFFFFF

INTMSK	Bit	Description	Initial State
INT_ADC	[31]	0 = Service available, 1 = Masked	1
INT_RTC	[30]	0 = Service available, 1 = Masked	1
INT_SPI1_SPITO	[29]	0 = Service available, 1 = Masked	1
INT_UART0	[28]	0 = Service available, 1 = Masked	1
INT_IIC	[27]	0 = Service available, 1 = Masked	1
INT_USBH	[26]	0 = Service available, 1 = Masked	1
INT_USBD	[25]	0 = Service available, 1 = Masked	1
INT_NAND	[24]	0 = Service available, 1 = Masked	1
INT_UART1	[23]	0 = Service available, 1 = Masked	1
INT_SPI0	[22]	0 = Service available, 1 = Masked	1
INT_SDI_CF	[21]	0 = Service available, 1 = Masked	1
INT_DMA3	[20]	0 = Service available, 1 = Masked	1
INT_DMA2	[19]	0 = Service available, 1 = Masked	1
INT_DMA1	[18]	0 = Service available, 1 = Masked	1
INT_DMA0	[17]	0 = Service available, 1 = Masked	1
INT_LCD	[16]	0 = Service available, 1 = Masked	1
INT_UART2	[15]	0 = Service available, 1 = Masked	1
INT_TIMER4	[14]	0 = Service available, 1 = Masked	1
INT_TIMER3	[13]	0 = Service available, 1 = Masked	1
INT_TIMER2	[12]	0 = Service available, 1 = Masked	1
INT_TIMER1	[11]	0 = Service available, 1 = Masked	1
INT_TIMER0	[10]	0 = Service available, 1 = Masked	1
INT_WDT	[9]	0 = Service available, 1 = Masked	1
INT_TICK	[8]	0 = Service available, 1 = Masked	1
nBATT_FLT	[7]	0 = Service available, 1 = Masked	1
CAMIF	[6]	0 = Service available, 1 = Masked	1
EINT8_23	[5]	0 = Service available, 1 = Masked	1
EINT4_7	[4]	0 = Service available, 1 = Masked	1
EINT3	[3]	0 = Service available, 1 = Masked	1
EINT2	[2]	0 = Service available, 1 = Masked	1
EINT1	[1]	0 = Service available, 1 = Masked	1
EINT0	[0]	0 = Service available, 1 = Masked	1

PRIORITY REGISTER (PRIORITY)

Register	Address	R/W	Description	Reset Value
PRIORITY	0x4A00000C	R/W	IRQ priority control register	0x7F

PRIORITY	Bit	Description	Initial State
ARB_SEL6	[20:19]	Arbiter 6 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL5	[18:17]	Arbiter 5 group priority order set 00 = REQ 1-2-3-4 01 = REQ 2-3-4-1 10 = REQ 3-4-1-2 11 = REQ 4-1-2-3	0
ARB_SEL4	[16:15]	Arbiter 4 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL3	[14:13]	Arbiter 3 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL2	[12:11]	Arbiter 2 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL1	[10:9]	Arbiter 1 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL0	[8:7]	Arbiter 0 group priority order set 00 = REQ 1-2-3-4 01 = REQ 2-3-4-1 10 = REQ 3-4-1-2 11 = REQ 4-1-2-3	0
ARB_MODE6	[6]	Arbiter 6 group priority rotate enable 0 = Priority does not rotate 1 = Priority rotate enable	1
ARB_MODE5	[5]	Arbiter 5 group priority rotate enable 0 = Priority does not rotate 1 = Priority rotate enable	1
ARB_MODE4	[4]	Arbiter 4 group priority rotate enable 0 = Priority does not rotate 1 = Priority rotate enable	1
ARB_MODE3	[3]	Arbiter 3 group priority rotate enable 0 = Priority does not rotate 1 = Priority rotate enable	1
ARB_MODE2	[2]	Arbiter 2 group priority rotate enable 0 = Priority does not rotate 1 = Priority rotate enable	1

PRIORITY REGISTER (PRIORITY) (Continued)

PRIORITY	Bit	Description	Initial State
ARB_MODE1	[1]	Arbiter 1 group priority rotate enable 0 = Priority does not rotate 1 = Priority rotate enable	1
ARB_MODE0	[0]	Arbiter 0 group priority rotate enable 0 = Priority does not rotate 1 = Priority rotate enable	1

INTERRUPT PENDING (INTPND) REGISTER

Each of the 32 bits in the interrupt pending register shows whether the corresponding interrupt request, which is unmasked and waits for the interrupt to be serviced, has the highest priority . Since the INTPND register is located after the priority logic, only one bit can be set to 1, and that interrupt request generates IRQ to CPU. In interrupt service routine for IRQ, you can read this register to determine which interrupt source is serviced among the 32 sources.

Like the SRCPND register, this register has to be cleared in the interrupt service routine after clearing the SRCPND register. We can clear a specific bit of the INTPND register by writing a data to this register. It clears only the bit positions of the INTPND register corresponding to those set to one in the data. The bit positions corresponding to those that are set to 0 in the data remains as they are.

Register	Address	R/W	Description	Reset Value
INTPND	0X4A000010	R/W	Indicate the interrupt request status. 0 = The interrupt has not been requested. 1 = The interrupt source has asserted the interrupt request.	0x00000000

NOTES:

1. If the FIQ mode interrupt occurs, the corresponding bit of INTPND will not be turned on as the INTPND register is available only for IRQ mode interrupt.
2. Cautions in clearing the INTPND register.
   The INTPND register is cleared to "0" by writing "1". If the INTPND bit, which has "1", is cleared by "0", the INTPND register & INTOFFSET register may have unexpected value in some case.
   So, you never write "0" on the INTPND bit having "1". The convenient method to clear the INTPND register is writing the INTPND register value on the INTPND register. (In even our example code, this guide hasn't been applied yet.)

INTPND	Bit	Description	Initial State
INT_ADC	[31]	0 = Not requested, 1 = Requested	0
INT_RTC	[30]	0 = Not requested, 1 = Requested	0
INT_SPI1_SPITO	[29]	0 = Not requested, 1 = Requested	0
INT_UART0	[28]	0 = Not requested, 1 = Requested	0
INT_IIC	[27]	0 = Not requested, 1 = Requested	0
INT_USBH	[26]	0 = Not requested, 1 = Requested	0
INT_USBD	[25]	0 = Not requested, 1 = Requested	0
INT_NAND	[24]	0 = Not requested, 1 = Requested	0
INT_UART1	[23]	0 = Not requested, 1 = Requested	0
INT_SPI0	[22]	0 = Not requested, 1 = Requested	0
INT_SDI_CF	[21]	0 = Not requested, 1 = Requested	0
INT_DMA3	[20]	0 = Not requested, 1 = Requested	0
INT_DMA2	[19]	0 = Not requested, 1 = Requested	0
INT_DMA1	[18]	0 = Not requested, 1 = Requested	0
INT_DMA0	[17]	0 = Not requested, 1 = Requested	0
INT_LCD	[16]	0 = Not requested, 1 = Requested	0
INT_UART2	[15]	0 = Not requested, 1 = Requested	0
INT_TIMER4	[14]	0 = Not requested, 1 = Requested	0
INT_TIMER3	[13]	0 = Not requested, 1 = Requested	0
INT_TIMER2	[12]	0 = Not requested, 1 = Requested	0
INT_TIMER1	[11]	0 = Not requested, 1 = Requested	0
INT_TIMER0	[10]	0 = Not requested, 1 = Requested	0
INT_WDT	[9]	0 = Not requested, 1 = Requested	0
INT_TICK	[8]	0 = Not requested, 1 = Requested	0
nBATT_FLT	[7]	0 = Not requested, 1 = Requested	0
INT_CAMIF	[6]	0 = Not requested, 1 = Requested	0
EINT8_23	[5]	0 = Not requested, 1 = Requested	0
EINT4_7	[4]	0 = Not requested, 1 = Requested	0
EINT3	[3]	0 = Not requested, 1 = Requested	0
EINT2	[2]	0 = Not requested, 1 = Requested	0
EINT1	[1]	0 = Not requested, 1 = Requested	0
EINT0	[0]	0 = Not requested, 1 = Requested	0

INTERRUPT OFFSET (INTOFFSET) REGISTER

The value in the interrupt offset register shows which interrupt request of IRQ mode is in the INTPND register. This bit can be cleared automatically by clearing SRCPND and INTPND.

Register	Address	R/W	Description	Reset Value
INTOFFSET	0X4A000014	R	Indicate the IRQ interrupt request source	0x00000000

INT Source	The OFFSET Value	INT Source	The OFFSET Value
INT_ADC	31	INT_UART2	15
INT_RTC	30	INT_TIMER4	14
INT_SPI1_SPITO	29	INT_TIMER3	13
INT_UART0	28	INT_TIMER2	12
INT_IIC	27	INT_TIMER1	11
INT_USBH	26	INT_TIMER0	10
INT_USBD	25	INT_WDT	9
INT_NAND	24	INT_TICK	8
INT_UART1	23	nBATT_FLT	7
INT_SPI0	22	INT_CAMIF	6
INT_SDI_CF	21	EINT8_23	5
INT_DMA3	20	EINT4_7	4
INT_DMA2	19	EINT3	3
INT_DMA1	18	EINT2	2
INT_DMA0	17	EINT1	1
INT_LCD	16	EINT0	0

NOTE: FIQ mode interrupt does not affect the INTOFFSET register as the register is available only for IRQ mode interrupt.

SUB SOURCE PENDING (SUBSRCPND) REGISTER

You can clear a specific bit of the SUBSRCPND register by writing a data to this register. It clears only the bit positions of the SUBSRCPND register corresponding to those set to one in the data. The bit positions corresponding to those that are set to 0 in the data remains as they are.

Register	Address	R/W	Description	Reset Value
SUBSRCPND	0X4A000018	R/W	Indicate the interrupt request status. 0 = The interrupt has not been requested. 1 = The interrupt source has asserted the interrupt request.	0x00000000

SUBSRCPND	Bit	Description	Initial State
Reserved	[31:16]	Not used	0
INT_SPI1	[15]	0 = Not requested, 1 = Requested	0
INT_CF	[14]	0 = Not requested, 1 = Requested	0
INT_SDI	[13]	0 = Not requested, 1 = Requested	0
INT_SPI1_TO	[12]	0 = Not requested, 1 = Requested	0
INT_SPI0_TO	[11]	0 = Not requested, 1 = Requested	0
INT_ADC	[10]	0 = Not requested, 1 = Requested	0
INT_TC	[9]	0 = Not requested, 1 = Requested	0
INT_ERR2	[8]	0 = Not requested, 1 = Requested	0
INT_TXD2	[7]	0 = Not requested, 1 = Requested	0
INT_RXD2	[6]	0 = Not requested, 1 = Requested	0
INT_ERR1	[5]	0 = Not requested, 1 = Requested	0
INT_TXD1	[4]	0 = Not requested, 1 = Requested	0
INT_RXD1	[3]	0 = Not requested, 1 = Requested	0
INT_ERR0	[2]	0 = Not requested, 1 = Requested	0
INT_TXD0	[1]	0 = Not requested, 1 = Requested	0
INT_RXD0	[0]	0 = Not requested, 1 = Requested	0

INTERRUPT SUB MASK (INTSUBMSK) REGISTER

This register has 11 bits each of which is related to an interrupt source. If a specific bit is set to 1, the interrupt request from the corresponding interrupt source is not serviced by the CPU (note that even in such a case, the corresponding bit of the SUBSRCPND register is set to 1). If the mask bit is 0, the interrupt request can be serviced.

Register	Address	R/W	Description	Reset Value
INTSUBMSK	0X4A00001C	R/W	Determine which interrupt source is masked. The masked interrupt source will not be serviced. 0 = Interrupt service is available. 1 = Interrupt service is masked.	0x7FF

INTSUBMSK	Bit	Description	Initial State
Reserved	[31:16]	Not used	0x0000
INT_SPI1	[15]	0 = Service available, 1 = Masked	1
INT_CF	[14]	0 = Service available, 1 = Masked	1
INT_SDI	[13]	0 = Service available, 1 = Masked	1
INT_SPI1_TO	[12]	0 = Service available, 1 = Masked	1
INT_SPI0_TO	[11]	0 = Service available, 1 = Masked	1
INT_ADC	[10]	0 = Service available, 1 = Masked	1
INT_TC	[9]	0 = Service available, 1 = Masked	1
INT_ERR2	[8]	0 = Service available, 1 = Masked	1
INT_TXD2	[7]	0 = Service available, 1 = Masked	1
INT_RXD2	[6]	0 = Service available, 1 = Masked	1
INT_ERR1	[5]	0 = Service available, 1 = Masked	1
INT_TXD1	[4]	0 = Service available, 1 = Masked	1
INT_RXD1	[3]	0 = Service available, 1 = Masked	1
INT_ERR0	[2]	0 = Service available, 1 = Masked	1
INT_TXD0	[1]	0 = Service available, 1 = Masked	1
INT_RXD0	[0]	0 = Service available, 1 = Masked	1

14 LCD CONTROLLER

OVERVIEW

The LCD controller in the S3C2413X consists of the logic for transferring LCD image data from a video buffer located in system memory to an external LCD driver.

The LCD controller supports monochrome, 2-bit per pixel (4-level gray scale) or 4-bit per pixel (16-level gray scale) mode on a monochrome STN (Gray STN), using a time-based dithering algorithm and Frame Rate Control (FRC) method and it can support 1-bit per pixel, 2-bit per pixel, 4-bit per pixel, 8-bit per pixel with the palettized mode, and 8-bit per pixel, 12-bit per pixel, and 16-bit per pixel with the non-palettized mode. It can supports 4 bit single, 4 bit dual, and 8bit single interface STN LCD.

It can support 1-bit per pixel, 2-bit per pixel, 4-bit per pixel, and 8-bit per pixel for interfacing with the palettized TFT color LCD panel, and 16-bit per pixel and 24-bit per pixel for non-palettized true-color display.

The LCD controller can be programmed to support different requirements on the screen related to the number of horizontal and vertical pixels, data line width for the data interface, interface timing, and refresh rate.

FEATURES

STN LCD displays:

- Supports 3 types of LCD panels: 4-bit dual scan, 4-bit single scan, and 8-bit single scan display type
- Supports the monochrome, 4 gray levels, and 16 gray levels for monochrome STN panel
- Supports 1, 2, 4 or 8-bpp(bit per pixel) palettized color displays for CSTN (Color STN)
- Supports 8, 12 or 16-bpp(bit per pixel) non-palettized color displays for CSTN (Color STN)
- Supports multiple screen size
  Typical actual screen size: 240 x 320, 320 x 240, 160 x 160, and others
  Maximum virtual screen size is 4Mbytes.
  Maximum virtual screen size in 256 color mode: 4096 x 1024, 2048 x 2048, 1024 x 4096, and others

TFT LCD displays:

- Supports 1, 2, 4 or 8-bpp (bit per pixel) palettized color displays for TFT
- Supports 16-bpp non-palettized true-color displays for color TFT
- Supports 24-bpp non-palettized true-color displays for color TFT
- Supports maximum 16M color TFT at 24bit per pixel mode
- Supports multiple screen size
  Typical actual screen size: 640 x 480, 320 x 240, 160 x 160, and others
  Maximum virtual screen size is 4Mbytes.
  Maximum virtual screen size in 64K color mode: 2048 x 1024 and others

COMMON FEATURES

The LCD controller has a dedicated DMA that supports to fetch the image data from video buffer located in system memory. Its features also include:

- Dedicated interrupt functions (INT_FrSyn and INT_FiCnt)
- The system memory is used as the display memory.
- Supports Multiple Virtual Display Screen (Supports Hardware Horizontal/Vertical Scrolling)
- Programmable timing control for different display panels
- Supports little and big-endian byte ordering, as well as WinCE data formats
- Supports 2-type SEC TFT LCD panel

  (SAMSUNG 3.5" Portrait / 256K Color /Reflective and Transflective a-Si TFT LCD)
  LTS350Q1-PD1: TFT LCD panel with touch panel and front light unit (Reflective type)
  LTS350Q1-PD2: TFT LCD panel only
  LTS350Q1-PE1: TFT LCD panel with touch panel and front light unit (Transflective type)
  LTS350Q1-PE2: TFT LCD panel only

NOTE

WinCE doesn't support the 12-bit packed data format.
Please check if WinCE can support the 12-bit color-mode.

EXTERNAL INTERFACE SIGNAL

STN	TFT	SEC TFT (LTS350Q1-PD1/2)	SEC TFT (LTS350Q1-PE1/2)
VFRAME (Frame sync. Signal)	VSYNC (Vertical sync. Signal)	STV	STV
VLINE (Line sync pulse signal)	HSYNC (Horizontal sync. Signal)	CPV	CPV
VCLK (Pixel clock signal)	VCLK (Pixel clock signal)	LCD_HCLK	LCD_HCLK
VD[23:0] (LCD pixel data output ports)	VD[23:0] (LCD pixel data output ports)	VD[23:0]	VD[23:0]
VD[0]	VD[0]	STH	STH
VM (AC bias signal for LCD driver)	VDEN (Data enable signal)	TP	TP
-	-	LPC_OE	LCC_INV
-	-	LPC_REV	LCC_REV
-	-	LPC_REVB	LCC_REVB

BLOCK DIAGRAM

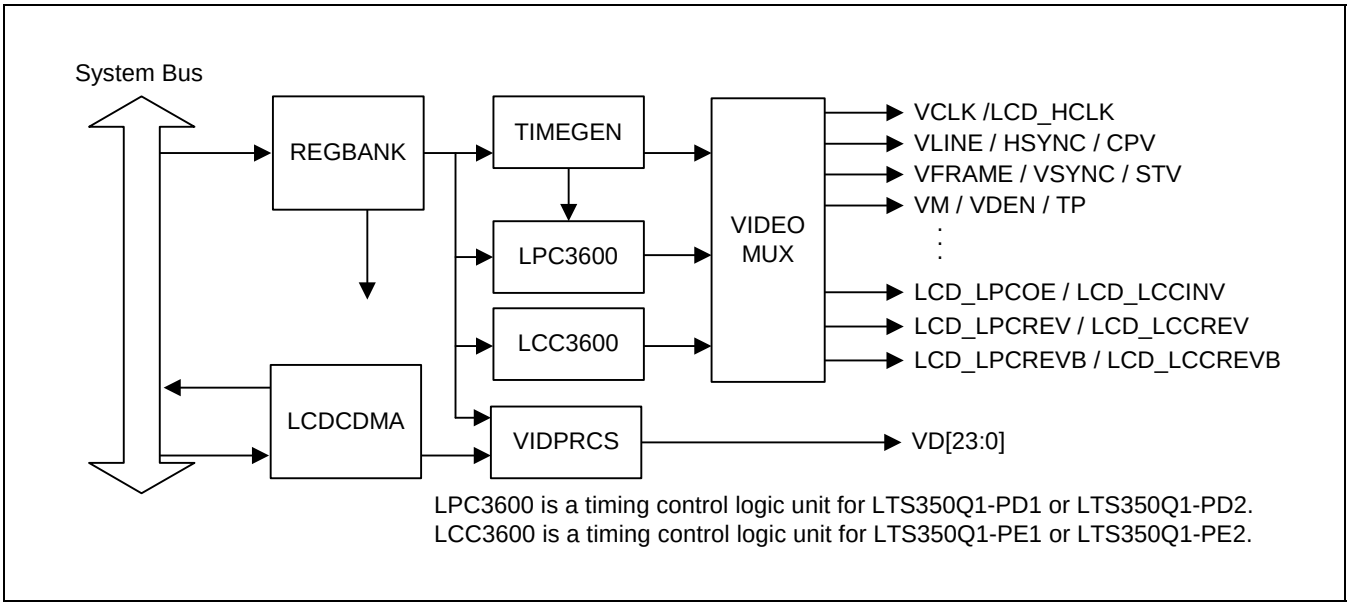


Figure 14-1. LCD Controller Block Diagram

The S3C2413X LCD controller is used to transfer the video data and to generate the necessary control signals, such as VFRAME, VLINE, VCLK, VM, and so on. In addition to the control signals, the S3C2413X has the data ports for video data, which are VD[23:0] as shown in Figure 14-1. The LCD controller consists of a REGBANK, LCDCDMA, VIDPRCS, TIMEGEN, and LPC3600 (See the Figure 14-1 LCD Controller Block Diagram). The REGBANK has 17 programmable register sets and 256x16 palette memory which are used to configure the LCD controller. The LCDCDMA is a dedicated DMA, which can transfer the video data in frame memory to LCD driver automatically. By using this special DMA, the video data can be displayed on the screen without CPU intervention. The VIDPRCS receives the video data from the LCDCDMA and sends the video data through the VD[23:0] data ports to the LCD driver after changing them into a suitable data format, for example 4/8-bit single scan or 4-bit dual scan display mode. The TIMEGEN consists of programmable logic to support the variable requirements of interface timing and rates commonly found in different LCD drivers. The TIMEGEN block generates VFRAME, VLINE, VCLK, VM, and so on.

The description of data flow is as follows:

FIFO memory is present in the LCDCDMA. When FIFO is empty or partially empty, the LCDCDMA requests data fetching from the frame memory based on the burst memory transfer mode (consecutive memory fetching of 4 words (16 bytes) per one burst request without allowing the bus mastership to another bus master during the bus transfer). When the transfer request is accepted by bus arbitrator in the memory controller, there will be four successive word data transfers from system memory to internal FIFO. The total size of FIFO is 28 words, which consists of 12 words FIFOL and 16 words FIFOH, respectively. The S3C2413X has two FIFOs to support the dual scan display mode. In case of single scan mode, one of the FIFOs (FIFOH) can only be used.

STN LCD CONTROLLER OPERATION

TIMING GENERATION

The STN Controller generates the control signals for LCD driver, such as VFRAME, VLINE, VCLK, and VM signal. These control signals are highly related with the configurations on the LCDCON1/2/3/4/5 registers in the SFR (Special Function Register) Block. Base on these programmable configurations on the LCD control registers in the SFR (Special Function Register) Block, the STN Controller can generate the programmable control signals suitable for the support of many different types of LCD drivers.

The VFRAME signal is asserted to cause the LCD's line pointer to start over at the top of the display.

The VFRAME and VLINE pulse generation depends on the configurations of both the HOZVAL field and the LINEVAL field in the LCDCON2/3 registers. The HOZVAL and LINEVAL can be determined by the size of the LCD panel according to the following equations:

HOZVAL = (Horizontal display size)

LINEVAL = (Vertical display size)

The rate of VCLK signal depends on the CLKVAL field in the LCDCON1 register. Table 14-1 defines the relationship of the frequency of VCLK and CLKVAL. The minimum value of CLKVAL is 2.

VCLK(Hz)=HCLK(Hz)/[CLKVAL] (Where, CLKVAL >= 2)

The frame rate is VFRAME signal frequency. The frame rate is related with the field of LINEVAL, WDLY, LINEBLANK, WLH, HOZVAL, and CLKVAL in LCDCON1 and LCDCON2/3/4 registers. Most LCD drivers need their own adequate frame rate. The frame rate is calculated as follows:

Frame Rate = 1/ [LIINEVAL x { WLH + WDLY + HOZVAL + LINEBLANK } x { CLKVAL / HCLK[Hz] }]

Table 14-1. Relation between VCLK and CLKVAL ex) HCLK=60MHz

CLKVAL	60MHz/X	VCLK
2	60 MHz/2	30.0 MHz
3	60 MHz/3	20.0 MHz
:	:	:

DISPLAY INTERFACE TYPES

The LCD controller supports 3 types of LCD drivers: 4-bit dual scan, 4-bit single scan, and 8-bit single scan display mode.

4-bit Dual Scan Display Type

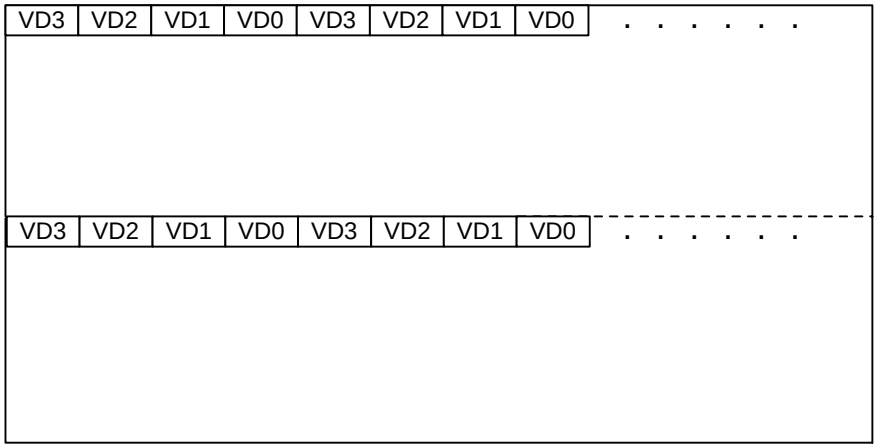
A 4-bit dual scan display uses 8 parallel data lines to shift data to both the upper and lower halves of the display at the same time. The 4 bits of data in the 8 parallel data lines are shifted to the upper half and 4 bits of data is shifted to the lower half. The end of frame is reached when each half of the display has been shifted and transferred. The 8 pins (VD[7:0]) for the LCD output from the LCD controller can be directly connected to the LCD driver.

4-bit Single Scan Display Type

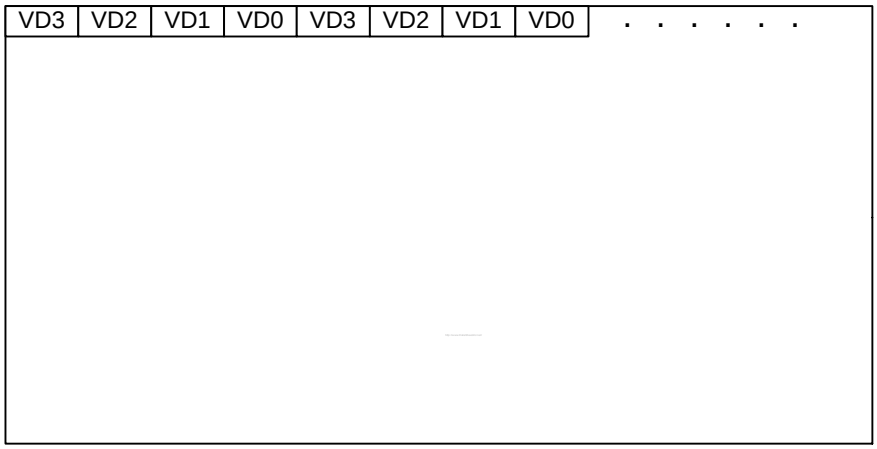
A 4-bit single scan display uses 4 parallel data lines to shift data to successive single horizontal lines of the display at a time, until the entire frame has been shifted and transferred. The 4 pins (VD[3:0]) for the LCD output from the LCD controller can be directly connected to the LCD driver, and the 4 pins (VD[7:4]) for the LCD output are not used.

8-bit Single Scan Display Type

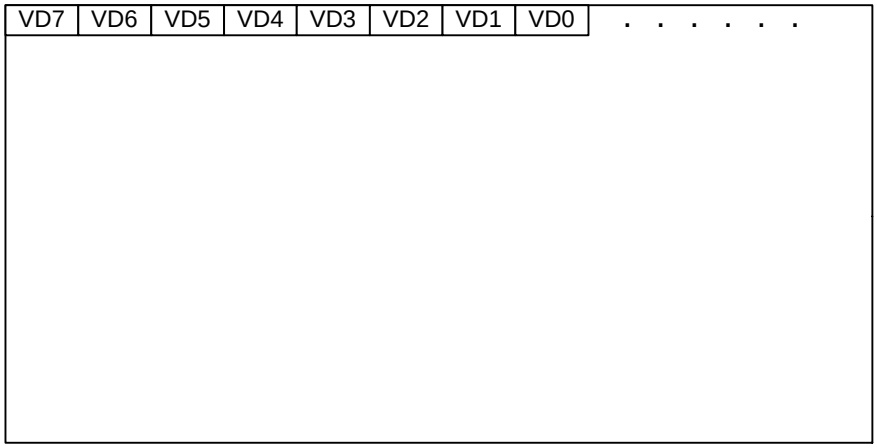
An 8-bit single scan display uses 8 parallel data lines to shift data to successive single horizontal lines of the display at a time, until the entire frame has been shifted and transferred. The 8 pins (VD[7:0]) for the LCD output from the LCD controller can be directly connected to the LCD driver.



4-bit Dual Scan Display



4-bit Single Scan Display



8-bit Single Scan Display

Figure 14-2. Monochrome Display Types (STN)

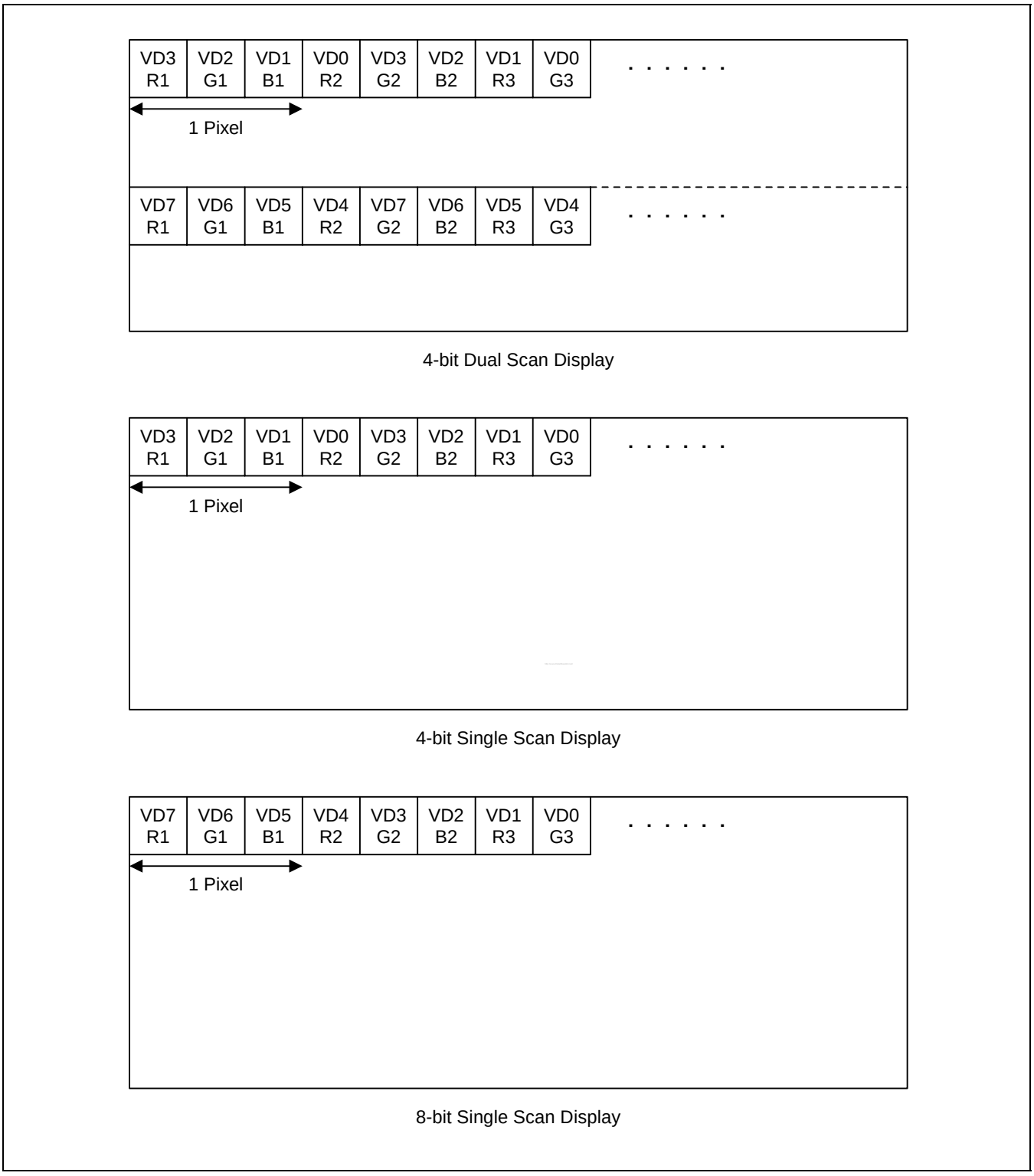


Figure 14-3. Color Display Types (STN)

VIDEO OPERATION

The STN controller within the S3C2413X supports the monochrome, 4 gray levels, and 16 gray levels for monochrome STN panel. And it supports 1, 2, 4 or 8-bpp(bit per pixel) palettized color displays, and 8, 12 or 16-bpp(bit per pixel) non-palettized color displays for CSTN (Color STN). It supports the dedicated DMA for the successive image data fetch from the system memory (frame buffer). The data fetched from memory could use palette memory if it is needed. The data fetch from palette or by-passed palette data should use gamma correction table, which block will submit the gamma corrected data. For the gray or color mode, it is required to implement the shades of gray level or color according to time-based dithering algorithm and Frame Rate Control (FRC) method. The monochrome mode bypasses these modules (FRC and lookup table). The data path is illustrated following Figure.

The following sections describe the operation on the gray and color mode in terms of the lookup table, FRC and so on.

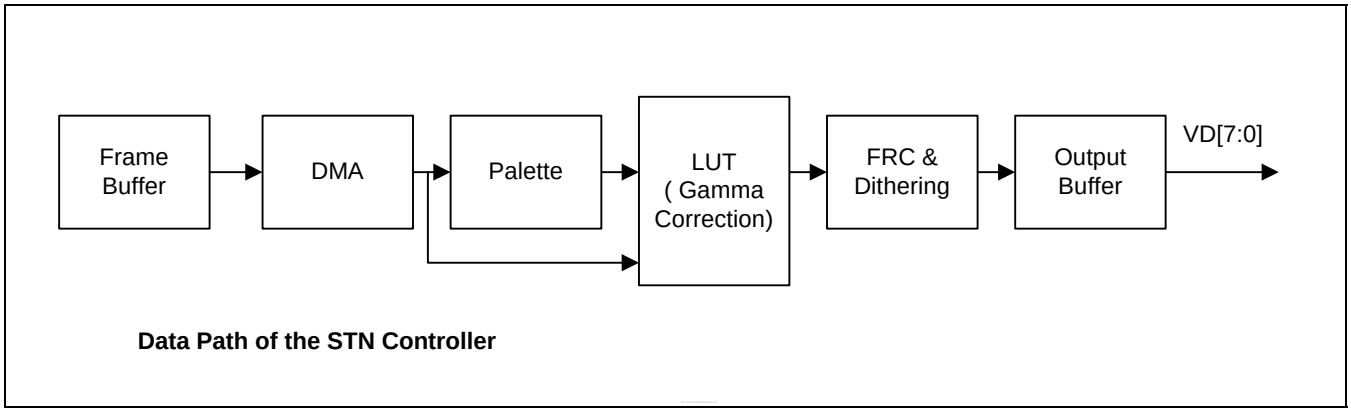


Figure 14-4. Data Path of the STN Controller

LOOKUP TABLE (GAMMA CORRECTION TABLE FOR STN)

The S3C2413X can support the lookup table for various selection of color or gray level mapping, ensuring flexible operation for users. The lookup table is the palette which allows the selection on the level of color or gray (Selection on 16-gray levels among 64 gray levels in case of 4-bit gray mode, selection on 32 red levels among 128 levels, 64 green levels among 128 levels and 32 blue levels among 128 levels in case of 16-bit (64K) color mode). In other words, users can select 16 gray levels (4bit gray) among 128 gray levels by using the lookup table in the 16 gray level mode. In case of 64K color mode(16-bit color), 5 bits are allocated for red, 6 bits for green and 5 bits for blue. The 64K colors mean that the colors are formed from the combination of 32 red, 64 green and 32 blue levels (32x64x32 = 64K). In the color mode, the lookup table can be used for suitable selections. Thirty two red levels can be selected among 128 possible red levels, Sixty four green levels among 128 green levels, and thirty two blue levels among 128 blue levels. In case of 4096 color mode, the colors are formed from the combination of 16 red, 16 green and 16 blue levels (16x16x16 = 4096).

The GREENLUT[223:0] and BLUELUT[223:0] has the lut (lookup table) of green color and blue color, which is consist of 32 x 7bit (32 level and 7bit per level). And the REDLUT[447:0]] has the lut (lookup table) of red color, which is consist of 64 x 7bit (64 level and 7bit per level). If you use the recommended sfr set, gamma table will be linear line. So, you should change the value if you want to use the characteristic curve (well tempered curve for specific LCD panel).

FRC and Dithering (STN)

Video data must process by a dithering and FRC algorithm for STN LCD displays (except monochrome). The main principle of gray and color level display on the STN panel based on FRC is described. For example, to display the third gray (3/16) level from a total of 16 levels, the 3 times pixel should be on and 13 times pixel off. In other words, 3 frames should be selected among the 16 frames, of which 3 frames should have a pixel-on on a specific pixel while the remaining 13 frames should have a pixel-off on a specific pixel. These 16 frames should be displayed periodically. This is basic principle on how to display the gray level on the screen, so-called gray level display by FRC. In the STN LCD display, we should be reminded of one item, i.e., Flicker Noise due to the simultaneous pixel-on and -off on adjacent frames. For example, if all pixels on first frame are turned on and all pixels on next frame are turned off, the Flicker Noise will be maximized. To reduce the Flicker Noise on the screen, the average probability of pixel-on and -off between frames should be the same. In order to realize this, the Time-based Dithering Algorithm, which varies the pattern of adjacent pixels on every frame, should be used. The STN controller within S3C2413X use random generation number to dither flicker noises.

The FRCPAT register has the FRC table. And the value of this register must be set by the recommended value set for the proper operation.

256 Color Palette (Color Mode Only)

The S3C2413X provides 256 color palette for CSTN Control.
The user can select 256 colors from the 64K colors in these two formats.
The 256 color palette consists of the 256 (depth) x 16-bit SPSRAM. The palette supports 5:6:5 (R:G:B) format.
The user can write the palette as in Table 14-2.

Table 14-2. 5:6:5 Format

INDEX\Bit Pos.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
00H	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1)0X4D000400
01H	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0X4D000404
.....																	.....
FFH	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0X4D0007FC

DMA ADDRESS PARAMETERS (STN/TFT)

DMA Controller within the LCD Controller has 5 address registers, which controller the operation. The 5 address parameters (bold characters) are described below.

LCDBANK

These bits indicate system address[30:22] of the bank location for the video buffer in the system memory. LCDBANK value cannot be changed even when moving the view port. LCD frame buffer should be within aligned 4MB region, which ensures that LCDBANK value will not be changed when moving the view port. So, care should be taken to use the malloc() function.

LCDBASEU

For dual-scan LCD : These bits indicate A[21:1] of the start address of the upper address counter, which is for the upper frame memory of dual scan LCD or the frame memory of single scan LCD.

LCDBASEU

For single-scan LCD : These bits indicate A[21:1] of the start address of the LCD frame buffer.
For dual-scan LCD: These bits indicate A[21:1] of the start address of the lower address counter, which is used for the lower frame memory of dual scan LCD. For single scan LCD: These bits indicate A[21:1] of the end address of the LCD frame buffer.

TFT:

LCDBASEL = ((the frame end address) >>1) + 1
= LCDBASEU +
(PAGEWIDTH+OFFSIZE) x (LINEVAL+1)

STN:

LCDBASEL = ((the frame end address) >>1) + 1
= LCDBASEU +
(PAGEWIDTH+OFFSIZE) x (LINEVAL)

OFFSIZE

Virtual screen offset size (the number of half words).
This value defines the difference between the address of the last half word displayed on the previous LCD line and the address of the first half word to be displayed in the new LCD line.

PAGEWIDTH

Screen page width (the number of half words).
This value defines the width of the view port in the frame.

MEMORY DATA FORMAT (STN)

This section includes some examples of each display mode.

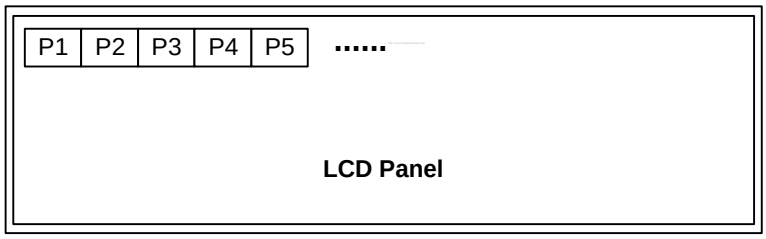
16BPP Display

(BSWP = 0, HWSWP = 0)

	D[31:16]	D[15:0]
000H	P1	P2
004H	P3	P4
008H	P5	P6
...		

(BSWP = 0, HWSWP = 1)

	D[31:16]	D[15:0]
000H	P2	P1
004H	P4	P3
008H	P6	P5
...		



12BPP Display (Non-Palettized type)

(BSWP = 0, HWSWP = 0)

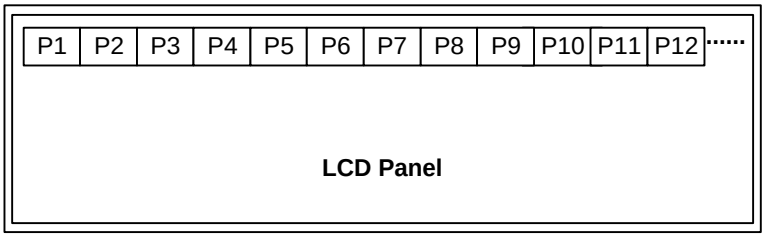
	D[31:16]	D[15:0]
000H	P1	P2
004H	P3	P4
008H	P5	P6
...		

(BSWP = 0, HWSWP = 1)

	D[31:16]	D[15:0]
000H	P2	P1
004H	P4	P3
008H	P6	P5
...		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R3	R2	R1	R0	x	G3	G2	G1	G0	x	x	B3	B2	B1	B0	x

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3	R2	R1	R0	x	G3	G2	G1	G0	x	x	B3	B2	B1	B0	x



8BPP Display (Non-Palettized type or Palettized type)

(BSWP = 0, HWSWP = 0)

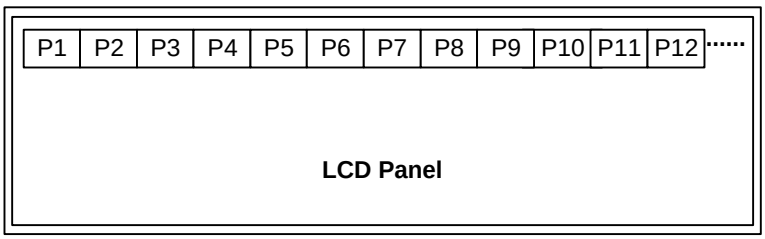
	D[31:24]	D[23:16]	D[15:8]	D[7:0]
000H	P1	P2	P3	P4
004H	P5	P6	P7	P8
008H	P9	P10	P11	P12
...				

(BSWP = 1, HWSWP = 0)

	D[31:24]	D[23:16]	D[15:8]	D[7:0]
000H	P4	P3	P2	P1
004H	P8	P7	P6	P5
008H	P12	P11	P10	P9
...				

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R2	R1	R0	G2	G1	G0	B1	B0	R2	R1	R0	G2	G1	G0	B1	B0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R2	R1	R0	G2	G1	G0	B1	B0	R2	R1	R0	G2	G1	G0	B1	B0



4BPP Display

(BSWP = 0, HWSWP = 0)

	D[31:28]	D[27:24]	D[23:20]	D[19:16]	D[15:12]	D[11:8]	D[7:4]	D[3:0]
000H	P1	P2	P3	P4	P5	P6	P7	P8
004H	P9	P10	P11	P12	P13	P14	P15	P16
008H	P17	P18	P19	P20	P21	P22	P23	P24
...								

(BSWP = 1, HWSWP = 0)

	D[31:28]	D[27:24]	D[23:20]	D[19:16]	D[15:12]	D[11:8]	D[7:4]	D[3:0]
000H	P7	P8	P5	P6	P3	P4	P1	P2
004H	P15	P16	P13	P14	P11	P12	P9	P10
008H	P23	P24	P21	P22	P19	P20	P17	P18
...								

2BPP Display

(BSWP = 0, HWSWP = 0)

D	[31:30]	[29:28]	[27:26]	[25:24]	[23:22]	[21:20]	[19:18]	[17:16]
000H	P1	P2	P3	P4	P5	P6	P7	P8
004H	P17	P18	P19	P20	P21	P22	P23	P24
008H	P33	P34	P35	P36	P37	P38	P39	P40
...								

D	[15:14]	[13:12]	[11:10]	[9:8]	[7:6]	[5:4]	[3:2]	[1:0]
000H	P9	P10	P11	P12	P13	P14	P15	P16
004H	P25	P26	P27	P28	P29	P30	P31	P32
008H	P41	P42	P43	P44	P45	P46	P47	P48
...								

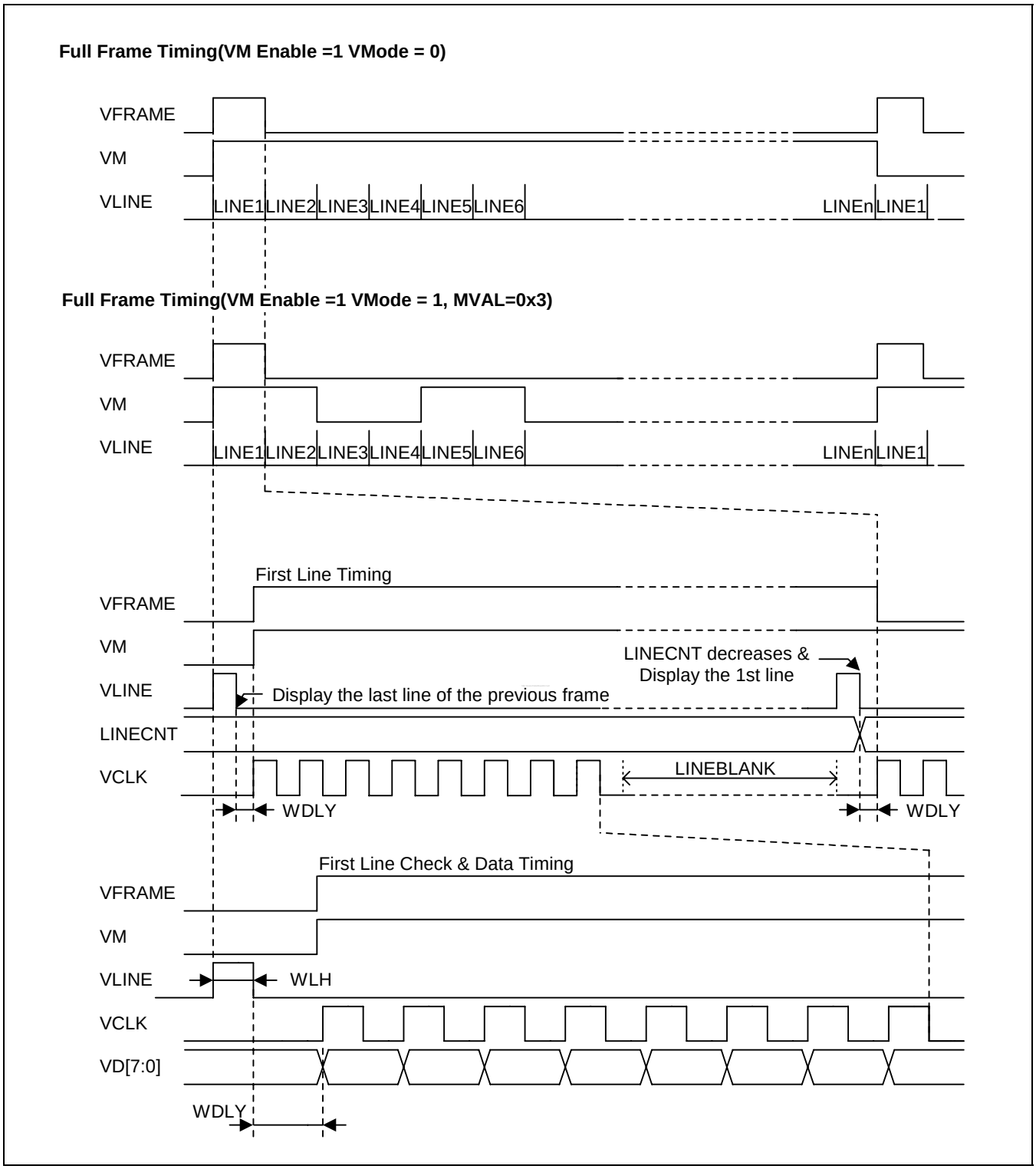


Figure 14-5. STN LCD Timing Example

TFT LCD CONTROLLER OPERATION

The TIMEGEN generates the control signals for LCD driver, such as VSYNC, HSYNC, VCLK, VDEN, and LEND signal. These control signals are highly related with the configurations on the LCDCON1/2/3/4/5 registers in the REGBANK. Base on these programmable configurations on the LCD control registers in the REGBANK, the TIMEGEN can generate the programmable control signals suitable for the support of many different types of LCD drivers.

The VSYNC signal is asserted to cause the LCD's line pointer to start over at the top of the display.

The VSYNC and HSYNC pulse generation depends on the configurations of both the HOZVAL field and the LINEVAL field in the LCDCON2/3 registers. The HOZVAL and LINEVAL can be determined by the size of the LCD panel according to the following equations:

HOZVAL = (Horizontal display size) -1

LINEVAL = (Vertical display size) -1

The rate of VCLK signal depends on the CLKVAL field in the LCDCON1 register. Table 14-3 defines the relationship of VCLK and CLKVAL. The minimum value of CLKVAL is 0.

VCLK(Hz)=HCLK/[(CLKVAL+1)x2]

The frame rate is VSYNC signal frequency. The frame rate is related with the field of VSYNC, VBPD, VFPD, LINEVAL, HSYNC, HBPD, HFPD, HOZVAL, and CLKVAL in LCDCON1 and LCDCON2/3/4 registers. Most LCD drivers need their own adequate frame rate. The frame rate is calculated as follows:

Frame Rate = 1/ [{ (VSPW+1) + (VBPD+1) + (LIINEVAL + 1) + (VFPD+1) } x {(HSPW+1) + (HBPD +1) + (HFPD+1) + (HOZVAL + 1) } x { 2 x (CLKVAL+1) / (HCLK) }]

Table 14-3. Relation between VCLK and CLKVAL (TFT, HCLK=60MHz)

CLKVAL	60MHz/X	VCLK
1	60 MHz/4	15.0 MHz
2	60 MHz/6	10.0 MHz
:	:	:
1023	60 MHz/2048	30.0 kHz

VIDEO OPERATION

The TFT LCD controller within the S3C2413X supports 1, 2, 4 or 8 bpp (bit per pixel) palettized color displays and 16 or 24 bpp non-palettized true-color displays.

256 Color Palette

The S3C2413X can support the 256 color palette for various selection of color mapping, providing flexible operation for users.

MEMORY DATA FORMAT (TFT)

This section includes some examples of each display mode.

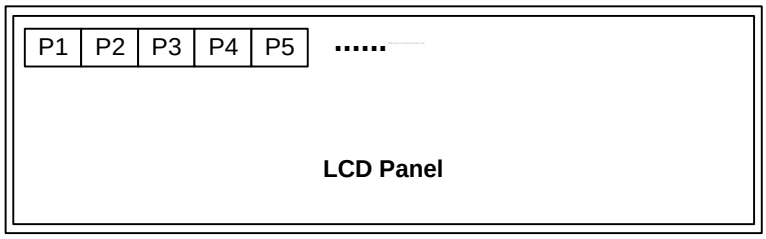
24BPP Display

(BSWP = 0, HWSWP = 0, BPP24BL = 0)

	D[31:24]	D[23:0]
000H	Dummy Bit	P1
004H	Dummy Bit	P2
008H	Dummy Bit	P3
...		

(BSWP = 0, HWSWP = 0, BPP24BL = 1)

	D[31:8]	D[7:0]
000H	P1	Dummy Bit
004H	P2	Dummy Bit
008H	P3	Dummy Bit
...		



VD Pin Descriptions at 24BPP

VD	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED	7	6	5	4	3	2	1	0																
GREEN									7	6	5	4	3	2	1	0								
BLUE																	7	6	5	4	3	2	1	0

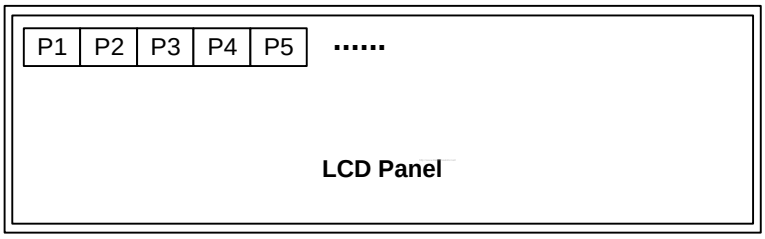
16BPP Display]

(BSWP = 0, HWSWP = 0)

	D[31:16]	D[15:0]
000H	P1	P2
004H	P3	P4
008H	P5	P6
...		

(BSWP = 0, HWSWP = 1)

	D[31:16]	D[15:0]
000H	P2	P1
004H	P4	P3
008H	P6	P5
...		



VD Pin Descriptions at 16BPP

(5:6:5)

VD	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED	4	3	2	1	0	NC									NC							NC		
GREEN									5	4	3	2	1	0										
BLUE																	4	3	2	1	0			

(5:5:5:I)

VD	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED	4	3	2	1	0	**I**	NC								NC								NC	
GREEN									4	3	2	1	0	**I**										
BLUE																	4	3	2	1	0	**I**		

NOTE : The unused VD pins can be used as GPIO

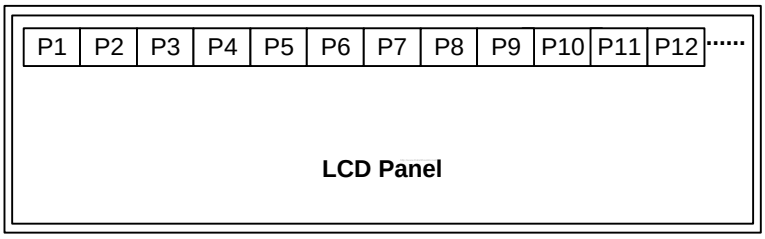
8BPP Display

(BSWP = 0, HWSWP = 0)

	D[31:24]	D[23:16]	D[15:8]	D[7:0]
000H	P1	P2	P3	P4
004H	P5	P6	P7	P8
008H	P9	P10	P11	P12
...				

(BSWP = 1, HWSWP = 0)

	D[31:24]	D[23:16]	D[15:8]	D[7:0]
000H	P4	P3	P2	P1
004H	P8	P7	P6	P5
008H	P12	P11	P10	P9
...				



4BPP Display

(BSWP = 0, HWSWP = 0)

	D[31:28]	D[27:24]	D[23:20]	D[19:16]	D[15:12]	D[11:8]	D[7:4]	D[3:0]
000H	P1	P2	P3	P4	P5	P6	P7	P8
004H	P9	P10	P11	P12	P13	P14	P15	P16
008H	P17	P18	P19	P20	P21	P22	P23	P24
...								

(BSWP = 1, HWSWP = 0)

	D[31:28]	D[27:24]	D[23:20]	D[19:16]	D[15:12]	D[11:8]	D[7:4]	D[3:0]
000H	P7	P8	P5	P6	P3	P4	P1	P2
004H	P15	P16	P13	P14	P11	P12	P9	P10
008H	P23	P24	P21	P22	P19	P20	P17	P18
...								

2BPP Display

(BSWP = 0, HWSWP = 0)

D	[31:30]	[29:28]	[27:26]	[25:24]	[23:22]	[21:20]	[19:18]	[17:16]
000H	P1	P2	P3	P4	P5	P6	P7	P8
004H	P17	P18	P19	P20	P21	P22	P23	P24
008H	P33	P34	P35	P36	P37	P38	P39	P40
...								

D	[15:14]	[13:12]	[11:10]	[9:8]	[7:6]	[5:4]	[3:2]	[1:0]
000H	P9	P10	P11	P12	P13	P14	P15	P16
004H	P25	P26	P27	P28	P29	P30	P31	P32
008H	P41	P42	P43	P44	P45	P46	P47	P48
...								

256 PALETTE USAGE (TFT)

Palette Configuration and Format Control

The S3C2413X provides 256 color palette for TFT LCD Control.
The user can select 256 colors from the 64K colors in these two formats.
The 256 color palette consists of the 256 (depth) x 16-bit SPSRAM. The palette supports 5:6:5 (R:G:B) format and 5:5:5:1(R:G:B:I) format.
When the user uses 5:5:5:1 format, the intensity data(I) is used as a common LSB bit of each RGB data. So, 5:5:5:1 format is the same as R(5+I):G(5+I):B(5+I) format.
In 5:5:5:1 format, for example, the user can write the palette as in Table 14-5 and then connect VD pin to TFT LCD panel(R(5+I)=VD[23:19]+VD[18], VD[10] or VD[2], G(5+I)=VD[15:11]+ VD[18], VD[10] or VD[2], B(5+I)=VD[7:3]+ VD[18], VD[10] or VD[2].), and set FRM565 of LCDCON5 register to 0.

Table 14-4. 5:6:5 Format

INDEX\Bit Pos.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
00H	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	[1)]0X4D000400
01H	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0X4D000404
.....																	.....
FFH	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0X4D0007FC
Number of VD	23	22	21	20	19	15	14	13	12	11	10	7	6	5	4	3	

Table 14-5. 5:5:5:1 Format

INDEX\Bit Pos.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
00H	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	I	0X4D000400
01H	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	I	0X4D000404
.....																	.....
FFH	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	I	0X4D0007FC
Number of VD	23	22	21	20	19	15	14	13	12	11	7	6	5	4	3	[2)]	

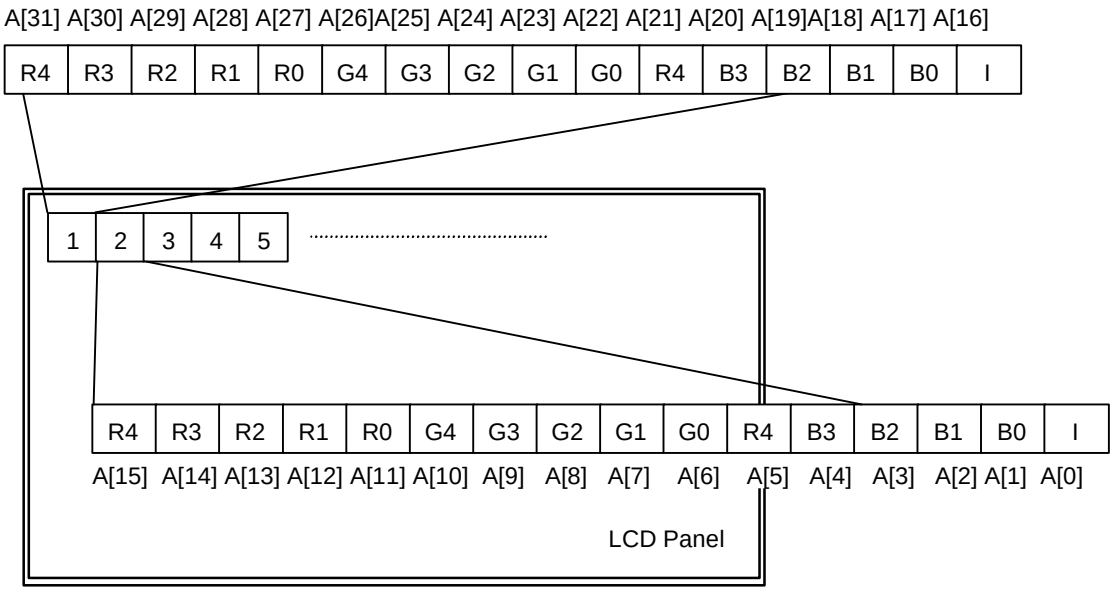
NOTES:
1. 0x4D000400 is Palette start address.
2. VD18, VD10 and VD2 have the same output value, I.
3. DATA[31:16] is invalid.

Palette Read/Write

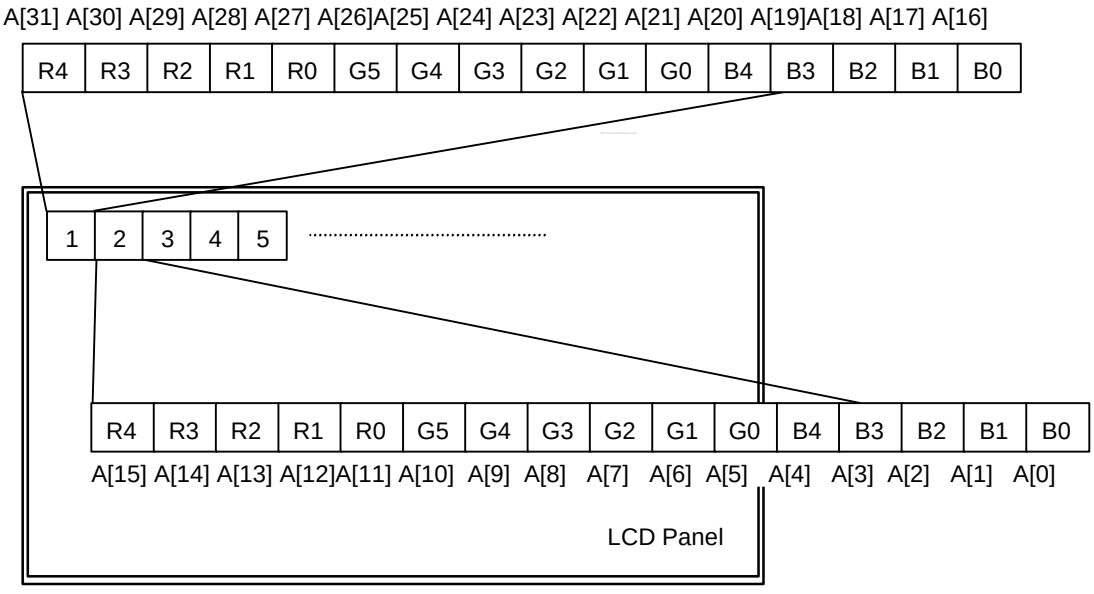
The Read/Write operation on the palette must be written only while ENVID bit set 0.

Temporary Palette Configuration

The S3C2413X allows the user to fill a frame with one color without complex modification to fill the one color to the frame buffer or palette. The one colored frame can be displayed by the writing a value of the color which is displayed on LCD panel to TPALVAL of TPAL register and enable TPALEN.



16BPP 5:5:5+1 Format(Non-Palette)



16BPP 5:6:5 Format(Non-Palette)

Figure 14-5. 16BPP Display Types (TFT)

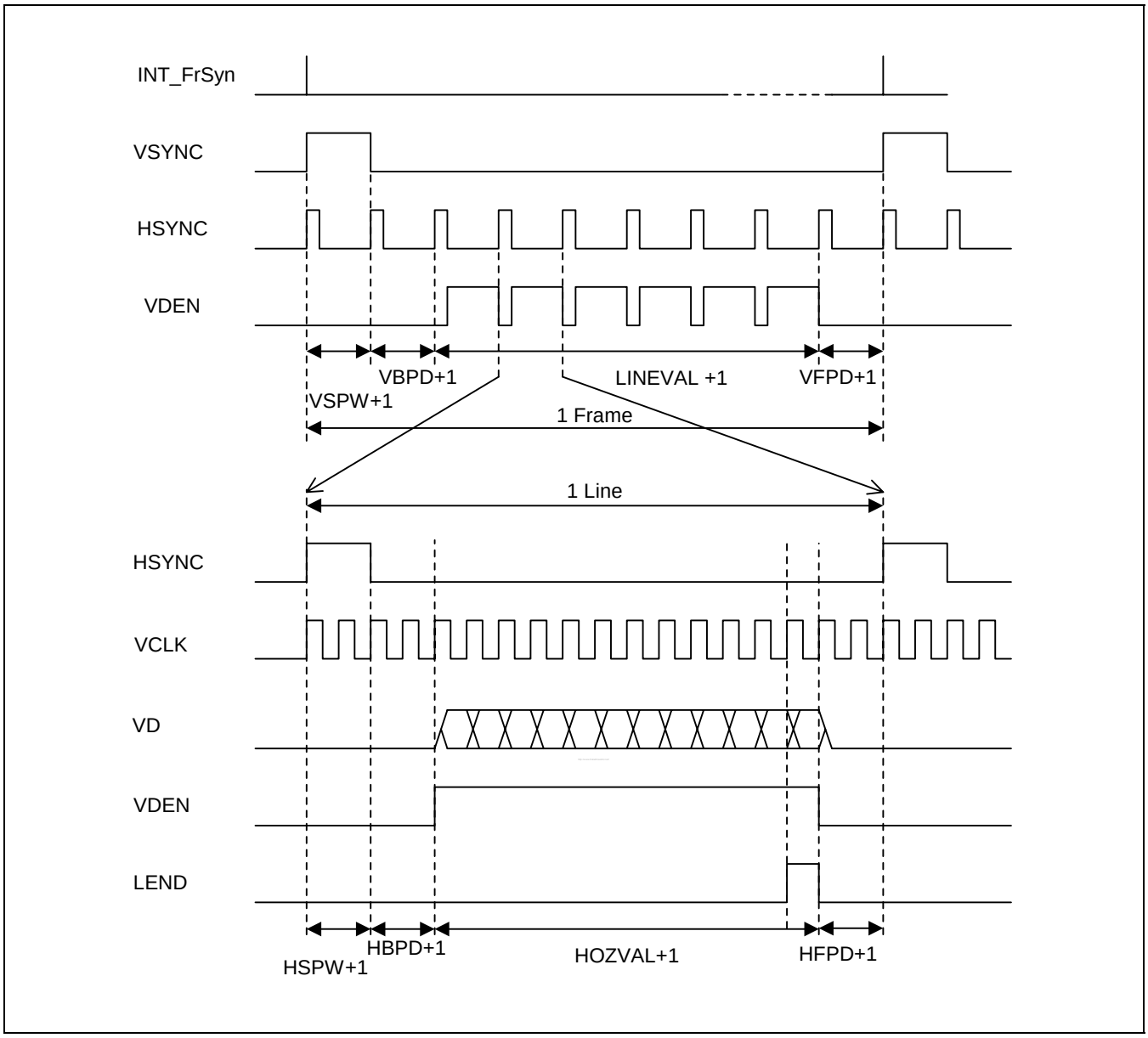


Figure 14-6. TFT LCD Timing Example

SAMSUNG TFT LCD PANEL (3.5" PORTRAIT / 256K COLOR / REFLECTIVE A-SI/TRANSFLECTIVE A-SI TFT LCD)

The S3C2413X supports following SEC TFT LCD panels.

1. SAMSUNG 3.5" Portrait / 256K Color /Reflective a-Si TFT LCD.
   LTS350Q1-PD1: TFT LCD panel with touch panel and front light unit
   LTS350Q1-PD2: TFT LCD panel only
2. SAMSUNG 3.5" Portrait / 256K Color /Transflective a-Si TFT LCD.
   LTS350Q1-PE1: TFT LCD panel with touch panel and front light unit
   LTS350Q1-PE2: TFT LCD panel only

The S3C2413X provides timing signals as follows to use LTS350Q1-PD1 / PD2 and LTS350Q1-PE1 / PE2

LTS350Q1-PD1 / PD2	LTS350Q1-PE1 / PE2
STH: Horizontal Start Pulse TP: Source Driver Data Load Pulse INV: Digital Data Inversion LCD_HCLK: Horizontal Sampling Clock CPV: Vertical Shift Clock STV: Vertical Start Pulse OE: Gate On Enable REV: Inversion Signal REVB: Inversion Signal	STH: Horizontal Start Pulse TP: Source Driver Data Load Pulse INV: Digital Data Inversion LCD_HCLK: Horizontal Sampling Clock CPV: Vertical Shift Clock STV: Vertical Start Pulse LCCINV: Source drive IC sampling inversion signal REV: VCOM modulation Signal REVB: Inversion Signal

So, LTS350Q1-PD1/2 and PE1/2 can be connected with the S3C2413X without using the additional timing control logic.
But the user should additionally apply Vcom generator circuit, various voltages, INV signal and Gray scale voltage generator circuit, which is recommended by PRODUCT INFORMATION (SPEC) of LTS350Q1-PD1/2 and PE1/2.
Detailed timing diagram is also described in PRODUCT INFORMATION (SPEC) of LTS350Q1-PD1/2 and PE1/2.

Refer to the documentation (PRODUCT INFORMATION of LTS350Q1-PD1/2 and PE1/2), which is prepared by AMLCD Technical Customer Center of Samsung Electronics Co., LTD.

CAUTION:

The S3C2413X has HCLK, working as the clock of AHB bus.
Accidentally, SEC TFT LCD panel (LTS350Q1-PD1/2 and PE1/2) has Horizontal Sampling Clock (HCLK).
These two HCLKs may cause a confusion. So, note that HCLK of the S3C2413X is HCLK and other HCLK of the LTS350 is LCD_HCLK.

Check that the HCLK of SEC TFT LCD panel (LTS350Q1-PD1/2 and PE1/2) is changed to LCD_HCLK.

VIRTUAL DISPLAY (TFT/STN)

The S3C2413X supports hardware horizontal or vertical scrolling. If the screen is scrolled, the fields of LCDBASEU and LCDBASEL in LCDSADDR1/2 registers need to be changed (see Figure 14-8), except the values of PAGEWIDTH and OFFSIZE.
The video buffer in which the image is stored should be larger than the LCD panel screen in size.

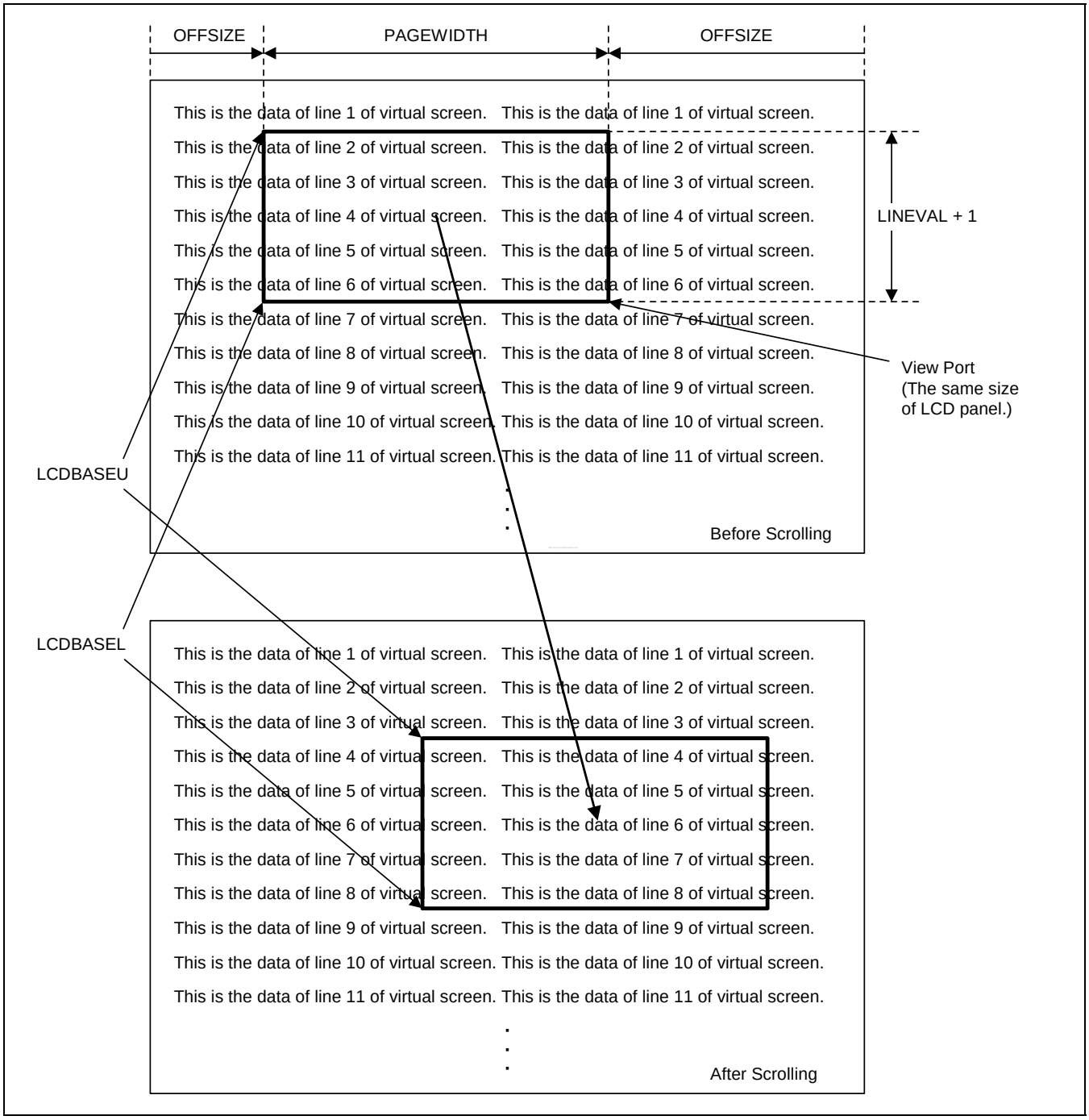


Figure 14-7. Example of Scrolling in Virtual Display (Single Scan)

LCD CONTROLLER SPECIAL REGISTERS

LCD Control 1 Register

Register	Address	R/W	Description	Reset Value
LCDCON1	0X4D000000	R/W	LCD control 1 register	0x00000000

LCDCON1	Bit	Description	Initial State
LINECNT (read only)	[27:18]	Provide the status of the line counter. Down count from LINEVAL to 0	0
CLKVAL	[17:8]	Determine the rates of VCLK and CLKVAL[9:0]. **STN:** VCLK = HCLK / (CLKVAL) (CLKVAL ≥ 2) **TFT:** VCLK = HCLK / [(CLKVAL+1) x 2] (CLKVAL ≥ 0)	0
STNCOL	[7]	**STN**: Select Color or Monochrome STN 0: Color 1: Monochrome	0
PNRMODE	[6:5]	Select the display mode. 00 = 4-bit dual scan display mode (STN) 01 = 4-bit single scan display mode (STN) 10 = 8-bit single scan display mode (STN) 11 = TFT LCD panel	0
BPPMODE	[4:1]	Select the BPP (Bits Per Pixel) mode. 0000 = 1 bpp for CSTN, (STNCOL = 0) 1 bpp for STN, (STNCOL = 1) 0001 = 2 bpp for CSTN, (STNCOL = 0) 2 bpp for STN, (STNCOL = 1) 0010 = 4 bpp for CSTN, (STNCOL = 0) 4 bpp for STN, (STNCOL = 1) 0011 = 8 bpp for CSTN, (STNCOL = 0) 0100 = 8 bpp for CSTN, (STNCOL = 0) 0101 = 12 bpp for CSTN,(STNCOL = 0) 0110 = 16 bpp for CSTN,(STNCOL = 0) 1000 = 1 bpp for TFT 1001 = 2 bpp for TFT 1010 = 4 bpp for TFT 1011 = 8 bpp for TFT 1100 = 16 bpp for TFT 1101 = 24 bpp for TFT	0
ENVID	[0]	LCD video output and the logic enable/disable. 0 = Disable the video output and the LCD control signal. 1 = Enable the video output and the LCD control signal.	0

LCD Control 2 Register

Register	Address	R/W	Description	Reset Value
LCDCON2	0X4D000004	R/W	LCD control 2 register	0x00000000

LCDCON2	Bit	Description	Initial State
VBPD	[31:24]	**TFT**: Vertical back porch is the number of inactive lines at the start of a frame, after vertical synchronization period. **STN**: These bits should be set to zero on STN LCD.	0
LINEVAL	[23:14]	**TFT:**These bits determine the vertical size of LCD panel. STN: LCD VERTICAL SIZE (Panel Y size)	0
VFPD	[13:6]	**TFT**: Vertical front porch is the number of inactive lines at the end of a frame, before vertical synchronization period. **STN**: These bits should be set to zero on STN LCD.	0
VSPW	[5:0]	**TFT**: Vertical sync pulse width determines the VSYNC pulse's high level width by counting the number of inactive lines. **STN**: These bits should be set to zero on STN LCD.	0

LCD Control 3 Register

Register	Address	R/W	Description	Reset Value
LCDCON3	0X4D000008	R/W	LCD control 3 register	0x00000000

LCDCON3	Bit	Description	Initial state
Reserved	[27]	Should be '0'	0
HBPD (TFT)	[25:19]	**TFT**: Horizontal back porch is the number of VCLK periods between the falling edge of HSYNC and the start of active data.	0
WDLY (STN)		**STN**: WDLY (Base on System Clock)	
HOZVAL	[18:8]	**TFT**: These bits determine the horizontal size of LCD panel. HOZVAL has to be determined to meet the condition that total bytes of 1 line are 4n bytes. If the x size of LCD is 120 dot in mono mode, x=120 cannot be supported because 1 line consists of 15 bytes. Instead, x=128 in mono mode can be supported because 1 line is composed of 16 bytes (2n). LCD panel driver will discard the additional 8 dot. **STN**: LCD HORIZONTAL SIZE (Panel X size)	0
HFPD (TFT)	[7:0]	**TFT**: Horizontal front porch is the number of VCLK periods between the end of active data and the rising edge of HSYNC.	0
LINEBLANK (STN)		**STN**: LINE BLANK (Base on System Clock)	

LCD Control 4 Register

Register	Address	R/W	Description	Reset Value
LCDCON4	0X4D00000C	R/W	LCD control 4 register	0x00000000

LCDCON4	Bit	Description	Initial state
VMMODE	[18:16]	**STN**: VMMODE [18] VM Enable [17] VMode [16] Reset per Frame when VMMODE[21:20] is all high [15:8] Valid Line Number when VMMODE[21:20] is all high (Minimum 1).	0
MVAL	[15:8]	**STN**: These bit define the rate at which the VM signal will toggle if the VMMODE[18:17] bit is set to logic '0x3'. (Minimum value : 1)	0
HSPW(TFT)	[7:0]	**TFT**: Horizontal sync pulse width determines the HSYNC pulse's high level width by counting the number of the VCLK.	0
WLH(STN)		**STN**: WLH (Base on System Clock, Minimum=1)	

LCD Control 5 Register

Register	Address	R/W	Description	Reset Value
LCDCON5	0X4D000010	R/W	LCD control 5 register	0x00000000

LCDCON5	Bit	Description	Initial state
Reserved	[31:17]	This bit is reserved and the value should be '0'.	0
VSTATUS	[16:15]	**TFT**: Vertical Status (read only). 00 = VSYNC 01 = BACK Porch 10 = ACTIVE 11 = FRONT Porch	0
HSTATUS	[14:13]	**TFT**: Horizontal Status (read only). 00 = HSYNC 01 = BACK Porch 10 = ACTIVE 11 = FRONT Porch	0
BPP24BL	[12]	**TFT**: This bit determines the order of 24 bpp video memory. 0 = LSB valid 1 = MSB Valid	0
FRM565	[11]	**TFT**: This bit selects the format of 16 bpp output video data. 0 = 5:5:5:1 Format 1 = 5:6:5 Format	0
INVVCLK	[10]	**STN/TFT**: This bit controls the polarity of the VCLK active edge. 0 = The video data is fetched at VCLK falling edge 1 = The video data is fetched at VCLK rising edge	0
INVVLINE	[9]	**STN/TFT**: This bit indicates the VLINE/HSYNC pulse polarity. 0 = Normal 1 = Inverted	0
INVVFRAME	[8]	**STN/TFT**: This bit indicates the VFRAME/VSYNC pulse polarity. 0 = Normal 1 = Inverted	0
INVVD	[7]	**STN/TFT**: This bit indicates the VD (video data) pulse polarity. 0 = Normal 1 = VD is inverted.	0
INVVDEN	[6]	**TFT**: This bit indicates the VDEN signal polarity. 0 = normal 1 = inverted	0
Reserved	[5]	This bit is reserved and the value should be '0'.	0
INVLEND	[4]	**TFT**: This bit indicates the LEND signal polarity. 0 = normal 1 = inverted	0
Reserved	[3]	This bit is reserved and the value should be '0'.	0
ENLEND	[2]	**TFT**: LEND output signal enable/disable. 0 = Disable LEND signal 1 = Enable LEND signal	0
BSWP	[1]	**STN/TFT**: Byte swap control bit. 0 = Swap Disable 1 = Swap Enable	0
HWSWP	[0]	**STN/TFT**: Half-Word swap control bit. 0 = Swap Disable 1 = Swap Enable	0

FRAME Buffer Start Address 1 Register

Register	Address	R/W	Description	Reset Value
LCDSADDR1	0X4D000014	R/W	**STN/TFT**: Frame buffer start address 1 register	0x00000000

LCDSADDR1	Bit	Description	Initial State
LCDBANK	[29:21]	These bits indicate A[30:22] of the bank location for the video buffer in the system memory. LCDBANK value cannot be changed even when moving the view port. LCD frame buffer should be within aligned 4MB region, which ensures that LCDBANK value will not be changed when moving the view port. So, care should be taken to use the malloc() function.	0x00
LCDBASEU	[20:0]	For dual-scan LCD : These bits indicate A[21:1] of the start address of the upper address counter, which is for the upper frame memory of dual scan LCD or the frame memory of single scan LCD. For single-scan LCD : These bits indicate A[21:1] of the start address of the LCD frame buffer.	0x000000

FRAME Buffer Start Address 2 Register

Register	Address	R/W	Description	Reset Value
LCDSADDR2	0X4D000018	R/W	**STN/TFT**: Frame buffer start address 2 register	0x00000000

LCDSADDR2	Bit	Description	Initial State
LCDBASEL	[20:0]	For dual-scan LCD: These bits indicate A[21:1] of the start address of the lower address counter, which is used for the lower frame memory of dual scan LCD. For single scan LCD: These bits indicate A[21:1] of the end address of the LCD frame buffer. LCDBASEL = ((the frame end address) >>1) + 1 = LCDBASEU + (PAGEWIDTH+OFFSIZE) x (LINEVAL+1)	0x0000

NOTE: Users can change the LCDBASEU and LCDBASEL values for scrolling while the LCD controller is turned on.
But, users must not change the value of the LCDBASEU and LCDBASEL registers at the end of FRAME by referring to the LINECNT field in LCDCON1 register, for the LCD FIFO fetches the next frame data prior to the change in the frame.
So, if you change the frame, the pre-fetched FIFO data will be obsolete and LCD controller will display an incorrect screen. To check the LINECNT, interrupts should be masked. If any interrupt is executed just after reading LINECNT, the read LINECNT value may be obsolete because of the execution time of Interrupt Service Routine (ISR).

FRAME Buffer Start Address 3 Register

Register	Address	R/W	Description	Reset Value
LCDSADDR3	0X4D00001C	R/W	**STN/TFT**: Frame buffer start address 3 register	0x00000000

LCDSADDR3	Bit	Description	Initial State
OFFSIZE	[21:11]	Virtual screen offset size (the number of half words). This value defines the difference between the address of the last half word displayed on the previous LCD line and the address of the first half word to be displayed in the new LCD line.	00000000000
PAGEWIDTH	[10:0]	Virtual screen page width (the number of half words). This value defines the width of the view port in the frame.	000000000

NOTE: The values of PAGEWIDTH and OFFSIZE must be changed when ENVID bit is 0.

Example 1. LCD panel = 320 x 240, 16gray, single scan
Frame start address = 0x0c500000
Offset dot number = 2048 dots (512 half words)

LINEVAL = 240-1 = 0xef
PAGEWIDTH = 320 x 4 / 16 = 0x50
OFFSIZE = 512 = 0x200
LCDBANK = 0x0c500000 >> 22 = 0x31
LCDBASEU = 0x100000 >> 1 = 0x80000
LCDBASEL = 0x80000 + (0x50 + 0x200) x (0xef + 1) = 0xa2b00

Example 2. LCD panel = 320 x 240, 16gray, dual scan
Frame start address = 0x0c500000
Offset dot number = 2048 dots (512 half words)

LINEVAL = 120-1 = 0x77
PAGEWIDTH = 320 x 4 / 16 = 0x50
OFFSIZE = 512 = 0x200
LCDBANK = 0x0c500000 >> 22 = 0x31
LCDBASEU = 0x100000 >> 1 = 0x80000
LCDBASEL = 0x80000 + (0x50 + 0x200) x (0x77 + 1) = 0x91580

Example 3. LCD panel = 320*240, color, single scan
Frame start address = 0x0c500000
Offset dot number = 1024 dots (512 half words)

LINEVAL = 240-1 = 0xef
PAGEWIDTH = 320 x 8 / 16 = 0xa0
OFFSIZE = 512 = 0x200
LCDBANK = 0x0c500000 >> 22 = 0x31
LCDBASEU = 0x100000 >> 1 = 0x80000
LCDBASEL = 0x80000 + (0xa0 + 0x200) x (0xef + 1) = 0xa7600

Temp Palette Register

Register	Address	R/W	Description	Reset Value
TPAL	0X4D000020	R/W	**TFT**: Temporary palette register. This register value will be video data at next frame.	0x00000000

TPAL	Bit	Description	Initial state
TPALEN	[24]	Temporary palette register enable bit. 0 = Disable 1 = Enable	0
TPALVAL	[23:0]	Temporary palette value register. TPALVAL[23:16] : RED TPALVAL[15:8] : GREEN TPALVAL[7:0] : BLUE	0x000000

LCD Interrupt Pending Register

Register	Address	R/W	Description	Reset Value
LCDINTPND	0X4D000024	R/W	Indicate the LCD interrupt pending register	0x0

LCDINTPND	Bit	Description	Initial state
INT_FrSyn	[1]	LCD frame synchronized interrupt pending bit. 0 = The interrupt has not been requested. 1 = The frame has asserted the interrupt request.	0
INT_FiCnt	[0]	LCD FIFO interrupt pending bit. 0 = The interrupt has not been requested. 1 = LCD FIFO interrupt is requested when LCD FIFO reaches trigger level.	0

LCD Source Pending Register

Register	Address	R/W	Description	Reset Value
LCDSRCPND	0X4D000028	R/W	Indicate the LCD interrupt source pending register	0x0

LCDSRCPND	Bit	Description	Initial state
INT_FrSyn	[1]	LCD frame synchronized interrupt source pending bit. 0 = The interrupt has not been requested. 1 = The frame has asserted the interrupt request.	0
INT_FiCnt	[0]	LCD FIFO interrupt source pending bit. 0 = The interrupt has not been requested. 1 = LCD FIFO interrupt is requested when LCD FIFO reaches trigger level. Note)	0

Note : Though this bit refers to interrupt, at the time of reset, this bit is set. Hence at the time of reset there is no relation with interrupt. You should clear this bit one time to get valid information regarding FIFO after LCDCON1[0] is set.

You can clear a specific bit of the LCDINTPND and LCDSRCPND register by writing a data to this register. It clears only the bit positions of the LCDINTPND or LCDSRCPND register corresponding to those bits which set to 1 in the data. The bit positions corresponding to those that are set to 0 in the data remains as they are.

LCD Interrupt Mask Register

Register	Address	R/W	Description	Reset Value
LCDINTMSK	0X4D00002C	R/W	Determine which interrupt source is masked. The masked interrupt source will not be serviced.	0x3

LCDINTMSK	Bit	Description	Initial state
FIWSEL	[2]	Determine the trigger level of LCD FIFO. 0 = 4 words 1 = 8 words	0
INT_FrSyn	[1]	Mask LCD frame synchronized interrupt. 0 = The interrupt service is available. 1 = The interrupt service is masked.	1
INT_FiCnt	[0]	Mask LCD FIFO interrupt. 0 = The interrupt service is available. 1 = The interrupt service is masked.	1

TCON Control Register

Register	Address	R/W	Description	Reset Value
TCONSEL	0X4D000030	R/W	This register controls the LPC3600/LCC3600 modes.	0xCE6

TCONSEL	Bit	Description	Initial state
LCC_TEST2	[11]	LCC3600 Test Mode 2 (Read Only)	1
LCC_TEST1	[10]	LCC3600 Test Mode 1 (Read Only)	1
LCC_SEL5	[9]	Select STV polarity	0
LCC_SEL4	[8]	Select CPV signal pin 0	0
LCC_SEL3	[7]	Select CPV signal pin 1	1
LCC_SEL2	[6]	Select Line/Dot inversion	1
LCC_SEL1	[5]	Select DG/Normal mode	1
LCC_EN	[4]	Determine LCC3600 Enable/Disable 0 = LCC3600 Disable 1 = LCC3600 Enable	0
CPV_SEL	[3]	Select CPV Pulse low width	0
MODE_SEL	[2]	Select DE/Sync mode 0 = Sync mode 1 = DE mode	1
RES_SEL	[1]	Select output resolution type 0 = 320 x 240 1 = 240 x 320	1
LPC_EN	[0]	Determine LPC3600 Enable/Disable 0 = LPC3600 Disable 1 = LPC3600 Enable	0

NOTE: Both LPC_EN and LCC_EN enable is not permitted. Only one TCON can be enabled at the same time.

LCD Control 6 Register

Register	Address	R/W	Description	Reset Value
LCDCON6	0X4D000034	R/W	LCD control 6 register	0x10503000

LCDCON6	Bit	Description	Initial state
-	[31:0]	**STN**: Reserved for test set to recommand value 0x10803000	0x10503000

LCD Control 7 Register

Register	Address	R/W	Description	Reset Value
LCDCON7	0X4D000038	R/W	LCD control 7 register	0x00000000

LCDCON7	Bit	Description	Initial state
-	[31:0]	**STN**: Reserved for test set to recommand value 0x00000000	0

LCD Control 8 Register

Register	Address	R/W	Description	Reset Value
LCDCON8	0X4D00003C	R/W	LCD control 8 register	0x5C000000

LCDCON8	Bit	Description	Initial state
-	[31:0]	**STN**: Reserved set to recommand value 0x50000000	0x5C000000

LCD Control 9 Register

Register	Address	R/W	Description	Reset Value
LCDCON9	0X4D000040	R/W	LCD control 9 register	0x00000000

LCDCON9	Bit	Description	Initial state
Reserved	[31:0]	This bit is reserved and the value should be ‘0’.	0

RED Lookup Table

Register	Address	R/W	Description	Reset Value
REDLUT0	0X4D000044	R/W	Red Lookup table[31:0]	0
REDLUT1	0X4D000048	R/W	Red Lookup table[63:32]	0
REDLUT2	0X4D00004C	R/W	Red Lookup table[95:64]	0
REDLUT3	0X4D000050	R/W	Red Lookup table[127:96]	0
REDLUT4	0X4D000054	R/W	Red Lookup table[159:128]	0
REDLUT5	0X4D000058	R/W	Red Lookup table[191:160]	0
REDLUT6	0X4D00005C	R/W	Red Lookup table[223:192]	0

GREEN Lookup Table

Register	Address	R/W	Description	Reset Value
GREENLUT0	0X4D000060	R/W	GREEN Lookup table[31:0]	0
GREENLUT1	0X4D000064	R/W	GREEN Lookup table[63:32]	0
GREENLUT2	0X4D000068	R/W	GREEN Lookup table[95:64]	0
GREENLUT3	0X4D00006C	R/W	GREEN Lookup table[127:96]	0
GREENLUT4	0X4D000070	R/W	GREEN Lookup table[159:128]	0
GREENLUT5	0X4D000074	R/W	GREEN Lookup table[191:160]	0
GREENLUT6	0X4D000078	R/W	GREEN Lookup table[223:192]	0
GREENLUT7	0X4D00007C	R/W	GREEN Lookup table[255:224]	0
GREENLUT8	0X4D000080	R/W	GREEN Lookup table[287:256]	0
GREENLUT9	0X4D000084	R/W	GREEN Lookup table[319:288]	0
GREENLUT10	0X4D000088	R/W	GREEN Lookup table[351:320]	0
GREENLUT11	0X4D00008C	R/W	GREEN Lookup table[383:352]	0
GREENLUT12	0X4D000090	R/W	GREEN Lookup table[415:384]	0
GREENLUT13	0X4D000094	R/W	GREEN Lookup table[447:416]	0

BLUE Lookup Table

Register	Address	R/W	Description	Reset Value
BLUELUT0	0X4D000098	R/W	BLUE Lookup table[31:0]	0
BLUELUT1	0X4D00009C	R/W	BLUE Lookup table[63:32]	0
BLUELUT2	0X4D0000A0	R/W	BLUE Lookup table[95:64]	0
BLUELUT3	0X4D0000A4	R/W	BLUE Lookup table[127:96]	0
BLUELUT4	0X4D0000A8	R/W	BLUE Lookup table[159:128]	0
BLUELUT5	0X4D0000AC	R/W	BLUE Lookup table[191:160]	0
BLUELUT6	0X4D0000B0	R/W	BLUE Lookup table[223:192]	0

FRC PATTERN

Register	Address	R/W	Description	Reset Value
FRCPAT0	0X4D0000B4	R/W	FRC Pattern Register	0
FRCPAT1	0X4D0000B8	R/W	FRC Pattern Register	0
FRCPAT2	0X4D0000BC	R/W	FRC Pattern Register	0
FRCPAT3	0X4D0000C0	R/W	FRC Pattern Register	0
FRCPAT4	0X4D0000C4	R/W	FRC Pattern Register	0
FRCPAT5	0X4D0000C8	R/W	FRC Pattern Register	0
FRCPAT6	0X4D0000CC	R/W	FRC Pattern Register	0
FRCPAT7	0X4D0000D0	R/W	FRC Pattern Register	0
FRCPAT8	0X4D0000D4	R/W	FRC Pattern Register	0
FRCPAT9	0X4D0000D8	R/W	FRC Pattern Register	0
FRCPAT10	0X4D0000DC	R/W	FRC Pattern Register	0
FRCPAT11	0X4D0000E0	R/W	FRC Pattern Register	0
FRCPAT12	0X4D0000E4	R/W	FRC Pattern Register	0
FRCPAT13	0X4D0000E8	R/W	FRC Pattern Register	0
FRCPAT14	0X4D0000EC	R/W	FRC Pattern Register	0
FRCPAT15	0X4D0000F0	R/W	FRC Pattern Register	0
FRCPAT16	0X4D0000F4	R/W	FRC Pattern Register	0
FRCPAT17	0X4D0000F8	R/W	FRC Pattern Register	0
FRCPAT18	0X4D0000FC	R/W	FRC Pattern Register	0
FRCPAT19	0X4D000100	R/W	FRC Pattern Register	0
FRCPAT20	0X4D000104	R/W	FRC Pattern Register	0
FRCPAT21	0X4D000108	R/W	FRC Pattern Register	0
FRCPAT22	0X4D00010C	R/W	FRC Pattern Register	0
FRCPAT23	0X4D000110	R/W	FRC Pattern Register	0
FRCPAT24	0X4D000114	R/W	FRC Pattern Register	0
FRCPAT25	0X4D000118	R/W	FRC Pattern Register	0
FRCPAT26	0X4D00011C	R/W	FRC Pattern Register	0
FRCPAT27	0X4D000120	R/W	FRC Pattern Register	0
FRCPAT28	0X4D000124	R/W	FRC Pattern Register	0
FRCPAT29	0X4D000128	R/W	FRC Pattern Register	0
FRCPAT30	0X4D00012C	R/W	FRC Pattern Register	0
FRCPAT31	0X4D000130	R/W	FRC Pattern Register	0
FRCPAT32	0X4D000134	R/W	FRC Pattern Register	0

Register	Address	R/W	Description	Reset Value
FRCPAT33	0X4D000138	R/W	FRC Pattern Register	0
FRCPAT34	0X4D00013C	R/W	FRC Pattern Register	0
FRCPAT35	0X4D000140	R/W	FRC Pattern Register	0
FRCPAT36	0X4D000144	R/W	FRC Pattern Register	0
FRCPAT37	0X4D000148	R/W	FRC Pattern Register	0
FRCPAT38	0X4D00014C	R/W	FRC Pattern Register	0
FRCPAT39	0X4D000150	R/W	FRC Pattern Register	0
FRCPAT40	0X4D000154	R/W	FRC Pattern Register	0
FRCPAT41	0X4D000158	R/W	FRC Pattern Register	0
FRCPAT42	0X4D00015C	R/W	FRC Pattern Register	0
FRCPAT43	0X4D000160	R/W	FRC Pattern Register	0
FRCPAT44	0X4D000164	R/W	FRC Pattern Register	0
FRCPAT45	0X4D000168	R/W	FRC Pattern Register	0
FRCPAT46	0X4D00016C	R/W	FRC Pattern Register	0
FRCPAT47	0X4D000170	R/W	FRC Pattern Register	0
FRCPAT48	0X4D000174	R/W	FRC Pattern Register	0
FRCPAT49	0X4D000178	R/W	FRC Pattern Register	0
FRCPAT50	0X4D00017C	R/W	FRC Pattern Register	0
FRCPAT51	0X4D000180	R/W	FRC Pattern Register	0
FRCPAT52	0X4D000184	R/W	FRC Pattern Register	0
FRCPAT53	0X4D000188	R/W	FRC Pattern Register	0
FRCPAT54	0X4D00018C	R/W	FRC Pattern Register	0
FRCPAT55	0X4D000190	R/W	FRC Pattern Register	0
FRCPAT56	0X4D000194	R/W	FRC Pattern Register	0
FRCPAT57	0X4D000198	R/W	FRC Pattern Register	0
FRCPAT58	0X4D00019C	R/W	FRC Pattern Register	0
FRCPAT59	0X4D0001A0	R/W	FRC Pattern Register	0
FRCPAT60	0X4D0001A4	R/W	FRC Pattern Register	0
FRCPAT61	0X4D0001A8	R/W	FRC Pattern Register	0
FRCPAT62	0X4D0001AC	R/W	FRC Pattern Register	0
FRCPAT63	0X4D0001B0	R/W	FRC Pattern Register	0

LUT & FRC Pattern Setting Guide (STN)

The LCD controller use following setting on STN application.

Recommended FRC Value of STN/CSTN:

FRCPAT0	0X00000000
FRCPAT1	0X80000000
FRCPAT2	0X80000000
FRCPAT3	0X80000000
FRCPAT4	0X00080000
FRCPAT5	0X80000200
FRCPAT6	0X80008000
FRCPAT7	0X80008000
FRCPAT8	0X00000000
FRCPAT9	0X80000000
FRCPAT10	0X00000000
FRCPAT11	0X80000000
FRCPAT12	0X00000000
FRCPAT13	0X80000000
FRCPAT14	0X80808080
FRCPAT15	0X80808080
FRCPAT16	0X00000000
FRCPAT17	0X81000000
FRCPAT18	0X00000000
FRCPAT19	0X82000000
FRCPAT20	0X00000000
FRCPAT21	0X82000000
FRCPAT22	0X84208420
FRCPAT23	0X84208420
FRCPAT24	0X00000000
FRCPAT25	0X84000000
FRCPAT26	0X00000000
FRCPAT27	0X88000000
FRCPAT28	0X00000000
FRCPAT29	0X88800000

FRCPAT30	0X88888888
FRCPAT31	0X88888888
FRCPAT32	0X00000000
FRCPAT33	0X88880000
FRCPAT34	0X00000000
FRCPAT35	0X91200000
FRCPAT36	0X00000000
FRCPAT37	0X92000000
FRCPAT38	0XA248A248
FRCPAT39	0XA248A248
FRCPAT40	0X00000000
FRCPAT41	0X92000000
FRCPAT42	0X00000000
FRCPAT43	0X92928000
FRCPAT44	0X00000000
FRCPAT45	0X92480000
FRCPAT46	0XA8A8A8A8
FRCPAT47	0XA8A8A8A8
FRCPAT48	0X00000000
FRCPAT49	0X94A00000
FRCPAT50	0X00000000
FRCPAT51	0XA5000000
FRCPAT52	0X00000000
FRCPAT53	0XA5200000
FRCPAT54	0XAA54AA54
FRCPAT55	0XAA54AA54
FRCPAT56	0X00000000
FRCPAT57	0XAA800000
FRCPAT58	0X00000000
FRCPAT59	0XAAA80000
FRCPAT60	0X00000000
FRCPAT61	0XAAAA8000
FRCPAT62	0XAAAAAAAA
FRCPAT63	0XAAAAAAAA

Recommended LUT Value in case of CSTN regardless of BPP

Register	Recommend Value
REDLUT4	0X62A50992
REDLUT5	0X9A3260B9
REDLUT6	0XF9E3A70D
GREENLUT4	0XB15284C9
GREENLUT5	0XCD19305C
GREENLUT6	0X7CF1D386
GREENLUT7	0X88D12140
GREENLUT8	0X509D3254
GREENLUT9	0XD58AD529
GREENLUT10	0X3160BD72
GREENLUT11	0XB3568CD9
GREENLUT12	0XDD3970DD
GREENLUT13	0XFDF3D78E
BLUELUT4	0X62A50992
BLUELUT5	0X9A3260B9
BLUELUT6	0XF9E3A70D

Recommended LUT Value in case of CSTN 1/2/4/16BPP

REDLUT0	0X01820200
REDLUT1	0X203860A1
REDLUT2	0XA3058A12
REDLUT3	0X224078E1
GREENLUT0	0X80C10100
GREENLUT1	0X101C3050
GREENLUT2	0XD182C509
GREENLUT3	0X11203C70
BLUELUT0	0X01820200
BLUELUT1	0X203860A1
BLUELUT2	0XA3058A12
BLUELUT3	0X224078E1

Recommended LUT Value in case of CSTN 12BPP

REDLUT0	0X43850600
REDLUT1	0X4478D162
REDLUT2	0X664B9526
REDLUT3	0X2240F9D3
GREENLUT0	0X63C58700
GREENLUT1	0X467CD972
GREENLUT2	0X766BD5A7
GREENLUT3	0X1120FDDB
BLUELUT0	0X43850600
BLUELUT1	0X4478D162
BLUELUT2	0X664B9526
BLUELUT3	0X2240F9D3

Recommended LUT Value in case of CSTN 8BPP

REDLUT0	0X678B0E00
REDLUT1	0X20F9B2B4
REDLUT2	0XA3058A12
REDLUT3	0X224078E1
GREENLUT0	0XE7CB8F00
GREENLUT1	0X10FABAF4
GREENLUT2	0XD182C509
GREENLUT3	0X11203C70
BLUELUT0	0X0F971E00
BLUELUT1	0X203860A1
BLUELUT2	0XA3058A12
BLUELUT3	0X224078E1

Recommended LUT Value in case of STN monochrome

GREENLUT0	0x3F80

Recommended LUT Value in case of STN 4-Gray

GREENLUT0	0xFF55500

Recommended LUT Value in case of STN 16-Gray

GREENLUT0	0x23244400
GREENLUT1	0x4476CD52
GREENLUT2	0x766BB566
GREENLUT3	0xFFDF

Register Setting Guide (TFT LCD)

The CLKVAL register value determines the frequency of VCLK and frame rate.

Frame Rate = 1/ [{ (VSPW+1) + (VBPD+1) + (LIINEVAL + 1) + (VFPD+1) } x {(HSPW+1) + (HBPD +1) + (HFPD+1) + (HOZVAL + 1) } x { 2 x (CLKVAL+1) / (HCLK) }]

For applications, the system timing must be considered to avoid under-run condition of the fifo of the lcd controller caused by memory bandwidth contention.

Example 4:

TFT Resolution: 240 x 240,

VSPW =2, VBPD =14, LINEVAL = 239, VFPD =4

HSPW =25, HBPD =15, HOZVAL = 239, HFPD =1

CLKVAL = 5

HCLK = 60 M (hz)

The parameters below must be referenced by LCD size and driver specifications:

VSPW, VBPD, LINEVAL, VFPD, HSPW, HBPD, HOZVAL, and HFPD

If target frame rate is 60–70Hz, then CLKVAL should be 5.

So, Frame Rate = 67Hz

15 ADC & TOUCH SCREEN INTERFACE

OVERVIEW

The 10-bit CMOS analog to digital converter (ADC) of the S3C2413X is a recycling typed device with 8-channel analog inputs. It converts the analog input signal into 10-bit binary digital codes at a maximum conversion rate of 500KSPS with 2.5 MHz A/D converter clock. The A/D converter operates with on-chip, sample-and-hold function and power down mode is supported.

Touch Screen Interface is controlling pads (XP, XM, YP, YM) of Touch Screen and selecting pads (XP, XM, YP, YM) of The Touch Screen for X-position conversion, Y-position conversion. The Touch Screen Interface contains Touch Screen Pads control logic and ADC interface logic with an interrupt generation logic.

FEATURES

- Resolution: 10-bit
- Differential Linearity Error: ± 1.0 LSB
- Integral Linearity Error: ± 2.0 LSB
- Maximum Conversion Rate: 500 KSPS
- Low Power Consumption
- Power Supply Voltage: 3.3V
- Analog Input Range: 0 ~ 3.3V
- On-chip Sample-and-hold Function
- Normal Conversion Mode
- Separate X/Y position conversion Mode
- Auto (Sequential) X/Y Position Conversion Mode
- Waiting for Interrupt Mode

ADC & TOUCH SCREEN INTERFACE OPERATION

BLOCK DIAGRAM

Figure 15-1 shows the functional block diagram of A/D converter and Touch Screen Interface. Note that the A/D converter device is a recycling type.

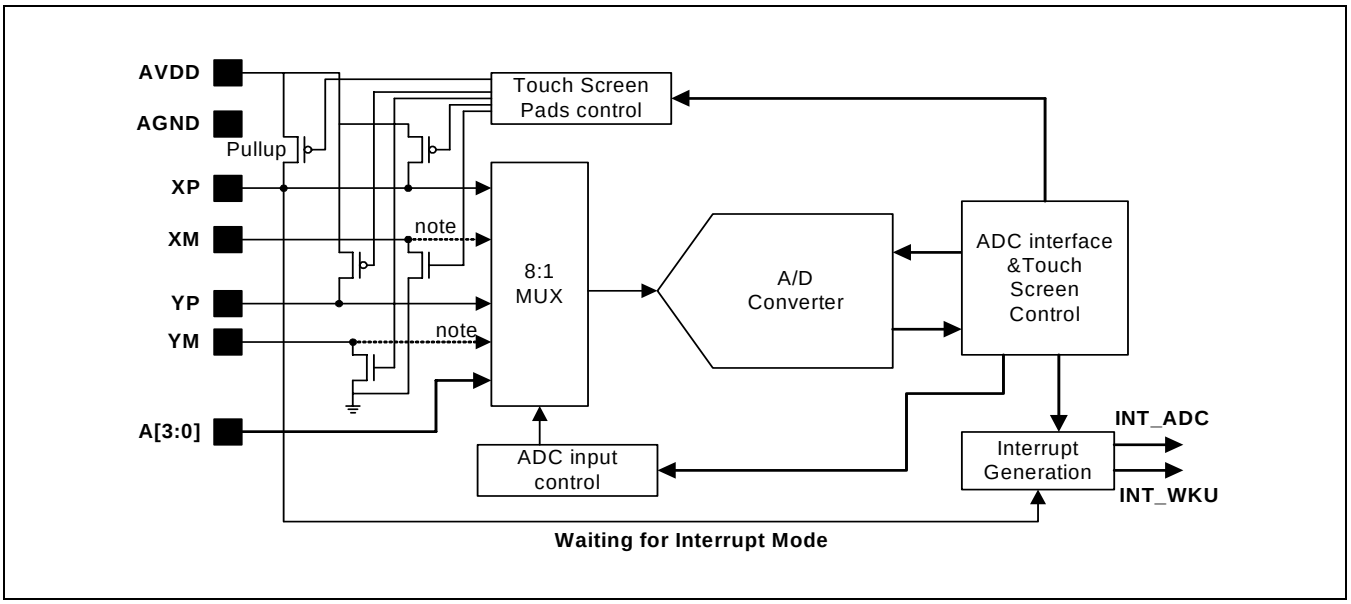


Figure 15-1. ADC and Touch Screen Interface Functional Block Diagram

*__NOTE__ (symbol ·····>)
When Touch Screen device is used; XM or PM is only connected ground for Touch Screen I/F.
When Touch Screen device is not used, XM or PM is connecting Analog Input Signal for Normal ADC conversion.

FUNCTION DESCRIPTIONS

A/D Conversion Time

When the PCLK frequency is 50 MHz and the prescaler value is 49, total 10-bit conversion time is given:

A/D converter freq. = 50 MHz/(49+1) = 1 MHz

Conversion time = 1/(1 MHz / 5cycles) = 1/200 kHz = 5 us

NOTE:

This A/D converter is designed to operate at maximum 2.5 MHz clock, so the conversion rate can go up to 500 KSPS.

Normal Conversion Mode

1. Normal Conversion Mode

   Normal Conversion Mode (AUTO_PST = 0, XY_PST = 0) is generally used for General Purpose ADC Conversion. This mode can be initialized by setting the ADCCON and ADCTSC and completed with a read the XPDATA (Normal ADC) value of ADCDAT0 (ADC Data Register 0).

Touch Screen Interface Mode

1. Separate X/Y Position Conversion Mode

   Separate X/Y Position Conversion Mode is consist of two Conversion Modes: X-Position Mode and Y-Position Mode.
   The first mode is operated in the following way:
   X-Position Mode (AUTO_PST = 0 and XY_PST = 1) writes X-position conversion data to XPDATA of ADCDAT0 register. After conversion, The Touch Screen Interface generates the Interrupt source (INT_ADC) to Interrupt Controller.
   Y-Position Mode (AUTO_PST = 0 and XY_PST = 2) writes Y-position conversion data to YPDATA of ADCDAT1. After the conversion, the Touch Screen Interface also generates the Interrupt source (INT_ADC) to Interrupt Controller.

Table 15-1. Condition of Touch Screen Panel Pads in Separate X/Y Position Conversion Mode

	XP	XM	YP	YM
X Position Conversion	External Voltage	GND	AIN[5]	Hi-Z
Y Position Conversion	AIN[7]	Hi-Z	External Voltage	GND

2. Auto (Sequential) X/Y Position Conversion Mode.

   Auto (Sequential) X/Y Position Conversion Mode (AUTO_PST = 1 and XY_PST = 0) is operated in the following way:
   The Touch Screen Controller automatically converts X-position and Y-position. The Touch Screen Controller writes X-measurement data to XPDATA of ADCDAT0, and then writes Y-measurement data to YPDATA of ADCDAT1. After Auto (Sequential) Position Conversion, The Touch Screen Controller generates Interrupt source (INT_ADC) to Interrupt Controller.

Table 15-2. Condition of Touch Screen Panel Pads in Auto (Sequential) X/Y Position Conversion Mode.

	XP	XM	YP	YM
X Position Conversion	External Voltage	GND	AIN[5]	Hi-Z
Y Position Conversion	AIN[7]	Hi-Z	External Voltage	GND

3. Waiting for Interrupt Mode.

   When Touch Screen Controller is in Waiting for Interrupt Mode, it waits for Stylus down. The controller generates Interrupt (INT_TC) signals when the Stylus is down on Touch Screen Panel.
   After an interrupt occurs, X and Y position can be read by the proper conversion mode (Separate X/Y position conversion Mode or Auto X/Y Position Conversion Mode).

Table 15-3. Condition of Touch Screen Panel Pads in Waiting for Interrupt Mode.

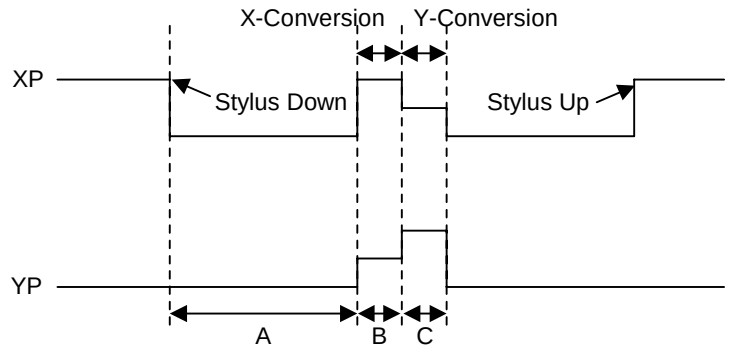
	XP	XM	YP	YM
Waiting for Interrupt Mode	Pull-up	Hi-Z	AIN[5]	GND

Standby Mode

Standby mode is activated when STDBM of ADCCON register is set to '1'. In this mode, A/D conversion operation is halted and XPDATA (Normal ADC) of ADCDAT0 and YPDATA of ADCDAT1 contain the previous converted data.

Programming Notes

1. The A/D converted data can be accessed by means of interrupt or polling method. With interrupt method, the overall conversion time - from A/D converter start to converted data read - may be delayed because of the return time of interrupt service routine and data access time. With polling method, by checking the ADCCON[15] - end of conversion flag-bit, the read time from ADCDAT register can be determined.
2. A/D conversion can be activated in different way: After ADCCON[1] - A/D conversion start-by-read mode-is set to 1, A/D conversion starts simultaneously whenever converted data is read.



A = **D** x (1/X-Tal Clock) or **A** = **D** x (1/External Clock)
B = **D** x (1/PCLK)
C = **D** x (1/PCLK)
D = DELAY value of ADCDLY Register

Figure 15-2. Timing Diagram in Auto (Sequential) X/Y Position Conversion Mode

ADC AND TOUCH SCREEN INTERFACE SPECIAL REGISTERS

ADC CONTROL (ADCCON) REGISTER

Register	Address	R/W	Description	Reset Value
ADCCON	0x58000000	R/W	ADC control register	0x3FC4

ADCCON	Bit	Description	Initial State
ECFLG	[15]	End of conversion flag (read only). 0 = A/D conversion in process 1 = End of A/D conversion	0
PRSCEN	[14]	A/D converter prescaler enable. 0 = Disable 1 = Enable	0
PRSCVL	[13:6]	A/D converter prescaler value. Data value: 1 ~ 255 Note that division factor is (N+1) when the prescaler value is N. **NOTE:** ADC frequency should be set less than PCLK by 5 times. (Ex. PCLK = 10MHz, ADC Frequency < 2MHz)	0xFF
SEL_MUX	[5:3]	Analog input channel select. 000 = AIN 0 001 = AIN 1 010 = AIN 2 011 = AIN 3 100 = AIN 4 101 = AIN 5 110 = AIN 6 111 = AIN 7 (XP)	0
STDBM	[2]	Standby mode select. 0 = Normal operation mode 1 = Standby mode	1
READ_ START	[1]	A/D conversion start by read. 0 = Disable start by read operation 1 = Enable start by read operation	0
ENABLE_ START	[0]	A/D conversion starts by setting this bit. If READ_START is enabled, this value is not valid. 0 = No operation 1 = A/D conversion starts and this bit is cleared after the start-up.	0

ADC TOUCH SCREEN CONTROL (ADCTSC) REGISTER

Register	Address	R/W	Description	Reset Value
ADCTSC	0x58000004	R/W	ADC touch screen control register	0x058

ADCTSC	Bit	Description	Initial State
UD_SEN	[8]	Detect Stylus Up or Down status. 0 = Detect Stylus Down Interrupt Signal. 1 = Detect Stylus Up Interrupt Signal.	0
YM_SEN	[7]	Select output value of YMON. 0 = YMON output is 0 (YM = Hi-Z). 1 = YMON output is 1 (YM = GND).	0
YP_SEN	[6]	Select output value of nYPON. 0 = nYPON output is 0 (YP = External voltage). 1 = nYPON output is 1 (YP is connected with AIN[5]).	1
XM_SEN	[5]	Select output value of XMON. 0 = XMON output is 0 (XM = Hi-Z). 1 = XMON output is 1 (XM = GND).	0
XP_SEN	[4]	Select output value of nXPON. 0 = nXPON output is 0 (XP = External voltage). 1 = nXPON output is 1 (XP is connected with AIN[7]).	1
PULL_UP	[3]	Pull-up switch enable. 0 = XP pull-up enable 1 = XP pull-up disable	1
AUTO_PST	[2]	Automatically sequencing conversion of X-position and Y-position 0 = Normal ADC conversion 1 = Auto (Sequential) X/Y Position Conversion Mode	0
XY_PST	[1:0]	Manual measurement of X-position or Y-position. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	0

NOTE: In Auto mode, ADCTSC register should be reconfigured before starting read operation.

ADC START DELAY (ADCDLY) REGISTER

Register	Address	R/W	Description	Reset Value
ADCDLY	0x58000008	R/W	ADC start or interval delay register	0x00ff

ADCDLY	Bit	Description	Initial State
DELAY	[15:0]	1) Normal Conversion Mode, Separate X/Y Position Conversion Mode, and Auto (Sequential) X/Y Position Conversion Mode. → X/Y Position Conversion Delay Value. 2) Waiting for Interrupt Mode. When Stylus down occurs in Waiting for Interrupt Mode, this register generates Interrupt signal (INT_TC) at intervals of several ms for Auto X/Y Position conversion. **NOTE:** Do not use Zero value (0x0000)	00ff

NOTES:

1. Before ADC conversion, Touch screen uses X-tal clock or EXTCLK (Waiting for Interrupt Mode).
2. During ADC conversion, PCLK is used.

ADC CONVERSION DATA (ADCDAT0) REGISTER

Register	Address	R/W	Description	Reset Value
ADCDAT0	0x5800000C	R	ADC conversion data register	-

ADCDAT0	Bit	Description	Initial State
UPDOWN	[15]	Up or down state of Stylus at Waiting for Interrupt Mode. 0 = Stylus down state 1 = Stylus up state	-
AUTO_PST	[14]	Automatic sequencing conversion of X-position and Y-position. 0 = Normal ADC conversion 1 = Sequencing measurement of X-position, Y-position	-
XY_PST	[13:12]	Manual measurement of X-position or Y-position. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	-
Reserved	[11:10]	Reserved	
XPDATA (Normal ADC)	[9:0]	X-position conversion data value. (include Normal ADC conversion data value) Data value: 0 ~ 3FF	-

ADC CONVERSION DATA (ADCDAT1) REGISTER

Register	Address	R/W	Description	Reset Value
ADCDAT1	0x58000010	R	ADC conversion data register	-

ADCDAT1	Bit	Description	Initial State
UPDOWN	[15]	Up or down state of Stylus at Waiting for Interrupt Mode. 0 = Stylus down state 1 = Stylus up state	-
AUTO_PST	[14]	Automatically sequencing conversion of X-position and Y-position. 0 = Normal ADC conversion 1 = Sequencing measurement of X-position, Y-position	-
XY_PST	[13:12]	Manual measurement of X-position or Y-position. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	-
Reserved	[11:10]	Reserved	
YPDATA	[9:0]	Y-position conversion data value Data value: 0 ~ 3FF	-

ADC TOUCH SCREEN UP-DOWN INT CHECK REGISTER (ADCUPDN)

Register	Address	R/W	Description	Reset Value
ADCUPDN	0x58000014	R/W	Stylus Up or Down Interrupt status register	0x0

ADCUPDN	Bit	Description	Initial State
TSC_UP	[1]	Stylus Up Interrupt. 0 = No stylus up status. 1 = Stylus up interrupt occurred.	0
TSC_DN	[0]	Stylus Down Interrupt. 0 = No stylus down status. 1 = Stylus down interrupt occurred.	0

16 REAL TIME CLOCK (RTC)

OVERVIEW

The Real Time Clock (RTC) unit can be operated by the backup battery while the system power is off. The RTC can transmit 8-bit data to CPU as Binary Coded Decimal (BCD) values using the STRB/LDRB ARM operation. The data include the time by second, minute, hour, date, day, month, and year. The RTC unit works with an external 32.768 kHz crystal and also can perform the alarm function.

FEATURES

- BCD number: second, minute, hour, date, day, month, and year
- Leap year generator
- Alarm function: alarms interrupt or wake-up from power-off mode
- Year 2000 problem is removed.
- Independent power pin (RTCVDD)
- Supports millisecond tick time interrupt for RTOS kernel time tick.

REAL TIME CLOCK OPERATION

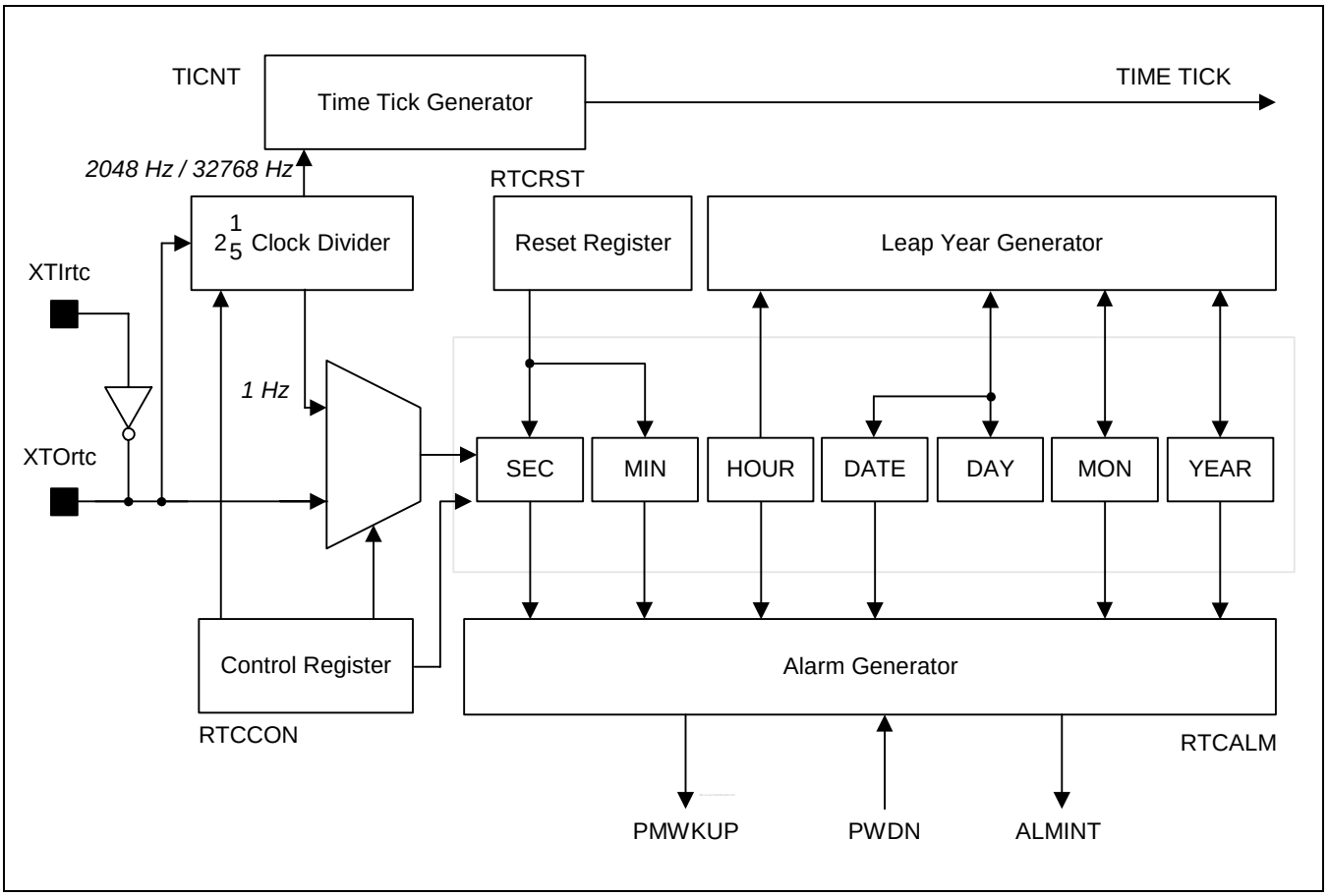


Figure 16-1. Real Time Clock Block Diagram

LEAP YEAR GENERATOR

The leap year generator can determine the last date of each month out of 28, 29, 30, or 31, based on data from BCDDATE, BCDMON, and BCDYEAR. This block considers leap year in deciding on the last date. An 8-bit counter can only represent 2 BCD digits, so it cannot decide whether "00" year (the year with its last two digits zeros) is a leap year or not. For example, it cannot discriminate between 1900 and 2000. To solve this problem, the RTC block in S3C2413X has hard-wired logic to support the leap year in 2000. Note 1900 is not leap year while 2000 is leap year. Therefore, two digits of 00 in S3C2413X denote 2000, not 1900.

READ/WRITE REGISTERS

Bit 0 of the RTCCON register must be set high in order to write the BCD register in RTC block. To display the second, minute, hour, date, month, and year, the CPU should read the data in BCDSEC, BCDMIN, BCDHOUR, BCDDAY, BCDDATE, BCDMON, and BCDYEAR registers, respectively, in the RTC block. However, a one second deviation may exist because multiple registers are read. For example, when the user reads the registers from BCDYEAR to BCDMIN, the result is assumed to be 2059 (Year), 12 (Month), 31 (Date), 23 (Hour) and 59 (Minute). When the user read the BCDSEC register and the value ranges from 1 to 59 (Second), there is no problem, but, if the value is 0 sec., the year, month, date, hour, and minute may be changed to 2060 (Year), 1 (Month), 1 (Date), 0 (Hour) and 0 (Minute) because of the one second deviation that was mentioned. In this case, the user should re-read from BCDYEAR to BCDSEC if BCDSEC is zero.

BACKUP BATTERY OPERATION

The RTC logic can be driven by the backup battery, which supplies the power through the RTCVDD pin into the RTC block, even if the system power is off. When the system is off, the interfaces of the CPU and RTC logic should be blocked, and the backup battery only drives the oscillation circuit and the BCD counters to minimize power dissipation.

ALARM FUNCTION

The RTC generates an alarm signal at a specified time in the power-off mode or normal operation mode. In normal operation mode, the alarm interrupt (ALMINT) is activated. In the power-off mode, the power management wakeup (PMWKUP) signal is activated as well as the ALMINT. The RTC alarm register (RTCALM) determines the alarm enable/disable status and the condition of the alarm time setting.

TICK TIME INTERRUPT

The RTC tick time is used for interrupt request. The TICNT register has an interrupt enable bit and the count value for the interrupt. The count value reaches '0' when the tick time interrupt occurs. Then the period of interrupt is as follows:

$$\text{Period} = \begin{cases} (n+1) / 2048 \text{ second} & \text{(when, TICsel : 0)} \\ (n+1) / 32768 \text{ second} & \text{(when, TICsel : 1)} \end{cases}$$

n: Tick time count value (1~32767)

NOTES:

1. Tick time resolution can be extended by selecting the appropriate tick time clock source.

   This RTC time tick may be used for real time operating system (RTOS) kernel time tick. If time tick is generated by the RTC time tick, the time related function of RTOS will always synchronized in real time.

ROUND RESET FUNCTION

The round reset function can be performed by the RTC round reset register (RTCRST). The round boundary (30, 40, or 50 sec.) of the second carry generation can be selected, and the second value is rounded to zero in the round reset. For example, when the current time is 23:37:47 and the round boundary is selected to 40 sec, the round reset changes the current time to 23:38:00.

32.768KHZ X-TAL CONNECTION EXAMPLE

The Figure 16-2 shows a circuit of the RTC unit oscillation at 32.768 kHz.

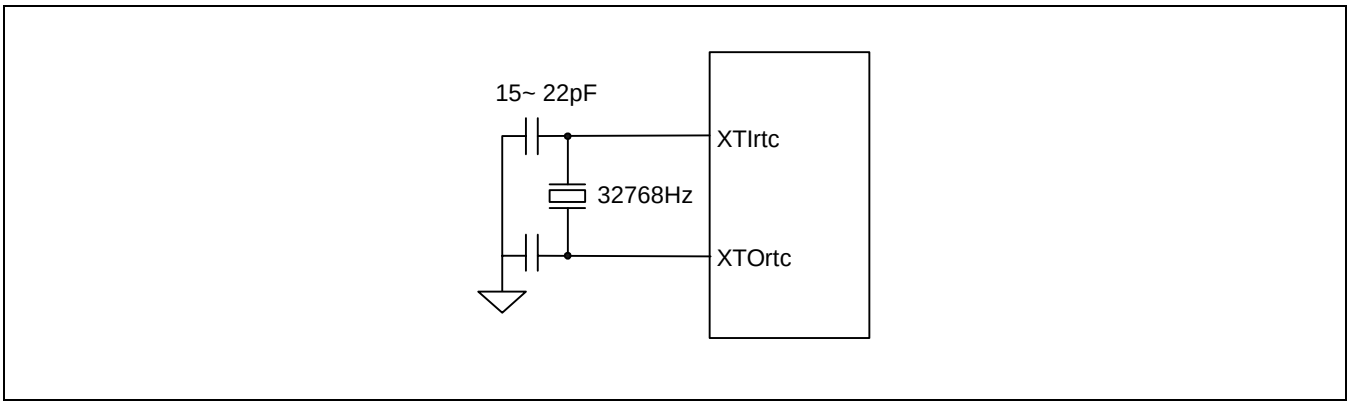


Figure 16-2. Main Oscillator Circuit Example

REAL TIME CLOCK SPECIAL REGISTERS

REAL TIME CLOCK CONTROL (RTCCON) REGISTER

The RTCCON register consists of 4 bits such as the RTCEN, which controls the read/write enable of the BCD registers, CLKSEL, CNTSEL, and CLKRST for testing.

RTCEN bit can control all interfaces between the CPU and the RTC, so it should be set to 1 in an RTC control routine to enable data read/write after a system reset. Also before power off, the RTCEN bit should be cleared to 0 to prevent inadvertent writing into RTC registers.

Register	Address	R/W	Description	Reset Value
RTCCON	0x57000040(L) 0x57000043(B)	R/W (by byte)	RTC control register	0x0

RTCCON	Bit	Description	Initial State
TICsel	[4]	Tick Time clock select. 0 = clock period of 1/2048 second 1 = clock period of 1/32768 second	0
CLKRST	[3]	RTC clock count reset. 0 = No reset, 1 = Reset	0
CNTSEL	[2]	BCD count select. 0 = Merge BCD counters 1 = Reserved (Separate BCD counters)	0
CLKSEL	[1]	BCD clock select. 0 = XTAL 1/215 divided clock 1 = Reserved (XTAL clock only for test)	0
RTCEN	[0]	RTC control enable. 0 = Disable 1 = Enable **NOTE:** Only BCD time count and read operation can be performed.	0

NOTES:

1. All RTC registers have to be accessed for each byte unit using STRB and LDRB instructions or char type pointer.
2. (L): Little endian.
   (B): Big endian.

TICK TIME COUNT (TICNT0) REGISTER 0

Register	Address	R/W	Description	Reset Value
TICNT0	0x57000044(L) 0x57000047(B)	R/W (by byte)	Tick time count register	0x0

TICNT	Bit	Description	Initial State
TICK INT ENABLE	[7]	Tick time interrupt enable. 0 = Disable 1 = Enable	0
TICK TIME COUNT 0	[6:0]	Upper 7bits of 15-bit tick time count value	000000

TICK TIME COUNT (TICNT1) REGISTER 1

Register	Address	R/W	Description	Reset Value
TICNT1	0x5700004C(L) 0x5700004F(B)	R/W (by byte)	Tick time count register 1	0x0

TICNT	Bit	Description	Initial State
TICK TIME COUNT 1	[7:0]	Lower 8 bits of 15bit tick time count value	000000

NOTES:

1. Tick time count value = (TICK TIME COUNT 0) x 2^8 + (TICK TIME COUNT 1)

RTC ALARM CONTROL (RTCALM) REGISTER

The RTCALM register determines the alarm enable and the alarm time. Note that the RTCALM register generates the alarm signal through both ALMINT and PMWKUP in power down mode, but only through ALMINT in the normal operation mode.

Register	Address	R/W	Description	Reset Value
RTCALM	0x57000050(L) 0x57000053(B)	R/W (by byte)	RTC alarm control register	0x0

RTCALM	Bit	Description	Initial State
XTBSEL	[7]	Clock divider clock select 0 = clock period of 1/128 second 1 = Reserved (test clock)	0
ALMEN	[6]	Alarm global enable. 0 = Disable, 1 = Enable	0
YEAREN	[5]	Year alarm enable. 0 = Disable, 1 = Enable	0
MONREN	[4]	Month alarm enable. 0 = Disable, 1 = Enable	0
DATEEN	[3]	Date alarm enable. 0 = Disable, 1 = Enable	0
HOUREN	[2]	Hour alarm enable. 0 = Disable, 1 = Enable	0
MINEN	[1]	Minute alarm enable. 0 = Disable, 1 = Enable	0
SECEN	[0]	Second alarm enable. 0 = Disable, 1 = Enable	0

ALARM SECOND DATA (ALMSEC) REGISTER

Register	Address	R/W	Description	Reset Value
ALMSEC	0x57000054(L) 0x57000057(B)	R/W (by byte)	Alarm second data register	0x0

ALMSEC	Bit	Description	Initial State
Reserved	[7]		0
SECDATA	[6:4]	BCD value for alarm second. 0 ~ 5	000
	[3:0]	0 ~ 9	0000

ALARM MIN DATA (ALMMIN) REGISTER

Register	Address	R/W	Description	Reset Value
ALMMIN	0x57000058(L) 0x5700005B(B)	R/W (by byte)	Alarm minute data register	0x00

ALMMIN	Bit	Description	Initial State
Reserved	[7]		0
MINDATA	[6:4]	BCD value for alarm minute. 0 ~ 5	000
	[3:0]	0 ~ 9	0000

ALARM HOUR DATA (ALMHOUR) REGISTER

Register	Address	R/W	Description	Reset Value
ALMHOUR	0x5700005C(L) 0x5700005F(B)	R/W (by byte)	Alarm hour data register	0x0

ALMHOUR	Bit	Description	Initial State
Reserved	[7:6]		00
HOURDATA	[5:4]	BCD value for alarm hour. 0 ~ 2	00
	[3:0]	0 ~ 9	0000

ALARM DATE DATA (ALMDATE) REGISTER

Register	Address	R/W	Description	Reset Value
ALMDATE	0x57000060(L) 0x57000063(B)	R/W (by byte)	Alarm date data register	0x01

ALMDAY	Bit	Description	Initial State
Reserved	[7:6]		00
DATEDATA	[5:4]	BCD value for alarm date, from 0 to 28, 29, 30, 31. 0 ~ 3	00
	[3:0]	0 ~ 9	0001

ALARM MON DATA (ALMMON) REGISTER

Register	Address	R/W	Description	Reset Value
ALMMON	0x57000064(L) 0x57000067(B)	R/W (by byte)	Alarm month data register	0x01

ALMMON	Bit	Description	Initial State
Reserved	[7:5]		00
MONDATA	[4]	BCD value for alarm month. 0 ~ 1	0
	[3:0]	0 ~ 9	0001

ALARM YEAR DATA (ALMYEAR) REGISTER

Register	Address	R/W	Description	Reset Value
ALMYEAR	0x57000068(L) 0x5700006B(B)	R/W (by byte)	Alarm year data register	0x0

ALMYEAR	Bit	Description	Initial State
YEARDATA	[7:0]	BCD value for year. 00 ~ 99	0x0

BCD SECOND (BCDSEC) REGISTER

Register	Address	R/W	Description	Reset Value
BCDSEC	0x57000070(L) 0x57000073(B)	R/W (by byte)	BCD second register	Undefined

BCDSEC	Bit	Description	Initial State
SECDATA	[6:4]	BCD value for second. 0 ~ 5	-
	[3:0]	0 ~ 9	-

BCD MINUTE (BCDMIN) REGISTER

Register	Address	R/W	Description	Reset Value
BCDMIN	0x57000074(L) 0x57000077(B)	R/W (by byte)	BCD minute register	Undefined

BCDMIN	Bit	Description	Initial State
MINDATA	[6:4]	BCD value for minute. 0 ~ 5	-
	[3:0]	0 ~ 9	-

BCD HOUR (BCDHOUR) REGISTER

Register	Address	R/W	Description	Reset Value
BCDHOUR	0x57000078(L) 0x5700007B(B)	R/W (by byte)	BCD hour register	Undefined

BCDHOUR	Bit	Description	Initial State
Reserved	[7:6]		-
HOURDATA	[5:4]	BCD value for hour. 0 ~ 2	-
	[3:0]	0 ~ 9	-

BCD DATE (BCDDATE) REGISTER

Register	Address	R/W	Description	Reset Value
BCDDATE	0x5700007C(L) 0x5700007F(B)	R/W (by byte)	BCD date register	Undefined

BCDDATE	Bit	Description	Initial State
Reserved	[7:6]		-
DATEDATA	[5:4]	BCD value for date. 0 ~ 3	-
	[3:0]	0 ~ 9	-

BCD DAY (BCDDAY) REGISTER

Register	Address	R/W	Description	Reset Value
BCDDAY	0x57000080(L) 0x57000083(B)	R/W (by byte)	BCD a day of the week register	Undefined

BCDDAY	Bit	Description	Initial State
Reserved	[7:3]		-
DAYDATA	[2:0]	BCD value for a day of the week. 1 ~ 7	-

BCD MONTH (BCDMON) REGISTER

Register	Address	R/W	Description	Reset Value
BCDMON	0x57000084(L) 0x57000087(B)	R/W (by byte)	BCD month register	Undefined

BCDMON	Bit	Description	Initial State
Reserved	[7:5]		-
MONDATA	[4]	BCD value for month. 0 ~ 1	-
	[3:0]	0 ~ 9	-

BCD YEAR (BCDYEAR) REGISTER

Register	Address	R/W	Description	Reset Value
BCDYEAR	0x57000088(L) 0x5700008B(B)	R/W (by byte)	BCD year register	Undefined

BCDYEAR	Bit	Description	Initial State
YEARDATA	[7:0]	BCD value for year. 00 ~ 99	-

17 WATCHDOG TIMER

OVERVIEW

The S3C2413X watchdog timer is used to resume the controller operation whenever it is disturbed by malfunctions such as noise and system errors. It can be used as a normal 16-bit interval timer to request interrupt service. The watchdog timer generates the reset signal for 128 PCLK cycles.

FEATURES

- Normal interval timer mode with interrupt request
- Internal reset signal is activated for 128 PCLK cycles when the timer count value reaches 0 (time-out).

WATCHDOG TIMER OPERATION

Figure 17-1 shows the functional block diagram of the watchdog timer. The watchdog timer uses only PCLK as its source clock. The PCLK frequency is prescaled to generate the corresponding watchdog timer clock, and the resulting frequency is divided again.

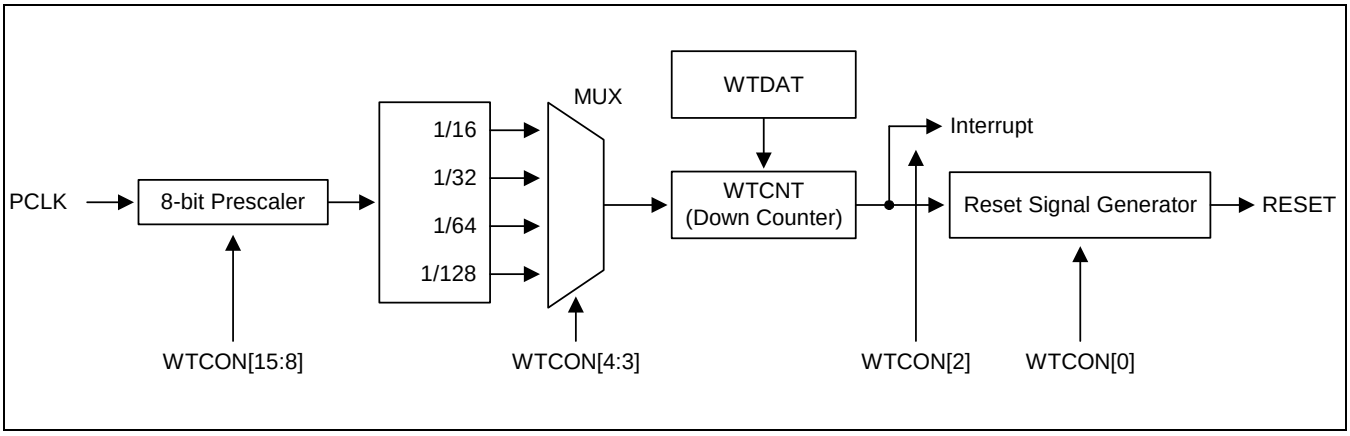


Figure 17-1. Watchdog Timer Block Diagram

The prescaler value and the frequency division factor are specified in the watchdog timer control (WTCON) register. Valid prescaler values range from 0 to 2^8-1. The frequency division factor can be selected as 16, 32, 64, or 128.

Use the following equation to calculate the watchdog timer clock frequency and the duration of each timer clock cycle:

t_watchdog = 1/(PCLK / (Prescaler value + 1) / Division_factor)

WTDAT & WTCNT

Once the watchdog timer is enabled, the value of watchdog timer data (WTDAT) register cannot be automatically reloaded into the timer counter (WTCNT). In this reason, an initial value must be written to the watchdog timer count (WTCNT) register, before the watchdog timer starts.

WATCHDOG TIMER SPECIAL REGISTERS

WATCHDOG TIMER CONTROL (WTCON) REGISTER

The WTCON register allows the user to enable/disable the watchdog timer, select the clock signal from 4 different sources, enable/disable interrupts, and enable/disable the watchdog timer output.
The Watchdog timer is used to resume the S3C2413X restart on mal-function after its power on; if controller restart is not desired, the Watchdog timer should be disabled.

If the user wants to use the normal timer provided by the Watchdog timer, enable the interrupt and disable the Watchdog timer.

Register	Address	R/W	Description	Reset Value
WTCON	0x53000000	R/W	Watchdog timer control register	0x8021

WTCON	Bit	Description	Initial State
Prescaler Value	[15:8]	Prescaler value. The valid range is from 0 to (2^8-1).	0x80
Reserved	[7:6]	Reserved. These two bits must be 00 in normal operation.	00
Watchdog Timer	[5]	Enable or disable bit of Watchdog timer. 0 = Disable 1 = Enable	1
Clock Select	[4:3]	Determine the clock division factor. 00: 16 01: 32 10: 64 11: 128	00
Interrupt Generation	[2]	Enable or disable bit of the interrupt. 0 = Disable 1 = Enable	0
Reserved	[1]	Reserved. This bit must be 0 in normal operation.	0
Reset Enable/Disable	[0]	Enable or disable bit of Watchdog timer output for reset signal. 1: Assert reset signal of the S3C2410A at watchdog time-out 0: Disable the reset function of the watchdog timer.	1

WATCHDOG TIMER DATA (WTDAT) REGISTER

The WTDAT register is used to specify the time-out duration. The content of WTDAT cannot be automatically loaded into the timer counter at initial watchdog timer operation. However, using 0x8000 (initial value) will drive the first time-out. In this case, the value of WTDAT will be automatically reloaded into WTCNT.

Register	Address	R/W	Description	Reset Value
WTDAT	0x53000004	R/W	Watchdog timer data register	0x8000

WTDAT	Bit	Description	Initial State
Count Reload Value	[15:0]	Watchdog timer count value for reload.	0x8000

WATCHDOG TIMER COUNT (WTCNT) REGISTER

The WTCNT register contains the current count values for the watchdog timer during normal operation. Note that the content of the WTDAT register cannot be automatically loaded into the timer count register when the watchdog timer is enabled initially, so the WTCNT register must be set to an initial value before enabling it.

Register	Address	R/W	Description	Reset Value
WTCNT	0x53000008	R/W	Watchdog timer count register	0x8000

WTCNT	Bit	Description	Initial State
Count Value	[15:0]	The current count value of the watchdog timer	0x8000

Errata Descriptions: **S3C2413X01 Watch-Dog/Software Reset Problem**

1. Summary

There are Watch-Dog Reset and Software Reset in S3C2413X01 which resets all parts of the device except alive-logic and clock divider. When Watch-Dog Timer expires and the reset function of the Watch-Dog Timer is enabled, the Watch-Dog Reset is issued. Otherwise, the Software Reset is issued by software command by writing the SWRSTCON (0x4C000030) register to "0x533C2412". Occasionally, the Watch-Dog or Software Reset may cause S3C2413X01 to hang-up due to glitch. The reason why Watch-Dog and Software Reset don't work properly is described in section 2. The available workaround is explained in section 3 and implementation example, specifically for Watch-Dog Reset problem, is also explained in section 4.

2. Watch-Dog and Software Reset Problem

The SYSCLK (system clock) is changed to EXTCLK from FOUT by force when the Watch-Dog or Software Reset is issued. At this moment, a glitch may be produced if the synchronization between FOUT and EXTCLK does not match as shown in figure 1. The glitch could be recognized as a clock by the following logic (which generates the ARMCLK, HCLK, PCLK and other clocks from SYSCLK) and the internal clock divider circuit may operate abnormally. As a consequence, the ARM core may not access the IP or Memory properly due to mismatch of the synchronization among ARMCLK, HCLK, PCLK and etc.

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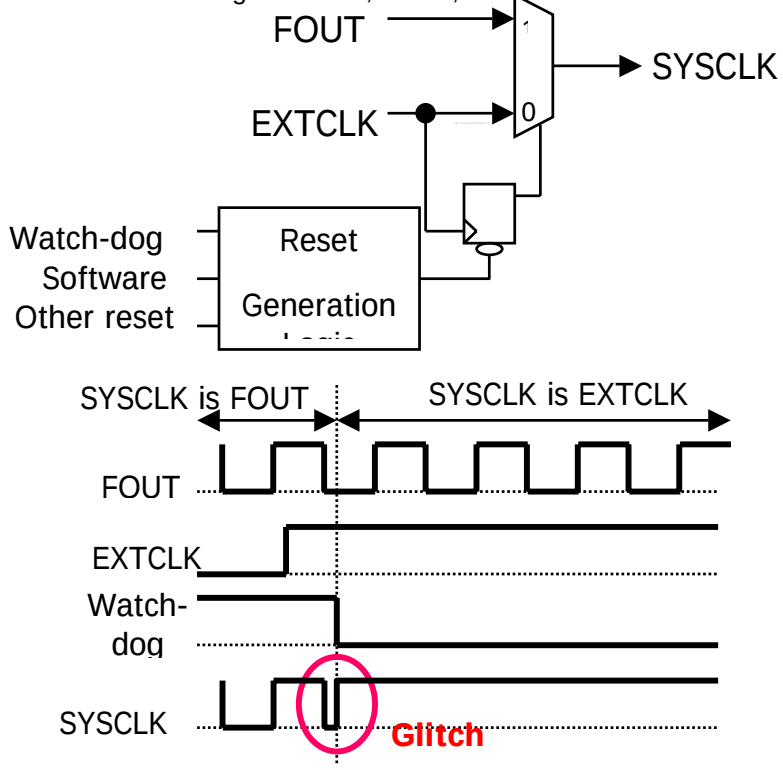


Figure 1 The diagram for root cause of Watch-Dog and Software Reset Problem.

3. The workaround Watch-Dog and Software Reset Problem

3.1 Watch-Dog Reset Workaround

We suggest an S/W workaround to avoid Watch-Dog Reset Problem with two transactions below.

a) Use software reset with timer interrupt.
Background:
One timer is used for implementing the workaround. The timer will invoke FIQ interrupt when the timer is expired. When the system is working properly, the timer should be on and off (stopped and restarted) periodically controlled by OS timer.
If system works abnormally, the timer will be expired. Then the FIQ interrupt mentioned above will be invoked by the timer interrupt. The same will happen when the system goes in hang-up state due to some unknown reason.
Remedy:
Change the SYSCLK to EXTCLK from FOUT in FIQ service routine. The glitch won't be produced when the SYSCLK is changed to EXTCLK from FOUT prior to Software Reset.
Then, issue **software reset after changing the system clock** in that routine. Finally, the system can be released from the software hung by the software reset.

If the hardware including bus system, system controller, and memory controller operates properly, this remedy will work properly.

b) In addition to adopting software reset, enable the Watch-Dog Reset.
The Watch-Dog Reset may not operate properly at all time due to the hardware problem, but the possibility of errors will be decreased when the both Software Reset with timer interrupt and the Watch-Dog Resets are used.

3.2 Software Reset Workaround

To avoid **Software Reset problem**, change the SYSCLK to EXTCLK from FOUT prior to S3C2413X to command Software Reset.

4. An implementation example for Watch-Dog Reset Workaround

Figure 2 depicts a simple flow chart of Watch-Dog Reset workaround. The vector tables including Reset, Undefined exception, SWI, Pre-fetch abort, Data abort, IRQ and FIQ exception are shown in the first region of entry point. Disabling the watch-dog, setting the clock, setting up IRQ and FIQ and etc. are executed in ResetHandler. The Workaround implementation in this example is to insert **Watch-Dog Reset Enable and Timer interrupt Enable** before OS (Operating System) is loaded.

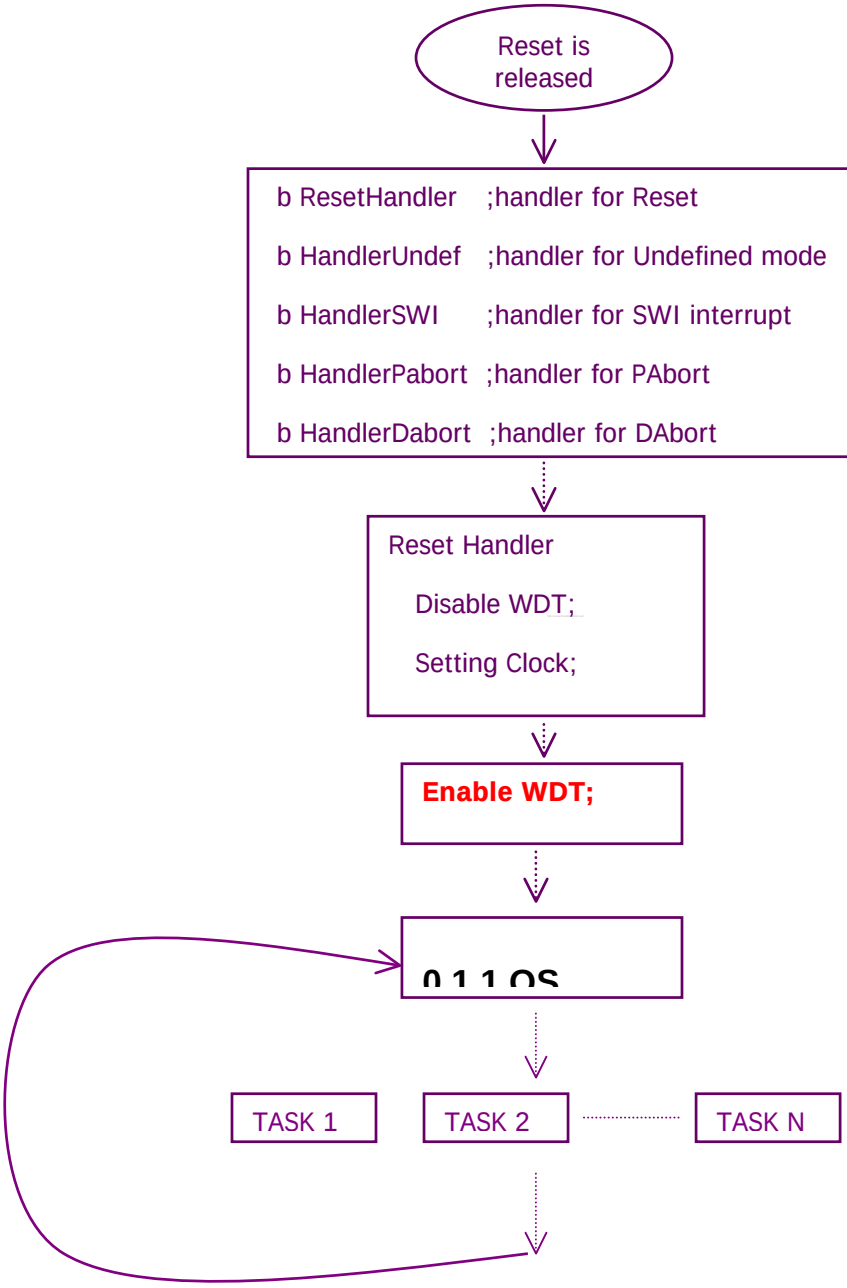


Figure 2 Simple flow chart

Timer4 is selected for this workaround example. An “InitFiq” in figure 3 is to set Timer4 interrupt to FIQ interrupt. The Timer4 interrupt will be considered to FIQ interrupt when the bit 14 of INTMOD (0x4A000004) register on Interrupt Controller is set to ‘1’.

```
InitFiq  PROC
; Setup Timer4 Interrupt to FIQ
        ldr r0, =INTMOD ; Set Interrupt Mode
```

Figure 3 An implementation of InitFiq

An “OS Timer” will operate tasks related with the operating system. In addition, it also should stop and restart the Timer4 and reload the Watch-Dog Timer as shown in figure 4.

```
OS Timer
; To do something
  Reload WDT
```

Figure 4 The implementation of OS Timer

If the system gets hung for some unknown reason, the timer4 will be expired. Then timer4 interrupt will be asserted. A “ServiceFiq” in figure 5 will be invoked because the timer4 interrupt is FIQ interrupt. The SYSCLK (system clock) is changed to EXTCLK from FOUT and software reset is issued in the FIQ service routine. Finally, the S3C2413X01 will be reset. The reason why FIQ is used for the timer4 interrupt, FIQ will not be blocked by any exception such as IRQ, Abort, Undefined, and SWI. We recommend that the FIQ service routine, “ServiceFiq” should reside in a NOR Flash to avoid SDRAM corruption.

```
ServiceFiq   PROC ; FIQ Service Routine
        ldr r0, =CLKSRC ; Change Clock
                        ;source to External Clock
        mov r1, #0x0
        str  r1, [r0]
        ldr  r0, =SWRSTCON ; Issue Software Reset
```

Figure 5 The implementation of ServiceFiq (FIQ Service Routine)

18 MMC/SD/SDIO CONTROLLER

FEATURES

- SD Memory Card Spec(ver 1.0) / MMC Spec(2.11) compatible
- SDIO Card Spec(Ver 1.0) compatible
- 16 words(64 bytes) FIFO for data Tx/Rx
- 40-bit Command Register
- 136-bit Response Register
- 8-bit Prescaler logic(Freq = System Clock / (P + 1))
- Normal, and DMA data transfer mode(byte, halfword, word transfer)
- DMA burst4 access support(only word transfer)
- 1-bit / 4-bit(wide bus) mode & block / stream mode switch support

BLOCK DIAGRAM

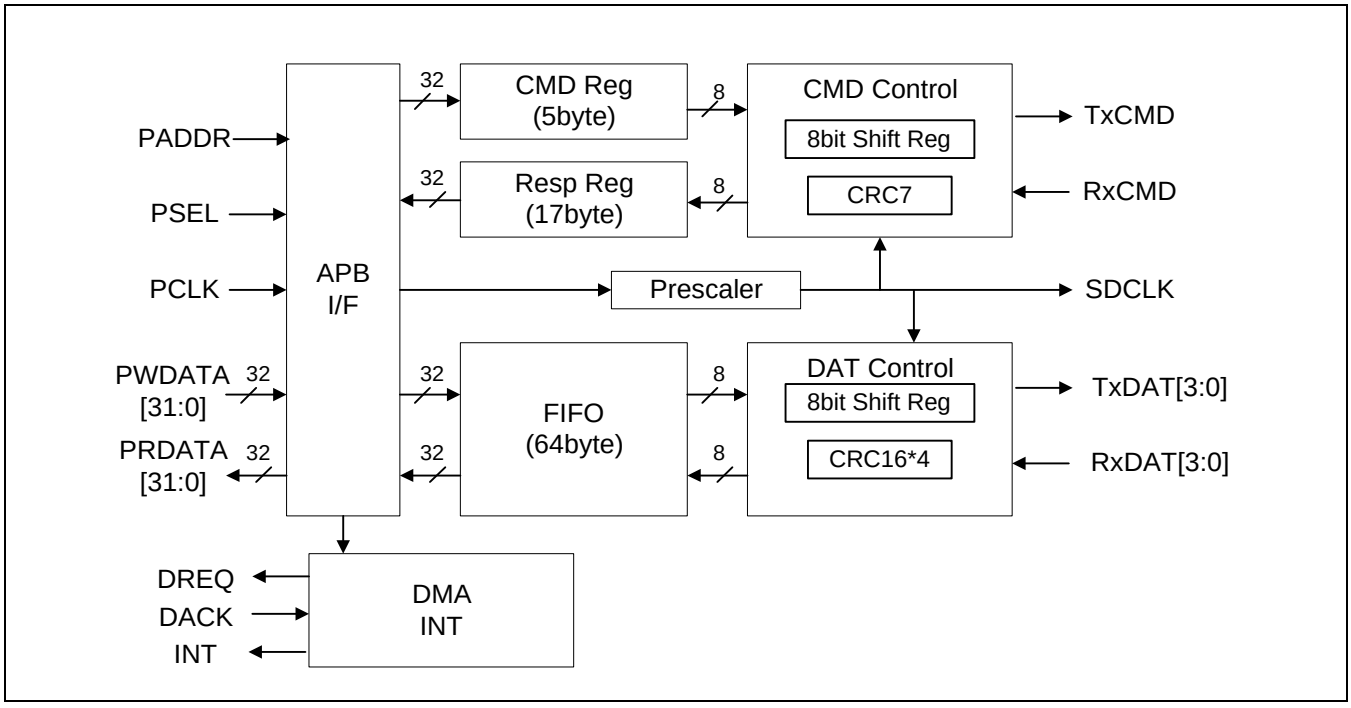


Figure 18-1 MMC/SD/SDIO Controller Block Diagram

SD OPERATION

A serial clock line synchronizes shifting and sampling of the information on the five data lines. The transmission frequency is controlled by making the appropriate bit settings to the SDIPRE register. You can modify its frequency to adjust the baud rate data register value.

Programming Procedure(common)

To program the SDI modules, follow these basic steps :

1. Set SDICON to configure properly with clock & interrupt enable
2. Set SDIPRE to configure with a proper value.
3. Wait 74 SDCLK clock cycle in order to initialize the card.

CMD Path Programming

1. Write command argument 32bit to SDICmdArg.
2. Determine command types and start command transmit with setting SDICmdCon.
3. Confirm the end of SDI CMD path operation when the specific flag of SDICmdSta is set
4. The flag is CmdSent if command type is no response.
5. The flag is RspFin if command type is with response.
6. Clear the corresponding flag of SDICmdSta through writing one with this bit

DAT Path Programming

1. Write data timeout period to SDIDTimer.
2. Write block size(block length) to SDIBSize(normally 0x80 word).
3. Determine the mode of block, wide bus, dma, etc and start data transfer with setting SDIDatCon.
4. Tx data → Write data to Data Register(SDIDAT) while Tx FIFO is available(TFDET is set), or half(TFHalf is set), or empty(TFEmpty is set).
5. Rx data → Read data from Data Register(SDIDAT) while Rx FIFO is available(RFDET is set), or full(RFFull is set), or half(RFHalf is set), or ready for last data(RFLast is set).
6. Confirm the end of SDI DAT path operation when DatFin flag of SDIDatSta is set
7. Clear the corresponding flag of SDIDatSta through writing one with this bit

SDIO OPERATION

There are two functions of SDIO operation : SDIO Interrupt receiving and Read Wait Request generation. These two function can operate when RcvIOInt bit and RwaitEn bit of SDICON register is activated respectively. And two functions have the steps and conditions like below.

SDIO Interrupt

In SD 1-bit mode, Interrupt is received through all range from RxDAT[1] pin.

In SD 4-bit mode, RxDAT[1] pin is shared between data receiving and interrupt receiving.
When interrupt detection range(Interrupt Period) is :

1. Single Block : the time between A and B
   - A : 2clocks after the completion of a data packet
   - B : The completion of sending the end bit of the next withdata command
2. Multi Block, PrdType = 0 : the time between A and B, restart at C
   - A : 2clocks after the completion of a data packet
   - B : 2clocks after A
   - C : 2clocks after the end bit of the abort command response
3. Multi Block, PrdType = 1 : the time between A and B, restart at A
   - A : 2clocks after the completion of a data packet
   - B : 2clocks after A
   - In case of last block, interrupt period begins at A, but not ends at B(CMD53 case)

Read Wait Request

Regardless of 1bit or 4bit mode, Read Wait Request signal transmits to TxDAT[2] pin in condition of below.

- In read multiple operation, request signal transmission begins at 2clocks after the end of the data block
- Transmission ends when user sets to one RwaitReq bit of SDIDatSta register

SDI SPECIAL REGISTERS

SDI Control Register(SDICON)

Register	Address	R/W	Description	Reset Value
SDICON	0x5A000000	R/W	SDI Control Register	0x0

SDICON	Bit	Description	Initial Value
Reserved	[31:9]		
SDMMC Reset (SDreset)	[8]	Reset whole sdmmc block. This bit is automatically clear. 0 = normal mode, 1 = SDMMC reset	0
Hold Margin (HoldMgn)	[7:6]	Determines how much you delay CMD, DAT lines for hold margin in MMC clock type 00 = 1/2 PCLK cycle, 01 = 1 PCLK cycle 10 = 3/2 PCLK cycles, 11 = 2 PCLK cycles	0
Clock Type (CTYP)	[5]	Determines which clock type is used as SDCLK. 0 = SD type, 1 = MMC type	0
Byte Order Type(ByteOrder)	[4]	Determines byte order type when you read(write) data from(to) sd host FIFO with word boundary. 0 = Type A, 1 = Type B	0
Receive SDIO Interrupt from card (RcvIOInt)	[3]	Determines whether sd host receives SDIO Interrupt from the card or not(for SDIO). 0 = ignore, 1 = receive SDIO Interrupt	0
Read Wait Enable(RWaitEn)	[2]	Determines read wait request signal generate when sd host waits the next block in multiple block read mode. This bit needs to delay the next block to be transmitted from the card(for SDIO). 0 = disable(no generate), 1 = Read wait enable(use SDIO)	0
Reserved	[1]		
Clock Out Enable (ENCLK)	[0]	Determines whether SDCLK Out enable or not 0 = disable(prescaler off), 1 = clock enable	0

* Byte Order Type

- Type A : (Access by Word) D[7:0] → D[15:8] → D[23:16] → D[31:24]
  (Access by Halfword) D[7:0] → D[15:8]
- Type B : (Access by Word) D[31:24] → D[23:16] → D[15:8] → D[7:0]
  (Access by Halfword) D[15:8] → D[7:0]

SDI Baud Rate Prescaler Register(SDIPRE)

Register	Address	R/W	Description	Reset Value
SDIPRE	0x5A000004	R/W	SDI Buad Rate Prescaler Register	0x01

SDIPRE	Bit	Description	Initial Value
Prescaler Value	[7:0]	Determines SDI clock(SDCLK) rate as above equation. Baud rate = PCLK / (Prescaler value + 1)	0x01

* Prescaler Value should be greater than zero.

SDI Command Argument Register(SDICmdArg)

Register	Address	R/W	Description	Reset Value
SDICmdArg	0x5A000008	R/W	SDI Command Argument Register	0x0

SDICmdArg	Bit	Description	Initial Value
CmdArg	[31:0]	Command Argument	0x00000000

SDI Command Control Register(SDICmdCon)

Register	Address	R/W	Description	Reset Value
SDICmdCon	0x5A00000C	R/W	SDI Command Control Register	0x0

SDICommand	Bit	Description	Initial Value
Reserved	[31:13]		
Abort Command (AbortCmd)	[12]	Determines whether command type is for abort(for SDIO). 0 = normal command, 1 = abort command(CMD12, CMD52)	0
Command with Data (WithData)	[11]	Determines whether command type is with data(for SDIO). 0 = without data, 1 = with data	0
LongRsp	[10]	Determines whether host receives a 136-bit long response or not 0 = short response, 1 = long response	0
WaitRsp	[9]	Determines whether host waits for a response or not 0 = no response, 1 = wait response	0
Command Start(CMST)	[8]	Determines whether command operation starts or not. . This bit is automatically clear 0 = command ready, 1 = command start	0
CmdIndex	[7:0]	Command index with start 2bit(8bit)	0x00

SDI Command Status Register(SDICmdSta)

Register	Address	R/W	Description	Reset Value
SDICmdSta	0x5A000010	R/(C)	SDI Command Status Register	0x0

SDICmdSta	Bit	Description	Initial Value
Reserved	[31:13]		
Response CRC Fail(RspCrc)	[12] R/C	CRC check failed when command response received. This flag is cleared by setting to one this bit. 0 = not detect, 1 = crc fail	0
Command Sent (CmdSent)	[11] R/C	Command sent(not concerned with response). This flag is cleared by setting to one this bit. 0 = not detect, 1 = command end	0
Command Time Out (CmdTout)	[10] R/C	Command response timeout(64clk). This flag is cleared by setting to one this bit. 0 = not detect, 1 = timeout	0
Response Receive End (RspFin)	[9] R/C	Command response received. This flag is cleared by setting to one this bit. 0 = not detect, 1 = response end	0
CMD line progress On (CmdOn)	[8]	Command transfer in progress 0 = not detect, 1 = in progress	0
RspIndex	[7:0]	Response index 6bit with start 2bit(8bit)	0x00

SDI Response Register 0(SDIRSP0)

Register	Address	R/W	Description	Reset Value
SDIRSP0	0x5A000014	R	SDI Response Register 0	0x0

SDIRSP0	Bit	Description	Initial Value
Response0	[31:0]	Card status[31:0](short), card status[127:96](long)	0x00000000

SDI Response Register 1(SDIRSP1)

Register	Address	R/W	Description	Reset Value
SDIRSP1	0x5A000018	R	SDI Response Register 1	0x0

SDIRSP1	Bit	Description	Initial Value
RCRC7	[31:24]	CRC7(with end bit, short), card status[95:88](long)	0x00
Response1	[23:0]	unused(short), card status[87:64](long)	0x000000

SDI Response Register 2(SDIRSP2)

Register	Address	R/W	Description	Reset Value
SDIRSP2	0x5A00001C	R	SDI Response Register 2	0x0

SDIRSP2	Bit	Description	Initial Value
Response2	[31:0]	unused(short), card status[63:32](long)	0x00000000

SDI Response Register 3(SDIRSP3)

Register	Address	R/W	Description	Reset Value
SDIRSP3	0x5A000020	R	SDI Response Register 3	0x0

SDIRSP3	Bit	Description	Initial Value
Response3	[31:0]	unused(short), card status[31:0](long)	0x00000000

SDI Data / Busy Timer Register(SDIDTimer)

Register	Address	R/W	Description	Reset Value
SDIDTimer	0x5A000024	R/W	SDI Data / Busy Timer Register	0x0

SDIDTimer	Bit	Description	Initial Value
Reserved	[31:23]		
DataTimer	[22:0]	Data / Busy timeout period	0x10000

SDI Block Size Register(SDIBSize)

Register	Address	R/W	Description	Reset Value
SDIBSize	0x5A000028	R/W	SDI Block Size Register	0x0

SDIBSize	Bit	Description	Initial Value
Reserved	[31:12]		
BlkSize	[11:0]	Block Size value(0~4095 byte) , don't care when stream mode	0x000

* In Case of multi block, BlkSize must be aligned to word(4byte) size.(BlkSize[1:0] = 00)

SDI Data Control Register(SDIDatCon)

Register	Address	R/W	Description	Reset Value
SDIDatCon	0x5A00002C	R/W	SDI Data control Register	0x0

SDIDatCon	Bit	Description	Initial Value
Reserved	[31:25]		
Burst4 enable (Burst4)	[24]	Enable Burst4 mode in DMA mode. This bit should be set only when Data Size is word. 0 = disable, 1 = Burst4 enable	0
Data Size (DataSize)	[23:22]	Indicates the size of the transfer with FIFO, which is typically byte, halfword or word. 00 = Byte transfer, 01 = Halfword transfer 10 = Word transfer, 11 = reserved	0
SDIO Interrupt Period Type (PrdType)	[21]	Determines whether SDIO Interrupt period is 2 cycle or extend more cycle when last data block is transferred(for SDIO). 0 = exactly 2 cycle, 1 = more cycle(likely single block)	0
Transmit After Response (TARSP)	[20]	Determines when data transmit start after response receive or not 0 = directly after DatMode set, 1 = after response receive(assume DatMode sets to 2'b11)	0
Receive After Command (RACMD)	[19]	Determines when data receive start after command sent or not 0 = directly after DatMode set, 1 = after command sent (assume DatMode sets to 2'b10)	0
Busy After Command (BACMD)	[18]	Determines when busy receive start after command sent or not 0 = directly after DatMode set, 1 = after command sent (assume DatMode sets to 2'b01)	0
Block mode (BlkMode)	[17]	Data transfer mode 0 = stream data transfer, 1 = block data transfer	0
Wide bus enable (WideBus)	[16]	Determines enable wide bus mode 0 = standard bus mode(only SDIDAT[0] used), 1 = wide bus mode(SDIDAT[3:0] used)	0
DMA Enable (EnDMA)	[15]	Enable DMA 0 = disable(polling), 1 = dma enable	0
Data Transfer Start(DTST)	[14]	Determines whether data transfer start or not. . This bit is auto-matically clear 0 = data ready, 1 = data start	0
Data Transfer Mode (DatMode)	[13:12]	Determines which direction of data transfer 00 = no operation, 01 = only busy check start 10 = data receive start, 11 = data transmit start	00
BlkNum	[11:0]	Block Number(0~4095), don't care when stream mode	0x000

* If you want one of TARSP, RACMD, BACMD bits(SDIDatCon[20:18]) to "1", you need to write on SDIDatCon register ahead of on SDICmdCon register.(always need for SDIO)

SDI Data Remain Counter Register(SDIDatCnt)

Register	Address	R/W	Description	Reset Value
SDIDatCnt	0x5A000030	R	SDI Data Remain Counter Register	0x0

SDIDatCnt	Bit	Description	Initial Value
Reserved	[31:24]		
BlkNumCnt	[23:12]	Remaining Block number	0x000
BlkCnt	[11:0]	Remaining data byte of 1 block	0x000

SDI Data Status Register(SDIDatSta)

Register	Address	R/W	Description	Reset Value
SDIDatSta	0x5A000034	R/(C)	SDI Data Status Register	0x0

SDIDatSta	Bit	Description	Initial Value
Reserved	[31:12]		
No Busy(NoBusy)	[11] R/C	Busy is not active during 16cycle after cmd packet transmitted in only busy check mode. This flag is cleared by setting to 1 this bit. 0 = not detect, 1 = no busy signal	0
Read Wait Request Occur (RWaitReq)	[10] R/C	Read wait request signal transmits to sd card. The request signal is stopped and this flag is cleared by setting to one this bit. 0 = not occur, 1 = Read wait request occur	0
SDIO Interrupt Detect(IOIntDet)	[9] R/C	SDIO interrupt detect. This flag is cleared by setting to one this bit. 0 = not detect, 1 = SDIO interrupt detect	0
Reserved	[8]		
CRC Status Fail(CrcSta)	[7] R/C	CRC Status error when data block sent(CRC check failed). This flag is cleared by setting to one this bit. 0 = not detect, 1 = crc status fail	0
Data Receive CRC Fail(DatCrc)	[6] R/C	Data block received error(CRC check failed). This flag is cleared by setting to one this bit. 0 = not detect, 1 = receive crc fail	0
Data Time Out(DatTout)	[5] R/C	Data / Busy receive timeout. This flag is cleared by setting to one this bit. 0 = not detect, 1 = timeout	0
Data Transfer Finish(DatFin)	[4] R/C	Data transfer completes(data counter is zero). This flag is cleared by setting to one this bit. 0 = not detect, 1 = data finish detect	0
Busy Finish (BusyFin)	[3] R/C	Only busy check finish. This flag is cleared by setting to one this bit 0 = not detect, 1 = busy finish detect	0
Reserved	[2]		0
Tx Data progress On(TxDatOn)	[1]	Data transmit in progress 0 = not active, 1 = data Tx in progress	0
Rx Data Progress On(RxDatOn)	[0]	Data receive in progress 0 = not active, 1 = data Rx in progress	0

SDI FIFO Status Register(SDIFSTA)

Register	Address	R/W	Description	Reset Value
SDIFSTA	0x5A000038	R/(C)	SDI FIFO Status Register	0x0

SDIFSTA	Bit	Description	Initial State
Reserved	[31:16]		
FIFO Reset(FRST)	[16] C	Reset FIFO value. This bit is automatically clear. 0 = normal mode, 1 = FIFO reset	0
FIFO Fail error (FFfail)	[15:14] R/C	FIFO fail error when FIFO occurs overrun / underrun data saving. This flag is cleared by setting to one these bits. 00 = not detect, 01 = FIFO fail 10 = FIFO fail in the last transfer(only FIFO reset need) 11 = reserved	0
FIFO available Detect for Tx (TFDET)	[13]	This bit indicates that FIFO data is available for transmit when DatMode is data transmit mode. If DMA mode is enable, sd host requests DMA operation. 0 = not detect(FIFO full), 1 = detect(0 ≤ FIFO ≤ 63)	0
FIFO available Detect for Rx (RFDET)	[12]	This bit indicates that FIFO data is available for receive when DatMode is data receive mode. If DMA mode is enable, sd host requests DMA operation. 0 = not detect(FIFO empty), 1 = detect(1 ≤ FIFO ≤ 64)	0
Tx FIFO Half Full (TFHalf)	[11]	This bit sets to 1 whenever Tx FIFO is less than 33byte. 0 = 33 ≤ Tx FIFO ≤ 64, 1 = 0 ≤ Tx FIFO ≤ 32	0
Tx FIFO Empty (TFEmpty)	[10]	This bit sets to 1 whenever Tx FIFO is empty. 0 = 1 ≤ Tx FIFO ≤ 64, 1 = Empty(0byte)	0
Rx FIFO Last Data Ready (RFLast)	[9] R/C	This bit sets to 1 when Rx FIFO occurs to behave last data of all block. This flag is cleared by setting to one this bit. 0 = not received yet, 1 = Rx FIFO gets Last data	0
Rx FIFO Full (RFFull)	[8]	This bit sets to 1 whenever Rx FIFO is full. 0 = 0 ≤ Rx FIFO ≤ 63, 1 = Full(64byte)	0
Rx FIFO Half Full (RFHalf)	[7]	This bit sets to 1 whenever Rx FIFO is more than 31byte. 0 = 0 ≤ Rx FIFO ≤ 31, 1 = 32 ≤ Rx FIFO ≤ 64	0
FIFO Count (FFCNT)	[6:0]	Number of data(byte) in FIFO	0000000

* Although the last Rx data size is lager than remained count of FIFO data, you could read this data. If this event happens, you should clear FFfail field, and FIFO reset field

SDI Interrupt Mask Register(SDIIntMsk)

Register	Address	R/W	Description	Reset Value
SDIIntMsk	0x5A00003C	R/W	SDI Interrupt Mask Register	0x0

SDICON	Bit	Description	Initial Value
Reserved	[31:19]		
NoBusy Interrupt Enable (NoBusyInt)	[18]	Determines SDI generate an interrupt if busy signal is not active 0 = disable, 1 = interrupt enable	0
RspCrc Interrupt Enable (RspCrcInt)	[17]	Determines SDI generate an interrupt if response CRC check fails 0 = disable, 1 = interrupt enable	0
CmdSent Interrupt Enable (CmdSentInt)	[16]	Determines SDI generate an interrupt if command sent(no response required) 0 = disable, 1 = interrupt enable	0
CmdTout Interrupt Enable (CmdToutInt)	[15]	Determines SDI generate an interrupt if command response timeout occurs 0 = disable, 1 = interrupt enable	0
RspEnd Interrupt Enable (RspEndInt)	[14]	Determines SDI generate an interrupt if command response received 0 = disable, 1 = interrupt enable	0
RWaitReq Interrupt Enable (RWReqInt)	[13]	Determines SDI generate an interrupt if read wait request occur. 0 = disable, 1 = interrupt enable	0
IOIntDet Interrupt Enable (IntDetInt)	[12]	Determines SDI generate an interrupt if sd host receives SDIO Interrupt from the card(for SDIO). 0 = disable, 1 = interrupt enable	0
FFfail Interrupt Enable (FFfailInt)	[11]	Determines SDI generate an interrupt if FIFO fail error occurs 0 = disable, 1 = interrupt enable	0
CrcSta Interrupt Enable (CrcStaInt)	[10]	Determines SDI generate an interrupt if CRC status error occurs 0 = disable, 1 = interrupt enable	0
DatCrc Interrupt Enable (DatCrcInt)	[9]	Determines SDI generate an interrupt if data receive CRC failed 0 = disable, 1 = interrupt enable	0
DatTout Interrupt Enable (DatToutInt)	[8]	Determines SDI generate an interrupt if data receive timeout occurs 0 = disable, 1 = interrupt enable	0

SDICON	Bit	Description	Initial Value
DatFin Interrupt Enable (DatFinInt)	[7]	Determines SDI generate an interrupt if data counter is zero 0 = disable, 1 = interrupt enable	0
BusyFin Interrupt Enable(BusyFinInt)	[6]	Determines SDI generate an interrupt if only busy check completes 0 = disable, 1 = interrupt enable	0
Reserved	[5]		0
TFHalf Interrupt Enable (TFHalfInt)	[4]	Determines SDI generate an interrupt if Tx FIFO fills half 0 = disable, 1 = interrupt enable	0
TFEmpty Interrupt Enable(TFEmptInt)	[3]	Determines SDI generate an interrupt if Tx FIFO is empty 0 = disable, 1 = interrupt enable	0
RFLast Interrupt Enable (RFLastInt)	[2]	Determines SDI generate an interrupt if Rx FIFO has last data 0 = disable, 1 = interrupt enable	0
RFFull Interrupt Enable (RFFullInt)	[1]	Determines SDI generate an interrupt if Rx FIFO fills full 0 = disable, 1 = interrupt enable	0
RFHalf Interrupt Enable (RFHalfInt)	[0]	Determines SDI generate an interrupt if Rx FIFO fills half 0 = disable, 1 = interrupt enable	0

SDI Data Register(SDIDAT)

Register	Address	R/W	Description	Reset Value
SDIDAT	0x5A000040(Li/W, Li/HW, Li/B, Bi/W) 0x5A000041(Bi/HW), 0x5A000043(Bi/B)	R/W	SDI Data Register	0x0

SDIDAT	Bit	Description	Initial State
Data Register	[31:0]	This field contains the data to be transmitted or received over the SDI channel	0x00000000

* (Li/W, Li/HW, Li/B) : Access by Word/HalfWord//Byte unit when endian mode is Little

* (Bi/W) : Access by Word unit when endian mode is Big

* (Bi/HW) : Access by HalfWord unit when endian mode is Big

* (Bi/B) : Access by Byte unit when endian mode is Big

19 IIC-BUS INTERFACE

OVERVIEW

The S3C2413X RISC microprocessor can support a multi-master IIC-bus serial interface. A dedicated serial data line (SDA) and a serial clock line (SCL) carry information between bus masters and peripheral devices which are connected to the IIC-bus. The SDA and SCL lines are bi-directional.

In multi-master IIC-bus mode, multiple S3C2413X RISC microprocessors can receive or transmit serial data to or from slave devices. The master S3C2413X can initiate and terminate a data transfer over the IIC-bus. The IIC-bus in the S3C2413X uses Standard bus arbitration procedure.

To control multi-master IIC-bus operations, values must be written to the following registers:

- Multi-master IIC-bus control register, IICCON
- Multi-master IIC-bus control/status register, IICSTAT
- Multi-master IIC-bus Tx/Rx data shift register, IICDS
- Multi-master IIC-bus address register, IICADD

When the IIC-bus is free, the SDA and SCL lines should be both at High level. A High-to-Low transition of SDA can initiate a Start condition. A Low-to-High transition of SDA can initiate a Stop condition while SCL remains steady at High Level.

The Start and Stop conditions can always be generated by the master devices. A 7-bit address value in the first data byte, which is put onto the bus after the Start condition has been initiated, can determine the slave device which the bus master device has selected. The 8th bit determines the direction of the transfer (read or write).

Every data byte put onto the SDA line should be eight bits in total. The bytes can be unlimitedly sent or received during the bus transfer operation. Data is always sent from most-significant bit (MSB) first, and every byte should be immediately followed by an acknowledge (ACK) bit.

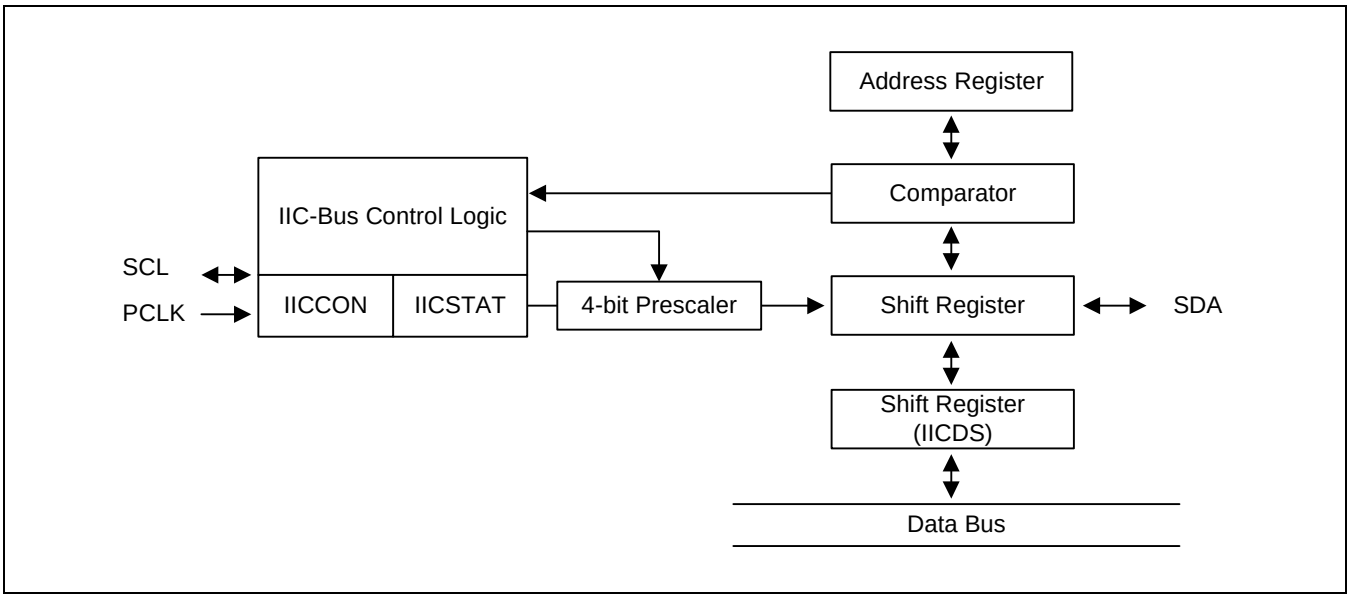


Figure 19-1. IIC-Bus Block Diagram

NOTE: IIC DATA HOLD TIME

The IIC data hold time(tSDAH) is minimum 0ns.
(IIC data hold time is minimum 0ns for standard/fast bus mode in IIC specification v2.1.)
Please check the data hold time of your IIC device if it's 0 nS or not.
The IIC controller supports only IIC bus device(standard/fast bus mode), not C bus device.

IIC-BUS INTERFACE

The S3C2413X IIC-bus interface has four operation modes:

- Master transmitter mode
- Master receive mode
- Slave transmitter mode
- Slave receive mode

Functional relationships among these operating modes are described below.

START AND STOP CONDITIONS

When the IIC-bus interface is inactive, it is usually in Slave mode. In other words, the interface should be in Slave mode before detecting a Start condition on the SDA line (a Start condition can be initiated with a High-to-Low transition of the SDA line while the clock signal of SCL is High). When the interface state is changed to Master mode, a data transfer on the SDA line can be initiated and SCL signal generated.

A Start condition can transfer a one-byte serial data over the SDA line, and a Stop condition can terminate the data transfer. A Stop condition is a Low-to-High transition of the SDA line while SCL is High. Start and Stop conditions are always generated by the master. The IIC-bus gets busy when a Start condition is generated. A Stop condition will make the IIC-bus free.

When a master initiates a Start condition, it should send a slave address to notify the slave device. One byte of address field consists of a 7-bit address and a 1-bit transfer direction indicator (showing write or read).
If bit 8 is 0, it indicates a write operation (transmit operation); if bit 8 is 1, it indicates a request for data read (receive operation).

The master will finish the transfer operation by transmitting a Stop condition. If the master wants to continue the data transmission to the bus, it should generate another Start condition as well as a slave address. In this way, the read-write operation can be performed in various formats.

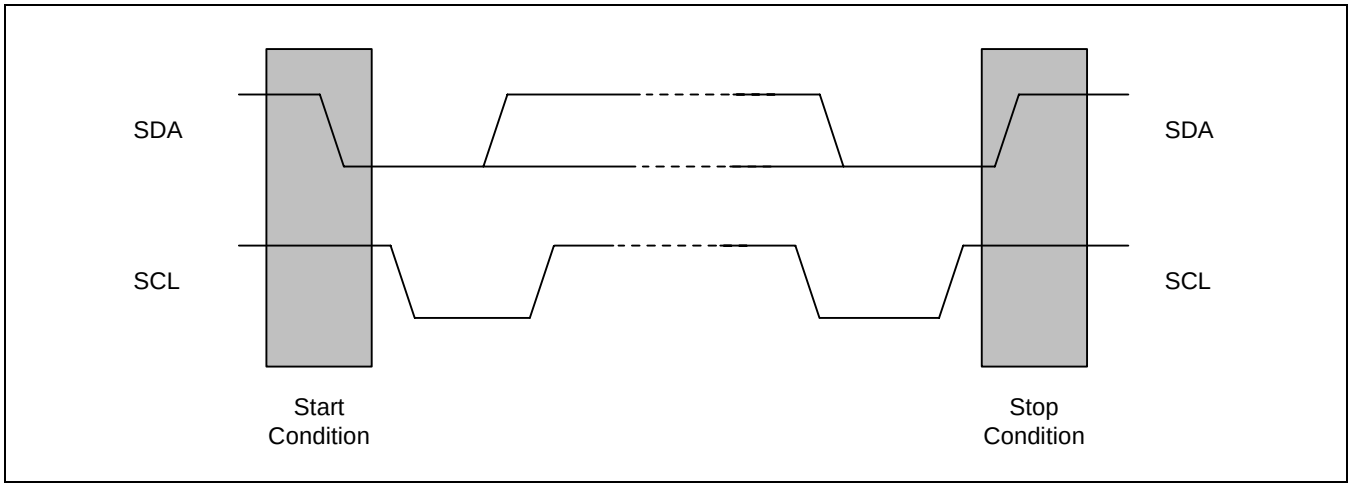


Figure 19-2. Start and Stop Condition

DATA TRANSFER FORMAT

Every byte placed on the SDA line should be eight bits in length. The bytes can be unlimitedly transmitted per transfer. The first byte following a Start condition should have the address field. The address field can be transmitted by the master when the IIC-bus is operating in Master mode. Each byte should be followed by an acknowledgement (ACK) bit. The MSB bit of the serial data and addresses are always sent first.

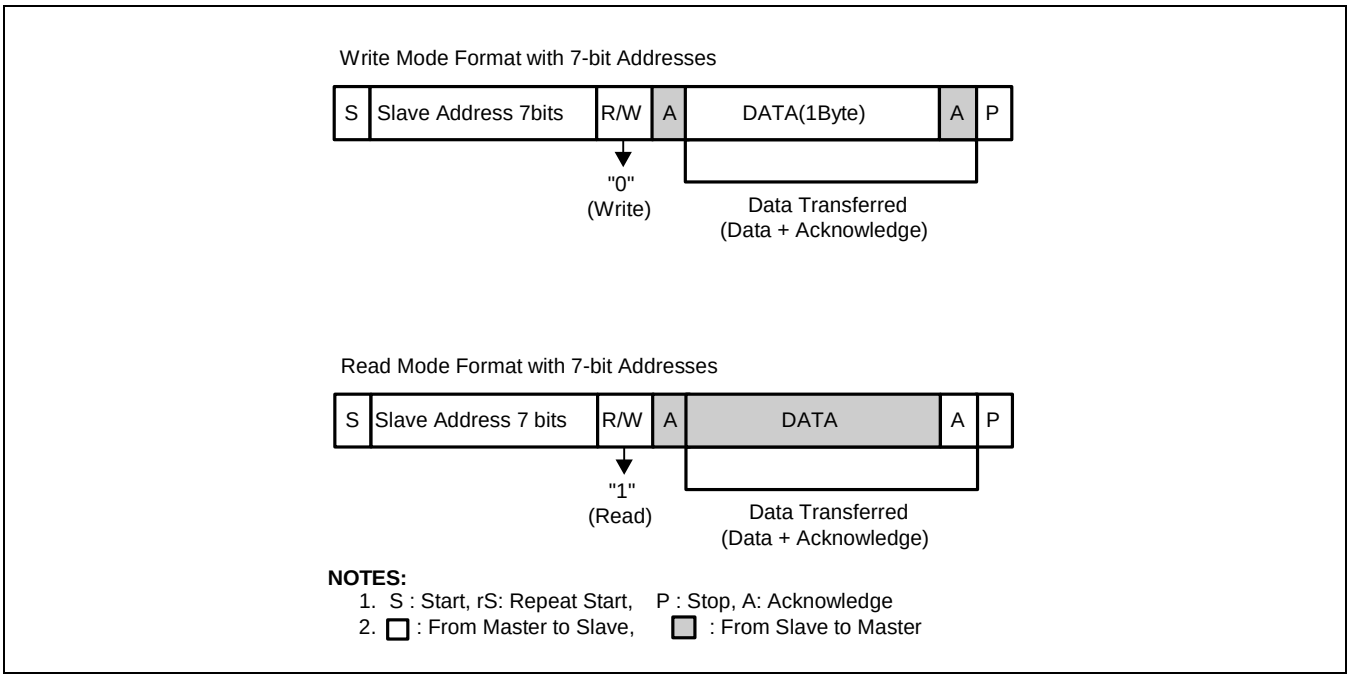


Figure 19-3. IIC-Bus Interface Data Format

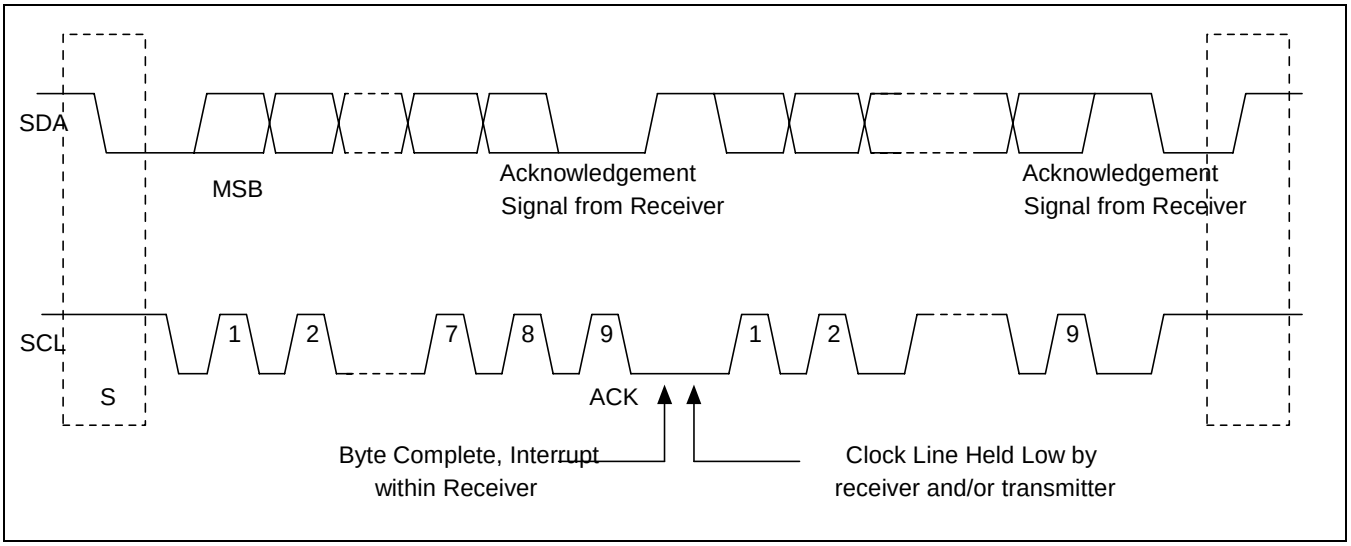


Figure 19-4. Data Transfer on the IIC-Bus

ACK SIGNAL TRANSMISSION

To complete a one-byte transfer operation, the receiver should send an ACK bit to the transmitter. The ACK pulse should occur at the ninth clock of the SCL line. Eight clocks are required for the one-byte data transfer. The master should generate the clock pulse required to transmit the ACK bit.

The transmitter should release the SDA line by making the SDA line High when the ACK clock pulse is received. The receiver should also drive the SDA line Low during the ACK clock pulse so that the SDA keeps Low during the High period of the ninth SCL pulse.

The ACK bit transmit function can be enabled or disabled by software (IICSTAT). However, the ACK pulse on the ninth clock of SCL is required to complete the one-byte data transfer operation.

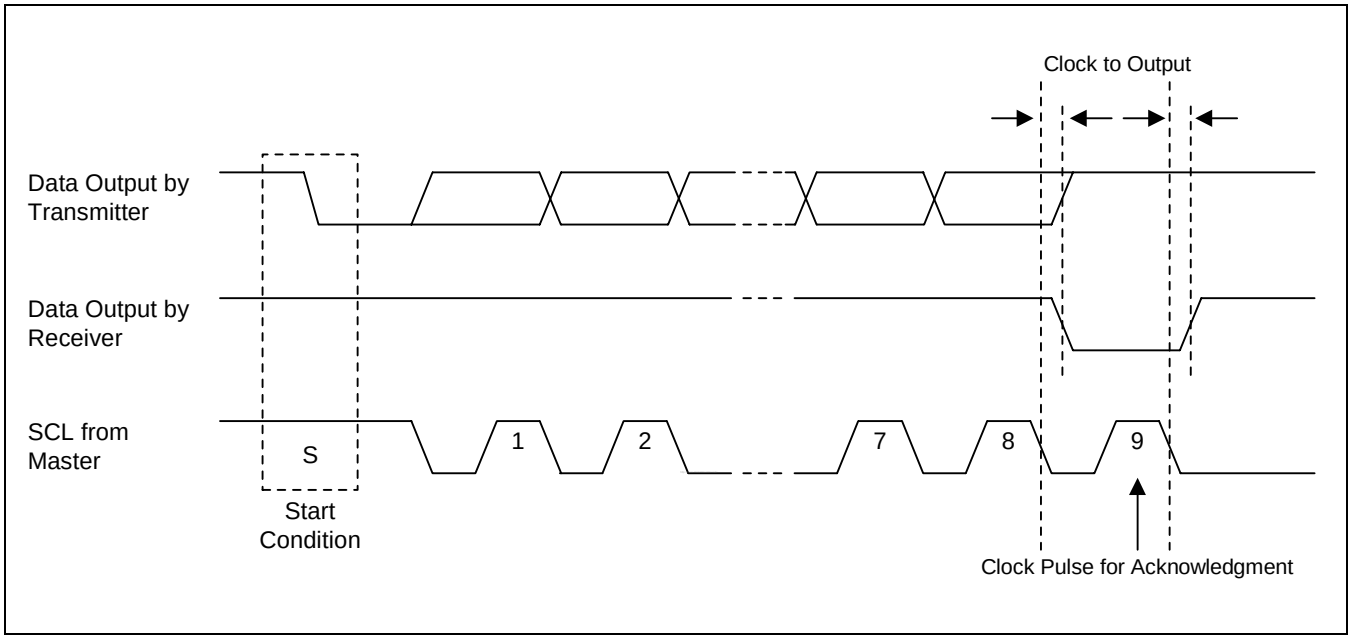


Figure 19-5. Acknowledge on the IIC-Bus

READ-WRITE OPERATION

In Transmitter mode, when the data is transferred, the IIC-bus interface will wait until IIC-bus Data Shift (IICDS) register receives a new data. Before the new data is written into the register, the SCL line will be held low, and then released after it is written. The S3C2413X should hold the interrupt to identify the completion of current data transfer. After the CPU receives the interrupt request, it should write a new data into the IICDS register, again.

In Receive mode, when a data is received, the IIC-bus interface will wait until IICDS register is read. Before the new data is read out, the SCL line will be held low and then released after it is read. The S3C2413X should hold the interrupt to identify the completion of the new data reception. After the CPU receives the interrupt request, it should read the data from the IICDS register.

BUS ARBITRATION PROCEDURES

Arbitration takes place on the SDA line to prevent the contention on the bus between two masters. If a master with a SDA High level detects the other master with a SDA active Low level, it will not initiate a data transfer because the current level on the bus does not correspond to its own. The arbitration procedure will be extended until the SDA line turns High.

However, when the masters simultaneously lower the SDA line, each master should evaluate whether or not the mastership is allocated to itself. For the purpose of evaluation, each master should detect the address bits. While each master generates the slaver address, it should also detect the address bit on the SDA line because the SDA line is likely to get Low rather than to keep High. Assume that one master generates a Low as first address bit, while the other master is maintaining High. In this case, both masters will detect Low on the bus because the Low status is superior to the High status in power. When this happens, Low (as the first bit of address) generating master will get the mastership while High (as the first bit of address) generating master should withdraw the mastership. If both masters generate Low as the first bit of address, there should be an arbitration for the second address bit, again. This arbitration will continue to the end of last address bit.

ABORT CONDITIONS

If a slave receiver cannot acknowledge the confirmation of the slave address, it should hold the level of the SDA line High. In this case, the master should generate a Stop condition and to abort the transfer.

If a master receiver is involved in the aborted transfer, it should signal the end of the slave transmit operation by canceling the generation of an ACK after the last data byte received from the slave. The slave transmitter should then release the SDA to allow a master to generate a Stop condition.

CONFIGURING IIC-BUS

To control the frequency of the serial clock (SCL), the 4-bit prescaler value can be programmed in the IICCON register. The IIC-bus interface address is stored in the IIC-bus address (IICADD) register. (By default, the IIC-bus interface address has an unknown value.)

FLOWCHARTS OF OPERATIONS IN EACH MODE

The following steps must be executed before any IIC Tx/Rx operations.

1) Write own slave address on IICADD register, if needed.
2) Set IICCON register.
   a) Enable interrupt
   b) Define SCL period
3) Set IICSTAT to enable Serial Output

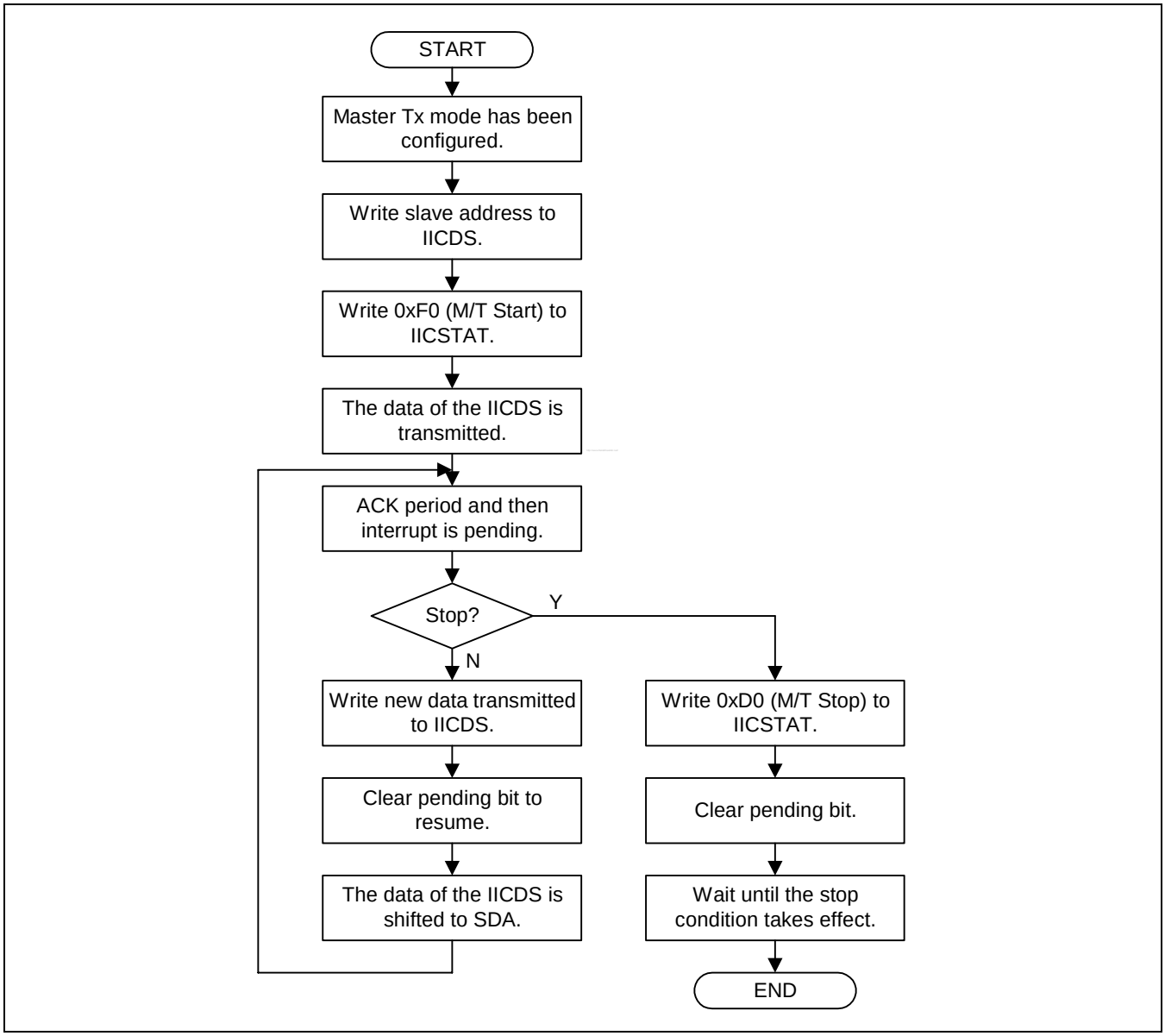


Figure 19-6. Operations for Master/Transmitter Mode

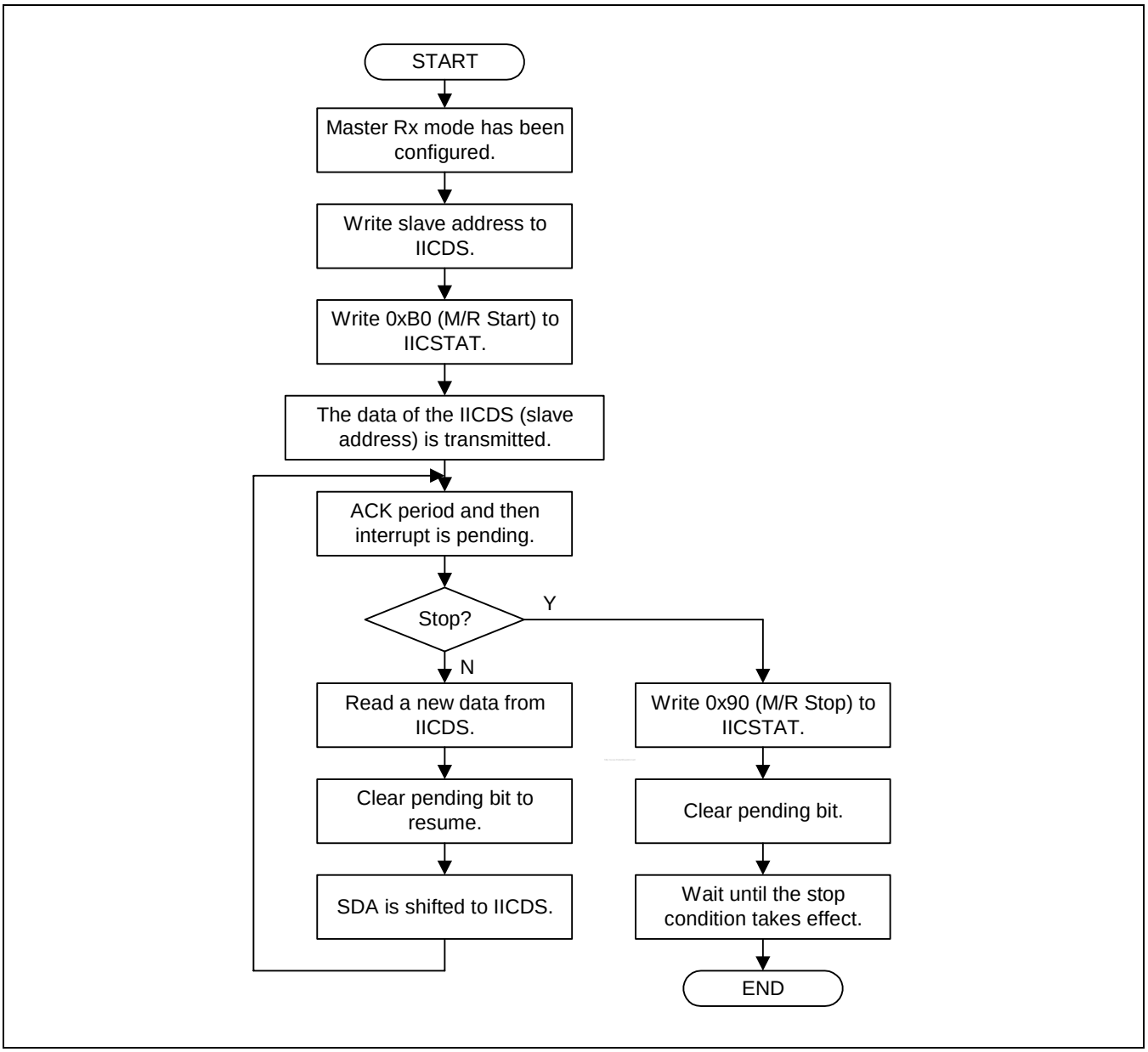


Figure 19-7. Operations for Master/Receiver Mode

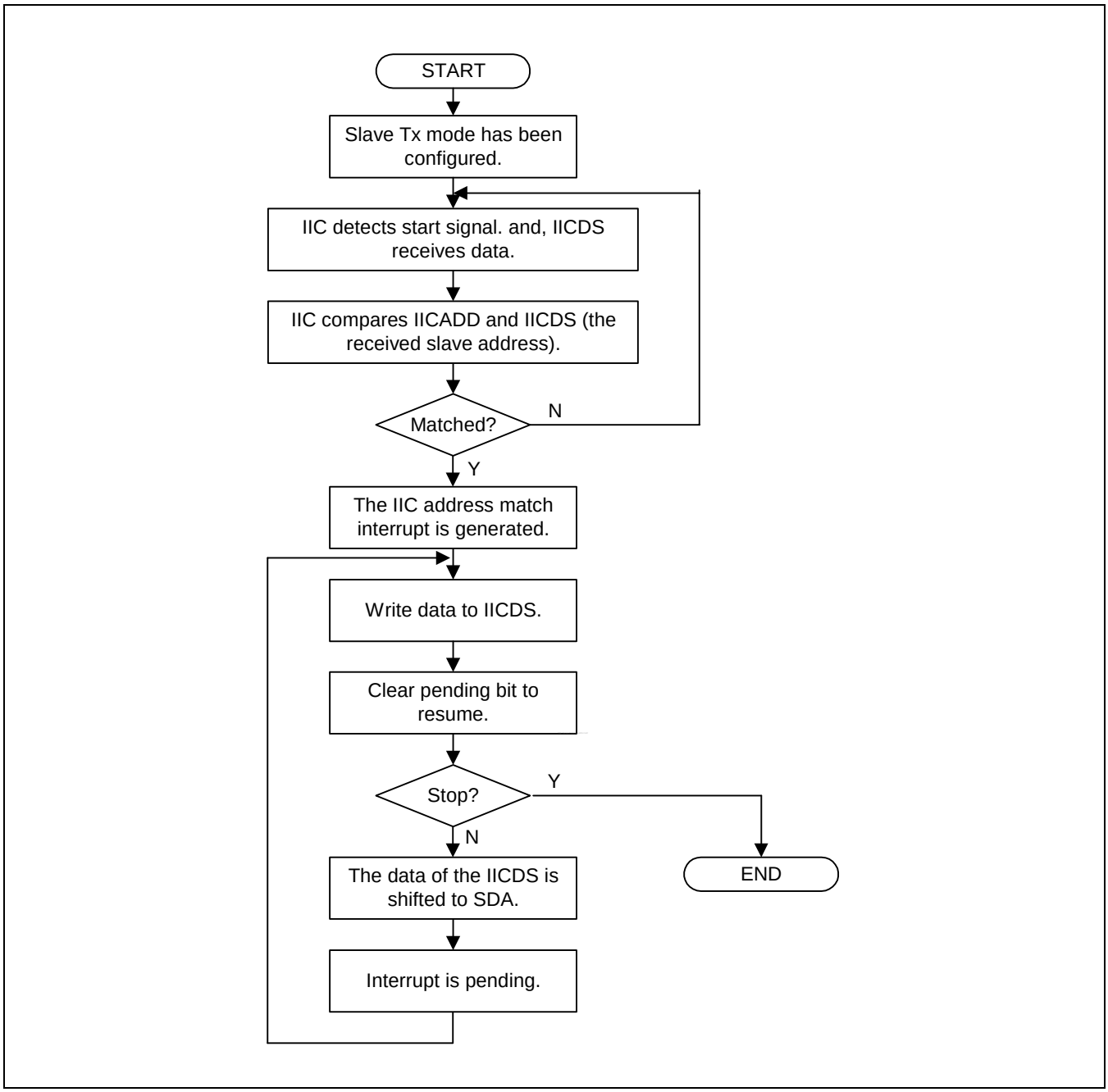


Figure 19-8. Operations for Slave/Transmitter Mode

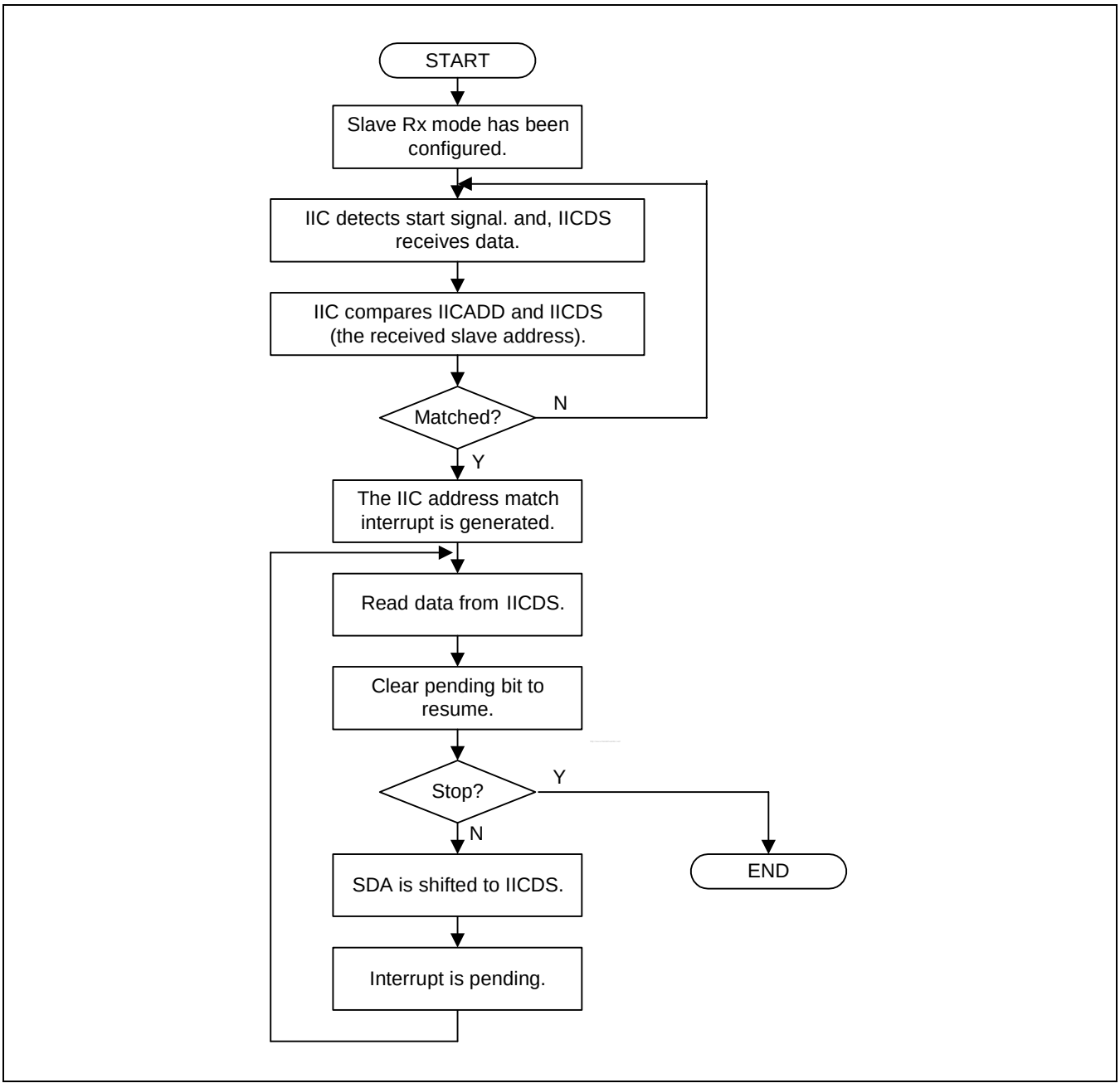


Figure 19-9. Operations for Slave/Receiver Mode

IIC-BUS INTERFACE SPECIAL REGISTERS

MULTI-MASTER IIC-BUS CONTROL (IICCON) REGISTER

Register	Address	R/W	Description	Reset Value
IICCON	0x54000000	R/W	IIC-Bus control register	0x0X

IICCON	Bit	Description	Initial State
Acknowledge generation (note 1)	[7]	IIC-bus acknowledge enable bit. 0 = Disable, 1 = Enable In Tx mode, the IICSDA is free in the ack time. In Rx mode, the IICSDA is L in the ack time.	0
Tx clock source selection	[6]	Source clock of IIC-bus transmit clock prescaler selection bit. 0 = IICCLK = fPCLK /16 1 = IICCLK = fPCLK /512	0
Tx/Rx Interrupt (note 5)	[5]	IIC-Bus Tx/Rx interrupt enable/disable bit. 0 = Disable, 1 = Enable	0
Interrupt pending flag (note 2), (note 3)	[4]	IIC-bus Tx/Rx interrupt pending flag. This bit cannot be written to 1. When this bit is read as 1, the IICSCL is tied to L and the IIC is stopped. To resume the operation, clear this bit as 0. 0 = 1) No interrupt pending (when read). 2) Clear pending condition & Resume the operation (when write). 1 = 1) Interrupt is pending (when read) 2) N/A (when write)	0
Transmit clock value (note 4)	[3:0]	IIC-Bus transmit clock prescaler. IIC-Bus transmit clock frequency is determined by this 4-bit prescaler value, according to the following formula: Tx clock = IICCLK/(IICCON[3:0]+1).	Undefined

NOTES:

1. Interfacing with EEPROM, the ack generation may be disabled before reading the last data in order to generate the STOP condition in Rx mode.
2. An IIC-bus interrupt occurs 1) when a 1-byte transmit or receive operation is completed, 2) when a general call or a slave address match occurs, or 3) if bus arbitration fails.
3. To adjust the setup time of IICSDA before IISSCL rising edge, IICDS has to be written before clearing the IIC interrupt pending bit.
4. IICCLK is determined by IICCON[6].
   Tx clock can vary by SCL transition time.
   When IICCON[6]=0, IICCON[3:0]=0x0 or 0x1 is not available.
5. If the IICON[5]=0, IICON[4] does not operate correctly.
   So, It is recommended that you should set IICCON[5]=1, although you does not use the IIC interrupt.

MULTI-MASTER IIC-BUS CONTROL/STATUS (IICSTAT) REGISTER

Register	Address	R/W	Description	Reset Value
IICSTAT	0x54000004	R/W	IIC-Bus control/status register	0x0

IICSTAT	Bit	Description	Initial State
Mode selection	[7:6]	IIC-bus master/slave Tx/Rx mode select bits. 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode	00
Busy signal status / START STOP condition	[5]	IIC-Bus busy signal status bit. 0 = read) Not busy (when read) write) STOP signal generation 1 = read) Busy (when read) write) START signal generation. The data in IICDS will be transferred automatically just after the start signal.	0
Serial output	[4]	IIC-bus data output enable/disable bit. 0 = Disable Rx/Tx, 1 = Enable Rx/Tx	0
Arbitration status flag	[3]	IIC-bus arbitration procedure status flag bit. 0 = Bus arbitration successful 1 = Bus arbitration failed during serial I/O	0
Address-as-slave status flag	[2]	IIC-bus address-as-slave status flag bit. 0 = Cleared when START/STOP condition was detected 1 = Received slave address matches the address value in the IICADD	0
Address zero status flag	[1]	IIC-bus address zero status flag bit. 0 = Cleared when START/STOP condition was detected. 1 = Received slave address is 00000000b.	0
Last-received bit status flag	[0]	IIC-bus last-received bit status flag bit. 0 = Last-received bit is 0 (ACK was received). 1 = Last-received bit is 1 (ACK was not received).	0

MULTI-MASTER IIC-BUS ADDRESS (IICADD) REGISTER

Register	Address	R/W	Description	Reset Value
IICADD	0x54000008	R/W	IIC-Bus address register	0xXX

IICADD	Bit	Description	Initial State
Slave address	[7:0]	7-bit slave address, latched from the IIC-bus. When serial output enable = 0 in the IICSTAT, IICADD is write-enabled. The IICADD value can be read any time, regardless of the current serial output enable bit (IICSTAT) setting. Slave address = [7:1] Not mapped = [0]	XXXXXXXX

MULTI-MASTER IIC-BUS TRANSMIT/RECEIVE DATA SHIFT (IICDS) REGISTER

Register	Address	R/W	Description	Reset Value
IICDS	0x5400000C	R/W	IIC-Bus transmit/receive data shift register	0xXX

IICDS	Bit	Description	Initial State
Data shift	[7:0]	8-bit data shift register for IIC-bus Tx/Rx operation. When serial output enable = 1 in the IICSTAT, IICDS is write-enabled. The IICDS value can be read any time, regardless of the current serial output enable bit (IICSTAT) setting.	XXXXXXXX

MULTI-MASTER IIC-BUS LINE CONTROL(IICLC) REGISTER

Register	Address	R/W	Description	Reset Value
IICLC	0x54000010	R/W	IIC-Bus multi-master line control register	0x00

IICLC	Bit	Description	Initial State
Filter enable	[2]	IIC-bus filter enable bit. When SDA port is operating as input, this bit should be High. This filter can prevent from occurred error by a glitch during double of PCLK time. 0: Filter disable 1: Filter enable	0
SDA output delay	[1:0]	IIC-Bus SDA line delay length selection bits. SDA line is delayed as following clock time(PCLK) 00: 0 clocks 01: 5 clocks 10: 10 clocks 11: 15 clocks	00

NOTES

20 IIS-BUS INTERFACE

OVERVIEW

IIS (Inter-IC Sound) interface transmits or receives sound data from or to external stereo audio codec. For transmit and receive data, two 32x16 FIFOs (First-In-First-Out) data structures are included and DMA transfer mode for transmitting or receiving samples can be supported. IIS-specific clock can be supplied from internal system clock controller through IIS clock divider or direct clock source.

BLOCK DIAGRAM

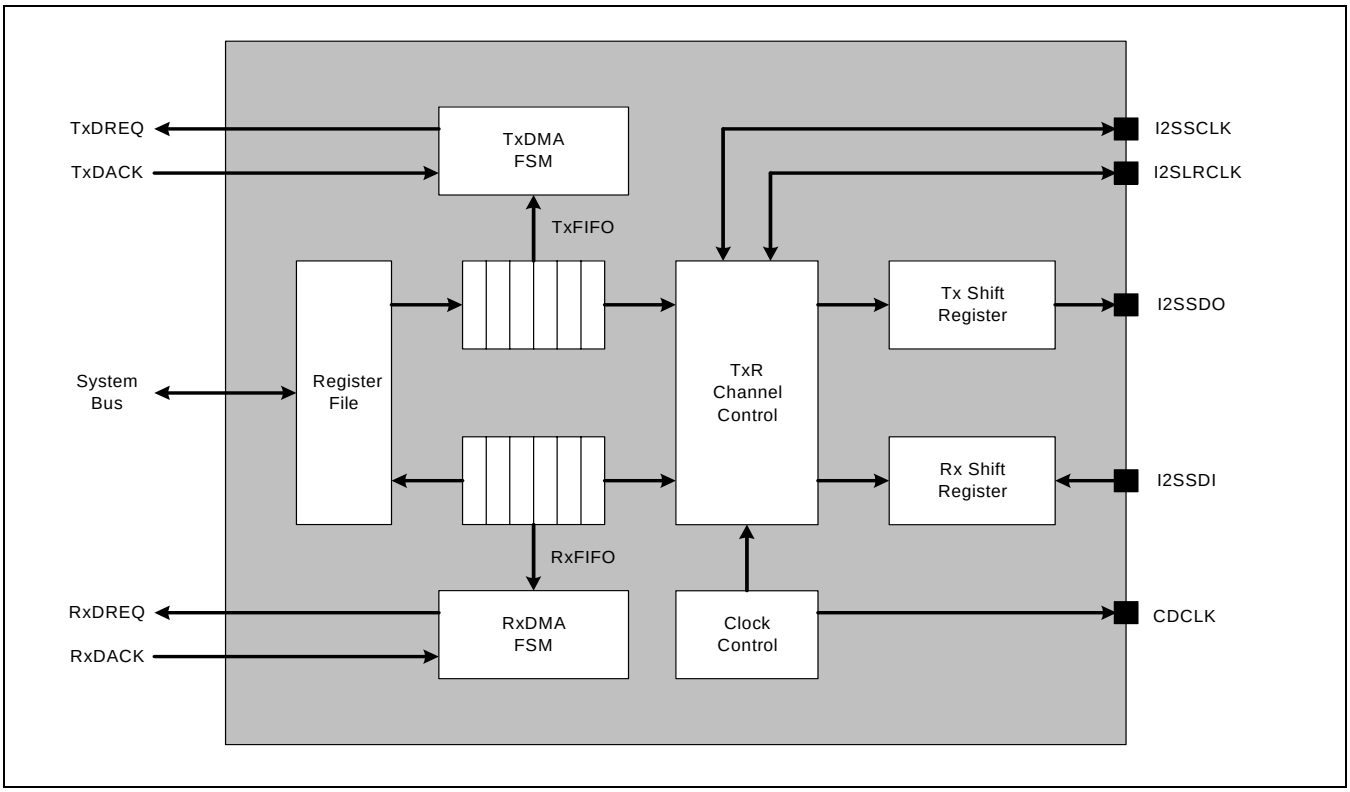


Figure 20-1. IIS-Bus Block Diagram

FUNCTIONAL DESCRIPTIONS

IIS interface consists of register bank, FIFOs, shift registers, clock control, DMA finite state machine, and channel control block as shown in Figure. Note that each FIFO has 32-bit width and 16 depth structure, which contains left/right channel data. So, FIFO access and data transfer are handled with left/right pair unit. Figure 20-1 shows the functional block diagram of IIS interface.

MASTER/SLAVE MODE

Master or slave mode can be chosen by setting IMS bit of IISMOD register. In master mode, I2SSCLK and I2SLRCLK are generated internally and supplied to external device. Therefore a root clock is needed for generating I2SSCLK and I2SLRCLK by dividing. The IIS prescaler (clock divider) is employed for generating a root clock with divided frequency from internal system clock. In external master mode, the root clock can be fed from IIS external directly. The I2SSCLK and I2SLRCLK are fed from chip external pin in slave mode. Figure 20-2 shows the route of the root clock with internal master or external master mode setting in the IIS clock control block. Note that RCLK indicates root clock and this clock can be provided to external with CDCLK form.

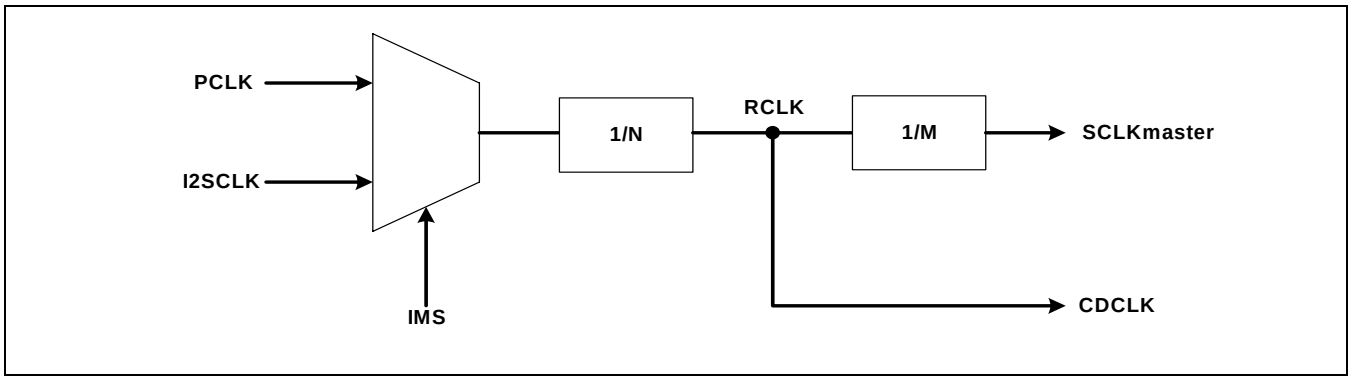


Figure 20-2. IIS Clock Control Block Diagram

DMA Transfer

In the DMA transfer mode, the transmitter or receiver FIFO are accessible by DMA controller. DMA service request is activated internally by the transmitter or receiver FIFO state. The FTXEMPT, FRXEMPT, FTXFULL, and FRXFULL bits of IISCON register represent the transmitter or receiver FIFO data state. Especially, FTXEMPT and FRXFULL bit are the ready flag for DMA service request; the transmit DMA service request is activated when TxFIFO is not empty and the receiver DMA service request is activated when RxFIFO is not full.

The DMA transfer uses only handshaking method for single data. Note that during DMA acknowledge activation, the data read or write operation should be performed.

AUDIO SERIAL DATA FORMAT

IIS-BUS FORMAT

The IIS bus has four lines including serial data input I2SSDI, serial data output I2SSDO, left/right channel select clock I2SLRCLK, and serial bit clock I2SSCLK; the device generating I2SLRCLK and I2SSCLK is the master.

Serial data is transmitted in 2's complement with the MSB first with a fixed position, whereas the position of the LSB depends on the word length. The transmitter sends the MSB of the next word at one clock period after the I2SLRCLK is changed. Serial data sent by the transmitter may be synchronized with either the trailing or the leading edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when transmitting data that is synchronized with the leading edge.

The LR channel select line indicates the channel being transmitted. I2SLRCLK may be changed either on a trailing or leading edge of the serial clock, but it does not need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The I2SLRCLK line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word.

MSB (LEFT) JUSTIFIED

MSB-Justified (Left-Justified) format is similar to IIS bus format, except that in MSB-justified format, the transmitter always sends the MSB of the next word at the same time whenever the I2SLRCLK is changed.

LSB (RIGHT) JUSTIFIED

LSB-Justified (Right-Justified) format is opposite to the MSB-justified format. In other word, the transferring serial data is aligned with ending point of I2SLRCLK transition.

Figure 20-3 shows the audio serial format of IIS, MSB-justified, and LSB-justified. Note that in this figure, the word length is 16 bit and I2SLRCLK makes transition every 24 cycle of I2SSCLK (BFS is 48 fs, where fs is sampling frequency; I2SLRCLK frequency).

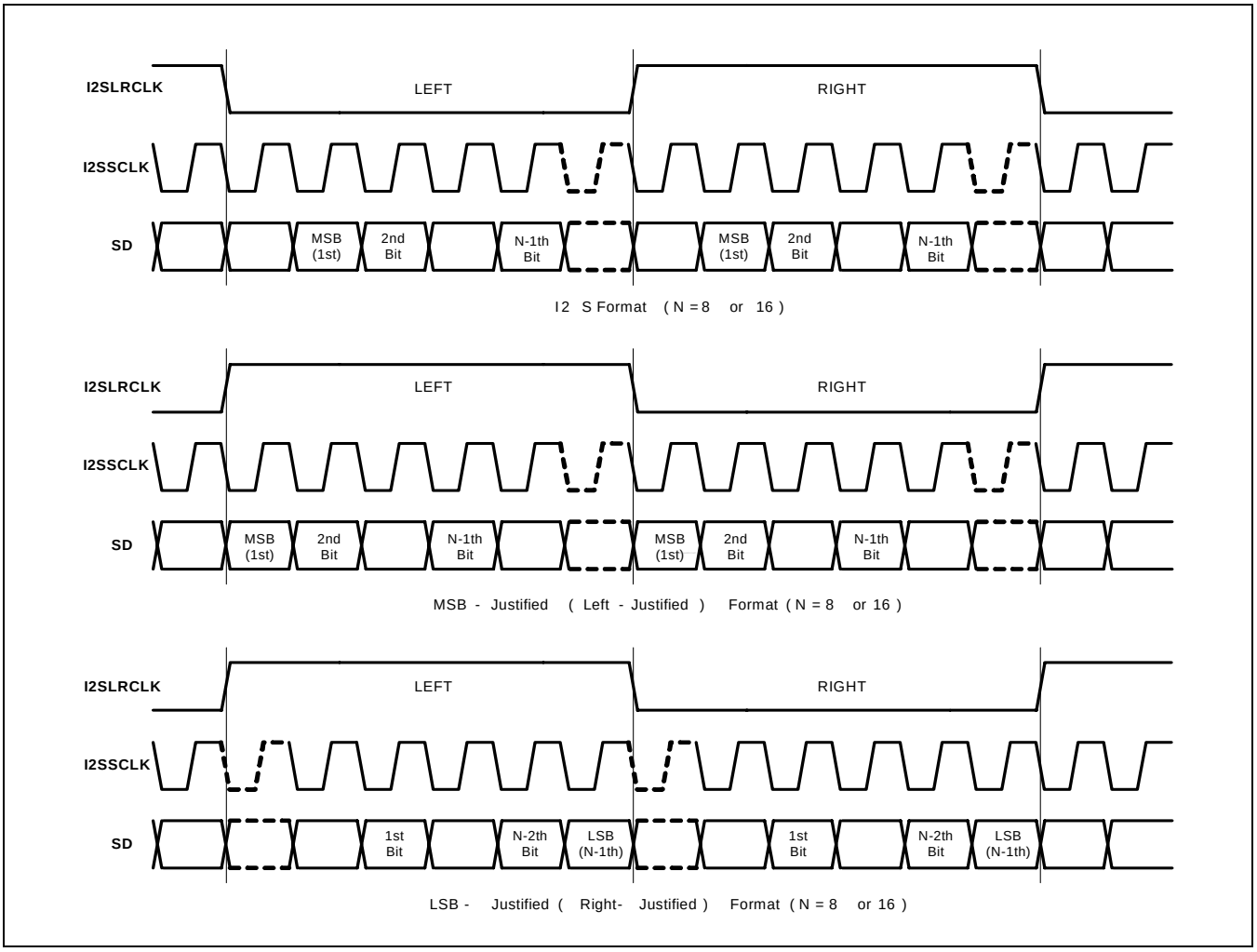


Figure 20-3. IIS Audio Serial Data Formats

SAMPLING FREQUENCY AND MASTER CLOCK

Master clock frequency (PCLK) can be selected by sampling frequency as shown in Table 20-1. Because PCLK is made by IIS prescaler, the prescaler value and PCLK type (256 or 384fs) should be determined properly.

Table 20-1. CODEC clock (CODECLK = 256 or 384fs)

IISLRCK (fs)	8.000 kHz	11.025 kHz	16.000 kHz	22.050 kHz	32.000 kHz	44.100 kHz	48.000 kHz	64.000 kHz	88.200 kHz	96.000 kHz
CODECLK (MHz)	256fs									
	2.0480	2.8224	4.0960	5.6448	8.1920	11.2896	12.2880	16.3840	22.5792	24.5760
	384fs									
	3.0720	4.2336	6.1440	8.4672	12.2880	16.9344	18.4320	24.5760	33.8688	36.8640

IIS CLOCK MAPPING TABLE

On selecting BFS, RFS, and BLC bits of IISMOD register, user should refer to the following table. Table 20-2 shows the allowable clock frequency mapping relations.

Table 20-2. IIS clock mapping table

Clock Frequency		RFS			
		256 fs (00B)	512 fs (01B)	384 fs (10B)	768 fs (11B)
BFS	16 fs (10B)	(a)	(a)	(a)	(a)
	24 fs (11B)	-	-	(a)	(a)
	32 fs (00B)	(a) (b)	(a) (b)	(a) (b)	(a) (b)
	48 fs (01B)	-	-	(a) (b)	(a) (b)
Descriptions		(a) Allowed when BLC is 8-bit (b) Allowed when BLC is 16-bit			

IIS-BUS INTERFACE SPECIAL REGISTERS

Table 20-3. Register summary of IIS interface

Register	Address	R/W	Description	Reset Value
IISCON	0x55000000	R/W	IIS interface control register	0xE00
IISMOD	0x55000004	R/W	IIS interface mode register	0x0
IISFIC	0x55000008	R/W	IIS interface FIFO control register	0x0
IISPSR	0x5500000C	R/W	IIS interface clock divider control register	0x0
IISTXD	0x55000010	W	IIS interface transmit data register	0x0
IISRXD	0x55000014	R	IIS interface receive data register	0x0

NOTE: All registers of IIS interface are accessible by word unit with STR/LDR instructions.

IISCON	Bit	R/W	Description
	[31:12]	R/W	Reserved. Program to zero.
LRI	[11]	R	Left/Right channel clock indication. Note that LRI meaning is dependent on the value of LRP bit of IISMOD register. 0: Left (when LRP bit is low) or right (when LRP bit is high) 1: Right (when LRP bit is low) or left (when LRP bit is high)
FTXEMPT	[10]	R	Tx FIFO empty status indication. 0: FIFO is not empty (ready for transmit data to channel) 1: FIFO is empty (not ready for transmit data to channel)
FRXEMPT	[9]	R	Rx FIFO empty status indication. 0: FIFO is not empty 1: FIFO is empty
FTXFULL	[8]	R	Tx FIFO full status indication. 0: FIFO is not full 1: FIFO is full
FRXFULL	[7]	R	Rx FIFO full status indication. 0: FIFO is not full (ready for receive data from channel) 1: FIFO is full (not ready for receive data from channel)
TXDMAPAUSE	[6]	R/W	Tx DMA operation pause command. Note that when this bit is activated at any time, the DMA request will be halted after current on-going DMA transfer is completed. 0: No pause DMA operation 1: Pause DMA operation
RXDMAPAUSE	[5]	R/W	Rx DMA operation pause command. Note that when this bit is activated at any time, the DMA request will be halted after current on-going DMA transfer is completed. 0: No pause DMA operation

			1: Pause DMA operation

IISCON	Bit	R/W	Description
TXCHPAUSE	[4]	R/W	Tx channel operation pause command. Note that when this bit is activated at any time, the channel operation will be halted after left-right channel data transfer is completed. 0: No pause operation 1: Pause operation
RXCHPAUSE	[3]	R/W	Rx channel operation pause command. Note that when this bit is activated at any time, the channel operation will be halted after left-right channel data transfer is completed. 0: No pause operation 1: Pause operation
TXDMACTIVE	[2]	R/W	Tx DMA active (start DMA request). Note that when this bit is set from high to low, the DMA operation will be forced to stop immediately. 0: Inactive, 1: Active
RXDMACTIVE	[1]	R/W	Rx DMA active (start DMA request). Note that when this bit is set from high to low, the DMA operation will be forced to stop immediately. 0: Inactive, 1: Active
IISACTIVE	[0]	R/W	IIS interface active (start operation). 0: Inactive, 1:Active

IISMOD	Bit	R/W	Description
	[31:12]	R/W	Reserved. Program to zero.
IMS	[11:10]	R/W	IIS master (internal/external) or slave mode select. 00: Internal master mode (divide mode, using PCLK) 01: External master mode (bypass mode, using I2SCLK) 1x: Slave mode
TXR	[9:8]	R/W	Transmit or receive mode select. 00: Transmit only mode 01: Receive only mode 10: Transmit and receive simultaneous mode 11: Reserved
LRP	[7]	R/W	Left/Right channel clock polarity select. 0: Low for left channel and high for right channel 1: High for left channel and low for right channel
SDF	[6:5]	R/W	Serial data format. 00: IIS format 01: MSB-justified (left-justified) format 10: LSB-justified (right-justified) format 11: Reserved
RFS	[4:3]	R/W	IIS root clock (codec clock) frequency select. 00: 256 fs, where fs is sampling frequency 01: 512 fs 10: 384 fs 11: 768 fs
BFS	[2:1]	R/W	Bit clock frequency select. 00: 32 fs, where fs is sampling frequency 01: 48 fs 10:16 fs 11: 24 fs
BLC	[0]	R/W	Bit length per channel. 0: 16-bit, 1: 8-bit

IISFIC	Bit	R/W	Description
	[31:16]	R/W	Reserved. Program to zero.
TFLUSH	[15]	R/W	Tx FIFO flush command. 0: No flush, 1: Flush
	[14:13]	R/W	Reserved. Program to zero.
FTXCNT	[12:8]	R	Tx FIFO data count. FIFO has 16 dept, so value ranges from 0 to 16. N: Data count N of FIFO
RFLUSH	[7]	R/W	Rx FIFO flush command. 0: No flush, 1: Flush
	[6:5]	R/W	Reserved. Program to zero.
FRXCNT	[4:0]	R	Rx FIFO data count. FIFO has 16 dept, so value ranges from 0 to 16. N: Data count N of FIFO

IISPSR	Bit	R/W	Description
	[31:16]	R/W	Reserved. Program to zero.
PSRAEN	[15]	R/W	Prescaler (Clock divider) A active. If you use the slave mode, you can set ‘0’. But if you use the master mode, you must set ‘1’. 0: Inactive, 1: Active
	[14]	R/W	Reserved. Program to zero.
PSVALA	[13:8]	R/W	Prescaler (Clock divider) A division value. N: Division factor is N+1
	[7:0]	R/W	Reserved. Program to zero.

IISTXD	Bit	R/W	Description
IISTXD	[31:0]	W	Tx FIFO write data. Note that the left/right channel data is allocated as the following bit fields. R[31:16], L[15:0] when 16-bit BLC R[23:16], L[7:0] when 8-bit BLC

IISRXD	Bit	R/W	Description
IISRXD	[31:0]	R	Rx FIFO read data. Note that the left/right channel data is allocated as the following bit fields. R[31:16], L[15:0] when 16-bit BLC R[23:16], L[7:0] when 8-bit BLC

NOTES

21 SPI INTERFACE

OVERVIEW

The S3C2413 X Serial Peripheral Interface (SPI) can interface the serial data transfer. The S3C2413 X includes two SPI, each of which has two 8-bit shift registers for transmission and receiving, respectively. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). And each SPI also supports Tx and Rx FIFO mode respectively for consecutive data transfer. 8-bit serial data at a frequency is determined by its corresponding control register settings. If you only want to transmit, received data can be dummy. Otherwise, if you only want to receive, you should transmit dummy '1' data.

There are 4 I/O pin signals associated with SPI transfers: the SCK (SPICLK0,1), the MISO (SPIMISO0,1) data line, the MOSI (SPIMOSI0,1) data line, and the active low /SS (nSS0,1) pin (input).

FEATURES

- SPI Protocol (ver. 2.11) compatible
- 8-bit Shift Register for transmit
- 8-bit Shift Register for receive
- Support 16-Byte Tx/Rx FIFO mode respectively
- 8-bit Prescaler logic
- Polling, Interrupt, and DMA transfer mode

BLOCK DIAGRAM

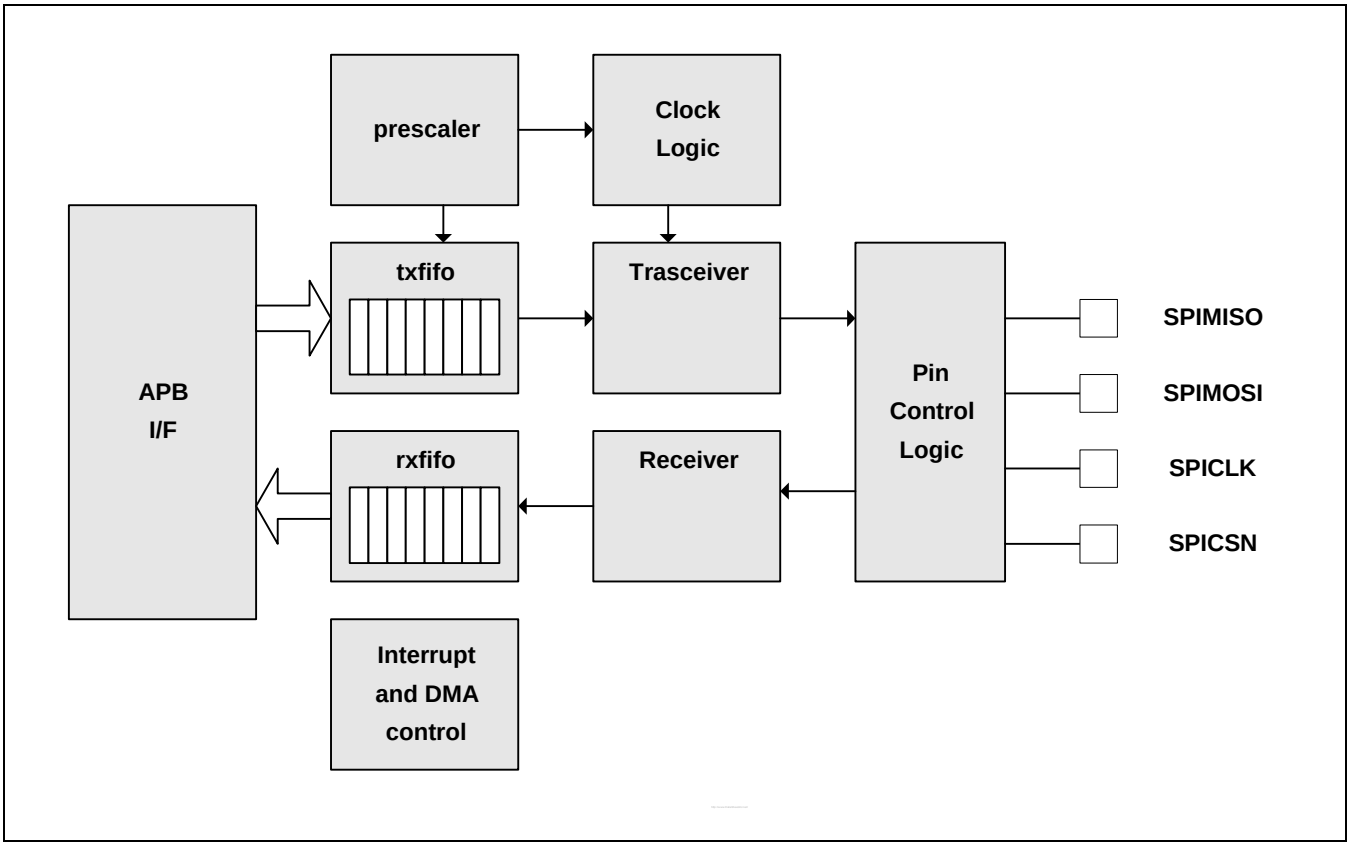


Figure 21-1. SPI Block Diagram

SPI OPERATION

Using the SPI interface, 8-bit data can be sent and received simultaneously to/from an external device. A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. When SPI is the master, transmit frequency can be controlled by setting the appropriate bit to SPPREn register. User can modify its frequency to adjust the baud rate data register value. When SPI is used as a slave mode, external master supplies the operating clock. When a programmer writes byte data to SPTDATn register, SPI transmit and receive operation will start simultaneously. In some cases, nSS should be activated before writing byte data to SPTDATn.

Programming Procedure

When a byte data is written into the SPTDATn register, SPI starts to transmit if ENSCK and MSTR of SPCONn register are set. There is a typical programming procedure to operate an SPI card.

When a byte data is written into the SPTDATn register, SPI starts to transmit if ENSCK and MSTR of SPCONn register are set. You can use a typical programming procedure to operate an SPI card.

To program the SPI modules, follow these basic steps:

1. Set Baud Rate Prescaler Register (SPPREn).
2. Set SPCONn to configure properly the SPI module.
3. Write data 0xFF to SPTDATn 10 times in order to initialize MMC or SD card.
4. Set a GPIO pin, which acts as nSS, low to activate the MMC or SD card.
5. Tx data →Check the status of Transfer Ready flag (REDY_org=1), and then write data to SPTDATn.
6. Rx data : SPCONn's TAGD bit enable = Tx Auto Garbage Data mode

   → confirm REDY to set, and then read data from Read Buffer (First 2 datas are garbages)
7. Set a GPIO pin, which acts as nSS, high to deactivate the MMC or SD card.

SPI Transfer Format

The S3C2413 X supports 4 different format to transfer the data. Figure 21-2 shows four waveforms for SPICLK..

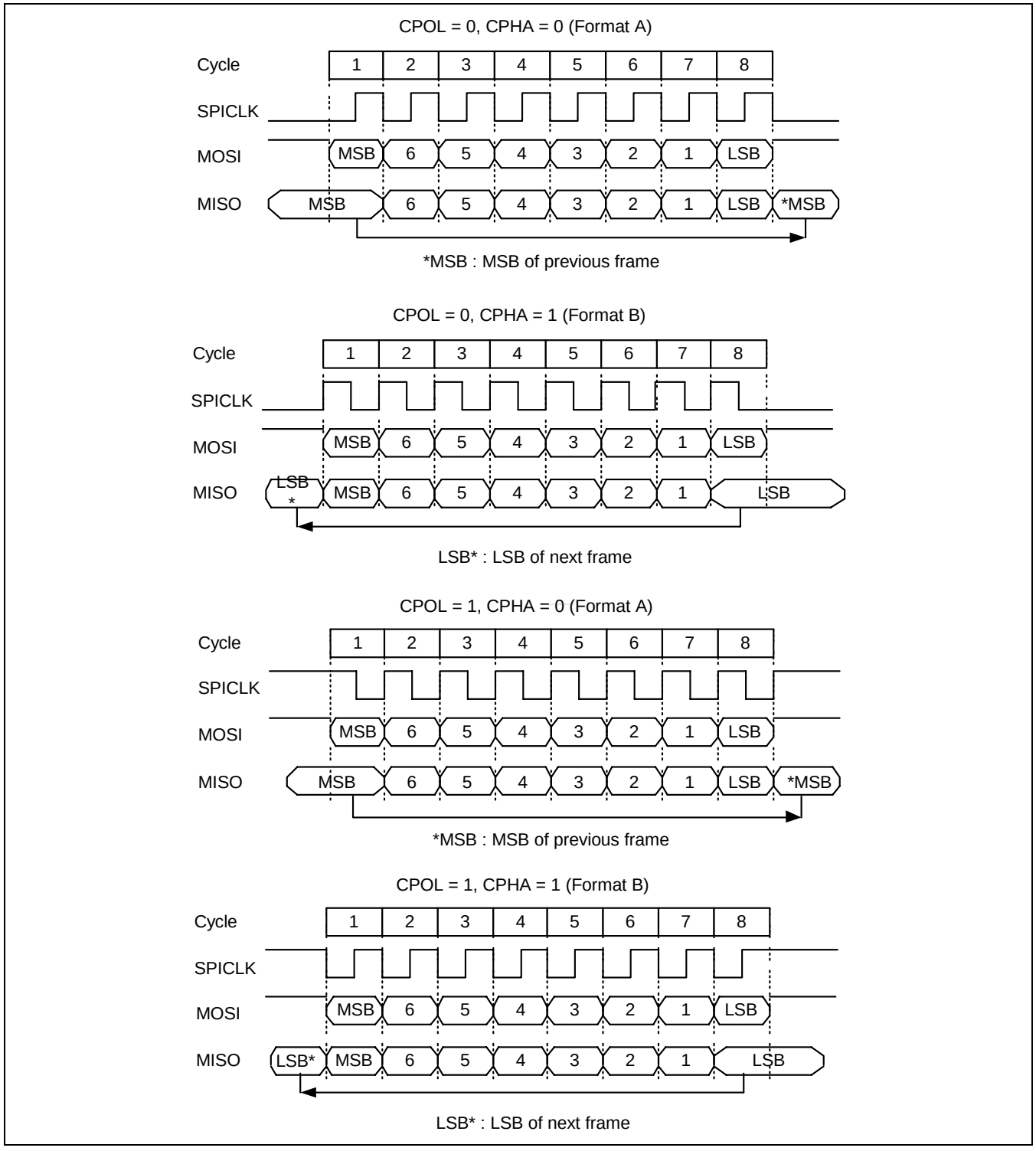


Figure 21-2. SPI Transfer Format

Transmitting Procedure by DMA

1. The SPI is configured as DMA mode.
2. SPI is configured as DMA mode.
3. SPI requests DMA service.
4. DMA transmits 1byte data to the SPI.
5. SPI transmits the data to card.
6. Return to Step 3 until DMA count becomes 0.
7. SPI is configured as interrupt or polling mode with SMOD bits.

Receiving Procedure by DMA

1. SPI is configured with TAGD bit set.
2. Read 2 times for dummy byte pull out.
3. SPI is configured as DMA start with SMOD bits.
4. DMA is configured properly.
5. SPI receives 1byte data from card.
6. SPI requests DMA service.
7. DMA receives the data from the SPI.
8. Write data 0xFF automatically to SPTDATn.
9. Return to Step 6 until DMA count becomes 0.
10. SPI is configured as polling mode with SMOD bits.
11. If SPSTAn's READY flag is set, then read the last byte data.

NOTE

Total received data = the first 2 data in polling mode + DMA TC values + the last data in polling mode (Step 11).
The first two DMA received datas are dummy and the user can neglect it.
The last data can be neglected

SPI Slave Rx Mode with Format B

If the SPI slave Rx mode is activated and SPI format is set to format B, then SPI operation will be failed:

The READY signal, one of internal signals, becomes high before the SPI_CNT reaches 0. Therefore, in DMA mode, DATA_READ signal is generated before the last data is latched.

Guide

1) DMA mode: This mode cannot be used at SPI slave Rx mode with format B.
2) Polling mode:
   DATA_READ signal should be delayed by 1phase of SPICLK at SPI slave Rx mode with format B.
3) Interrupt mode:
   DATA_READ signal should be delayed 1phase of SPICLK at SPI slave Rx mode with format B.

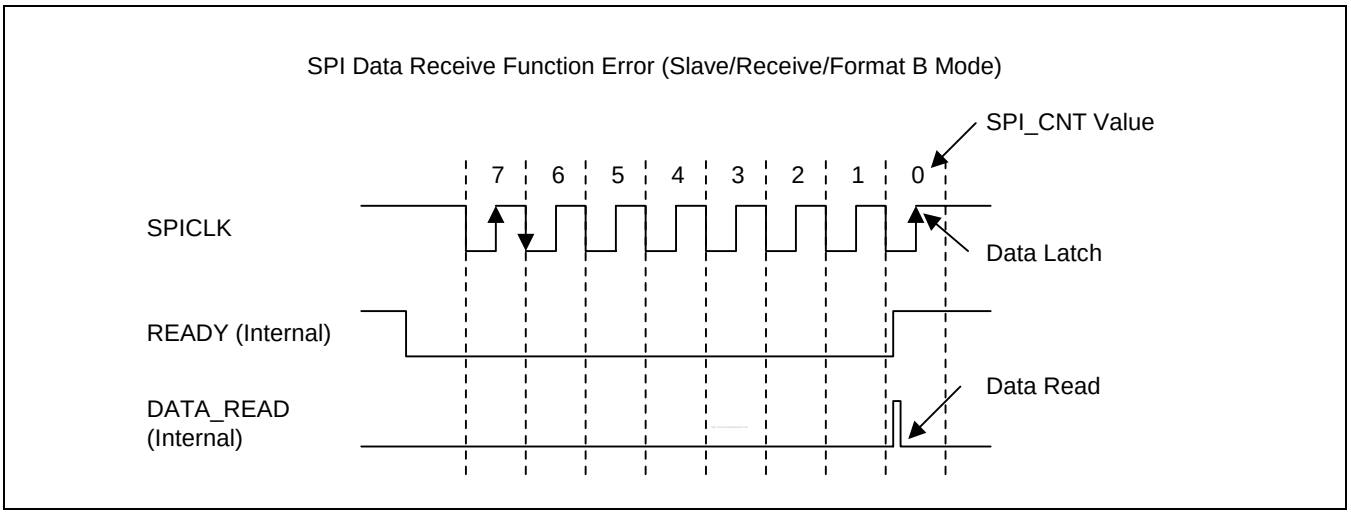


Figure 21-3. SPI Slave Rx mode with Format B (1-Byte Buffer mode)

Remaining Bytes in the Receive FIFO

When the Slave Rx FIFO mode is used, the SPI might not know the end of the byte transfer. In this case, the number of bytes in the receive FIFO less than the trigger threshold still remains. For the processing of the remaining bytes, Timeout Interrupt can be set using the PWMTIMER2 (external module). TOUT2 signal, the output of the PWMTIMER2, is used as a timeout clock(TIMER_CLK). Condition for Timeout Interrupt is no Rx FIFO read operation for 2 TIMER_CLK or no new data is received for that time. The period of TIMER_CLK can be controlled by the corresponding register in PWM TIMER.

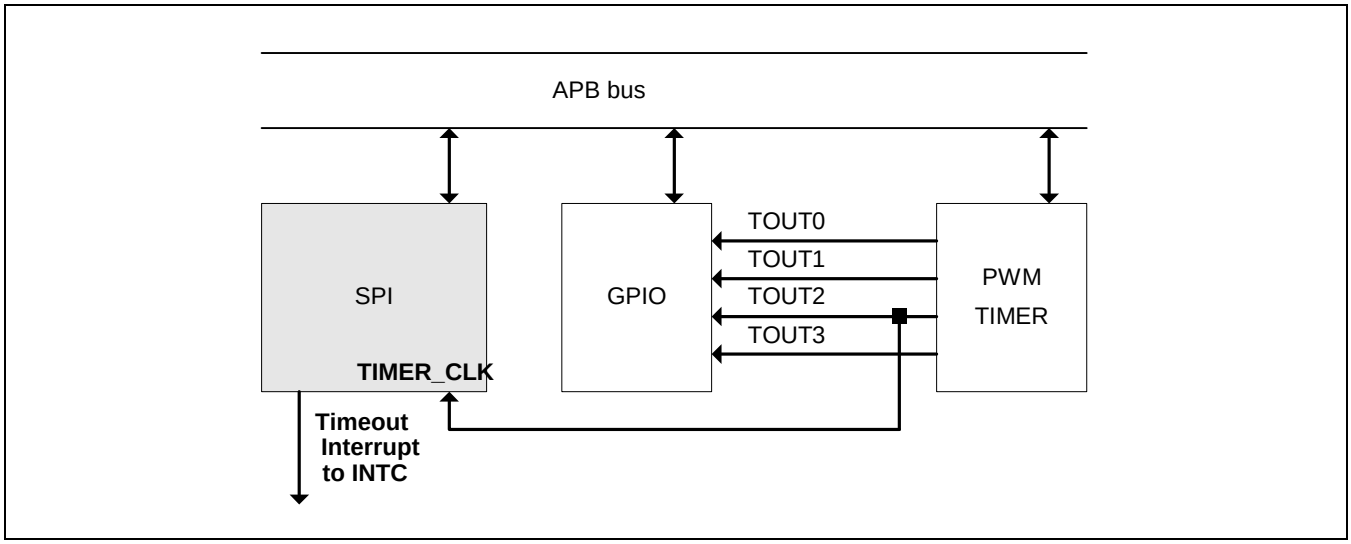


Figure 21-4. SPI Timeout Interrupt usage in the S3C2413X

SPI SPECIAL REGISTERS

SPI CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
SPCON0	0x59000000	R/W	SPI Channel 0 Control Register	0x0008
SPCON1	0x59000100	R/W	SPI Channel 1 Control Register	0x0008

SPCONn	Bit	Description	Initial State
RXFIFORB	[15:14]	Rx FIFO Remaining Byte control (almost full control) ‘00’=2-byte, ‘01’=4-byte, ‘10’=12-byte, ‘11’=14-byte	00
TXFIFORB	[13:12]	Tx FIFO Remaining Byte control (almost empty control) ‘00’=2-byte, ‘01’=4-byte, ‘10’=12-byte, ‘11’=14-byte	00
RXFIFORST	[11]	Rx FIFO Reset control When set to 1 = Rx FIFO software reset, auto cleared	0
TXFIFORST	[10]	Tx FIFO Reset control When set to 1 = Tx FIFO software reset, auto cleared.	0
SPI Rx FIFO Enable (RXFIFOEN)	[9]	Rx FIFO Enable 0= Rx FIFO path disable (So, Rx path is for Byte Access mode) 1= Rx FIFO path enable	0
SPI Tx FIFO Enable (TXFIFOEN)	[8]	Tx FIFO Enable 0=Tx FIFO path disable (So, Tx path is for Byte Access mode) 1=Tx FIFO path enable	0
SPI Direction (DIRC)	[7]	Transfer Direction 0=Tx, 1=Rx 1) Byte Access mode : When Rx mode, this bit should be set to High 2) FIFO mode : When this bit is high, SPICLK out for receiving data	0
SPI Mode Select (SMOD)	[6:5]	Determines how and by what SPTDAT is read/written 00 = polling mode, 01 = interrupt mode 10 = Buffer DMA mode using DREQ_TXFIFO, DACK_TXFIFO ports, 11 = Buffer DMA mode using DREQ_RXFIFO, DACK_RXFIFO ports Note : When this buffer transmit DMA mode is used, the FIFO DMA should not be used.	00
SCK Enable (ENSCK)	[4]	Determines what you want SCK enable or not(only master) 0 = disable, 1 = enable	0

SPCONn	Bit	Description	Initial State
Master/Slave Select(MSTR)	[3]	Determines what mode you want master or slave 0 = slave, 1 = master **NOTE:** In slave mode, there should be set up time for master to initiate Tx / Rx.	1
Clock Polarity Select(CPOL)	[2]	Determines an active high or active low clock. 0 = active high, 1 = active low	0
Clock Phase Select(CPHA)	[1]	This bit selects one of two fundamentally different transfer formats. 0 = format A, 1 = format B	0
Tx Auto Garbage Data mode enable (TAGD)	[0]	This bit decides whether the receiving data only needs or not. 0 = normal mode, 1 = Tx auto garbage data mode **NOTE:** In normal mode, you only want to receive data, you should transmit dummy 0xFF data. 1) Byte Access mode : when this bit is 'H', SPI clock is out whenever read operation is done. When write operation, don't care 2) FIFO Access mode : don't care	0

NOTES :

1. Chip selection (nCSI) must be accomplished after CPOL and CPHA is chosen
   RXFIFORST, TXFIFORST, RXFIFOEN, TXFIFOEN bit write access is allowed when the REDY_org (Status register bit 3) is high.
2. SMOD field should be set to polling mode(2'b00) when TX or RXFIFO DMA mode is used.

SPI STATUS REGISTER

Register	Address	R/W	Description	Reset Value
SPSTA0	0x59000004	R	SPI Channel 0 Status Register	0x439
SPSTA1	0x59000104	R	SPI Channel 1 Status Register	0x439

SPSTAn	Bit	Description	Initial State
Reserved	[15:12]	-	
RXFIFOAF	[11]	Rx FIFO Almost Full, Remaining bytes are RXFIFORB field in the SPCON[15:14] 0=Rx FIFO not almost full, 1=Rx FIFO almost full	0
TXFIFOAE	[10]	Tx FIFO Almost Empty, Remaining bytes are TXFIFORB field in the SPCON[13:12] 0=Tx FIFO not almost empty, 1=Tx FIFO almost empty	1
RXFIFOFERR	[9]	Rx FIFO full error 0=nomal, 1=Rx FIFO full error Note : When Master mode, if RxFIFO is full, Rx block do not write to RxFIFO.	0
TXFIFOEERR	[8]	Tx FIFO empty error 0=nomal, 1=Tx FIFO empty error Note : When Master mode, if TxFIFO is empty, Tx block do not read from TxFIFO.	0
RXFIFOFULL	[7]	Rx FIFO full 0=Rx FIFO not full, 1=Rx FIFO full	0
RXFIFONEMPTY	[6]	Rx FIFO not empty 0=Rx FIFO empty, 1=Rx FIFO not empty	0
TXFIFONFULL	[5]	Tx FIFO not full 0=Tx FIFO full, 1=Tx FIFO not full	1
TXFIFOEMPTY	[4]	Tx FIFO empty 0=Tx FIFO not empty, 1=Tx FIFO empty	1
Transfer Ready Flag PRE (REDY_org)	[3]	Rx Pre Buffer Transfer Ready Flag This bit indicates that SPTDATn or SPRDATBn is ready to transmit or receive. This flag is automatically cleared by writing data to SPTDATn when Tx mode and by reading data from SPRDATBn when Rx mode. 0 = not ready, 1 = data Tx/Rx ready	1
Data Collision Error Flag(DCOL)	[2]	This flag is set if the SPTDATn is written or the SPRDATBn is read while a transfer is in progress and cleared by reading the SPSTAn. 0 = not detect, 1 = collision error detect	0
Reserved	[1]	Reserved	0
Transfer Ready Flag (REDY)	[0]	This bit indicates that SPRDATn(Rx 2nd buffer) is ready to receive. This flag is automatically cleared by writing data to SPTDATn when Tx mode and by reading data from SPRDATn when Rx mode. 0 = not ready, 1 = data Tx/Rx ready	1

NOTES :

1. When Master Tx FIFO mode is used, TXFIFOEERR field has no meaning.
2. When Master Rx FIFO mode is used, RXFIFOFERR field has no meaning.

SPI PIN CONTROL REGISTER

When the SPI system is enabled, the direction of pins is controlled by MSTR bit of SPCONn register. If the SPI is configured as a Slave, nSS pin is used to chip select input pin by one master. If the SPI is configured as a Master, nSS pin can be used to chip select output pin to external slave device.

Register	Address	R/W	Description	Reset Value
SPPIN0	0x59000008	R/W	SPI Channel 0 Pin Control Register	0x02
SPPIN1	0x59000108	R/W	SPI Channel 1 Pin Control Register	0x02

SPPINn	Bit	Description	Initial State
Reserved	[7:3]	-	
FDCKEN	[3]	Feedback Clock enable 0=Disable, 1=Enable Note : Only in master mode, Rx block may use feedback SPI clock.	0
Multi Master error detect Enable (ENMUL)	[2]	The /SS pin is used as an input to detect multi master error when the SPI system is a master. 0 = disable(general purpose), 1 = multi master error detect enable	0
CS out	[1]	Master mode Chip select output (active low) 0=Chip select active, 1=Chip select inactive Note : Only in master mode this bit is to output port.	1
Master Out Keep(KEEP)	[0]	Determines MOSI drive or release when 1byte transmit finish(only master) 0 = release, 1 = drive the previous level	0

The SPIMISO(MISO) and SPIMOSI(MOSI) data pins are used for transmitting and receiving serial data. When the SPI is configured as a master, SPIMISO(MISO) is the master data input line, SPIMOSI(MOSI) is the master data output line, SPISSN is the chip select output, and SPICLK(SCK) is the clock output line. When as a slave, these pins reverse roles.

SPI Baud Rate Prescaler Register

Register	Address	R/W	Description	Reset Value
SPPRE0	0x5900000C	R/W	SPI Cannel 0 Baud Rate Prescaler Register	0x00
SPPRE1	0x5900010C	R/W	SPI Cannel 1 Baud Rate Prescaler Register	0x00

SPPREn	Bit	Description	Initial State
Prescaler Value	[7:0]	Determines SPI clock rate as above equation. Baud rate = PCLK / 2 / (Prescaler value + 1)	0x00

NOTE: Baud rate should be less than 25 MHz.

SPI Tx Data Register

Register	Address	R/W	Description	Reset Value
SPTDAT0	0x59000010	R/W	SPI Channel 0 Tx Data Register	0x00
SPTDAT1	0x59000110	R/W	SPI Channel 1 Tx Data Register	0x00

SPTDATn	Bit	Description	Initial State
Tx Data Register	[7:0]	This field contains the data byte to be transmitted over the SPI channel (when Not TxFIFO is not enabled)	0x00

SPI Rx Data Register

Register	Address	R/W	Description	Reset Value
SPRDAT0	0x59000014	R	SPI Channel 0 Rx Data Register	0x00
SPRDAT1	0x59000114	R	SPI Channel 1 Rx Data Register	0x00

SPRDATn	Bit	Description	Initial State
Rx Data Register	[7:0]	This field contains the data to be received over the SPI channel (Second byte Rx Buffer)	0x00

SPI TxFIFO Data Register

Register	Address	R/W	Description	Reset Value
SPTXFIFO0	0x59000018	W	SPI Channel 0 Tx FIFO Register	0x00
SPTXFIFO1	0x59000118	W	SPI Channel 1 Tx FIFO Register	0x00

SPRDATn	Bit	Description	Initial State
Tx FIFO Data Register	[7:0]	This field contains the data to be transferred when TXFIFO is enabled.	0x00

SPI RxFIFO Data Register

Register	Address	R/W	Description	Reset Value
SPRXFIFO0	0x5900001C	R	SPI Channel 0 Rx FIFO Register	0x00
SPRXFIFO1	0x5900011C	R	SPI Channel 1 Rx FIFO Register	0x00

SPRXFIFOn	Bit	Description	Initial State
Rx FIFO Data Register	[7:0]	This field contains the data to be transferred when TXFIFO is enabled.	0x00

SPI Pre-Data Register

Register	Address	R/W	Description	Reset Value
SPRDATB0	0x59000020	R	SPI Channel 0 Rx Data Register	0xFF
SPRDATB1	0x59000120	R	SPI Channel 1 Rx Data Register	0xFF

SPRDATBn	Bit	Description	Initial State
Rx Data Register	[7:0]	This field contains the data to be received over the SPI channel : First byte Rx Buffer, before transmitted to SPRDAT register	0xFF

SPI FIFO Interrupt/DMA Control Register

Register	Address	R/W	Description	Reset Value
SPFIC0	0x59000024	R/W	SPI Channel 0 FIFO Interrupt and DMA control Register	0xA00
SPFIC1	0x59000124	R/W	SPI Channel 0 FIFO Interrupt and DMA control Register	0xA00

SPFICn	Bit	Description	Initial State
Reserved	[15:12]	-	0
RXFIFODMACTL	[11:10]	Rx FIFO DMA Control register 00=disable, 01=RxFIFO not empty, 10=RxFIFO almost full 11=reserved	10
TXFIFODMACTL	[9:8]	Tx FIFO DMA Control register 00=disable, 01=TxFIFO empty, 10=TxFIFO almost empty 11=reserved	10
Reserved	[7:6]	-	0
RXFIFOAFIE	[5]	Rx FIFO Almost Full Interrupt Enable 0=disable, 1=enable	0
TXFIFOAEIE	[4]	Tx FIFO Almost Empty Interrupt Enable 0=disable, 1=enable	0
RXFIFOFEIE	[3]	Rx FIFO Full Error Interrupt Enable Receiver tries to write into the Rx FIFO when full state. 0=disable, 1=enable	0
TXFIFOEEIE	[2]	Tx FIFO Empty Error Interrupt Enable Transmitter tries to read from the Tx FIFO when empty state. 0=disable, 1=enable	0
RXFIFOFLIE	[1]	Rx FIFO Full Interrupt Enable 0=disable, 1=enable	0
TXFIFOEMIE	[0]	Tx FIFO Empty Interrupt Enable 0=disable, 1=enable	0

NOTE : Tx FIFO DMA request condition

1)Tx FIFO empty

2)Tx FIFO almost empty : TxFIFO almost empty state is defined in the register field TxFIFORB (SPCON[13:12]), recommended setting is 10-byte(initial value).

Rx FIFO DMA request condition

3)Rx FIFO not empty

4) Rx FIFO not almost full : RxFIFO almost full state is defined in the register field RxFIFORB(SPCON[15:14]), recommended setting is 4-byte(initial value)

NOTE : When Master Rx FIFO mode is used and RXFIFODMACTL is set to 2'b10 (RxFIFO almost full, 4-byte setting), 4-byte burst operation is requested to the DMA Controller. In this mode, DCON register APBANI field of the DMA Controller should be set to High (fixed address out when burst 4 mode). DMA Controller is external SPI module.

22 CAMERA INTERFACE

OVERVIEW

This specification defines the interface of camera. The CAMERA INTRERACE module consists of five parts. They are the pattern mux, capturing unit, codec scaler, codec DMA, and SFR. The camera interface supports ITU R BT-601/656 YCbCr 8-bit standard. Maximum input size is 1600x1200 pixels (1600x1200 pixels for scaling). This module has one scaler. Codec scaler is dedicated to generate codec useful image like plane type YCbCr 4:2:0 or 4:2:2. Master DMAs can do mirror and rotate the captured image for mobile environments. This features are very useful at folder type cellular phone. And test pattern generation can be used to calibration of input sync signals as HREF,VSYNC. Also, video sync signals and pixel clock polarity can be inverted in the camera interface side with using register setting.

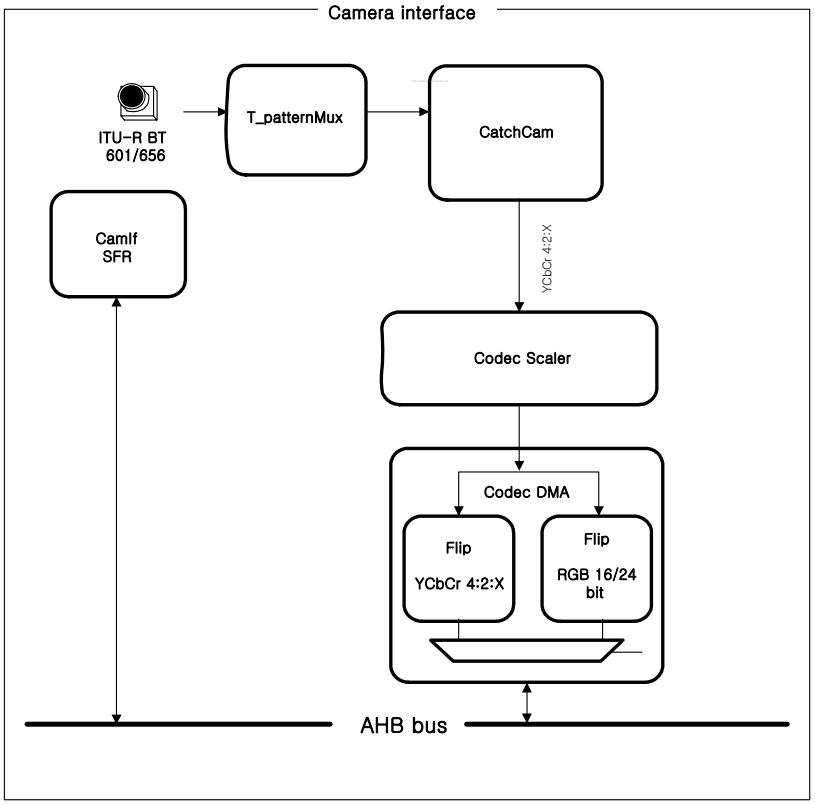


Figure 22-1. Camera interface overview

FEATURES

— ITU-R BT 601/656 8-bit mode support
— DZI (Digital Zoom In) capability
— Multiple camera input support
— Programmable polarity of video sync signals
— Max. 1600x1200 pixels input support (1600 x 1200 pixel input support for scaling)
— Codec Image mirror (X-axis mirror, Y-axis mirror)
— Codec input image generation (YCbCr 4:2:0 / 4:2:2 format or RGB 16 / 24-bit format)
— Capture frame control support in codec_path
— Scan line offset support
— YCbCr 4:2:2 codec image format interleave support

EXTERNAL INTERFACE

FIMC 2.2 can support the next video standards.

— ITU-R BT 601 YCbCr 8-bit mode

— ITU-R BT 656 YCbCr 8-bit mode

SIGNAL DESCRIPTION

Name	I/O[1)]	Active	Description
External camera processor interface signal			
PCAMPCLK	I	-	Pixel Clock, driven by the Camera processor
PCAMVSYNC	I	H/L	Frame Sync, driven by the Camera processor
PCAMHREF	I	H/L	Horizontal Sync, driven by the Camera processor
PCAMDATA [7:0]	I	-	Pixel Data driven by the Camera processor
PCAMPCLKOUT	O	-	Master Clock to the Camera processors
PCAMRESET	O	H/L	Software Reset or Power Down for the Camera processor

Note [1)] I/O direction is on the S3C2413 side. I : input, O : output, B : bi-direction

TIMING DIAGRAM

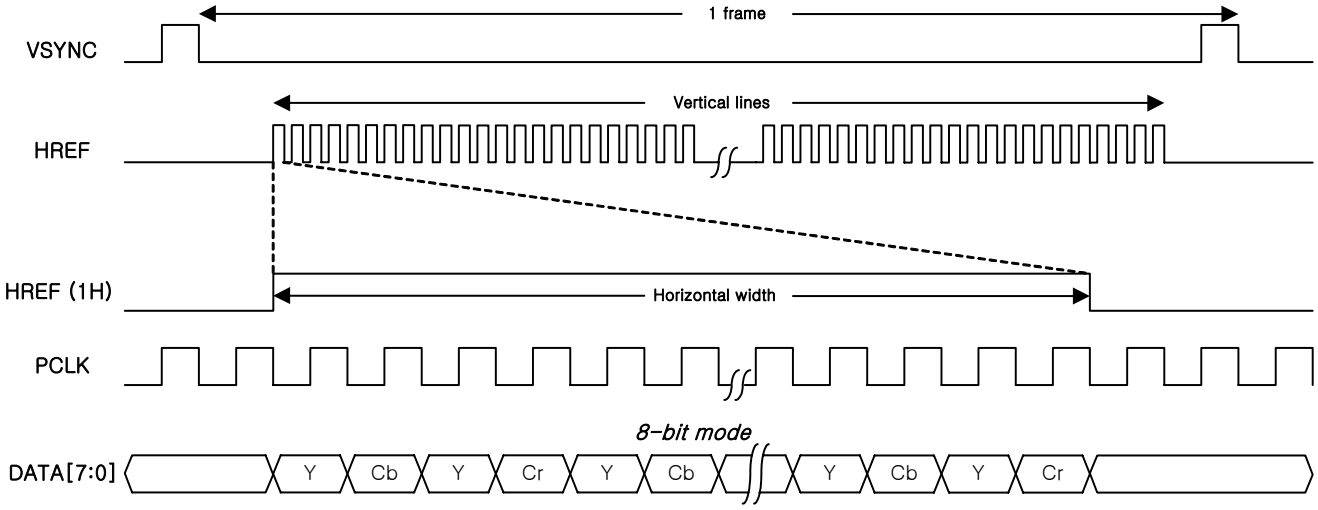


Figure 22-2a. ITU-R BT 601 Input timing diagram

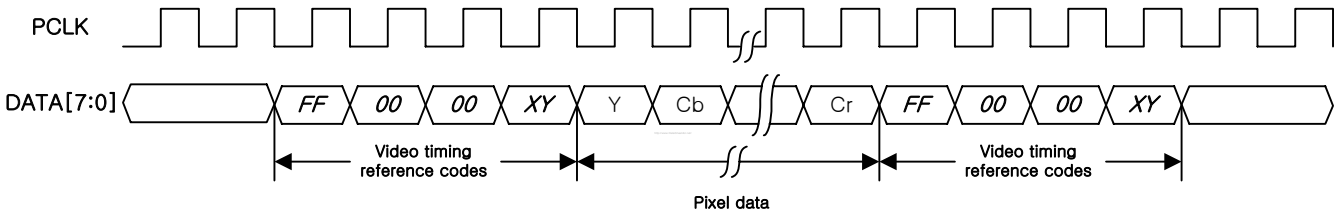


Figure 22-2b. ITU-R BT 656 Input timing diagram

There are two timing reference signals in ITU-R BT 656 format, one at the beginning of each video data block (start of active video, SAV) and one at the end of each video data block(end of active video, EAV) as shown in Figure 22-2 and Table 22-1.

Table 22-1. Video timing reference codes of ITU-656 format

Data bit number	First word	Second word	Third word	Fourth word
9 (MSB)	1	0	0	1
8	1	0	0	F
7	1	0	0	V
6	1	0	0	H
5	1	0	0	P3
4	1	0	0	P2
3	1	0	0	P1
2	1	0	0	P0
1 (Note 1)	1	0	0	0
0	1	0	0	0

Note 1) For compatibility with existing 8-bit interfaces, the values of bits D1 and D0 are not defined.
F = 0 (during field 1), 1 (during field 2)
V = 0 (elsewhere), 1 (during field blanking)
H = 0 (in SAV : Start of Active Video), 1 (in EAV : End of Active Video)
P0, P1, P2, P3 = protection bit

Camera interface logic can catch the video sync bits like H(SAV,EAV) and V(Frame Sync) after reserved data as “FF-00-00”.

EXTERNAL/INTERNAL CONNECTION GUIDE

All FIMC2.2 input signals should not occur inter-skewing to pixel clock line. Recommend next pin location and routing.

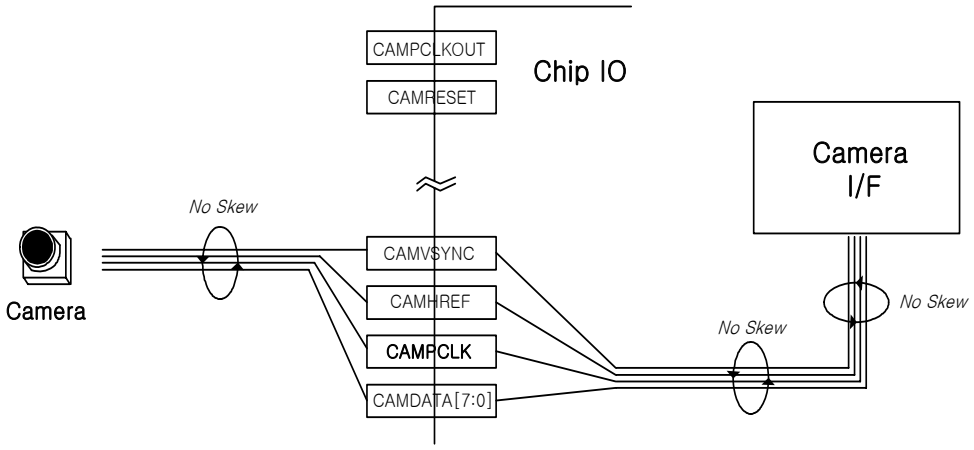


Figure 22-3. IO connection guide

In this case, Camera data are fed into S3C2413 through only PCAMDATA[7:0]. Therefore, Signal levels of PCAMDATA[7:0] are determined in appropriate value to prevent leakage current. If you connect these signals to ground, internal pull-up must be disabled at both normal and power saving mode.

CAMERA INTERFACE OPERATION

DMA PORT

CAMIF has DMA port. The C-port(Codec port) stores the YCbCr 4:2:0 or 4:2:2 image data into memory for Codec as MPEG-4, H.263, etc. This master port supports the variable applications like DSC (Digital Steel Camera), MPEG-4 video conference, video recording, etc. For example, C-port image can be used as JPEG image in DSC application.

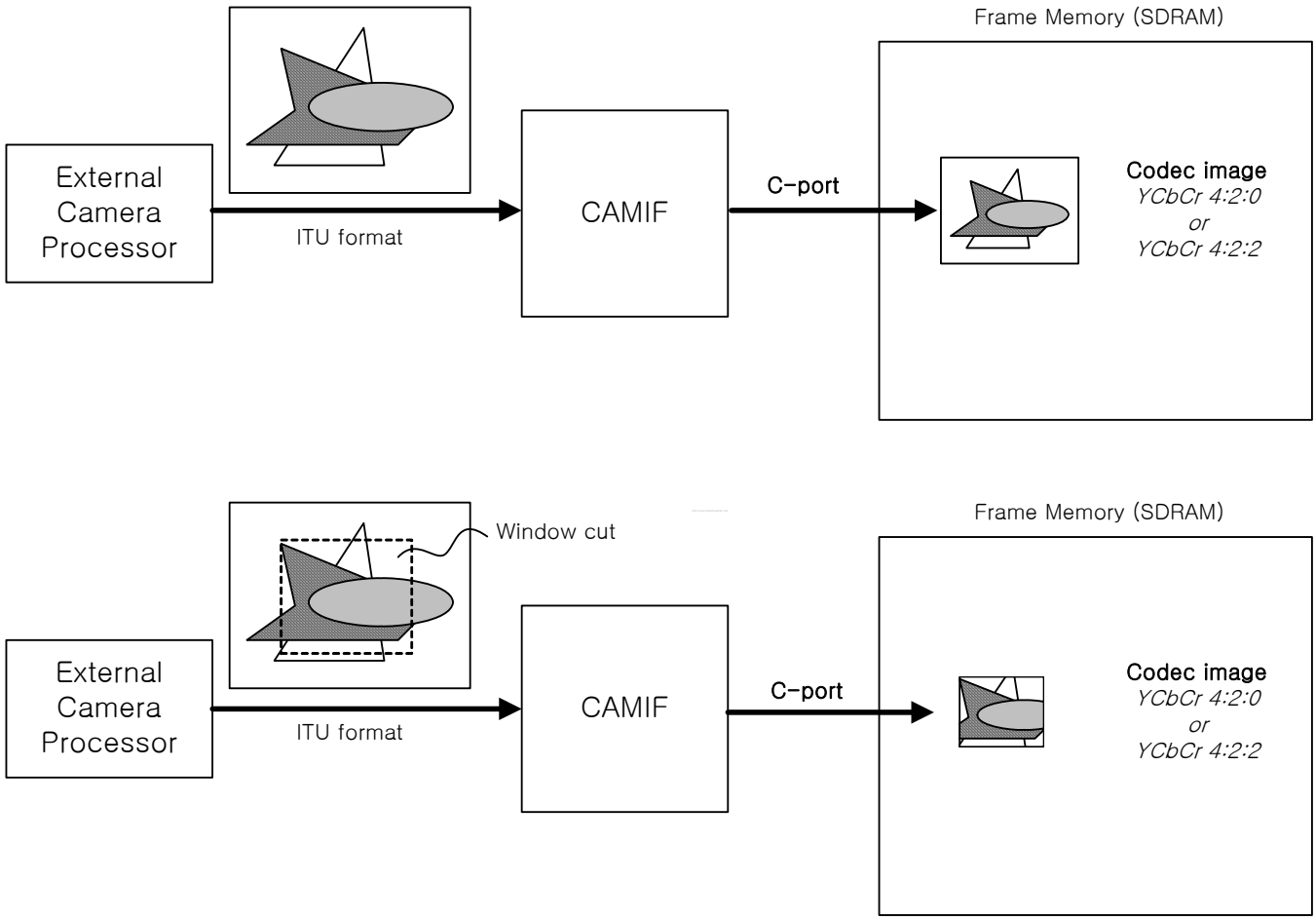


Figure 22-4. Codec DMA port

CLOCK DOMAIN

CAMIF has two clock domains. The one is the system bus clock, which is HCLK. The other is the pixel clock, which is PCLK. *The system clock must be faster than pixel clock*. As shown in Figure 22-5, CAMCLK must be divided from the fixed frequency like USB PLL clock. If external clock oscillator were used, CAMCLK should be floated. Internal scaler clock is system clock. It is not necessary for two clock domains to be synchronized each other. Other signals as PCLK should be similarly connected to shimitt-triggered level shifter.

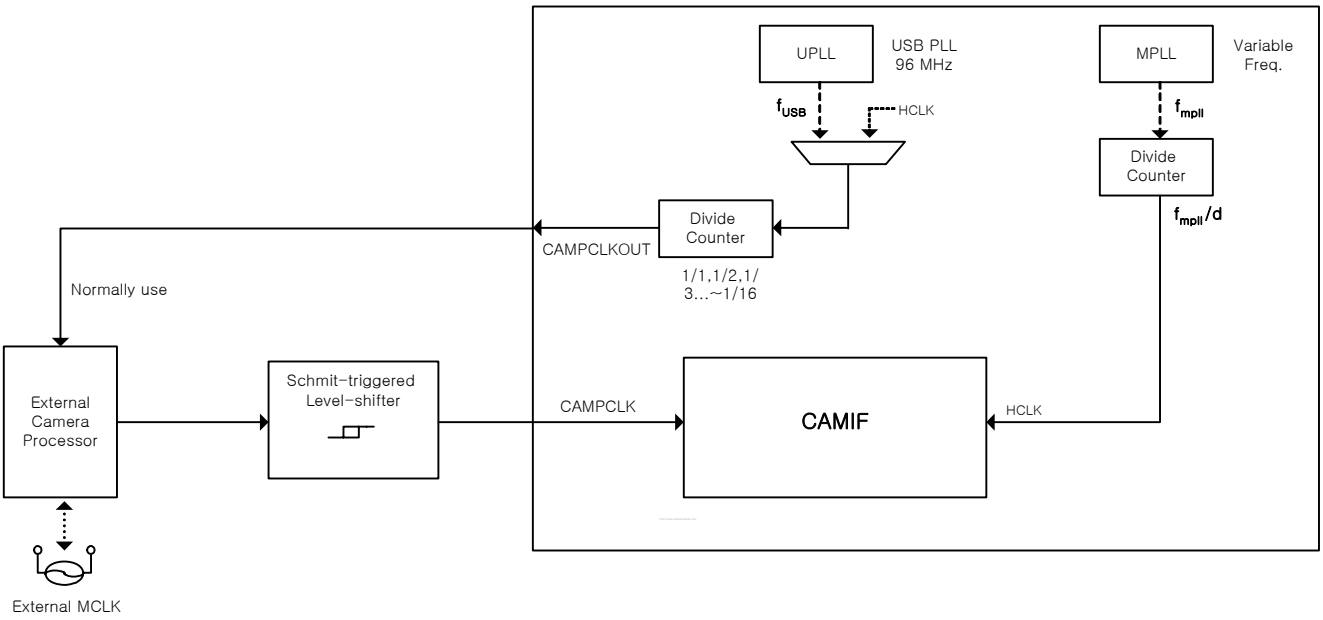


Figure 22-5. CAMIF clock generation

FRAME MEMORY HIRERARCHY

Frame memories consist of four ping-pong memories for C-ports. C-port ping-pong memories have three element memories that are luminance Y, chrominance Cb, and chrominance Cr.

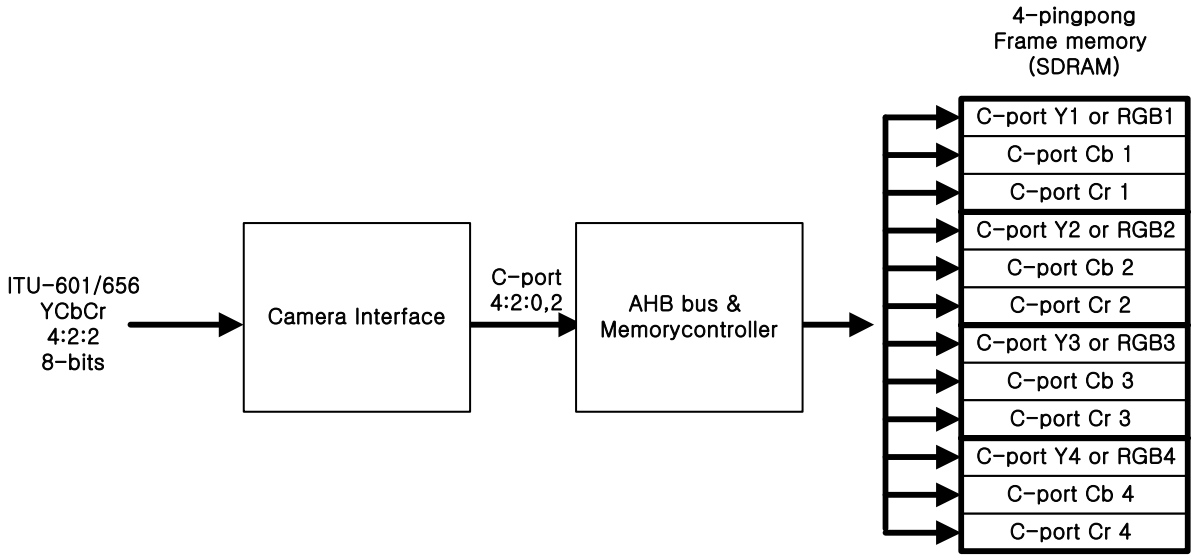


Figure 22-6. Ping-pong memory hierarchy

MEMORY STORING METHOD

The storing method to the frame memory is the little-endian method in codec path. The first entering pixels stored into LSB sides, and the last entering pixels stored into MSB sides. The carried data by AHB bus is 32-bit word. So, CAMIF make the each Y-Cb-Cr words by little endian style.

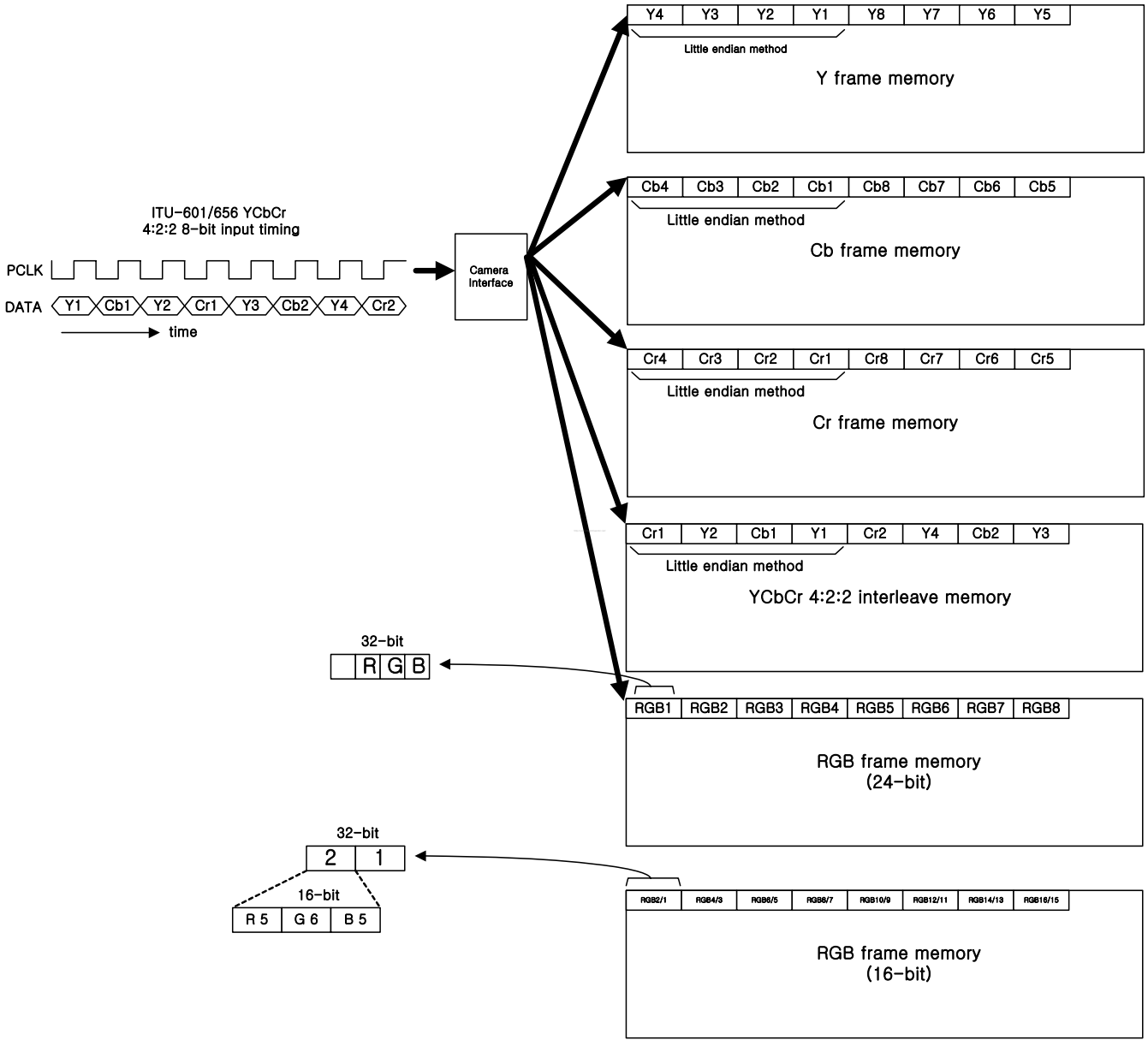


Figure 22-7. Memory storing style

TIMING DIAGRAM FOR REGISTER SETTING

The first register setting for frame capture command can be occurred in anywhere of frame period. But, it is recommend to do first setting at the VSYNC “L” state. VSYNC information can be read from status SFR. Refer to next pages. All command include ImgCptEn, is valid at VSYNC falling edge. Be sure that except first SFR setting, all command should be programmed in ISR(Interrupt Service Routine). It is not allowed for target size information to be changed during capture operation. However, image mirror or rotation, windowing, and Zoom In settings are allowed to change in capturing operation.

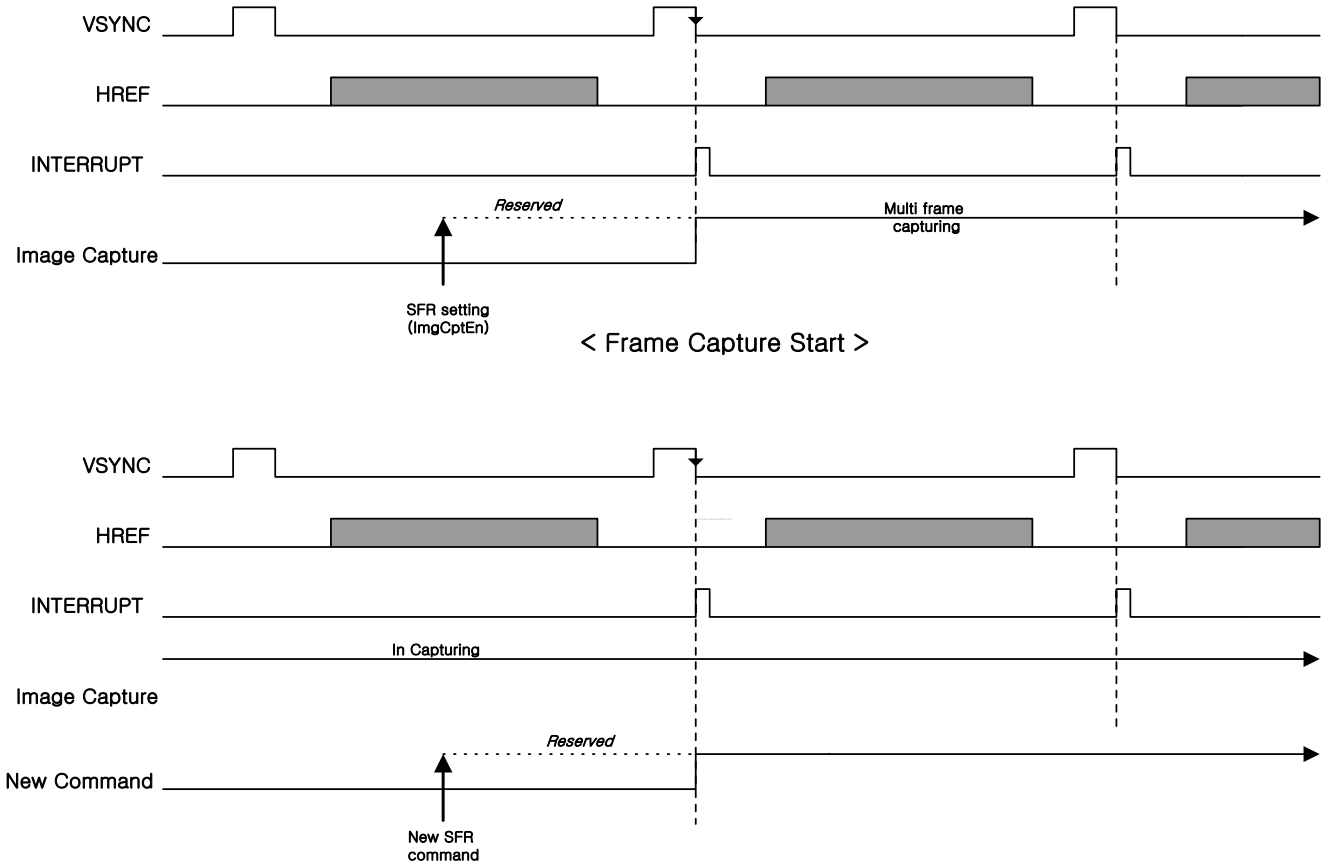


Figure 22-8. Timing diagram for register setting

TIMING DIAGRAM FOR LAST IRQ

IRQ except LastIRQ is generated before image capturing. Last IRQ which means capture-end can be set by following timing diagram. LastIRQEn is auto-cleared and ,as mentioned, SFR setting in ISR is for next frame command. So, for adequate last IRQ, you should follow next sequence between LastIRQEn and ImgCptEn/ImgCptEn_CoSc/ImgCptEnPrSC. It is recommended that ImgCptEn/ImgCptEn_CoSc/ImgCptEnPrSC are set at same time and at last of SFR setting in ISR. FrameCnt which is read in ISR, means next frame count. On following diagram, last captured frame count is “1”. That is, Frame 1 is the last-captured frame among frame 0~3. FrameCnt is increased by 1 at IRQ rising.

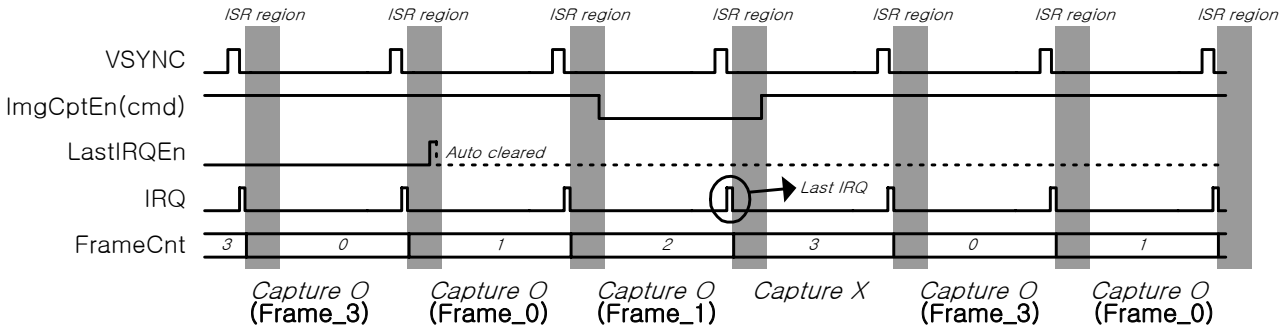


Figure 22-9. Timing diagram for last IRQ

SOFTWARE INTERFACE

Camera Interface SFR (Special Function Register)

CAMERA INTERFACE SPECIAL REGISTERS

SOURCE FORMAT REGISTER

Register	Address	R/W	Description	Reset Value
CISRCFMT	0x4D800000	RW	Input Source Format	0

CISRCFMT	Bit	Description	Initial State
ITU601_656n	[31]	1 : ITU-R BT.601 YCbCr 8-bit mode enable 0 : ITU-R BT.656 YCbCr 8-bit mode enable	0
UVOffset	[30]	Cb,Cr value offset control. 1 : +128 0 : +0 (normally used)	0
In16bit	[29]	ITU-R BT 601 YCbCr 16-bit mode enable	0
SourceHsize	[28:16]	Source horizontal pixel number (must be 8's multiple) (Also, must be 4's multiple of PreHorRatio_Co if WinOfsEn is 0)	0
Order422	[15:14]	Input YCbCr order inform for input 8bit mode 8-bit mode (In16bit = 0) 00 : YCbYCr 01 : YCrYCb 10 : CbYCrY 11 : CrYCbY	0
Reserved	[13]		0
SourceVsize	[12:0]	Source vertical pixel number	0

WINDOW OPTION REGISTER

Register	Address	R/W	Description	Reset Value
CIWDOFST	0x4D800004	RW	Window offset register	0

CIWDOFST	Bit	Description	Initial State
WinOfsEn	[31]	1 : window offset enable 0 : no offset	0
ClrOvCoFiY	[30]	1 : clear the overflow indication flag of input CODEC FIFO Y 0 : normal	0
Reserved	[29:27]		0
WinHorOfst	[26:16]	Window horizontal offset by pixel unit. (It should be 2's multiple) Caution : SourceHsize-WinHorOfst- WinHorOfst2 should be 8's multiple.	0
ClrOvCoFiCb	[15]	1 : clear the overflow indication flag of input CODEC FIFO Cb 0 : normal	0
ClrOvCoFiCr	[14]	1 : clear the overflow indication flag of input CODEC FIFO Cr 0 : normal	0
ClrOvPrFiCb	[13]	Not used	0
ClrOvPrFiCr	[12]	Not used	0
Reserved	[11]		0
WinVerOfst	[10:0]	Window vertical offset by pixel unit	0

Note. Clear bits should be set by zero after clearing the flags.

Crop Hsize (= SourceHsize – WinHorOfst - WinHorOfst2) must be 4's multiple of PreHorRatio_Co.

Crop Vsize (= SourceVsize – WinVerOfst - WinVerOfst2) must be multiple of PreVerRatio_Co when scale down.

< Example >

Crop Hsize	Permitted Prescale_ratio	PreDstWidth_Co
8n	2	4n
16n	2 or 4	4n
32n	2, 4 or 8	4n

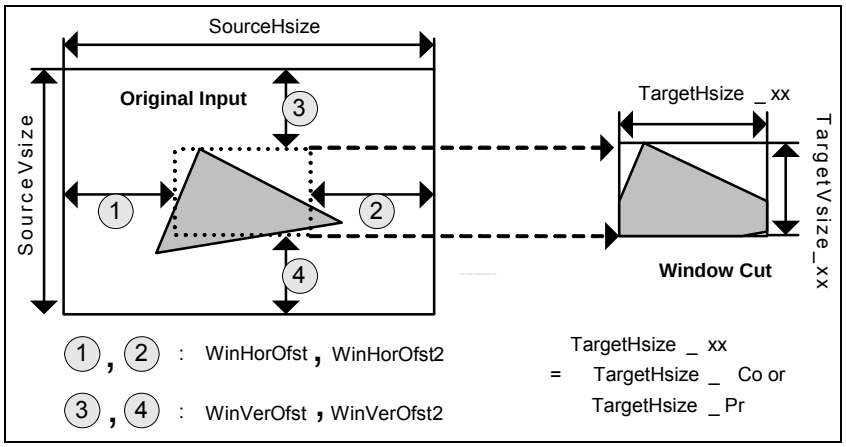


Figure 22-10 Window offset scheme
(WinHorOfst2 & WinVerOfst2 are assigned in the CIWDOFST2 register)

GLOBAL CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
CIGCTRL	0x4D800008	RW	Global control register	0x2000_0000

CIGCTRL	Bit	Description	Initial State
SwRst	[31]	Camera interface software reset. Before setting this bit, you should set the ITU601_656n bit of CISRCFMT as “1” temporarily at first SFR setting. Next sequence is recommended. (ITU601 case : ITU601_656n “1” → SwRst “1” → SwRst “0” for first SFR setting , ITU656 case : ITU601_656n “1” → SwRst “1” → SwRst “0” → ITU601_656n “0” for first SFR setting)	0
CamRst	**[30]**	**External camera processor A Reset or Power Down control**	**0**
Reserved	[29]	Should be ‘1’	1
TestPattern	[28:27]	This register should be set at only ITU-T 601 8-bit mode. Not allowed with input 16-bit mode or ITU-T 656 mode. (max. 1280 X 1024) 00 : external camera processor input (normal) 01 : color bar test pattern 10 : horizontal increment test pattern 11 . vertical increment test pattern	0
InvPolPCLK	[26]	1 : inverse the polarity of PCLK 0 : normal	0
InvPolVSYNC	[25]	1 : inverse the polarity of VSYNC 0 : normal	0
InvPolHREF	[24]	1 : inverse the polarity of HREF 0 : normal	0
Reserved	[23]		0
IRQ_Ovfen	[22]	1 : Overflow interrupt enable (Interrupt is generated during overflow occurrence) 0 : Overflow interrupt disable (normal)	0
Href_mask	[21]	1 : mask out Href during Vsync high 0 : no mask	0
Reserved	[20:0]		0

WINDOW OPTION REGISTER 2

Register	Address	R/W	Description	Reset Value
CIDOWSFT2	0x4D800014	RW	Window option register 2	0

CIWDOFST2	Bit	Description	Initial State
Reserved	[31:27]		0
WinHorOfst2	[26:16]	Window horizontal offset2 by pixel unit. (It should be 2's multiple) Caution : SourceHsize-WinHorOfst- WinHorOfst2 should be 8's multiple.	0
Reserved	[15:11]		0
WinVerOfst2	[10:0]	Window vertical offset2 by pixel unit	0

Y1 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOYSA1	0x4D800018	RW	Y 1st frame start address for codec DMA	0

CICOYSA1	Bit	Description	Initial State
CICOYSA1	[31:0]	Output format : YCbCr 4:2:2 or 4:2:0 → Y 1st frame start address Output format : RGB 16/24 bit → RGB 1st frame start address	0

Y2 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOYSA2	0x4D80001C	RW	Y 2nd frame start address for codec DMA	0

CICOYSA2	Bit	Description	Initial State
CICOYSA2	[31:0]	Output format : YCbCr 4:2:2 or 4:2:0 → Y 2nd frame start address Output format : RGB 16/24 bit → RGB 2nd frame start address	0

Y3 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOYSA3	0x4D800020	RW	Y 3rd frame start address for codec DMA	0

CICOYSA3	Bit	Description	Initial State
CICOYSA3	[31:0]	Output format : YCbCr 4:2:2 or 4:2:0 → Y 3rd frame start address Output format : RGB 16/24 bit → RGB 3rd frame start address	0

Y4 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOYSA4	0x4D800024	RW	Y 4th frame start address for codec DMA	0

CICOYSA4	Bit	Description	Initial State
CICOYSA4	[31:0]	Output format : YCbCr 4:2:2 or 4:2:0 → Y 4th frame start address Output format : RGB 16/24 bit → RGB 4th frame start address	0

CB1 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCBSA1	0x4D800028	RW	Cb 1st frame start address for codec DMA	0

CICOCBSA1	Bit	Description	Initial State
CICOCBSA1	[31:0]	Cb 1st frame start address for codec DMA	0

CB2 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCBSA2	0x4D80002C	RW	Cb 2nd frame start address for codec DMA	0

CICOCBSA2	Bit	Description	Initial State
CICOCBSA2	[31:0]	Cb 2nd frame start address for codec DMA	0

CB3 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCBSA3	0x4D800030	RW	Cb 3rd frame start address for codec DMA	0

CICOCBSA3	Bit	Description	Initial State
CICOCBSA3	[31:0]	Cb 3rd frame start address for codec DMA	0

CB4 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCBSA4	0x4D800034	RW	Cb 4th frame start address for codec DMA	0

CICOCBSA4	Bit	Description	Initial State
CICOCBSA4	[31:0]	Cb 4thframe start address for codec DMA	0

CR1 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCRSA1	0x4D800038	RW	Cr 1st frame start address for codec DMA	0

CICOCRSA1	Bit	Description	Initial State
CICOCRSA1	[31:0]	Cr 1st frame start address for codec DMA	0

CR2 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCRSA2	0x4D80003C	RW	Cr 2nd frame start address for codec DMA	0

CICOCRSA2	Bit	Description	Initial State
CICOCRSA2	[31:0]	Cr 2nd frame start address for codec DMA	0

CR3 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCRSA3	0x4D800040	RW	Cr 3rd frame start address for codec DMA	0

CICOCRSA3	Bit	Description	Initial State
CICOCRSA3	[31:0]	Cr 3rd frame start address for codec DMA	0

CR4 START ADDRESS REGISTER

Register	Address	R/W	Description	Reset Value
CICOCRSA4	0x4D800044	RW	Cr 4th frame start address for codec DMA	0

CICOCRSA4	Bit	Description	Initial State
CICOCRSA4	[31:0]	Cr 4thframe start address for codec DMA	0

CODEC TARGET FORMAT REGISTER

Register	Address	R/W	Description	Reset Value
CICOTRGFMT	0x4D800048	RW	Target image format of codec DMA	0

CICOTRGFMT	Bit	Description	Initial State
In422_Co	[31]	1 : YCbCr 4:2:2 codec scaler input image format. 0 : YCbCr 4:2:0 codec scaler input image format. In this case, horizontal line decimation is performed before codec scaler. (normal)	0
Out422_Co	[30]	1 : YCbCr 4:2:2 codec scaler output image format. This mode is mainly for S/W JPEG. 0 : YCbCr 4:2:0 codec scaler output image format. This mode is mainly for MPEG-4 codec and H/W JPEG DCT.(normal) It must not be set to 0 when In422_Co is set to 0.	0
Interleave_Co	[29]	1 : Interleave ON (support image format YCbCr 4:2:2 only) $Y_0Cb_0Y_1Cr_0Y_2Cb_1Y_3Cr_{1.....}$ 0 : Interleave OFF $Y_0Y_1Y_2Y_{3....}Cb_0Cb_{1....}Cr_0Cr_{1....}$	0
TargetHsize_Co	[28:16]	Horizontal pixel number of target image for codec DMA (16's multiple)	0
FlipMd_Co	[15:14]	Image mirror and rotation for codec DMA 00 : Normal 01 : X-axis mirror 10 : Y-axis mirror 11 : 180° rotation	0
Reserved	[13]		0
TargetVsize_Co	[12:0]	Vertical pixel number of target image for codec DMA	0

TargetHsize_Co and TargetVsize_Co should not be larger than SourceHsize and SourceVsize.

Caution! If TargetVsize_Co value is set to an odd number(N) and output format is YCbCr 4:2:0, The odd number(N) of Y lines and the (N-1)/2 of Cb, Cr lines are generated.

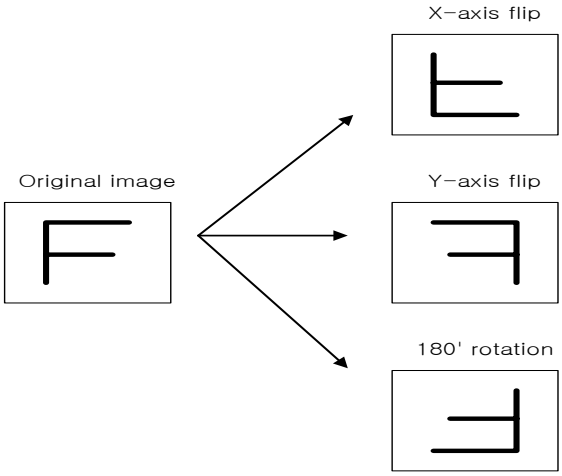


Figure 22-11 Codec image mirror and rotation

CODEC DMA CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
CICOCTRL	0x4D80004C	RW	Codec DMA control related	0

CICOCTRL	Bit	Description	Initial State
Reserved	[31:24]		0
Yburst1_Co	[23:19]	Main burst length for codec Y frames	0
Yburst2_Co	[18:14]	Remained burst length for codec Y frames	0
Cburst1_Co	[13:9]	Main burst length for codec Cb/Cr frames	0
Cburst2_Co	[8:4]	Remained burst length for codec Cb/Cr frames	0
Reserved	[3]		0
LastIRQEn_Co	[2]	1 : enable last IRQ at the end of frame capture (It is recommended to check the done signal of capturing image for JPEG. One pulse) 0 : normal	0
Reserved	[1:0]		0

※ Interleaved burst length (Interleave YCbCr 4:2:2 and RGB output format)

Y burst length	2 , 4 , 8
C burst length (C burst length = Y burst length / 2)	1 , 2 , 4
Wanted burst length (= Y + 2C)	4 , 8 , 16

Note) When Codec output format is YCbCr 4:2:2 interleave ,ScalerBypass_Co = 0 and ScaleUp_V_Co = 1 , Wanted main burst length = 16 and Wanted remained burst length ≠ 16 is not allowed.

※ Non-Interleaved burst length (YCbCr 4:2:0 , YCbCr 4:2:2 non-interleave)

Y	Main burst length = 4, 8, 16	Remained burst length = 4, 8, 16
C	Main burst length = 2, 4, 8, 16	Remained burst length = 2, 4, 8, 16

When output format YCbCr 4:2:2 interleave or RGB, there are some restricts in burst length setting as below.

Y : wanted Main burst length = 2 * Yburst1_Co, and wanted Remained burst length = 2 * Yburst2_Co.

Cb/Cr : wanted Main burst length = Yburst1_Co / 2, and wanted Remained burst length = Yburst2_Co / 2

Example 1. Target image size : QCIF (horizontal Y width = 176 pixels. 1 pixel = 1 Byte)

If output format non-interleave YCbCr 4:2:2,0 (1 word = 4 pixel)

176 / 4 = 44 words , 44 % 8 = 4 → Y main burst = 8, Y remained burst = 4

If output format YCbCr 4:2:2 interleave or RGB565 mode (1 word = 2 pixel)

176 x (1 word / 2 pixles) = 88 words , 88 % 16 = 8 → Wanted main burst = 16, Wanted remained burst = 8

Example 2. Target image size : VGA (horizontal Y width = 640 pixels. 1 pixel = 1 Byte)

If output format non-interleave YCbCr 4:2:2,0 (1 word = 4 pixel)

640 / 4 = 160 word , 160 % 8 = 0 → Y main burst = 8, Y remained burst = 8

If output format Interleave 4:2:2 or RGB565 mode (1 word = 2 pixel)

640 x (1 word / 2 pixel) = 320 words , 320 % 16 = 0 → Wanted main burst = 16, Wanted remained burst = 16

If output format RGB888 mode (1 word = 1 pixel)

640 x (1 word / 1 pixels) = 640 words, 640 % 16 = 0 → Wanted main burst = 16, Wanted remained burst = 16

Example 3. Target image size : QCIF (horizontal C width = 88 pixels. 1 pixel = 1 Byte)

If output format non-interleave YCbCr 4:2:2,0 (1 word = 4 pixel)

88 / 4 = 22 word. , 22 % 4 = 2 → main burst = 4, remained burst = 2 (HTRANS==INCR)

Caution! Camera I/F generate INCR (HBURST of AMBA) transfer type at abnormal burst length as 2, and at crossing 1024 address boundary by burst transfer. System controller including FIMC2.2, must support to treat INCR burst as several single transfer accesses. Watch over your memory controller and system arbiter specification!

REGISTER SETTING GUIDE FOR CODEC SCALER

SRC_Width and DST_Width satisfy the word boundary constraints such that the number of horizontal pixel can be represented to kn where n = 1,2,3, … and k = 8 for YCbCr420 image, respectively. TargetHsize should not be larger than SourceHsize. Similarly, TargetVsize should not be larger than SourceVsize.

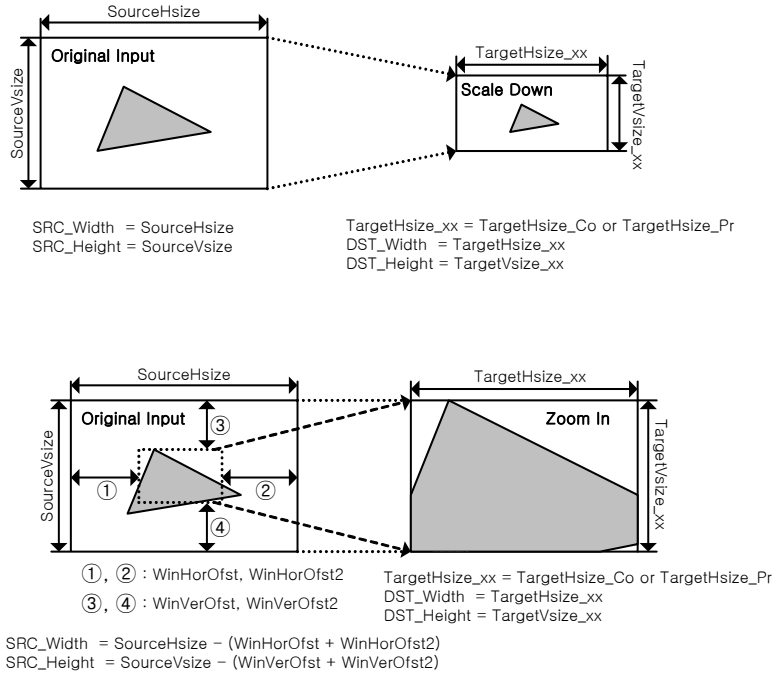


Figure 22-12 Scaling scheme

The other control registers of pre-scaled image size, pre-scale ratio, pre-scale shift ratio and main scale ratio are defined according to the following equations.

```
If ( SRC_Width >= 64 × DST_Width ) {  Exit(-1);  /* Out Of Horizontal Scale Range */  }
else if (SRC_Width >= 32 × DST_Width) { PreHorRatio_xx = 32;  H_Shift = 5; }
else if (SRC_Width >= 16 × DST_Width) { PreHorRatio_xx = 16;  H_Shift = 4; }
else if (SRC_Width >= 8 × DST_Width) { PreHorRatio_xx = 8;  H_Shift = 3; }
else if (SRC_Width >= 4 × DST_Width) { PreHorRatio_xx = 4;  H_Shift = 2; }
else if (SRC_Width >= 2 × DST_Width) { PreHorRatio_xx = 2;  H_Shift = 1; }
else { PreHorRatio_xx = 1;  H_Shift = 0; }
PreDstWidth_xx = SRC_Width / PreHorRatio_xx;
MainHorRatio_xx = ( SRC_Width << 8 ) / ( DST_Width << H_Shift);

If ( SRC_Height >= 64 × DST_Height ) {  Exit(-1);  /* Out Of Vertical Scale Range */  }
else if (SRC_Height >= 32 × DST_Height) { PreVerRatio_xx = 32;  V_Shift = 5; }
```

else if (SRC_Height >= 16 × DST_Height) { PreVerRatio_xx = 16; V_Shift = 4; }

else if (SRC_Height >= 8 × DST_Height) { PreVerRatio_xx = 8; V_Shift = 3; }

else if (SRC_Height >= 4 × DST_Height) { PreVerRatio_xx = 4; V_Shift = 2; }

else if (SRC_Height >= 2 × DST_Height) { PreVerRatio_xx = 2; V_Shift = 1; }

else { PreVerRatio_xx = 1; V_Shift = 0; }
PreDstHeight_xx = SRC_Height / PreVerRatio_xx;
MainVerRatio_xx = (SRC_Height << 8) / (DST_Height << V_Shift);

SHfactor_xx = 10 – (H_Shit + V_Shift);
SRC_width and SRC_Height should be the multiple of 8.

Caution! In Zoom-In case, you should check the next equation.

((SourceHsize – (WinHorOfst + WinHorOfst2)) / PreHorRatio_Pr) <= 320

CODEC PRE-SCALER CONTROL REGISTER 1

Register	Address	R/W	Description	Reset Value
CICOSCPRERATIO	0x4D800050	RW	Codec pre-scaler ratio control	0

CICOSCPRERATIO	Bit	Description	Initial State
SHfactor_Co	[31:28]	Shift factor for codec pre-scaler	0
Reserved	[27:23]		0
PreHorRatio_Co	[22:16]	Horizontal ratio of codec pre-scaler	0
Reserved	[15:7]		0
PreVerRatio_Co	[6:0]	Vertical ratio of codec pre-scaler	0

CODEC PRE-SCALER CONTROL REGISTER 2

Register	Address	R/W	Description	Reset Value
CICOSCPREDST	0x4D800054	RW	Codec pre-scaler destination format	0

CICOSCPREDST	Bit	Description	Initial State
Reserved	[31:28]		0
PreDstWidth_Co	[27:16]	Destination width for codec pre-scaler	0
Reserved	[15:12]		0
PreDstHeight_Co	[11:0]	Destination height for codec pre-scaler	0

CODEC MAIN-SCALER CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
CICOSCCTRL	0x4D800058	RW	Codec main-scaler control	0

CICOSCCTRL	Bit	Description	Initial State
ScalerBypass_Co	[31]	Codec scaler bypass for upper 2048 x 2048 size (In this case, ImgCptEn_CoSC should be 0, but ImgCptEn should be 1. It is not allowed to capturing preview image. This mode is intended to capture JPEG input image for DSC application) In this case, input pixel buffering depends on only input FIFOs, so system bus should be not busy in this mode.	0
ScaleUp_H_Co	[30]	Horizontal scale up/down flag for codec scaler (In 1:1 scale ratio, this bit should be “1”) 1: up, 0:down	0
ScaleUp_V_Co	[29]	Vertical scale up/down flag for codec scaler (In 1:1 scale ratio, this bit should be “1”) 1: up, 0:down	0
Reserved	[28:25]		0
MainHorRatio_Co	[24:16]	Horizontal scale ratio for codec main-scaler	0
CoScalerStart	[15]	Codec scaler start	0
Reserved	[14:9]		0
MainVerRatio_Co	[8:0]	Vertical scale ratio for codec main-scaler	0

CODEC DMA TARGET AREA REGISTER

Register	Address	R/W	Description	Reset Value
CICOTAREA	0x4D80005C	RW	Codec pre-scaler destination format	0

CICOTAREA	Bit	Description	Initial State
Reserved	[31:26]		0
CICOTAREA	[25:0]	Target area for codec DMA = Target H size x Target V size	0

CODEC STATUS REGISTER

Register	Address	R/W	Description	Reset Value
CICOSTATUS	0x4D800064	R	Codec path status	0

CICOSTATUS	Bit	Description	Initial State
OvFiY_Co	[31]	Overflow state of codec FIFO Y	0
OvFiCb_Co	[30]	Overflow state of codec FIFO Cb	0
OvFiCr_Co	[29]	Overflow state of codec FIFO Cr	0
VSYNC	[28]	Camera VSYNC (This bit can be referred by CPU for first SFR setting after external camera muxing. And, it can be seen in the ITU-R BT 656 mode)	0
FrameCnt_Co	[27:26]	Frame count of codec DMA (This counter value means the next frame number)	0
WinOfstEn_Co	[25]	Window offset enable status	0
FlipMd_Co	[24:23]	Flip mode of codec DMA	0
ImgCptEn_CamIf	[22]	Image capture enable of camera interface	0
ImgCptEn_CoSC	[21]	Image capture enable of codec path	0
VSYNC_A	[20]	External camera A VSYNC (polarity inversion was not adopted.)	x
VSYNC_B	[19]	External camera B VSYNC (polarity inversion was not adopted.)	x
Reserved	[18:0]		0

COLOR SPACE DYNAMIC RANGE REGISTER

Register	Address	R/W	Description	Reset Value
CICSCRAN	0x4D80007C	RW	Dynamic Range for the CSC	0x8000_0000

CICSCRAN	Bit	Description	Initial State
CSCRange	[31:30]	YCbCr Input Data Dynamic Range Selection for the Color Space Conversion 2'b11 : Forbidden 2'b10 : 0 < Y/Cb/Cr <255 (Recommended) 2'b01 : 16 <= Y <= 235, 16 <= Cb/Cr <= 240 2'b00 : Reserved	10
Reserved	[29:0]		0

IMAGE CAPTURE ENABLE REGISTER

Register	Address	R/W	Description	Reset Value
CIIMGCPT	0x4D8000A0	RW	Image capture enable command	0

This register must be set at last.

CIIMGCPT	Bit	Description	Initial State
ImgCptEn	[31]	Camera interface global capture enable	0
ImgCptEn_CoSc	[30]	Capture enable for codec scaler. This bit must be zero in scaler-bypass mode.	0
ImgCptEn_PrSc	[29]	Not used	0
Reserved	[28:27]		0
Cpt_CoDMA_Sel	[26]	Codec DMA output format 1 : RGB 16/24 bit (Must be Out422_Co=1 , Interleave_Co=1) 0 : YCbCr 4:2:2 or 4:2:0	0
Cpt_CoDMA_RGB FMT	[25]	Codec DMA RGB format 1 : RGB 24 bit 0 : RGB 16 bit	0
Cpt_CoDMA_En	[24]	Capture codec dma frame control. It is also used for start signal of Codec image capture. Therefore, it must be set to 1 if codec image is wanted. 1 : Enable 0 : Disable	0
Cpt_CoDMA_Ptr	[23:19]	Capture sequence turn-around pointer	0
Cpt_CoDMA_Mod	[18]	Capture codec dma mode 1 : Apply Cpt_CoDMA_Cnt mode (capture frames along the Cpt_CoDMA_Seq during Cpt_CoDMA_En is high until Cpt_CoDMA_Cnt = 0) 0 : Apply Cpt_CoDMA_En mode (capture frames along the Cpt_CoDMA_Seq during Cpt_CoDMA_En is high)	0
Cpt_CoDMA_Cnt	[17:10]	Wanted number of frames to be captured (This value is down-counted when a frame is captured.)	0
Reserved	[9:0]		0

※ Start register order. start register should be set at last other registers.

CoScalerStart → Cpt_CoDMA_En → ImgCptEn_CoSc → ImgCptEn

CODEC CAPTURE SEQUENCE REGISTER

Register	Address	R/W	Description	Reset Value
CICOCPTSEQ	0x4D8000A4	RW	Codec dma capture sequence related	0xFFFF_FFFF

CICOCPTSEQ	Bit	Description	Initial State
Cpt_CoDMA_Seq	[31:0]	Capture sequence pattern in Codec DMA	0xFFFF_FFFF

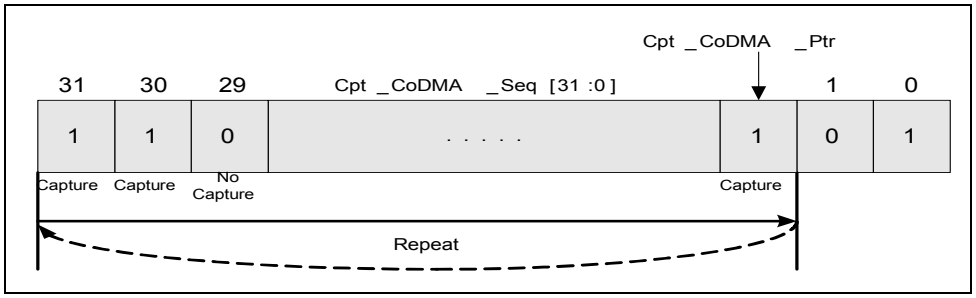


Figure 22-13 Capture codec dma frame control

CODEC SCAN LINE OFFSET REGISTER

Register	Address	R/W	Description	Reset Value
CICOSCOS	0x4D8000A8	RW	Codec scan line offset related	0

CICOSCOS	Bit	Description	Initial State
Reserved	[31:29]		0
Initial_offset_Co	[28:16]	The number of the skipped pixels for initial offset (should be even number for word boundary alignment). This value must be set to 0 when scanline offset is not used. And, scanline offset can be used only when Interleave_Co is set to 1.	0
Reserved	[15:13]		0
Line_offset_Co	[12:0]	The number of the skipped pixels in the screen of the target image when scan line is changed (should be even number for word boundary alignment). This value must be set to 0 when scanline offset is not used. And, scanline offset can be used only when Interleave_Co is set to 1.	0

※ Scan line offset is allowed only when the output pixel format of codec path is Interleaved YCbCr422.

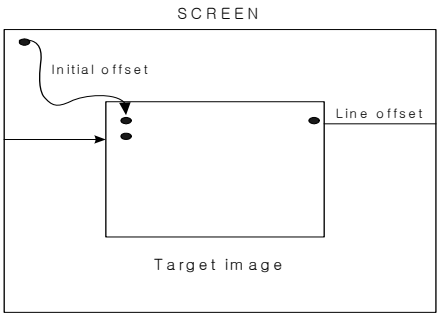


Figure 22-14 Scan line offset

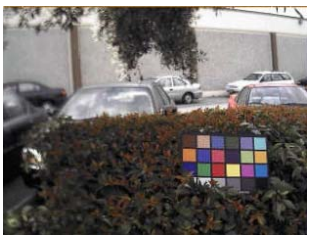
IMAGE EFFECTS REGISTER

Register	Address	R/W	Description	Reset Value
CIIMGEFF	0x4D8000B0	RW	Image Effects related	0x0010_0080

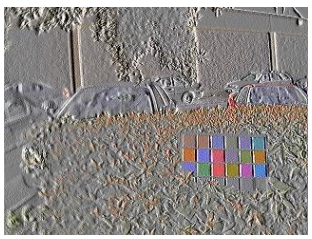
CIIMGEFF	Bit	Description	Initial State
Reserved	[31:29]		0
FIN	[28:26]	Image Effect selection 3'd0 : Bypass 3'd1 : Arbitrary Cb/Cr 3'd2 : Negative 3'd3 : Art Freeze 3'd4 : Embossing 3'd5 : Silhouette	0
Reserved	[25:21]		0
PAT_Cb	[20:13]	It is used only for FIN is Arbitrary Cb/Cr (PAT_Cb/Cr == 8'd128 for GRAYSCALE) 16 ≤ PAT_Cb ≤ 223	0x80
Reserved	[12:8]		0
PAT_Cr	[7:0]	It is used only for FIN is Arbitrary Cb/Cr (PAT_Cb/Cr == 8'd128 for GRAYSCALE) 16 ≤ PAT_Cr ≤ 223	0x80

Cf) Sepia : PAT_Cb == 8'd115 , PAT_Cr == 8'd145

Original Arbitrary(sepia) Negative



Art freeze Embossing Silhouette


Note) Minimum Timing Requirements

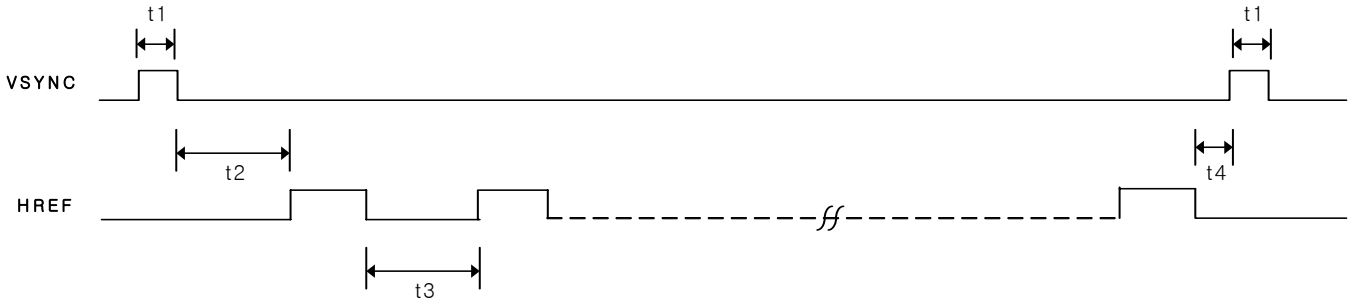


Figure 22-15 Sync Signal Timing Diagram

	Minimum	Maximum
t1	12 cycles of Pixel clock	-
t2	12 cycles of Pixel clock	-
t3	2 cycles of Pixel clock	-
t4	12 cycles of Pixel clock	-

Table 22-2. Sync signal timing requirement

23 ATA CONTROLLER

INTRODUCTION

S3C2413X has ATA controller which is compatible with the ATA/ATAPI-6 standard.
Detailed features are the followings

- compatible with the ATA/ATAPI-6 standard.
- 30 word-sized (32bits) Special Function Registers.
- Only 1 FIFO
- When read operation, the FIFO depth & size is “16 x 32-bit”.
- When write operation, the FIFO depth & size is “32 x 16-bit”.
- It support True-IDE mode in CF card, but don’t support hot-plug-in.
- It support “PIO mode” or “PDMA mode”, but don’t support “UDMA mode”.
- “PDMA mode” is PIO mode using DMA controller in ATA controller
- (from ATA device to memory / from memory to ATA device).
- DMA controller in ATA controller support only 8 burst-word size transfer.

BLOCK DIAGRAM

Figure 23-1 shows the block diagram of ATA Controller

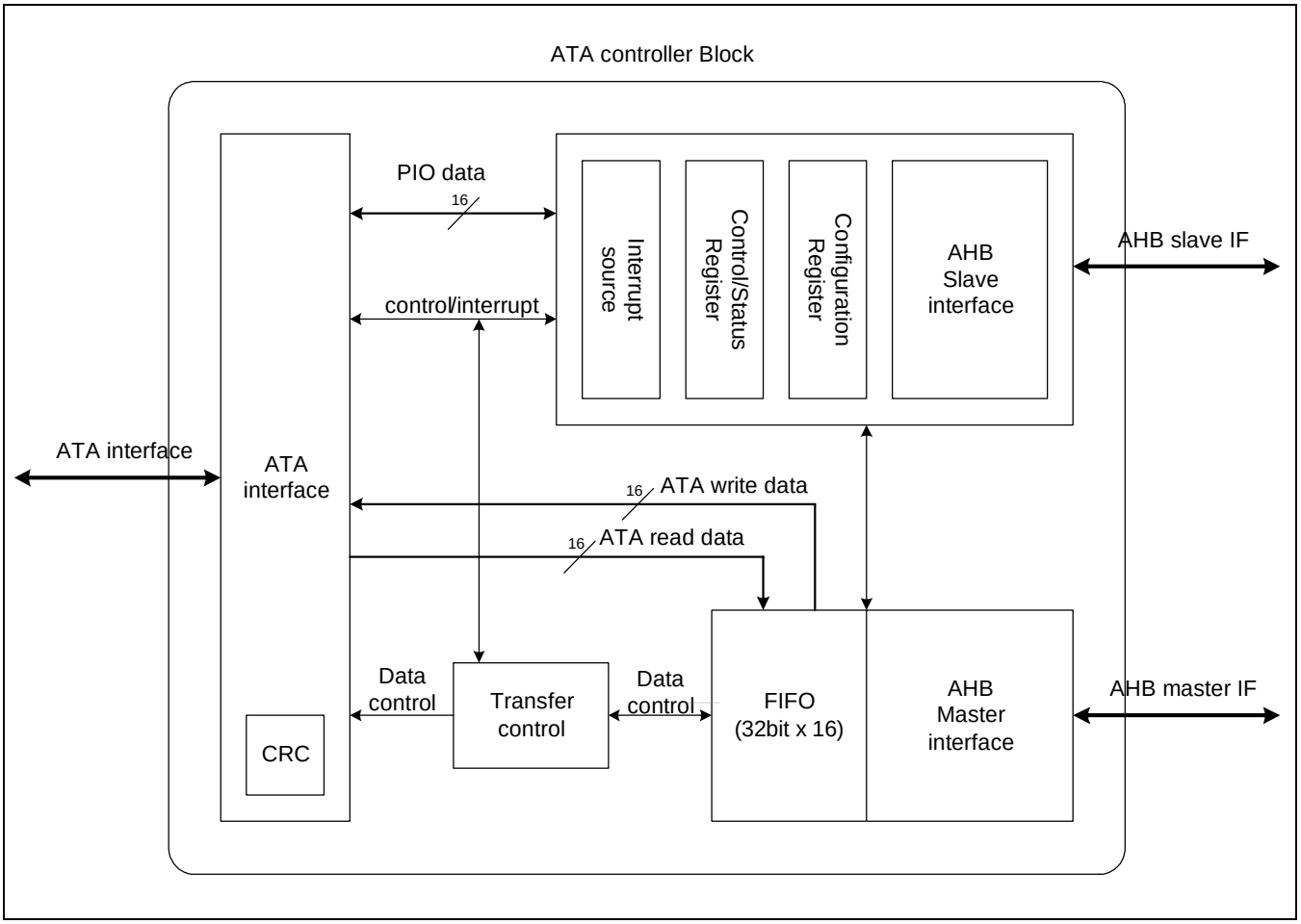


Figure 23-1. ATA Controller Top Block Diagram

BASIC FUNCTION FLOWCHART

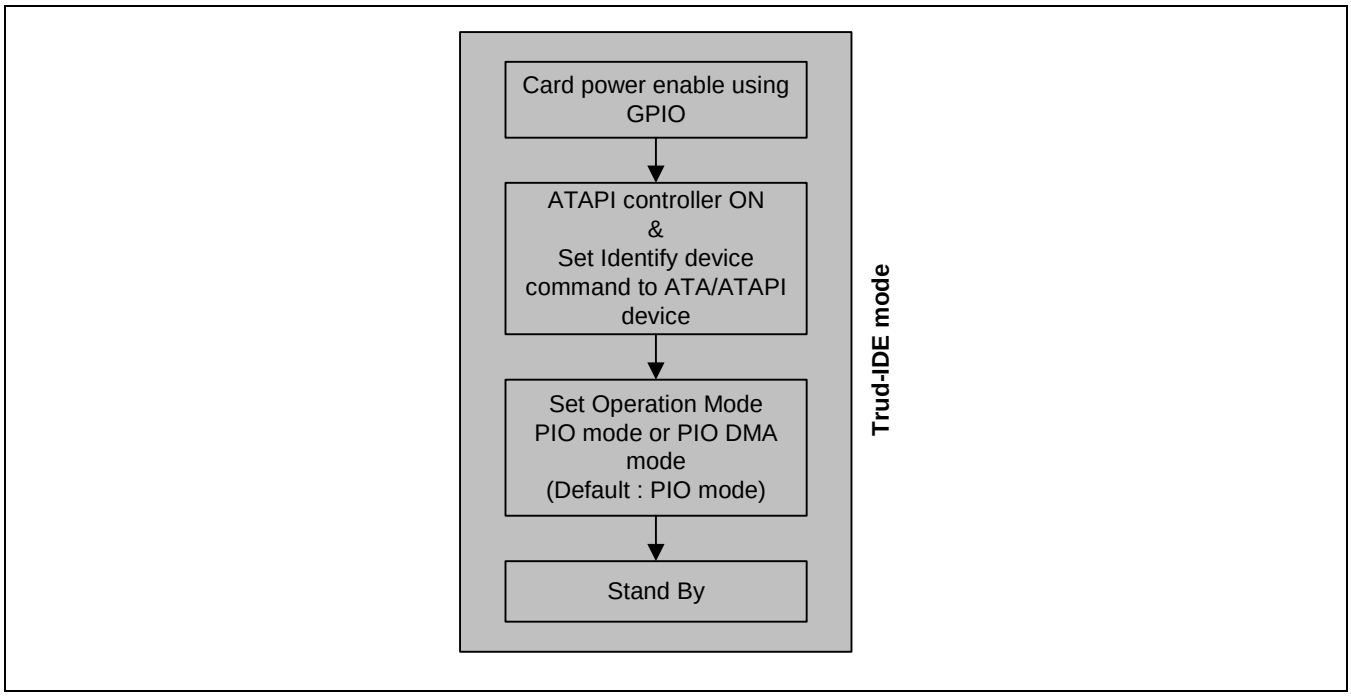


Figure 23-2. ATA Controller Basic Function Flow Chart

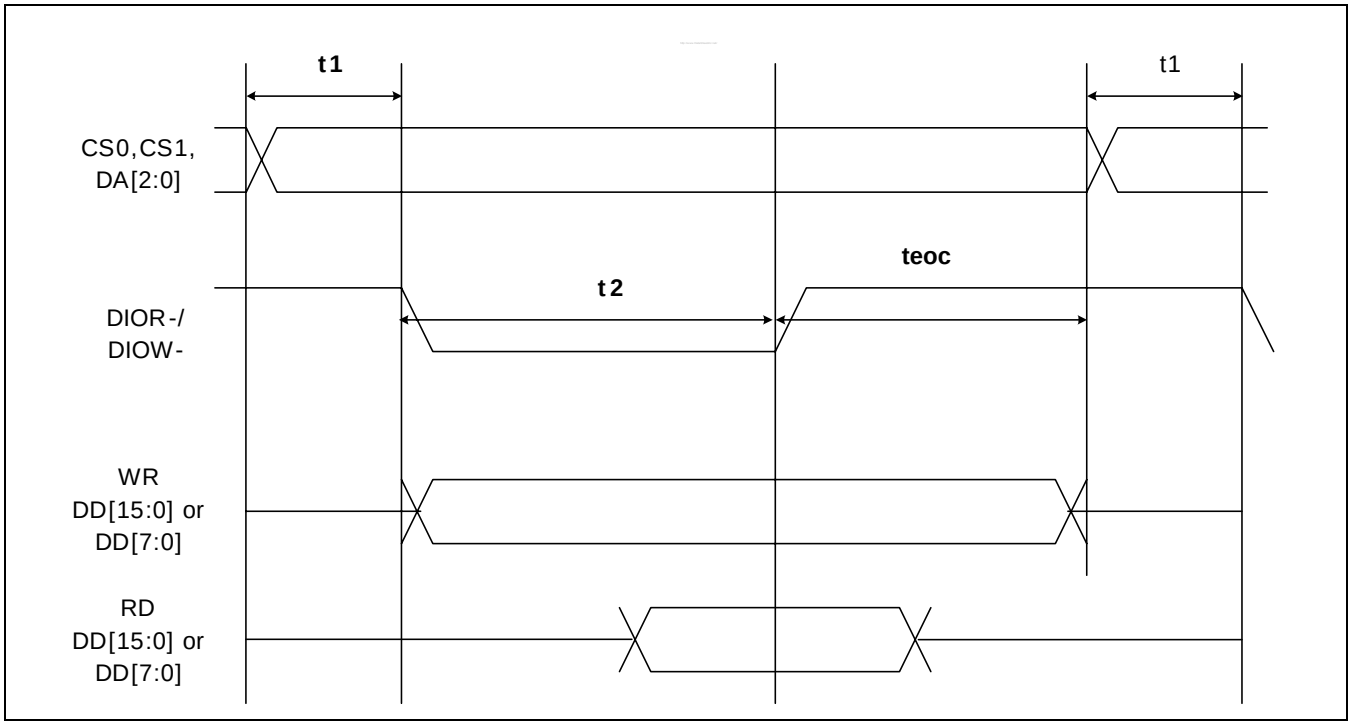


Figure 23-3. ATA Controller Basic Function Flow Chart

Table 23-1. Timing Parameter Each PIO Mode

PIO mode	PIO 0	PIO 1	PIO 2	PIO 3	PIO 4
T1	(70, --)	(50, --)	(30, --)	(30, --)	(25, --)
T2 (16-bit)	(165, --)	(125, --)	(100, --)	(80, --)	(70, --)
T2 Register (8-bit)	(290, --)	(290, --)	(290, --)	(80, --)	(70, --)
TEOC	(20, --)	(15, --)	(10, --)	(10, --)	(10, --)
T1 + T2 + TEOC	(600, --)	(383, --)	(240, --)	(180, --)	(120, --)

ATA_CONTROL CONFIGURATION REGISTER

Register	Address	R/W	Description	Reset Value
ATA_CONTROL	0x4B800000	R/W	ATA_CONTROL register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:2]	Reserved	0
Clk_down_ready	[1]	Status for clock down (Read only) This bit is asserted in idle state when ATA_CONTROL bit [0] is zero. 0 : not ready for clock down 1 : ready for clock down	0
ata_enable	[0]	ATA enable 0 : ATA is disabled and preparation for clock down maybe in progress 1 : ATA is enabled.	0

ATA_STATUS REGISTER

Register	Address	R/W	Description	Reset Value
ATA_STATUS	0x4B800004	R	ATA_STATUS register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:5]	Reserved	0
atadev_irq	[4]	ATA interrupt signal line	0
atadev_iordy	[3]	ATA iordy signal line	0
atadev_dmareq	[2]	ATA dmareq signal line	0
xfr_state	[1:0]	Transfer state 00 : idle state 01 : transfer state 11 : wait for completion state	0

ATA_COMMAND

Register	Address	R/W	Description	Reset Value
ATA_COMMAND	0x4B800008	R/W	ATA_COMMAND register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:2]	Reserved bits	0
xfr_command	[1:0]	ATA transfer command Four command types (START, STOP, ABORT and CONTINUE) are supported for data transfer control. The “START” command is used to start data transfer. The “STOP” command can pause transfer temporarily. The “CONTINUE” command shall be used after “STOP” command or internal state of “pause” when track buffer is full. The “ABORT” command terminated current data transfer sequences and make ATA host controller move to idle state. 00 : command stop 01 : command start (Only available in idle state) 10 : command abort 11 : command continue (Only available in transfer pause)	0

ATA_ SWRST

Register	Address	R/W	Description	Reset Value
ATA_SWRST	0x4B80000C	R/W	ATA_SWRST register	0x0000_0001

BANKCFG	Bit	Description	Initial State
Reserved	[31:1]	Reserved bits	0
ata_swrstn	[0]	Software reset for the ATA host 0: No reset 1: Software reset for all ATA host module.	1

ATA_ IRQ

Register	Address	R/W	Description	Reset Value
ATA_IRQ	0x4B800010	R/W	ATA_IRQ register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:5]	Reserved bits	0
sbuf_empty_int	[4]	When source buffer is empty. CPU can clear this interrupt by writing “1”.	0
tbuf_full_int	[3]	When track buffer is half full. CPU can clear this interrupt by writing “1”.	0
atadev_irq_int	[2]	When ATA device generates interrupt. CPU can clear this interrupt by writing “1”.	0
Reserved	[1]	Reserved bits	0
xfr_done_int	[0]	When all data transfers are finished. CPU can clear this interrupt by writing “1”.	0

ATA_ IRQ_MASK

Register	Address	R/W	Description	Reset Value
ATA_IRQ_MASK	0x4B800014	R/W	ATA_IRQ MASK register	**0x0000_001F**

BANKCFG	Bit	Description	Initial State
Reserved	[31:5]	Reserved bits	0
sbuf_empty_int	[4]	**Interrupt mask bit of source buffer empty** **0 : unmask 1 : mask**	**0x1**
tbuf_full_int	[3]	**Interrupt mask bit of source buffer empty** **0 : unmask 1 : mask**	**0x1**
atadev_irq_int	[2]	**Interrupt mask bit of source buffer empty** **0 : unmask 1 : mask**	**0x1**
Reserved	[1]	**Interrupt mask bit of source buffer empty** **0 : unmask 1 : mask**	**0x1**
xfr_done_int	[0]	**Interrupt mask bit of source buffer empty** **0 : unmask 1 : mask**	**0x1**

ATA_ CFG

Register	Address	R/W	Description	Reset Value
ATA_CFG	0x4B800018	R/W	ATA_CFG register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:9]	Reserved bits	0
sbuf_full_mode	[8]	Determines whether to continue automatically when source buffer is empty. This bit should not be changed during runtime operation. 0: continue automatically with new source buffer address. 1: stay in pause state and wait for CPU's action.	0
tbuf_full_mode	[7]	Determines whether to continue automatically when track buffer is full. This bit should not be changed during runtime operation. 0: continue automatically with new track buffer address. 1: stay in pause state and wait for CPU's action.	0
byte_swap	[6]	Determines whether data endian is little or big in 16bit data. 0 : little endian (data[15:8], data[7:0]) 1 : big endian (data[7:0], data[15:8])	0
atadev_irq_al	[5]	Device interrupt signal level 0: active high 1: active low	0
dma_dir	[4]	DMA transfer direction 0 : Host read data from device 1 : Host write data to device	0
ata_class	[3:2]	ATA transfer class select 00 : transfer class is PIO 01 : transfer class is PIO DMA	0
ata_iordy_en	[1]	Determines whether IORDY input can extend data transfer. 0 : IORDY disable(ignored) 1 : IORDY enable (can extend)	0
ata_rst	[0]	ATA device reset by this host. 0 : no reset 1 : reset	0

ATA_PIO_TIME

Register	Address	R/W	Description	Reset Value
ATA_PIO_TIME	0x4B80002C	R/W	ATA_PIO_TIME register	0x0001_C238

BANKCFG	Bit	Description	Initial State
Reserved	[31:20]	Reserved bits	0
pio_teoc	[19:12]	PIO timing parameter, teoc, end of cycle time It shall not have zero value.	1
pio_t2	[11:4]	PIO timing parameter, t2, DIOR/Wn pulse width It shall not have zero value.	0x23
pio_t1	[3:0]	PIO timing parameter, t1, address valid to DIOR/Wn	0x08

ATA_XFR_NUM

Register	Address	R/W	Description	Reset Value
ATA_XFR_NUM	0x4B800034	R/W	ATA_XFR_NUM register	0x0000_0000

BANKCFG	Bit	Description	Initial State
xfr_num	[31:1]	Data transfer number.	0
Reserved	[0]	Reserved bits	0

ATA_XFR_CNT

Register	Address	R/W	Description	Reset Value
ATA_XFR_CNT	0x4B800038	R/W	ATA_XFR_CNT register	0x0000_0000

BANKCFG	Bit	Description	Initial State
xfr_cnt	[31:1]	Current remaining transfer counter. This value counts down from ATA_XFR_NUM. It goes to zero when pre-defined all data has been transferred.	0
Reserved	[0]	Reserved bits	0

ATA_TBUF_START

Register	Address	R/W	Description	Reset Value
ATA_TBUF_ START	0x4B80003C	R/W	ATA_TBUF_START register	0x0000_0000

BANKCFG	Bit	Description	Initial State
track_buffer_start	[31:2]	Start address of track buffer (4byte unit)	0
Reserved	[1:0]	Reserved bits	0

ATA_TBUF_SIZE

Register	Address	R/W	Description	Reset Value
ATA_TBUF_SIZE	0x4B800040	R/W	ATA_TBUF_SIZE register	0x0000_0000

BANKCFG	Bit	Description	Initial State
track_buffer_size	[31:5]	Size of track buffer (32byte unit)	0
Reserved	[4:0]	Reserved bits	0

ATA_SBUF_START

Register	Address	R/W	Description	Reset Value
ATA_SBUF_ START	0x4B800044	R/W	ATA_SBUF_START register	0x0000_0000

BANKCFG	Bit	Description	Initial State
src_buffer_start	[31:2]	Start address of source buffer (4byte unit)	0
Reserved	[1:0]	Reserved bits	0

ATA_SBUF_SIZE

Register	Address	R/W	Description	Reset Value
ATA_SBUF_SIZE	0x4B800048	R/W	ATA_SBUF_SIZE register	0x0000_0000

BANKCFG	Bit	Description	Initial State
src_buffer_size	[31:5]	Size of source buffer (32byte unit)	0
Reserved	[4:0]	Reserved bits	0

ATA_CADDR_TBUR

Register	Address	R/W	Description	Reset Value
ATA_CADDR_ TBUR	0x4B80004C	R/W	ATA_ CADDR_TBUR register	0x0000_0000

BANKCFG	Bit	Description	Initial State
track_buf_cur_adr	[31:2]	Current address of track buffer	0
Reserved	[1:0]	Reserved bits	0

ATA_CADDR_SBUF

Register	Address	R/W	Description	Reset Value
ATA_CADDR_ SBUF	0x4B800050	R/W	ATA_ CADDR_SBUF register	0x0000_0000

BANKCFG	Bit	Description	Initial State
src_buf_cur_adr	[31:2]	Current address of source buffer	0
Reserved	[1:0]	Reserved bits	0

ATA_PIO_DTR

Register	Address	R/W	Description	Reset Value
ATA_PIO_DTR	0x4B800054	R/W	ATA_PIO_DTR register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:16]	Reserved bits	0
pio_dev_dtr	[15:0]	16-bit PIO data register	0

ATA_PIO_FED

Register	Address	R/W	Description	Reset Value
ATA_PIO_FED	0x4B800058	R/W	ATA_PIO_FED register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:8]	Reserved bits	0
pio_dev_fed	[7:0]	8-bit PIO device feature/error (command block) register	0

ATA_PIO_SCR

Register	Address	R/W	Description	Reset Value
ATA_PIO_SCR	0x4B80005C	R/W	ATA_PIO_SCR register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:8]	Reserved bits	0
pio_dev_scr	[7:0]	8-bit PIO device sector count (command block) register	0

ATA_PIO_LLR

Register	Address	R/W	Description	Reset Value
ATA_PIO_LLR	0x4B800060	R/W	ATA_PIO_LLR register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:8]	Reserved bits	0
pio_dev_llr	[7:0]	8-bit PIO device LBA low (command block) register	0

ATA_PIO_LMR

Register	Address	R/W	Description	Reset Value
ATA_PIO_LMR	0x4B800064	R/W	ATA_PIO_LMR register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:8]	Reserved bits	0
pio_dev_lmr	[7:0]	8-bit PIO device LBA middle (command block) register	0

ATA_PIO_LHR

Register	Address	R/W	Description	Reset Value
ATA_PIO_LHR	0x4B800068	R/W	ATA_PIO_LHR register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:8]	Reserved bits	0
pio_dev_lhr	[7:0]	8-bit PIO LBA high (command block) register	0

ATA_PIO_DVR

Register	Address	R/W	Description	Reset Value
ATA_PIO_DVR	0x4B80006C	R/W	ATA_PIO_DVR register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:8]	Reserved bits	0
pio_dev_dvr	[7:0]	8-bit PIO device (command block) register	0

ATA_PIO_CSD

Register	Address	R/W	Description	Reset Value
ATA_PIO_CSD	0x4B800070	R/W	ATA_PIO_CSD register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:8]	Reserved bits	0
pio_dev_csd	[7:0]	8-bit PIO device command/status (command block) register	0

ATA_PIO_DAD

Register	Address	R/W	Description	Reset Value
ATA_PIO_DAD	0x4B800074	R/W	ATA_PIO_DAD register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:8]	Reserved bits	0
pio_dev_dad	[7:0]	8-bit PIO device control/alternate status (control block) register	0

ATA_PIO_READY

Register	Address	R/W	Description	Reset Value
ATA_PIO_READY	0x4B800078	R	ATA_PIO_READY register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:2]	Reserved bits	0
dev_acc_ready	[1]	Indicates whether host can start access to device register 0 : not ready to start access ATA device register 1 : ready to start access ATA device register	0
pio_data_ready	[0]	Indicates whether data is valid in ATA_PIO_DATA register 0 : no valid data in ATA_PIO_DATA register 1 : valid data in ATA_PIO_DATA register	0

ATA_PIO_RDATA

Register	Address	R/W	Description	Reset Value
ATA_PIO_RDATA	0x4B80007C	R/W	ATA_PIO_RDATA register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:16]	Reserved bits	0
pio_rdata	[15:0]	PIO read data register while HOST read from ATA device register	0

BUS_FIFO_STATUS

Register	Address	R/W	Description	Reset Value
BUS_FIFO_ STATUS	0x4B800090	R	BUS_FIFO_STATUS register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31:19]	Reserved bits	0
bus_state	[18:16]	000 : IDLE 001 : BUSYW 010 : PREP 011 : BUSYR 100 : PAUSER 101 : PAUSEW	0
Reserved	[15:14]	Reserved bits	0
bus_fifo_rdpnt	[13:8]	bus fifo read pointer	0
Reserved	[7:6]	Reserved bits	0
bus_fifo_wrpnt	[5:0]	bus fifo write pointer	0

ATA_FIFO_STATUS

Register	Address	R/W	Description	Reset Value
ATA_FIFO_ STATUS	0x4B800094	R	ATA_FIFO_STATUS register	0x0000_0000

BANKCFG	Bit	Description	Initial State
Reserved	[31]	Reserved bits	0
ata_state	[30:28]	PIO read data register while HOST read from ATA device register	0
pio_state	[27:26]	00 : IDLE 01 : T1 10 : T2 11 : TEOC	0
pdma_state	[25:24]	00 : IDLE 01 : T1 10 : T2 11 : TEOC	0
Reserved	[23:21]	Reserved bits	0
Reserved	[20:0]	Reserved bits	0

24 ELECTRICAL DATA

ABSOLUTE MAXIMUM RATINGS

Table 24-1. Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	VDDI, VDDIARM, VDDALIVE, VDDI_MPLL, VDDI_UPLL	-0.5	1.8	V
	VDDOP1/2/3/4	-0.5	4.8	
	RTCVDD	-0.5	4.8	
	VDDMOP	-0.5	4.8	
	VDDA_ADC	-0.5	4.8	
DC Input Voltage	VIN	-0.5	4.8	
DC Output Voltage	VOUT	-0.5	4.8	
DC Input Current	IIN	± 200		mA
Storage Temperature	TSTG	– 65 to 150		°C

RECOMMENDED OPERATING CONDITIONS

Table 24-2. Recommended Operating Conditions(266MHz)

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage for Alive Block	VDDALIVE	1.15	1.25	1.5	V
DC Supply Voltage for internal	VDDI VDDI_MPLL VDDI_UPLL	1.15	1.25	1.5	
DC Supply Voltage for ARM Core	VDDIARM*	1.3	1.4	1.5	
DC Supply Voltage for I/O Block	VDDOP1,2	2.3	2.5V / 2.8V / 3.3V	3.6	
	VDDOP3,4	3.0	3.3V	3.6	
DC Supply Voltage for Memory Interface	VDDMOP	1.7	1.8V / 2.5V / 3.3V	3.6	
DC Supply Voltage for RTC	RTCVDD	2.5V	3.0V	3.6	
DC Supply Voltage for ADC	VDDA_ADC	3.3-5%	3.3 V	3.3+5%	
DC Input Voltage	VIN	3.0	3.3 V	3.6	
		2.3	2.5 V	2.7	
		1.7	1.8 V	1.9	
DC Output Voltage	VOUT	3.0	3.3 V	3.6	
		2.3	2.5 V	2.7	
		1.7	1.8 V	1.9	
Operating Temperature	TA	Commercial	0 to 70		^{o}C
		Industrial	-40 to 85		^{o}C

NOTES:

1. VDDMOP includes VDDMOP1, VDDMOP2, VDDMOP3, VDDMOP4, VDDMOP5, VDDMOP6, VDDMOP7.
2. DC input/output voltage is depend on the voltage of IO supply voltage corresponding IOs.
3. Load Capacitance (CL) < 50pF. If max CL is changed, above operation conditions must be changed.

*: The specification especially related with VDDIARM is a preliminary. So, It can be changed.

D.C. ELECTRICAL CHARACTERISTICS

Table 24-3. Normal I/O PAD DC Electrical Characteristics

(VDDOP* = 3.3V ± 0.3V, TA = -40 to 85°C)

Symbol	Parameters	Condition	Min	Typ	Max	Unit
VIH	High level input voltage					
	LVCMOS interface		2.0			V
VIL	Low level input voltage					
	LVCMOS interface				0.8	V
VT	Switching threshold			$0.5V_{DD}$		V
VT+	Schmitt trigger, positive-going threshold	CMOS			2.0	V
VT-	Schmitt trigger, negative-going threshold	CMOS	0.8			V
IIH	High level input current					
	Input buffer	VIN = VDD	-10		10	µA
	Input buffer with pull-down		10	33	71	
IIL	Low level input current					
	Input buffer	VIN = VSS	-10		10	µA
	Input buffer with pull-up		-71	-33	-10	
VOH	High level output voltage					
	Type B2 to B12	IOH= - 1uA	V_{DD} - 0.05			V
	Type B2	IOH= - 2mA	2.4			
	Type B4	IOH= - 4mA				
	Type B8	IOH = -8 mA				
	Type B12	IOH = -12 mA				
VOL	Low level output voltage					
	Type B2 to B12	IOL = 1 uA			0.05	
	Type B2	IOL = 2 mA			0.4	V
	Type B4	IOL = 4 mA				
	Type B8	IOL = 8 mA				
	Type B12	IOL = 12 mA				
I_{OZ}	Tri-state output leakage current	V_{OUT} = V_{SS} or V_{DD}	-10		10	µA
I_{Ds}	ALIVE module Current (Quiescent supply current)				100	µA
C_{IN}	Input Capacitance (Any input and Bi-directional buffers)				5	pF
C_{OUT}	Output Capacitance (Any output buffers)				5	pF

Table 24-4. Normal I/O PAD DC Electrical Characteristics

(VDDOP1,2 = 2.8V ± 0.3V, TA = -40 to 85°C)

Symbol	Parameters	Condition	Min	Typ	Max	Unit
VIH	High level input voltage					
	LVCMOS interface		2.0			V
VIL	Low level input voltage					
	LVCMOS interface				0.8	V
VT	Switching threshold			$0.5V_{DD}$		V
VT+	Schmitt trigger, positive-going threshold	CMOS			2.0	V
VT-	Schmitt trigger, negative-going threshold	CMOS	0.8			V
IIH	High level input current					
	Input buffer	VIN = VDD	-10		10	µA
	Input buffer with pull-down		10	33	71	
IIL	Low level input current					
	Input buffer	VIN = VSS	-10		10	µA
	Input buffer with pull-up		-71	-33	-10	
VOH	High level output voltage					
	Type B2 to B12	IOH= - 1uA	V_{DD} - 0.05			
VOL	Low level output voltage					
	Type B2 to B12	IOL = 1 uA			0.05	
I_{OZ}	Tri-state output leakage current	V_{OUT} = V_{SS} or V_{DD}	-10		10	µA
I_{DD}	STOP Current (Quiescent supply current)				100	µA
C_{IN}	Input Capacitance (Any input and Bi-directional buffers)				5	pF
C_{OUT}	Output Capacitance (Any output buffers)				5	pF

Table 24-5. Normal I/O PAD DC Electrical Characteristics

(VDDOP1,2 = 2.5V ± 0.2V, TA = -40 to 85°C)

Symbol	Parameters	Condition	Min	Typ	Max	Unit
VIH	High level input voltage					
	LVCMOS interface		1.7			V
VIL	Low level input voltage					
	LVCMOS interface				0.7	V
VT	Switching threshold			$0.5V_{DD}$		V
VT+	Schmitt trigger, positive-going threshold	CMOS			1.7	V
VT-	Schmitt trigger, negative-going threshold	CMOS	0.7			V
IIH	High level input current					
	Input buffer	VIN = VDD	-10		10	µA
	Input buffer with pull-down		5	25	50	
IIL	Low level input current					
	Input buffer	VIN = VSS	-10		10	µA
	Input buffer with pull-up		-50	-25	-5	
VOH	High level output voltage					
	Type B2 to B12	IOH= - 1uA	V_{DD} - 0.05			
VOL	Low level output voltage					
	Type B2 to B12	IOL = 1 uA			0.05	
I_{OZ}	Tri-state output leakage current	$V_{OUT} = V_{SS}$ or V_{DD}	-10		10	µA
I_{DD}	STOP Current (Quiescent supply current)				100	µA
C_{IN}	Input Capacitance (Any input and Bi-directional buffers)				5	pF
C_{OUT}	Output Capacitance (Any output buffers)				5	pF

Table 24-6. Special I/O PAD DC Electrical Characteristics

(VDDMOP = 1.8V ± 0.1V, TA = -40 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
VEXT	Output Supply Voltage	1.7	1.8	1.9	V
VINT	Internal Core Voltage	Refer table24-2			V
T_A	Ambient Temperature	-40	25	85	°C
V_{IH}	DC Input Logic High	0.7*V_{DD}			V
V_{IL}	DC Input Logic Low			0.25*V_{DD}	V
VT+	Schmitt Trigger, Positive-Going Threshold			1.25	V
VT-	Schmitt Trigger, Negative-Going Threshold	0.57			V
I_{IH}	High Level Input Current	-10		10	µA
I_{IL}	Low Level Input Current	-10		10	µA
I_{IH}	High Level Input Current with Pull Down	8		46	µA
I_{IL}	Low Level Input Current with Pull Up	-33		-10	µA
V_{OH}	Output High Voltage	V_{DD}-0.45			V
V_{OL}	Output Low Voltage			0.45	V

NOTE: DATA, SCLK, DQS.

Table 24-7. Special I/O PAD DC Electrical Characteristics

(VDDMOP = 1.8V ± 0.1V, TA = -40 to 85°C)

Symbol	Parameter	Condition	Min	Max	Unit
VOH	Output High Voltage	12mA Buffer, I_{OH} = -12mA	1.1	-	V
VOL	Output Low Voltage	12mA Buffer, I_{OH} = -12mA	-	0.5	V

NOTE: nSCAS, nSRAS, nBE, nWE, nGCS, ADDR, SCKE, nSCLK

Table 24-8. Special I/O PAD DC Electrical Characteristics

(VDDMOP = 3.3V ± 0.3V, TA = -40 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
VEXT	Output Supply Voltage	3.0	3.3	3.6	V
VINT	Internal Core Voltage	Refer table 24-2			V
T_A	Ambient Temperature	-40	25	85	°C
V_{IH}	DC Input Logic High	0.7*V_{DD}			V
V_{IL}	DC Input Logic Low			0.25*V_{DD}	V
VT+	Schmitt Trigger, Positive-Going Threshold			2.3	V
VT-	Schmitt Trigger, Negative-Going Threshold	1.18			V
I_{IH}	High Level Input Current	-10		10	µA
I_{IL}	Low Level Input Current	-10		10	µA
I_{IH}	High Level Input Current with Pull Down	39		183	µA
I_{IL}	Low Level Input Current with Pull Up	-114		-37	µA
V_{OH}	Output High Voltage	V_{DD}-0.45			V
V_{OL}	Output Low Voltage			0.45	V

NOTE: DATA, RnB

Table 24-9. Special I/O PAD DC Electrical Characteristics

(VDDMOP = 3.3V ± 0.3V, TA = -40 to 85°C)

Symbol	Parameter	Condition	Min	Max	Unit
VOH	Output High Voltage	12mA Buffer, I_{OH} = -12mA	1.1	-	V
VOL	Output Low Voltage	12mA Buffer, I_{OH} = -12mA	-	0.5	V

NOTE: nBE, ADDR, nWE, ALE, CLE, nGCS, nOE

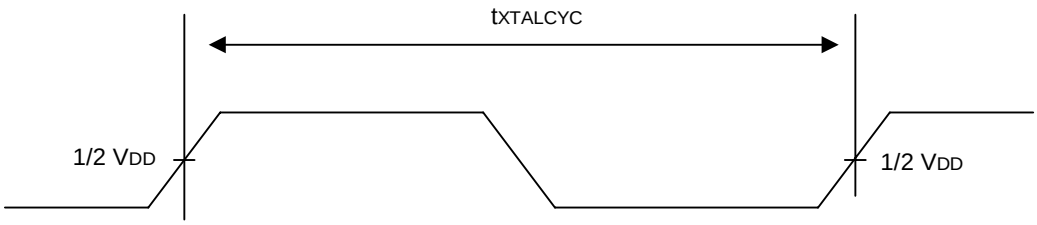
Table 24-10. USB DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
VIH	High level input voltage		2.5		V
VIL	Low level input voltage			0.8	V
IIH	High level input current	Vin = 3.3V	-10	10	µA
IIL	Low level input current	Vin = 0.0V	-10	10	µA
VOH	Static Output High	15K to GND	2.8	3.6	V
VOL	Static Output Low	1.5K to 3.6V		0.3	V

Table 24-11. RTC OSC DC Electrical Characteristics

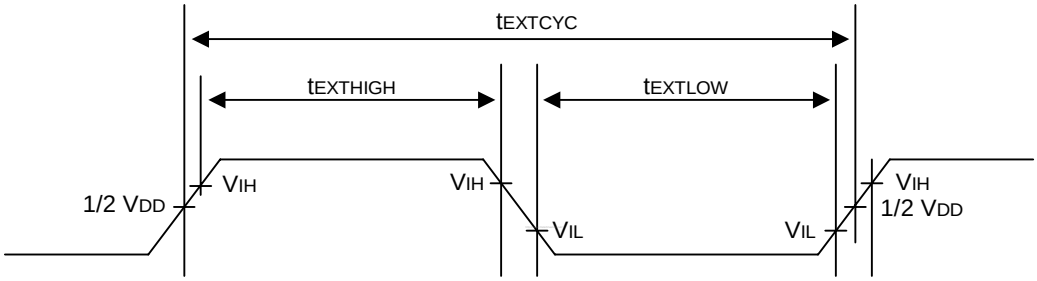
Symbol	Parameter	Min	Typ	Max	Unit
VEXT	Output supply voltage	2.7	3.0	3.3	V
VINT	Internal core voltage	2.7	3.0	3.3	V
V_{IH}	DC input logic high	$0.8*V_{DDIO}$			V
V_{IL}	DC input logic low			$0.2*V_{DDIO}$	V
IIH	High level input current	-10		10	μA
IIL	Low level input current	-10		10	μA

A.C. ELECTRICAL CHARACTERISTICS



NOTE: The clock input from the XTIpll pin.

Figure 24-1. XTIpll Clock Timing



NOTE: The clock input from the EXTCLK pin.

Figure 24-2. EXTCLK Clock Input Timing

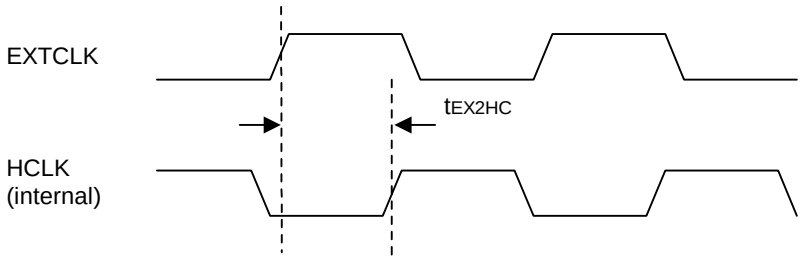


Figure 24-3. EXTCLK/HCLK in case that EXTCLK is used without the PLL

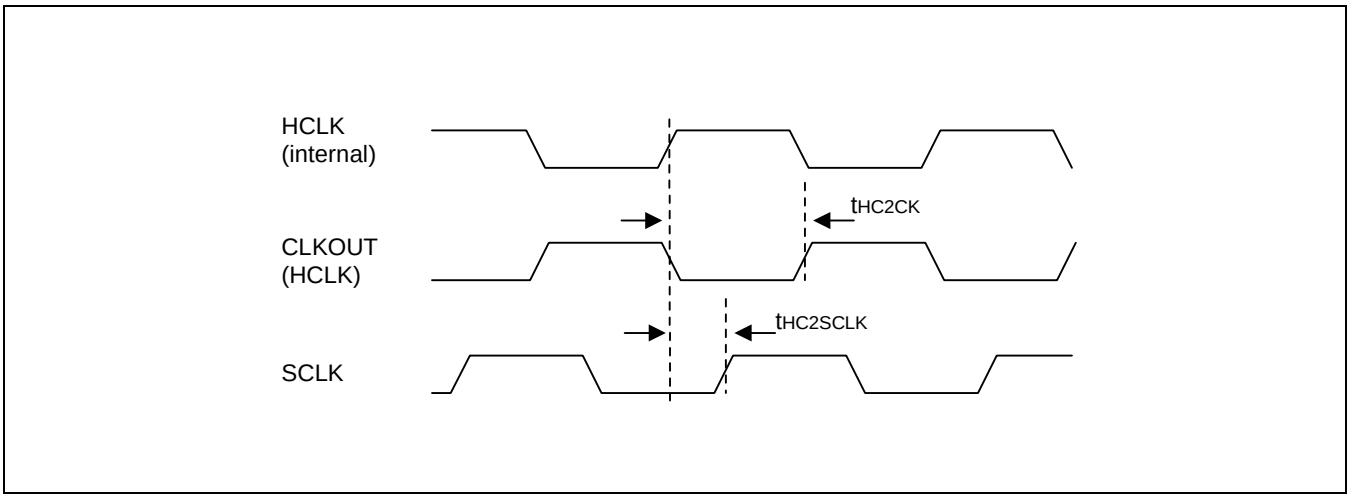


Figure 24-4. HCLK/CLKOUT/SCLK in case that EXTCLK is used

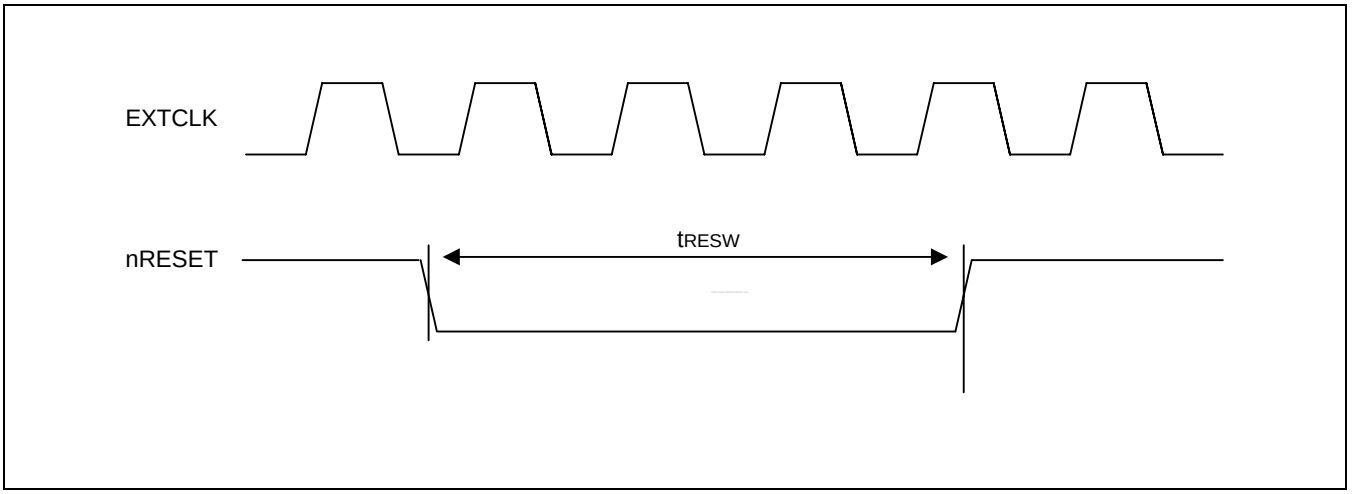


Figure 24-5. Manual Reset Input Timing

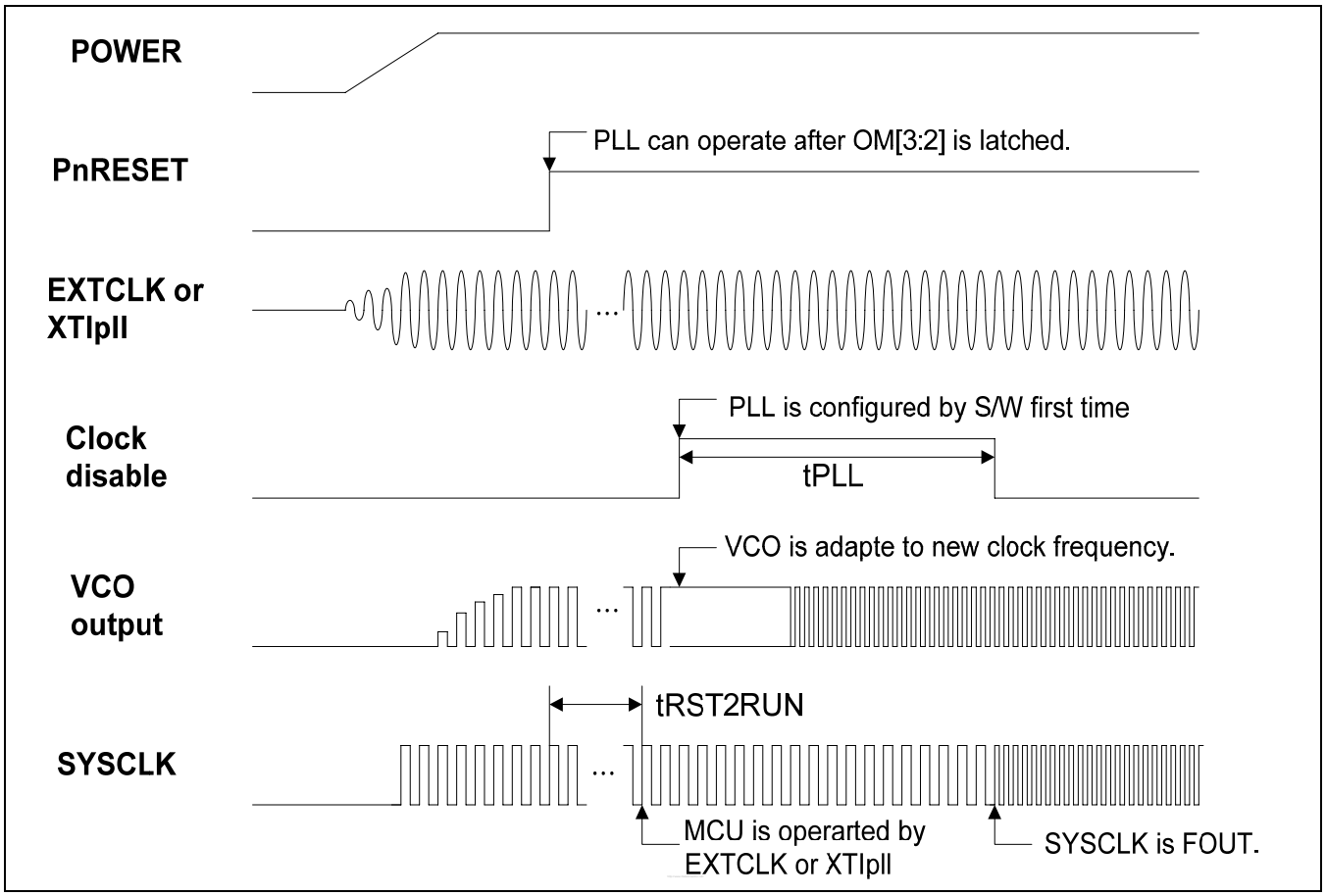


Figure 24-6. Power-On Oscillation Setting Timing

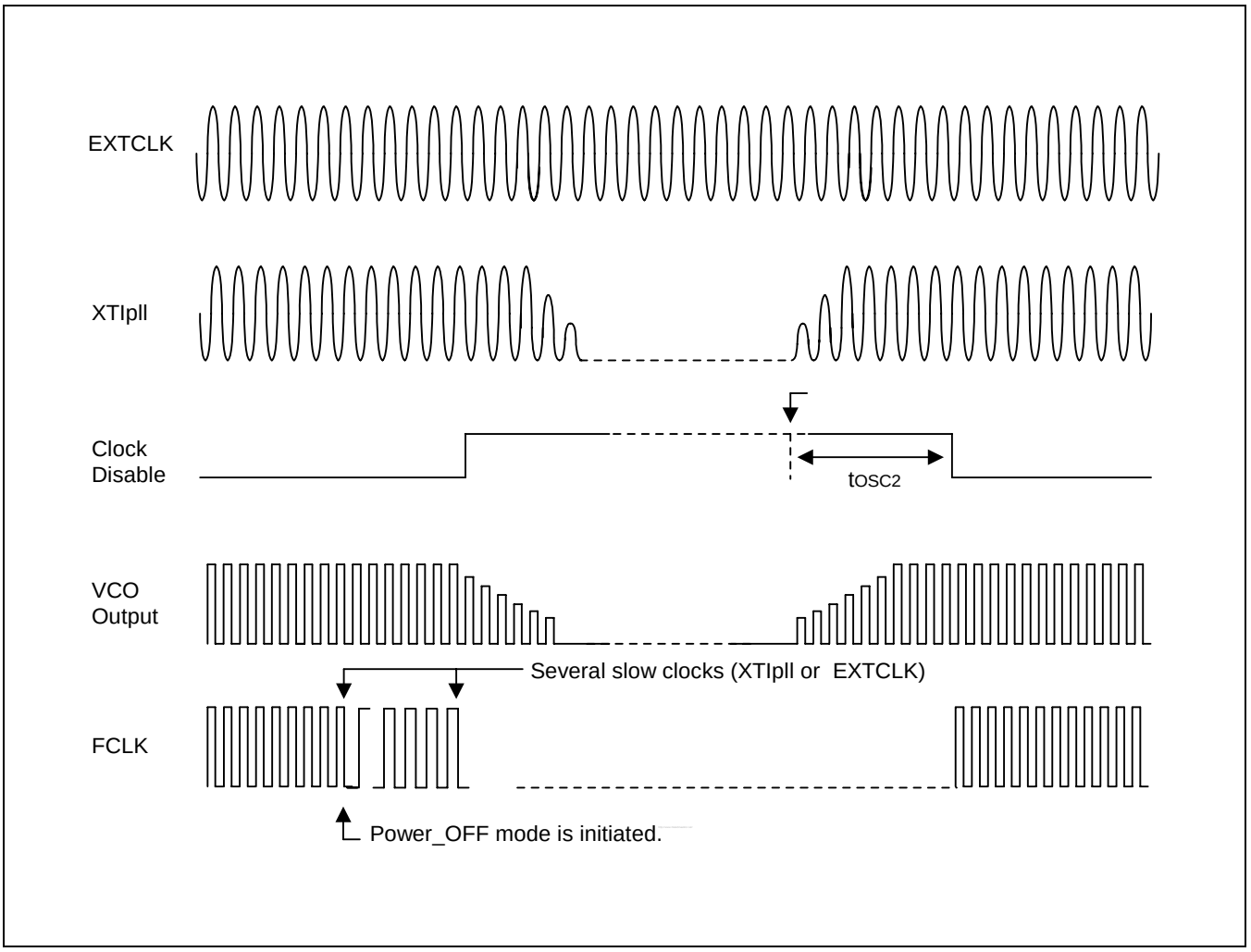


Figure 24-7. Sleep Mode Return Oscillation Setting Timing

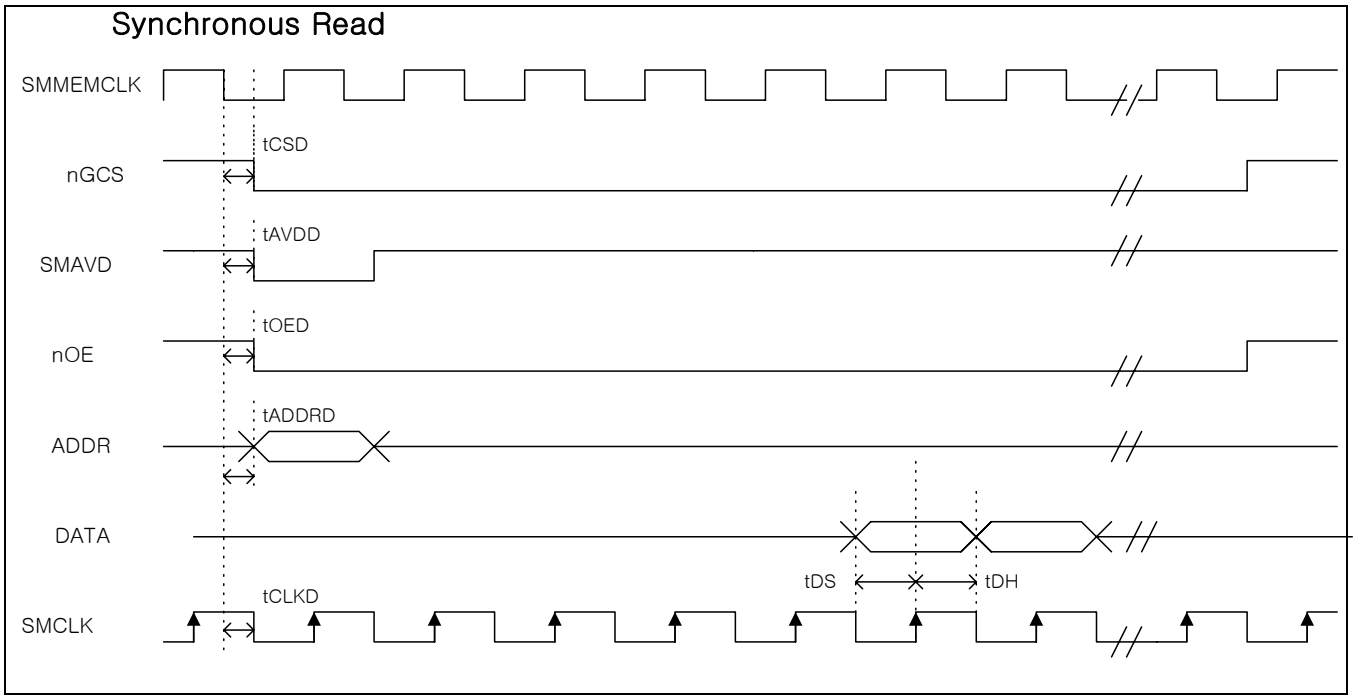


Figure 24-8. SSMC Synchronous Read Timing

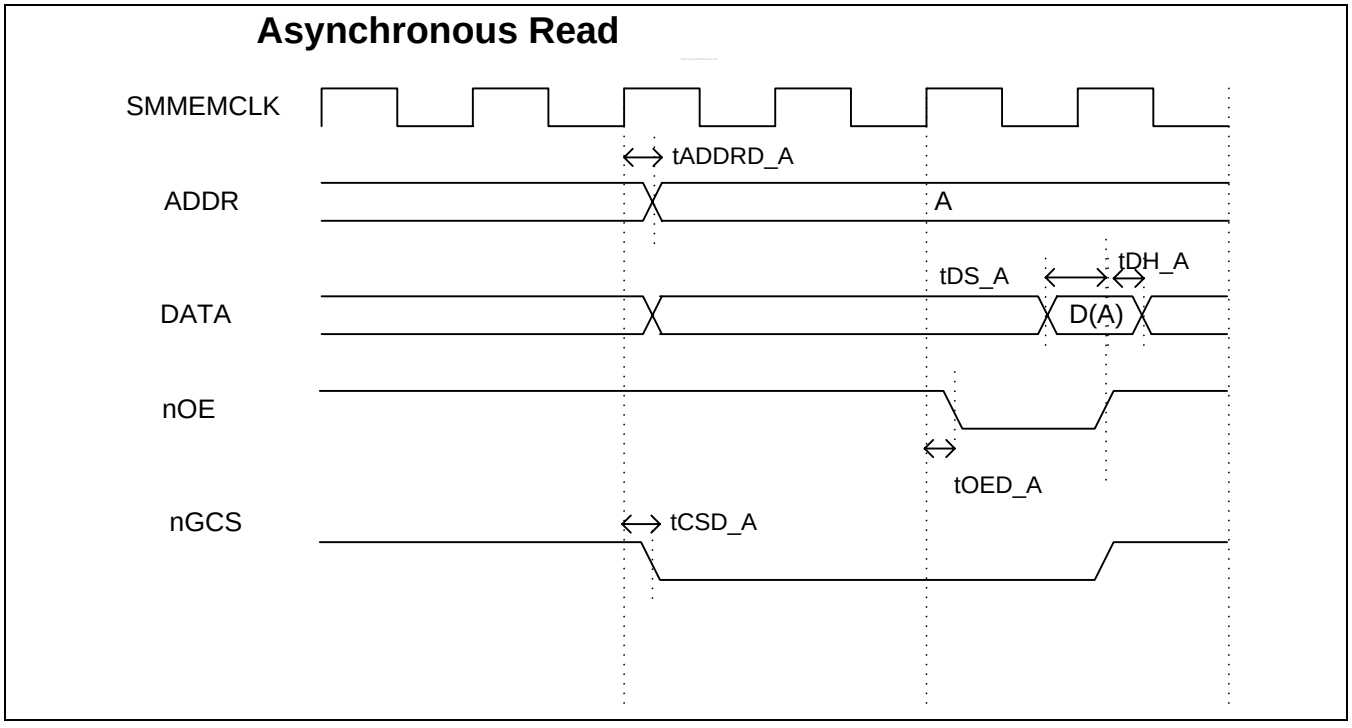


Figure 24-9. SSMC Asynchronous Read Timing

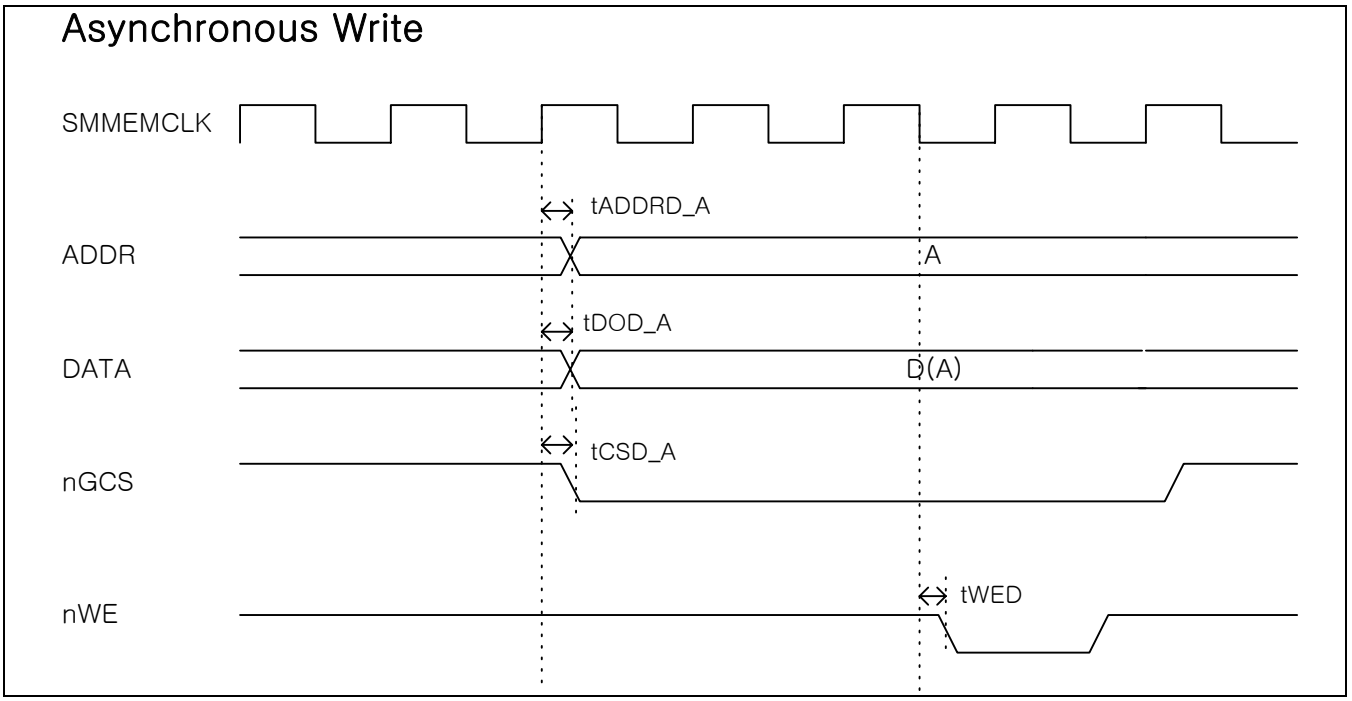


Figure 24-10. SSMC Asynchronous Write Timing

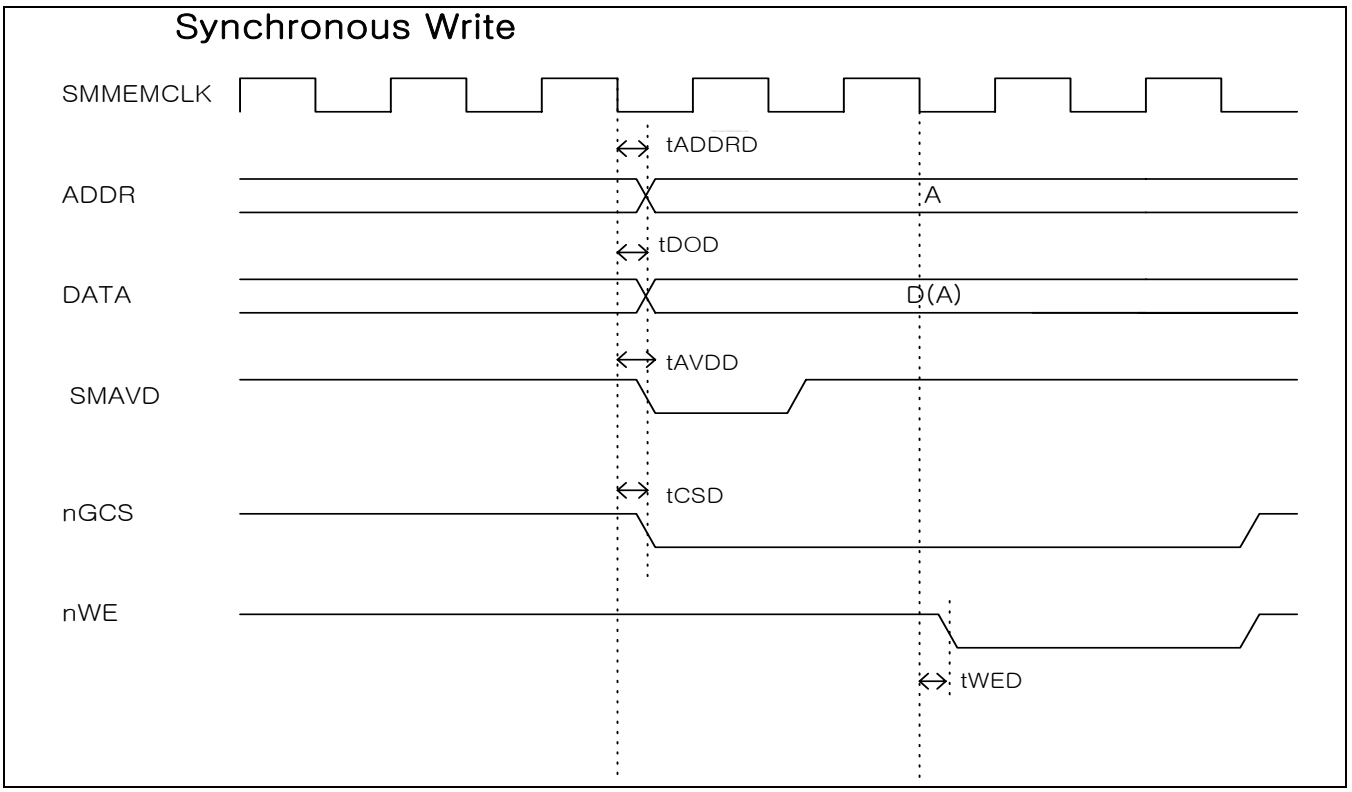


Figure 24-11. SSMC Synchronous Write Timing

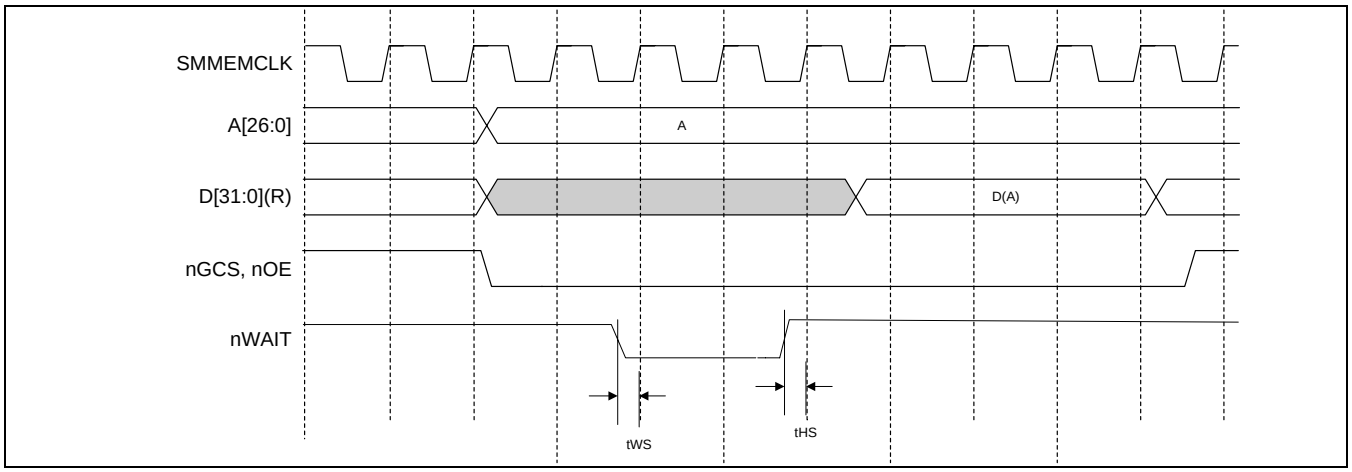


Figure 24-12. SSMC Wait Timing

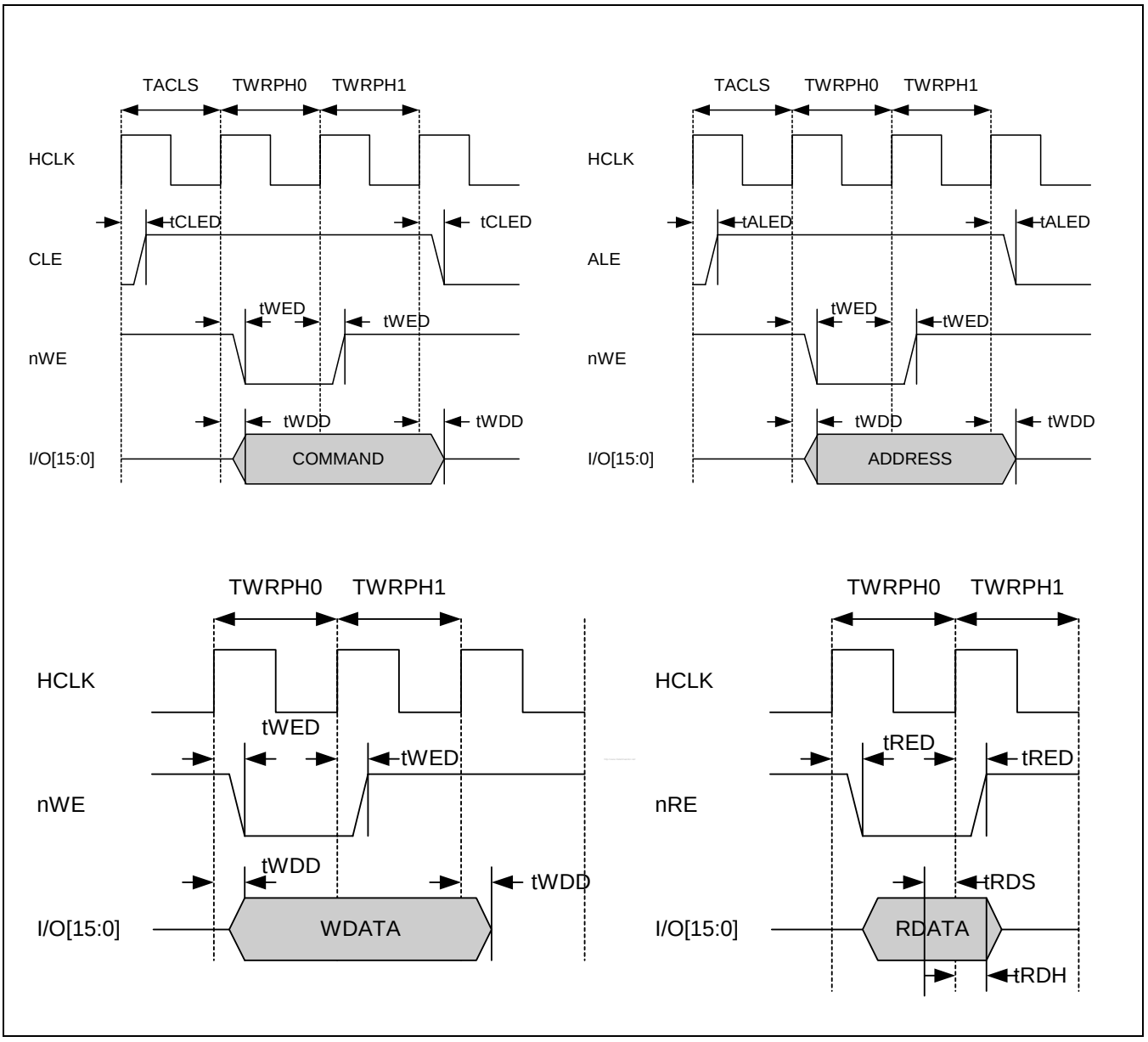


Figure 24-13. Nand Flash Timing

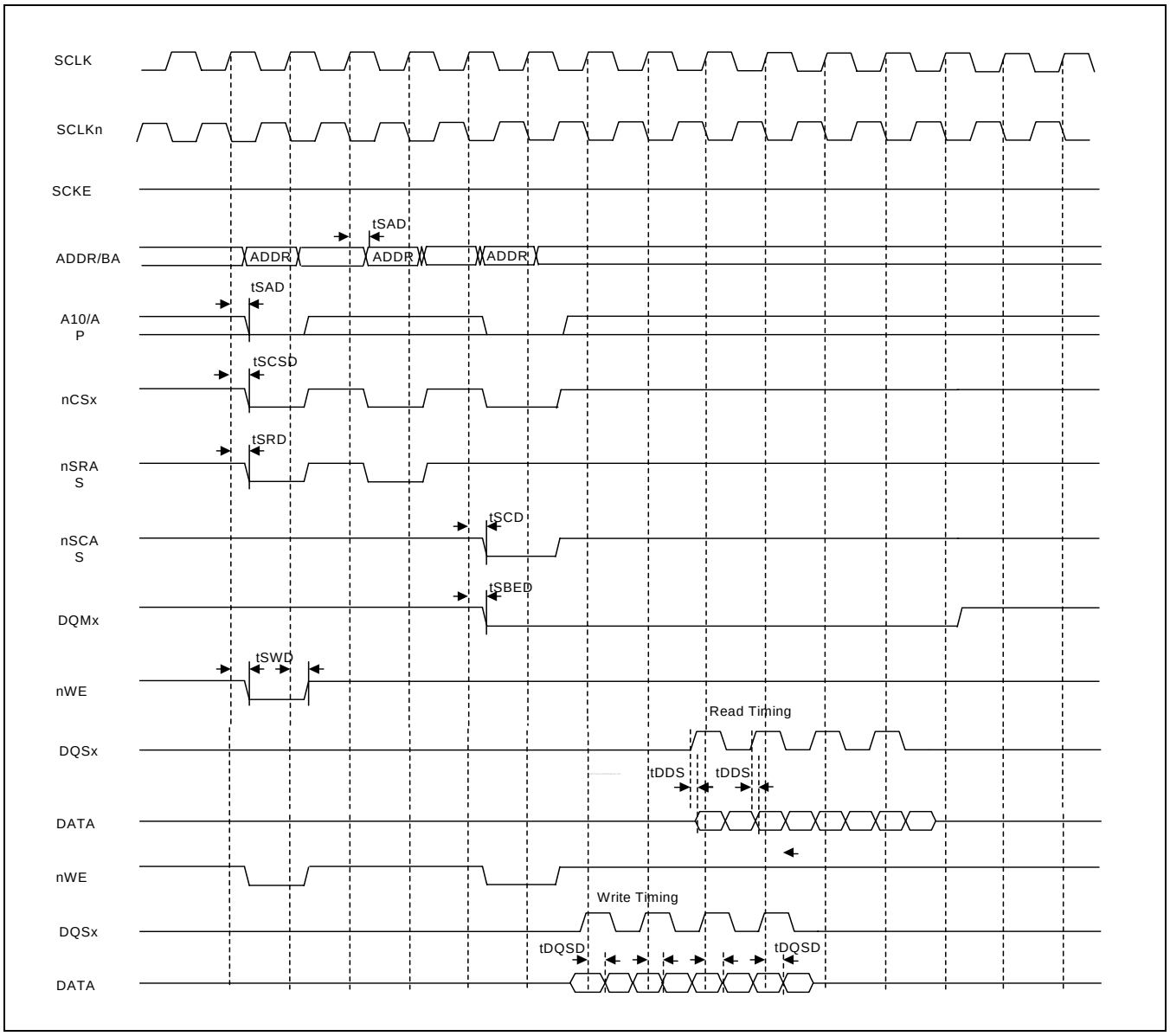


Figure 24-14. DDR SDRAM READ / WRITE Timing

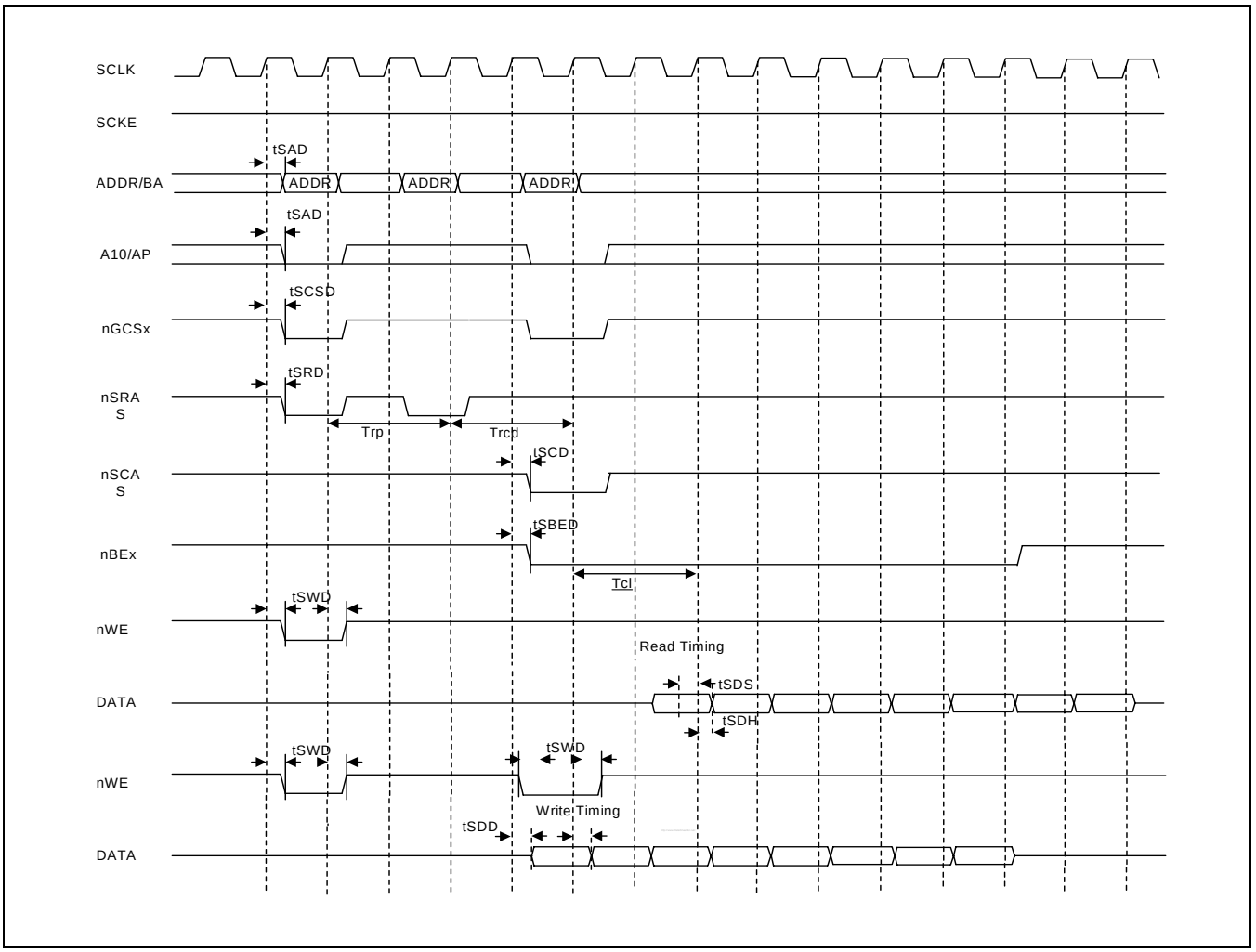


Figure 24-15. SDRAM READ / WRITE Timing (Trp = 2, Trcd = 2, Tcl = 2, DW = 16-bit)

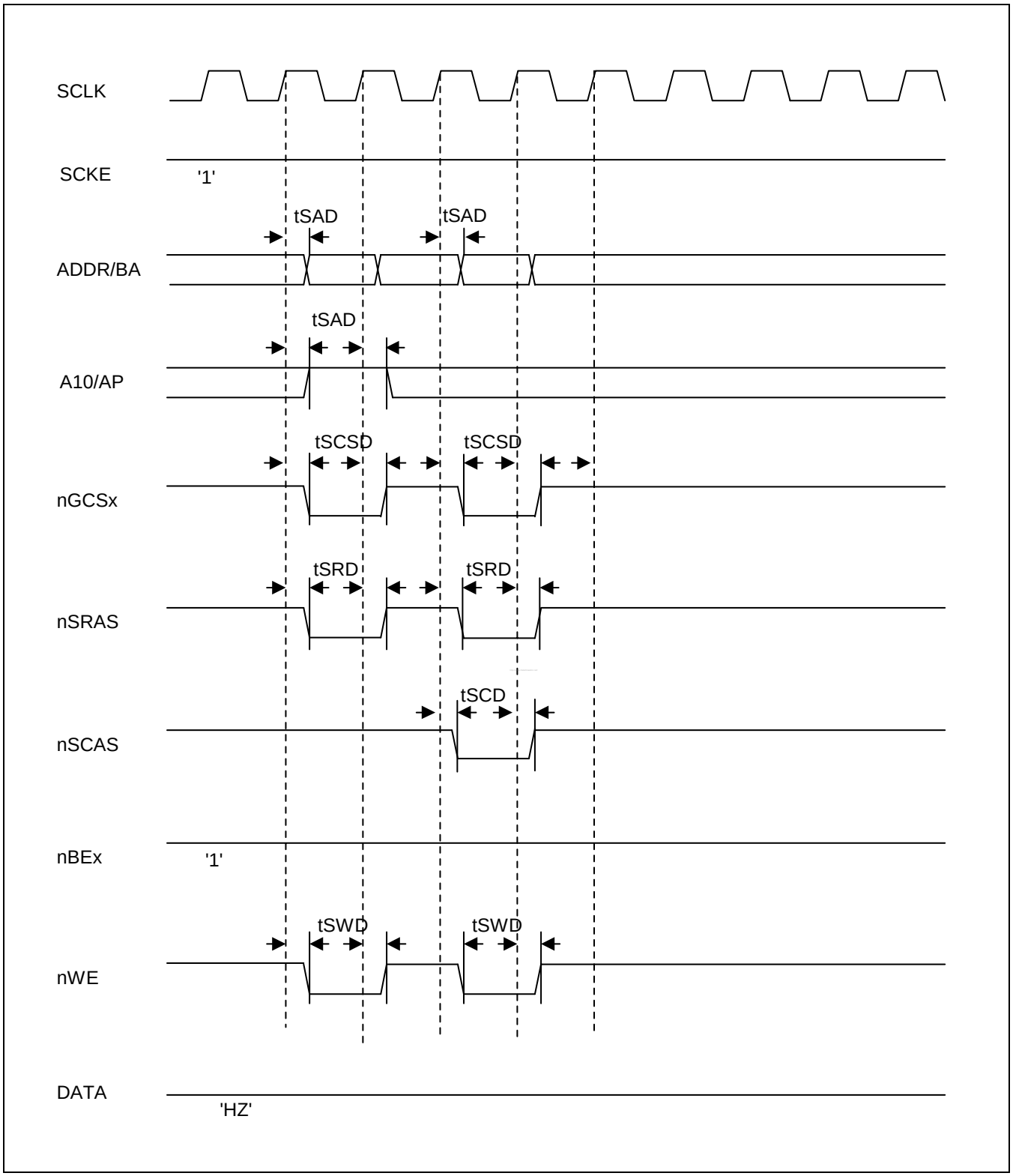
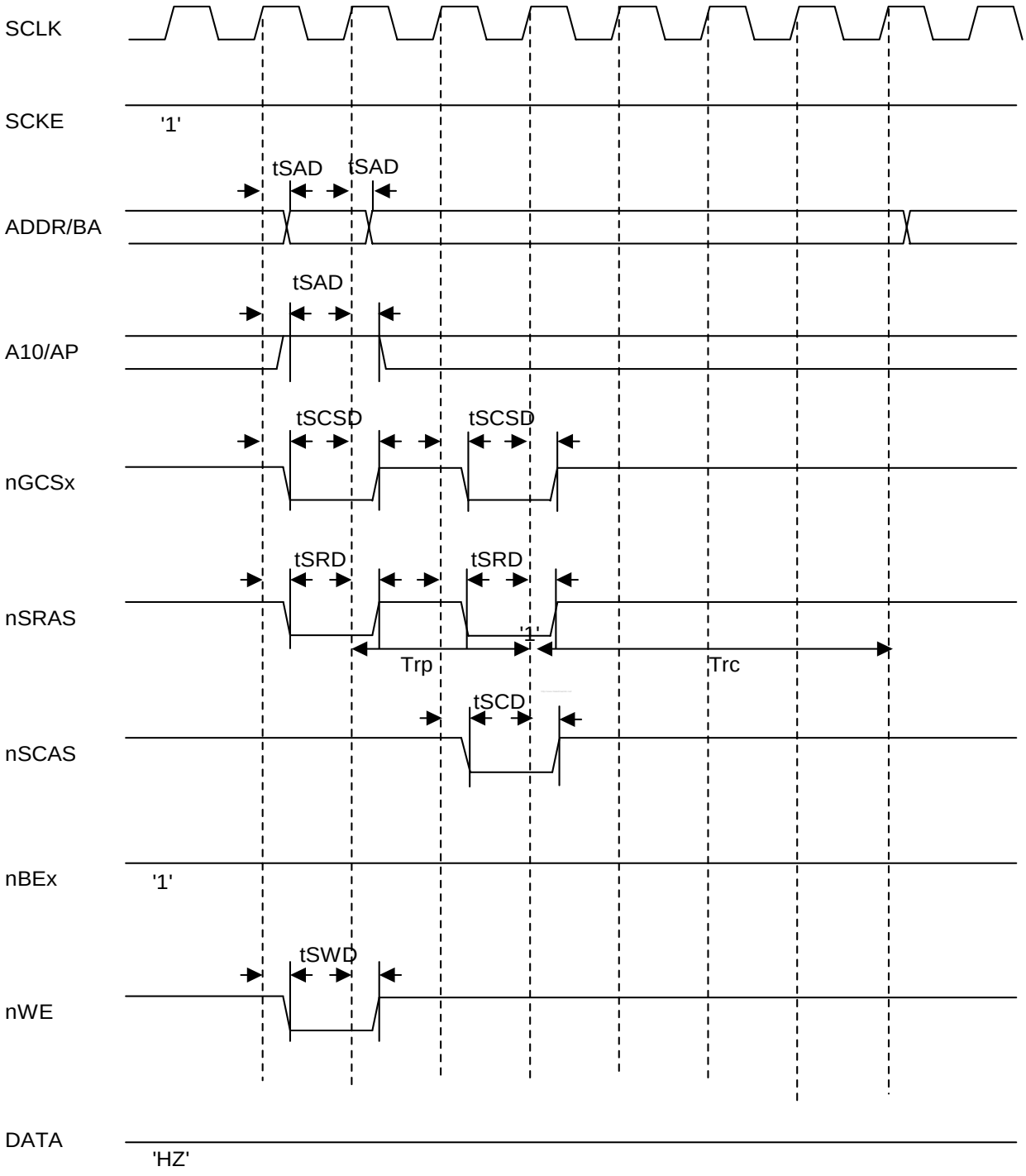


Figure 24-16. SDRAM MRS Timing



NOTE: Before executing auto/self refresh command, all banks must be in idle state.

Figure 24-17. SDRAM Auto Refresh Timing (Trp = 2, Trc = 4)

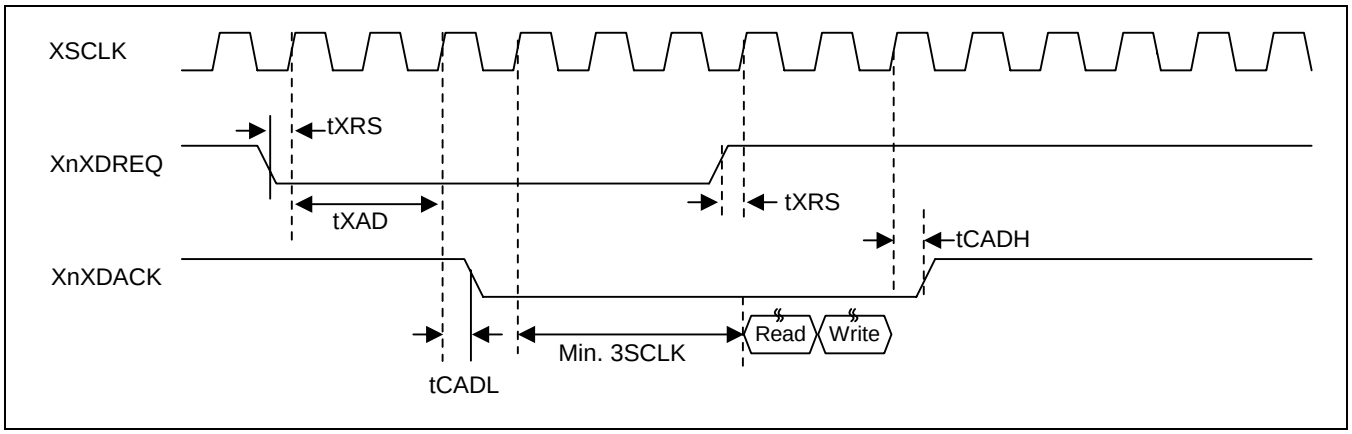


Figure 24-18. External DMA Timing (Handshake, Single transfer)

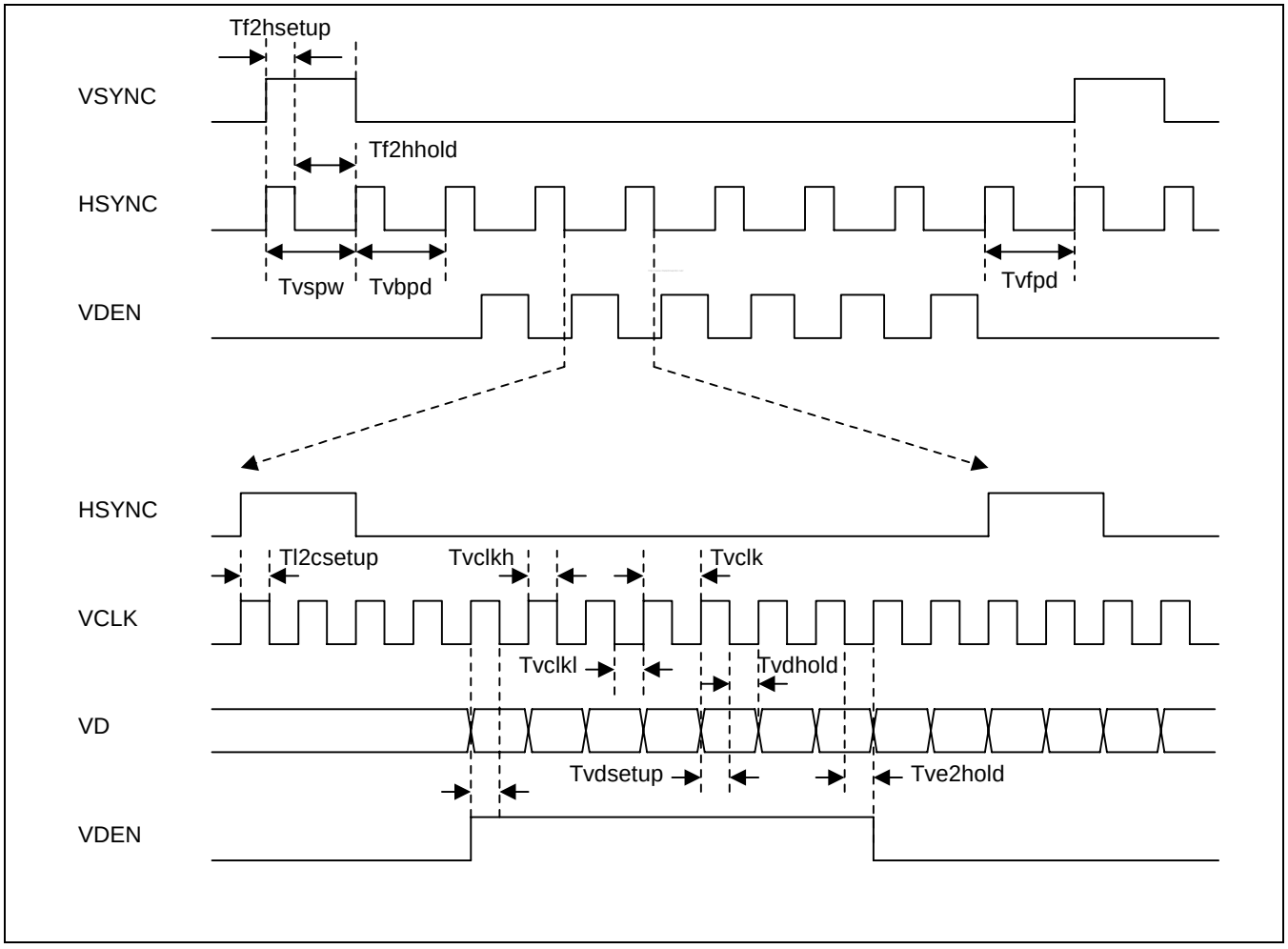


Figure 24-19. TFT LCD Controller Timing

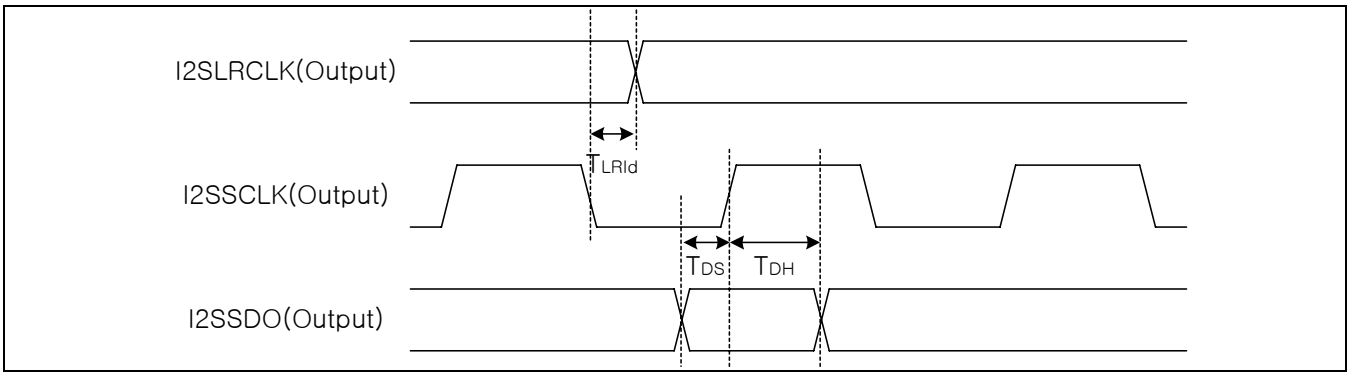


Figure 24-20. IIS Interface Timing (I2S Master Mode Only)

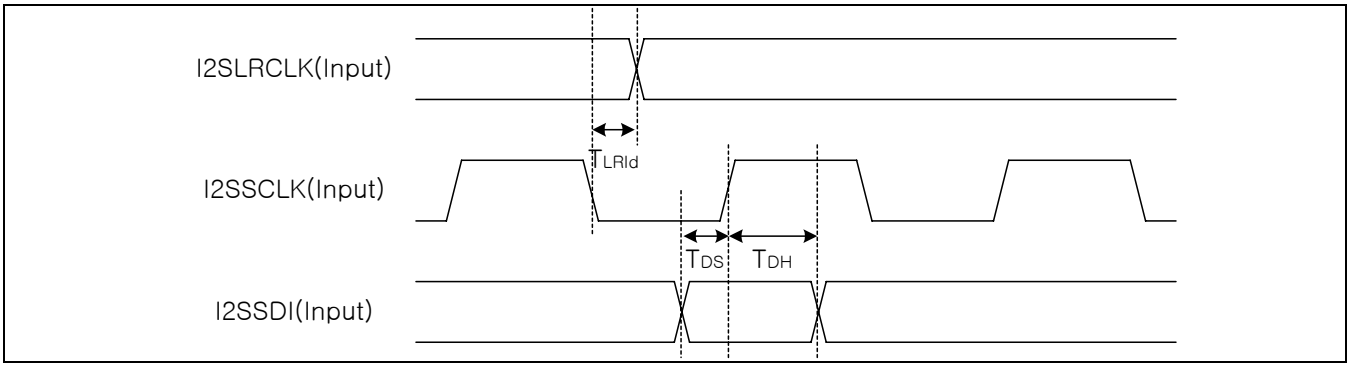


Figure 24-21. IIS Interface Timing (I2S Slave Mode Only)

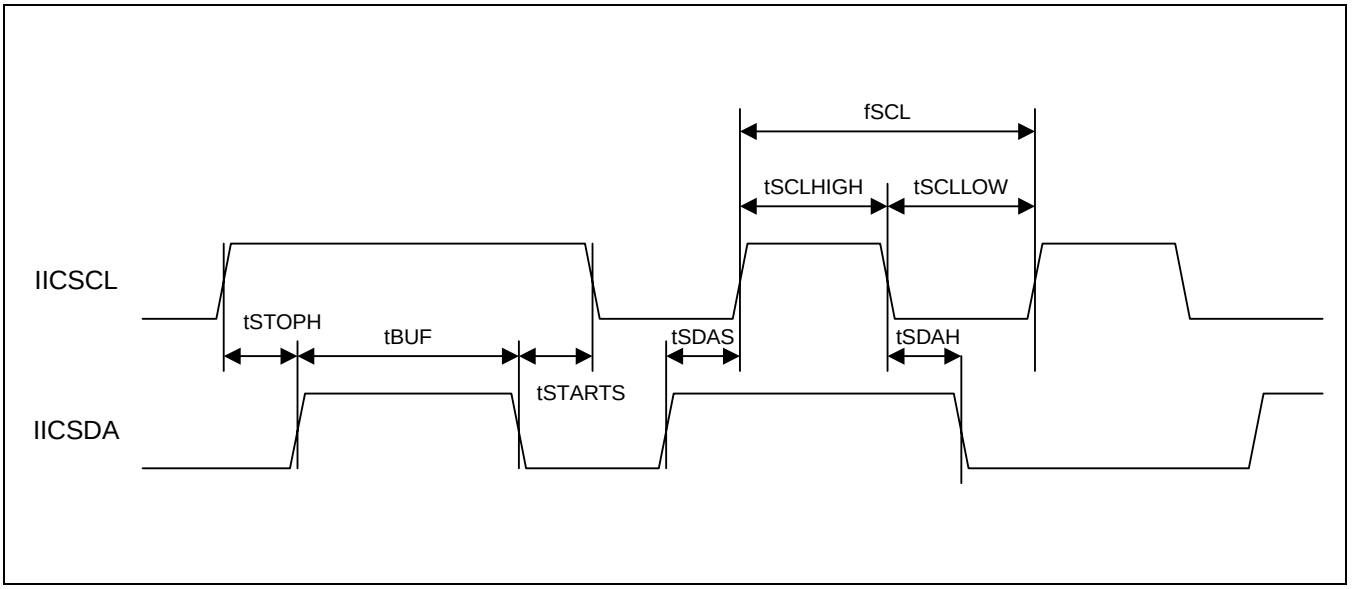


Figure 24-22. IIC Interface Timing

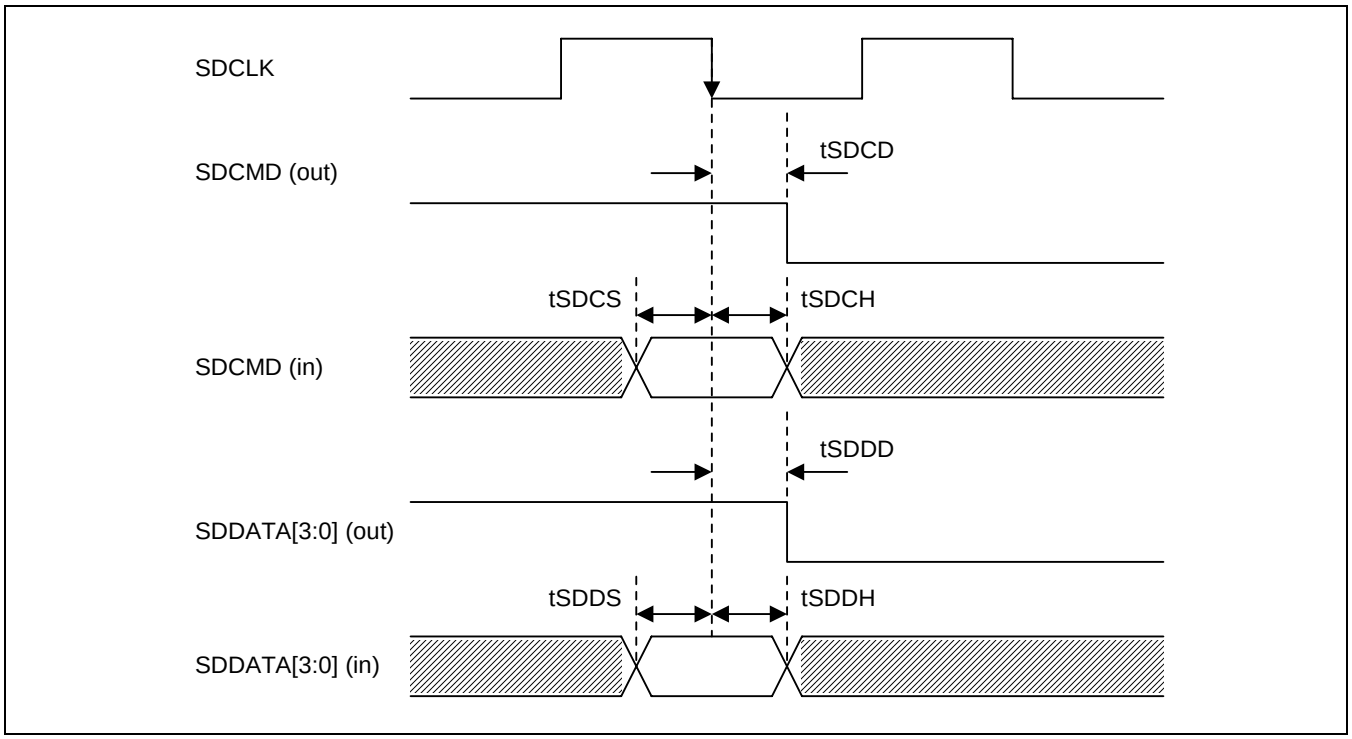


Figure 24-23. SD/MMC Interface Timing

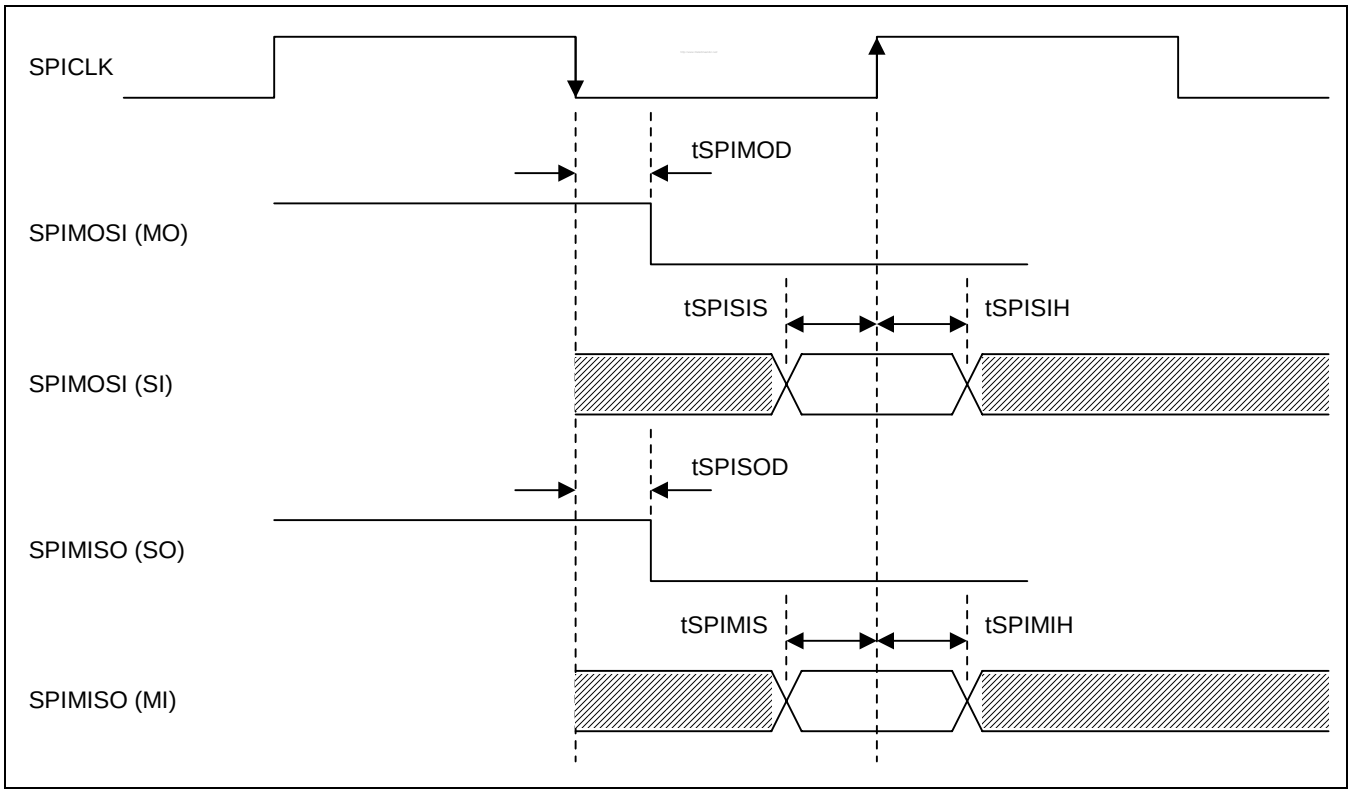


Figure 24-24. SPI Interface Timing (CPHA = 1, CPOL = 1)

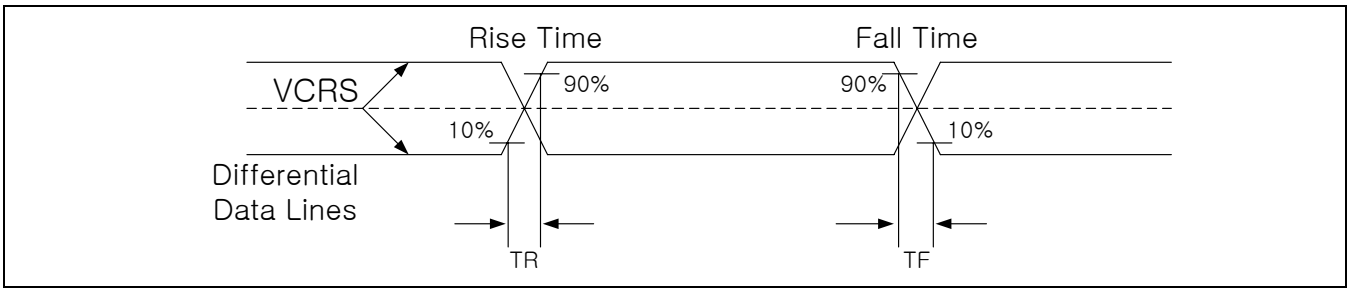


Figure 24-25. USB Timing(Data signal rise/fall time)

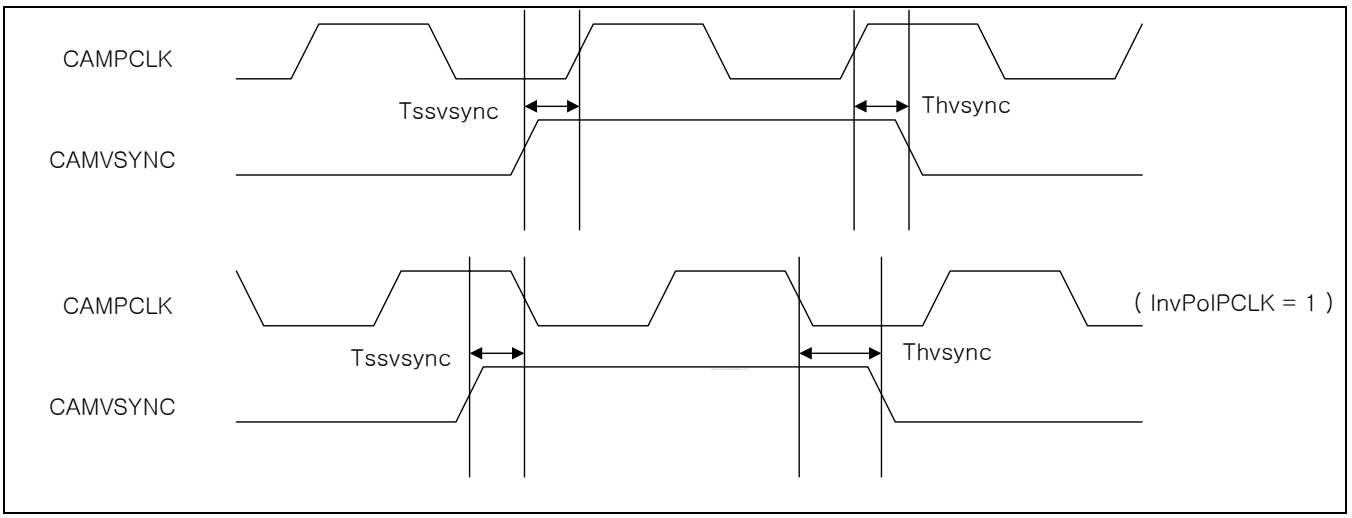


Figure 24-26. CAMIF Timing(VSYNC Timing Diagram)

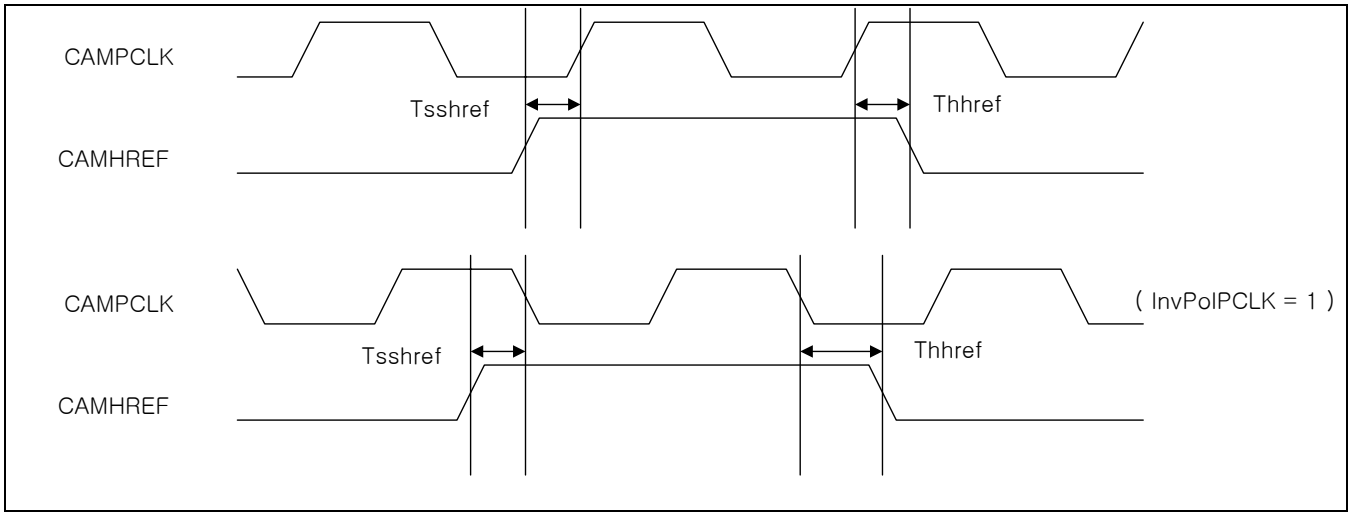


Figure 24-27. CAMIF Timing(HREF Timing Diagram)

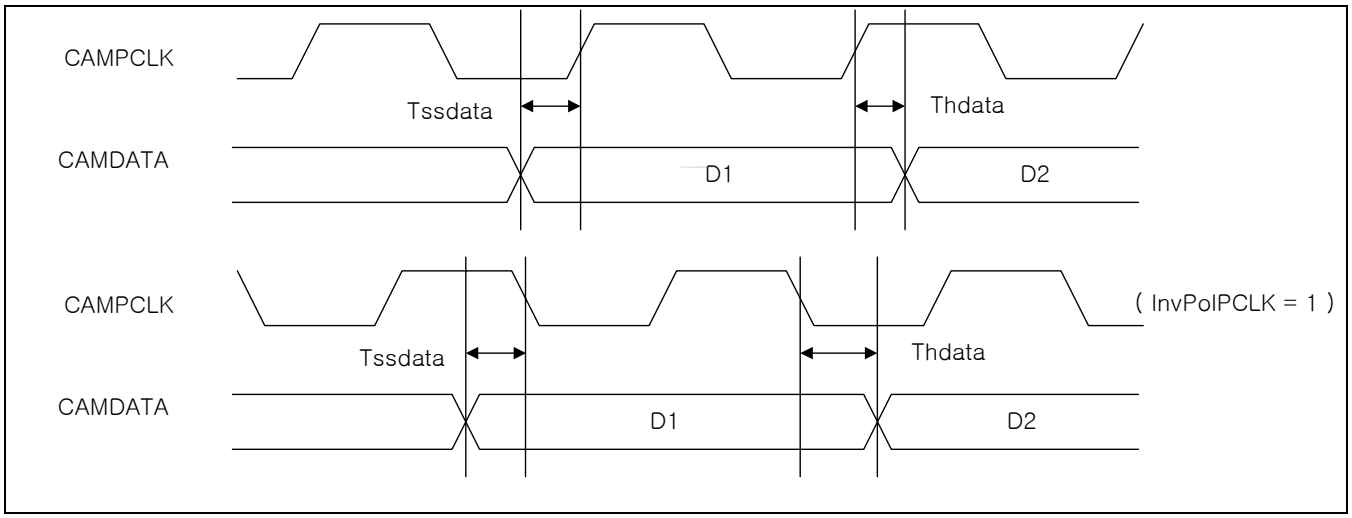


Figure 24-28. CAMIF Timing(Data Timing Diagram)

Table 24-12. Clock Timing Constants

(VDDi = typ:1.25(1.15 ~ 1.5V), TA = -40 to 85°C, VDDIO = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Crystal clock input frequency	f_{XTAL}	10	-	20	MHz
Crystal clock input cycle time	$t_{XTALCYC}$	25	-	100	ns
External clock input frequency	f_{EXT}	10		133	MHz
External clock input cycle time	t_{EXTCYC}	7.5		100	ns
External clock input low level pulse width	t_{EXTLOW}	3.5		-	ns
External clock input high level pulse width	$t_{EXTHIGH}$	3.5		-	ns
External clock to HCLK (without PLL)	t_{EX2HC}	5		13	ns
HCLK (internal) to CLKOUT	t_{HC2CK}	3.3		8.8	ns
HCLK (internal) to SCLK	$t_{HC2SCLK}$	1.9		5.8	ns
Reset assert time after clock stabilization	t_{RESW}	4		-	XTIpll or EXTCLK
PLL Lock Time	t_{PLL}	300		-	us
Sleep mode return oscillation setting time.[1)]	t_{OSC2}	2		524290	XTIpll or EXTCLK
The interval before CPU runs after nRESET is released.	$t_{RST2RUN}$	5		-	XTIpll or EXTCLK

NOTE: tOSC2 is programmable by setting the PWRSETCNT bits in Reset Count register.
tOSC2 = PWRSETCNT * 2^11 + 2

Table 24-13. SSMC Timing Constants(asynchronous and synchronous)

Parameter	Symbol		Min	Typ	Max	Unit
SSMC Sync Chip Select Delay	tCSD	bank0	3	–	8	ns
		bank1	3	–	8	ns
		bank2	3	–	7	ns
		bank3	3	–	8	ns
		bank4	3	–	7	ns
		bank5	3	–	7	ns
		bank6	3	–	7	ns
		bank7	3	–	7	ns
SSMC Clock Delay	tCLKD		3		8	ns
SSMC Sync Output Enable Delay	tOED		3	–	8	ns
SSMC Write Enable Delay	tWED		3	–	8	ns
SSMC Sync Address Delay	tADDRD		3	–	8	ns
SSMC Sync Data Output Delay	tDOD		3	–	7	ns
SSMC Address Valid Delay	tAVDD		3	–	7	ns
SSMC Sync Data Input setup time	tDS		2		4	ns
SSMC Sync Data Input hold time	tDH		0		0	ns
SSMC Async Data Input setup time	tDS_A		4	–	11	ns
SSMC Async Data Input hold time	tDH_A		0	–	0	ns
SSMC Async Address Delay	tADDRD_A		3	–	8	ns
SSMC Async Chip Select Delay	tCSD_A	bank0	3	–	9	ns
		bank1	3	–	9	ns
		bank2	3	–	8	ns
		bank3	3	–	9	ns
		bank4	3	–	8	ns
		bank5	3	–	8	ns
		bank6	3	–	7	ns
		bank7	3	–	8	ns

SSMC Async Output Enable Delay	tOED_A	3	–	8	ns
SSMC Async Data Output Delay	tDOD_A	3	–	10	ns

Table 24-14. NFCON Bus Timing Constants

(VDDi = typ:1.25(1.15 ~ 1.5V), TA = -40 to 85°C, VDDMOP = 1.8V ± 0.1V)

Parameter	Symbol	Min	Max	Unit
NFCON Chip Enable delay	t_{CED}	-	7.83	ns
NFCON CLE delay	t_{CLED}	-	8.96	ns
NFCON ALE delay	t_{ALED}	-	8.38	ns
NFCON Write Enable delay	t_{WED}	-	9.42	ns
NFCON Read Enable delay	t_{RED}	-	10.03	ns
NFCON Write Data delay	t_{WDD}	-	8.78	ns
NFCON Read Data Setup requirement time	t_{RDS}	1.00	-	ns
NFCON Read Data Hold requirement time	t_{RDH}	0.20	-	ns

Table 24-15. Memory Interface Timing Constants (SDRAM)

(VDDi = typ:1.25(1.15 ~ 1.5V), TA = -40 to 85°C, VDDMOP = 1.8V ± 0.1V, 133MHz, CL = 25pF)

Parameter	Symbol	Min	Max	Unit
SDRAM Address Delay	t_{SAD}	1.58	5.61	ns
SDRAM Chip Select Delay	t_{SCSD}	1.98	5.27	ns
SDRAM Row active Delay	t_{SRD}	1.88	4.67	ns
SDRAM Column active Delay	t_{SCD}	1.63	3.96	ns
SDRAM Byte Enable Delay	t_{SBED}	1.80	4.58	ns
SDRAM Write enable Delay	t_{SWD}	2.13	5.51	ns
SDRAM read Data Setup time	t_{SDS}	3.00	-	ns
SDRAM read Data Hold time	t_{SDH}	1.50	-	ns
SDRAM output Data Delay	t_{SDD}	1.59	5.65	ns
SDRAM Clock Enable Delay	t_{CKED}	1.62	4.11	ns

Table 24-16. Memory Interface Timing Constants (Mobile DDR)

(VDDi = typ:1.25(1.15 ~ 1.5V), TA = -40 to 85°C, VDDMOP = 1.8V ± 0.1V, 133MHz, CL = 25pF)

Parameter	Symbol	Min	Max	Unit
DDR SDRAM Address Delay	tSAD	1.69	5.61	ns
DDR SDRAM Chip Select Delay	tSCSD	2.09	5.27	ns
DDR SDRAM Row active Delay	tSRD	1.88	4.67	ns
DDR SDRAM Column active Delay	tSCD	1.63	3.96	ns
DDR SDRAM Byte Enable Delay	tSBED	-0.06	0.02	ns
DDR SDRAM Write enable Delay	tSWD	2.24	5.51	ns
DDR SDRAM read Data Setup time	tDDS	-	0.70	ns
DDR SDRAM output Data Delay	tDDD	-0.05	0.26	ns
DDR SDRAM DQS Delay	tDQSD	-0.30	0.83	ns

Note) If CL increase over the 25pF, operation conditions follow the guide table

Load Capacitance (CL)	Bus clock	Voltage
< 25 pF	133MHz	1.8V± 0.1V
25 pF < CL < 50 pF	100MHz	
50 pF < CL < 70 pF	90MHz	

Table 24-17. DMA Controller Module Signal Timing Constants

(VDDi = typ:1.25(1.15 ~ 1.5V), TA = -40 to 85°C, VDDOP4 = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
eXternal Request Setup	tXRS	6.4/6.4	–	9.9/9.9	ns
aCcess to Ack Delay when Low transition	tCADL	3.1/2.8		7.8/7.1	ns
aCcess to Ack Delay when High transition	tCADH	2.8/2.5		7.8/6.9	ns
eXternal Request Delay	tXAD	2	–	–	HCLK

Table 24-18. TFT LCD Controller Module Signal Timing Constants

(VDDi = typ:1.25(1.15 ~ 1.5V), TA = -40 to 85°C, VDDOP2 = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Units
VCLK pulse width	Tvclk	18	200	–	ns
VCLK pulse width high	Tvclkh	0.3	–	–	Pvclk(1)
VCLK pulse width low	Tvclkl	0.3	–	–	Pvclk
Vertical sync pulse width	Tvspw	VSPW + 1	–	–	Phclk(2)
Vertical back porch delay	Tvbpd	VBPD+1	–	–	Phclk
Vertical front porch dealy	Tvfpd	VFPD+1	–	–	Phclk
Hsync setup to VCLK falling edge	Tl2csetup	0.3	–	–	Pvclk
VDEN set up to VCLK falling edge	Tde2csetup	0.3	–	–	Pvclk
VDEN hold from VCLK falling edge	Tde2chold	0.3	–	–	Pvclk
VD setup to VCLK falling edge	Tvd2csetup	0.3	–	–	Pvclk
VD hold from VCLK falling edge	Tvd2chold	0.3	–	–	Pvclk
VSYNC setup to HSYNC falling edge	Tf2hsetup	HSPW + 1	–	–	Pvclk
VSYNC hold from HSYNC falling edge	Tf2hhold	HBPD + HFPD + HOZVAL + 3	–	–	Pvclk

NOTES :

1. VCLK period
2. HSYNC period

Table 24-19. IIS Controller Module Signal Timing Constants(I2S Master Mode Only)

(VDDi = typ:1.25(1.15 ~ 1.5V), T_A = –40 to 85 °C, VDDOP3 = 3.3V ± 0.3V)

Parameter	Symbol	Min.	Typ.	Max	Unit
LR Clock Input Delay	TLRId	5	-	13	ns
Serial Data Setup Time	TDS	10	-		ns
Serial Data Hold Time	TDH	10	-		ns

Table 24-20. IIS Controller Module Signal Timing Constants(I2S Slave Mode Only)

(VDDi = typ:1.25(1.15 ~ 1.5V), T_A = –40 to 85 °C, VDDOP3 = 3.3V ± 0.3V)

Parameter	Symbol	Min.	Typ.	Max	Unit
LR Clock Input Delay	TLRId	0	-		ns
Serial Data Setup Time	TDS	10	-		ns
Serial Data Hold Time	TDH	10	-		ns

Table 24-21. IIC BUS Controller Module Signal Timing

(VDDi = typ:1.25(1.15 ~ 1.5V), TA = -40 to 85°C, VDDOP3 = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ.	Max	Unit
SCL clock frequency	fSCL	–	–	std. 100 fast 400	kHz
SCL high level pulse width	tSCLHIGH	std. 4.0 fast 0.6	–	–	µs
SCL low level pulse width	tSCLLOW	std. 4.7 fast 1.3	–	–	µs
Bus free time between STOP and START	tBUF	std. 4.7 fast 1.3	–	–	µs
START hold time	tSTARTS	std. 4.0 fast 0.6	–	–	µs
SDA hold time	tSDAH	std. 0 fast 0	–	std. - fast 0.9	µs
SDA setup time	tSDAS	std. 250 fast 100	–	–	ns
STOP setup time	tSTOPH	std. 4.0 fast 0.6	–	–	µs

NOTES: Std. means Standard Mode and fast means Fast Mode.

1. The IIC data hold time(tSDAH) is minimum 0ns.
   (IIC data hold time is minimum 0ns for standard/fast bus mode in IIC specification v2.1.)
   Please check the data hold time of your IIC device if it's 0 nS or not.
2. The IIC controller supports only IIC bus device(standard/fast bus mode), not C bus device.

Table 24-22. SD/MMC Interface Transmit/Receive Timing Constants

(VDDi = typ:1.25(1.15 ~ 1.5V), TA = -40 to 85°C, VDDOP3 = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ.	Max	Unit
SD Command output Delay time	tSDCD	0.3	–	1.0	ns
SD Command input Setup time	tSDCS	14.5	–	–	ns
SD Command input Hold time	tSDCH	-	–	0.1	ns
SD Data output Delay time	tSDDD	0.1	–	1.0	ns
SD Data input Setup time	tSDDS	15.0	–	–	ns
SD Data input Hold time	tSDDH	-	–	0.1	ns

Table 24-23. SPI Interface Transmit/Receive Timing Constants

(VDDi = typ:1.25(1.15 ~ 1.5V), TA = -40 to 85°C, VDDOP3 = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ.	Max	Unit
SPI MOSI Master Output Delay time	tSPIMOD	0.6	–	2.8	ns
SPI MOSI Slave Input Setup time	tSPISIS	0.0	–	0.0	ns
SPI MOSI Slave Input Hold time	tSPISIH	0.0	–	0.0	ns
SPI MISO Slave output Delay time	tSPISOD	5.6	–	19.0	ns
SPI MISO Master Input Setup time	tSPIMIS	0 / 15.0 *	–	–	ns
SPI MISO Master Input Hold time	tSPIMIH	0.0	–	0.0	ns

NOTES: * tSPIMIS value is 0 when the feedback clock use mode

Table 24-24. USB Electrical Specifications

(VDDi = typ:1.25(1.15 ~ 1.5V), TA = -40 to 85°C, VDDOP3 = 3.3V ± 0.3V)

Parameter	Symbol	Condition	Min	Max	Unit
Supply Current					
Suspend Device	ICCS			10	µA
Leakage Current					
Hi-Z state Input Leakage	ILO	0V < VIN < 3.3V	-10	10	µA
Input Levels					
Differential Input Sensitivity	VDI	| (D+) – (D-) |	0.2		V
Differential Common Mode Range	VCM	Includes VDI range	0.8	2.5	
Single Ended Receiver Threshold	VSE		0.8	2.0	
Output Levels					
Static Output Low	VOL	RL of 1.5Kohm to 3.6V		0.3	V
Static Output High	VOH	RL of 15Kohm to GND	2.8	3.6	
Capacitance					
Transceiver Capacitance	CIN	Pin to GND		20	pF

Table 24-25. USB Full Speed Output Buffer Electrical Characteristics

(VDDi = typ:1.25(1.15 ~ 1.5V), TA = -40 to 85°C, VDDOP3 = 3.3V ± 0.3V)

Parameter	Symbol	Condition	Min	Max	Unit
Driver Characteristics					
Transition Time Rise Time Fall Time	 TR TF	 CL = 50pF CL = 50pF	 4.0 4.0	 2.0 2.0	 ns
Rise/Fall Time Matching	TRFM	(TR / TF)	90	110	%
Output Signal Crossover Voltage	VCRS		1.3	2.0	V
Drive Output Resistance	ZDRV	Steady state drive	28	43	ohm

Table 24-26. USB Low Speed Output Buffer Electrical Characteristics

(VDDi = typ:1.25(1.15 ~ 1.5V), TA = -40 to 85°C, VDDOP3 = 3.3V ± 0.3V)

Parameter	Symbol	Condition	Min	Max	Unit
Driver Characteristics					
Transition Time Rising Time Falling Time 	 TR TF 	 CL = 50pF CL = 350pF CL = 50pF CL = 350pF	 75 75 	 300 300	 ns
Rise/Fall Time Matching	TRFM	(TR / TF)	80	120	%
Output Signal Crossover Voltage	VCRS		1.3	2.0	V

Table 24-27. CAMIF Timing Constants

(VDDi = typ:1.25(1.15 ~ 1.5V), TA = -40 to 85°C, VDDcam = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Units
VSYNC input Setup time	TssVsync	0	-	-	ns
VSYNC input Hold time	ThVsync	2	-	-	ns
HREF input Setup time	TssHref	0	-	-	ns
HREF input Hold time	ThHref	2	-	-	ns
DATA input Setup time	TssData	0	-	-	ns
DATA input Hold time	ThData	3	-	-	ns

25 MECHANICAL DATA

PACKAGE DIMENSIONS

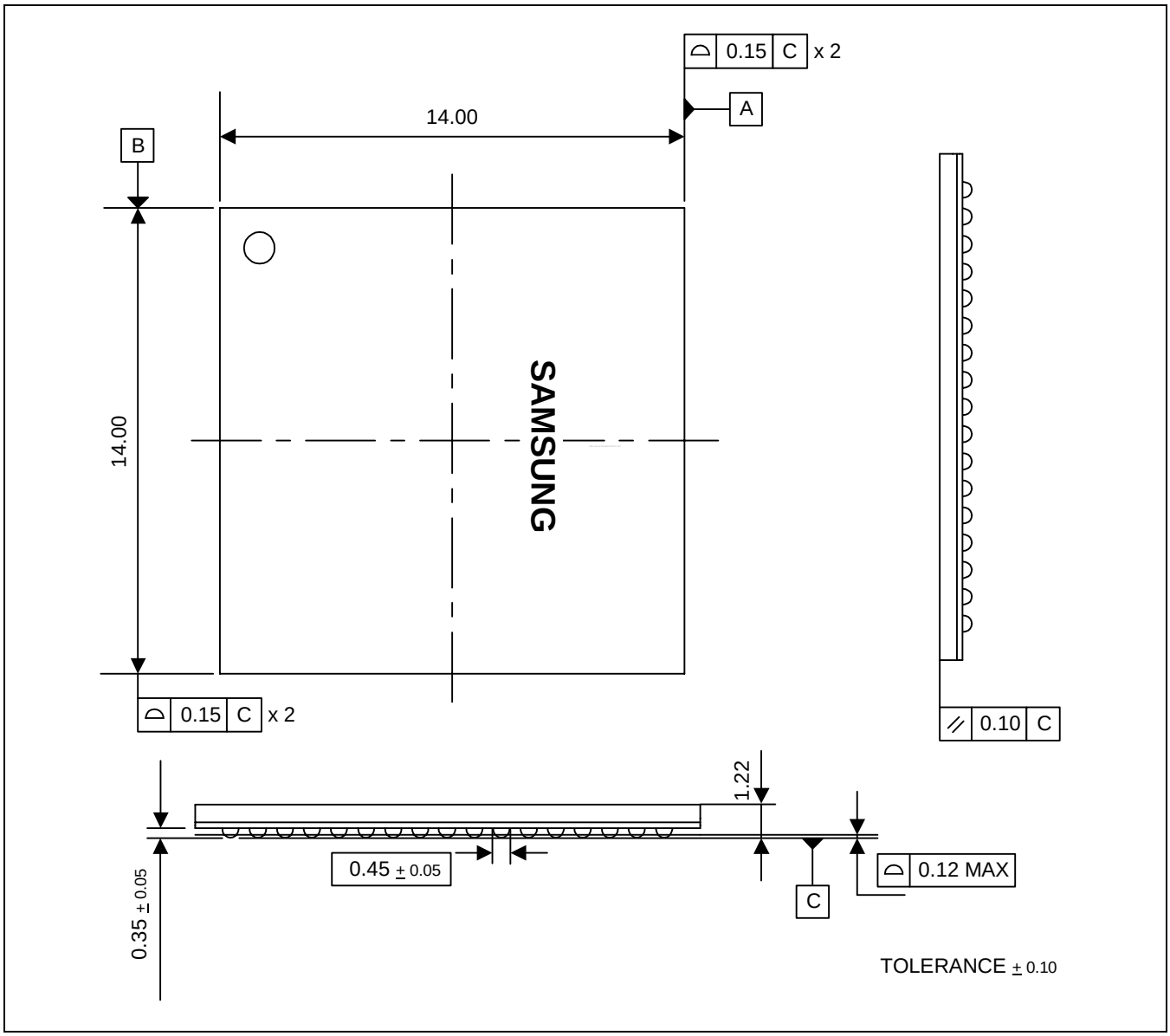


Figure 25-1. 289-FBGA-1414 Package Dimension 1 (Top View)

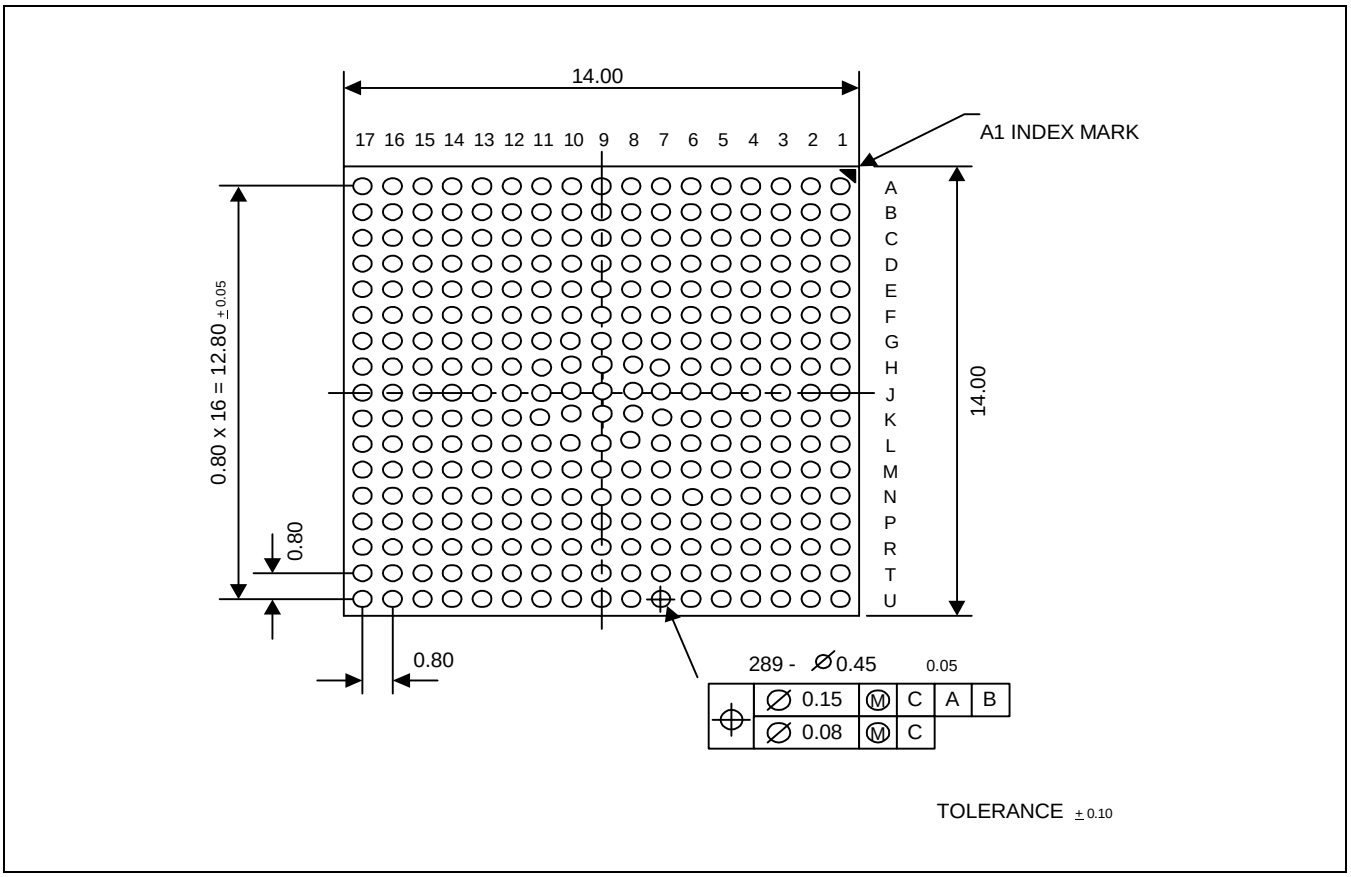


Figure 25-2. 289-FBGA-1414 Package Dimension 2 (Bottom View)

The recommended land open size is 390 – 410 um (0.39 – 0.41mm) diameter.