S3C2412X

32-BIT CMOS
MICROCONTROLLER
Application Note
- Power Design Guide -

Revision 1.0

SAMSUNG ELECTRONICS

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1. POWER DESIGN GUIDE

1-1. OVERVIEW

DVS(Dynamic Voltage Scaling) is useful to reduce power consumption in Idle mode & Stop mode.

The basic concept of DVS is to drop the Core and Internal voltage and reduce the power consumption when those blocks don't need to operate heavily.

There are two methods to reduce power consumption; one is drop the voltage while the internal blocks does not work or the system operates slowly. The other is lengthening the system clock speed to reduce power consumption.

DVS uses the two methods, voltage scaling and change clocking.

1-2. RECOMMENDED OPERATING CONDITIONS

Table 1-1 Recommended Operating Conditions

Parameter	Symbol		Min	Typ	Max	Unit
DC Supply Voltage for Alive Block:200MHz	VDDALIVE		1.15	1.25	1.35	V
DC Supply Voltage for Alive Block:266MHz	VDDALIVE		1.15	1.25	1.5	
DC Supply Voltage for internal	ARMCLK / HCLK					
	266 / 133 Mhz	VDDI VDDI_MPLL VDDI_UPLL	1.15	1.25	1.50	
	200 / 100 Mhz	VDDI VDDI_MPLL VDDI_UPLL	1.15	1.25	1.35	
	133 / 133 Mhz	VDDI VDDI_MPLL VDDI_UPLL	1.15	1.25	1.50	
	100 / 100 Mhz	VDDI VDDI_MPLL VDDI_UPLL	1.15	1.25	1.50	
	66 / 66 Mhz	VDDI VDDI_MPLL VDDI_UPLL	1.10	1.15	1.35	
	50 / 50 Mhz	VDDI VDDI_MPLL VDDI_UPLL	1.10	1.15	1.35	
DC Supply Voltage for ARM Core	ARMCLK / HCLK					
	266 / 133 Mhz	VDDI VDDI_MPLL VDDI_UPLL	1.30	1.40	1.50	
	200 / 100 Mhz	VDDI VDDI_MPLL VDDI_UPLL	1.15	1.25	1.35	
	133 / 133 Mhz	VDDI VDDI_MPLL VDDI_UPLL	1.15	1.25	1.35	
	100 / 100 Mhz	VDDI VDDI_MPLL VDDI_UPLL	1.15	1.25	1.35	
	66 / 66 Mhz	VDDI VDDI_MPLL VDDI_UPLL	1.10	1.15	1.35	

Parameter	Symbol		Min	Typ	Max	Unit
	50 / 50 Mhz	VDDI VDDI_MPLL VDDI_UPLL	1.10	1.15	1.35	
DC Supply Voltage for I/O Block	VDDOP1,2		2.3	2.5V / 2.8V / 3.3V	3.6	
DC Supply Voltage for I/O Block	VDDOP3,4		3.0	3.3V	3.6	
DC Supply Voltage for Memory Interface	VDDMOP		1.7	1.8V / 2.5V / 3.3V	3.6	
DC Supply Voltage for RTC	RTCVDD		2.5V	3.0V	3.6	
DC Supply Voltage for ADC	VDDA_ADC		3.3-5%	3.3 V	3.3+5%	
DC Input Voltage	VIN		3.0	3.3 V	3.6	
			2.3	2.5 V	2.7	
			1.7	1.8 V	1.9	
DC Output Voltage	VOUT		3.0	3.3 V	3.6	
			2.3	2.5 V	2.7	
			1.7	1.8 V	1.9	
Operating Temperature	TA		Extended	-20 to 70		^{o}C
			Industrial	-40 to 85		^{o}C

NOTES:

1. VDDOP includes VDDOP1, VDDOP2, VDDOP3, VDDOP4
2. VDDMOP includes VDDMOP1, VDDMOP2, VDDMOP3, VDDMOP4, VDDMOP5, VDDMOP6, VDDMOP7.
3. DC input/output voltage is depend on the voltage of IO supply voltage corresponding IOs.
4. Load Capacitancd(CL) < 50pF. If max CL is changed, above operation conditions must be changed.

*; The specification especially related with VDDIARM is a preliminary. So, It can be changed.

1-3. POWER SCHEMATIC DESIGN FOR DVS

Applicable DVS power supply pins are VDDi(Internal block power) and VDDiarm(ARM926EJS power). To use DVS, the system power has to be supplied two variable voltages. One for normal operation, the other for lower level voltage (for DVS). The DVS High and Low voltage is as follows.

Table 1-2. DVS voltage level

DVS Pins	Voltage spec.	Normal operating voltage	DVS low voltage
VDDiarm VDDi/VDDmpll/VDDupll	266MHz: 1.4V(1.26V ~ 1.55V)	266MHz: 1.4V	1.15V

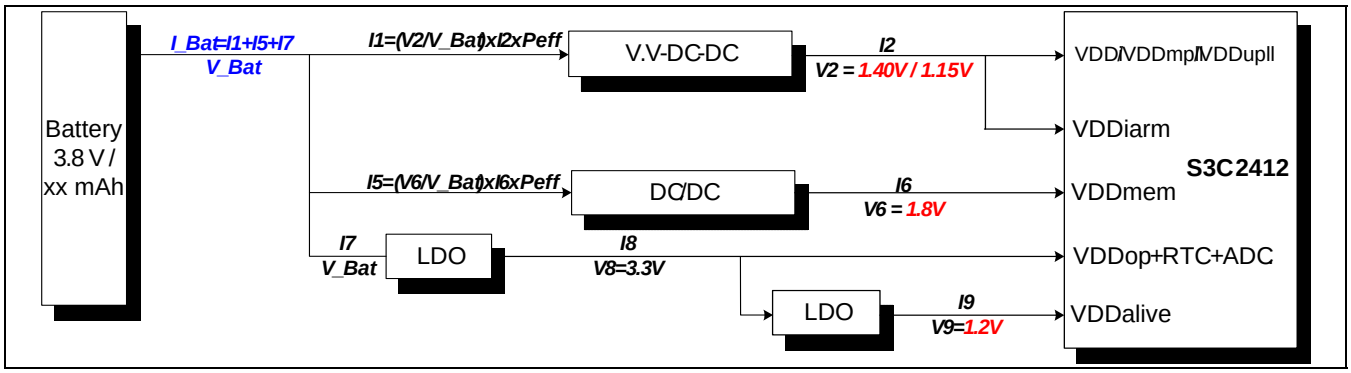

Figure 1-1. Power Scheme Diagram : 266MHz

Hardware Implementation of DVS

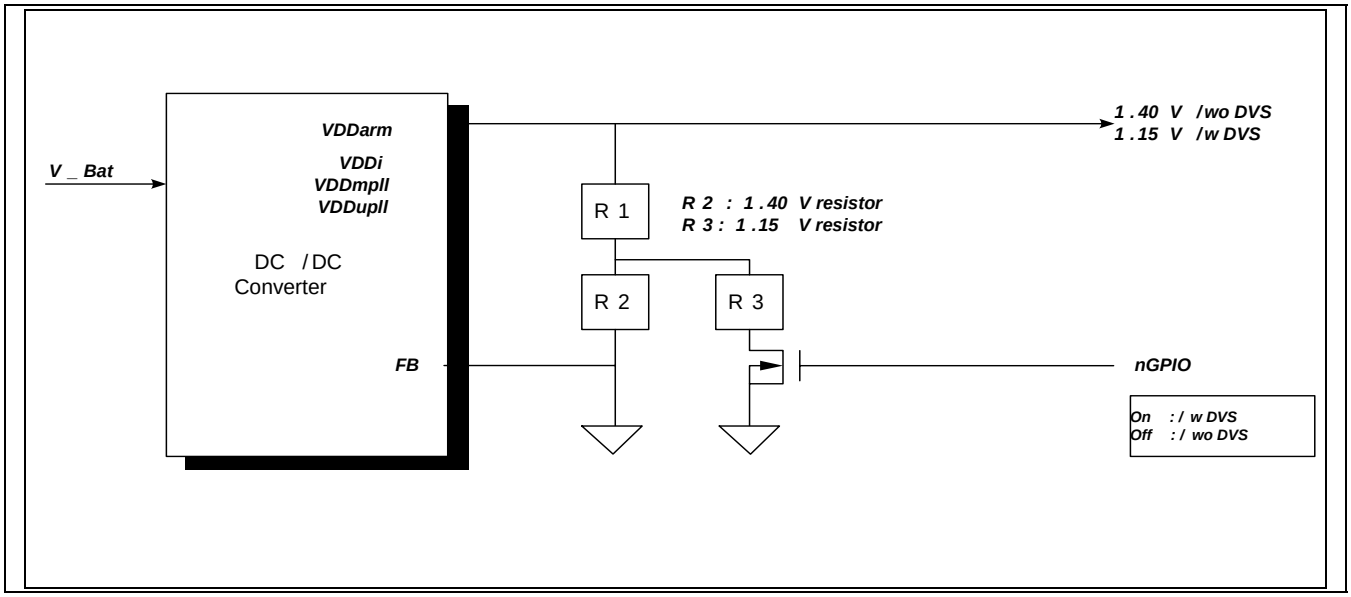

Figure 1-3. Power Scheme Diagram :266MHz

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1-4. DVS SOFTWARE OPERATING GUIDE

Refer to DVS software application note

1-5. POWER CONSUMPTION OF DVS

Table 1-3 shows how much the power consumption will be reduced when using DVS for Linux.

Table 1-3. Core current Consumption

DVS Type	OS Idle State	Core Power [mW]	Difference Without→with
A	DVS Off	214.8	113.8mW(53%↓)
	DVS On	101.0	
AI	DVS Off	79.4	27.4mW(34.5%↓)
	DVS On	52	
B	DVS Off	214.8	154.3mW(71.8%↓)
	DVS On	60.5	

NOTE: Type AI is Type A with CPU Idle

Test condition:

— Core Voltage = VDDi = 1.4V, VDDiarm =1.4V
(Voltage of VDDUPLL/VDDMPLL are same with Core Voltage).

— For DVS the Core voltage will be down to 1.15V

(1) No threads ready to run on Linux 2.6.16.11

(2) OS idle mode : FCLK:HCLK:PCLK = (266:133:66), (133:133:66) MHz for 266MHz in Type A
(266:133:66), (133:133:66) MHz for 266MHz in Type AI.
(266:133:66), (66:66:66) MHz for 266MHz. In Type B

(3) Sample # : NZO75NN
OS timer scheduler: 10msec.