MF1542-01

EPSON

LCD Controller ICs

S1D13700

Technical Manual

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✻ In this manual, Zilog's Z80-CPU or its equivalent shall be called Z80, Intel's 8085A or its equivalent shall be called 8085 and Motorola's MC6809 and MC6802 or their equivalents shall be called 6809 and 6802, respectively.

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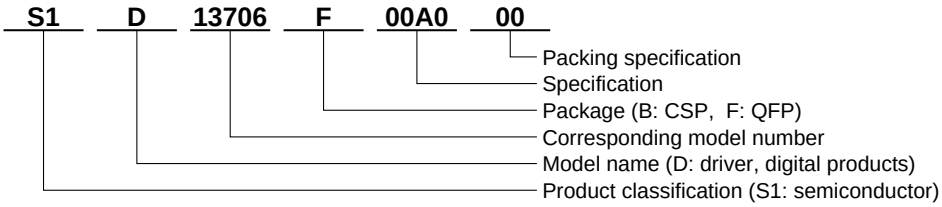
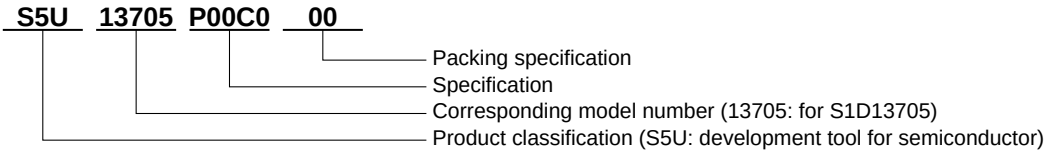
Configuration of product number

● Devices



● Evaluation Board



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1 OVERVIEW

The S1D13700 Controller displays text and graphics on a midsize, dot-matrix liquid crystal display (LCD). A very flexible, low-power display system can be configured using the S1D13700 in combination with various LCD modules. The character code or bitmap display data from the microprocessor is temporarily stored in frame buffer memory, then periodically read out and converted into LCD module signals for output to the LCD. Its abundant command functions make it possible to overlay the text and graphic screens, scroll the screen in any direction (except in grayscale mode), and split the screen for multi-window display, as well as display pictures in grayscale mode. Moreover, the embedded-type 32-KB SRAM display buffer, built-in LCD module control circuit, and high-speed character generator allow you to build an LCD control block with only a few external circuits.

1.1 Features

- Number of display dots:..... Text display mode
  80 columns x 30 rows (monochrome, 1 bpp)
  40 columns x 30 rows (4 gray shades, 2 bpp)
  30 columns x 20 rows (16 gray shades, 4 bpp) + graphic screen overlay

  Graphic display mode
  640 dots x 240 dots (monochrome, 1 bpp)
  320 dots x 240 dots (4 gray shades, 2 bpp)
  240 dots x 160 dots (16 gray shades, 4 bpp) x three-screen overlay
- Three display modes: ..... Text display mode, graphic display mode, and text/graphic overlay mode (Layered display functions)
- Grayscale display function: ..... 1 bpp, 2 bpp, or 4 bpp selectable
- Flexible scroll function: ..... The text/graphics display screen can be easily moved and smoothly scrolled horizontally.
- Frame buffer: ..... Up to 32 KB of SRAM, virtual screen configuration
- Internal character generator: ..... 160 characters (Internal mask ROM dots 5 x 7 dots) + 64 characters (internal CGRAM 8 dots x 16 dots) or 256 characters (internal CGRAM 8 dots x 16 dots)
- Drive duty cycle: ..... Can be set without any required increments from 1/2 up to 1/256 duty cycles.
- MPU interface ..... Generic, 6800 series or M68K series
  Direct access or indirect access selectable
- Power supply voltage ..... 5 V/3.3 V (dual power supplies) with MPU interface and LCD interface pins independently selectable or 3.3 V (single power supply)
- Package: ..... 64-pin QFP13 (Pd-free)

1.2 System Overview

Positioned midway between the MPU and LCD panel, the S1D13700 enables the sending and receiving of control commands and data, and access of registers by the MPU for display, thus making it possible to control up to 32 Kbytes of internal display memory (VRAM).

Moreover, because the S1D13700 has a built-in a control circuit for LCD units, it is possible to take full advantage of the features of midsize, dot-matrix liquid crystal display units without using any external circuit.

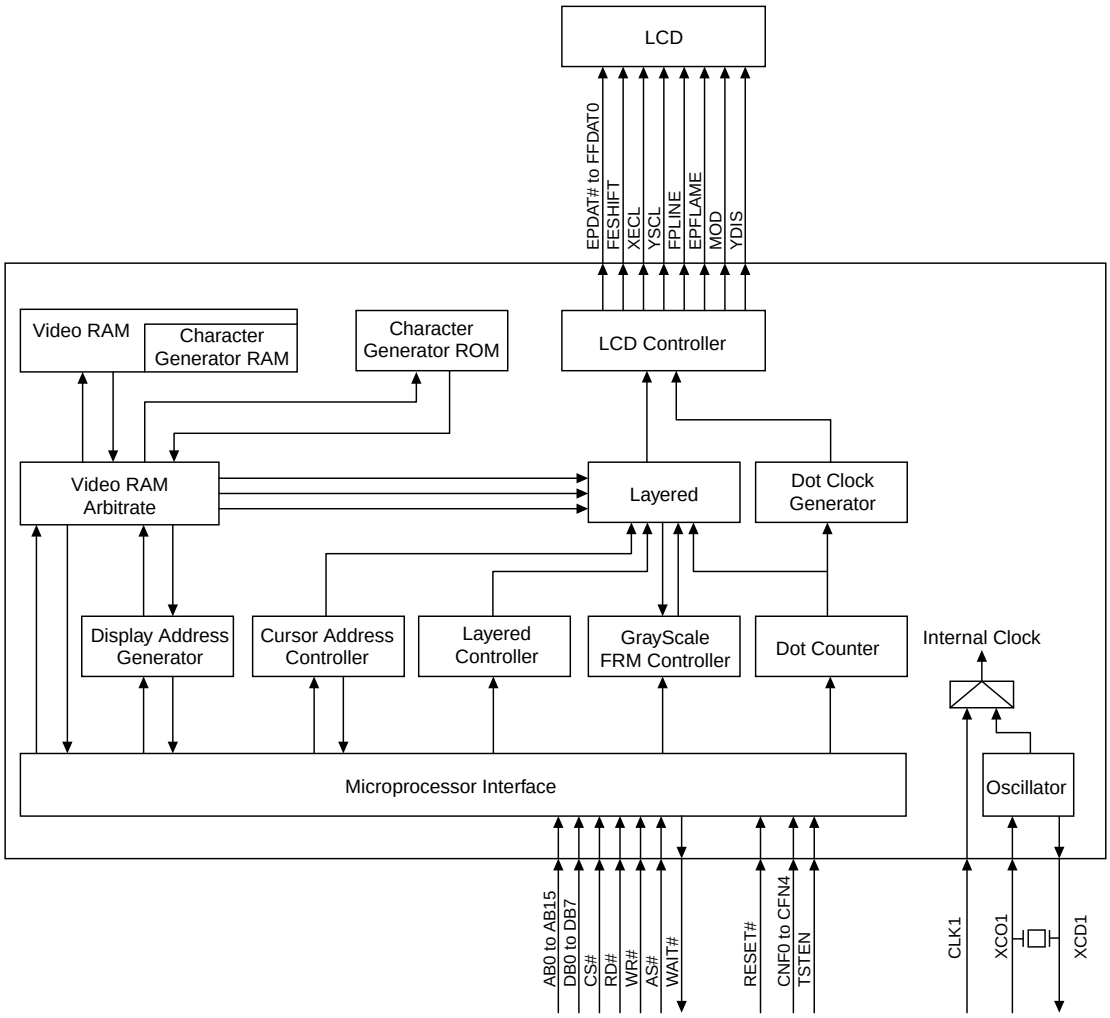


Figure 1-1 Block diagram of the S1D13700

The S1D13700 divides the display memory space into the four areas shown below. When this configuration is combined with the layered (overlaid) display and flexible scroll functions of the S1D13700, it is possible to greatly reduce the MPU load when inverting or underlining text, displaying graphs with text, or creating simple animation.

The S1D13700 uses the display memory space by dividing it into the four areas shown below to realize the layered display functions using only a single controller.

Example of display memory mapping by the S1D13700

(1)Character code table

- A memory area to store character code when displaying text
- 1 character = 8 bits
- Variable table mapping (by altering the scroll start address)

(2)Graphic data table

- A memory area to store bitmap data
- 1 word = 8 bits
- Variable table mapping

(3)CG RAM table (for external characters)

- A character generator whose character patterns can be altered by the MPU as desired
- Maximum 8 x 16 bits (16 bytes per character)
- Maximum 64 discrete characters, or 256 characters when not using CGROM
- Internal CG RAM used
- Variable table mapping

(4)CG ROM table

- Maximum 5 x 7 bits
- Maximum 160 characters
- Mapped to addresses 8030h–85AFh. Data cannot be read out by the MPU.

To make the most of the above-mentioned functions of the S1D13700, a high-speed interfacing method is used to enable pipelined command processing between the MPU and S1D13700. Most commands of the S1D13700 are processed so that the controller completes the processing of any input command before the next command is issued from the MPU. Therefore, the MPU does not need to frequently check the status of the S1D13700, and is not kept waiting by the S1D13700. Thus, the high-speed interfacing method adopted for the S1D13700 helps minimize possible reduction in the MPU's processing capability.

Moreover, the MPU can access the above display space at any time irrespective of display mode (except in sleep mode).

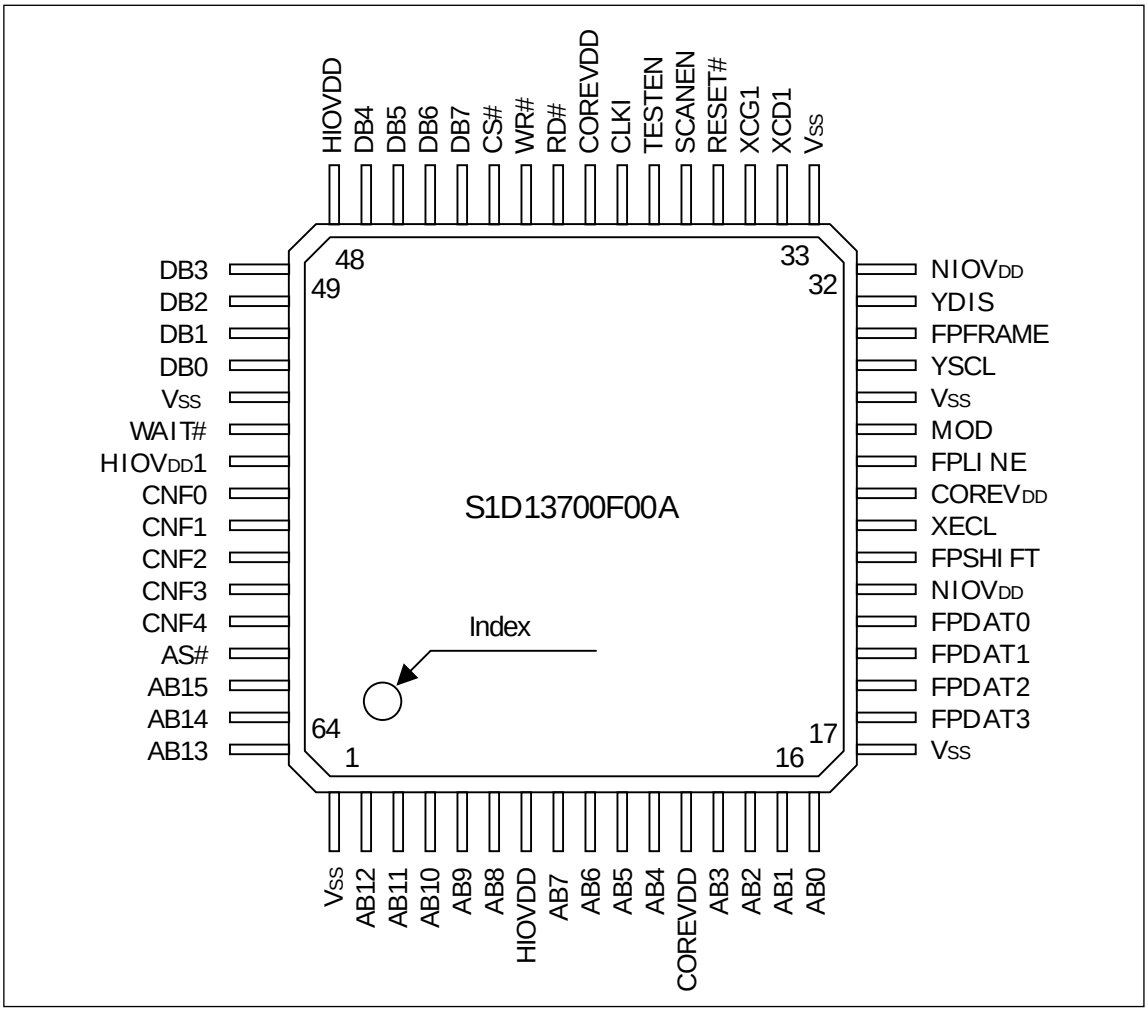
1.3 List of Abbreviations

Abbreviation	Meaning
• AB	Address
• AP	Address pitch
• C	Text display mode (Denotes a command in command code descriptions.)
• CD	Cursor movement direction
• CG	Character generator
• CGRAM ADR	Character generator memory offset address
• CM	Cursor shape
• C/R	Number of characters per line
• CRX	Cursor size in the X direction
• CRY	Cursor size in the Y direction
• CSRDIR	Direction of cursor movement
• CSRFORM	Cursor shape
• CSRR	Cursor address read
• CSRW	Cursor address write
• DM	Display mode
• FC	Flashing cursor
• f_{FR}	Frame frequency
• f_{OSC}	Oscillation frequency
• FP	Layer flashing
• FY	Character field in the Y direction
• G	Graphic display mode
• GLC	Graphic liquid crystal unit controller
• HDOT SCR	Smooth scrolling in horizontal direction
• IV	Inverse
• L	Layer
• L/F	Number of lines per screen
• MREAD	Display memory readout
• MX	Screen composition method
• MWRITE	Display memory write
• OV	Screen overlay
• OVRAY	Screen overlay
• P	Parameter
• R	Row
• RAM	Random access memory
• ROM	Read-only memory
• SAD	Display start address
• SL	Number of scanning lines
• TC/R	Total number of characters per line
• VRAM	Display memory
• MOD(WF)	AC drive waveform
• W/S	Double common/single common
• XDr	X direction driver
• YDr	Y direction driver

2 PINS

2.1 Pin Connection

2.1.1 Pin Assignments



2.1.2 Pin Description

Key :

I = Input

O = Output

IO = Input/output

P = Power supply

HIBC = CMOS input

HIBH = CMOS Schmitt input

HIBCD1 = CMOS input with pulldown resistor (60 ohms typ. at 5.0 V)

HOB2T = Normal buffer (8 mA/-8 mA at 5 V)

HBC2T = LVTTL I/O buffer (6 mA/-6 mA at 3.3 V)

HTB2T = Tri-state output (6 mA/-6 mA at 3.3 V)

HLIN = Transparent input

HLOT = Transparent output

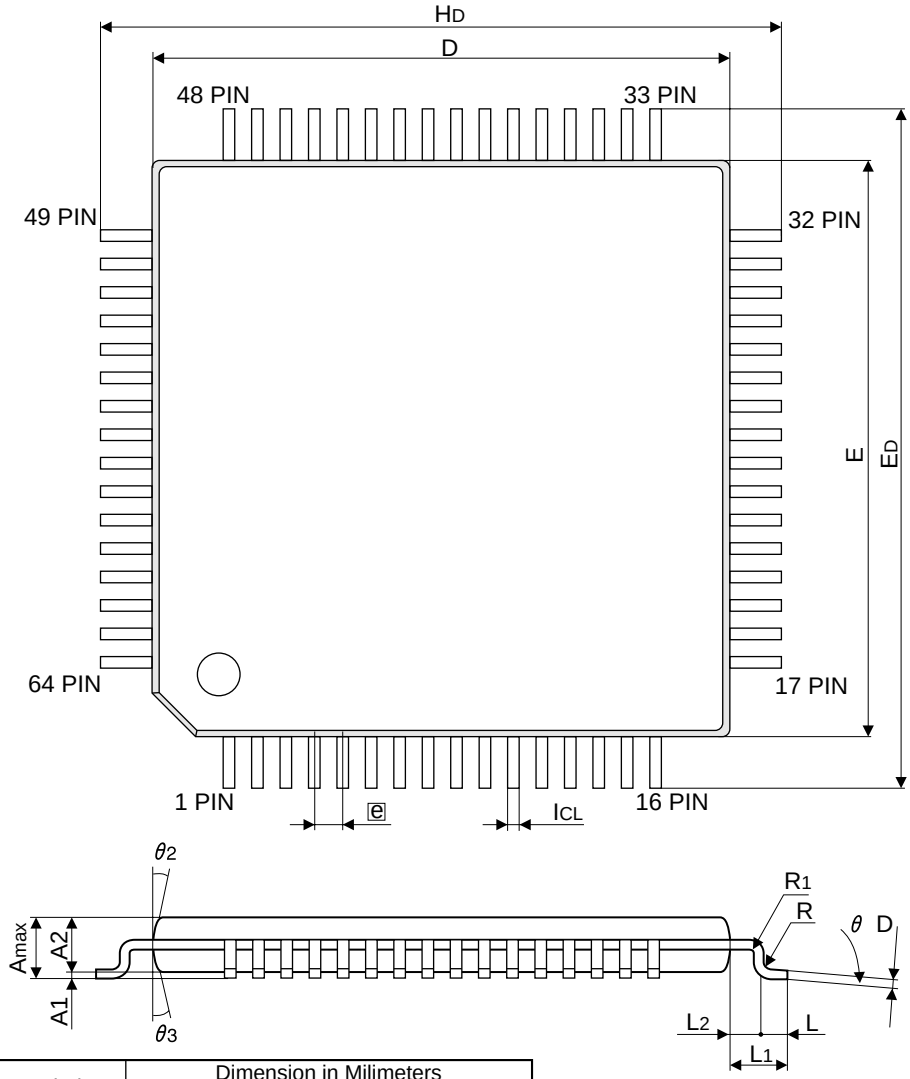
ITST1 = Test mode control input with pulldown resistor (50 ohms typ. at 3.3 V)

Pin Name	Pin No.	I/O Type	I/O Voltage	I/O Cell	RESET# State	Description
HIOVDD(V_{DD})	7 • 48 • 55	P	HIOVDD	—	—	Power supply for host interface
NIOVDD(V_{DD})	22 • 32	P	NIOVDD	—	—	Power supply for LCD interface
COREVDD(V_{DD})	12 • 25 • 40	P	COREVDD	—	—	Power supply for core logic
V_{SS}	1 • 17 • 28 • 33 • 53	P	V_{SS}	—	—	Ground
CLKI	39	I	HIOVDD	HIBH	—	Externally sourced system clock
XCG1(XG)	35	I	HIOVDD	HLOT	—	Gate input for oscillator
XCD1(XD)	34	O	HIOVDD	HLIN	—	Drain output for oscillator
CNF0 – CNF4 (SEL0 – SEL4)	56-60	I	HIOVDD	HIBH	0	Input pin for S1D13700 settings
DB0 – DB7 (D0 – D7)	44-47 • 49-52	IO	HIOVDD	HBC2T	Hi-Z	Data bus for MPU interface
AB0 – AB15 (A0 – A15)	2-6 • 8-11 • 13-16	I	HIOVDD	HIBC	0	Address bus for MPU interface
RD#	41	I	HIOVDD	HIBH	1	Read strobe for MPU interface
WR#	42	I	HIOVDD	HIBH	1	Write strobe for MPU interface
CS#	43	I	HIOVDD	HIBH	1	Chip select for MPU interface
WAIT#	54	O	HIOVDD	HOB2T	Hi-Z	Wait output for MPU interface
AS#	61	I	HIOVDD	HIBC	1	Address strobe for MPU interface
FPDAT0 – FPDAT3(XD0 – XD3)	18-21	O	NIOVDD	HOB2T	X	Data bus for X driver
FPSHIFT(XSCL)	23	O	NIOVDD	HOB2T	X	Shift clock for X driver
XECL	24	O	NIOVDD	HOB2T	X	X driver enable chain clock
FPLINE(LP)	26	O	NIOVDD	HOB2T	X	Latch pulse
MOD(WF)	27	O	NIOVDD	HOB2T	X	Frame signal
YSCL	29	O	NIOVDD	HOB2T	X	Scan shift clock
FPFRAME (YD)	30	O	NIOVDD	HOB2T	X	Scan start pulse

Pin Name	Pin No.	I/O Type	I/O Voltage	I/O Cell	RESET# State	Description
YDIS	31	O	NIOVDD	HOB2T	L	LCD power-down output
RESET# (RES)	36	I	HIOVDD	HIBH	0	Reset input
TESTEN	38	I	HIOVDD	ITST1	0	Test mode setup input
SCANEN	37	I	HIOVDD	HIBCD1	0	Test mode setup input

Note: The corresponding pin names of the earlier LCD controller (i.e., S1D13305) are enclosed in parentheses.

2.1.3 Package Dimensions



	Symbol	Dimension in Milimeters		
		Min.	Nom.	Max.
*	E	10.1	10.2	10.3
*	D	10.1	10.2	10.3
	Amax			1.2
	AL		0.1	
	AP	0.9	1	1.1
	e		0.5	
*	ICL	0.17	0.2	0.27
*	CL	0.125	0.15	0.2
	ÉΔ	0°		10°
	L	0.3	0.5	0.7
	L1		1	
	L2		0.5	
	HE	11.6	12	12.4
	HD	11.6	12	12.4
	ÉΔ2		15°	
	ÉΔ3		15°	
	R		0.1	
	R1		0.1	

* E,D Excluding the tie bar cutting stub.
ICL Lead width of basemetal.
CL Lead thickness of basemetal.

1 = 1mm

2.2 Pin Functions

2.2.1 Power Supply Pins

Pin Name	Function
HIOVDD	Power supply for host interface I/O drive. Connect a 5 V or 3.3 V power supply to this pin. (Shared with MPU power supply pin, V_{CC}) Note 1
NIOVDD	Power supply for LCD I/O drive other than host of interface I/O. Connect a 5 V or 3.3 V power supply to this pin. Note 1
COREVDD	Power supply for internal logic. Connect a 3.3 V power supply to this pin. Note 1
V_{SS}	Connects to 0 V earth ground (GND).

Note 1: Because the spike power supply current in the S1D13700 could reach levels that are several tens higher than the average amount of dynamically consumed current, measures must be taken to minimize the power supply impedance of the S1D13700. For example, use thick power supply wiring from the power supply to the S1D13700 or insert a capacitor of 0.47 mF or more (with good frequency characteristics) between V_{DD} and V_{SS} close to the S1D13700. These measures will help to reduce power supply impedance.

2.2.2 Oscillator and Clock Input Pins

<table>
<tr><td>CLKI</td><td>Generally used as the input clock source for the bus and memory clocks.</td></tr>
<tr><td>XCG1
XCD1</td><td>These pins are used to connect a crystal resonator for the internal clock-generating oscillator. For details, see Section 4.2 “Oscillator Circuit” on page 70. To use the external clock (fed in from the CLKI pin), fix XCG1 for input with a pullup resistor and leave XCD1 open. Note 2</td></tr>
<tr><td>CNF0
CNF1</td><td>Input, active low
Set the frequency divide ratio of the display clock (pixel clock) relative to CLKI or an internally generated system clock.
<table>
<tr><th>CNF3</th><th>CNF2</th><th>Clock Retio</th></tr>
<tr><td>0</td><td>0</td><td>1/4</td></tr>
<tr><td>0</td><td>1</td><td>1/8</td></tr>
<tr><td>1</td><td>0</td><td>1/16</td></tr>
<tr><td>1</td><td>1</td><td>Not USE</td></tr>
</table></td></tr>
</table>

Note 2: Because the external clock fed in from the CLKI pin is needed to internally generate the fundamental timing in the S1D13700, the oscillation characteristic requirements given in Section 5.4.3 “External Clock Input Characteristics” on page 92 must be met.

2.2.3 System Bus Connecting Pins

<table>
<tr><td>DB0 – DB7</td><td>Tristate input/output, active high
These pins comprise an 8-bit bidirectional data bus, which is connected to the 8-bit or 16-bit MPU data bus.</td></tr>
<tr><td>CNF2
CNF3</td><td>Input, active high
The S1D13700 allows the MPU interface format to be changed depending on how CNF2 and CNF3 are set, so that it can be connected directly to the 80-series MPU (e.g., Z80® or GenericBus), 68-series MPU (6809 or 6802), or the MC68K-series MPU (68000) bus.
<table>
<tr><th>CNF3</th><th>CNF2</th><th>Mode</th><th>AB15 – AB1</th><th>AB0</th><th>RD#</th><th>WR#</th><th>CS#</th><th>DB7 – DB0</th><th>WAIT#</th><th>AS#</th></tr>
<tr><td>0</td><td>0</td><td>80 series</td><td>↑</td><td>↑</td><td>↑</td><td>↑</td><td>↑</td><td>↑</td><td>↑</td><td>–</td></tr>
<tr><td>0</td><td>1</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td></tr>
<tr><td>1</td><td>0</td><td>6800</td><td>↑</td><td>↑</td><td>E</td><td>R/W#</td><td>↑</td><td>↑</td><td>–</td><td>–</td></tr>
<tr><td>1</td><td>1</td><td>MC68K</td><td>↑</td><td>↑</td><td>LDS#</td><td>R/W#</td><td>↑</td><td>↑</td><td>DTACK#</td><td>↑</td></tr>
</table>
Settings marked with * are inhibited.
Note 3</td></tr>
</table>

Note 3: Normally, CNF2 and CNF3 should be corrected directly to power supply V_{DD} or V_{SS} to prevent the mixture of noise. Should noise be mixed in, insert a capacitor between the CNF2 and CNF3 lines and V_{SS}, as close to the IC pins as possible. This will help to effectively eliminate noise.

<table>
<tr><td>AB15 – AB1
AB0</td><td>Input, active high
Normally, the MPU address bus is connected to these pins. The data bus signal is discriminated by a combination of RD# and WR# signals, or R/W#, E, and LDS signals, as listed in the table below.</td></tr>
<tr><td>CMF4</td><td>Input: CNF4 = 0 selects direct access; CNF4 = 1 selects indirect access.
<Direct access for the 80-series interface>
<table>
<tr><th>CNF4</th><th>AB15 – AB1</th><th>AB0</th><th>RD#</th><th>WR#</th><th>Function</th></tr>
<tr><td>0</td><td>0or1</td><td>0or1</td><td>0</td><td>1</td><td>Read from command/parameter registers</td></tr>
<tr><td>0</td><td>0or1</td><td>0or1</td><td>1</td><td>0</td><td>Write to command/parameter registers</td></tr>
</table>
*AB15–AB0 are used as register addresses.

<Indirect access for the 80-series interface>
<table>
<tr><th>CNF4</th><th>AB15 – AB1</th><th>AB0</th><th>RD#</th><th>WR#</th><th>Function</th></tr>
<tr><td>1</td><td>–</td><td>0</td><td>0</td><td>1</td><td>–</td></tr>
<tr><td>1</td><td>–</td><td>1</td><td>0</td><td>1</td><td>Data (display data and cursor address) read</td></tr>
<tr><td>1</td><td>–</td><td>0</td><td>1</td><td>0</td><td>Data (display data and parameter) write</td></tr>
<tr><td>1</td><td>–</td><td>1</td><td>1</td><td>0</td><td>Command write (code only)</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>CMF4</td><td>Input: CNF4 = 0 selects direct access; CNF4 = 1 selects indirect access.
<Direct access for the 68-series interface>

<table>
<tr><th>CNF4</th><th>AB15 – AB1</th><th>AB0</th><th>WR# (R/W#)</th><th>RD# (E)</th><th>Function</th></tr>
<tr><td>0</td><td>0or1</td><td>0or1</td><td>1</td><td>1</td><td>Read from command/parameter registers</td></tr>
<tr><td>0</td><td>0or1</td><td>0or1</td><td>0</td><td>1</td><td>Write to command/parameter registers</td></tr>
</table>
*A15–A0 are used as register addresses.

<Indirect access for the 68-series interface>

<table>
<tr><th>CNF4</th><th>AB15 – AB1</th><th>AB0</th><th>WR# (R/W#)</th><th>RD# (E)</th><th>Function</th></tr>
<tr><td>1</td><td>–</td><td>0</td><td>1</td><td>1</td><td>–</td></tr>
<tr><td>1</td><td>–</td><td>1</td><td>1</td><td>1</td><td>Data (display data and cursor address) read</td></tr>
<tr><td>1</td><td>–</td><td>0</td><td>0</td><td>1</td><td>Data (display data and parameter) write</td></tr>
<tr><td>1</td><td>–</td><td>1</td><td>0</td><td>1</td><td>Command write (code only)</td></tr>
</table>
</td></tr>
<tr><td>RD# (E)</td><td>• When the 80-series MPU is connected
Input, active low
This is the strobe signal used by the MPU as it reads data or status flags from the S1D13700. The data bus of the S1D13700 is in output mode while this signal remains low.
• When the 68-series MPU is connected
Input, active high
This is an enable clock input pin of the 68-series MPU.
• When the MC68K-series MPU is connected
Input, active low
Normally, this is an LDS# input pin of the MC68K-series MPU.</td></tr>
<tr><td>WR# (R/W#)</td><td>• When the 80-series MPU is connected
Input, active low
This is the strobe signal used by the 80-series MPU as it writes data or parameters to the S1D13700. The S1D13700 latches the data bus signal at the rising edge of WR#.
• When the 68-series MPU is connected
Input
This is a R/W# control signal input pin of the 68-series MPU.
R/W# = HIGH : READ
R/W# = LOW : WRITE
• When the MC68K-series MPU is connected
Input
This is a R/W# control signal input pin of the MC68K-series MPU.
R/W# = HIGH : READ
R/W# = LOW : WRITE</td></tr>
<tr><td>CS#</td><td>Input, active low
This chip select signal is used by the MPU to activate the S1D13700 before accessing it, and is normally derived by decoding the address bus signal.</td></tr>
</table>

WAIT#	This signal forcibly inserts a wait state into the system during data transfer. When this signal is deasserted, data transfer is completed. After data transfer is complete, this signal is left free (placed in high-impedance state). • When the 80-series MPU is connected Tri-state output, active low (wait state when asserted low) Connect this pin to WAIT# of the 80-series MPU. • When the 68-series MPU is connected Unused. Therefore, leave this pin open. • When the MC68K-series MPU is connected Tri-state output, active low (no wait state when asserted low) This pin serves as the DTACK# pin of the MC68K-series MPU.
AS#	• When the 80-series MPU is connected Unused. Therefore, fix this pin low. • When the 68-series MPU is connected Unused. Therefore, fix this pin low. • When the MC68K-series MPU is connected Input, active low Connect this pin to the address strobe AS# pin of the MC68K-series MPU.
RESET#	Input, active low The RESET# input is used to initially reset the S1D13700 in hardware. Note 4

Note 4: Although this pin is a Schmitt trigger input to prevent the S1D13700 from being inavertently reset by noise, care must be taken when intentionally lowering the power supply voltage.

2.2.4 LCD Driver Control Pins

The S1D13700 can directly control both the X and Y drivers based on an enable chain, which is a method of effectively reducing the amount of current consumption needed to drive dot-matrix liquid crystal display elements.

FPDAT0 – FPDAT3	Output, active high This 4-bit dot data bus for the X driver (column driver) is connected to the data input pins of the X driver.
FPSHIFT	Output, falling edge triggered This signal causes the dot data bus signals (FPDAT0–FPDAT3) to be stored in the X driver at the signal's falling edge, and thus functions as a shift clock for the internal shift register of the X driver. To reduce power consumption, this clock is turned off until the MPU starts sending data for the next display line after outputting the LP signal. (For details, see Section 5.4.4 "LCD Control Signal Timing Characteristics" on page 93.)
XECL	Output, falling edge triggered XECL is a dedicated clock signal for the X drivers cascaded by an enable chain. It causes the enable signal to be successively passed to the next X driver every 16 XSCL periods.
FPLINE	Output, falling edge triggered For the liquid crystal display elements to be successively driven, the X driver contains a circuit to latch each output bit of the internal shift register at the falling edge of LP. This signal is output for every display line.
MOD	Output This signal provides a one-frame interval for the X and Y drivers to determine the AC drive waveform for the LCD panel. Two types of cyclic signals are output depending on how the System Set command parameters are set.
YSCL	Output, active high, rising edge triggered This signal is a clock for the Y driver, and is equivalent to XSCL for the X driver. The Y data signal (YD) is stored in the Y driver at the beginning of a frame, and YSCL is used as an internal shift clock.
FPFRAME	Output, active high YD is data for the Y driver, and is a cyclic signal output at the first display line interval of a frame. The electrodes on the common side of liquid crystal display elements are sequentially scanned as the YD signal is sequentially shifted inside the Y driver synchronously with the YSCL signal.
YDIS	Output, active high This signal is used to power down the LCD unit and is held high during the display period. Note 5

Note 5: The YDIS signal goes low at a time equivalent to one to two frames after the sleep command is written. When the YDIS signal goes low, all Y driver outputs are forcibly brought to an intermediate level (unselected), thus causing display to turn off. Therefore, to power off the LCD unit, the liquid crystal drive power supply (with relatively large steady-state current) must be turned off at the same time display is turned off by using the YDIS signal.

2.2.5 TEST Control Pins

TESTEN	Input, active high Test-enable input used only for production testing (with type-1 pulldown resistor, 50 ohms typ. at 3.3 V).
SCANEN	Input, active high Test-enable input used only for production testing (with type-1 pulldown resistor, 50 ohms typ. at 3.3 V).

3 COMMANDS AND COMMAND REGISTERS

3.1 Types of Commands (when Indirectly Interfaced)

When indirect mode is selected for the system interface, use commands to set up the display.

The table below lists the types of commands, including the code of each command.

Purpose	Command	Code												Command description	Parameters following the command		Remarks
		WR#	RD#	AB0	DB BIN 7	6	5	4	3	2	1	0	DB HEX		No. of parameters	See pages	
Operation control	SYSTM SET	1	0	1	0	1	0	0	0	0	0	0	40	Sets initial operation and window size.	8	19	
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Sleep operation.	0	27	Note 1
Display control	DISPON/OFF	1	0	1	0	1	0	1	1	0	0	D	58 • 59	Instructs to turn display on or off and make the screen flash on and off.	1	28	Note 1
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Sets the display start address and display area.	10	29	
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Sets the cursor shape, etc.	2	37	
	CSRDIR	1	0	1	0	1	0	0	1	1	CD 1	CD 0	4C – 4F	Sets the direction of cursor movement.	0	38	
	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Instructs screen overlay mode.	1	39	
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Sets the start address of CG RAM.	2	43	
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Sets the horizontal direction dot unit and scroll position.	1	44	
	GRAY SCALE	1	0	1	0	1	1	0	0	0	0	0	60	Sets grayscale mode.	0	45	
Drawing control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Sets the cursor address.	2	45	Note 1
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Instructs to read the cursor address.	2	46	Note 1
Memory control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Instructs to write to display memory.	—	47	Note 1
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Instructs to read display memory data.	—	47	

Note 1: As a rule, each command is executed every time a parameter for the command is input to the S1D13700, and completed before the next parameter (P) or command (C) is input. Therefore, the MPU can stop sending parameters in the middle and send the next command. In this case, the parameters that have already been sent are effective and other parameters not input to the S1D13700 retain their original values. However, two-byte parameters are handled as described below.

Note 1:

1. CSRW and CSRR commands: The parameter is executed one byte at a time. Therefore, the MPU can only alter or check the low-order byte.
2. Commands other than CSRW and CSRR: The parameter is not executed until its second byte is input.

   SYSTEM SET
   SCROLL
   CGRAM ADR
3. Two-byte parameters consist of two bytes of data (as in the case of APL and APH).
4. Because the value of each register after power-on is indeterminate, make sure all command parameters are set.

3.2 Command Register Map (when Directly Interfaced)

When direct mode is selected for the system interface, directly access the registers to set up the display.

Address	Hard Reset	Register name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0 x 8000	0 x 10	R_P1_ SystemSet	0	0	IV	1	WS	M2	M1	M0
0 x 8001	0 x 00	R_P2_ SystemSet	WF	0	0	0	FX			
0 x 8002	0 x 00	R_P3_ SystemSet	0	0	0	0	FY			
0 x 8003	0 x 00	R_P4_ SystemSet	CR							
0 x 8004	0 x 00	R_P5_ SystemSet	TCR							
0 x 8005	0 x 00	R_P6_ SystemSet	LF							
0 x 8006	0 x 00	R_P7_ SystemSet	APL							
0 x 8007	0 x 00	R_P8_ SystemSet	APH							
0 x 8008 *2	0 x 01	R_SleepIn	0	0	0	0	0	0	0	Sleep In
0 x 8009	0 x 00	r_DispOnOff	0	0	0	0	0	0	0	Disp On
0 x 800A	0 x 00	r_P1_ DispOnOff	FP5	FP4	FP3	FP2	FP1	FP0	FC1	FC0
0 x 800B	0 x 00	r_P1_Scroll	SAD1L A7	SAD1L A6	SAD1L A5	SAD1L A4	SAD1L A3	SAD1L A2	SAD1L A1	SAD1L A0
0 x 800C *1	0 x 00	r_P2_Scroll	SAD1H A15	SAD1H A14	SAD1H A13	SAD1H A12	SAD1H A11	SAD1H A10	SAD1H A9	SAD1H A8
0 x 800D	0 x 00	r_P3_Scroll	SL1L7	SL1L6	SL1L5	SL1L4	SL1L3	SL1L2	SL1L1	SL1L0
0 x 800E	0 x 00	r_P4_Scroll	SAD2L A7	SAD2L A6	SAD2L A5	SAD2L A4	SAD2L A3	SAD2L A2	SAD2L A1	SAD2L A0
0 x 800F *1	0 x 00	r_P5_Scroll	SAD2H A15	SAD2H A14	SAD2H A13	SAD2H A12	SAD2H A11	SAD2H A10	SAD2H A9	SAD2H A8
0 x 8010	0 x 00	r_P6_Scroll	SL2L7	SL2L6	SL2L5	SL2L4	SL2L3	SL2L2	SL2L1	SL2L0
0 x 8011	0 x 00	r_P7_Scroll	SAD3L A7	SAD3L A6	SAD3L A5	SAD3L A4	SAD3L A3	SAD3L A2	SAD3L A1	SAD3L A0
0 x 8012 *1	0 x 00	r_P8_Scroll	SAD3H A15	SAD3H A14	SAD3H A13	SAD3H A12	SAD3H A11	SAD3H A10	SAD3H A9	SAD3H A8
0 x 8013	0 x 00	r_P9_Scroll	SAD4L A7	SAD4L A6	SAD4L A5	SAD4L A4	SAD4L A3	SAD4L A2	SAD4L A1	SAD4L A0
0 x 8014 *1	0 x 00	r_P10_Scroll	SAD4H A15	SAD4H A14	SAD4H A13	SAD4H A12	SAD4H A11	SAD4H A10	SAD4H A9	SAD4H A8
0 x 8015	0 x 00	r_P1_ CsrForm	0	0	0	0	CRX3	CRX2	CRX1	CRX0
0 x 8016	0 x 00	r_P2_ CsrForm	CM	0	0	0	CRY3	CRY2	CRY1	CRY0
0 x 8017	0 x 00	r_P1_CsrDir	0	0	0	0	0	0	CD1	CD2
0 x 8018	0 x 00	r_P1_OvLay	0	0	0	OV	DM2	DM1	MX1	MX0

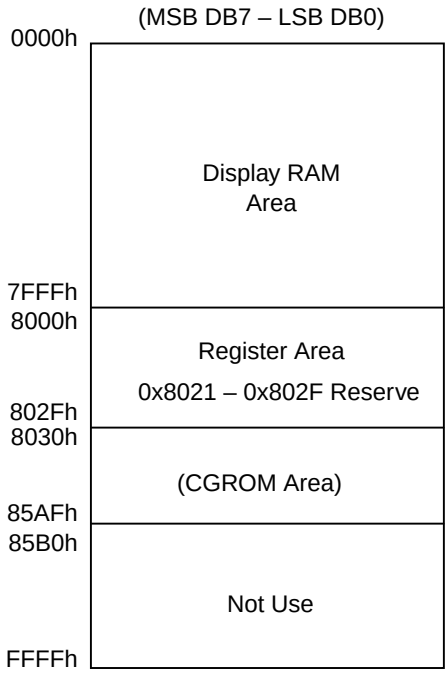
Address	Hard Reset	Register name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0 x 8019	0 x 00	r_P1_ CGRAMAdr	SAGL A7	SAGL A6	SAGL A5	SAGL A4	SAGL A3	SAGL A2	SAGL A1	SAGL A0
0 x 801A *1	0 x 00	r_P2_ CGRAMAdr	SAGH A15	SAGH A14	SAGH A13	SAGH A12	SAGH A11	SAGH A10	SAGH A9	SAGH A8
0 x 801B	0 x 00	r_P1_HdotScr	0	0	0	0	0	D2	D1	D0
0 x 801C *3	0 x 00	r_P1_CSRW	CSRL A7	CSRL A6	CSRL A5	CSRL A4	CSRL A3	CSRL A2	CSRL A1	CSRL A0
0 x 801D *3	0 x 00	r_P2_CSRW	CSRH A15	CSRH A14	CSRH A13	CSRH A12	CSRH A11	CSRH A10	CSRH A9	CSRH A8
0 x 801E *3	0 x 00	r_P1_CSRR	CSRL A7	CSRL A6	CSRL A5	CSRL A4	CSRL A3	CSRL A2	CSRL A1	CSRL A0
0 x 801F *3	0 x 00	r_P2_CSRR	CSRH A15	CSRH A14	CSRH A13	CSRH A12	CSRH A11	CSRH A10	CSRH A9	CSRH A8
0 x 8020	0 x 00	r_P1_ GrayScale	0	0	0	0	0	0	BPP1	BPP0

*1 To ensure that two bytes are set at the same time, the low-order byte is fixed when the high-order byte is written.

*2 SLEEPIN = 0: Clock enable
Using the internal oscillator circuit causes the oscillator to start oscillating. Using an externally sourced clock causes the clock to propagate to the internal circuits.
The internal timing circuit is released from reset status by writing to any register after setting SLEEPIN = 0. (Therefore, internal SRAM cannot be accessed until that time.)

*3 CSRW: Write only (00h when read), CSRR: read only (write invalid).
Other registers can be written to or read from (in units of bits).

The following shows the relationship between memory and register maps in the S1D13700.



S1D13700 Memory Mapping (AB15 – AB0)

* The S1D13700 ignores any attempt to access address space 8030h–FFFFh. This address space may be employed as a user area, but because there is no negate output available for the WAIT# pin of the S1D13700, inhibit access to this address space when not in use.

3.3 Command Description

3.3.1 Operation Control Commands

SYSTEM SET

This command and the parameters that follow specify initial reset of the device, set the window size, and the method of connecting with the LCD unit. This command determines the fundamental operation of the S1D13700. Therefore, if this command is incorrectly set, the functions of other commands may not work normally.

<Indirect mode>	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	<Direct mode> Address	Register name
C	0	1	0	0	0	0	0	0	–	–
P1	0	0	IV	1	WS	M2	M1	M0	0x8000	r_P1_SystemSet bit5 : IV bit3 : WS bit2 : M2 bit1 : M1 bit0 : M0
P2	WF	0	0	0	0	FX			0x8001	r_P2_SystemSet bit7 : WF bit2-0 : FX
P3	0	0	0	0	FY				0x8002	r_P3_SystemSet bit3-0 : FX
P4	C/R								0x8003	r_P4_SystemSet bit7-0 : CR
P5	TC/R								0x8004	r_P5_SystemSet bit7-0 : TCR
P6	L/F								0x8005	r_P6_SystemSet bit7-0 : LF
P7	APL								0x8006	r_P7_SystemSet bit7-0 : APL
P8	APH								0x8007	r_P8_SystemSet bit7-0 : APH

● C The command alone has the following initial reset functions:

- Resets the internal timing circuit.
- Turns display off.
- Deactivates sleep mode (internal operation stopped state) (thus starting the oscillator).

To deactivate sleep mode, make sure the command and one parameter (P1) are input.

In direct interface mode, clearing the SleepIn bit has the same effect.

[Parameter P1]

●M0 Specify the CG ROM to be used for display. Although internal CG ROM can generate 160 discrete character fonts (each consisting of 5 x 7 dots as shown in Section 4.4.1 “Character Fonts (Internal CG)” on page 81), internal CG RAM may be used when different character fonts or more characters (up to 256) are needed.

M0 0: Internal CG ROM (160 characters) + internal CG RAM (64 characters)

1: Internal CG RAM (256 characters)

Note: When the CG area is mapped in the display memory space, the memory area available to store display data is reduced by the amount of CG area mapped.

●M1 Selects the CG RAM definition area where the user can define any desired character pattern. The CG RAM code may be selected from the 64 discrete codes assigned in Section 4.4.2 “Character Codes” on page 82.

M1 0: Without bit D6 correction — The CG RAM1 and CG RAM2 areas are noncontiguous. Only CG RAM1 is handled as CG RAM, with CG RAM2 handled as CG ROM.

1: With bit D6 correction — The CG RAM1 and CG RAM2 areas are contiguous. Both CG RAM1 and RAM2 are handled as CG RAM.

●M2 Select the CG size in the Y direction for more economical use of internal CG RAM. CGs whose sizes in the Y direction are 17 dots or more cannot be handled with the character codes of the S1D13700. In such case, characters may be decomposed into bit images and displayed in graphic display mode of the S1D13700.

M2 0: 8 dots

1: 16 dots

The table below summarizes bank configurations by M1, M2, and M3.

Bank configurations

M2	M1	M0				
0	0	0	Internal ROM	160 characters (5 x 7 x 160)	10 – 1F 20 – 2F 30 – 3F 40 – 4F 50 – 5F 60 – 6F 70 – 7F A0 – AF B0 – BF C0 – CF D0 – DF	Internal ROM used Without correction Y size = 8
			External RAM	64 characters (8 x 6 x 64)	SAG+ { [80 – 8F], Row [2 : 0]} [90 – 9F] [E0 – EF] [F0 – FF]	
0	1	0	Internal ROM	160 characters (5 x 7 x 160)	Same as shown above.	Internal ROM used With correction Y size = 8
			External RAM	64 characters (6 x 8 x 64)	SAG+ { [A0 – AF], Row [2 : 0]} [B0 – BF] [C0 – CF] [D0 – DF]	

M2	M1	M0				
1	0	0	Internal ROM	160 characters (5 x 7 x 160)	Same as shown above.	Internal ROM used Without correction Y size = 16
			External RAM	64 characters (6 x 8 x 64)	SAG+ { [80 – 8F], Row [3 : 0]} [90 – 9F] [E0 – EF] [F0 – FF]	
1	1	0	Internal ROM	160 characters (5 x 7 x 160)	Same as shown above.	Internal ROM used With correction Y size = 16
			External RAM	64 characters (6 x 16 x 64)	SAG+ { [A0 – AF], Row [3 : 0]} [B0 – BF] [C0 – CF] [D0 – DF]	
0	0	1	External RAM	256 characters (8 x 8 x 256)	F000 – F7FF	External RAM Without correction Y size = 8
0	1	1	External RAM	256 characters (8 x 8 x 256)	F000 – F7FF	External RAM With correction Y size = 8
1	0	1	External RAM	256 characters (8 x 16 x 256)	F000 – FFFF	External RAM Without correction Y size = 16
1	1	1	External RAM	256 characters (8 x 16 x 256)	F000 – FFFF	External RAM With correction Y size = 16

M1 = 0			M1 = 1 (code [6] converted)		
00 – 0F	00000000 – 00001111	Blank	40 – 4F	00000000 – 00001111	ROM
10 – 1F	00010000 – 00011111	ROM	50 – 5F	01010000 – 01011111	ROM
20 – 2F	00100000 – 00101111	ROM	60 – 6F	01100000 – 01101111	ROM
30 – 3F	00110000 – 00111111	ROM	70 – 7F	01110000 – 01111111	ROM
40 – 4F	01000000 – 01001111	ROM	00 – 0F	00000000 – 00001111	Blank
50 – 5F	01010000 – 01011111	ROM	10 – 1F	00010000 – 00011111	ROM
60 – 6F	01100000 – 01101111	ROM	20 – 2F	00100000 – 00101111	ROM
70 – 7F	01110000 – 01111111	ROM	30 – 3F	00110000 – 00111111	ROM
80 – 8F	10000000 – 10001111	RAM	C0 – CF	11000000 – 11001111	ROM
90 – 9F	10010000 – 10011111	RAM	D0 – DF	11010000 – 11011111	ROM
A0 – AF	10100000 – 10101111	ROM	E0 – EF	11100000 – 11101111	RAM
B0 – BF	10110000 – 10111111	ROM	F0 – FF	11110000 – 11111111	RAM
C0 – CF	11000000 – 11001111	ROM	80 – 8F	10000000 – 10001111	RAM
D0 – DF	11010000 – 11011111	ROM	90 – 9F	10010000 – 10011111	RAM
E0 – EF	11100000 – 11101111	RAM	A0 – AF	10100000 – 10101111	ROM
F0 – FF	11110000 – 11111111	RAM	B0 – BF	10110000 – 10111111	ROM

*M1: The 6th bit of the character code is automatically converted by hardware. The memory area accessed changes.

●W/S Selects the LCD unit drive method.

W/S 0: Single-screen drive method

1: Dual-screen drive method

Table 3-1 W/S Related Registers

Parameter	W/S = 0		W/S = 1	
	IV = 1	IV = 0	IV = 1	IV = 0
C/R	C/R	C/R	C/R	C/R
TC/R	TC/R	TC/R	TC/R	TC/R
L/F	L/F	L/F	L/F	L/F
SL1	00H – L/F	00H – L/F + 1	(L/F)/2	(L/F)/2
SL2	00H – L/F	00H – L/F + 1	(L/F)/2	(L/F)/2
SAD1	First screen block	First screen block	First screen block	First screen block
SAD2	Second screen block	Second screen block	Second screen block	Second screen block
SAD3	Third screen block	Third screen block	Third screen block	Third screen block
SAD4	Invalid	Invalid	Fourth screen block	Fourth screen block
Cursor	Successively movable on all screens		Upper/lower screen configuration: Successively movable on all screens	

Note: 1. For details on how to set C/R and TC/R when using the HDOT SCR command, see Section 4.1.6 “Determining Various Parameters” on page 64.

2. The SL value for IV = 0 is the SL value for IV = 1 plus 1.

●IV Corrects the screen origin during inverse display. Normally set IV = 1.
The most effective way to display characters in inverse video is to use a unique function of the S1D13700 that allows the text screen and graphics back-layered screen to be exclusive OR’d. However, because the character origin is at the upper-left corner of the screen when characters are mapped on the screen by the S1D13700, the uppermost line and leftmost column on the display screen do not have dots to draw the outline of characters, thus making the displayed characters illegible. Therefore, the S1D13700 uses the IV specification and horizontal direction dot scroll function (HDOTSCR command) to shift the origin of the text screen for correction with respect to the graphics back-layered screen, allowing characters to be displayed in inverse video anywhere on the screen. For details, see Section 4.1.7 “Scrolling” on page 65.

IV 0: Uppermost line of screen corrected
1: Uppermost line of screen not corrected

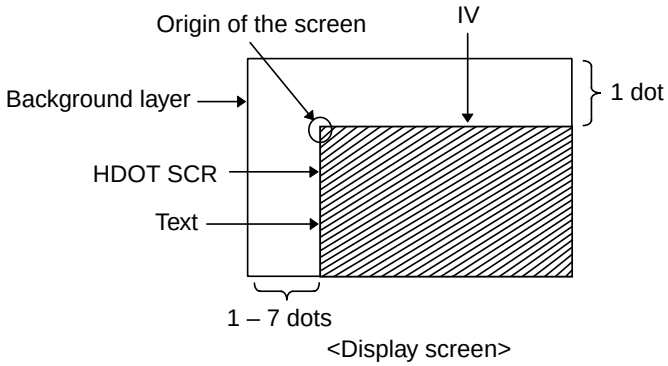


Figure 3-1 Combination of IV and HDOT SCR

Note: If the leftmost column must also be corrected, shift dots in the horizontal direction.

[Parameter P2]

●FX Defines the size of the character field in the X direction (i.e., size of one character including a space).

HEX	BIN					Number of dots [FX]
	D4	D3	D2	D1	D0	
00	0	0	0	0	0	1
01	0	0	0	0	1	2
•	•	•	•	•	•	•
•	•	•	•	•	•	•
07	0	0	1	1	1	8

Structure of the character field

1. Because the S1D13700 processes the display data in 8-bit units, if the character font exceeds 8 bits, the text screen must configure one character with two or more display memory addresses as normally practiced. In this case, odd-numbered bits less than a unit of 8 bits are not displayed as shown below. Odd-numbered bits less than a unit of 8 bits are also not displayed on the back-layered screen as shown below.
2. In graphic display mode, the character field must normally be 8 bits long. For other character fields, odd-numbered bits less than a unit of 8 bits are not displayed.

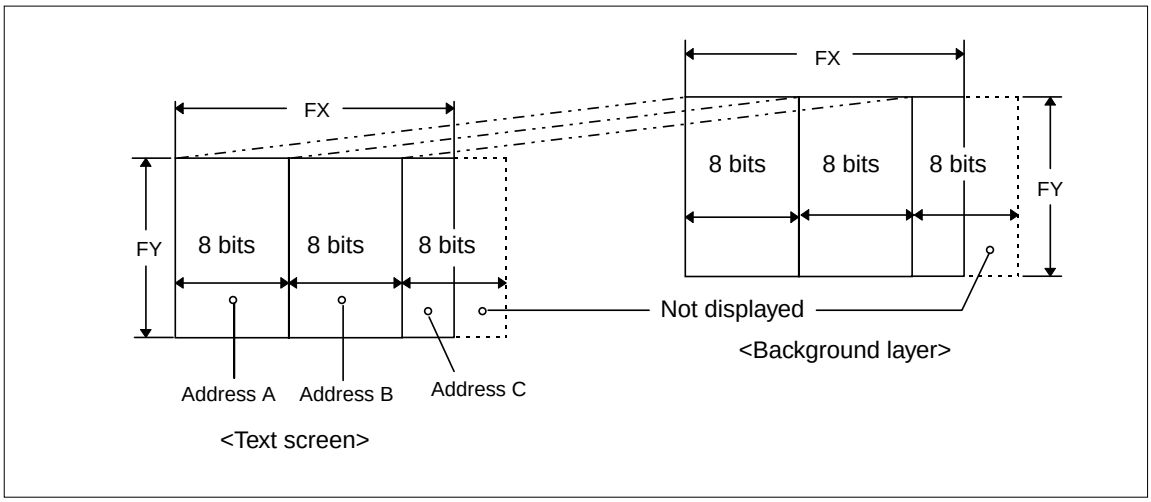


Figure 3-2 Typical relationship between FX/FY and display addresses

In grayscale mode, FX must be fixed to ‘00111’ (8 dots).

●WF Specifies the AC drive method of the liquid crystal.

WF 0: Line inversion drive method
1: Two-frame AC drive method (method B)

The two-frame AC drive method is an AC drive method in which the half period of the WF signal constitutes a one-frame interval. Normally, set WF = 1.

The line inversion drive method is a modified AC drive method in which the WF signal has its waveform inverted every 16 Y lines.

Note: Although the LCD may look better when WF is set to 0, stripes in the X direction will appear when the LCD drive voltage is high or viewing angle large.

[Parameter P3]

●FY Defines the size of the character field in the Y direction.

HEX	BIN				Number of dots [FX]
	D3	D2	D1	D0	
00	0	0	0	0	1
01	0	0	0	1	2
•	•	•	•	•	•
•	•	•	•	•	•
07	0	1	1	1	8
•	•	•	•	•	•
0E	1	1	1	0	15
0F	1	1	1	1	16

[Parameter P4]

●C/R Defines the display interval in the X direction by indicating the number of display characters counted in address units, as described in the section on parameter FX. When [FX] = 10 dots, for example, two memory addresses are counted per character. For details on how to calculate the [C/R] value, see Section 4.1.6 “Determining Various Parameters” on page 64. The value set for this parameter cannot be greater than the calculated [C/R] value, but can be equal to or less than the calculated [C/R] value. In that case, excess display sections are left blank.

HEX	BIN								Characters per line [C/R]
	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
4F	0	1	0	0	1	1	1	1	80
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
EE	1	1	1	0	1	1	1	0	239
EF	1	1	1	0	1	1	1	1	240

Note: 1. Make sure the number of dots in excess display sections is within 64.

2. For grayscale to be set to 2 Bpp or 4 Bpp, the set value of CR must be increased.
CR (bytes) = [(Panel Width) /8pixel character]*Bpp

[Parameter P5]

●TC/R The condition [TC/R] ≥ [C/R] + 4 must always be met.
To minimize the amount of current consumed by the S1D13700 and LCD unit for a given display capacity, the S1D13700's oscillation frequency (fosc) must be adjusted. Moreover, because the one-frame time ($1/f_{FR}$) must be made constant to prevent flicker, define [TC/R] according to the equation to calculate [TC/R] as described in Chapter 4 and adjust the S1D13700's divide-by-n ratio.

HEX	BIN								Characters per line [TC/R]
	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
52	0	1	0	1	0	0	1	0	83
•		•	•	•	•	•	•	••	•
•	•	•	•	•	•	•	•	•	•
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

[Parameter P6]

●L/F Defines the display interval in the Y direction by indicating the number of display lines per screen.

HEX	BIN								Number of lines per screen
	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
7F	0	1	1	1	1	1	1	1	128
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

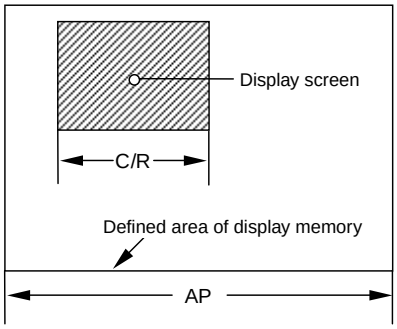
Note: When W/S = 1, [L/F] must be defined as an even number because dual-screen display is assumed.

[Parameters P7, P8]

●AP Defines the number of memory addresses in the X direction of a virtual screen.

	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
APL	AP7	AP6	AP5	AP4	AP3	AP2	AP1	AP0
APH	AP15	AP14	AP13	AP12	AP11	AP10	AP9	AP8

HEX		Number of memory addresses per line [AP]
APH	APL	
0 0	0 0	0
0 0	0 1	1
• •	• •	•
• •	• •	•
0 0	5 0	80
• •	• •	•
• •	• •	•
F F	F E	2^{16}-2
F F	F F	2^{16}-1



SLEEP IN

●C When this command is input, the S1D13700 blanks the display for at least a one-frame period, then stops all internal operations including clock oscillation before entering sleep mode. At this time, the LCD unit sends OFF data to the X driver while simultaneously sending the YDIS signal to the Y driver to turn the bias voltage off. Therefore, in no case will unexpected display remain on the screen when the liquid crystal is powered off by the YDIS signal.

In sleep mode, the S1D13700 registers retain the original state before entering sleep mode. Moreover, the display memory control pins are fixed high or low to maintain the integrity of data stored in display memory.

To restore the S1D13700 from sleep mode, write the command and one parameter (P1) of the SYSTEM SET to the S1D13700 once to immediately wake up the S1D13700. In direct interface mode, the S1D13700 can be restored from sleep mode by clearing the SleepIn bit. However, display memory cannot be accessed immediately after exiting sleep mode. The display RAM space (0000h–7FFFh) can be accessed by first accessing any other register once. To restore display, execute the DISP ON command immediately after exiting sleep mode.

Regardless of whether the S1D13700 is directly or indirectly interfaced, the entire screen must be set to the ON state before entering sleep mode. When in indirect interface mode, issue the DISP ON command. When in direct interface mode, set the DispOn bit to 1 before entering sleep mode.

<Indirect mode>

	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
C	0	1	0	1	0	0	1	1

<Direct mode>

Address	Register name
0x8008	r_SleepIn bit0 : SleepIn

Note: 1. The YDIS signal goes low at a time equivalent to one to two frames after the sleep command is written. When the YDIS signal goes low, all Y driver outputs are forcibly brought to an inter-

mediate level (unselected), causing display to turn off. Therefore, for the LCD unit to be powered down, the liquid crystal drive power supply (with relatively large steady-state current) must be turned off at the same time display is turned off by using the YDIS signal.

2. If the drive power supply of the liquid crystal remains on in sleep mode, a DC component may be applied to the LCD panel because all internal operations of the S1D13700 have been stopped in that mode. When priority is placed on reliability, however, the liquid crystal drive power supply must be turned off before writing the sleep command to prevent DC components from being applied to the LCD panel.
3. Although the bus is placed in the high-impedance state during sleep mode, some voltage may be supplied to the bus line for a bus with pull-up/pull-down resistors.

3.3.2 Display Control Commands

DISP ON/OFF

This command turns display of the entire screen on or off.

The parameters that follow this command turn the cursor and each layered screen on or off individually, and select the cursor blink rate and screen flashing rate. Setting a blink rate and flashing rate makes area flashing possible (i.e., flashing one entire line) instead of flashing just one character by means of cursor display.

<Indirect mode> <Direct mode>

	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	Address	Register name
C	0	1	0	1	1	0	0	0	0x8009	r_DispOnOff bit0 : DispOn
P1	FP5	FP4	FP3	FP2	FP1	FP0	FC1	FC0	0x800A	r_P1_DispOnOff bit7-2 : FP5-FP0 bit1-0 : FC1-FC0

●C

D 0: Disables entire screen display.
1: Restores entire screen display.

Note: Parameter D (to disable entire screen display) has priority over parameter FP.

Note: When the entire screen display is disabled (D=0), power to the panel is off (YDIS = 0 level) and the panel timing signal is off.

[Parameter P1]

●FC Selects turning the cursor on or off and defines a blink rate.

FC1, FC0		Cursor display	
0	0	OFF (blank)	
0	1	ON	Blinking off
1	0		Blink at fFR/32 Hz (approx. 2 Hz)
1	1		Blink at fFR/64 Hz (approx. 1 Hz)

Cusor blink on/off ratio
ON : OFF = 7 : 3

Note: As the MWRITE command always enables the cursor, the cursor position can be checked, even when performing consecutive writes to display memory while the cursor is flashing.

Note: To display the cursor in direct interface mode, read or write data to the frame buffer. This action causes the cursor to move automatically to that position.

●FP

FP1, FP0 FP3, FP2 FP5, FP4		First screen block (SAD1) Second screen block (SAD2, SAD4) Note Third screen block (SAD3)	
0	0	Screen display off (blank)	
0	1	Display on	Screen flashing off
1	0		Flash at fFR/32 Hz (approx. 2 Hz)
1	1		Flash at fFR/4 Hz (approx. 15 Hz)

Screen flashing on/off ratio
ON:OFF = 7:3

Note: Although SAD4 is assumed when W/S = 1, the screens specified by SAD2 and SAD4 cannot be made to flash independently of each other due to simultaneous control by parameters FP2 and FP3.

SCROLL

●C Defines the scroll start address (SAD) and number of lines per block to be scrolled (SL). Parameters P1 through P10 can be omitted when not required. However, the parameters must be set sequentially as shown below.

<Indirect mode>										<Direct mode>	
	MSB							LSB		Address	Register name
	D7	D6	D5	D4	D3	D2	D1	D0			
C	0	1	0	0	0	1	0	0		–	–
P1	A7	A6	A5	A4	A3	A2	A1	A0	(SAD1L)	0x800B	r_P1_Scroll bit7-0 : A7-A0
P2	A15	A14	A13	A12	A11	A10	A9	A8	(SAD1H)	0x800C	r_P2_Scroll bit7-0 : A15-A8
P3	L7	L6	L5	L4	L3	L2	L1	L0	(SL1)	0x800D	r_P3_Scroll bit7-0 : L7-L0
P4	A7	A6	A5	A4	A3	A2	A1	A0	(SAD2L)	0x800E	r_P4_Scroll bit7-0 : A7-A0
P5	A15	A14	A13	A12	A11	A10	A9	A8	(SAD2H)	0x800F	r_P5_Scroll bit7-0 : A15-A8
P6	L7	L6	L5	L4	L3	L2	L1	L0	(SL2)	0x8010	r_P6_Scroll bit7-0 : L7-L0
P7	A7	A6	A5	A4	A3	A2	A1	A0	(SAD3L)	0x8011	r_P7_Scroll bit7-0 : A7-A0
P8	A15	A14	A13	A12	A11	A10	A9	A8	(SAD3H)	0x8012	r_P8_Scroll bit7-0 : A15-A8
P9	A7	A6	A5	A4	A3	A2	A1	A0	(SAD4L) Note	0x8013	r_P9_Scroll bit7-0 : A7-A0
P10	A15	A14	A13	A12	A11	A10	A9	A8	(SAD4H) Note	0x8014	r_P10_Scroll bit7-0 : A15-A8

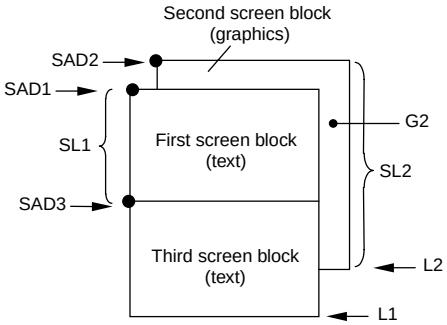
Note: Parameters P9 and P10 must be set only when the dual-screen drive method (W/S = 1) and two-layered configuration are selected. SAD4 defines the fourth screen block display start address.

HEX	BIN								Number of lines [SL]
	L7	L6	L5	L4	L3	L2	L1	L0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
7F	0	1	1	1	1	1	1	1	128
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

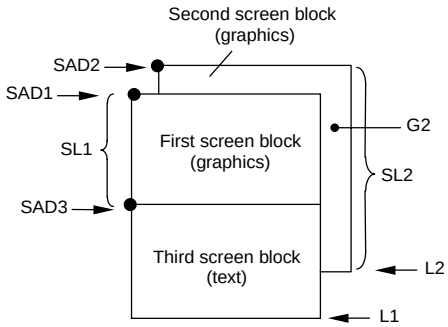
The next page shows the relationship between display modes and SAD and SL.

[Display modes]

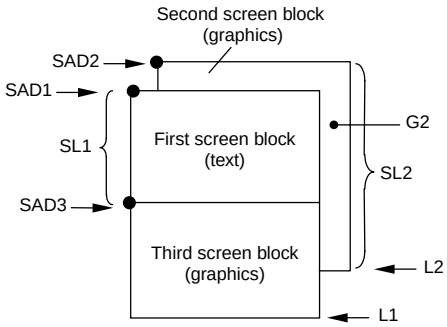
W/S OV DM2, 1		First layer	Second layer
	First screen block Second screen block	SAD1 SL1	SAD2 SL2
0 0 00	Third screen block (split)	SAD3 Note 1	
	When not using split screens, set both SL1 and SL2 to L/F + 1. <Example of screen configuration> Note 3		



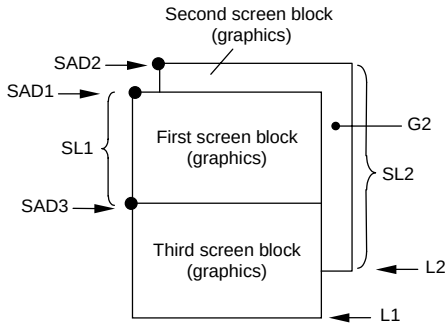
W/S OV DM2, 1		First layer	Second layer
	First screen block Second screen block	SAD1 SL1	SAD2 SL2
0 0 01	Third screen block (split)	SAD3 Note 1	
	When not using split screens, set both SL1 and SL2 to L/F + 1. <Example of screen configuration> Note 3		



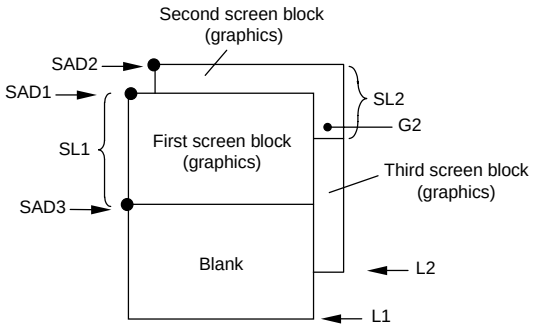
W/S OV DM2, 1		First layer	Second layer
	First screen block Second screen block	SAD1 SL1	SAD2 SL2
0 0 10	Third screen block (split)	SAD3 Note 1	
	When not using split screens, set both SL1 and SL2 to L/F + 1. <Example of screen configuration> Note 3		



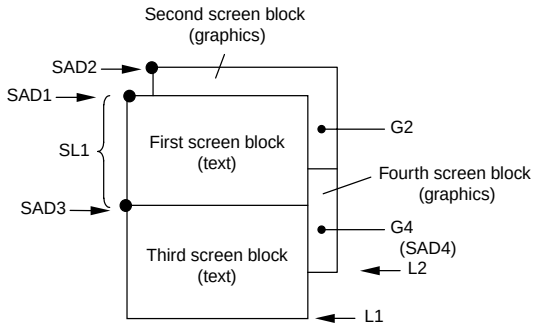
W/S OV DM2, 1		First layer	Second layer
	First screen block Second screen block	SAD1 SL1	SAD2 SL2
0 0 11	Third screen block (split)	SAD3 Note 1	
	SL1 ≤ SL2 <Example of screen configuration> Note 3		



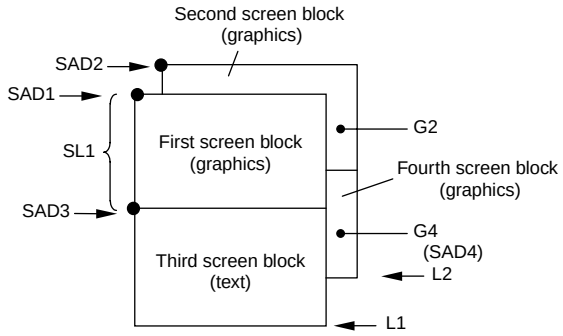
W/S OV DM2, 1		First layer	Second layer
	First screen block Second screen block	SAD1 SL1	SAD2 SL2
0 0 11	Third screen block (split)	SAD3 Note 1	
	SL1 > SL2 <Example of screen configuration> Note 3		



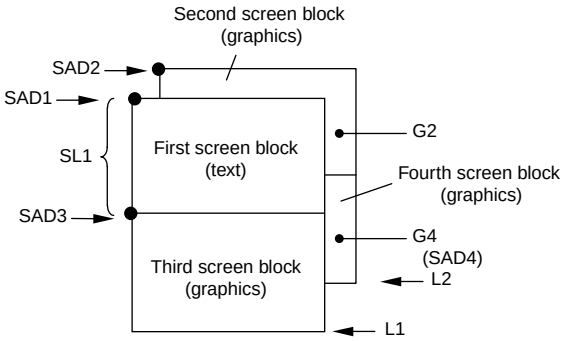
W/S OV DM2, 1		First layer	Second layer
	Upper screen	SAD1 SL1	SAD2 SL2
1 0 00	Lower screen	SAD3 Note 2	SAD4 Note 2
	<Example of screen configuration> Note 3		



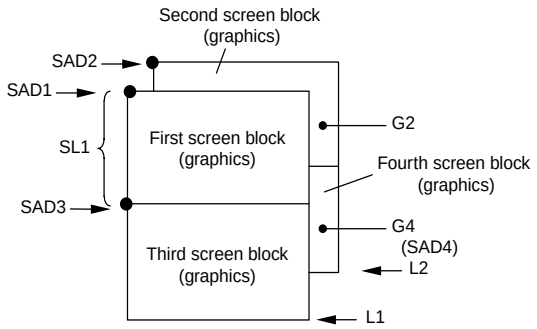
W/S OV DM2, 1		First layer	Second layer
	Upper screen	SAD1 SL1	SAD2 SL2
1 0 01	Lower screen	SAD3 Note 2	SAD4 Note 2
	<Example of screen configuration> Note 3		



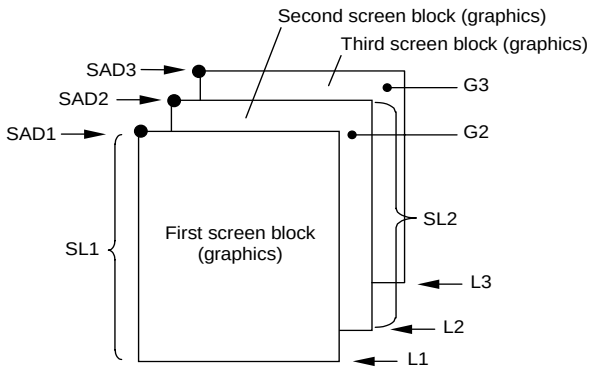
W/S OV DM2, 1		First layer	Second layer
	Upper screen	SAD1 SL1	SAD2 SL2
1 0 10	Lower screen	SAD3 Note 2	SAD4 Note 2
	<Example of screen configuration> Note 3		



W/S OV DM2, 1		First layer	Second layer
	Upper screen	SAD1 SL1	SAD2 SL2
1 0 11	Lower screen	SAD3 Note 2	SAD4 Note 2
	<Example of screen configuration> Note 3		



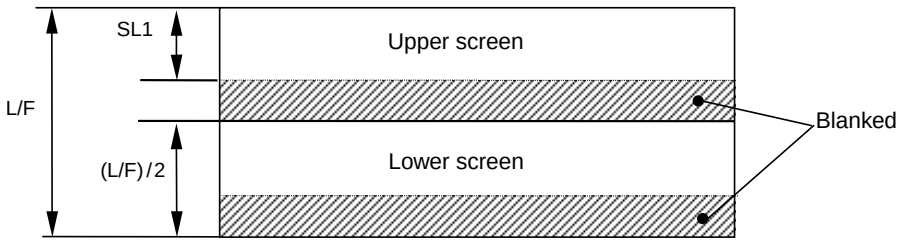
W/S OV DM2, 1		First layer	Second layer	Third layer
	Three-layer composition	SAD1 SL1	SAD2 SL2	SAD3
0 1 11	<Example of screen configuration> Note 3			



Note 1: SAD3 is added to SL1 or SL2 (whichever has the fewest lines).

Note 2: Parameters corresponding to SL3 and SL4 are determined by L/F, and thus need not be set.

Note 3: When W/S = 1, the differences between SL1 and (L/F) / 2 and between SL2 and (L/F) / 2 are blanked.



No.	WS	OV	DM2	DM1	Panel	Layer	(block3,block1)
1	0	0	0	0	Single	2	(char, char)
2	0	0	0	1	Single	2	(char, graph)
3	0	0	1	0	Single	2	(graph, char)
4	0	0	1	1	Single	2	(graph, graph)
5	0	1	0	0	Single	2	↑No.1
6	0	1	0	1	Single	2	↑No.2
7	0	1	1	0	Single	2	↑No.3
8	0	1	1	1	Single	3	(graph, graph,graph)
9	1	0	0	0	Dual	2	(char, char)
10	1	0	0	1	Dual	2	(char, graph)
11	1	0	1	0	Dual	2	(graph, char)
12	1	0	1	1	Dual	2	(graph, graph)
13	1	1	0	0	Dual	2	↑No.9
14	1	1	0	1	Dual	2	↑No.10
15	1	1	1	0	Dual	2	↑No.11
16	1	1	1	1	Dual	2	↑No.12

CSRFORM

Defines the size and shape of the cursor displayed.

Although the cursor is normally used in text display mode, the S1D13700 can also display the cursor in graphic display mode to display kanji and other special characters.

<Indirect mode> <Direct mode>

	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	Address	Register name
C	0	1	0	1	1	1	0	1	–	–
P1	0	0	0	0	X3	X2	X1	X0	0x8015	r_P1_CsrForm bit3-0 : CRX3-CRX0
P2	CM	0	0	0	Y3	Y2	Y1	Y0	0x8016	r_P2_CsrForm bit7 : CM bit3-0 : CRX3-CRX0

[Parameter P1]

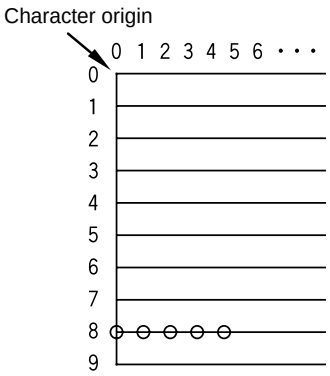
●CRX Defines the size of the cursor in the X direction by the number of dots counted from the character origin. Always make sure that CRX ≤ FX.

HEX	BIN				Number of dots [CRX]
	X3	X2	X1	X0	
0	0	0	0	0	1
1	0	0	0	1	2
•	•	•	•	•	•
4	0	1	0	0	5
•	•	•	•	•	•
E	1	1	1	0	15
F	1	1	1	1	16

[Parameter P2]

●CRY Defines the display line position of an underscored cursor in a character field by the number of dots counted from the character origin, or the size of a block cursor in the Y direction by the number of dots counted from the character origin.

HEX	BIN				Number of dots [CRX]
	Y3	Y2	Y1	Y0	
0	0	0	0	0	Illegal
1	0	0	0	1	2
•	•	•	•	•	•
8	1	0	0	0	9
•	•	•	•	•	•
E	1	1	1	0	15
F	1	1	1	1	16



[CRX] = 5 dots
[CRY] = 9 dots
CM = 0

●CM Defines the cursor shape.

CM 0: Underscore cursor
1: Block cursor

The S1D13700 allows CM to be set to either 0 or 1 on the graphic display screen. If CRY < FY when CM is set to 1 on the text display screen, the set value of FY has priority.

CSRDIR

●C Specifies the direction in which the cursor address counter is automatically shifted. When horizontal screen movement is specified, the cursor address is shifted –1 or +1 by the S1D13700 internal arithmetic/logic circuit. When vertical screen movement is specified, the cursor address is made to jump as many as the number of memory addresses defined by the address pitch (AP). Therefore, when accessing display memory successively in a given direction, it is only necessary to set the start address first. Then the cursor address need not be set by the MPU from the next data on.

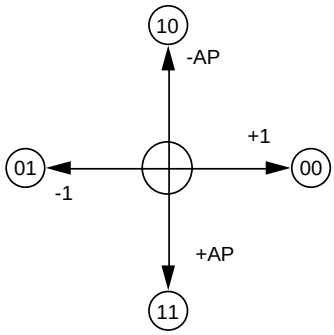
<Indirect mode>

	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
C	0	1	0	0	1	1	CD1	CD2

<Direct mode>

Address	Register name
0x8017	r_P1_CsrDir bit1-0 : CD1-CD2

HEX	BIN CD1	BIN CD2	Shift direction
4C	0	0	Right
4D	0	1	Left
4E	1	0	Up
4F	1	1	Down



Note: Because the cursor moves in address units even if FX ≥ 9, the cursor address must be preset for movement in character units. (See Section 4.1.4 “Cursor” on page 61.

OVLAY

●C Specifies the method of composing layered screens and text or graphic display mode for each screen.

<Indirect mode>

	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
C	0	1	0	1	1	0	1	1
P1	0	0	0	OV	DM2	DM1	MX1	MX0

<Direct mode>

Address	Register name
–	–
0x8018	r_P1_OvLay bit4 : OV bit3-2 : DM2-DM1 bit4 : MX1-MX0

[Parameter P1]

●MX0 Specifies the method of composing layered screens.

●MX1 Selects the method of screen composition from OR, AND, Exclusive OR, and Prioritized OR as listed in the table below. Because screens are composed in units of layers, different composition methods cannot be used for individual screen blocks, even if a layer is divided into two screen blocks.

Prioritized OR is the same as simple OR unless the flashing of individual screens is used in combination with it.

MX1	MX0		Composition method	Application example
0	0	$L1 \cup L2 \cup L3$	Simple overlay (OR)	Underlining, rules, mixed text, and graphic display
0	1	$(L1 \oplus L2) \cup L3$	Black & white reverse overlay (EOR)	Characters in inverse video, area flashing, underlining
1	0	$(L1 \cap L2) \cup L3$	Selective overlay (AND)	Simple animation, three-dimensional appearance
1	1	$L1 > L2 > L3$	Prioritized overlay (As in Figure 3-4)	

Note: L1: First layer (text or graphics)
L2: Second layer (graphics only)
L3: Third layer (graphics only)

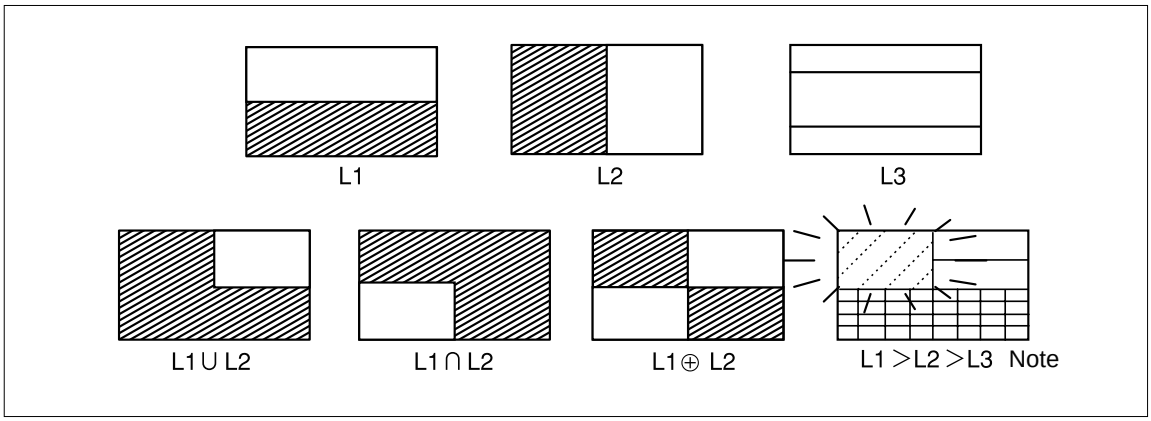


Figure 3-3 Example of screen compositions

Note: L1: Not flashing
L2: Flashing at 17 Hz (as specified by DISP ON/OFF command)
L3: Flashing at 2 Hz

The table below shows the relationship between L and FP when MX = 11b.

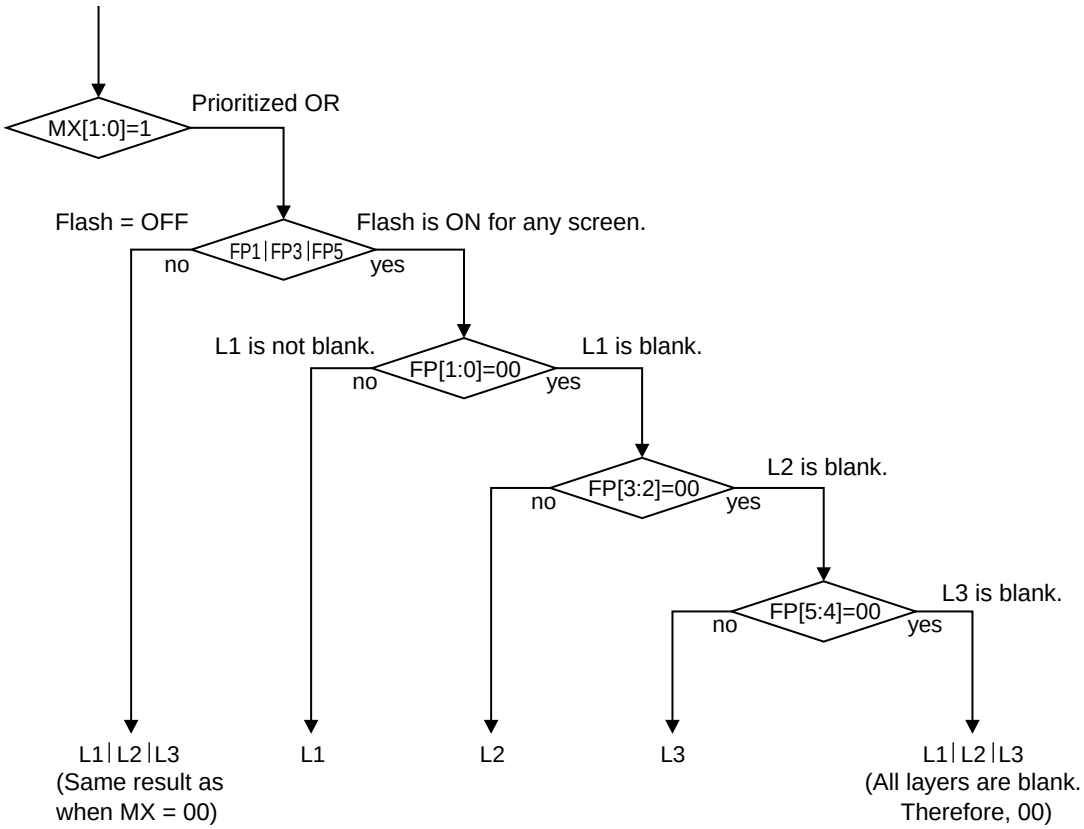


Figure 3-4 Prioritized overlay

Layered	MX[1:0]	FP[5:0]	Flash	Blank-off			
3	11	000000	x	–	–	–	L1 | L2 | L3
3		000001	x	–	–	L1	L1 | L2 | L3
3		000010	O	–	–	L1	L1
3		000011	O	–	–	L1	L1
3		000100	x	–	L2	–	L1 | L2 | L3
3		000101	x	–	L2	L1	L1 | L2 | L3
3		000110	O	–	L2	L1	L1
3		000111	O	–	L2	L1	L1
3		001000	O	–	L2	–	L2
3		001001	O	–	L2	L1	L1
3		001010	O	–	L2	L1	L1
3		001011	O	–	L2	L1	L1
3		001100	O	–	L2	–	L2
3		001101	O	–	L2	L1	L1
3		001110	O	–	L2	L1	L1
3		001111	O	–	L2	L1	L1
3		010000	x	L3	–	–	L1 | L2 | L3
3		010001	x	L3	–	L1	L1 | L2 | L3
3		010010	O	L3	–	L1	L1

Layered	MX[1:0]	FP[5:0]	Flash	Blank-off			
2	11	000000	x	–	–	–	L1 | L2
2		000001	x	–	–	L1	L1 | L2
2		000010	O	–	–	L1	L1
2		000011	O	–	–	L1	L1
2		000100	x	–	L2	–	L1 | L2
2		000101	x	–	L2	L1	L1 | L2
2		000110	O	–	L2	L1	L1
2		000111	O	–	L2	L1	L1
2		001000	O	–	L2	–	L2
2		001001	O	–	L2	L1	L1
2		001010	O	–	L2	L1	L1
2		001011	O	–	L2	L1	L1
2		001100	O	–	L2	–	L2
2		001101	O	–	L2	L1	L1
2		001110	O	–	L2	L1	L1
2		001111	O	–	L2	L1	L1
2		010000	x	–	–	–	L1 | L2
2		010001	x	–	–	L1	L1 | L2
2		010010	O	–	–	L1	L1

Layered	MX[1:0]	FP[5:0]	Flash	Blank-off			
3		010011	O	L3	–	L1	L1
3		010100	x	L3	L2	–	L1 | L2 | L3
3		010101	x	L3	L2	L1	L1 | L2 | L3
3		010110	O	L3	L2	L1	L1
3		010111	O	L3	L2	L1	L1
3		011000	O	L3	L2	–	L2
3		011001	O	L3	L2	L1	L1
3		011010	O	L3	L2	L1	L1
3		011011	O	L3	L2	L1	L1
3		011100	O	L3	L2	–	L2
3		011101	O	L3	L2	L1	L1
3		011110	O	L3	L2	L1	L1
3		011111	O	L3	L2	L1	L1
3		100000	O	L3	–	–	L3
3		100001	O	L3	–	L1	L1
3		100010	O	L3	–	L1	L1
3		100011	O	L3	–	L1	L1
3		100100	O	L3	L2	–	L2
3		100101	O	L3	L2	L1	L1
3		100110	O	L3	L2	L1	L1
3		100111	O	L3	L2	L1	L1
3		101000	O	L3	L2	–	L2
3		101001	O	L3	L2	L1	L1
3		101010	O	L3	L2	L1	L1
3		101011	O	L3	L2	L1	L1
3		101100	O	L3	L2	–	L2
3		101101	O	L3	L2	L1	L1
3		101110	O	L3	L2	L1	L1
3		101111	O	L3	L2	L1	L1
3		110000	O	L3	–	–	L3
3		110001	O	L3	–	L1	L1
3		110010	O	L3	–	L1	L1
3		110011	O	L3	–	L1	L1
3		110100	O	L3	L2	–	L2
3		110101	O	L3	L2	L1	L1
3		110110	O	L3	L2	L1	L1
3		110111	O	L3	L2	L1	L1
3		111000	O	L3	L2	–	L2
3		111001	O	L3	L2	L1	L1
3		111010	O	L3	L2	L1	L1
3		111011	O	L3	L2	L1	L1
3		111100	O	L3	L2	–	L2
3		111101	O	L3	L2	L1	L1
3		111110	O	L3	L2	L1	L1
3		111111	O	L3	L2	L1	L1

Layered	MX[1:0]	FP[5:0]	Flash	Blank-off			
2		010011	O	–	–	L1	L1
2		010100	x	–	L2	–	L1 | L2
2		010101	x	–	L2	L1	L1 | L2
2		010110	O	–	L2	L1	L1
2		010111	O	–	L2	L1	L1
2		011000	O	–	L2	–	L2
2		011001	O	–	L2	L1	L1
2		011010	O	–	L2	L1	L1
2		011011	O	–	L2	L1	L1
2		011100	O	–	L2	–	L2
2		011101	O	–	L2	L1	L1
2		011110	O	–	L2	L1	L1
2		011111	O	–	L2	L1	L1
2		100000	O	–	–	–	00
2		100001	O	–	–	L1	L1
2		100010	O	–	–	L1	L1
2		100011	O	–	–	L1	L1
2		100100	O	–	L2	–	L2
2		100101	O	–	L2	L1	L1
2		100110	O	–	L2	L1	L1
2		100111	O	–	L2	L1	L1
2		101000	O	–	L2	–	L2
2		101001	O	–	L2	L1	L1
2		101010	O	–	L2	L1	L1
2		101011	O	–	L2	L1	L1
2		101100	O	–	L2	–	L2
2		101101	O	–	L2	L1	L1
2		101110	O	–	L2	L1	L1
2		101111	O	–	L2	L1	L1
2		110000	O	–	–	–	00
2		110001	O	–	–	L1	L1
2		110010	O	–	–	L1	L1
2		110011	O	–	–	L1	L1
2		110100	O	–	L2	–	L2
2		110101	O	–	L2	L1	L1
2		110110	O	–	L2	L1	L1
2		110111	O	–	L2	L1	L1
2		111000	O	–	L2	–	L2
2		111001	O	–	L2	L1	L1
2		111010	O	–	L2	L1	L1
2		111011	O	–	L2	L1	L1
2		111100	O	–	L2	–	L2
2		111101	O	–	L2	L1	L1
2		111110	O	–	L2	L1	L1
2		111111	O	–	L2	L1	L1

●DM1 Specifies the display mode of the first screen block.

●DM2 Specifies the display mode of the third screen block.

DM1 (block1) 0: Text mode

1: Graphic mode

DM2 (block3) 0: Text mode

1: Graphic mode

Note: The second and fourth screen blocks are limited to graphics mode.

●OV Specifies a two-layer or three-layer composition in graphics mode.

OV 0: Tow-layer composition

1: Three-layer composition

Note: Set OV = 0 for mixed text and graphics mode. When three-layer composition is specified, both the first and third screen blocks should be set to the graphics mode. (OV, DM2, DM1) = (1, 1, 1)

CGRAM ADR

●C Defines the offset address of CG RAM in the display memory space.

<Indirect mode>									<Direct mode>	
	MSB							LSB	Address	Register name
	D7	D6	D5	D4	D3	D2	D1	D0		
C	0	1	0	1	1	1	0	0	–	–
P1	A7	A6	A5	A4	A3	A2	A1	A0	0x8019	r_P1_CGRAMAdr
								(SAGL)		bit7-0 : A7-A0
P2	*	A14	A13	A12	A11	A10	A9	A8	0x801A	r_P2_CGRAMAdr
								(SAGH)		bit7-0 : A15-A8

Note: For details on how to define CG RAM, see Section 4.1.2 “Character Generator (CG)” on page 47.

HDOT SCR

Although the screen can be scrolled left or right only in units of characters using the SCROLL command alone, the combined use of this command allows the screen to be scrolled in units of dots. The scrolling on individual layers, however, cannot be controlled.

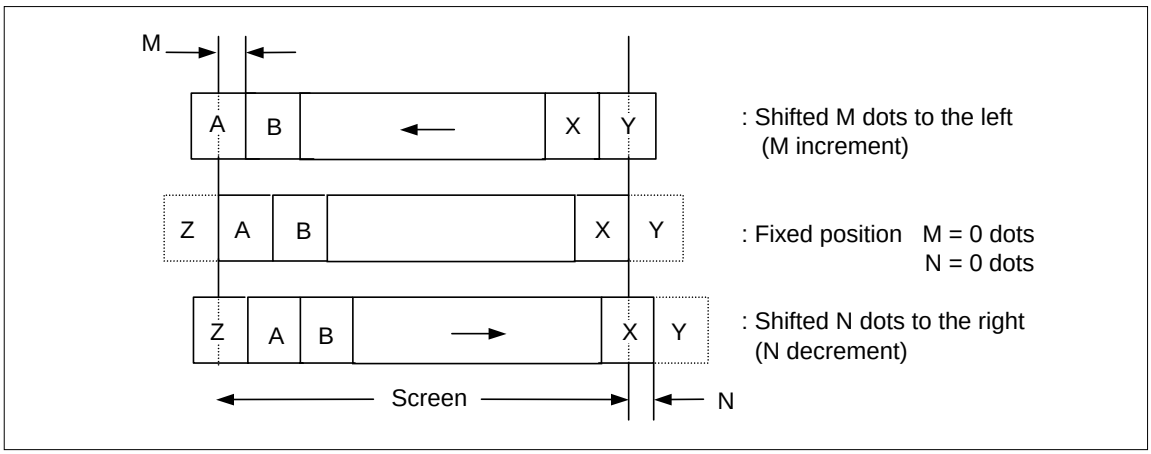
This command defines the number of dots to be shifted from the character origin.

<Indirect mode>									<Direct mode>	
	MSB							LSB	Address	Register name
	D7	D6	D5	D4	D3	D2	D1	D0		
C	0	1	0	1	1	0	1	0	–	–
P1	0	0	0	0	0	D2	D1	D0	0x801B	r_P1_HDotScr bit2-0 : D2-D0

[Parameter P1]

●D0 – D2 The C/R value must be set to one more than the number of display characters before using HDOT SCR to scroll the screen in units of dots. Smooth scrolling (dotwise scrolling) is possible when the MPU resends the HDOT SCR command to the S1D13700 at given time intervals for setting the number of dots to be shifted from the character origin.

HEX	BIN			Number of dots to be shifted
	D2	D1	D0	
00	0	0	0	0
01	0	0	1	1
02	0	1	0	2
•	•	•	•	•
•	•	•	•	•
06	1	1	0	6
07	1	1	1	7



Note: See Section 4.1.7 “Scrolling” on page 65, for more information about this function.

GRAY SCALE

This command sets up grayscale display mode.

<Indirect mode>	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	<Direct mode> Address	Register name
C	0	1	1	0	0	0	0	0	–	–
P1	0	0	0	0	0	0	D1	D0	0x8020	r_P1_GrayScale bit1-0 : D1-D0

[Parameter P1]

●D0 – D1 Specify the depth of grayscale.

HEX	BIN		Grayscale depth
	D2	D1	
00	0	0	1bpp
01	0	1	2bpp
02	1	0	4bpp
03	1	1	reserved

Note: For grayscale display, text and graphic mode overlays are inhibited.

3.3.3 *Drawing Control Commands*

CSRW

●C This command is used to write the cursor address to the cursor register. Because the S1D13700 has only one address input bit, only two addresses in the address space of the MPU can be specified at a time. Therefore, the MPU cannot directly access display memory. To compensate for this inconvenience, the S1D13700 has a 16-bit cursor register that serves the purpose of MPU addresses.

<Indirect mode>									<Direct mode>	
	MSB							LSB	Address	Register name
	D7	D6	D5	D4	D3	D2	D1	D0		
C	0	1	0	0	0	1	1	0	–	–
P1	A7	A6	A5	A4	A3	A2	A1	A0	0x801C	r_P1_CSRW
								(CSRL)		bit7-0 : A7-A0
P2	A15	A14	A13	A12	A11	A10	A9	A8	0x801D	r_P2_CSRW
								(CSRH)		bit7-0 : A15-A8

The cursor address is set in the S1D13700 before display memory (VRAM, CG RAM, or CG ROM) is automatically accessed. If this address is not set, display starts from the address set last or an automatically shifted address. (The cursor address register can only be modified by other than the CSRW command by executing a memory control command.)

The cursor address is not affected by scrolling display because it is managed by the absolute display memory addresses fixed in hardware. Note also that the cursor address points to the absolute display memory address where data for the origin part of the character field is stored.

CSRR

●C This command is used to read a cursor address from the cursor register.When this command is written to the S1D13700, the low-order byte of the cursor address (CSRL) is set in the output buffer. Therefore, the high-order byte of the cursor address (CSRH) also can be read out by entering the RD signal following this command.

<Indirect mode>									<Direct mode>	
	MSB							LSB	Address	Register name
	D7	D6	D5	D4	D3	D2	D1	D0		
C	0	1	0	0	0	1	1	0	–	–
P1	A7	A6	A5	A4	A3	A2	A1	A0	0x801E	r_P1_CSRR
								(CSRL) Note		bit7-0 : A7-A0
P2	A15	A14	A13	A12	A11	A10	A9	A8	0x801F	r_P2_CSRR
								(CSRH) Note		bit7-0 : A15-A8

Note: This is the read data.

3.3.4 Memory Control Commands

MWRITE

This command is used by the MPU to place the S1D13700 in the data input state before writing data to display memory. Each time the WR# signal is input following this command, the S1D13700 automatically modifies the cursor address at which to write display memory according to the CSRDIR value. This allows the MPU to write two or more consecutive items of data to display memory.

	MSB							LSB	
C	0	1	0	0	0	0	1	0	
P1	*	*	*	*	*	*	*	*	
P2	*	*	*	*	*	*	*	*	
Pn	*	*	*	*	*	*	*	*	n ≥ 1

P1, P2, ..., Pn: Display data

MREAD

This command is used to place the S1D13700 in the data output state and store the contents of display memory (specified by the cursor address) in the data bus buffer before reading data from display memory. Each time the RD# signal is input following this command, the read cursor address of display memory is automatically modified according to the CSRDIR value, and read data is stored in the data bus buffer. Because the command is executed in a manner similar to pipelined processing, high-speed readout limited only by the MPU cycle time is possible.

When the cursor is displayed, the read data and cursor positions do not match (with the cursor two positions ahead).

	MSB							LSB		
C	0	1	0	0	0	0	1	1		
P1	*	*	*	*	*	*	*	*		Read data
P2	*	*	*	*	*	*	*	*		
Pn	*	*	*	*	*	*	*	*	n ≥ 1	

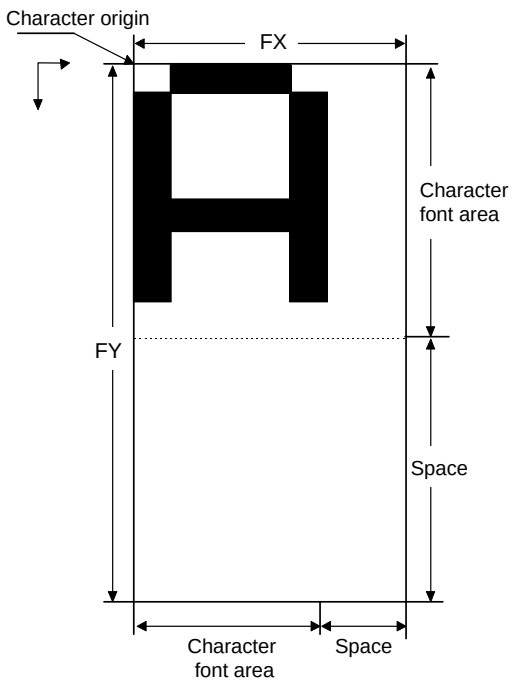
4 FUNCTION DESCRIPTION

4.1 Display Functions

4.1.1 Screen Management

(1) Character configuration

The S1D13700 can display characters using a row-scanning type of character generator that defines character patterns in the fourth quadrant with respect to the character origin as shown below. Although the character generator used determines the size of the character font area, the size of the character field can be varied in both the X and Y directions.



	D7 MSB			–				D0 LSB
R0	0	1	1	1	0	0	0	0
R1	1	0	0	0	1	0	0	0
R2	1	0	0	0	1	0	0	0
R3	1	0	0	0	1	0	0	0
R4	1	1	1	1	1	0	0	0
R5	1	0	0	0	1	0	0	0
R6	1	0	0	0	1	0	0	0
R7	0	0	0	0	0	0	0	0
R8	0	0	0	0	0	0	0	0
R9	0	0	0	0	0	0	0	0
R10	0	0	0	0	0	0	0	0
R11	0	0	0	0	0	0	0	0
R12	0	0	0	0	0	0	0	0
R13	0	0	0	0	0	0	0	0
R14	0	0	0	0	0	0	0	0
R15	0	0	0	0	0	0	0	0

Space data

Space data

Figure 4-1 Character display ([FX] ≤ 8 dots)

Figure 4-2 Example of character generator definition

Character font area: An area in which the character pattern is drawn

Character field: Character font area + space

To alter the character field, leave any portions other than the character font area set to 0 and increase FX or FY to enlarge the size of space as desired.

Even when one character requires two or more memory addresses, the character field can be set to any desired size.

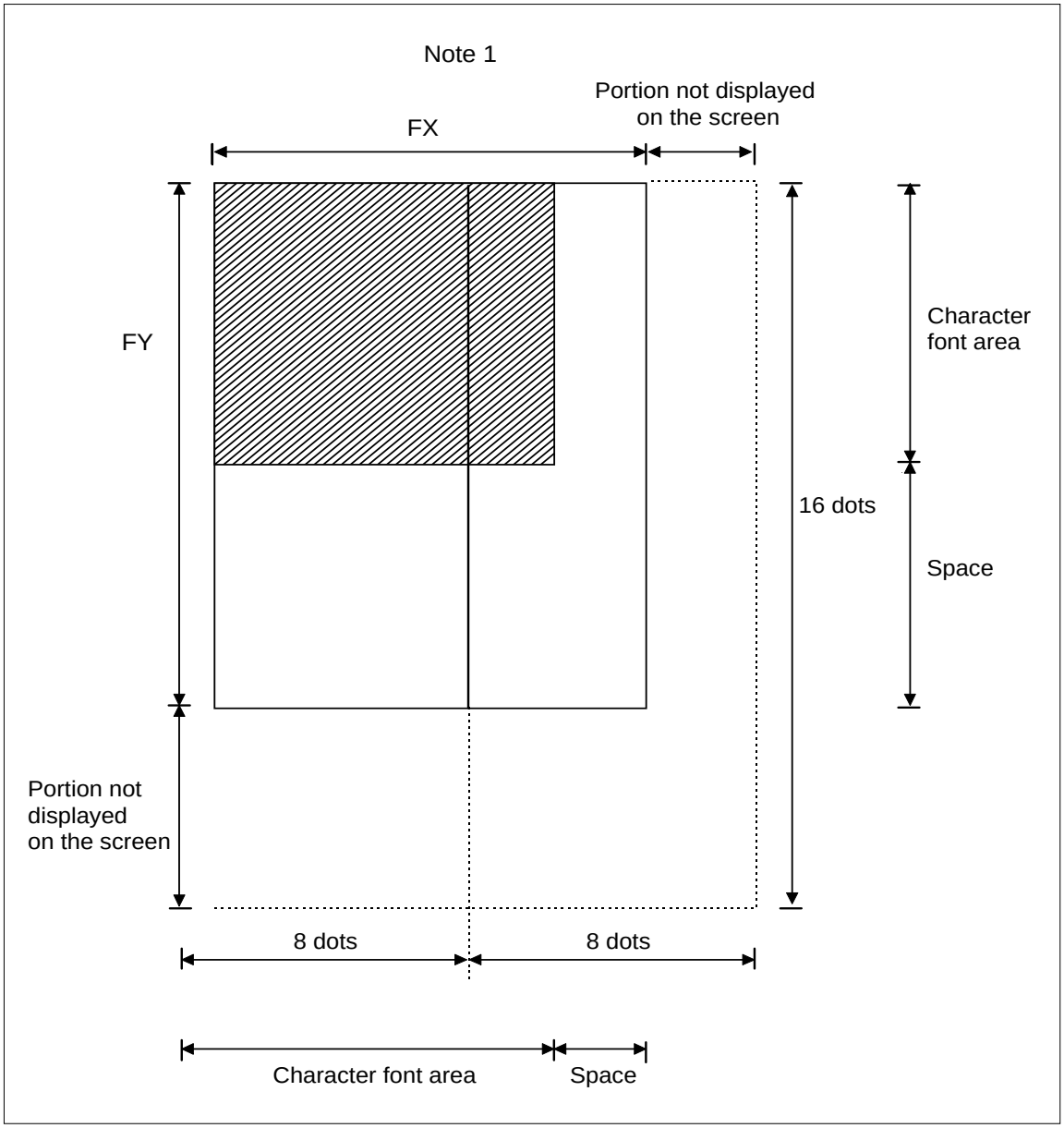


Figure 4-3 Example of character configuration consisting of two or more memory addresses (when [FX] = 9)

Note 1: The S1D13700 does not automatically insert character spaces. If the character field is greater than or equal to 9 dots, two memory addresses are required to configure one character even when the character font area may be within 8 dots.

4.1.2 Character Generator (CG)

(1) Features of each character generator

① Internal character generator

The internal character generator is effective for a minimum display system consisting of the S1D13700, display memory (data RAM), LCD unit, single-chip MPU, and a power supply. Moreover, because the internal character generator includes CMOS mask ROM, it is very advantageous when low power consumption is desired.

●Character font
- 5 x 7 dots (See Section 4.4.1 “Character Fonts (Internal CG)” on page 81.)

●Number of characters
- JIS-compliant 160 characters

●Combined use with CG RAM possible (up to 64 characters)

●Processing of the character field space part

The S1D13700 automatically sets spaces in the range of 8 x 16 dots maximum.

② CG RAM

CG RAM as a graphic generator allows any desired character font to be defined by the user. Moreover, because the MPU can alter address mapping in the display memory space can be altered as required, unused portions of display memory can be effectively utilized.

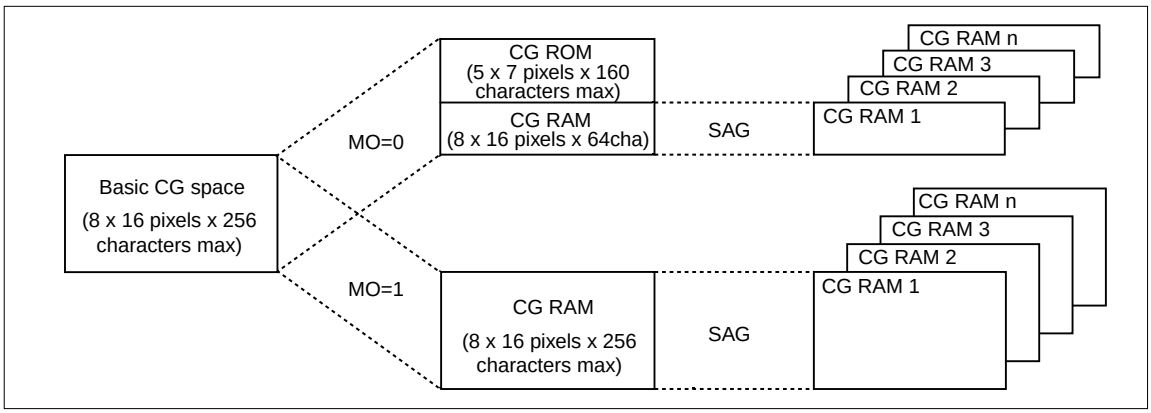
●Character font
- 8 x 8 dots maximum <M2 = 0>
- 8 x 16 dots maximum <M2 = 1>

●Number of characters
- Up to 64 characters when used in combination with CG ROM
- Up to 256 characters when used only in F000H to FFFFH

●Defined area of CG RAM in the display memory space
- CG RAM (maximum 64 characters) that can be used in combination with CG ROM can be allocated to any desired contiguous addresses.
- CG RAM (maximum 65 characters or more) that cannot be used in combination with CG ROM must be allocated to fixed addresses F000H through FFFFH. When 193 characters or more must be defined in this fixed address area, set SAG = F000H and M1 = 0.

(2) Concept of how character generator banks are set

Because the character codes handled by the S1D13700 consist of 8 bits, the number of discrete characters that can be displayed simultaneously is limited to a maximum of 256. The CGRAM ADR command can be used to switch banks, however, thus extending the number of usable characters as shown below.



Note: Up to 64 characters can be used in one bank when used in combination with CG ROM. When using only CG RAM, up to 256 characters can be used in one bank. Also note that the relationship between CG patterns and character codes changes when banks are switched over.

(3) Method of determining the CG address

The addition shown below is performed to generate CG RAM addresses. Therefore, note that CG RAM data is not mapped from addresses set in the SAG register to the VRAM space, but are mapped based on the SAG + character code + row select address.

①When number of lines that comprise the character font is equal to or less than 8 (M2 = 0, M1 = 0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0
+ row select address	0	0	0	0	0	0	0	0	0	0	0	0	0	R2	R1	R0
CG RAM address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

②When number of lines that comprise the character font is from 9 to 16, including both ends (M2 = 1, M1 = 0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0
+ row select address	0	0	0	0	0	0	0	0	0	0	0	0	R3	R2	R1	R0
CG RAM address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

Note: Only the addressing above is supported.

Table 4-1 Row Select Addresses

	R3	R2	R1	R0	
ROW0	0	0	0	0	Line count 1
ROW1	0	0	0	1	
ROW2	0	0	1	0	
.	.	.	.	.	
.	.	.	.	.	
.	.	.	.	.	
ROW7	0	1	1	1	
ROW8	1	0	0	0	Line count 2
.	.	.	.	.	
.	.	.	.	.	
.	.	.	.	.	
ROW14	1	1	1	0	
ROW15	1	1	1	1	

Note: 1. Line count l ... when character font consists of 8 lines or less
Line count 2 ... when character font consists of 9 lines or more

③When M1 = 1

For the character codes defined in CG RAM2, the S1D13700 automatically changes the D6 bit in the character code from 1 to 0. This ensures that the data storage area in CG RAM corresponds to

contiguous addresses in the display memory space. Therefore, the CG RAM addresses to which to write data must be calculated as follows:

- Add addresses the same way as described above (M1 = 0).
- Change bit D6 in one character code from 1 to 0 when adding addresses.

Example of CG RAM definition (method of storing data) (See Figure 4-9 “Example of display memory mapping” on page 63.)

●Conditions

- The pattern to define: Pattern A (8 x 16 dots per font) shown in Figure 4-1 “Character display ([FX] ≤ 8 dots)” on page 45.
- Start address of the CG RAM table: 4800H
- Character code of defined pattern: 80H (first character code in CG RAM area)

●Setting list

CG RAM ADR	5CH	Set SAG after calculating it by performing the method of CG RAM address calculation in reverse.
P1	00H	
P2	40H	
CSRDIR	4CH	Shift to the right
CSRW	46H	CG RAM area from 4800H
P1	00H	
P2	48H	
MWRITE	42H	
P1	70H	Write data for row 0
P2	88H	Write data for row 1
P3	88H	Write data for row 2
P4	88H	Write data for row 3
P5	F8H	Write data for row 4
P6	88H	Write data for row 5
P7	88H	Write data for row 6
P8	00H	Write data for row 7
P9	00H	Write data for row 8
.	.	. .
.	.	. .
.	.	. .
P16	00H	Write data for row 15

4.1.3 Screen Configuration

(1) Screen configuration

The basic screen configuration of the S1D13700 consists of a text or graphics screen and an overlapping graphics screen. The graphics screen uses at least eight times as much display memory as the text screen.

Figure 4-4 schematically shows the relationship between the virtual and physical screens.

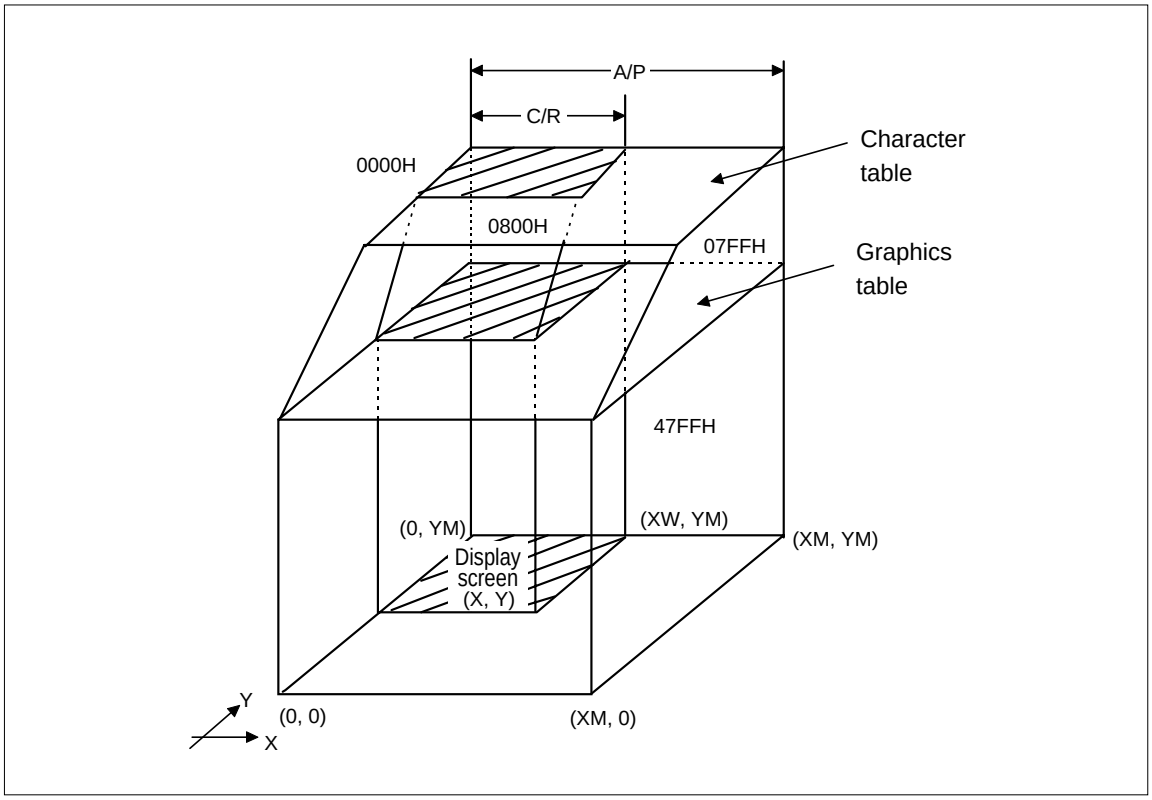


Figure 4-4 Relationship between virtual and physical screens

(2) Display address incrementation

The S1D13700 sequentially increments the display address in the X direction from the screen origin (home position) in the same way as a raster scan CRT. When the display address is incremented until the number of addresses equals C/R, one line of data is read from display memory. Next, to read the second line of data when in graphics mode, the S1D13700 starts from the address incremented by the distance equal to the address pitch (AP) from the address of the screen origin (SAD), then repeats the same operation as described above for the first line.

Conversely, in text mode the S1D13700 repeats the same operation as described above for the first line until the display address for one character is completed. (Character code is read from the same area, and data is read out in order of R0–R15 of the character generator.) (See Figure 4-2 “Example of character generator definition” on page 45.)

<< (W/S, OV, DM2, DM1, FY) = (0, 0, 0, 0, 8) >> (BK1, BK2, BK3, BK4) = (Character (Layer1), Graphic (Layer2), Character (Layer1), -)

*ReadTurn

LineNo 1	SAD1	SAD2		SAD1+1	SAD2+1		...	SAD1+CR	SAD2+CR		(1)
2	SAD1+AP	SAD2+AP		SAD1+AP+1	SAD2+AP+1			SAD1+AP+CR	SAD2+AP+CR		(2)
3	SAD1+2AP	SAD2+2AP		SAD1+2AP+1	SAD2+2AP+1		...	SAD1+2AP+CR	SAD2+2AP+CR		(3)
4	SAD1+3AP	SAD2+3AP		SAD1+3AP+1	SAD2+3AP+1			SAD1+3AP+CR	SAD2+3AP+CR		(4)
5	SAD1+4AP	SAD2+4AP		SAD1+4AP+1	SAD2+4AP+1		...	SAD1+4AP+CR	SAD2+4AP+CR		
6	SAD1+5AP	SAD2+5AP		SAD1+5AP+1	SAD2+5AP+1			SAD1+5AP+CR	SAD2+5AP+CR		
7	SAD1+6AP	SAD2+6AP		SAD1+6AP+1	SAD2+6AP+1		...	SAD1+6AP+CR	SAD2+6AP+CR		
8	SAD1+7AP	SAD2+7AP		SAD1+7AP+1	SAD2+7AP+1			SAD1+7AP+CR	SAD2+7AP+CR		
9	SAD1+8AP	SAD2+8AP		SAD1+8AP+1	SAD2+8AP+1		...	SAD1+8AP+CR	SAD2+8AP+CR		
10	SAD1+9AP	SAD2+9AP		SAD1+9AP+1	SAD2+9AP+1			SAD1+9AP+CR	SAD2+9AP+CR		
11	SAD1+10AP	SAD2+10AP		SAD1+10AP+1	SAD2+10AP+1		...	SAD1+10AP+CR	SAD2+10AP+CR		
12	SAD1+11AP	SAD2+11AP		SAD1+11AP+1	SAD2+11AP+1			SAD1+11AP+CR	SAD2+11AP+CR		
13	SAD1+12AP	SAD2+12AP		SAD1+12AP+1	SAD2+12AP+1		...	SAD1+12AP+CR	SAD2+12AP+CR		
14	SAD1+13AP	SAD2+13AP		SAD1+13AP+1	SAD2+13AP+1			SAD1+13AP+CR	SAD2+13AP+CR		
15	SAD1+14AP	SAD2+14AP		SAD1+14AP+1	SAD2+14AP+1		...	SAD1+14AP+CR	SAD2+14AP+CR		
16	SAD1+15AP	SAD2+15AP		SAD1+15AP+1	SAD2+15AP+1			SAD1+15AP+CR	SAD2+15AP+CR		
SL1-7	SAD1+(SL1-7)AP	SAD2+(SL1-7)AP		SAD1+(SL1-7)AP+1	SAD2+(SL1-7)AP+1		...	SAD1+(SL1-7)AP+CR	SAD2+(SL1-7)AP+CR		
SL1-6	SAD1+(SL1-6)AP	SAD2+(SL1-6)AP		SAD1+(SL1-6)AP+1	SAD2+(SL1-6)AP+1			SAD1+(SL1-6)AP+CR	SAD2+(SL1-6)AP+CR		
SL1-5	SAD1+(SL1-5)AP	SAD2+(SL1-5)AP		SAD1+(SL1-5)AP+1	SAD2+(SL1-5)AP+1		...	SAD1+(SL1-5)AP+CR	SAD2+(SL1-5)AP+CR		
SL1-4	SAD1+(SL1-4)AP	SAD2+(SL1-4)AP		SAD1+(SL1-4)AP+1	SAD2+(SL1-4)AP+1			SAD1+(SL1-4)AP+CR	SAD2+(SL1-4)AP+CR		
SL1-3	SAD1+(SL1-3)AP	SAD2+(SL1-3)AP		SAD1+(SL1-3)AP+1	SAD2+(SL1-3)AP+1		...	SAD1+(SL1-3)AP+CR	SAD2+(SL1-3)AP+CR		
SL1-2	SAD1+(SL1-2)AP	SAD2+(SL1-2)AP		SAD1+(SL1-2)AP+1	SAD2+(SL1-2)AP+1			SAD1+(SL1-2)AP+CR	SAD2+(SL1-2)AP+CR		
SL1-1	SAD1+(SL1-1)AP	SAD2+(SL1-1)AP		SAD1+(SL1-1)AP+1	SAD2+(SL1-1)AP+1		...	SAD1+(SL1-1)AP+CR	SAD2+(SL1-1)AP+CR		
SL1	SAD1+(SL1)AP	SAD2+(SL1)AP		SAD1+(SL1)AP+1	SAD2+(SL1)AP+1			SAD1+(SL1)AP+CR	SAD2+(SL1)AP+CR		
SL1+1		SAD2+(SL1+1)AP			SAD2+(SL1+1)AP+1		...		SAD2+(SL1+1)AP+CR		
SL1+2		SAD2+(SL1+2)AP			SAD2+(SL1+2)AP+1				SAD2+(SL1+2)AP+CR		
SL1+3		SAD2+(SL1+3)AP			SAD2+(SL1+3)AP+1		...		SAD2+(SL1+3)AP+CR		
SL1+4	SAD3	SAD2+(SL1+4)AP	CG3	SAD3+1	SAD2+(SL1+4)AP+1	CG3		SAD3+CR	SAD2+(SL1+4)AP+CR	CG3	
SL1+5		SAD2+(SL1+5)AP			SAD2+(SL1+5)AP+1		...		SAD2+(SL1+5)AP+CR		
SL1+6		SAD2+(SL1+6)AP			SAD2+(SL1+6)AP+1				SAD2+(SL1+6)AP+CR		
SL1+7		SAD2+(SL1+7)AP			SAD2+(SL1+7)AP+1		...		SAD2+(SL1+7)AP+CR		
SL1+8		SAD2+(SL1+8)AP			SAD2+(SL1+8)AP+1				SAD2+(SL1+8)AP+CR		
SL1+9		SAD2+(SL1+9)AP			SAD2+(SL1+9)AP+1		...		SAD2+(SL1+9)AP+CR		
SL1+10		SAD2+(SL1+10)AP			SAD2+(SL1+10)AP+1				SAD2+(SL1+10)AP+CR		
SL1+11		SAD2+(SL1+11)AP			SAD2+(SL1+11)AP+1		...		SAD2+(SL1+11)AP+CR		
SL1+12	SAD3+AP	SAD2+(SL1+12)AP	CG3	SAD3+AP+1	SAD2+(SL1+12)AP+1	CG3		SAD3+AP+CR	SAD2+(SL1+12)AP+CR	CG3	
SL1+13		SAD2+(SL1+13)AP			SAD2+(SL1+13)AP+1		...		SAD2+(SL1+13)AP+CR		
SL1+14		SAD2+(SL1+14)AP			SAD2+(SL1+14)AP+1				SAD2+(SL1+14)AP+CR		
SL1+15		SAD2+(SL1+15)AP			SAD2+(SL1+15)AP+1		...		SAD2+(SL1+15)AP+CR		
SL1+16		SAD2+(SL1+16)AP			SAD2+(SL1+16)AP+1				SAD2+(SL1+16)AP+CR		
LF-7		SAD2+(LF-7)AP			SAD2+(LF-7)AP+1		...		SAD2+(LF-7)AP+CR		
LF-6		SAD2+(LF-6)AP			SAD2+(LF-6)AP+1				SAD2+(LF-6)AP+CR		
LF-5		SAD2+(LF-5)AP			SAD2+(LF-5)AP+1		...		SAD2+(LF-5)AP+CR		(LF-5)
LF-4	SAD3+(LD/8)AP	SAD2+(LF-4)AP	CG3	SAD3+(LF/8)+1	SAD2+(LF-4)AP+1	CG3		SAD3+(LF/8)+CR	SAD2+(LF-4)AP+CR	CG3	(LF-4)
LF-3		SAD2+(LF-3)AP			SAD2+(LF-3)AP+1		...		SAD2+(LF-3)AP+CR		(LF-3)
LF-2		SAD2+(LF-2)AP			SAD2+(LF-2)AP+1				SAD2+(LF-2)AP+CR		(LF-2)
LF-1		SAD2+(LF-1)AP			SAD2+(LF-1)AP+1		...		SAD2+(LF-1)AP+CR		(LF-1)
LF		SAD2+(LF)AP			SAD2+(LF)AP+1				SAD2+(LF)AP+CR		(LF)

<< (W/S, OV, DM2, DM1, FY) = (0, 0, 0, 0, 8) >> (BK1, BK2, BK3, BK4) = (Character (Layer1), Graphic (Layer2), Character (Layer1), -)

*ReadTurn

LineNo										
1	SAD1	SAD2	CG1	SAD1+1	SAD2+1	CG1	…	SAD1+CR	SAD2+CR	CG1	(1)
2		SAD2+AP			SAD2+AP+1				SAD2+AP+CR		(2)
3		SAD2+2AP			SAD2+2AP+1		…		SAD2+2AP+CR		(3)
4		SAD2+3AP			SAD2+3AP+1				SAD2+3AP+CR		(4)
5		SAD2+4AP			SAD2+4AP+1		…		SAD2+4AP+CR		
6		SAD2+5AP			SAD2+5AP+1				SAD2+5AP+CR		
7		SAD2+6AP			SAD2+6AP+1		…		SAD2+6AP+CR		
8		SAD2+7AP			SAD2+7AP+1				SAD2+7AP+CR		
9	SAD1+AP	SAD2+8AP	CG1	SAD1+AP+1	SAD2+8AP+1	CG1	…	SAD1+AP+CR	SAD2+8AP+CR	CG1	
10		SAD2+9AP			SAD2+9AP+1				SAD2+9AP+CR		
11		SAD2+10AP			SAD2+10AP+1		…		SAD2+10AP+CR		
12		SAD2+11AP			SAD2+11AP+1				SAD2+11AP+CR		
13		SAD2+12AP			SAD2+12AP+1		…		SAD2+12AP+CR		
14		SAD2+13AP			SAD2+13AP+1				SAD2+13AP+CR		
15		SAD2+14AP			SAD2+14AP+1		…		SAD2+14AP+CR		
16		SAD2+15AP			SAD2+15AP+1				SAD2+15AP+CR		
SL1-7	SAD1+(SL1/8)AP	SAD2+(SL1-7)AP	CG1	SAD1+(SL1/8)AP+1	SAD2+(SL1-7)AP+1	CG1	…	SAD1+(SL1/8)AP+CR	SAD2+(SL1-7)AP+CR	CG1	
SL1-6		SAD2+(SL1-6)AP			SAD2+(SL1-6)AP+1				SAD2+(SL1-6)AP+CR		
SL1-5		SAD2+(SL1-5)AP			SAD2+(SL1-5)AP+1		…		SAD2+(SL1-5)AP+CR		
SL1-4		SAD2+(SL1-4)AP			SAD2+(SL1-4)AP+1				SAD2+(SL1-4)AP+CR		
SL1-3		SAD2+(SL1-3)AP			SAD2+(SL1-3)AP+1		…		SAD2+(SL1-3)AP+CR		
SL1-2		SAD2+(SL1-2)AP			SAD2+(SL1-2)AP+1				SAD2+(SL1-2)AP+CR		
SL1-1		SAD2+(SL1-1)AP			SAD2+(SL1-1)AP+1		…		SAD2+(SL1-1)AP+CR		
SL1		SAD2+(SL1)AP			SAD2+(SL1)AP+1				SAD2+(SL1)AP+CR		
SL1+1	SAD3	SAD2+(SL1+1)AP		SAD3+1	SAD2+(SL1+1)AP+1		…	SAD3+CR	SAD2+(SL1+1)AP+CR		
SL1+2	SAD3+AP	SAD2+(SL1+2)AP		SAD3+AP+1	SAD2+(SL1+2)AP+1			SAD3+AP+CR	SAD2+(SL1+2)AP+CR		
SL1+3	SAD3+2AP	SAD2+(SL1+3)AP		SAD3+2AP+1	SAD2+(SL1+3)AP+1		…	SAD3+2AP+CR	SAD2+(SL1+3)AP+CR		
SL1+4	SAD3+3AP	SAD2+(SL1+4)AP		SAD3+3AP+1	SAD2+(SL1+4)AP+1			SAD3+3AP+CR	SAD2+(SL1+4)AP+CR		
SL1+5	SAD3+4AP	SAD2+(SL1+5)AP		SAD3+4AP+1	SAD2+(SL1+5)AP+1		…	SAD3+4AP+CR	SAD2+(SL1+5)AP+CR		
SL1+6	SAD3+5AP	SAD2+(SL1+6)AP		SAD3+5AP+1	SAD2+(SL1+6)AP+1			SAD3+5AP+CR	SAD2+(SL1+6)AP+CR		
SL1+7	SAD3+6AP	SAD2+(SL1+7)AP		SAD3+6AP+1	SAD2+(SL1+7)AP+1		…	SAD3+6AP+CR	SAD2+(SL1+7)AP+CR		
SL1+8	SAD3+7AP	SAD2+(SL1+8)AP		SAD3+7AP+1	SAD2+(SL1+8)AP+1			SAD3+7AP+CR	SAD2+(SL1+8)AP+CR		
SL1+9	SAD3+8AP	SAD2+(SL1+9)AP		SAD3+8AP+1	SAD2+(SL1+9)AP+1		…	SAD3+8AP+CR	SAD2+(SL1+9)AP+CR		
SL1+10	SAD3+9AP	SAD2+(SL1+10)AP		SAD3+9AP+1	SAD2+(SL1+10)AP+1			SAD3+9AP+CR	SAD2+(SL1+10)AP+CR		
SL1+11	SAD3+10AP	SAD2+(SL1+11)AP		SAD3+10AP+1	SAD2+(SL1+11)AP+1		…	SAD3+10AP+CR	SAD2+(SL1+11)AP+CR		
SL1+12	SAD3+11AP	SAD2+(SL1+12)AP		SAD3+11AP+1	SAD2+(SL1+12)AP+1			SAD3+11AP+CR	SAD2+(SL1+12)AP+CR		
SL1+13	SAD3+12AP	SAD2+(SL1+13)AP		SAD3+12AP+1	SAD2+(SL1+13)AP+1		…	SAD3+12AP+CR	SAD2+(SL1+13)AP+CR		
SL1+14	SAD3+13AP	SAD2+(SL1+14)AP		SAD3+13AP+1	SAD2+(SL1+14)AP+1			SAD3+13AP+CR	SAD2+(SL1+14)AP+CR		
SL1+15	SAD3+14AP	SAD2+(SL1+15)AP		SAD3+14AP+1	SAD2+(SL1+15)AP+1		…	SAD3+14AP+CR	SAD2+(SL1+15)AP+CR		
SL1+16	SAD3+15AP	SAD2+(SL1+16)AP		SAD3+15AP+1	SAD2+(SL1+16)AP+1			SAD3+15AP+CR	SAD2+(SL1+16)AP+CR		
LF-7	SAD3+(LF-SL1-7)AP	SAD2+(LF-7)AP		SAD3+(LF-SL1-7)AP+1	SAD2+(LF-7)AP+1		…	SAD3+(LF-SL1-7)AP+CR	SAD2+(LF-7)AP+CR		
LF-6	SAD3+(LF-SL1-6)AP	SAD2+(LF-6)AP		SAD3+(LF-SL1-6)AP+1	SAD2+(LF-6)AP+1			SAD3+(LF-SL1-6)AP+CR	SAD2+(LF-6)AP+CR		
LF-5	SAD3+(LF-SL1-5)AP	SAD2+(LF-5)AP		SAD3+(LF-SL1-5)AP+1	SAD2+(LF-5)AP+1		…	SAD3+(LF-SL1-5)AP+CR	SAD2+(LF-5)AP+CR		(LF-5)
LF-4	SAD3+(LF-SL1-4)AP	SAD2+(LF-4)AP		SAD3+(LF-SL1-4)AP+1	SAD2+(LF-4)AP+1			SAD3+(LF-SL1-4)AP+CR	SAD2+(LF-4)AP+CR		(LF-4)
LF-3	SAD3+(LF-SL1-3)AP	SAD2+(LF-3)AP		SAD3+(LF-SL1-3)AP+1	SAD2+(LF-3)AP+1		…	SAD3+(LF-SL1-3)AP+CR	SAD2+(LF-3)AP+CR		(LF-3)
LF-2	SAD3+(LF-SL1-2)AP	SAD2+(LF-2)AP		SAD3+(LF-SL1-2)AP+1	SAD2+(LF-2)AP+1			SAD3+(LF-SL1-2)AP+CR	SAD2+(LF-2)AP+CR		(LF-2)
LF-1	SAD3+(LF-SL1-1)AP	SAD2+(LF-1)AP		SAD3+(LF-SL1-1)AP+1	SAD2+(LF-1)AP+1		…	SAD3+(LF-SL1-1)AP+CR	SAD2+(LF-1)AP+CR		(LF-1)
LF	SAD3+(LF-SL1)AP	SAD2+(LF)AP		SAD3+(LF-SL1)AP+1	SAD2+(LF)AP+1			SAD3+(LF-SL1)AP+CR	SAD2+(LF)AP+CR		(LF)

VA0-15(case1)

<< (W/S, OV, DM2, DM1, FY) = (0, 0, 0, 0, 8) >> **(BK1, BK2, BK3, BK4) = (Character (Layer1), Graphic (Layer2), Character (Layer1), -)**

LineNo										*ReadTurn
1	SAD1	SAD2	CG1	SAD1+1	SAD2+1	CG1	…	SAD1+CR	SAD2+CR	CG1	(1)
2		SAD2+AP			SAD2+AP+1				SAD2+AP+CR		(2)
3		SAD2+2AP			SAD2+2AP+1		…		SAD2+2AP+CR		(3)
4		SAD2+3AP			SAD2+3AP+1				SAD2+3AP+CR		(4)
5		SAD2+4AP			SAD2+4AP+1		…		SAD2+4AP+CR		
6		SAD2+5AP			SAD2+5AP+1				SAD2+5AP+CR		
7		SAD2+6AP			SAD2+6AP+1		…		SAD2+6AP+CR		
8		SAD2+7AP			SAD2+7AP+1				SAD2+7AP+CR		
9	SAD1+AP	SAD2+8AP	CG1	SAD1+AP+1	SAD2+8AP+1	CG1	…	SAD1+AP+CR	SAD2+8AP+CR	CG1	
10		SAD2+9AP			SAD2+9AP+1				SAD2+9AP+CR		
11		SAD2+10AP			SAD2+10AP+1		…		SAD2+10AP+CR		
12		SAD2+11AP			SAD2+11AP+1				SAD2+11AP+CR		
13		SAD2+12AP			SAD2+12AP+1		…		SAD2+12AP+CR		
14		SAD2+13AP			SAD2+13AP+1				SAD2+13AP+CR		
15		SAD2+14AP			SAD2+14AP+1		…		SAD2+14AP+CR		
16		SAD2+15AP			SAD2+15AP+1				SAD2+15AP+CR		
SL1-7	SAD1+(SL1/8)AP	SAD2+(SL1-7)AP	CG1	SAD1+(SL1/8)AP+1	SAD2+(SL1-7)AP+1	CG1	…	SAD1+(SL1/8)AP+CR	SAD2+(SL1-7)AP+CR	CG1	
SL1-6		SAD2+(SL1-6)AP			SAD2+(SL1-6)AP+1				SAD2+(SL1-6)AP+CR		
SL1-5		SAD2+(SL1-5)AP			SAD2+(SL1-5)AP+1		…		SAD2+(SL1-5)AP+CR		
SL1-4		SAD2+(SL1-4)AP			SAD2+(SL1-4)AP+1				SAD2+(SL1-4)AP+CR		
SL1-3		SAD2+(SL1-3)AP			SAD2+(SL1-3)AP+1		…		SAD2+(SL1-3)AP+CR		
SL1-2		SAD2+(SL1-2)AP			SAD2+(SL1-2)AP+1				SAD2+(SL1-2)AP+CR		
SL1-1		SAD2+(SL1-1)AP			SAD2+(SL1-1)AP+1		…		SAD2+(SL1-1)AP+CR		
SL1		SAD2+(SL1)AP			SAD2+(SL1)AP+1				SAD2+(SL1)AP+CR		
SL1+1	SAD3	SAD2+(SL1+1)AP	CG3	SAD3+1	SAD2+(SL1+1)AP+1	CG3	…	SAD3+CR	SAD2+(SL1+1)AP+CR	CG3	
SL1+2		SAD2+(SL1+2)AP			SAD2+(SL1+2)AP+1				SAD2+(SL1+2)AP+CR		
SL1+3		SAD2+(SL1+3)AP			SAD2+(SL1+3)AP+1		…		SAD2+(SL1+3)AP+CR		
SL1+4		SAD2+(SL1+4)AP			SAD2+(SL1+4)AP+1				SAD2+(SL1+4)AP+CR		
SL1+5		SAD2+(SL1+5)AP			SAD2+(SL1+5)AP+1		…		SAD2+(SL1+5)AP+CR		
SL1+6		SAD2+(SL1+6)AP			SAD2+(SL1+6)AP+1				SAD2+(SL1+6)AP+CR		
SL1+7		SAD2+(SL1+7)AP			SAD2+(SL1+7)AP+1		…		SAD2+(SL1+7)AP+CR		
SL1+8		SAD2+(SL1+8)AP			SAD2+(SL1+8)AP+1				SAD2+(SL1+8)AP+CR		
SL1+9	SAD3+AP	SAD2+(SL1+9)AP	CG3	SAD3+AP+1	SAD2+(SL1+9)AP+1	CG3	…	SAD3+AP+CR	SAD2+(SL1+9)AP+CR	CG3	
SL1+10		SAD2+(SL1+10)AP			SAD2+(SL1+10)AP+1				SAD2+(SL1+10)AP+CR		
SL1+11		SAD2+(SL1+11)AP			SAD2+(SL1+11)AP+1		…		SAD2+(SL1+11)AP+CR		
SL1+12		SAD2+(SL1+12)AP			SAD2+(SL1+12)AP+1				SAD2+(SL1+12)AP+CR		
SL1+13		SAD2+(SL1+13)AP			SAD2+(SL1+13)AP+1		…		SAD2+(SL1+13)AP+CR		
SL1+14		SAD2+(SL1+14)AP			SAD2+(SL1+14)AP+1				SAD2+(SL1+14)AP+CR		
SL1+15		SAD2+(SL1+15)AP			SAD2+(SL1+15)AP+1		…		SAD2+(SL1+15)AP+CR		
SL1+16		SAD2+(SL1+16)AP			SAD2+(SL1+16)AP+1				SAD2+(SL1+16)AP+CR		
LF-7	SAD3+(LD/8)AP	SAD2+(LF-7)AP	CG3	SAD3+(LF/8)+1	SAD2+(LF-7)AP+1	CG3	…	SAD3+(LF/8)+CR	SAD2+(LF-7)AP+CR	CG3	
LF-6		SAD2+(LF-6)AP			SAD2+(LF-6)AP+1				SAD2+(LF-6)AP+CR		
LF-5		SAD2+(LF-5)AP			SAD2+(LF-5)AP+1		…		SAD2+(LF-5)AP+CR		(LF-5)
LF-4		SAD2+(LF-4)AP			SAD2+(LF-4)AP+1				SAD2+(LF-4)AP+CR		(LF-4)
LF-3		SAD2+(LF-3)AP			SAD2+(LF-3)AP+1		…		SAD2+(LF-3)AP+CR		(LF-3)
LF-2		SAD2+(LF-2)AP			SAD2+(LF-2)AP+1				SAD2+(LF-2)AP+CR		(LF-2)
LF-1		SAD2+(LF1)AP			SAD2+(LF-1)AP+1		…		SAD2+(LF-1)AP+CR		(LF-1)
LF		SAD2+(LF)AP			SAD2+(LF)AP+1				SAD2+(LF)AP+CR		(LF)

VA0-15(case2)

<< (W/S, OV, DM2, DM1, FY) = (0, 0, 1, 1, 8) >> **(BK1, BK2, BK3, BK4) = Graphic (Layer1), Graphic (Layer2), Graphic (Layer1), -)**

*ReadTurn

LineNo 1	SAD1	SAD2		SAD1+1	SAD2+1		...	SAD1+CR	SAD2+CR		(1)
2	SAD1+AP	SAD2+AP		SAD1+AP+1	SAD2+AP+1			SAD1+AP+CR	SAD2+AP+CR		(2)
3	SAD1+2AP	SAD2+2AP		SAD1+2AP+1	SAD2+2AP+1		...	SAD1+2AP+CR	SAD2+2AP+CR		(3)
4	SAD1+3AP	SAD2+3AP		SAD1+3AP+1	SAD2+3AP+1			SAD1+3AP+CR	SAD2+3AP+CR		(4)
5	SAD1+4AP	SAD2+4AP		SAD1+4AP+1	SAD2+4AP+1		...	SAD1+4AP+CR	SAD2+4AP+CR		
6	SAD1+5AP	SAD2+5AP		SAD1+5AP+1	SAD2+5AP+1			SAD1+5AP+CR	SAD2+5AP+CR		
7	SAD1+6AP	SAD2+6AP		SAD1+6AP+1	SAD2+6AP+1		...	SAD1+6AP+CR	SAD2+6AP+CR		
8	SAD1+7AP	SAD2+7AP		SAD1+7AP+1	SAD2+7AP+1			SAD1+7AP+CR	SAD2+7AP+CR		
9	SAD1+8AP	SAD2+8AP		SAD1+8AP+1	SAD2+8AP+1		...	SAD1+8AP+CR	SAD2+8AP+CR		
10	SAD1+9AP	SAD2+9AP		SAD1+9AP+1	SAD2+9AP+1			SAD1+9AP+CR	SAD2+9AP+CR		
11	SAD1+10AP	SAD2+10AP		SAD1+10AP+1	SAD2+10AP+1		...	SAD1+10AP+CR	SAD2+10AP+CR		
12	SAD1+11AP	SAD2+11AP		SAD1+11AP+1	SAD2+11AP+1			SAD1+11AP+CR	SAD2+11AP+CR		
13	SAD1+12AP	SAD2+12AP		SAD1+12AP+1	SAD2+12AP+1		...	SAD1+12AP+CR	SAD2+12AP+CR		
14	SAD1+13AP	SAD2+13AP		SAD1+13AP+1	SAD2+13AP+1			SAD1+13AP+CR	SAD2+13AP+CR		
15	SAD1+14AP	SAD2+14AP		SAD1+14AP+1	SAD2+14AP+1		...	SAD1+14AP+CR	SAD2+14AP+CR		
16	SAD1+15AP	SAD2+15AP		SAD1+15AP+1	SAD2+15AP+1			SAD1+15AP+CR	SAD2+15AP+CR		
SL1-7	SAD1+(SL1-7)AP	SAD2+(SL1-7)AP		SAD1+(SL1-7)AP+1	SAD2+(SL1-7)AP+1		...	SAD1+(SL1-7)AP+CR	SAD2+(SL1-7)AP+CR		
SL1-6	SAD1+(SL1-6)AP	SAD2+(SL1-6)AP		SAD1+(SL1-6)AP+1	SAD2+(SL1-6)AP+1			SAD1+(SL1-6)AP+CR	SAD2+(SL1-6)AP+CR		
SL1-5	SAD1+(SL1-5)AP	SAD2+(SL1-5)AP		SAD1+(SL1-5)AP+1	SAD2+(SL1-5)AP+1		...	SAD1+(SL1-5)AP+CR	SAD2+(SL1-5)AP+CR		
SL1-4	SAD1+(SL1-4)AP	SAD2+(SL1-4)AP		SAD1+(SL1-4)AP+1	SAD2+(SL1-4)AP+1			SAD1+(SL1-4)AP+CR	SAD2+(SL1-4)AP+CR		
SL1-3	SAD1+(SL1-3)AP	SAD2+(SL1-3)AP		SAD1+(SL1-3)AP+1	SAD2+(SL1-3)AP+1		...	SAD1+(SL1-3)AP+CR	SAD2+(SL1-3)AP+CR		
SL1-2	SAD1+(SL1-2)AP	SAD2+(SL1-2)AP		SAD1+(SL1-2)AP+1	SAD2+(SL1-2)AP+1			SAD1+(SL1-2)AP+CR	SAD2+(SL1-2)AP+CR		
SL1-1	SAD1+(SL1-1)AP	SAD2+(SL1-1)AP		SAD1+(SL1-1)AP+1	SAD2+(SL1-1)AP+1		...	SAD1+(SL1-1)AP+CR	SAD2+(SL1-1)AP+CR		
SL1	SAD1+(SL1)AP	SAD2+(SL1)AP		SAD1+(SL1)AP+1	SAD2+(SL1)AP+1			SAD1+(SL1)AP+CR	SAD2+(SL1)AP+CR		
SL1+1	SAD3	SAD2+(SL1+1)AP		SAD3+1	SAD2+(SL1+1)AP+1		...	SAD3+CR	SAD2+(SL1+1)AP+CR		
SL1+2	SAD3+AP	SAD2+(SL1+2)AP		SAD3+AP+1	SAD2+(SL1+2)AP+1			SAD3+AP+CR	SAD2+(SL1+2)AP+CR		
SL1+3	SAD3+2AP	SAD2+(SL1+3)AP		SAD3+2AP+1	SAD2+(SL1+3)AP+1		...	SAD3+2AP+CR	SAD2+(SL1+3)AP+CR		
SL1+4	SAD3+3AP	SAD2+(SL1+4)AP		SAD3+3AP+1	SAD2+(SL1+4)AP+1			SAD3+3AP+CR	SAD2+(SL1+4)AP+CR		
SL1+5	SAD3+4AP	SAD2+(SL1+5)AP		SAD3+4AP+1	SAD2+(SL1+5)AP+1		...	SAD3+4AP+CR	SAD2+(SL1+5)AP+CR		
SL1+6	SAD3+5AP	SAD2+(SL1+6)AP		SAD3+5AP+1	SAD2+(SL1+6)AP+1			SAD3+5AP+CR	SAD2+(SL1+6)AP+CR		
SL1+7	SAD3+6AP	SAD2+(SL1+7)AP		SAD3+6AP+1	SAD2+(SL1+7)AP+1		...	SAD3+6AP+CR	SAD2+(SL1+7)AP+CR		
SL1+8	SAD3+7AP	SAD2+(SL1+8)AP		SAD3+7AP+1	SAD2+(SL1+8)AP+1			SAD3+7AP+CR	SAD2+(SL1+8)AP+CR		
SL1+9	SAD3+8AP	SAD2+(SL1+9)AP		SAD3+8AP+1	SAD2+(SL1+9)AP+1		...	SAD3+8AP+CR	SAD2+(SL1+9)AP+CR		
SL1+10	SAD3+9AP	SAD2+(SL1+10)AP		SAD3+9AP+1	SAD2+(SL1+10)AP+1			SAD3+9AP+CR	SAD2+(SL1+10)AP+CR		
SL1+11	SAD3+10AP	SAD2+(SL1+11)AP		SAD3+10AP+1	SAD2+(SL1+11)AP+1		...	SAD3+10AP+CR	SAD2+(SL1+11)AP+CR		
SL1+12	SAD3+11AP	SAD2+(SL1+12)AP		SAD3+11AP+1	SAD2+(SL1+12)AP+1			SAD3+11AP+CR	SAD2+(SL1+12)AP+CR		
SL1+13	SAD3+12AP	SAD2+(SL1+13)AP		SAD3+12AP+1	SAD2+(SL1+13)AP+1		...	SAD3+12AP+CR	SAD2+(SL1+13)AP+CR		
SL1+14	SAD3+13AP	SAD2+(SL1+14)AP		SAD3+13AP+1	SAD2+(SL1+14)AP+1			SAD3+13AP+CR	SAD2+(SL1+14)AP+CR		
SL1+15	SAD3+14AP	SAD2+(SL1+15)AP		SAD3+14AP+1	SAD2+(SL1+15)AP+1		...	SAD3+14AP+CR	SAD2+(SL1+15)AP+CR		
SL1+16	SAD3+15AP	SAD2+(SL1+16)AP		SAD3+15AP+1	SAD2+(SL1+16)AP+1			SAD3+15AP+CR	SAD2+(SL1+16)AP+CR		
LF-7	SAD3+(LF-SL1-7)AP	SAD2+(LF-7)AP		SAD3+(LF-SL1-7)AP+1	SAD2+(LF-7)AP+1		...	SAD3+(LF-SL1-7)AP+CR	SAD2+(LF-7)AP+CR		
LF-6	SAD3+(LF-SL1-6)AP	SAD2+(LF-6)AP		SAD3+(LF-SL1-6)AP+1	SAD2+(LF-6)AP+1			SAD3+(LF-SL1-6)AP+CR	SAD2+(LF-6)AP+CR		
LF-5	SAD3+(LF-SL1-5)AP	SAD2+(LF-5)AP		SAD3+(LF-SL1-5)AP+1	SAD2+(LF-5)AP+1		...	SAD3+(LF-SL1-5)AP+CR	SAD2+(LF-5)AP+CR		(LF-5)
LF-4	SAD3+(LF-SL1-4)AP	SAD2+(LF-4)AP		SAD3+(LF-SL1-4)AP+1	SAD2+(LF-4)AP+1			SAD3+(LF-SL1-4)AP+CR	SAD2+(LF-4)AP+CR		(LF-4)
LF-3	SAD3+(LF-SL1-3)AP	SAD2+(LF-3)AP		SAD3+(LF-SL1-3)AP+1	SAD2+(LF-3)AP+1		...	SAD3+(LF-SL1-3)AP+CR	SAD2+(LF-3)AP+CR		(LF-3)
LF-2	SAD3+(LF-SL1-2)AP	SAD2+(LF-2)AP		SAD3+(LF-SL1-2)AP+1	SAD2+(LF-2)AP+1			SAD3+(LF-SL1-2)AP+CR	SAD2+(LF-2)AP+CR		(LF-2)
LF-1	SAD3+(LF-SL1-1)AP	SAD2+(LF-1)AP		SAD3+(LF-SL1-1)AP+1	SAD2+(LF-1)AP+1		...	SAD3+(LF-SL1-1)AP+CR	SAD2+(LF-1)AP+CR		(LF-1)
LF	SAD3+(LF-SL1)AP	SAD2+(LF)AP		SAD3+(LF-SL1)AP+1	SAD2+(LF)AP+1			SAD3+(LF-SL1)AP+CR	SAD2+(LF)AP+CR		(LF)

VA0-15(case3)

<< (W/S, OV, DM2, DM1, FY) = (0, 1, 1, 1, 8) >> **(BK1, BK2, BK3, BK4) = Graphic (Layer1), Graphic (Layer2), Graphic (Layer3), -)**

											*ReadTurn
LineNo 1	SAD1	SAD2	SAD3	SAD1+1	SAD2+1	SAD3+1	…	SAD1+CR	SAD2+CR	SAD3+CR	(1)
2	SAD1+AP	SAD2+AP	SAD3+AP	SAD1+AP+1	SAD2+AP+1	SAD3+AP+1		SAD1+AP+CR	SAD2+AP+CR	SAD3+AP+CR	(2)
3	SAD1+2AP	SAD2+2AP	SAD3+2AP	SAD1+2AP+1	SAD2+2AP+1	SAD3+2AP+1	…	SAD1+2AP+CR	SAD2+2AP+CR	SAD3+2AP+CR	(3)
4	SAD1+3AP	SAD2+3AP	SAD3+3AP	SAD1+3AP+1	SAD2+3AP+1	SAD3+3AP+1		SAD1+3AP+CR	SAD2+3AP+CR	SAD3+3AP+CR	(4)
5	SAD1+4AP	SAD2+4AP	SAD3+4AP	SAD1+4AP+1	SAD2+4AP+1	SAD3+4AP+1	…	SAD1+4AP+CR	SAD2+4AP+CR	SAD3+4AP+CR	
6	SAD1+5AP	SAD2+5AP	SAD3+5AP	SAD1+5AP+1	SAD2+5AP+1	SAD3+5AP+1		SAD1+5AP+CR	SAD2+5AP+CR	SAD3+5AP+CR	
7	SAD1+6AP	SAD2+6AP	SAD3+6AP	SAD1+6AP+1	SAD2+6AP+1	SAD3+6AP+1	…	SAD1+6AP+CR	SAD2+6AP+CR	SAD3+6AP+CR	
8	SAD1+7AP	SAD2+7AP	SAD3+7AP	SAD1+7AP+1	SAD2+7AP+1	SAD3+7AP+1		SAD1+7AP+CR	SAD2+7AP+CR	SAD3+7AP+CR	
9	SAD1+8AP	SAD2+8AP	SAD3+8AP	SAD1+8AP+1	SAD2+8AP+1	SAD3+8AP+1	…	SAD1+8AP+CR	SAD2+8AP+CR	SAD3+8AP+CR	
10	SAD1+9AP	SAD2+9AP	SAD3+9AP	SAD1+9AP+1	SAD2+9AP+1	SAD3+9AP+1		SAD1+9AP+CR	SAD2+9AP+CR	SAD3+9AP+CR	
11	SAD1+10AP	SAD2+10AP	SAD3+10AP	SAD1+10AP+1	SAD2+10AP+1	SAD3+10AP+1	…	SAD1+10AP+CR	SAD2+10AP+CR	SAD3+10AP+CR	
12	SAD1+11AP	SAD2+11AP	SAD3+11AP	SAD1+11AP+1	SAD2+11AP+1	SAD3+11AP+1		SAD1+11AP+CR	SAD2+11AP+CR	SAD3+11AP+CR	
13	SAD1+12AP	SAD2+12AP	SAD3+12AP	SAD1+12AP+1	SAD2+12AP+1	SAD3+12AP+1	…	SAD1+12AP+CR	SAD2+12AP+CR	SAD3+12AP+CR	
14	SAD1+13AP	SAD2+13AP	SAD3+13AP	SAD1+13AP+1	SAD2+13AP+1	SAD3+13AP+1		SAD1+13AP+CR	SAD2+13AP+CR	SAD3+13AP+CR	
15	SAD1+14AP	SAD2+14AP	SAD3+14AP	SAD1+14AP+1	SAD2+14AP+1	SAD3+14AP+1	…	SAD1+14AP+CR	SAD2+14AP+CR	SAD3+14AP+CR	
16	SAD1+15AP	SAD2+15AP	SAD3+15AP	SAD1+15AP+1	SAD2+15AP+1	SAD3+15AP+1		SAD1+15AP+CR	SAD2+15AP+CR	SAD3+15AP+CR	
17	SAD1+16AP	SAD2+16AP	SAD3+16AP	SAD1+16AP+1	SAD2+16AP+1	SAD3+16AP+1	…	SAD1+16AP+CR	SAD2+16AP+CR	SAD3+16AP+CR	
18	SAD1+17AP	SAD2+17AP	SAD3+17AP	SAD1+17AP+1	SAD2+17AP+1	SAD3+17AP+1		SAD1+17AP+CR	SAD2+17AP+CR	SAD3+17AP+CR	
19	SAD1+18AP	SAD2+18AP	SAD3+18AP	SAD1+18AP+1	SAD2+18AP+1	SAD3+18AP+1	…	SAD1+18AP+CR	SAD2+18AP+CR	SAD3+18AP+CR	
20	SAD1+19AP	SAD2+19AP	SAD3+19AP	SAD1+19AP+1	SAD2+19AP+1	SAD3+19AP+1		SAD1+19AP+CR	SAD2+19AP+CR	SAD3+19AP+CR	
21	SAD1+20AP	SAD2+20AP	SAD3+20AP	SAD1+20AP+1	SAD2+20AP+1	SAD3+20AP+1	…	SAD1+20AP+CR	SAD2+20AP+CR	SAD3+20AP+CR	
22	SAD1+21AP	SAD2+21AP	SAD3+21AP	SAD1+21AP+1	SAD2+21AP+1	SAD3+21AP+1		SAD1+21AP+CR	SAD2+21AP+CR	SAD3+21AP+CR	
23	SAD1+22AP	SAD2+22AP	SAD3+22AP	SAD1+22AP+1	SAD2+22AP+1	SAD3+22AP+1	…	SAD1+22AP+CR	SAD2+22AP+CR	SAD3+22AP+CR	
24	SAD1+23AP	SAD2+23AP	SAD3+23AP	SAD1+23AP+1	SAD2+23AP+1	SAD3+23AP+1		SAD1+23AP+CR	SAD2+23AP+CR	SAD3+23AP+CR	
LF-15	SAD1+(LF-15)AP	SAD2+(LF-15)AP	SAD3+(LF-15)AP	SAD1+(LF-15)AP+1	SAD2+(LF-15)AP+1	SAD3+(LF-15)AP+1	…	SAD1+(LF-15)AP+CR	SAD2+(LF-15)AP+CR	SAD3+(LF-15)AP+CR	
LF-14	SAD1+(LF-14)AP	SAD2+(LF-14)AP	SAD3+(LF-14)AP	SAD1+(LF-14)AP+1	SAD2+(LF-14)AP+1	SAD3+(LF-14)AP+1		SAD1+(LF-14)AP+CR	SAD2+(LF-14)AP+CR	SAD3+(LF-14)AP+CR	
LF-13	SAD1+(LF-13)AP	SAD2+(LF-13)AP	SAD3+(LF-13)AP	SAD1+(LF-13)AP+1	SAD2+(LF-13)AP+1	SAD3+(LF-13)AP+1	…	SAD1+(LF-13)AP+CR	SAD2+(LF-13)AP+CR	SAD3+(LF-13)AP+CR	
LF-12	SAD1+(LF-12)AP	SAD2+(LF-12)AP	SAD3+(LF-12)AP	SAD1+(LF-12)AP+1	SAD2+(LF-12)AP+1	SAD3+(LF-12)AP+1		SAD1+(LF-12)AP+CR	SAD2+(LF-12)AP+CR	SAD3+(LF-12)AP+CR	
LF-11	SAD1+(LF-11)AP	SAD2+(LF-11)AP	SAD3+(LF-11)AP	SAD1+(LF-11)AP+1	SAD2+(LF-11)AP+1	SAD3+(LF-11)AP+1	…	SAD1+(LF-11)AP+CR	SAD2+(LF-11)AP+CR	SAD3+(LF-11)AP+CR	
LF-10	SAD1+(LF-10)AP	SAD2+(LF-10)AP	SAD3+(LF-10)AP	SAD1+(LF-10)AP+1	SAD2+(LF-10)AP+1	SAD3+(LF-10)AP+1		SAD1+(LF-10)AP+CR	SAD2+(LF-10)AP+CR	SAD3+(LF-10)AP+CR	
LF-9	SAD1+(LF-9)AP	SAD2+(LF-9)AP	SAD3+(LF-9)AP	SAD1+(LF-9)AP+1	SAD2+(LF-9)AP+1	SAD3+(LF-9)AP+1	…	SAD1+(LF-9)AP+CR	SAD2+(LF-9)AP+CR	SAD3+(LF-9)AP+CR	
LF-8	SAD1+(LF-8)AP	SAD2+(LF-8)AP	SAD3+(LF-8)AP	SAD1+(LF-8)AP+1	SAD2+(LF-8)AP+1	SAD3+(LF-8)AP+1		SAD1+(LF-8)AP+CR	SAD2+(LF-8)AP+CR	SAD3+(LF-8)AP+CR	
LF-7	SAD1+(LF-7)AP	SAD2+(LF-7)AP	SAD3+(LF-7)AP	SAD1+(LF-7)AP+1	SAD2+(LF-7)AP+1	SAD3+(LF-7)AP+1	…	SAD1+(LF-7)AP+CR	SAD2+(LF-7)AP+CR	SAD3+(LF-7)AP+CR	
LF-6	SAD1+(LF-6)AP	SAD2+(LF-6)AP	SAD3+(LF-6)AP	SAD1+(LF-6)AP+1	SAD2+(LF-6)AP+1	SAD3+(LF-6)AP+1		SAD1+(LF-6)AP+CR	SAD2+(LF-6)AP+CR	SAD3+(LF-6)AP+CR	
LF-5	SAD1+(LF-5)AP	SAD2+(LF-5)AP	SAD3+(LF-5)AP	SAD1+(LF-5)AP+1	SAD2+(LF-5)AP+1	SAD3+(LF-5)AP+1	…	SAD1+(LF-5)AP+CR	SAD2+(LF-5)AP+CR	SAD3+(LF-5)AP+CR	(LF-5)
LF-4	SAD1+(LF-4)AP	SAD2+(LF-4)AP	SAD3+(LF-4)AP	SAD1+(LF-4)AP+1	SAD2+(LF-4)AP+1	SAD3+(LF-4)AP+1		SAD1+(LF-4)AP+CR	SAD2+(LF-4)AP+CR	SAD3+(LF-4)AP+CR	(LF-4)
LF-3	SAD1+(LF-3)AP	SAD2+(LF-3)AP	SAD3+(LF-3)AP	SAD1+(LF-3)AP+1	SAD2+(LF-3)AP+1	SAD3+(LF-3)AP+1	…	SAD1+(LF-3)AP+CR	SAD2+(LF-3)AP+CR	SAD3+(LF-3)AP+CR	(LF-3)
LF-2	SAD1+(LF-2)AP	SAD2+(LF-2)AP	SAD3+(LF-2)AP	SAD1+(LF-2)AP+1	SAD2+(LF-2)AP+1	SAD3+(LF-2)AP+1		SAD1+(LF-2)AP+CR	SAD2+(LF-2)AP+CR	SAD3+(LF-2)AP+CR	(LF-2)
LF-1	SAD1+(LF-1)AP	SAD2+(LF-1)AP	SAD3+(LF-1)AP	SAD1+(LF-1)AP+1	SAD2+(LF-1)AP+1	SAD3+(LF-1)AP+1	…	SAD1+(LF-1)AP+CR	SAD2+(LF-1)AP+CR	SAD3+(LF-1)AP+CR	(LF-1)
LF	SAD+(LF)AP	SAD2+(LF)AP	SAD3+(LF)AP	SAD+(LF)AP+1	SAD2+(LF)AP+1	SAD3+(LF)AP+1		SAD+(LF)AP+CR	SAD2+(LF)AP+CR	SAD3+(LF)AP+CR	(LF)

VA0-15(case4)

<< (W/S, OV, DM2, DM1, FY) = (1, 0, 0, 0, 8) >> **(BK1, BK2, BK3, BK4) = (Character (Layer1), Graphic (Layer2), Character (Layer1), Graphic (Layer2))**

LineNo										*ReadTurn
1	SAD1	SAD2	CG1	SAD1+1	SAD2+1	CG1	…	SAD1+CR	SAD2+CR	CG1	(1)
2		SAD2+AP			SAD2+AP+1				SAD2+AP+CR		(3)
3		SAD2+2AP			SAD2+2AP+1		…		SAD2+2AP+CR		(5)
4		SAD2+3AP			SAD2+3AP+1				SAD2+3AP+CR		(7)
5		SAD2+4AP			SAD2+4AP+1		…		SAD2+4AP+CR		
6		SAD2+5AP			SAD2+5AP+1				SAD2+5AP+CR		
7		SAD2+6AP			SAD2+6AP+1		…		SAD2+6AP+CR		
8		SAD2+7AP			SAD2+7AP+1				SAD2+7AP+CR		
9	SAD1+AP	SAD2+8AP	CG1	SAD1+AP+1	SAD2+8AP+1	CG 1	…	SAD1+AP+CR	SAD2+8AP+CR	CG1	
10		SAD2+9AP			SAD2+9AP+1				SAD2+9AP+CR		
11		SAD2+10AP			SAD2+10AP+1		…		SAD2+10AP+CR		
12		SAD2+11AP			SAD2+11AP+1				SAD2+11AP+CR		
13		SAD2+12AP			SAD2+12AP+1		…		SAD2+12AP+CR		
14		SAD2+13AP			SAD2+13AP+1				SAD2+13AP+CR		
15		SAD2+14AP			SAD2+14AP+1		…		SAD2+14AP+CR		
16		SAD2+15AP			SAD2+15AP+1				SAD2+15AP+CR		
SL1-7	SAD1+(SL1/8)AP	SAD2+(SL1-7)AP	CG1	SAD1+(SL1/8)AP+1	SAD2+(SL1-7)AP+1	CG1	…	SAD1+(SL1/8)AP+CR	SAD2+(SL1-7)AP+CR	CG 1	
SL1-6		SAD2+(SL1-6)AP			SAD2+(SL1-6)AP+1				SAD2+(SL1-6)AP+CR		
SL1-5		SAD2+(SL1-5)AP			SAD2+(SL1-5)AP+1		…		SAD2+(SL1-5)AP+CR		
SL1-4		SAD2+(SL1-4)AP			SAD2+(SL1-4)AP+1				SAD2+(SL1-4)AP+CR		
SL1-3		SAD2+(SL1-3)AP			SAD2+(SL1-3)AP+1		…		SAD2+(SL1-3)AP+CR		
SL1-2		SAD2+(SL1-2)AP			SAD2+(SL1-2)AP+1				SAD2+(SL1-2)AP+CR		(LF-5)
SL1-1		SAD2+(SL1-1)AP			SAD2+(SL1-1)AP+1		…		SAD2+(SL1-1)AP+CR		(LF-3)
SL1		SAD2+(SL1)AP			SAD2+(SL1)AP+1				SAD2+(SL1)AP+CR		(LF-1)
SL1+1	SAD3	SAD4	CG3	SAD3+1	SAD4+1	CG3	…	SAD3+CR	SAD4+CR	CG3	(2)
SL1+2		SAD4+AP			SAD4+AP+1				SAD4+AP+CR		(4)
SL1+3		SAD4+2AP			SAD4+2AP+1		…		SAD4+2AP+CR		(6)
SL1+4		SAD4+3AP			SAD4+3AP+1				SAD4+3AP+CR		(8)
SL1+5		SAD4+4AP			SAD4+4AP+1		…		SAD4+4AP+CR		
SL1+6		SAD4+5AP			SAD4+5AP+1				SAD4+5AP+CR		
SL1+7		SAD4+6AP			SAD4+6AP+1		…		SAD4+6AP+CR		
SL1+8		SAD4+7AP			SAD4+7AP+1				SAD4+7AP+CR		
SL1+9	SAD3+AP	SAD4+8AP	CG3	SAD3+AP+1	SAD4+8AP+1	CG3	…	SAD3+AP+CR	SAD4+8AP+CR	CG3	
SL1+10		SAD4+9AP			SAD4+9AP+1				SAD4+9AP+CR		
SL1+11		SAD4+10AP			SAD4+10AP+1		…		SAD4+10AP+CR		
SL1+12		SAD4+11AP			SAD4+11AP+1				SAD4+11AP+CR		
SL1+13		SAD4+12AP			SAD4+12AP+1		…		SAD4+12AP+CR		
SL1+14		SAD4+13AP			SAD4+13AP+1				SAD4+13AP+CR		
SL1+15		SAD4+14AP			SAD4+14AP+1		…		SAD4+14AP+CR		
SL1+16		SAD4+15AP			SAD4+15AP+1				SAD4+15AP+CR		
LF-7	SAD3+(LD/8)AP	SAD4+(LF-SL2-7)AP	CG3	SAD3+(LF/8)+1	SAD4+(LF-SL2-7)AP+1	CG3	…	SAD3+(LF/8)+CR	SAD4+(LF-SL2-7)AP+CR	CG3	
LF-6		SAD4+(LF-SL2-6)AP			SAD4+(LF-SL2-6)AP+1				SAD4+(LF-SL2-6)AP+CR		
LF-5		SAD4+(LF-SL2-5)AP			SAD4+(LF-SL2-5)AP+1		…		SAD4+(LF-SL2-5)AP+CR		
LF-4		SAD4+(LF-SL2-4)AP			SAD4+(LF-SL2-4)AP+1				SAD4+(LF-SL2-4)AP+CR		
LF-3		SAD4+(LF-SL2-3)AP			SAD4+(LF-SL2-3)AP+1		…		SAD4+(LF-SL2-3)AP+CR		
LF-2		SAD4+(LF-SL2-2)AP			SAD4+(LF-SL2-2)AP+1				SAD4+(LF-SL2-2)AP+CR		(LF-4)
LF-1		SAD4+(LF-SL2-1)AP			SAD4+(LF-SL2-1)AP+1		…		SAD4+(LF-SL2-1)AP+CR		(LF-2)
LF		SAD4+(LF-SL2)AP			SAD4+(LF-SL2)AP+1				SAD4+(LF-SL2)AP+CR		(LF)

<< (W/S, OV, DM2, DM1, FY) = (1, 0, 0, 0, 8) >> (BK1, BK2, BK3, BK4) = (Character (Layer1), Graphic (Layer2), Character (Layer1), Graphic (Layer2))

											*ReadTurn
LineNo 1	SAD1	SAD2		SAD1+1	SAD2+1		...	SAD1+CR	SAD2+CR		(1)
2	SAD1+AP	SAD2+AP		SAD1+AP+1	SAD2+AP+1			SAD1+AP+CR	SAD2+AP+CR		(3)
3	SAD1+2AP	SAD2+2AP		SAD1+2AP+1	SAD2+2AP+1		...	SAD1+2AP+CR	SAD2+2AP+CR		(5)
4	SAD1+3AP	SAD2+3AP		SAD1+3AP+1	SAD2+3AP+1			SAD1+3AP+CR	SAD2+3AP+CR		(7)
5	SAD1+4AP	SAD2+4AP		SAD1+4AP+1	SAD2+4AP+1		...	SAD1+4AP+CR	SAD2+4AP+CR		
6	SAD1+5AP	SAD2+5AP		SAD1+5AP+1	SAD2+5AP+1			SAD1+5AP+CR	SAD2+5AP+CR		
7	SAD1+6AP	SAD2+6AP		SAD1+6AP+1	SAD2+6AP+1		...	SAD1+6AP+CR	SAD2+6AP+CR		
8	SAD1+7AP	SAD2+7AP		SAD1+7AP+1	SAD2+7AP+1			SAD1+7AP+CR	SAD2+7AP+CR		
9	SAD1+8AP	SAD2+8AP		SAD1+8AP+1	SAD2+8AP+1		...	SAD1+8AP+CR	SAD2+8AP+CR		
10	SAD1+9AP	SAD2+9AP		SAD1+9AP+1	SAD2+9AP+1			SAD1+9AP+CR	SAD2+9AP+CR		
11	SAD1+10AP	SAD2+10AP		SAD1+10AP+1	SAD2+10AP+1		...	SAD1+10AP+CR	SAD2+10AP+CR		
12	SAD1+11AP	SAD2+11AP		SAD1+11AP+1	SAD2+11AP+1			SAD1+11AP+CR	SAD2+11AP+CR		
13	SAD1+12AP	SAD2+12AP		SAD1+12AP+1	SAD2+12AP+1		...	SAD1+12AP+CR	SAD2+12AP+CR		
14	SAD1+13AP	SAD2+13AP		SAD1+13AP+1	SAD2+13AP+1			SAD1+13AP+CR	SAD2+13AP+CR		
15	SAD1+14AP	SAD2+14AP		SAD1+14AP+1	SAD2+14AP+1		...	SAD1+14AP+CR	SAD2+14AP+CR		
16	SAD1+15AP	SAD2+15AP		SAD1+15AP+1	SAD2+15AP+1			SAD1+15AP+CR	SAD2+15AP+CR		
SL1-7	SAD1+(SL1-7)AP	SAD2+(SL1-7)AP		SAD1+(SL1-7)AP+1	SAD2+(SL1-7)AP+1		...	SAD1+(SL1-7)AP+CR	SAD2+(SL1-7)AP+CR		
SL1-6	SAD1+(SL1-6)AP	SAD2+(SL1-6)AP		SAD1+(SL1-6)AP+1	SAD2+(SL1-6)AP+1			SAD1+(SL1-6)AP+CR	SAD2+(SL1-6)AP+CR		
SL1-5	SAD1+(SL1-5)AP	SAD2+(SL1-5)AP		SAD1+(SL1-5)AP+1	SAD2+(SL1-5)AP+1		...	SAD1+(SL1-5)AP+CR	SAD2+(SL1-5)AP+CR		
SL1-4	SAD1+(SL1-4)AP	SAD2+(SL1-4)AP		SAD1+(SL1-4)AP+1	SAD2+(SL1-4)AP+1			SAD1+(SL1-4)AP+CR	SAD2+(SL1-4)AP+CR		
SL1-3	SAD1+(SL1-3)AP	SAD2+(SL1-3)AP		SAD1+(SL1-3)AP+1	SAD2+(SL1-3)AP+1		...	SAD1+(SL1-3)AP+CR	SAD2+(SL1-3)AP+CR		
SL1-2	SAD1+(SL1-2)AP	SAD2+(SL1-2)AP		SAD1+(SL1-2)AP+1	SAD2+(SL1-2)AP+1			SAD1+(SL1-2)AP+CR	SAD2+(SL1-2)AP+CR		(LF-5)
SL1-1	SAD1+(SL1-1)AP	SAD2+(SL1-1)AP		SAD1+(SL1-1)AP+1	SAD2+(SL1-1)AP+1		...	SAD1+(SL1-1)AP+CR	SAD2+(SL1-1)AP+CR		(LF-3)
SL1	SAD1+(SL1)AP	SAD2+(SL1)AP		SAD1+(SL1)AP+1	SAD2+(SL1)AP+1			SAD1+(SL1)AP+CR	SAD2+(SL1)AP+CR		(LF-1)
SL1+1	SAD3	SAD4	CG3	SAD3+1	SAD4+1	CG3	...	SAD3+CR	SAD4+CR	CG3	(2)
SL1+2		SAD4+AP			SAD4+AP+1				SAD4+AP+CR		(4)
SL1+3		SAD4+2AP			SAD4+2AP+1		...		SAD4+2AP+CR		(6)
SL1+4		SAD4+3AP			SAD4+3AP+1				SAD4+3AP+CR		(8)
SL1+5		SAD4+4AP			SAD4+4AP+1		...		SAD4+4AP+CR		
SL1+6		SAD4+5AP			SAD4+5AP+1				SAD4+5AP+CR		
SL1+7		SAD4+6AP			SAD4+6AP+1		...		SAD4+6AP+CR		
SL1+8		SAD4+7AP			SAD4+7AP+1				SAD4+7AP+CR		
SL1+9	SAD3+AP	SAD4+8AP	CG3	SAD3+AP+1	SAD4+8AP+1	CG3	...	SAD3+AP+CR	SAD4+8AP+CR	CG3	
SL1+10		SAD4+9AP			SAD4+9AP+1				SAD4+9AP+CR		
SL1+11		SAD4+10AP			SAD4+10AP+1		...		SAD4+10AP+CR		
SL1+12		SAD4+11AP			SAD4+11AP+1				SAD4+11AP+CR		
SL1+13		SAD4+12AP			SAD4+12AP+1		...		SAD4+12AP+CR		
SL1+14		SAD4+13AP			SAD4+13AP+1				SAD4+13AP+CR		
SL1+15		SAD4+14AP			SAD4+14AP+1		...		SAD4+14AP+CR		
SL1+16		SAD4+15AP			SAD4+15AP+1				SAD4+15AP+CR		
LF-7	SAD3+(LD/8)AP	SAD4+(LF-SL2-7)AP	CG3	SAD3+(LF/8)+1	SAD4+(LF-SL2-7)AP+1	CG3	...	SAD3+(LF/8)+CR	SAD4+(LF-SL2-7)AP+CR	CG3	
LF-6		SAD4+(LF-SL2-6)AP			SAD4+(LF-SL2-6)AP+1				SAD4+(LF-SL2-6)AP+CR		
LF-5		SAD4+(LF-SL2-5)AP			SAD4+(LF-SL2-5)AP+1		...		SAD4+(LF-SL2-5)AP+CR		
LF-4		SAD4+(LF-SL2-4)AP			SAD4+(LF-SL2-4)AP+1				SAD4+(LF-SL2-4)AP+CR		
LF-3		SAD4+(LF-SL2-3)AP			SAD4+(LF-SL2-3)AP+1		...		SAD4+(LF-SL2-3)AP+CR		
LF-2		SAD4+(LF-SL2-2)AP			SAD4+(LF-SL2-2)AP+1				SAD4+(LF-SL2-2)AP+CR		(LF-4)
LF-1		SAD4+(LF-SL2-1)AP			SAD4+(LF-SL2-1)AP+1		...		SAD4+(LF-SL2-1)AP+CR		(LF-2)
LF		SAD4+(LF-SL2)AP			SAD4+(LF-SL2)AP+1				SAD4+(LF-SL2)AP+CR		(LF)

<< (W/S, OV, DM2, DM1, FY) = (1, 0, 0, 0, 8) >>

(BK1, BK2, BK3, BK4) = (Character (Layer1), Graphic (Layer2), Character (Layer1), Graphic (Layer2))

LineNo1										*ReadTurn
	SAD1	SAD2	CG1	SAD1+1	SAD2+1	CG1	...	SAD1+CR	SAD2+CR	CG1	(1)
2		SAD2+AP			SAD2+AP+1				SAD2+AP+CR		(3)
3		SAD2+2AP			SAD2+2AP+1		...		SAD2+2AP+CR		(5)
4		SAD2+3AP			SAD2+3AP+1				SAD2+3AP+CR		(7)
5		SAD2+4AP			SAD2+4AP+1		...		SAD2+4AP+CR		
6		SAD2+5AP			SAD2+5AP+1				SAD2+5AP+CR		
7		SAD2+6AP			SAD2+6AP+1		...		SAD2+6AP+CR		
8		SAD2+7AP			SAD2+7AP+1				SAD2+7AP+CR		
9	SAD1+AP	SAD2+8AP	CG1	SAD1+AP+1	SAD2+8AP+1	CG1	...	SAD1+AP+CR	SAD2+8AP+CR	CG1	
10		SAD2+9AP			SAD2+9AP+1				SAD2+9AP+CR		
11		SAD2+10AP			SAD2+10AP+1		...		SAD2+10AP+CR		
12		SAD2+11AP			SAD2+11AP+1				SAD2+11AP+CR		
13		SAD2+12AP			SAD2+12AP+1		...		SAD2+12AP+CR		
14		SAD2+13AP			SAD2+13AP+1				SAD2+13AP+CR		
15		SAD2+14AP			SAD2+14AP+1		...		SAD2+14AP+CR		
16		SAD2+15AP			SAD2+15AP+1				SAD2+15AP+CR		
SL1-7	SAD1+(SL1/8)AP	SAD2+(SL1-7)AP	CG1	SAD1+(SL1/8)AP+1	SAD2+(SL1-7)AP+1	CG1	...	SAD1+(SL1/8)AP+CR	SAD2+(SL1-7)AP+CR	CG1	
SL1-6		SAD2+(SL1-6)AP			SAD2+(SL1-6)AP+1				SAD2+(SL1-6)AP+CR		
SL1-5		SAD2+(SL1-5)AP			SAD2+(SL1-5)AP+1		...		SAD2+(SL1-5)AP+CR		
SL1-4		SAD2+(SL1-4)AP			SAD2+(SL1-4)AP+1				SAD2+(SL1-4)AP+CR		
SL1-3		SAD2+(SL1-3)AP			SAD2+(SL1-3)AP+1		...		SAD2+(SL1-3)AP+CR		
SL1-2		SAD2+(SL1-2)AP			SAD2+(SL1-2)AP+1				SAD2+(SL1-2)AP+CR		(LF-5)
SL1-1		SAD2+(SL1-1)AP			SAD2+(SL1-1)AP+1		...		SAD2+(SL1-1)AP+CR		(LF-3)
SL1		SAD2+(SL1)AP			SAD2+(SL1)AP+1				SAD2+(SL1)AP+CR		(LF-1)
SL1+1	SAD3	SAD4		SAD1+1	SAD4+1		...	SAD3+CR	SAD4+CR		(2)
SL1+2	SAD3+AP	SAD4+AP		SAD3+AP+1	SAD4+AP+1			SAD3+AP+CR	SAD4+AP+CR		(4)
SL1+3	SAD3+2AP	SAD4+2AP		SAD3+2AP+1	SAD4+2AP+1		...	SAD3+2AP+CR	SAD4+2AP+CR		(6)
SL1+4	SAD3+3AP	SAD4+3AP		SAD3+3AP+1	SAD4+3AP+1			SAD3+3AP+CR	SAD4+3AP+CR		(8)
SL1+5	SAD3+4AP	SAD4+4AP		SAD3+4AP+1	SAD4+4AP+1		...	SAD3+4AP+CR	SAD4+4AP+CR		
SL1+6	SAD3+5AP	SAD4+5AP		SAD3+5AP+1	SAD4+5AP+1			SAD3+5AP+CR	SAD4+5AP+CR		
SL1+7	SAD3+6AP	SAD4+6AP		SAD3+6AP+1	SAD4+6AP+1		...	SAD3+6AP+CR	SAD4+6AP+CR		
SL1+8	SAD3+7AP	SAD4+7AP		SAD3+7AP+1	SAD4+7AP+1			SAD3+7AP+CR	SAD4+7AP+CR		
SL1+9	SAD3+8AP	SAD4+8AP		SAD3+8AP+1	SAD4+8AP+1		...	SAD3+8AP+CR	SAD4+8AP+CR		
SL1+10	SAD3+9AP	SAD4+9AP		SAD3+9AP+1	SAD4+9AP+1			SAD3+9AP+CR	SAD4+9AP+CR		
SL1+11	SAD3+10AP	SAD4+10AP		SAD3+10AP+1	SAD4+10AP+1		...	SAD3+10AP+CR	SAD4+10AP+CR		
SL1+12	SAD3+11AP	SAD4+11AP		SAD3+11AP+1	SAD4+11AP+1			SAD3+11AP+CR	SAD4+11AP+CR		
SL1+13	SAD3+12AP	SAD4+12AP		SAD3+12AP+1	SAD4+12AP+1		...	SAD3+12AP+CR	SAD4+12AP+CR		
SL1+14	SAD3+13AP	SAD4+13AP		SAD3+13AP+1	SAD4+13AP+1			SAD3+13AP+CR	SAD4+13AP+CR		
SL1+15	SAD3+14AP	SAD4+14AP		SAD3+14AP+1	SAD4+14AP+1		...	SAD3+14AP+CR	SAD4+14AP+CR		
SL1+16	SAD3+15AP	SAD4+15AP		SAD3+15AP+1	SAD4+15AP+1			SAD3+15AP+CR	SAD4+15AP+CR		
LF-7	SAD3+(LF-SL1-7)AP	SAD4+(LF-SL2-7)AP		SAD3+(LF-SL1-7)AP+1	SAD4+(LF-SL2-7)AP+1		...	SAD3+(LF-SL1-7)AP+CR	SAD4+(LF-SL2-7)AP+CR		
LF-6	SAD3+(LF-SL1-6)AP	SAD4+(LF-SL2-6)AP		SAD3+(LF-SL1-6)AP+1	SAD4+(LF-SL2-6)AP+1			SAD3+(LF-SL1-6)AP+CR	SAD4+(LF-SL2-6)AP+CR		
LF-5	SAD3+(LF-SL1-5)AP	SAD4+(LF-SL2-5)AP		SAD3+(LF-SL1-5)AP+1	SAD4+(LF-SL2-5)AP+1		...	SAD3+(LF-SL1-5)AP+CR	SAD4+(LF-SL2-5)AP+CR		
LF-4	SAD3+(LF-SL1-4)AP	SAD4+(LF-SL2-4)AP		SAD3+(LF-SL1-4)AP+1	SAD4+(LF-SL2-4)AP+1			SAD3+(LF-SL1-4)AP+CR	SAD4+(LF-SL2-4)AP+CR		
LF-3	SAD3+(LF-SL1-3)AP	SAD4+(LF-SL2-3)AP		SAD3+(LF-SL1-3)AP+1	SAD4+(LF-SL2-3)AP+1		...	SAD3+(LF-SL1-3)AP+CR	SAD4+(LF-SL2-3)AP+CR		
LF-2	SAD3+(LF-SL1-2)AP	SAD4+(LF-SL2-2)AP		SAD3+(LF-SL1-2)AP+1	SAD4+(LF-SL2-2)AP+1			SAD3+(LF-SL1-2)AP+CR	SAD4+(LF-SL2-2)AP+CR		(LF-4)
LF-1	SAD3+(LF-SL1-1)AP	SAD4+(LF-SL2-1)AP		SAD3+(LF-SL1-1)AP+1	SAD4+(LF-SL2-1)AP+1		...	SAD3+(LF-SL1-1)AP+CR	SAD4+(LF-SL2-1)AP+CR		(LF-2)
LF	SAD3+(LF-SL1)AP	SAD4+(LF-SL2)AP		SAD3+(LF-SL1)AP+1	SAD4+(LF-SL2)AP+1			SAD3+(LF-SL1)AP+CR	SAD4+(LF-SL2)AP+CR		(LF)

VA0-15(case5)

<< (W/S, OV, DM2, DM1, FY) = (1, 0, 1, 1, 8) >> **(BK1, BK2, BK3, BK4) = (Graphic (Layer1), Graphic (Layer2), Graphic (Layer1), Graphic (Layer2))**

LineNo1	SAD1	SAD2	SAD1+1	SAD2+1	...	SAD1+CR	SAD2+CR	*ReadTurn (1)
2	SAD1+AP	SAD2+AP	SAD1+AP+1	SAD2+AP+1		SAD1+AP+CR	SAD2+AP+CR	(3)
3	SAD1+2AP	SAD2+2AP	SAD1+2AP+1	SAD2+2AP+1	...	SAD1+2AP+CR	SAD2+2AP+CR	(5)
4	SAD1+3AP	SAD2+3AP	SAD1+3AP+1	SAD2+3AP+1		SAD1+3AP+CR	SAD2+3AP+CR	(7)
5	SAD1+4AP	SAD2+4AP	SAD1+4AP+1	SAD2+4AP+1	...	SAD1+4AP+CR	SAD2+4AP+CR	
6	SAD1+5AP	SAD2+5AP	SAD1+5AP+1	SAD2+5AP+1		SAD1+5AP+CR	SAD2+5AP+CR	
7	SAD1+6AP	SAD2+6AP	SAD1+6AP+1	SAD2+6AP+1	...	SAD1+6AP+CR	SAD2+6AP+CR	
8	SAD1+7AP	SAD2+7AP	SAD1+7AP+1	SAD2+7AP+1		SAD1+7AP+CR	SAD2+7AP+CR	
9	SAD1+8AP	SAD2+8AP	SAD1+8AP+1	SAD2+8AP+1	...	SAD1+8AP+CR	SAD2+8AP+CR	
10	SAD1+9AP	SAD2+9AP	SAD1+9AP+1	SAD2+9AP+1		SAD1+9AP+CR	SAD2+9AP+CR	
11	SAD1+10AP	SAD2+10AP	SAD1+10AP+1	SAD2+10AP+1	...	SAD1+10AP+CR	SAD2+10AP+CR	
12	SAD1+11AP	SAD2+11AP	SAD1+11AP+1	SAD2+11AP+1		SAD1+11AP+CR	SAD2+11AP+CR	
13	SAD1+12AP	SAD2+12AP	SAD1+12AP+1	SAD2+12AP+1	...	SAD1+12AP+CR	SAD2+12AP+CR	
14	SAD1+13AP	SAD2+13AP	SAD1+13AP+1	SAD2+13AP+1		SAD1+13AP+CR	SAD2+13AP+CR	
15	SAD1+14AP	SAD2+14AP	SAD1+14AP+1	SAD2+14AP+1	...	SAD1+14AP+CR	SAD2+14AP+CR	
16	SAD1+15AP	SAD2+15AP	SAD1+15AP+1	SAD2+15AP+1		SAD1+15AP+CR	SAD2+15AP+CR	
SL1-7	SAD1+(SL1-7)AP	SAD2+(SL1-7)AP	SAD1+(SL1-7)AP+1	SAD2+(SL1-7)AP+1	...	SAD1+(SL1-7)AP+CR	SAD2+(SL1-7)AP+CR	
SL1-6	SAD1+(SL1-6)AP	SAD2+(SL1-6)AP	SAD1+(SL1-6)AP+1	SAD2+(SL1-6)AP+1		SAD1+(SL1-6)AP+CR	SAD2+(SL1-6)AP+CR	
SL1-5	SAD1+(SL1-5)AP	SAD2+(SL1-5)AP	SAD1+(SL1-5)AP+1	SAD2+(SL1-5)AP+1	...	SAD1+(SL1-5)AP+CR	SAD2+(SL1-5)AP+CR	
SL1-4	SAD1+(SL1-4)AP	SAD2+(SL1-4)AP	SAD1+(SL1-4)AP+1	SAD2+(SL1-4)AP+1		SAD1+(SL1-4)AP+CR	SAD2+(SL1-4)AP+CR	
SL1-3	SAD1+(SL1-3)AP	SAD2+(SL1-3)AP	SAD1+(SL1-3)AP+1	SAD2+(SL1-3)AP+1	...	SAD1+(SL1-3)AP+CR	SAD2+(SL1-3)AP+CR	
SL1-2	SAD1+(SL1-2)AP	SAD2+(SL1-2)AP	SAD1+(SL1-2)AP+1	SAD2+(SL1-2)AP+1		SAD1+(SL1-2)AP+CR	SAD2+(SL1-2)AP+CR	(LF-5)
SL1-1	SAD1+(SL1-1)AP	SAD2+(SL1-1)AP	SAD1+(SL1-1)AP+1	SAD2+(SL1-1)AP+1	...	SAD1+(SL1-1)AP+CR	SAD2+(SL1-1)AP+CR	(LF-3)
SL1	SAD1+(SL1)AP	SAD2+(SL1)AP	SAD1+(SL1)AP+1	SAD2+(SL1)AP+1		SAD1+(SL1)AP+CR	SAD2+(SL1)AP+CR	(LF-1)
SL1+1	SAD3	SAD4	SAD1+1	SAD4+1	...	SAD3+CR	SAD4+CR	(2)
SL1+2	SAD3+AP	SAD4+AP	SAD3+AP+1	SAD4+AP+1		SAD3+AP+CR	SAD4+AP+CR	(4)
SL1+3	SAD3+2AP	SAD4+2AP	SAD3+2AP+1	SAD4+2AP+1	...	SAD3+2AP+CR	SAD4+2AP+CR	(6)
SL1+4	SAD3+3AP	SAD4+3AP	SAD3+3AP+1	SAD4+3AP+1		SAD3+3AP+CR	SAD4+3AP+CR	(8)
SL1+5	SAD3+4AP	SAD4+4AP	SAD3+4AP+1	SAD4+4AP+1	...	SAD3+4AP+CR	SAD4+4AP+CR	
SL1+6	SAD3+5AP	SAD4+5AP	SAD3+5AP+1	SAD4+5AP+1		SAD3+5AP+CR	SAD4+5AP+CR	
SL1+7	SAD3+6AP	SAD4+6AP	SAD3+6AP+1	SAD4+6AP+1	...	SAD3+6AP+CR	SAD4+6AP+CR	
SL1+8	SAD3+7AP	SAD4+7AP	SAD3+7AP+1	SAD4+7AP+1		SAD3+7AP+CR	SAD4+7AP+CR	
SL1+9	SAD3+8AP	SAD4+8AP	SAD3+8AP+1	SAD4+8AP+1	...	SAD3+8AP+CR	SAD4+8AP+CR	
SL1+10	SAD3+9AP	SAD4+9AP	SAD3+9AP+1	SAD4+9AP+1		SAD3+9AP+CR	SAD4+9AP+CR	
SL1+11	SAD3+10AP	SAD4+10AP	SAD3+10AP+1	SAD4+10AP+1	...	SAD3+10AP+CR	SAD4+10AP+CR	
SL1+12	SAD3+11AP	SAD4+11AP	SAD3+11AP+1	SAD4+11AP+1		SAD3+11AP+CR	SAD4+11AP+CR	
SL1+13	SAD3+12AP	SAD4+12AP	SAD3+12AP+1	SAD4+12AP+1	...	SAD3+12AP+CR	SAD4+12AP+CR	
SL1+14	SAD3+13AP	SAD4+13AP	SAD3+13AP+1	SAD4+13AP+1		SAD3+13AP+CR	SAD4+13AP+CR	
SL1+15	SAD3+14AP	SAD4+14AP	SAD3+14AP+1	SAD4+14AP+1	...	SAD3+14AP+CR	SAD4+14AP+CR	
SL1+16	SAD3+15AP	SAD4+15AP	SAD3+15AP+1	SAD4+15AP+1		SAD3+15AP+CR	SAD4+15AP+CR	
LF-7	SAD3+(LF-SL1-7)AP	SAD4+(LF-SL2-7)AP	SAD3+(LF-SL1-7)AP+1	SAD4+(LF-SL2-7)AP+1	...	SAD3+(LF-SL1-7)AP+CR	SAD4+(LF-SL2-7)AP+CR	
LF-6	SAD3+(LF-SL1-6)AP	SAD4+(LF-SL2-6)AP	SAD3+(LF-SL1-6)AP+1	SAD4+(LF-SL2-6)AP+1		SAD3+(LF-SL1-6)AP+CR	SAD4+(LF-SL2-6)AP+CR	
LF-5	SAD3+(LF-SL1-5)AP	SAD4+(LF-SL2-5)AP	SAD3+(LF-SL1-5)AP+1	SAD4+(LF-SL2-5)AP+1	...	SAD3+(LF-SL1-5)AP+CR	SAD4+(LF-SL2-5)AP+CR	
LF-4	SAD3+(LF-SL1-4)AP	SAD4+(LF-SL2-4)AP	SAD3+(LF-SL1-4)AP+1	SAD4+(LF-SL2-4)AP+1		SAD3+(LF-SL1-4)AP+CR	SAD4+(LF-SL2-4)AP+CR	
LF-3	SAD3+(LF-SL1-3)AP	SAD4+(LF-SL2-3)AP	SAD3+(LF-SL1-3)AP+1	SAD4+(LF-SL2-3)AP+1	...	SAD3+(LF-SL1-3)AP+CR	SAD4+(LF-SL2-3)AP+CR	
LF-2	SAD3+(LF-SL1-2)AP	SAD4+(LF-SL2-2)AP	SAD3+(LF-SL1-2)AP+1	SAD4+(LF-SL2-2)AP+1		SAD3+(LF-SL1-2)AP+CR	SAD4+(LF-SL2-2)AP+CR	(LF-4)
LF-1	SAD3+(LF-SL1-1)AP	SAD4+(LF-SL2-1)AP	SAD3+(LF-SL1-1)AP+1	SAD4+(LF-SL2-1)AP+1	...	SAD3+(LF-SL1-1)AP+CR	SAD4+(LF-SL2-1)AP+CR	(LF-2)
LF	SAD3+(LF-SL1)AP	SAD4+(LF-SL2)AP	SAD3+(LF-SL1)AP+1	SAD4+(LF-SL2)AP+1		SAD3+(LF-SL1)AP+CR	SAD4+(LF-SL2)AP+CR	(LF)

(3) Basic timing

The basic read cycle of display memory in the S1D13700 varies with the clock divide ratios set, as shown below.

When the display clock frequency divide ratio = 1/4, display data is output every 8 system clock periods.

When the display clock frequency divide ratio = 1/8, display data is output every 16 system clock periods.

When the display clock frequency divide ratio = 1/16, display data is output every 32 system clock periods.

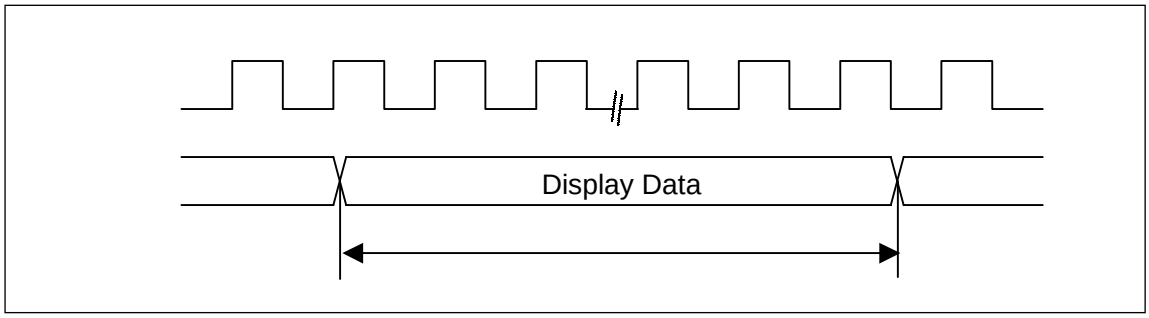


Figure 4-5 Basic read cycle of display memory

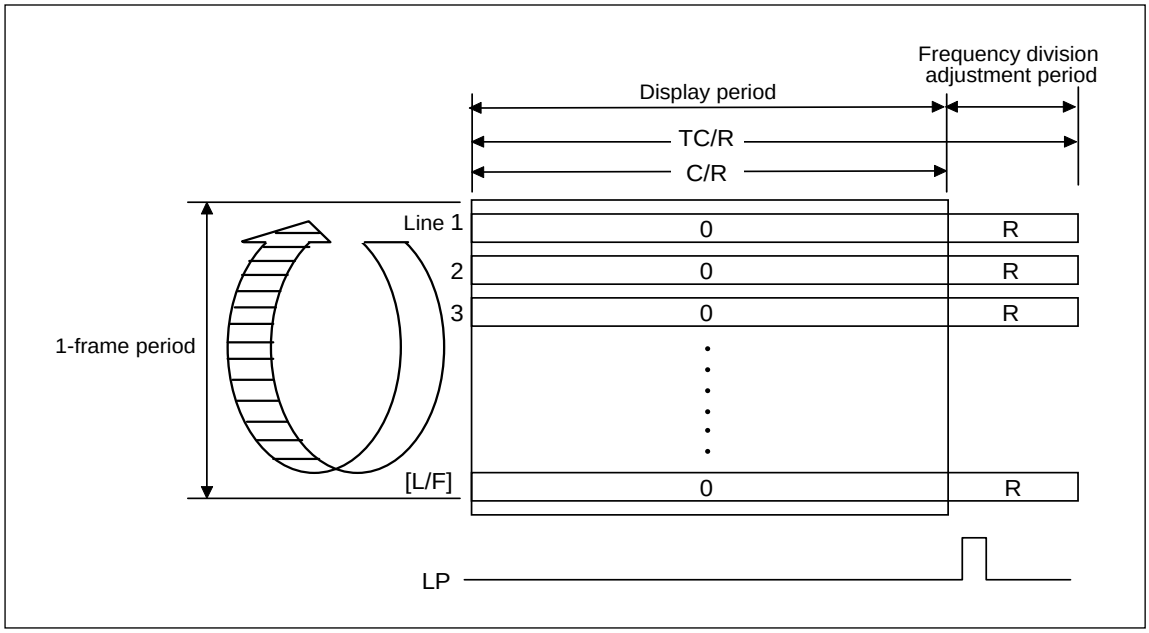


Figure 4-6 Relationship between TC/R and C/R

4.1.4 Cursor

(1) Cursor register function

The cursor register in the S1D13700 serves dual purposes as a cursor address register required to display the cursor on the screen, and as an address pointer to be referenced when accessing display memory.

Cursor register
- Cursor display address register
- Address pointer

To access any display memory area other than the screen while displaying the cursor, the cursor address must be preset before attempting such access and restored to the previous value after access is completed.

Note: The cursor will disappear if the cursor address is moved to any area other than the screen for more than several 100 ms.

(2) Direction of cursor movement

The cursor address is automatically shifted in the specified direction from the value preset by a memory control command.

(3) Cursor display layer

Although the S1D13700 can display up to three overlaid layers, the cursor can be displayed in only one of those layers. In other words, the cursor-attribute layer (or layer in which the cursor can be displayed) is:

First layer (L1) during two-layer composition, or
Third layer (L3) during three-layer composition.

The cursor will not appear if moved to other than those cursor-attribute layers. If the cursor must be displayed, change the layers or move the cursor-attribute layer to the cursor address location.

Although the cursor is generally displayed in text mode, the S1D13700 can also display a dummy cursor in graphics mode. This is accomplished by using the graphics screen as a display plane while not displaying the text screen, but using it to only generate addresses for cursor control.

Example: DISP ON/OFF

D = 1
FC1 = 0
FC0 = 1 } Cursor ON

FP1 = 0
FP0 = 0 } First screen block (text screen) OFF

FP3 = 0
FP2 = 1 } Second screen block (graphics screen) ON

4.1.5 Relationship between Display Memory and Screens

The display memory of the S1D13700 may be used as a virtual screen of greater width than the physical size of the LCD panel address range (C/R). One layer of the S1D13700 may be considered a window through which to look at the part of display memory that comprises a virtual screen. This window can be divided into two blocks that may correspond to independent areas on the virtual screen. Therefore, it is possible to use one block as a dynamically scrollable data area and the other as a stationary message area. (See Figures 4-7 and 4-8.)

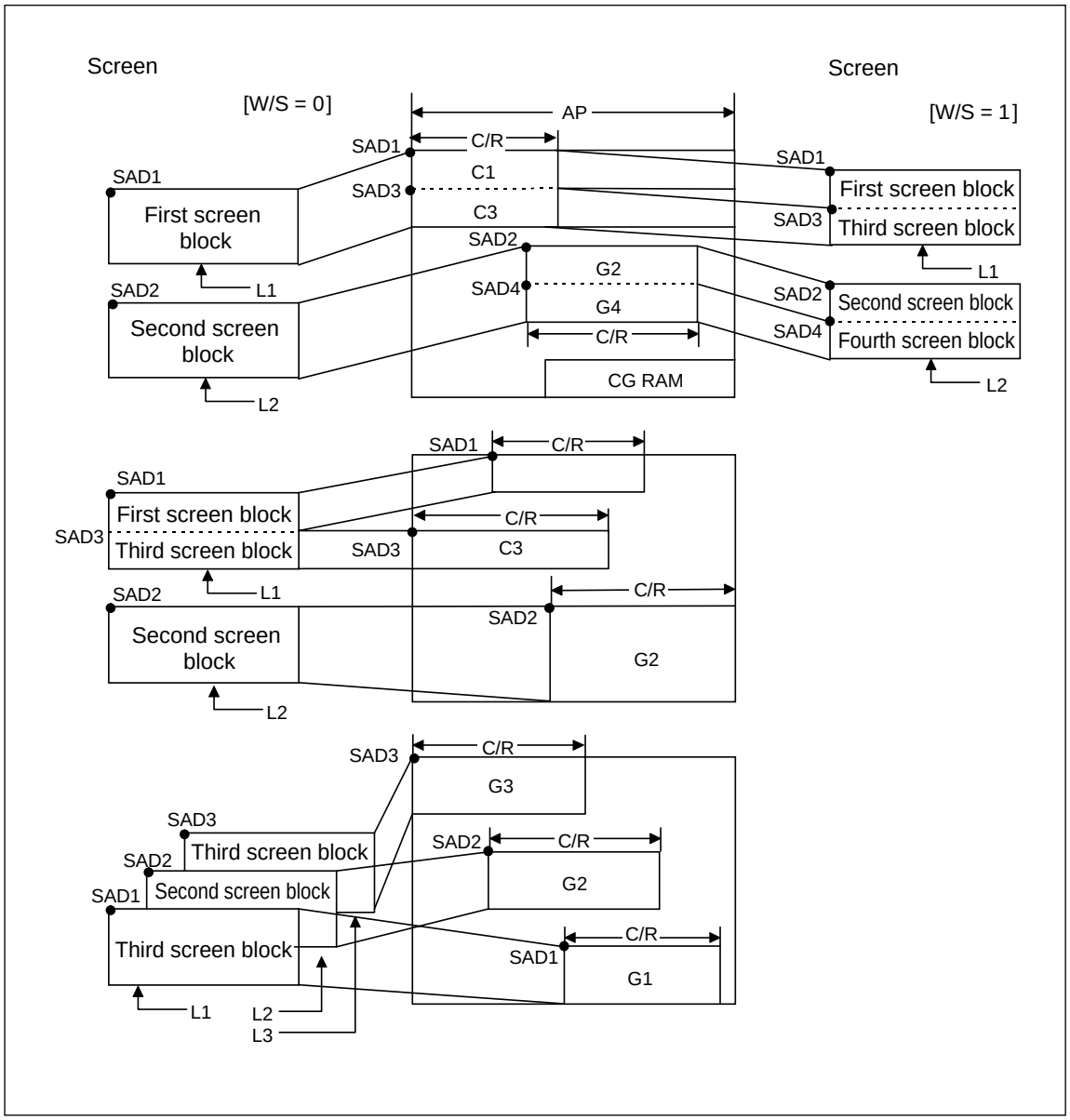


Figure 4-7 Relationship between display memory and screens

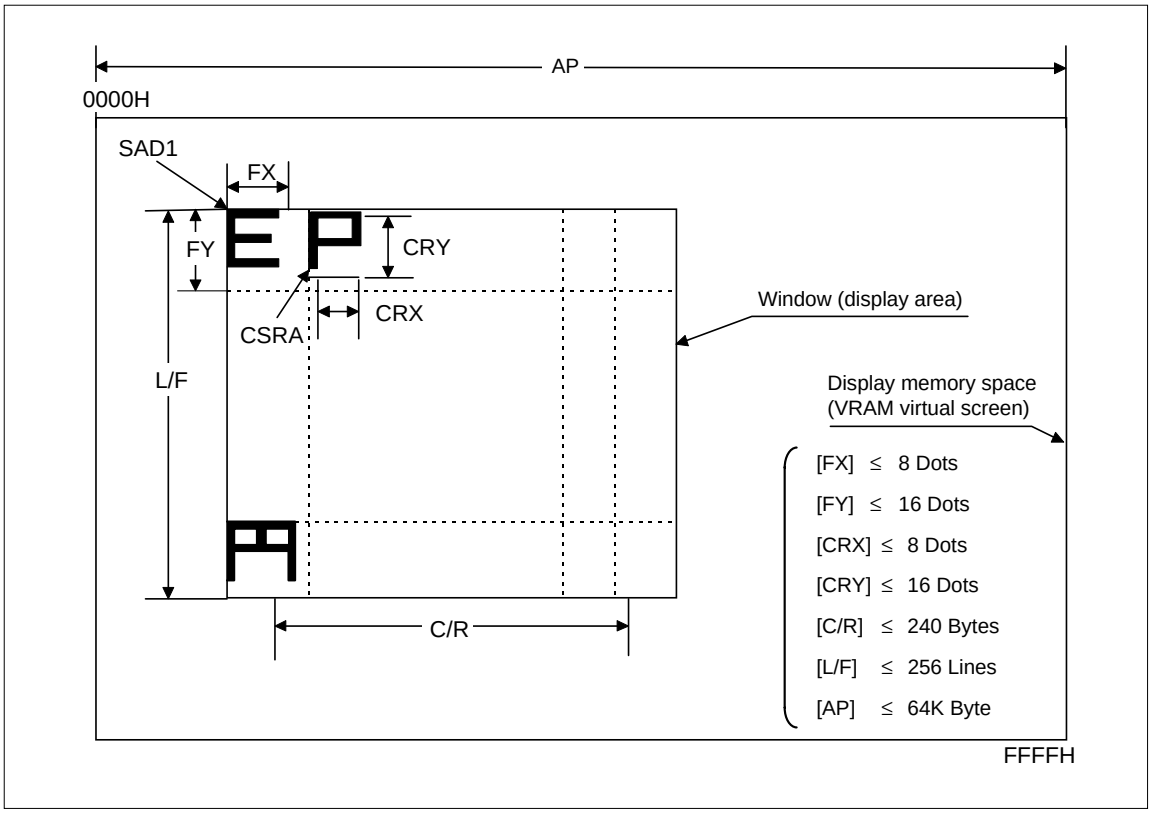


Figure 4-8 Window and display memory settings

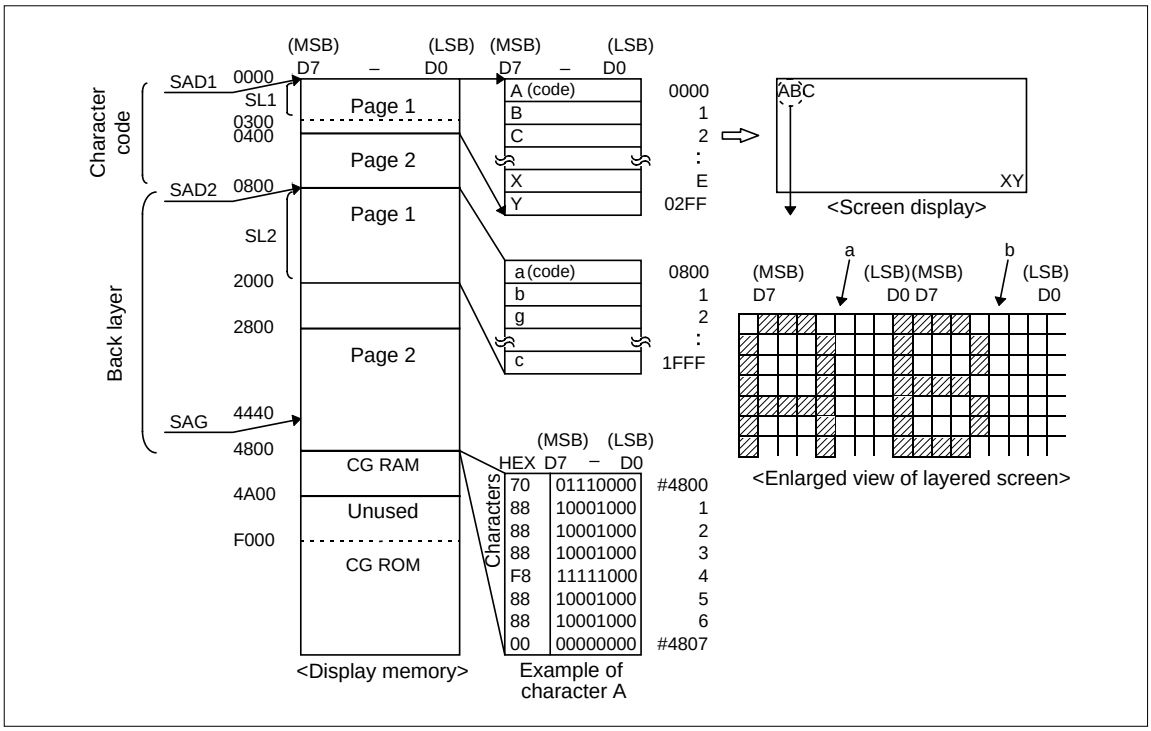


Figure 4-9 Example of display memory mapping

4.1.6 Determining Various Parameters

(1) Determining FX

Determine the character field size in the X direction [FX] from the number of dots in the X direction of display [VD] and the number of characters in the X direction [VC].

$$[VD] / [VC] \leq [FX]$$

The brackets [ ] denote an integral value beginning with 1, and [FX] indicates the number of dots.

(2) Determining C/R

Next, determine a value for [C/R] from the values of [VC] and [FX].

$$[C/R] = | [FX] / 8 | \text{ rounded up x } [VC]$$

Note: [C/R] indicates the number of characters obtained in units of addresses.

(3) Determining TC/R

TC/R must maintain the relationship $[TC/R] \geq [C/R] + 4$.

(4) Relationship between f_{OSC} and f_{FR}

Once TC/R has been determined, the lower-limit value of the oscillation frequency (f_{OSC}) can be obtained from the equation below because the frame frequency (f_{FR}) and number of display lines [L/F] are predetermined.

$$f_{OSC} \geq \{[TC/R] \text{ x } 9 + 1\} \text{ x } [L/F] \text{ x } f_{FR}$$

Note: 1. If standard crystals close to f_{OSC} thus obtained are unavailable, determine the appropriate f_{OSC} value for crystals with higher oscillation frequencies than the obtained value. To do so, reverse the calculation of the [TC/R] value in the equation above.

2. For the f_{FR} value of Epson LCD units, refer to the LCD unit specifications.

(5) Symptoms observed when TC/R is set incorrectly

- Scanning of display in the Y direction stops, with horizontal lines displayed in high contrast.
- All pixels go on or go off.
- The LP pin output signal is incomplete or inactive.
- The display of graphics or text becomes unstable.

Should any of the symptoms above be observed, even though the S1D13700's other signals connected to the LCD unit are normal, check whether the TC/R value is correct. If the TC/R value is the cause of the problem, simply set a larger TC/R value to restore normal operation.

Table 4-2 Example of Parameters for the LCD Unit

Number of pixels (X x Y)	[FX]	[FY]	[C/R]	TC/R	X'tal (MHz)
320 x 240	e.g., [FX] = 8 dots 320 ÷ 8 = 40...0 No blank dots	From a practical point of view, 8, 16, etc. are suitable.	[CR] = 40 = address → 27H During HDOT SCR, [C/R] = 41 addresses	2BH	5.72
	e.g., [FX] = 6 dots 320 ÷ 6 = 53...2 Two blank dots	↑	[CR] = 53 = address → 34H During HDOT SCR, [C/R] = 54 addresses	38H	7.40

Note: 1. Because the number of display dots varies with each LCD unit, there will be some fractional display dots depending on the value set for FX. In such case, the S1D13700 automatically blanks fractional parts at the right edge of the panel, and thus eliminates the need to manipulate display memory for adjustment.

2. Calculations are made assuming f_{FR} = 60 Hz.

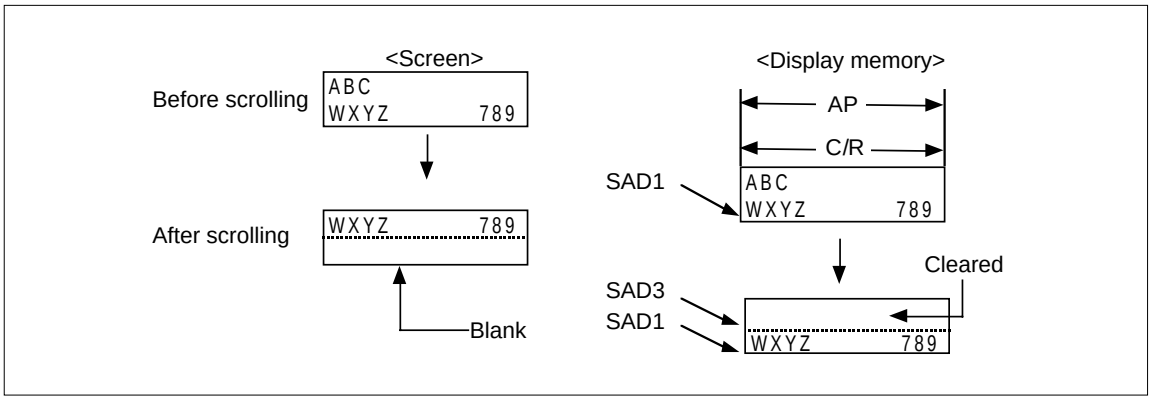
4.1.7 Scrolling

The MPU dynamically rewrites the scroll address registers (SAD1–SAD4) that provide the read start address in the S1D13700's display memory, thereby allowing various scroll modes to be set. In this case, the MPU manages all operations to execute scrolling, select scroll mode, and set a scroll rate.

(1) Intra-page scrolling

This refers to a mode of scroll operation whereby scrolling is performed within display memory space equivalent to one screen.

All lines are scrolled one line up and the bottom line is deleted as shown below. Since the S1D13700 does not automatically delete the bottom line, the MPU must rewrite the scroll address registers and simultaneously write blank data to the S1D13700.

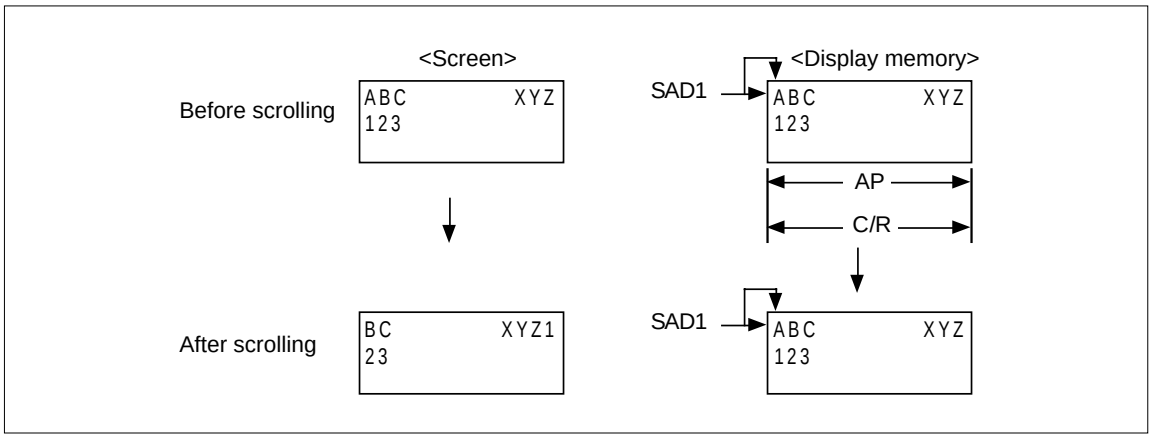


(2) Inter-page scrolling and page switching

Scrolling between pages and page switching can be performed only when display memory has more than one-screen equivalent capacity.

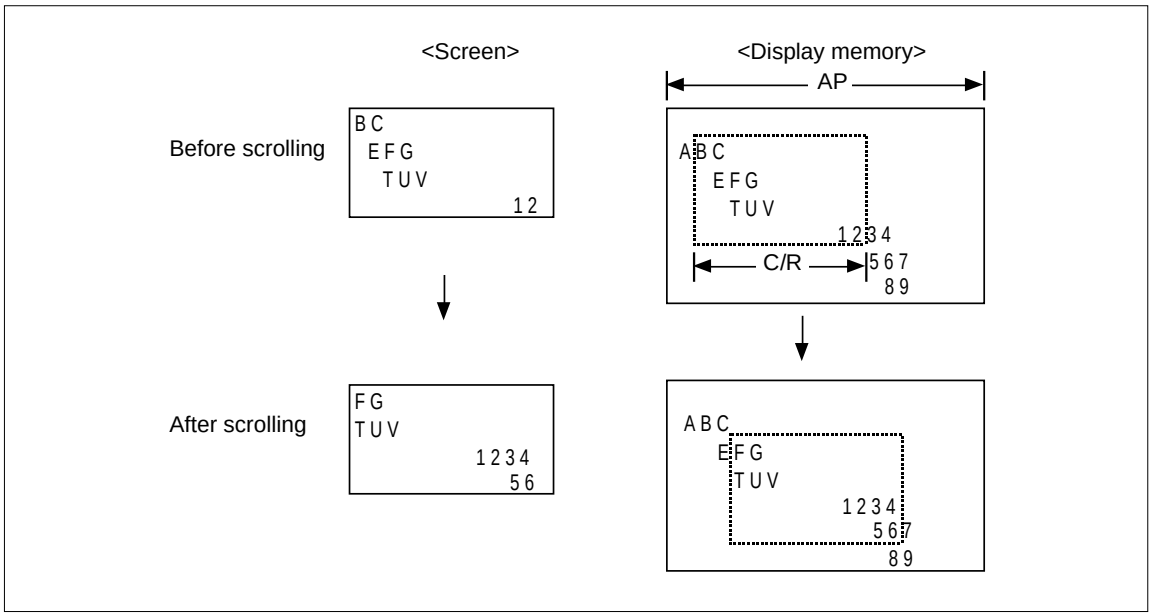
(3) Scrolling in the X direction

This refers to scrolling display in the X direction one character at a time, regardless of display memory size.



(4) Omnidirectional scrolling

This mode of scrolling is available when display memory has ample capacity larger than one screen in both the X and Y directions. Although display is normally scrolled one character at a time, the HDOT SCR command can be used to scroll display in the X direction one dot at a time.[Note 1]



(5) Scroll units

	Y direction	X direction
Text mode	Characters	Dots or characters
Graphics mode	Dots	Dots

Note 2

Note 1: Omnidirectional scrolling in units of dots is possible by using the SCROLL and HDOT SCR commands in combination.

Note 2: On a split screen, individual screen blocks cannot be independently scrolled in the X direction in dot units.

(6) Dotwise scrolling in the X direction (HDOT SCR)

Figure 4-10 shows the relationship between commands and display when a display pattern is smoothly scrolled to the left. In this case, the screen (window) moves to the right on a virtual screen. Therefore, the MPU only needs to sequentially increment the value of the HDOT SCR command parameter (number of dots to be shifted) without modifying the display start address (SAD) in the S1D13700 to shift display leftward one dot at a time. Then when display has been dot-shifted a distance equal to the character field, the MPU should reset the value of the HDOT SCR command parameter to 00H and simultaneously increment SAD by one address. Thus, smooth scrolling in the X direction is possible by performing this series of operations at appropriate time intervals.

To scroll the display pattern to the right, change the display dot address by reversing the order above. Should the window reach either edge of the virtual screen, use the MPU to manage the screen. Note that when smooth scrolling continues, the screen is not affected.

Also note that when scrolling display dotwise in the X direction using the HDOT SCR command, scrolling cannot be controlled separately in each layer because all layers are scrolled at the same time.

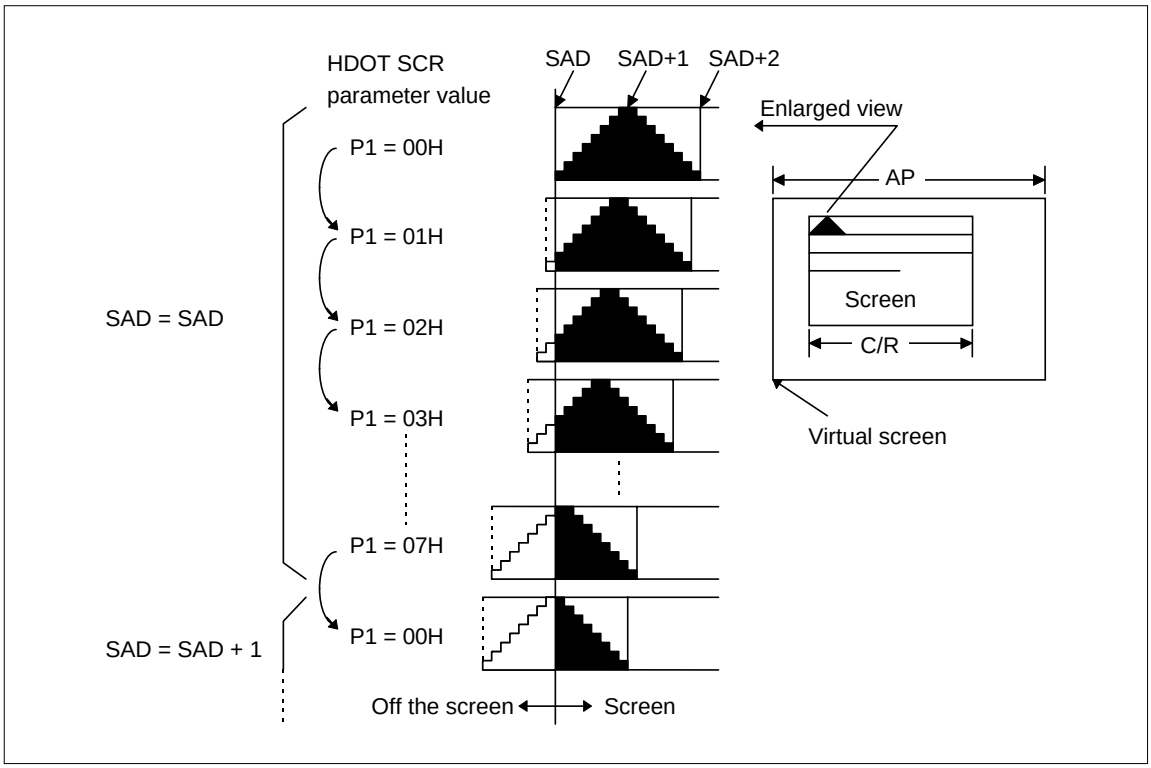


Figure 4-10 Example of using HDOT SCR ([FX] = 8)

Note: Because the speed at which the LCD responds to instructions varies with temperature, smooth scrolling at low temperatures in particular may not easily be recognized.

4.1.8 Attribute Display using the Layered Function

The S1D13700 provides a means of increasing the ability of expression on a monochrome liquid crystal display. More specifically, it uses the OVLAY and DISP ON/OFF commands to display characters in inverse video, produce halftone menu pads, and flash a given screen area for various highlighting effects as shown below.

Highlighting effects	MX1	MX0	Screen	First layer, single screen	Second layer, single screen
Inverse	0 1	1 1	IV EPSON	IV EPSON	
Halftone display	0 1	0 1	ME Yes, No	ME Yes, No	
Area flashing display	0 0	0 1	BL Error	BL	Error
Rules and underlining	0 0 1	0 1 1	RL LINE LINE	RL LINE LINE	

Use of the S1D13700's layered function will efficiently accomplish the highlighting effects above. The following describes a few examples of using this function to realize highlighting effects. Not all such effects can be used within the same screen block, however.

(1) Inverse

① Using the layered function

[Exclusive OR'ing of first layer (text) and second layer (graphics)]

①-1 CSRW
CSDIR
MWRITE

Write turn-on data "1" to the entire graphic area where characters are to be displayed in inverse video.

①-2 OVLAY
MX0 = "1"
MX1 = "0"

Specify an overlay method using the OVALY command so that the first and second layers will be exclusive OR'd.

①-3 DISP ON/OFF
FP0 = FP2
= "1"
FP1 = FP3
= "0"

Turn display of the first and second layers on using the DISP ON/OFF command. → Characters are displayed in inverse video.

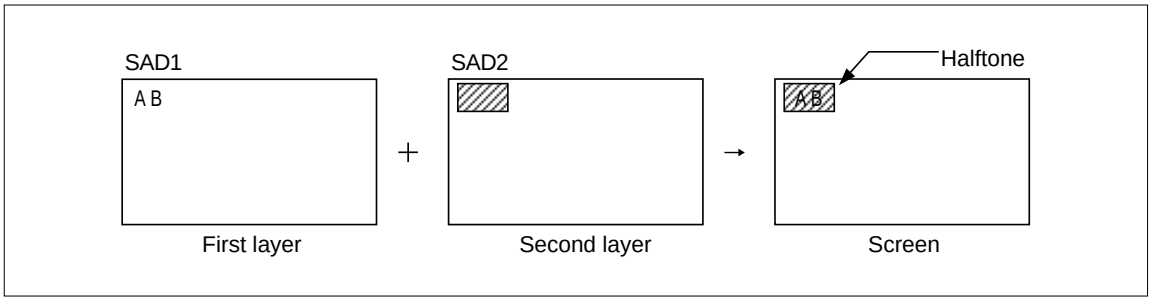
(2) Halftone display

The S1D13700 uses the DISP ON/OFF command's FP parameter to produce halftone display. This is accomplished by flashing the screen at 15 Hz. However, because this method of display may cause display to flicker, characteristics of the LCD module used must be carefully considered.

① Menu pad display

[OR'ing by the layered function]

OVLAY P1 = 00H DISP ON/OFF P1 = 34H	Disable flashing of the first layer and enable flashing of the second layer at 17 Hz, then overlay the first and second layers by OR'ing.



② Graph display

[OR'ing by the layered function]

OVLAY P1 = 00H DISP ON/OFF P1 = 34H	Disable flashing of the first layer and enable flashing of the second layer at 15 Hz, then overlay the first and second layers by OR'ing.

When displaying various data in the form of a graph for comparison purposes, this method of display is very effective because two types of diagrams distinguishable by differences in contrast can be displayed.

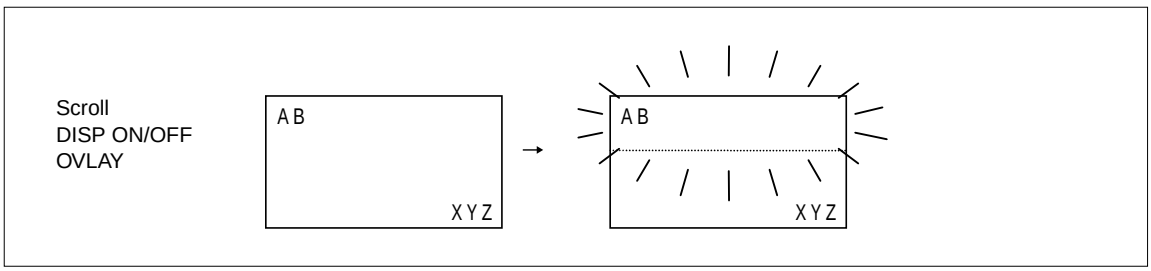
(3) Area flashing

① For flashing a few characters

Because the S1D13700 has a high-speed interface circuit, alternately rewriting the character and blank codes from the MPU to flash characters is an appropriate method. In this case, the MPU rewrites display data at intervals of 0.5 to 1.0 second as regulated by its internal timer.

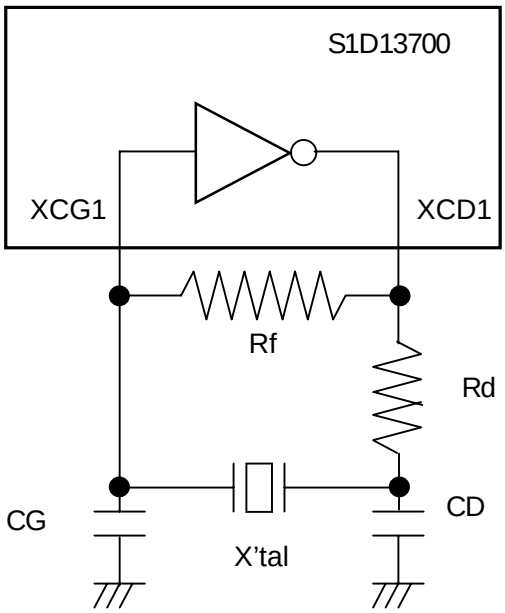
② For flashing a large area

Divide the first or second layer into halves with only the area required made to flash at 2 Hz, and overlay the halved layer blocks by OR'ing.



4.2 Oscillator Circuit

The S1D13700 features a built-in oscillator circuit, with a resonator connected to the XG and XD pins to generate oscillation. In addition to the crystal resonator, the feedback resistor Rf, drain resistor Rd, and oscillation capacitors CG and CD must be externally connected to the chip. The RC time constant needed to produce stable oscillation varies with the crystal resonator used and condition of the board. Determine the appropriate RC value through careful evaluation.

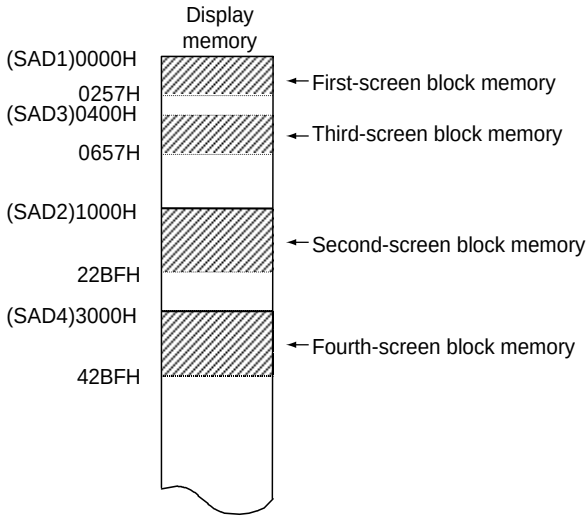
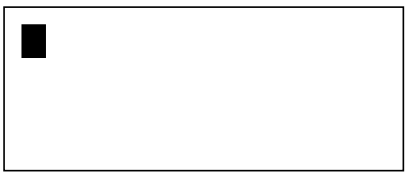


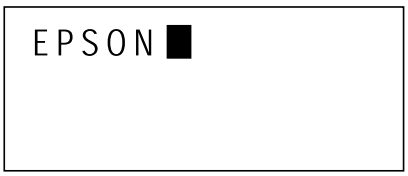
Note: Note that the higher the oscillation frequency, the smaller the CG and CD values.

4.3 Example of Initial Settings

8-bit bus interface
LCD unit 320 x 240 dot

No	Command	Operation
1	Power on	
2	Waits until power supply stabilizes.	Waits at least 3 ms after $V_{DD} \geq 4.5$ V and external reset are deasserted.
3	SYSTEM SET C = 40H P1 = 38H	Initializes the S1D13700. M0 : Internal CG ROM M1 : CG RAM (up to 32 characters) M2 : Y-direction character field range (8 lines) W/S : Dual-screen drive method IV : Uppermost line not corrected
	P2 = 87H	FX : X-direction character field (8 dots) WF : Two-frame AC drive
	P3 = 07H	FY : Y-direction character field (8 dots)
	P4 = 27FH	C/R : Display address range (40 columns per line)
	P5 = 2DH	TC/R : Total display address time in X direction (46 addresses per line) f_{OSC} = 6.0MHz, f_{FR} = 60Hz
	P6 = EFH	L/F : Number of display lines (240)
	P7 = 28H	AP : Virtual screen size in X direction (41 addresses)
	P8 = 00H	
4	SCROLL C = 44H P1 = 00H P2 = 00H	Sets start address of the first screen block to 0000H.
	P3 = 7FH	Sets number of display lines in the first screen block to 120.
	P4 = 00H P5 = 10H	Sets start address of the second screen block to 1000H.
	P6 = 7FH	Sets number of display lines in the second screen block to 120.
	P7 = 00H P8 = 04H	Sets start address of the third screen block to 0400H.
	P9 = 00H P10 = 30H	Sets start address of the fourth screen block to 3000H.

No	Command	Operation
		
5	HDOT SCR C = 5AH P1 = 00H	Sets number of dots to be shifted in the X direction to 0.
6	OVLAY C = 5BH P1 = 01H	MX1, MX0 : Overlaid for inverse display DM1 : First screen block in text mode DM2 : Third screen block in text mode
7	DISP ON/OFF C = 58H P1 = 56H	D : Entire screen display disabled FC1, FC0 : Cursor made to blink at 2 Hz FP1, FP0 : Display of first screen block turned on FC3, FP2 : Display of second and fourth screen blocks turned on FP5, FP4 : Display of third screen block turned on
8	CSRW C = 46H P1 = 00H P2 = 00H	Sets cursor address to the first screen block's start address (home position).
9	Clears the first layer display data.	Writes 20H (space character code) to memory location corresponding to the first layer (text screen).
10	Clears the second layer display data.	Writes 00H (dot turn-off data) to memory location corresponding to the second layer (graphics screen).
11	CSR FORM C = 5DH P1 = 04H P2 = 86H	CRX : Cursor size in X direction (5 dots) CRY : Cursor size in Y direction (7 dots) CM : Block cursor
12	DISP ON/OFF C = 59H	Restores entire screen display. screen 

No	Command	Operation
13	CSR DIR C = 4CH	Sets direction of cursor movement so that the cursor shifts to the right.
14	MWRITE C = 42H P1 = 20H P2 = 45H P3 = 50H P4 = 53H P5 = 4FH P6 = 4EH	Sets space code. Sets character code for the letter “E.” Sets character code for the letter “P.” Sets character code for the letter “S.” Sets character code for the letter “O.” Sets character code for the letter “N.” 
15	CSRW C = 46H P1 = 00H P2 = 10H	Presets cursor address to the second screen block’s start address.
16	CSR DIR C = 4FH	Sets direction of cursor movement so that the cursor shifts downward.
17	MWRITE C = 42H P1 = FFH ↓ P9 = FFH	Fills the left side of displayed letter E with dots by entering character code to 9 lines of the second screen block that corresponds to the first column on the first line.
18	CSRW C = 46H P1 = 01H P2 = 10H	Presets the cursor address to address 10001H.
19	MWRITE C = 42H P1 = FFH ↓ P9 = FFH	Fills the second screen block that corresponds to the second column on the first line with dots.

No	Command	Operation
20	CSRW	Repeats steps 18 and 19 until the background screen of the EPSON character string is filled with dots as shown below.
29	MWRITE	Inverse display
30	CSRW C = 46H P1 = 00H P2 = 04H	Presets the cursor address to the first column on the first line of the third screen block.
31	CSR DIR C = 4CH	Sets direction of cursor movement so that the cursor shifts to the right.
32	MWRITE C = 42H P1 = 44H P2 = 6FH P3 = 74H P4 = 20H P5 = 4DH P6 = 61H P7 = 74H P8 = 72H P9 = 69H P10 = 78H P11 = 20H P12 = 4CH P13 = 43H P14 = 44H	 Sets character code for the letter “D.” Sets character code for the letter “o.” Sets character code for the letter “t.” Sets character code for the letter “ ” Sets character code for the letter “M.” Sets character code for the letter “a.” Sets character code for the letter “t.” Sets character code for the letter “r.” Sets character code for the letter “i.” Sets character code for the letter “x.” Sets character code for the letter “ ” Sets character code for the letter “L.” Sets character code for the letter “C.” Sets character code for the letter “D.”

Example of display mode settings [1]

[1] For overlaying text and graphics

1. Conditions

   (1) 320 x 240 dots: Single-screen drive method (1/240 duty cycle)

   (2) First layer: Text display

   (3) Second layer: Graphic display

   (4) Character font: 8 x 8 dots

   (5) CG RAM unused

2. Display memory allocation

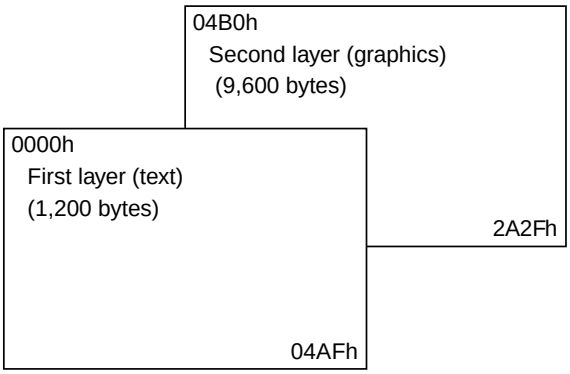
   (1) First layer (text display)
   Number of characters in horizontal direction = 320 / 8 = 40
   Number of characters in vertical direction = 240 / 8 = 30

   Therefore, the required size of memory is 40 x 30 = 1,200 bytes.

   (2) Second layer (graphic display)
   Number of characters in horizontal direction = 320 / 8 = 40
   Number of characters in vertical direction = 240 / 1 = 240

   Therefore, the required size of memory is 40 x 240 = 9,600 bytes.

[Relationship between display and memory]



3. Example of basic register settings

SYSTEM SET	Determination of TC/R
C = 40H	
P1 = 30H	Assuming f_{FR} = 60 Hz
P2 = 87H	when f_{OSC} = 6 MHz,
P3 = 07H	
P4 = 27H	6 MHz = {[TC/R] x 9 + 1} x 240 x 60
P5 = 2DH	Therefore, [TC/R] = 46
P6 = EFH	TC/R = 2DH
P7 = 28H	
P8 = 00H	
SCROLL	
C = 44H	
P1 = 00H	
P2 = 00H	
P3 = F0H	
P4 = B0H	
P5 = 04H	
P6 = F0H	
P7 = *H	
P8 = *H	
P9 = *H	
P10 = *H	* : don't care
CSRFORM	
C = 5DH	
P1 = 04H	
P2 = 86H	
HDOT SCR	
C = 5AH	
P1 = 00H	
OVLAY	
C = 5BH	
P1 = 00H	
DISP ON/OFF	
C = 59H	
P1 = 16H	

Example of display mode settings [2]

[2] For overlaying two graphic screens

1. Conditions

   (1) 320 x 240 dots: Single-screen drive method (1/240 duty cycle)

   (2) First layer: Graphic display

   (3) Second layer: Graphic display

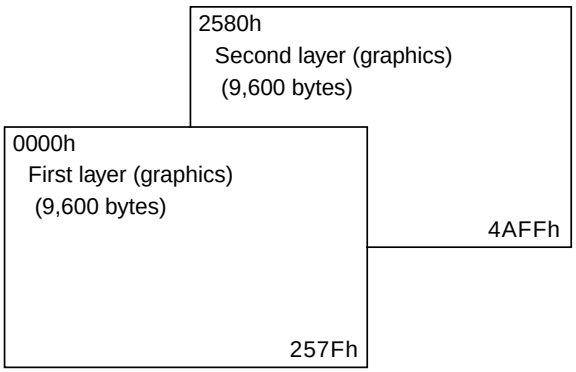
2. Display memory allocation

   (1) First layer (graphic display)
   Number of characters in horizontal direction = 320 / 8 = 40
   Number of characters in vertical direction = 240 / 1 = 240

   Therefore, the required size of memory is 40 x 240 = 9,600 bytes.

   (2) Second layer (graphic display)
   For the first layer, the required size of memory is 40 x 240 = 9,600 bytes.

[Relationship between display and memory]



3. Example of basic register settings

SYSTEM SET	Determination of TC/R
C = 40H	
P1 = 30H	Assuming f_{FR} = 60 Hz
P2 = 87H	when f_{OSC} = 6 MHz,
P3 = 00H	
P4 = 27H	6 MHz = {[TC/R] x 9 + 1} x 240 x 60
P5 = 2DH	Therefore, [TC/R] = 46
P6 = EFH	TC/R = 2DH
P7 = 28H	
P8 = 00H	
SCROLL	
C = 44H	
P1 = 00H	
P2 = 00H	
P3 = F0H	
P4 = 80H	
P5 = 25H	
P6 = F0H	
P7 = *H	
P8 = *H	
P9 = *H	
P10 = *H	* : don't care
CSRFORM	
C = 5DH	
P1 = 04H	
P2 = 86H	
HDOT SCR	
C = 5AH	
P1 = 00H	
OVLAY	
C = 5BH	
P1 = 00H	
DISP ON/OFF	
C = 59H	
P1 = 16H	

Example of display mode settings [3]

[3] For overlaying three graphic screens

1. Conditions

   (1) 320 x 240 dots: Single-screen drive method (1/240 duty cycle)

   (2) First layer: Graphic display

   (3) Second layer: Graphic display

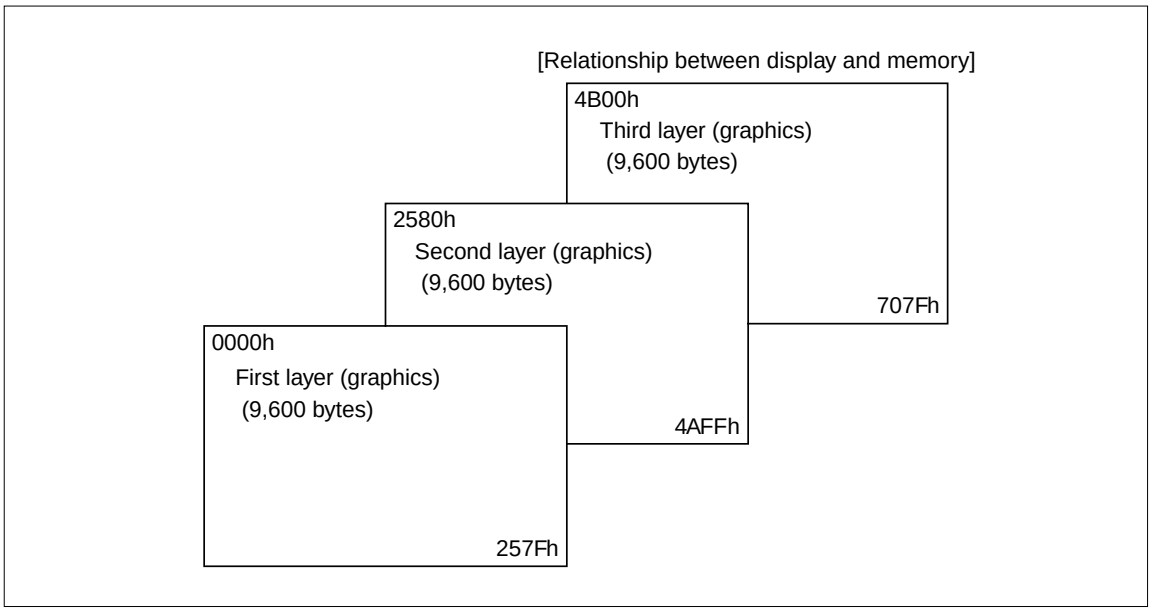
   (4) Third layer: Graphic display

2. Display memory allocation

   (1) First layer (graphic display)
   Number of characters in horizontal direction = 320 / 8 = 40
   Number of characters in vertical direction = 240 / 1 = 240

   Therefore, the required size of memory is 40 x 240 = 9,600 bytes.

   (2) Second and third layers (graphic display)
   For the first layer, the required size of memory is 40 x 240 = 9,600 bytes each.



3. Example of basic register settings

SYSTEM SET	Determination of TC/R
C = 40H	
P1 = 30H	Assuming f_{FR} = 60 Hz
P2 = 87H	when f_{OSC} = 6 MHz,
P3 = 00H	
P4 = 27H	6 MHz = {[TC/R] x 9 + 1} x 240 x 60
P5 = 2DH	Therefore, [TC/R] = 46
P6 = EFH	TC/R = 2DH
P7 = 28H	
P8 = 00H	
SCROLL	
C = 44H	
P1 = 00H	
P2 = 00H	
P3 = F0H	
P4 = 80H	
P5 = 25H	
P6 = F0H	
P7 = 00H	
P8 = 4BH	
P9 = *H	
P10 = *H	* : don't care
CSRFORM	
C = 5DH	
P1 = 04H	
P2 = 86H	
HDOT SCR	
C = 5AH	
P1 = 00H	
OVLAY	
C = 5BH	
P1 = 00H	
DISP ON/OFF	
C = 59H	
P1 = 16H	

4.4 Character Fonts and Character Codes

4.4.1 Character Fonts (Internal CG)

Note: The character size is 5 x 7 dots. ■ represents a 6 x 8-dot entirely black pattern.

4.4.2 Character Codes

Relationship between Character Codes and Those Usable as CG RAM (for combined use with internal CG ROM)

Table 4-3 Character Codes

								8-bit series							
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

YS3 LS3

D7	D6	D5	D4	D3	D2	D1	D0	4 high-order bits / 4 low-order bits		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				0	0	0	0	0					0	@	P	`	p				-	ﾀ	ﾐ		
				0	0	0	1	1				!	1	A	Q	a	q			。	ｱ	ﾁ	ﾑ		
				0	0	1	0	2				“	2	B	R	b	r			「	ｲ	ﾂ	ﾒ		
				0	0	1	1	3				#	3	C	S	c	s			」	ｳ	ﾃ	ﾓ		
				0	1	0	0	4				$	4	D	T	d	t			、	ｴ	ﾄ	ﾔ		
				0	1	0	1	5				%	5	E	U	e	u			・	ｵ	ﾅ	ﾕ		
				0	1	1	0	6				&	6	F	V	f	v			ｦ	ｶ	ﾆ	ﾖ		
				0	1	1	1	7				‘	7	G	W	g	w			ｧ	ｷ	ﾇ	ﾗ		
				1	0	0	0	8				(	8	H	X	h	x			ｨ	ｸ	ﾈ	ﾘ		
				1	0	0	1	9				)	9	I	Y	I	y			ｩ	ｹ	ﾉ	ﾙ		
				1	0	1	0	A	10			*	:	J	Z	j	z			ｪ	ｺ	ﾊ	ﾚ		
				1	0	1	1	B	11			+	;	K	[	k	{			ｫ	ｻ	ﾋ	ﾛ		
				1	1	0	0	C	12			,	<	L	¥	l	¦			ｬ	ｼ	ﾌ	ﾜ		
				1	1	0	1	D	13			.	=	M	]	m	}			ｭ	ｽ	ﾍ	ﾝ		
				1	1	1	0	E	14			-	>	N	^	n	→			ｮ	ｾ	ﾎ	゛		
				1	1	1	1	F	15			/	?	O	_	o	←			ｯ	ｿ	ﾏ	゜		

CG RAM1 CG RAM2

M1=0

M1=1

5 SPECIFICATIONS

5.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Power Supply Voltage	HV_{DD}	-0.3 – 7.0	V	
	LV_{DD}	-0.3 – 4.0	V	
Input Voltage	HV_{IN}	-0.3 – HV_{DD} + 0.5	V	
	LV_{IN}	-0.3 – LV_{DD} + 0.5	V	
Output Voltage	HV_{OUT}	-0.3 – HV_{DD} + 0.5	V	
	LV_{OUT}	-0.3 – LV_{DD} + 0.5	V	
Output Current per Pin	I_{OUT}	±30	mA	
Operating Temperature	T_{opr}	-40 – 85	°C	
Storage Temperature	T_{stg}	-65 – 150	°C	
Soldering Temperature and Time	T_{solder}	Heat resistance rank SE2	—	

Note: 1. When using a power supply with high impedance, a large potential difference between the chip's internal power supply voltage and the input voltage may occur, thus making the power supply susceptible to latch-up. Therefore, pay particular attention to the power supply and its wiring.

2. All voltage are based on V_{SS} = 0V

3. The symbol H*** indicates 5 V-block pins; L*** indicates 3.3 V-block pins.

5.2 Recommended Operating Conditions

Parameter	Symbol	Test Condition	Rated Value			Unit	Applicable Pins
			Min.	Typ.	Max.		
Power Supply Voltage (High Voltage)	HIOVDD	V_{SS} = 0V	4.5	5.0	5.5	V	HIOVDD
			3.0	3.3	3.6		
Power Supply Voltage (Low Voltage)	NIOVDD	V_{SS} = 0V	4.5	5.0	5.5	V	NIOVDD
			3.0	3.3	3.6		
Core Power Supply Voltage	COREVDD	V_{SS} = 0V	3.0	3.3	3.6	V	COREVDD
Input Voltage	HIOVIN	—	V_{SS}	—	HIOVDD	V	
Input Voltage	NIOVIN	—	V_{SS}	—	NIOVDD	V	
Operating Temperature	TOPR	—	-20	25	70	°C	

5.3 Electrical Characteristics

[V_{SS} = 0V, HV_{DD} = 4.5 – 5.5V, Ta = -40 – 85°C]

Parameter	Symbol	Test Condition	Rated Value			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	—	-1	—	1	uA
OFF-state Leakage Current	I_{OZ}	—Note 2)	-1	—	1	uA
High Level Output Voltage	V_{OH}	I_{OH} = -8.0mA HV_{DD}=Min	HV_{DD}-0.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 8.0m HV_{DD}=Min	—	—	0.4	V
High Level Input Voltage	V_{IH1}	CMOS level HV_{DD} = Max	3.5	—	—	V
Low Level Input Voltage	V_{IL1}	CMOS level HV_{DD} = Min	—	—	1.0	V
Positive Trigger Voltage	V_{T1+}	CMOS Schmitt	2.0	—	4.0	V
Negative Trigger Voltage	V_{T1-}	CMOS Schmitt	0.8	—	3.1	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt	0.3	—	—	V
High Level Input Voltage	V_{IH2}	TTL level HV_{DD} = Max	2.0	—	—	V
Low Level Input Voltage	V_{IL2}	TTL level HV_{DD} = Min	—	—	0.8	V
Pulldown Resistance	R_{PD}	VI = HV_{DD}	30	60	144	kΩ
Operating Supply Current	I_{opr}	f_{OSC} =10 MHz Nonloaded 256 x 200dot	—	TBD	TBD	mA
Quiescent Supply Current (between HV_{DD} and V_{SS})	I_{QH}	Sleep mode XCG1, CS#, $\overline{RD}$# = V_{DD}	—	—	30	uA
Quiescent Supply Current (between LV_{DD} and V_{SS})	I_{QH}	Sleep mode XCG1, CS#, $\overline{RD}$# = V_{DD}	—	—	35	uA

Note: 1. The pulse applied to the RESET# pin must be held low for 200 µs or more to be effective. However, avoid keeping the input pulse active for more than several seconds because the LCD's d.c. drive capability may be adversely affected.

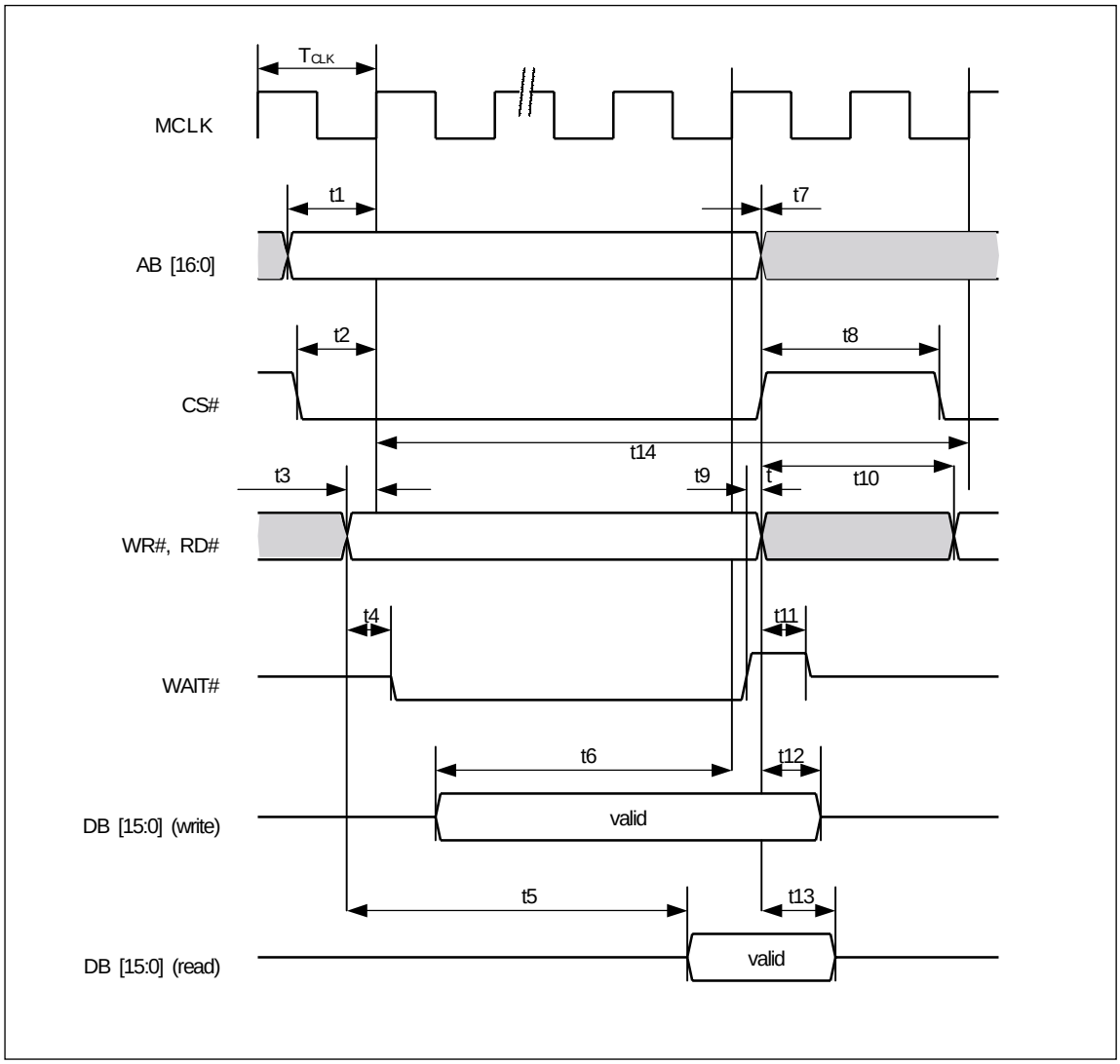
2. The VB0–DB7 pins come with a feedback circuit, so that even when input becomes high impedance, the pins retain the state held immediately before. Therefore, input voltage of an intermediate level allows input current to flow to the pin.

[V_{SS} = 0V, VDD = LV_{DD} = 3.3 – 0.3V, Ta = -40 – 85°C]

Parameter	Symbol	Test Condition	Rated Value			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	—	-1	—	1	uA
OFF-state Leakage Current	I_{OZ}	— Note 2)	-1	—	1	uA
High Level Output Voltage	V_{OH}	I_{OH} = -6.0mA HV_{DD}=Min	HV_{DD}-0.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 6.0m HV_{DD}=Min	—	—	0.4	V
High Level Input Voltage	V_{IH1}	LVTTL level V_{DD} = Max	2.0	—	—	V
Low Level Input Voltage	V_{IL1}	LVTTL level V_{DD} = Min	—	—	0.8	V
Positive Trigger Voltage	V_{T1+}	LVTTL Schmitt	1.1	—	2.4	V
Negative Trigger Voltage	V_{T1-}	LVTTL Schmitt	0.6	—	1.8	V
Hysteresis Voltage	V_{H1}	LVTTL Schmitt	0.1	—	—	V
Pulldown Resistance	R_{PD}	VI = V_{DD}	20	50	120	kΩ
Operating Supply Current	I_{opr}	f_{OSC} =10 MHz Nonloaded 256 x 200dot	—	TBD	TBD	mA
Quiescent Supply Current (between LV_{DD} and V_{SS})	I_{QH}	Sleep mode XCG1, CS#, RD# = V_{DD}	—	—	35	uA

5.4 Timing Characteristics

5.4.1 System Bus (Generic Bus/80-series MPU)



* MCLK denotes CLKI or the internally generated system clock.

Gemeric Bus Interface Timing

[V_{SS} = 0V, V_{DD} = 4.5 – 5.5V, Ta = -40 – 85°C]

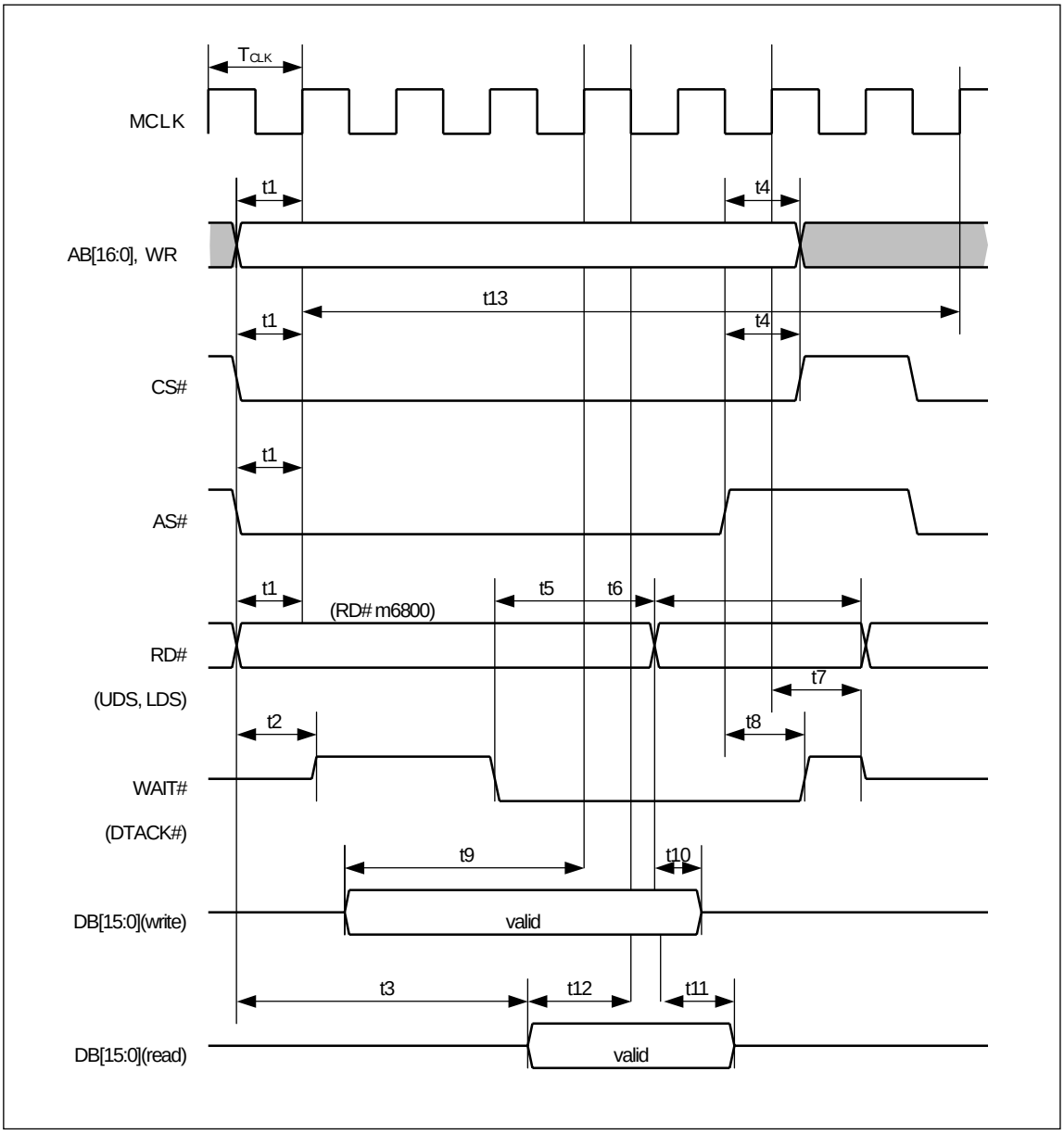
Symbol	Parameter	Spec		Unit
		Min.	Max.	
f_{CLK}	BUS clock frequency	—	64	MHz
T_{CLK}	BUS clock period	$1/f_{CLK}$	—	ns
t1	AB [16 : 0] setrup to first CLK rising edge where CS# = 0 and either RD# = 0 or WR# = 0	11	—	ns
t2	CS# setup to CLK rising edge	9	—	ns
t3	RD#, WR# setup to CLK rising edge	9	—	ns
t4	RD#, WR# state change to WAIT# driven low	1	5	ns
t5	RD# falling edge to DB [15 : 0] driven (ead cycle)	3Tc+9ns	—	Tclk
t6	DB [15 : 0] setup to 4th rising CLK edge after CS# = 0 and WR# = 0	1	—	T_{CLK}
t7	AB [16 : 0], CS# hold from RD#, WR# rising edge	8	—	ns
t8	CS# deasserted to reasserted - When read - when Write (next cycle = write cycle) - when Write (next cycle = read cycle)	 1Tclk 2Tclk+8ns 5Tclk+8ns	—	 ns ns ns
t9	WAIT# rising edge to RD#, WR# rising edge	0	—	ns
t10	WR#, RD# deasserted to reasserted - When read - when Write (next cycle = write cycle) - when Write (next cycle = read cycle)	 1Tclk 2Tclk+8ns 5Tclk+8ns	—	 ns ns ns
t11	Rising edge of either RD# or WR# to WAIT# high impedance 0.5 TCLK	—	0.5	T_{CLK}
t12	D [15 : 0] hold from WR# rising edge (write cycle)	1	—	ns
t13	D [15 : 0] hold from RD# rising edge (read cycle)	1	—	ns
t14	Cycle Length Read Write (next write cycle) Write (next read cycle)	6 7 10	—	T_{CLK}

Gemeric Bus Interface Timing

[V_{SS} = 0V, V_{DD} = 3.0 – 3.6V, Ta = -40 – 85°C]

Symbol	Parameter	Spec		Unit
		Min.	Max.	
f_{CLK}	BUS clock frequency	—	64	MHz
T_{CLK}	BUS clock period	$1/f_{CLK}$	—	ns
t1	AB [16 : 0] setrup to first CLK rising edge where CS# = 0 and either RD# = 0 or WR# = 0	12	—	ns
t2	CS# setup to CLK rising edge	11	—	ns
t3	RD#, WR# setup to CLK rising edge	11	—	ns
t4	RD#, WR# state change to WAIT# driven low	1	7	ns
t5	RD# falling edge to DB [15 : 0] driven (ead cycle)	3Tc+11ns	—	Tclk
t6	DB [15 : 0] setup to 4th rising CLK edge after CS# = 0 and WR# = 0	1	—	T_{CLK}
t7	AB [16 : 0], CS# hold from RD#, WR# rising edge	10	—	ns
t8	CS# deasserted to reasserted - When read - when Write (next cycle = write cycle) - when Write (next cycle = read cycle)	 1Tclk 2Tclk+10ns 5Tclk+10ns	—	 ns ns ns
t9	WAIT# rising edge to RD#, WR# rising edge	0	—	ns
t10	WR#, RD# deasserted to reasserted - When read - when Write (next cycle = write cycle) - when Write (next cycle = read cycle)	 1Tclk 2Tclk+10ns 5Tclk+10ns	—	 ns ns ns
t11	Rising edge of either RD# or WR# to WAIT# high impedance 0.5 TCLK	—	0.5	T_{CLK}
t12	D [15 : 0] hold from WR# rising edge (write cycle)	1	—	ns
t13	D [15 : 0] hold from RD# rising edge (read cycle)	1	—	ns
t14	Cycle Length Read Write (next write cycle) Write (next read cycle)	6 7 10	—	T_{CLK}

5.4.2 System Bus Read/write characteristics II (MC68K-series MPU)



* MCLK denotes CLKI or the internally generated system clock.

Motorola M68K#1 Interface Timing

[V_{SS} = 0V, V_{DD} = 4.5 – 5.5V, Ta = -40 – 85°C]

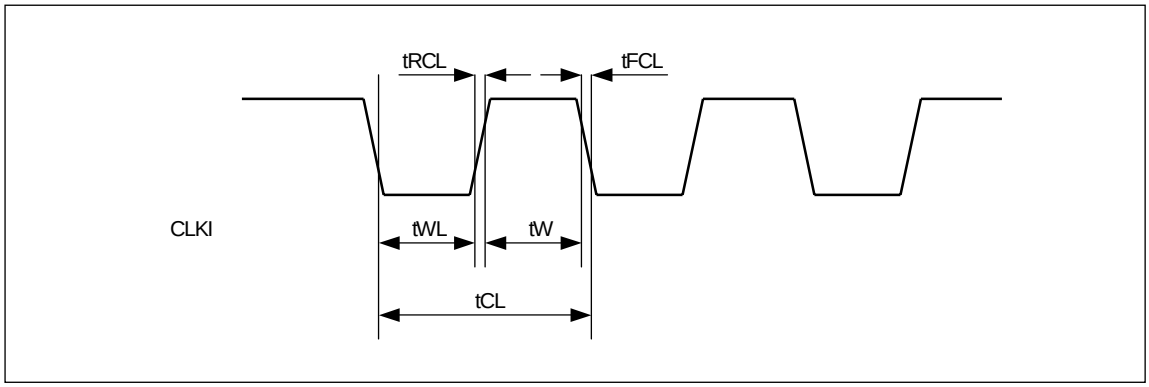
Symbol	Parameter	Spec		Unit
		Min.	Max.	
f_{CLK}	BUS clock frequency	—	64	MHz
T_{CLK}	BUS clock period	$1/f_{CLK}$	—	ns
t1	AB [16 : 0], WR# (R/W#) and CS# and AS# and RD# (UDS#, LDS#) setup to first CLK rising edge	9	—	ns
t2	CS# and AS# asserted to WAIT# (DTACK#) driven	1	7	ns
t3	RD# = 0 (UDS# = 0 or LDS# = 0) to DB [15 : 0] driven (read cycle)	3Tclk+9ns	—	ns
t4	AB [16 : 0], WR# (R/W#) and CS# hold from AS# rising edge	0	—	ns
t5	WAIT# (DTACK#) falling edge to RD# (UDS#, LDS#) rising edge	1	—	T_{CLK}
t6	RD# (USD#, LDS#) deasserted high to reasserted low - When read - when Write (next cycle = write cycle) - when Write (next cycle = read cycle)	 1Tclk 2Tclk+8ns 5Tclk+8ns	—	 ns ns ns
t7	CLK rising edge to WAIT# (DTACK#) high impedance	—	$1T_{CLK}$-2	ns
t8	AS# rising edge to WAIT# (DTACK#) rising edge	3	12	ns
t9	DB [15 : 0] valid to 4th CLK rising edge where CS# = 0, AS# = 0 and either RD# = 0 (UDS# = 0 or LDS# = 0) (wirte cycle)	1	—	T_{CLK}
t10	DB [15 : 0] hold from RD# (UDS#, LDS#) falling edge (wirte cycle)	4	—	ns
t11	RD# (UDS#, LDS#) rising edge to DB [15 : 0] high impedance (read cycle)	6	—	ns
t12	DB [15 : 0] valid setup time to 2nd CLK falling edge after WAIT# (DTACK#) goes low (read cycle)	6	—	ns
t13	t13 Cycle Length Read Write (next write cycle) Write (next read cycle)	7 8 11	—	T_{CLK}

Motorola M68K#1 Interface Timing

[V_{SS} = 0V, V_{DD} = 3.0 – 3.6V, Ta = -40 – 85°C]

Symbol	Parameter	Spec		Unit
		Min.	Max.	
f_{CLK}	BUS clock frequency	—	64	MHz
T_{CLK}	BUS clock period	$1/f_{CLK}$	—	ns
t1	AB [16 : 0], WR# (R/W#) and CS# and AS# and RD# (UDS#, LDS#) setup to first CLK rising edge	9	—	ns
t2	CS# and AS# asserted to WAIT# (DTACK#) driven	1	10	ns
t3	RD# = 0 (UDS# = 0 or LDS# = 0) to DB [15 : 0] driven (read cycle)	3Tclk+9ns	—	ns
t4	AB [16 : 0], WR# (R/W#) and CS# hold from AS# rising edge	0	—	ns
t5	WAIT# (DTACK#) falling edge to RD# (UDS#, LDS#) rising edge	1	—	T_{CLK}
t6	RD# (UDS#, LDS#) deasserted high to reasserted low - When read - when Write (next cycle = write cycle) - when Write (next cycle = read cycle)	 1Tclk 2Tclk+8ns 5Tclk+8ns	—	 ns ns ns
t7	CLK rising edge to WAIT# (DTACK#) high impedance	—	$1T_{CLK}$-2	ns
t8	AS# rising edge to WAIT# (DTACK#) rising edge	3	15	ns
t9	DB [15 : 0] valid to 4th CLK rising edge where CS# = 0, AS# = 0 and either RD# = 0 (UDS# = 0 or LDS# = 0) (wirte cycle)	1	—	T_{CLK}
t10	DB [15 : 0] hold from RD# (UDS#, LDS#) falling edge (wirte cycle)	4	—	ns
t11	RD# (UDS#, LDS#) rising edge to DB [15 : 0] high impedance (read cycle)	8	—	ns
t12	DB [15 : 0] valid setup time to 2nd CLK falling edge after WAIT# (DTACK#) goes low (read cycle)	8	—	ns
t13	Cycle Length Read Write (next write cycle) Write (next read cycle)	7 8 11	—	T_{CLK}

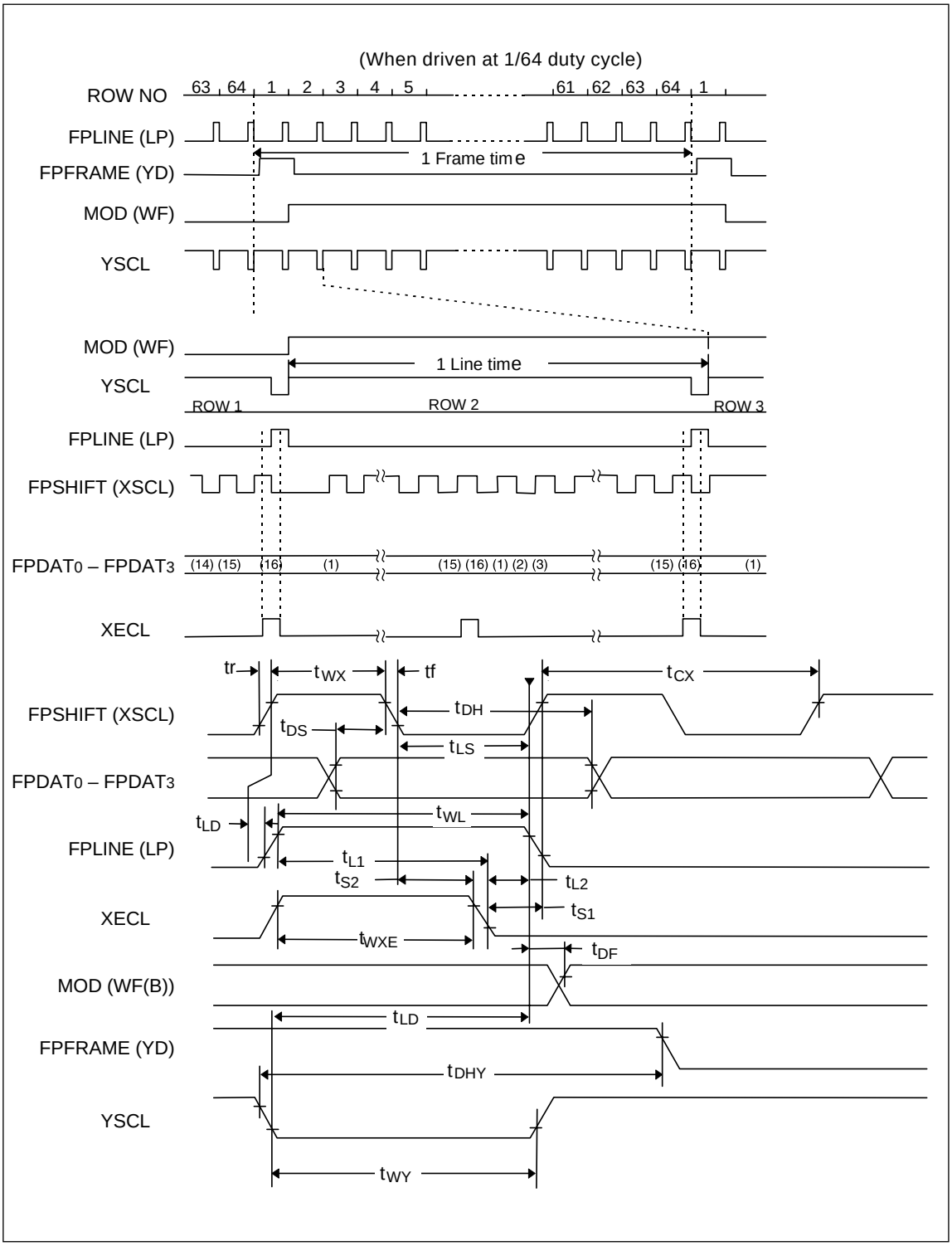
5.4.3 External Clock Input Characteristics



[V_{SS} = 0V, V_{DD} = 4.5 – 5.5V, Ta = -40 – 85°C]

Symbol	Parameter			Unit
		Min.	Max.	
t_{RCL}	External input clock rise time	—	2	ns
t_{FCL}	External input clock fall time	—	2	ns
t_{WH}	High-level pulse width of external input clock	7	—	ns
t_{WL}	Low-level pulse width of external input clock	7	—	ns
t_{CL}	External input clock period	16.4	—	ns

5.4.4 LCD Control Signal Timing Characteristics



Signal	Symbol	Parameter	Spec		Unit
			Min.	Max.	
FPSHIFT (XSCL)	t_{CX}	Shift Clock cycle time	*1		ns
	t_{WX}	XSCL Clock Pulse	$t_{CX}/2-6$		
FPDAT0 – FPDAT3	t_{DH}	XD [3 : 0] hold from XSCL falling edge	$2t_C$		ns
	t_{DS}	XD [3 : 0] setup to XSCL falling edge	$2t_C$		
FPLINE ÅiLPÅj	t_{LS}	Latch data setup time	$2t_C$		ns
	t_{WL}	Latch pulse setup time	$4t_C$		
	t_{LD}	XSCL rising edge to LP falling edge delay time	0		
MOD (WF)	t_{DF}	WF delay time		6	ns
FPFRAME (YD)	t_{DHY}	YSCL falling edge to YD falling edge	$2t_C$		ns
YSCL	t_{WY}	YSCL clock pulse width	$4t_C$		ns

*1

CNF [3 : 2]	XSCL Cycle Time
00	4Tc (= MCLK)
01	8Tc
10	16Tc
11	No Support

6 MPU INTERFACE

6.1 Connection to the System Bus

The S1D13700 uses a combination of CNF2/3/4, AB15–0, RD#, WR#, and CS# to discriminate information supplied to it via the system data bus as described in Section 2.2 “Pin Functions” on page 9.

In indirect interface mode, AB0 generally is connected to the least significant bit of the system address bus. CNF2 and CNF3 are provided for changing the functions of S1D13700 pins 58 and 59 to enable the chip to be connected directly to the 80 or 68-series MPU bus, and are pulled high or low through a resistor when in use. For the 80-series MPU, the S1D13700 should normally be mapped in I/O space.

6.1.1 80-series MPU

<Direct access for the 80-series interface>

CNF4	AB15 – AB1	AB0	RD#	WR#	Function
0	0or1	0or1	0	1	Read from command/parameter registers
0	0or1	0or1	1	1	Write to command/parameter registers

<Indirect access for the 80-series interface>

CNF4	AB15 – AB1	AB0	RD#	WR#	Function
1	—	0	0	1	—
1	—	1	0	1	Data (display data and cursor address) read
1	—	0	1	0	Data (display data and parameter) write
1	—	1	1	0	Command write (code only)

6.1.2 68-series MPU

<Direct access for the 68-series interface>

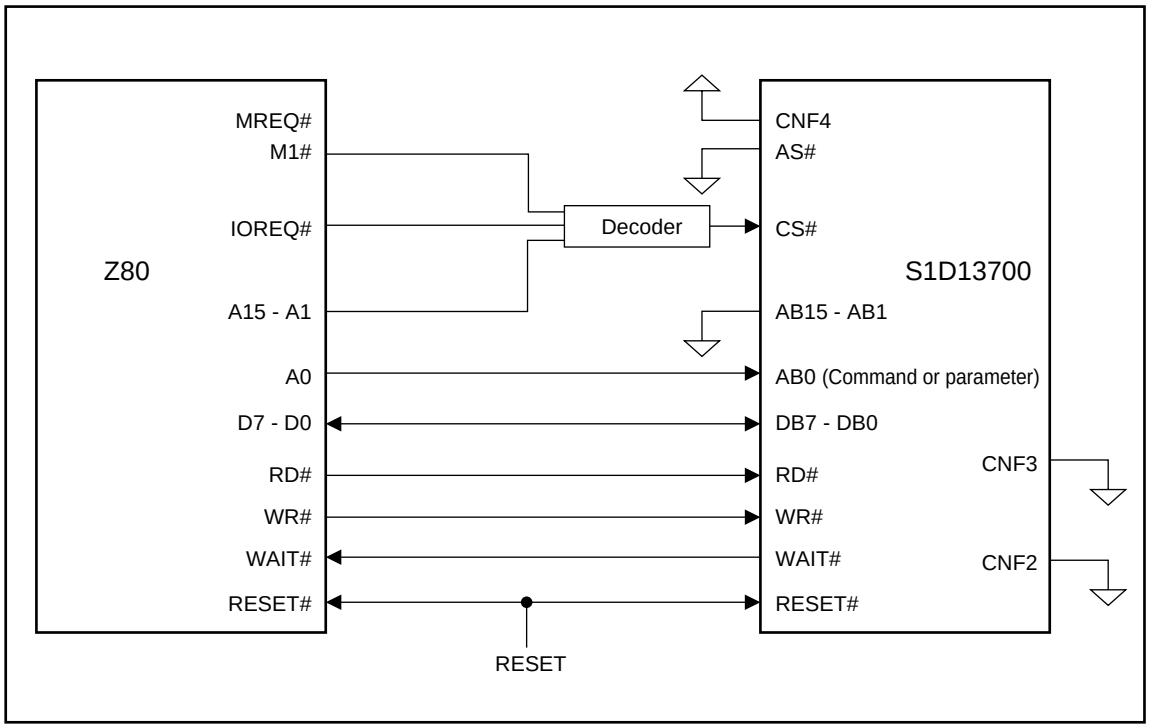
CNF4	AB15 – AB1	AB0	WR# (R/W#)	RD# (E)	Function
0	0or1	0or1	1	1	Read from command/parameter registers
0	0or1	0or1	0	1	Write to command/parameter registers

<Indirect access for the 68-series interface>

CNF4	AB15 – AB1	AB0	WR# (R/W#)	RD# (E)	Function
1	—	0	1	1	—
1	—	1	1	1	Data (display data and cursor address) read
1	—	0	0	1	Data (display data and parameter) write
1	—	1	0	1	Command write (code only)

6.2 Interfaces with the MPU (Reference)

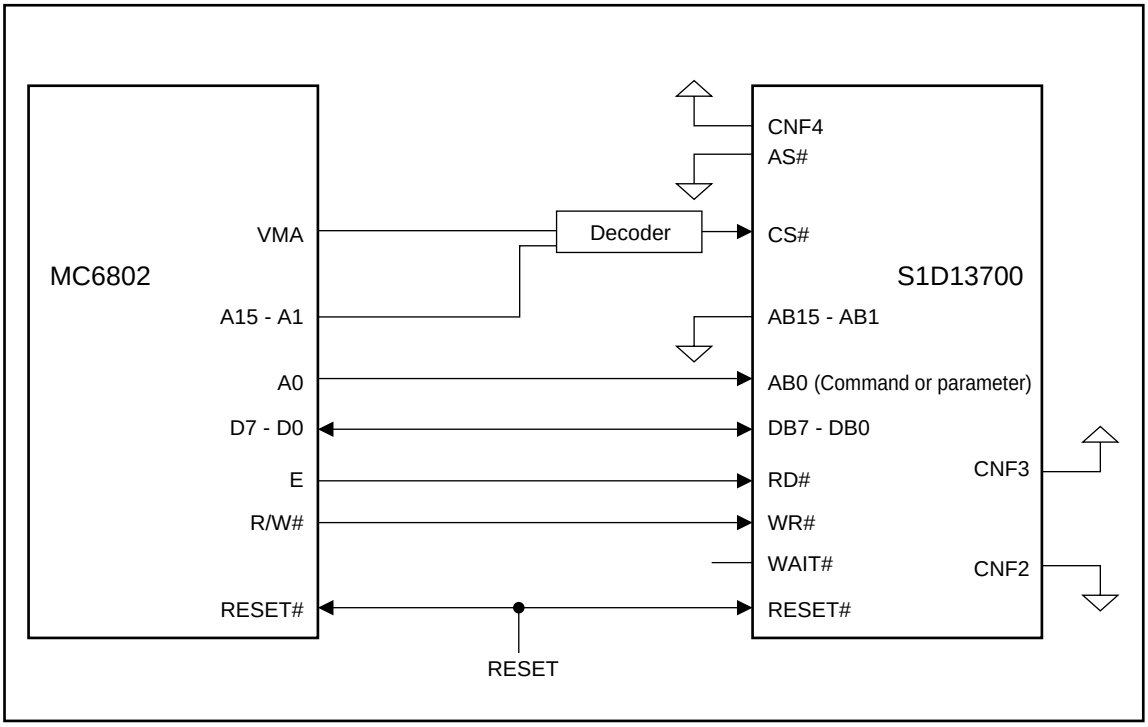
Z80 System Block Diagram (Indirect)



Z80 System Block Diagram (direct)

NOT SUPPORT

MC6802 System Block Diagram (Indirect)

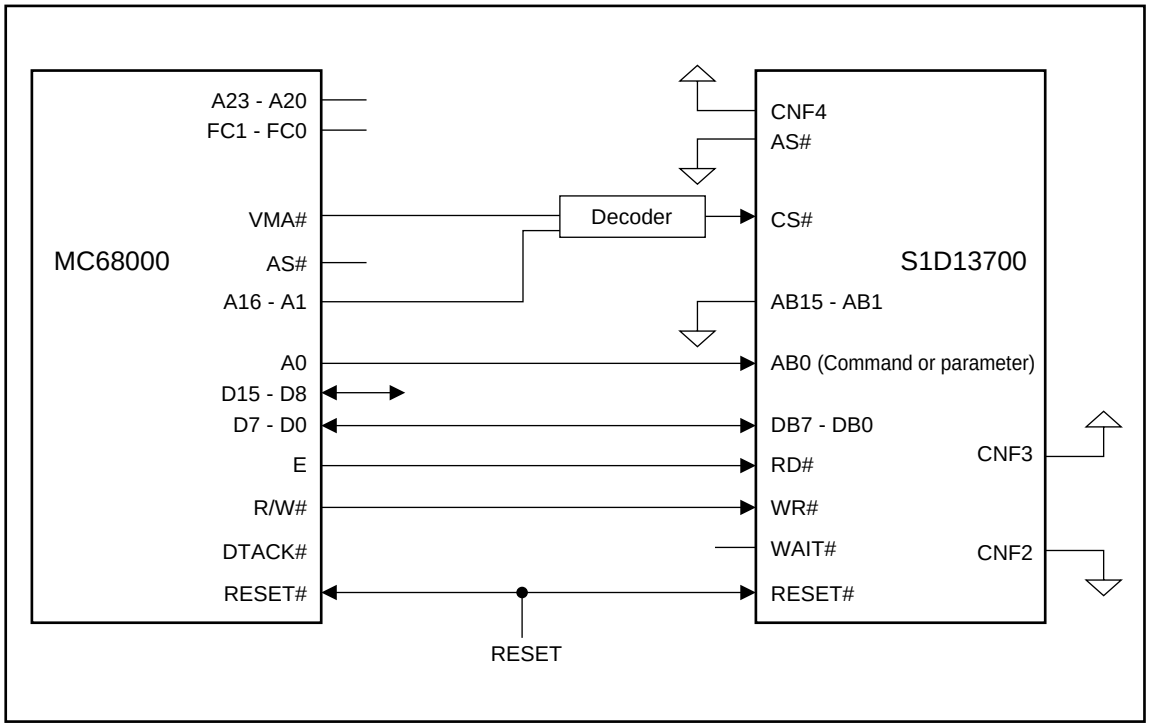


MC6802 System Block Diagram (direct)

NOT SUPPORT

MC68000 System Block Diagram (Indirect)

6800 I/F (Synchronous)



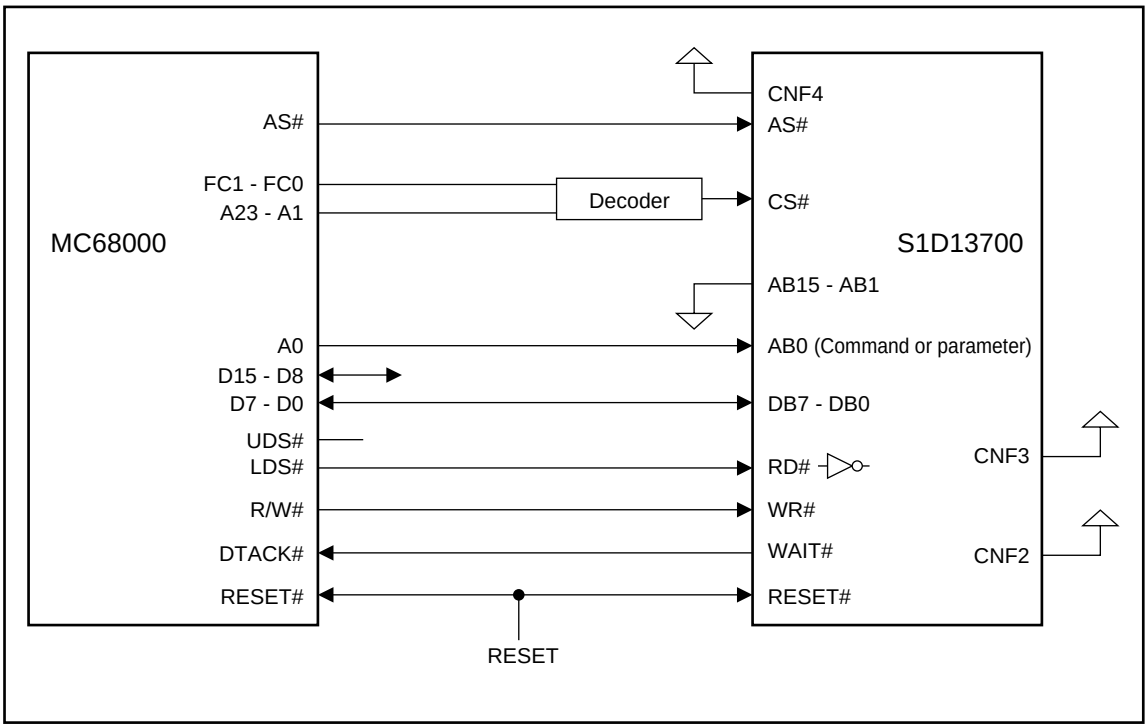
MC68000 System Block Diagram (direct)

6800 I/F (Synchronous)

NOT SUPPORT

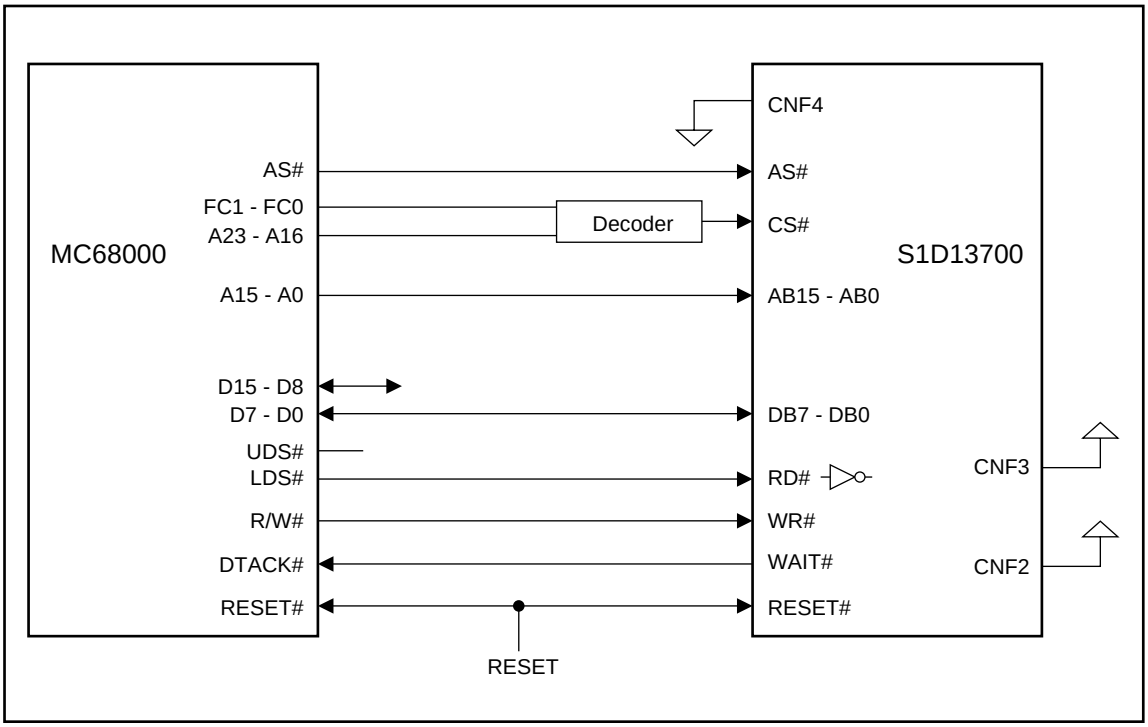
MC68000 System Block Diagram (Indirect)

6800 I/F (Asynchronous)

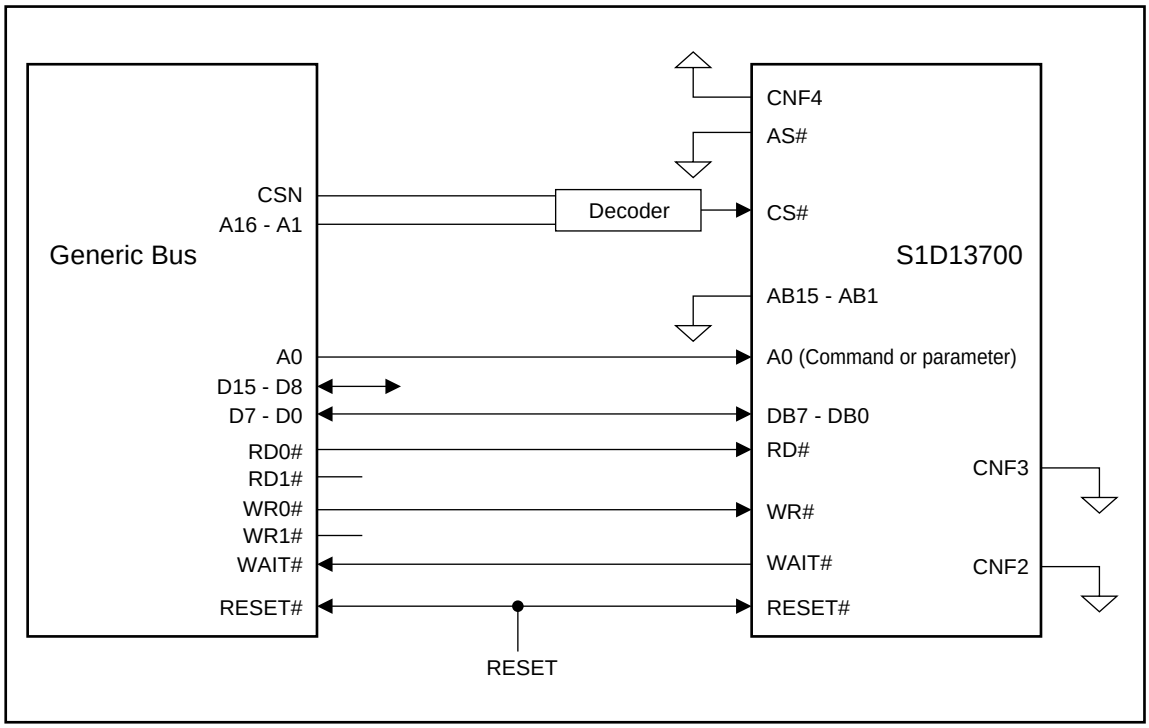


MC68000 System Block Diagram (direct)

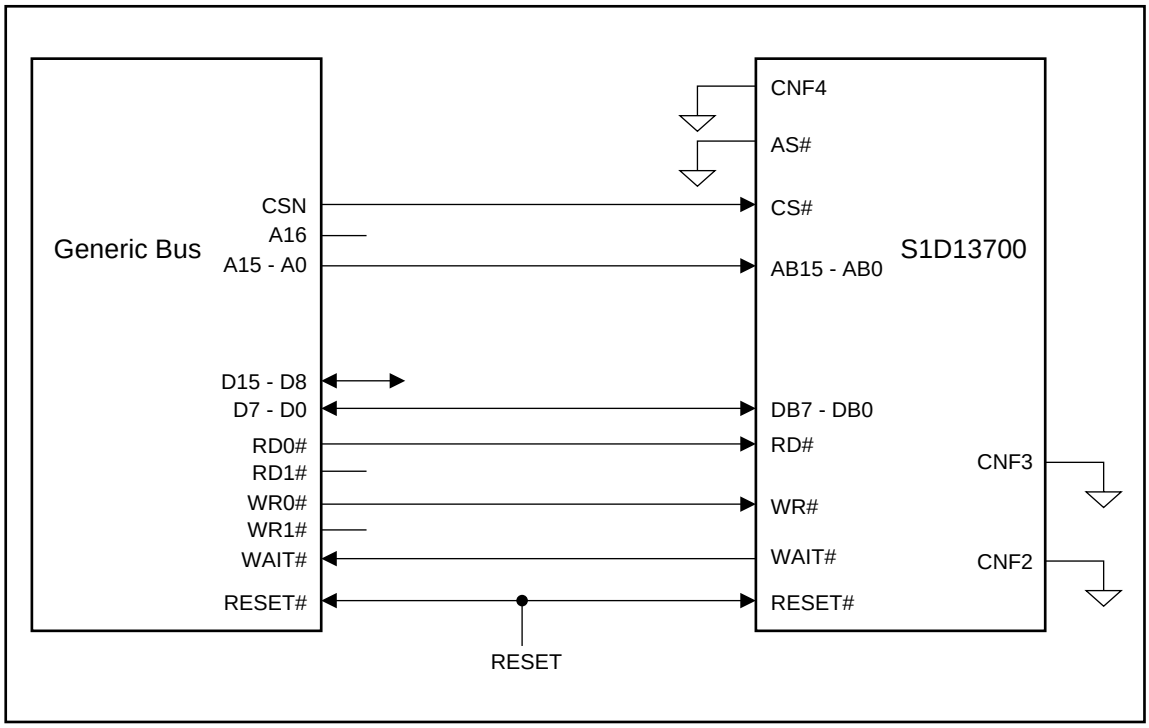
6800 I/F (Asynchronous)



Generic Bus System Block Diagram (Indirect)



Generic Bus System Block Diagram (direct)



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