SII

S-93S46A/56A/66A

150°C OPERATION 3-WIRE SERIAL E^{2}PROM FOR AUTOMOTIVE

www.sii-ic.com

Rev.2.1_00

This IC is a high temperature operation 3-wire serial E^{2}PROM for automotive components. This IC has the capacity of 1 K-bit, 2 K-bit and 4 K-bit, and the organization is 64 words × 16-bit, 128 words × 16-bit and 256 words × 16-bit, respectively. Sequential read is available, at which time addresses are automatically incremented in 16-bit blocks. The communication method is by the Microwire bus.

Caution **Before using the product in automobile control unit or medical equipment, contact to SII is indispensable. This IC is regulated by the relevant Japanese laws and regulations, and may not be exported from Japan without Japanese government approval.**

■ Features

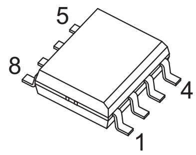
- Operation voltage range
  - Read: 4.0 V to 5.5 V (Ta = –40°C to +150°C)
  - Write: 4.0 V to 5.5 V (Ta = –40°C to +150°C)
- Operation frequency: 1 MHz (4.5 V to 5.5 V, Ta = –40°C to +150°C)
- Write time: 10.0 ms max.
- Sequential read
- Write protect function during the low power supply voltage
- Function to protect against write due to erroneous instruction recognition
- CMOS schmitt input (CS, SK)
- Endurance*1: 2×10^5 cycle / word*2 (Ta = +150°C)
- Data retention: 100 years (Ta = +25°C)
  50 years (Ta = +125°C)
  20 years (Ta = +150°C)
- Memory capacity
  - S-93S46A: 1 K-bit
  - S-93S56A: 2 K-bit
  - S-93S66A: 4 K-bit
- Initial delivery state: FFFFh
- Burn-in specification: Wafer level burn-in
- Operation temperature range: Ta = –40°C to +150°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 in process*3

***1.** Refer to "**■ Endurance**" for details.
***2.** For each address (Word: 16-bit)
***3.** Contact our sales office for details.

Remark Refer to "**3. Product name list**" in "**■ Product Name Structure**" for details of package and product.

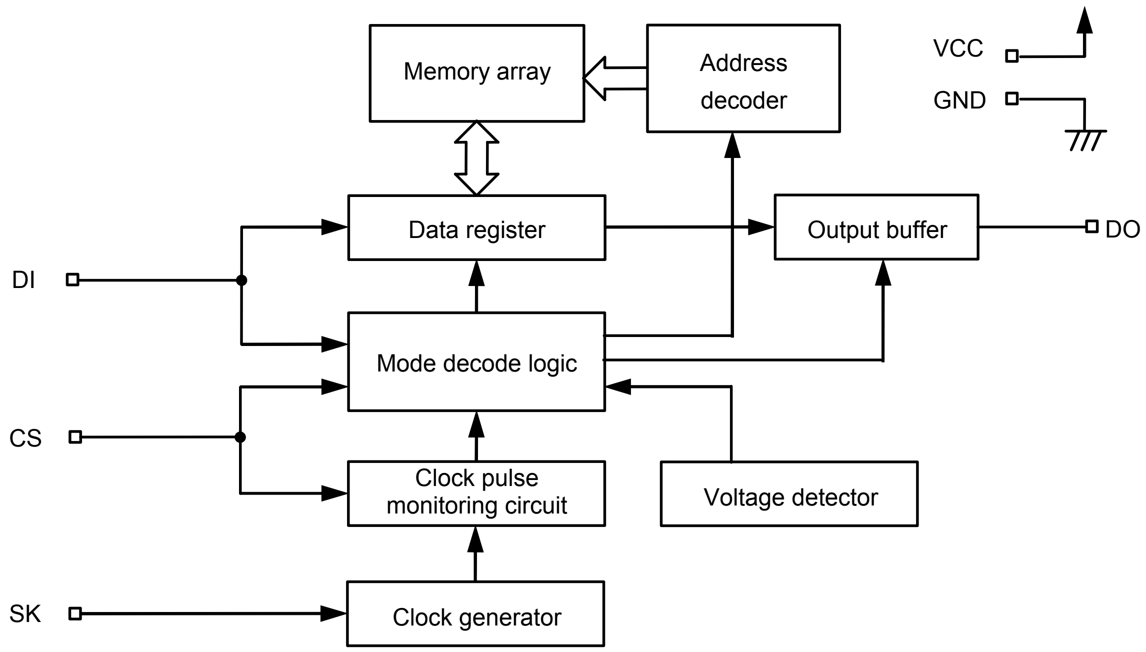
■ Package

- 8-Pin SOP (JEDEC)



(5.0 × 6.0 × t1.75 mm)

■ Block Diagram



■ AEC-Q100 in Process

Contact our sales office for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name

S-93SxxA 0 S - J8T2 U D

- D — Burn-in specification
  - D: Wafer level burn-in
- U — Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- J8T2 — Package name (abbreviation) and IC packing specification*1
  - J8T2: 8-Pin SOP (JEDEC), Tape
- S — Operation temperature
  - S: Ta = –40°C to +150°C
- 0 — Fixed
- S-93SxxA — Product name
  - S-93S46A: 1 K-bit
  - S-93S56A: 2 K-bit
  - S-93S66A: 4 K-bit

***1.** Refer to the tape drawing.

2. Package

Package Name	Dimension	Tape	Reel
8-Pin SOP (JEDEC)	FJ008-A-P-SD	FJ008-D-C-SD	FJ008-D-R-S1

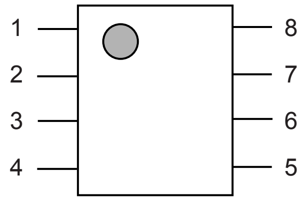
3. Product name list

Product Name	Capacity	Package Name
S-93S46A0S-J8T2UD	1 K-bit	8-Pin SOP (JEDEC)
S-93S56A0S-J8T2UD	2 K-bit	8-Pin SOP (JEDEC)
S-93S66A0S-J8T2UD	4 K-bit	8-Pin SOP (JEDEC)

■ Pin Configuration

1. 8-Pin SOP (JEDEC)

Top view



Pin No.	Symbol	Description
1	CS	Chip select input
2	SK	Serial clock input
3	DI	Serial data input
4	DO	Serial data output
5	GND	Ground
6	TEST*1	Test
7	NC	No connection
8	VCC	Power supply

***1.** Connect to GND or the VCC pin. Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

Remark This IC is wafer level burn-in specification.

■ Absolute Maximum Ratings

Table 1

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{CC}	−0.3 to +6.5	V
Input voltage	V_{IN}	−0.3 to +6.5	V
Output voltage	V_{OUT}	−0.3 to V_{CC}	V
Operation ambient temperature	T_{opr}	−40 to +150	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 2

Item	Symbol	Condition	Ta = −40°C to +150°C		Unit
			Min.	Max.	
Power supply voltage	V_{CC}	READ, EWDS	4.0	5.5	V
		WRITE, ERASE, WRAL, ERAL, EWEN	4.0	5.5	V
High level input voltage	V_{IH}	–	0.8 × V_{CC}	V_{CC}	V
Low level input voltage	V_{IL}	–	0.0	0.2 × V_{CC}	V

■ Pin Capacitance

Table 3

(Ta = +25°C, f = 1.0 MHz, V_{CC} = 5.0 V)

Item	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V	–	8	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V	–	10	pF

■ Endurance

Table 4

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Endurance	N_W	Ta = −40°C to +85°C	10^6	–	cycle / word*1
		Ta = −40°C to +105°C	8×10^5	–	cycle / word*1
		Ta = −40°C to +125°C	5×10^5	–	cycle / word*1
		Ta = −40°C to +150°C	2×10^5	–	cycle / word*1

***1.** For each address (Word: 16-bit)

■ Data Retention

Table 5

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Data retention	–	Ta = +25°C	100	–	year
		Ta = −40°C to +125°C	50	–	year
		Ta = −40°C to +150°C	20	–	year

■ DC Electrical Characteristics

Table 6

Item	Symbol	Condition	Ta = –40°C to +150°C				Unit
			V_{CC} = 4.0 V to 4.5 V		V_{CC} = 4.5 V to 5.5 V		
			Min.	Max.	Min.	Max.	
Current consumption (read)	I_{CC1}	No load at DO pin	–	0.6	–	1.0	mA

Table 7

Item	Symbol	Condition	Ta = –40°C to +150°C				Unit
			V_{CC} = 4.0 V to 4.5 V		V_{CC} = 4.5 V to 5.5 V		
			Min.	Max.	Min.	Max.	
Current consumption (write)	I_{CC2}	No load at DO pin	–	1.5	–	2.0	mA

Table 8

Item	Symbol	Condition	Ta = –40°C to +150°C				Unit
			V_{CC} = 4.0 V to 4.5 V		V_{CC} = 4.5 V to 5.5 V		
			Min.	Max.	Min.	Max.	
Standby current consumption	I_{SB}	CS = GND, DO = Open, Other input pins are V_{CC} or GND	–	20	–	25	μA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	–	2.0	–	2.0	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	–	2.0	–	2.0	μA
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	–	0.6	V
		I_{OL} = 100 μA	–	0.2	–	0.2	V
High level output voltage	V_{OH}	I_{OH} = –400 μA	–	–	2.4	–	V
		I_{OH} = –100 μA	V_{CC} – 0.3	–	V_{CC} – 0.3	–	V
		I_{OH} = –10 μA	V_{CC} – 0.2	–	V_{CC} – 0.2	–	V
Data hold voltage of write enable latch	V_{DH}	Only program disable mode	1.5	–	1.5	–	V

■ AC Electrical Characteristics

Table 9 Measurement Conditions

Input pulse voltage	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$
Output reference voltage	$0.5 \times V_{CC}$
Output load	100 pF

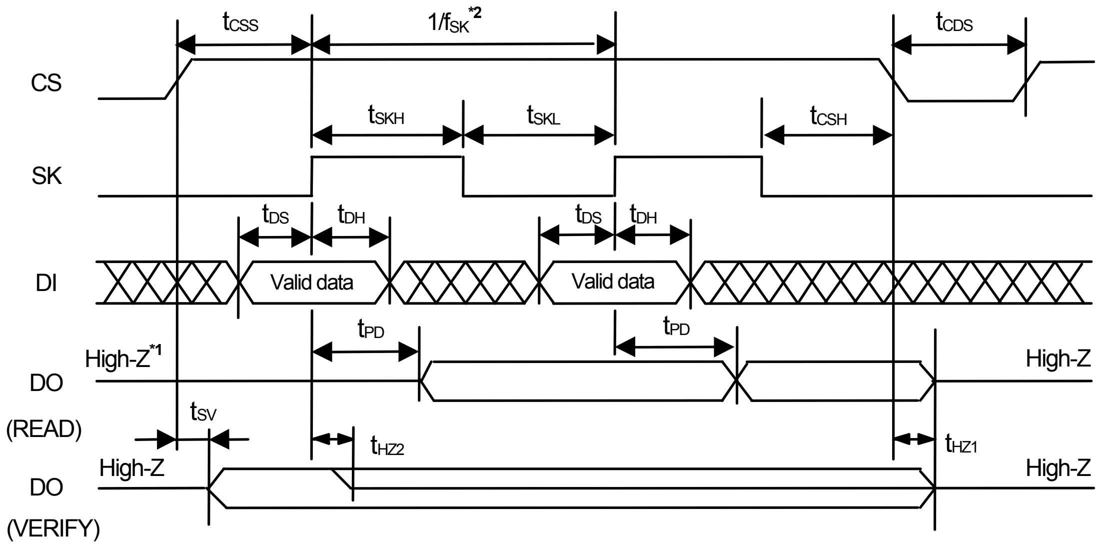
Table 10

Item	Symbol	Ta = –40°C to +150°C				Unit
		V_{CC} = 4.0 V to 5.5 V		V_{CC} = 4.5 V to 5.5 V		
		Min.	Max.	Min.	Max.	
CS pin setup time	t_{CSS}	0.4	–	0.2	–	μs
CS pin hold time	t_{CSH}	0	–	0	–	μs
CS pin deselect time	t_{CDS}	0.2	–	0.2	–	μs
Data setup time	t_{DS}	0.2	–	0.1	–	μs
Data hold time	t_{DH}	0.2	–	0.1	–	μs
Output delay time	t_{PD}	–	1.2	–	0.6	μs
Clock frequency*1	f_{SK}	0	0.5	0	1.0	MHz
Clock pulse width	t_{SKH}, t_{SKL}	0.5	–	0.2	–	μs
Output disable time	t_{HZ1}, t_{HZ2}	0	0.5	0	0.2	μs
Output enable time	t_{SV}	0	0.5	0	0.15	μs

***1.** The clock cycle of the SK clock (frequency f_{SK}) is $1/f_{SK}$ μs. This clock cycle is determined by a combination of several AC characteristics. Note that the clock cycle cannot be set as $(1/f_{SK}) = t_{SKL}$ (min.) + t_{SKH} (min.) by minimizing the SK clock cycle time.

Table 11

Item	Symbol	Ta = –40°C to +150°C			Unit
		V_{CC} = 4.0 V to 5.5 V			
		Min.	Typ.	Max.	
Write time	t_{PR}	–	4.0	10.0	ms



***1.** Indicates high impedance.
***2.** $1/f_{SK}$ is the SK clock cycle. This clock cycle is determined by a combination of several AC characteristics. Note that the clock cycle cannot be set as $(1/f_{SK}) = t_{SKL}$ (min.) + t_{SKH} (min.) by minimizing the SK clock cycle time.

Figure 1 Timing Chart

■ Initial Delivery State

Initial delivery state of all addresses is "FFFFh".

■ Instruction Sets

1. S-93S46A

Table 12 Instruction Set

Instruction	Start Bit	Operation Code		Address						Data
SK input clock	1	2	3	4	5	6	7	8	9	10 to 25
READ (Data read)	1	1	0	A5	A4	A3	A2	A1	A0	D15 to D0 output*1
WRITE (Data write)	1	0	1	A5	A4	A3	A2	A1	A0	D15 to D0 input
ERASE (Data erase)	1	1	1	A5	A4	A3	A2	A1	A0	–
WRAL (Chip write)	1	0	0	0	1	X	X	X	X	D15 to D0 input
ERAL (Chip erase)	1	0	0	1	0	X	X	X	X	–
EWEN (Write enable)	1	0	0	1	1	X	X	X	X	–
EWDS (Write disable)	1	0	0	0	0	X	X	X	X	–

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

Remark X = Don't care.

2. S-93S56A

Table 13 Instruction Set

Instruction	Start Bit	Operation Code		Address								Data
SK input clock	1	2	3	4	5	6	7	8	9	10	11	12 to 27
READ (Data read)	1	1	0	X	A6	A5	A4	A3	A2	A1	A0	D15 to D0 output*1
WRITE (Data write)	1	0	1	X	A6	A5	A4	A3	A2	A1	A0	D15 to D0 input
ERASE (Data erase)	1	1	1	X	A6	A5	A4	A3	A2	A1	A0	–
WRAL (Chip write)	1	0	0	0	1	X	X	X	X	X	X	D15 to D0 input
ERAL (Chip erase)	1	0	0	1	0	X	X	X	X	X	X	–
EWEN (Write enable)	1	0	0	1	1	X	X	X	X	X	X	–
EWDS (Write disable)	1	0	0	0	0	X	X	X	X	X	X	–

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

Remark X = Don't care.

3. S-93S66A

Table 14 Instruction Set

Instruction	Start Bit	Operation Code		Address								Data
SK input clock	1	2	3	4	5	6	7	8	9	10	11	12 to 27
READ (Data read)	1	1	0	A7	A6	A5	A4	A3	A2	A1	A0	D15 to D0 output*1
WRITE (Data write)	1	0	1	A7	A6	A5	A4	A3	A2	A1	A0	D15 to D0 input
ERASE (Data erase)	1	1	1	A7	A6	A5	A4	A3	A2	A1	A0	–
WRAL (Chip write)	1	0	0	0	1	X	X	X	X	X	X	D15 to D0 input
ERAL (Chip erase)	1	0	0	1	0	X	X	X	X	X	X	–
EWEN (Write enable)	1	0	0	1	1	X	X	X	X	X	X	–
EWDS (Write disable)	1	0	0	0	0	X	X	X	X	X	X	–

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

Remark X = Don't care.

■ Operation

All instructions are executed by inputting the DI pin in synchronization with the rising of the SK pulse after the CS pin goes to "H". An instruction set is input in the order of start bit, instruction, address, and data.
Instruction input finishes when the CS pin goes to "L". "L" must be input to the CS pin between commands during t_{CDS}.
While "L" is being input to the CS pin, this IC is in standby mode, so the SK pin and the DI pin inputs are invalid and no instructions are allowed.

■ Start Bit

A start bit is recognized when the DI pin goes to "H" at the rising of the SK after the CS pin goes to "H". After the CS pin goes to "H", a start bit is not recognized even if the SK pulse is input as long as the DI pin is "L".

1. Dummy clock

The SK clocks input while the DI pin is "L" before a start bit is input are called dummy clocks. Dummy clocks are effective when aligning the number of instruction sets (clocks) sent by the CPU with those required for serial memory operation. For example, when the CPU instruction set is 16 bits, the number of instruction set clocks can be adjusted by inserting the 7-bit dummy clock in S-93S46A and the 5-bit dummy clock in S-93S56A/66A.

2. Start bit input failure

- When the output of the DO pin is "H" during the verify period after a write operation, if "H" is input to the DI pin at the rising of the SK, this IC recognizes that a start bit has been input. To prevent this failure, input "L" to the DI pin during the verify operation period (refer to "**4. 1 Verify operation**").
- When a 3-wire interface is configured by connecting the DI pin and the DO pin, a period in which the data output from the CPU and the serial memory collide may be generated, preventing successful input of the start bit. Take the measures described in "**■ 3-Wire Interface (Direct Connection between DI Pin and DO Pin)**".

3. Reading (READ)

The READ instruction reads data from a specified address.
After the CS pin goes to "H", input an instruction in the order of the start bit, read instruction, and address. Since the last input address (A_0) has been latched, the output status of the DO pin changes from "High-Z" to "L", which is held until the next rising of the SK. 16-bit data starts to be output in synchronization with the next rising of the SK.

3. 1 Sequential read

After the 16-bit data at the specified address has been output, inputting the SK while the CS pin is "H" automatically increments the address, and causes the 16-bit data at the next address to be output sequentially. The above method makes it possible to read the data in the whole memory space. The last address (A_n ••• A_1 A_0 = 1 ••• 1 1) rolls over to the top address (A_n ••• A_1 A_0 = 0 ••• 0 0).

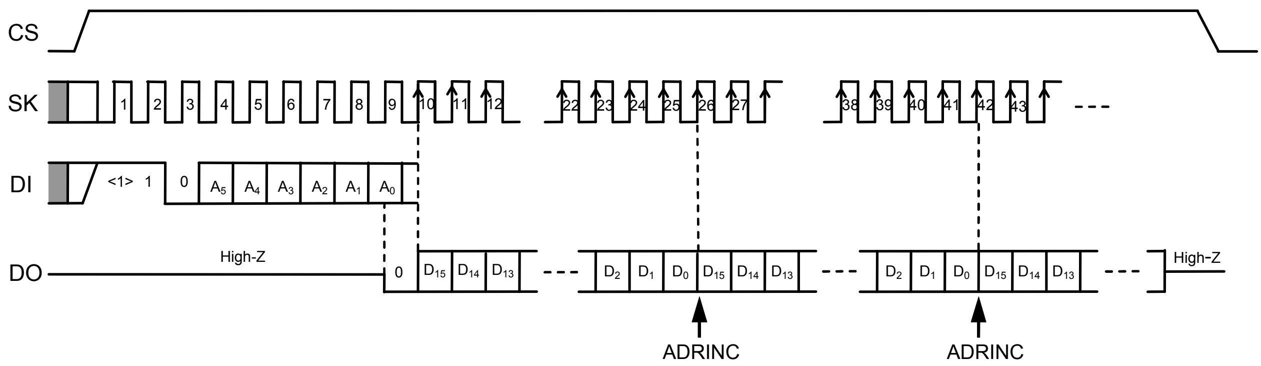


Figure 2 Read Timing (S-93S46A)

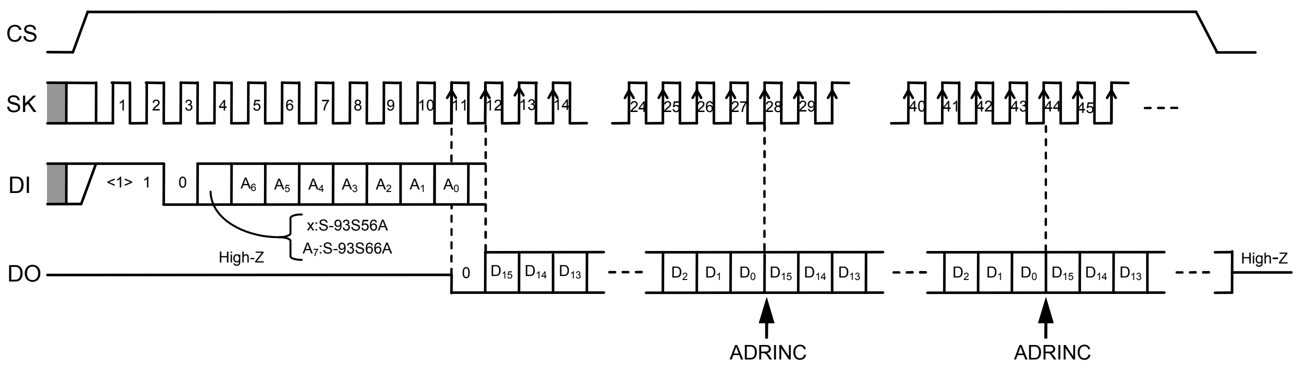


Figure 3 Read Timing (S-93S56A/66A)

4. Writing (WRITE, ERASE, WRAL, ERAL)

A write operation includes four write instructions: data write (WRITE), data erase (ERASE), chip write (WRAL), and chip erase (ERAL).
A write instruction (WRITE, ERASE, WRAL, ERAL) starts a write operation to the memory cell when "L" is input to the CS pin after a specified number of clocks have been input. The SK pin and the DI pin inputs are invalid during the write period, so do not input an instruction.
Input an instruction while the output status of the DO pin is "H" or "High-Z".
A write operation is valid only in program enable mode (refer to "**5. Write enable (EWEN) / write disable (EWDS)**").

4. 1 Verify operation

A write operation executed by any instruction is completed within 8 ms (write time t_{PR}: typically 4 ms), so if the completion of the write operation is recognized, the write cycle can be minimized. A sequential operation to confirm the status of a write operation is called a verify operation.

4. 1. 1 Operation method

After the write operation has started (CS pin = "L"), the status of the write operation can be verified by confirming the output status of the DO pin by inputting "H" to the CS pin again. This sequence is called a verify operation, and the period that "H" is input to the CS pin after the write operation has started is called the verify operation period.

- DO pin = "L": Writing in progress (busy)
- DO pin = "H": Writing completed (ready)

4. 1. 2 Operation example

There are two methods to perform a verify operation: Waiting for a change in the output of the DO pin while keeping the CS pin "H", or suspending the verify operation (CS pin = "L") once and then performing it again to verify the output of the DO pin. The latter method allows the CPU to perform other processing during the wait period, allowing an efficient system to be designed.

Caution 1. Input "L" to the DI pin during a verify operation.
2. If "H" is input to the DI pin at the rising of the SK when the output status of the DO pin is "H", this IC latches the instruction assuming that a start bit has been input. In this case, note that the DO pin immediately enters "High-Z".

4. 2 Writing data (WRITE)

To write 16-bit data to a specified address, change the CS pin to "H" and then input the WRITE instruction, address, and 16-bit data following the start bit. The write operation starts when the CS pin goes to "L". There is no need to set the data to "1" before writing. When the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the WRITE instruction. For details of the clock pulse monitoring circuit, refer to "■ **Function to Protect Against Write due to Erroneous Instruction Recognition**".

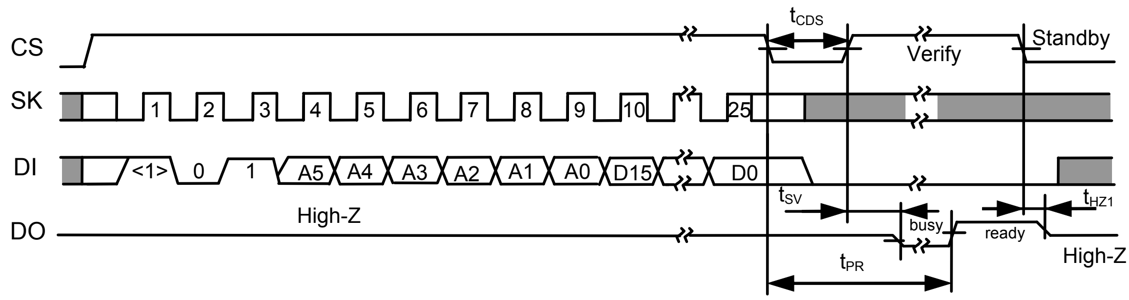


Figure 4 Data Write Timing (S-93S46A)

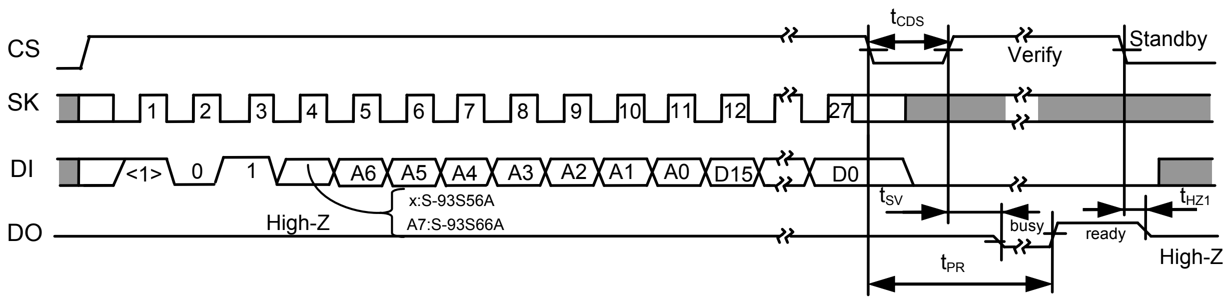


Figure 5 Data Write Timing (S-93S56A/66A)

4. 3 Erasing data (ERASE)

To erase 16-bit data at a specified address, set all 16 bits of the data to "1", change the CS pin to "H", and then input the ERASE instruction and address following the start bit. There is no need to input data. The data erase operation starts when the CS pin goes to "L". When the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the ERASE instruction. For details of the clock pulse monitoring circuit, refer to "■ **Function to Protect Against Write due to Erroneous Instruction Recognition**".

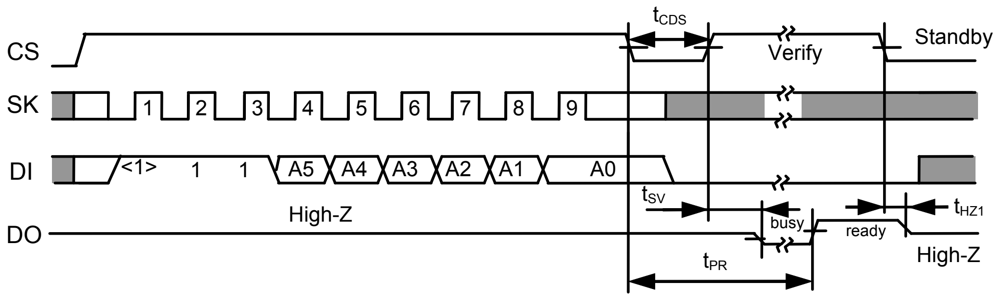


Figure 6 Data Erase Timing (S-93S46A)

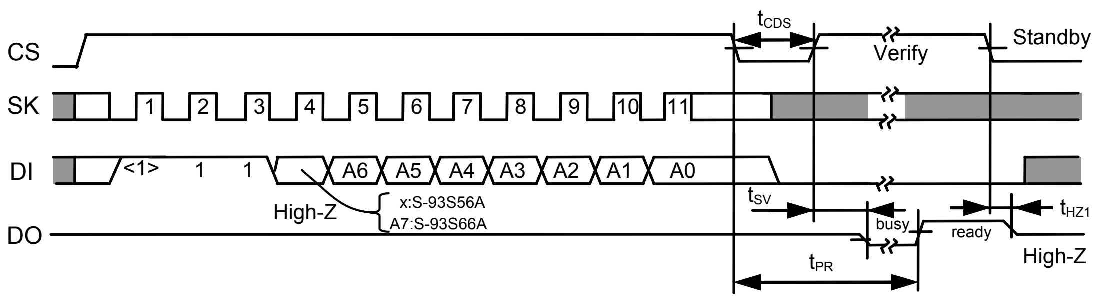


Figure 7 Data Erase Timing (S-93S56A/66A)

4. 4 Writing to chip (WRAL)

To write the same 16-bit data to the entire memory address space, change the CS pin to "H", and then input the WRAL instruction, an address, and 16-bit data following the start bit. Any address can be input. The write operation starts when the CS pin goes to "L". There is no need to set the data to "1" before writing. When the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the WRAL instruction. For details of the clock pulse monitoring circuit, refer to "■ **Function to Protect Against Write due to Erroneous Instruction Recognition**".

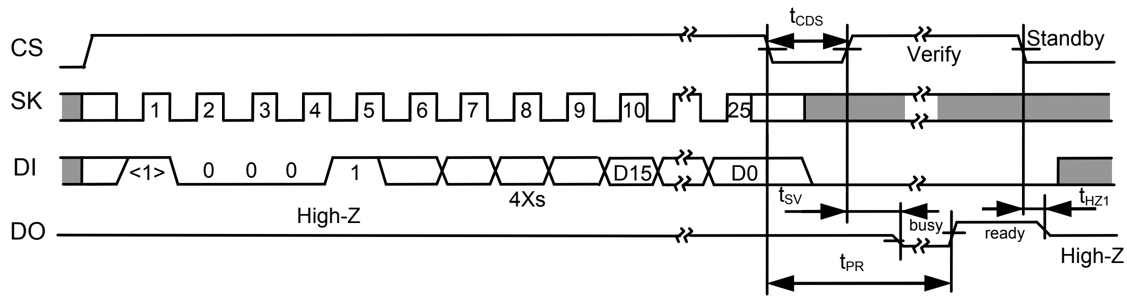


Figure 8 Chip Write Timing (S-93S46A)

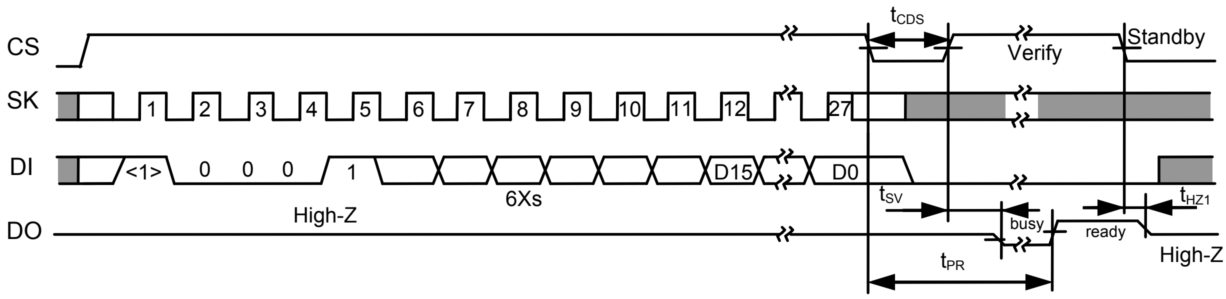


Figure 9 Chip Write Timing (S-93S56A/66A)

4. 5 Erasing chip (ERAL)

To erase the data of the entire memory address space, set all the data to "1", change the CS pin to "H", and then input the ERAL instruction and an address following the start bit. Any address can be input. There is no need to input data. The chip erase operation starts when the CS pin goes to "L". When the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the ERAL instruction. For details of the clock pulse monitoring circuit, refer to "■ **Function to Protect Against Write due to Erroneous Instruction Recognition**".

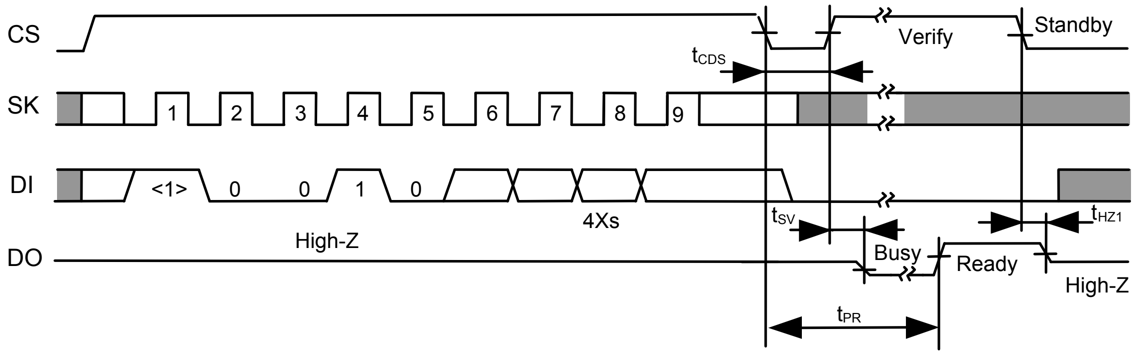


Figure 10 Chip Erase Timing (S-93S46A)

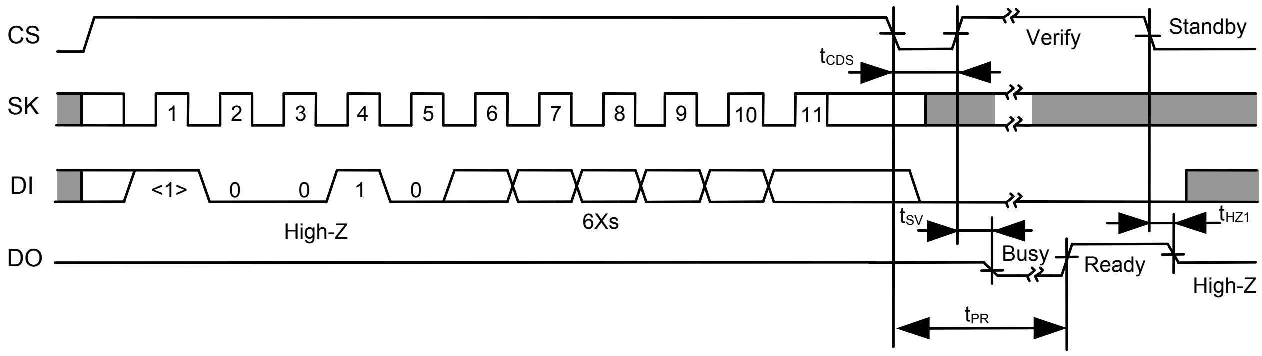


Figure 11 Chip Erase Timing (S-93S56A/66A)

5. Write enable (EWEN) / write disable (EWDS)

The EWEN instruction is an instruction that enables a write operation. The status in which a write operation is enabled is called the program enable mode.
The EWDS instruction is an instruction that disables a write operation. The status in which a write operation is disabled is called the program disable mode.
After the CS pin goes to "H", input an instruction in the order of the start bit, EWEN or EWDS instruction, and address (optional). Each mode becomes valid by inputting "L" to the CS pin after the last address (optional) has been input.

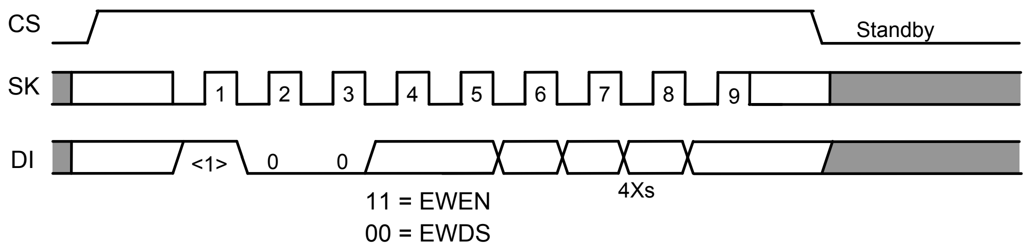


Figure 12 Write Enable / Disable Timing (S-93S46A)

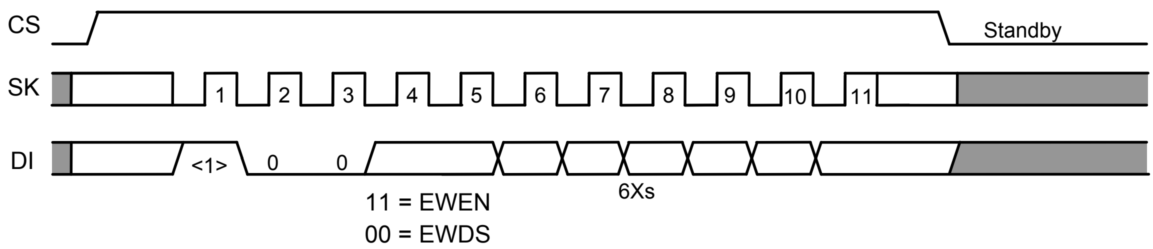


Figure 13 Write Enable / Disable Timing (S-93S56A/66A)

Remark It is recommended to execute an EWDS instruction for preventing an incorrect write operation if a write instruction is erroneously recognized when executing instructions other than write instruction, and immediately after power-on and before power-off.

■ Write Protect Function during the Low Power Supply Voltage

This IC provides a built-in detection circuit to detect a low power supply voltage. When the power supply voltage is low or at power-on, the write instructions (WRITE, ERASE, WRAL, and ERAL) are cancelled, and the write disable (EWDS) status is automatically set. The detection voltage is 1.75 V typ., the release voltage is 2.05 V typ., and there is a hysteresis of about 0.3 V (refer to **Figure 14**). Therefore, when a write operation is performed after the power supply voltage has dropped and then risen again up to the level at which writing is possible, a write enable instruction (EWEN) must be sent before a write instruction (WRITE, ERASE, WRAL, or ERAL) is executed.
When the power supply voltage drops during a write operation, the data being written to an address at that time is not guaranteed.

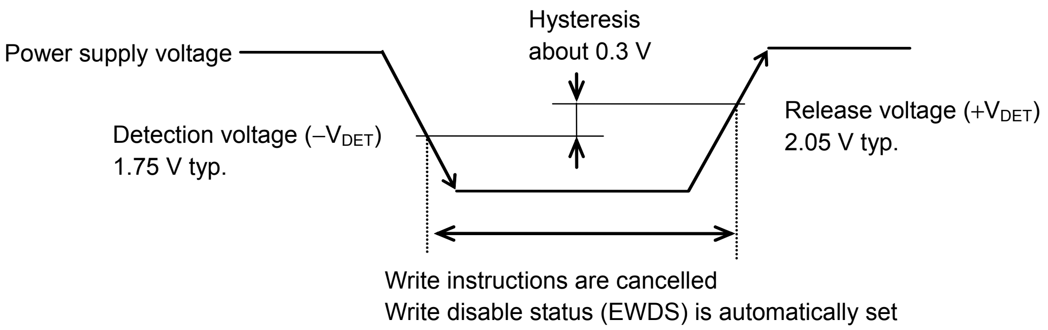
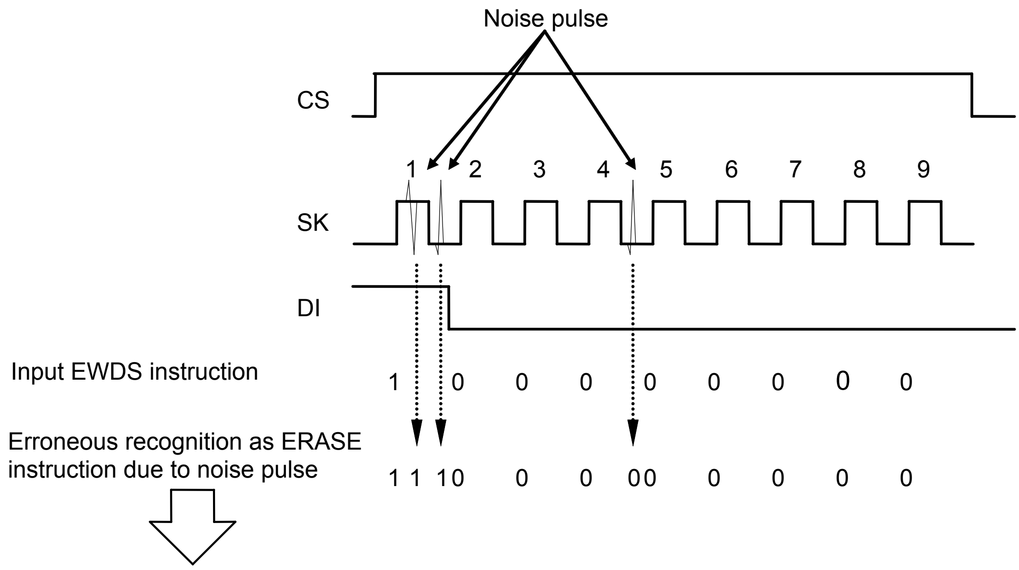


Figure 14 Operation during the Low Power Supply Voltage

■ Function to Protect Against Write due to Erroneous Instruction Recognition

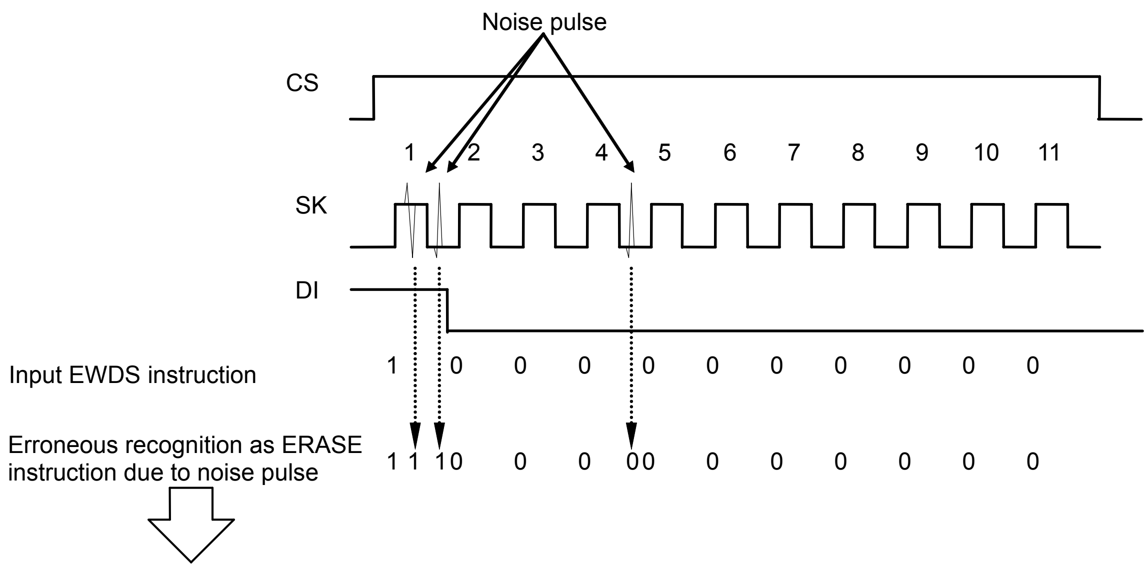
This IC provides a built-in clock pulse monitoring circuit which is used to prevent an erroneous write operation by canceling write instructions (WRITE, ERASE, WRAL, and ERAL) recognized erroneously due to an erroneous clock count caused by the application of noise pulses or double counting of clocks. Instructions are cancelled if a clock pulse whose count other than the one specified for each write instruction (WRITE, ERASE, WRAL, or ERAL) is detected.

Example: Erroneous Recognition of EWDS as ERASE



In products that do not incorporate a clock pulse monitoring circuit, "FFFF" is mistakenly written to address 00h. However the S-93S46A detects the overcount and cancels the instruction without performing a write operation.

Figure 15 Example of Clock Pulse Monitoring Circuit Operation (S-93S46A)



In products that do not incorporate a clock pulse monitoring circuit, "FFFF" is mistakenly written to address 00h. However the S-93S56A/66A detects the overcount and cancels the instruction without performing a write operation.

Figure 16 Example of Clock Pulse Monitoring Circuit Operation (S-93S56A/66A)

■ 3-Wire Interface (Direct Connection between DI Pin and DO Pin)

There are two types of serial interface configurations: a 4-wire interface configured using the CS pin, the SK pin, the DI pin and the DO pin and a 3-wire interface that connects the DI pin and the DO pin.
When the 3-wire interface is employed, a period in which the data output from the CPU and the data output from the serial memory collide may occur, causing a malfunction. To prevent such a malfunction, connect the DI pin and the DO pin of this IC via a resistor (10 kΩ to 100 kΩ) so that the data output from the CPU takes precedence in being input to the DI pin (refer to **Figure 17**).

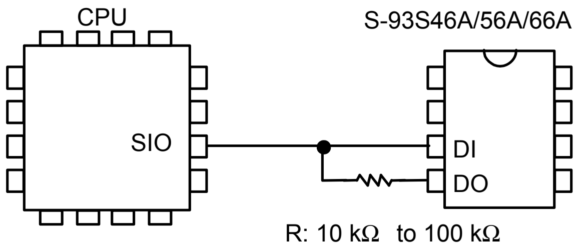


Figure 17 Connection of 3-Wire Interface

■ Input Pin and Output Pin

1. Connection of input pin

All input pins in this IC have the CMOS structure. Do not set these pins in "High-Z" during operation when you design. Especially, set the CS pin to "L" at power-on, power-off, and during standby. The error write does not occur as long as the CS pin is "L". Set the CS pin to GND via a resistor (the pull-down resistor of 10 kΩ to 100 kΩ).
To prevent the error for sure, it is recommended to use equivalent pull-down resistors for input pins other than the CS pin.

2. Equivalent circuit of input pin and output pin

Figure 18, **Figure 19**, **Figure 20** and **Figure 21** show the equivalent circuits of input pins in this IC. None of the input pins incorporate pull-up and pull-down resistors, so special care must be taken when designing to prevent a floating status.
Figure 22 shows the equivalent circuit of the output pin. This pin has the tri-state output of "H" / "L" / "High-Z".
The TEST pin is disconnected from the internal circuit by a switching transistor during normal operation.
As long as the absolute maximum rating is satisfied, the TEST pin and internal circuit will never be connected.

2. 1 Input pin

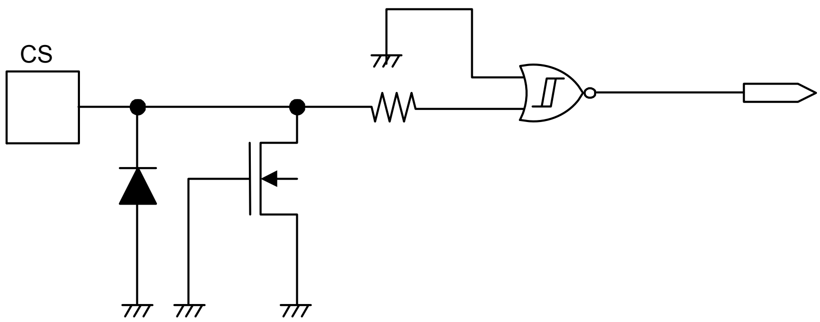


Figure 18 CS Pin

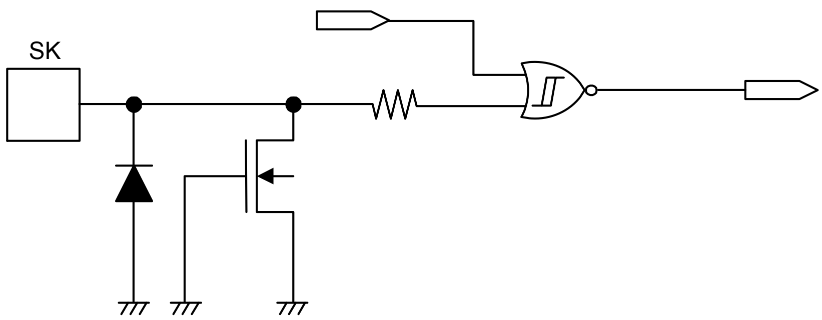


Figure 19 SK Pin

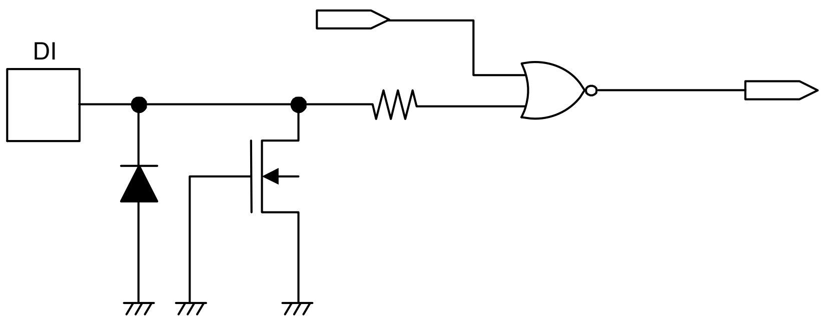


Figure 20 DI Pin

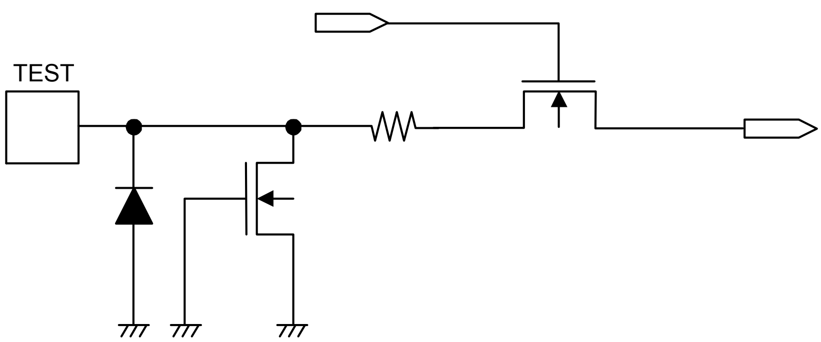


Figure 21 TEST Pin

2. 2 Output pin

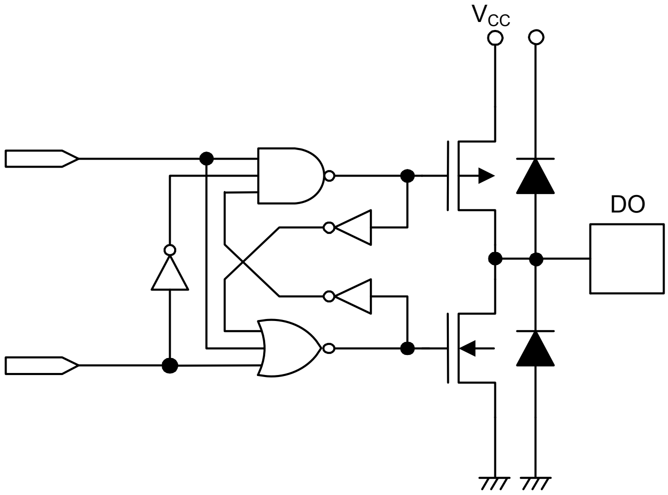


Figure 22 DO Pin

3. Input pin noise suppression time

This IC has a built-in low-pass filter at the SK pin, the DI pin and the CS pin to suppress noise. If the supply voltage is 5.0 V, noise with a pulse width of 20 ns or less at room temperature can be suppressed by the low-pass filter.
Note that noise with a pulse width of more than 20 ns is recognized as a pulse since the noise can not be suppressed if the voltage exceeds V_{IH} / V_{IL}.

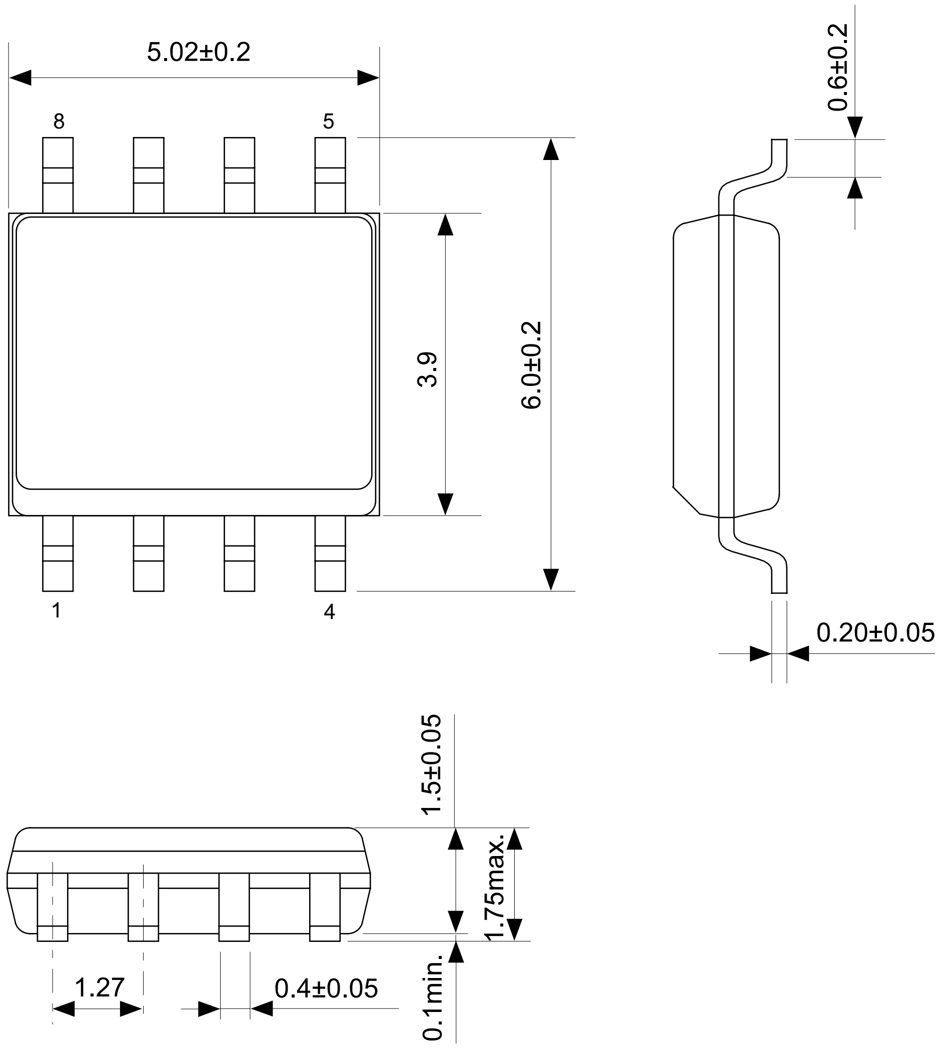
■ Precautions

- Do not operate these ICs in excess of the absolute maximum ratings. Attention should be paid to the power supply voltage, especially. The surge voltage which exceeds the absolute maximum ratings can cause latch-up and malfunction. Perform operations after confirming the detailed operation condition in the data sheet.

- Operations with moisture on this IC's pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking this IC up from low temperature tank during the evaluation. Be sure that not remain frost on this IC's pin to prevent malfunction by short-circuit.
  Also attention should be paid in using on environment, which is easy to dew for the same reason.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.



No. FJ008-A-P-SD-2.1

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No.	FJ008-A-P-SD-2.1
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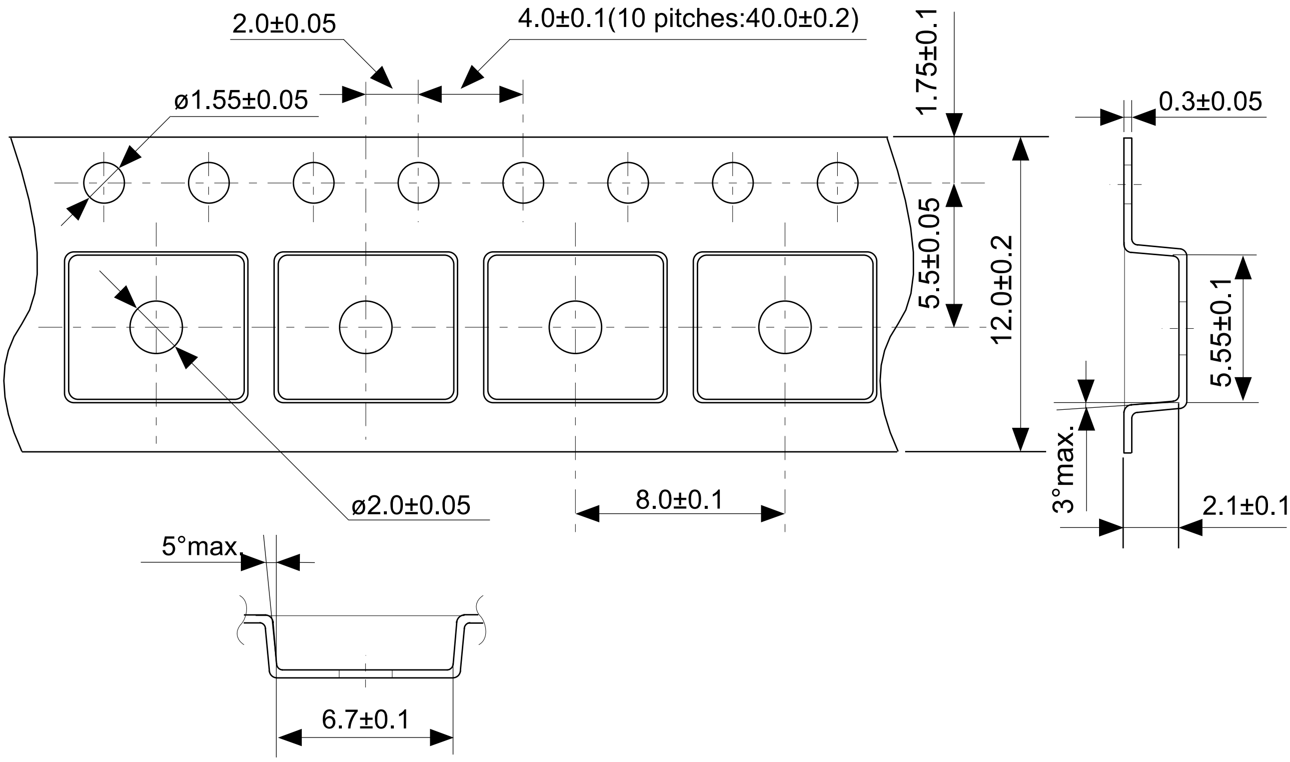
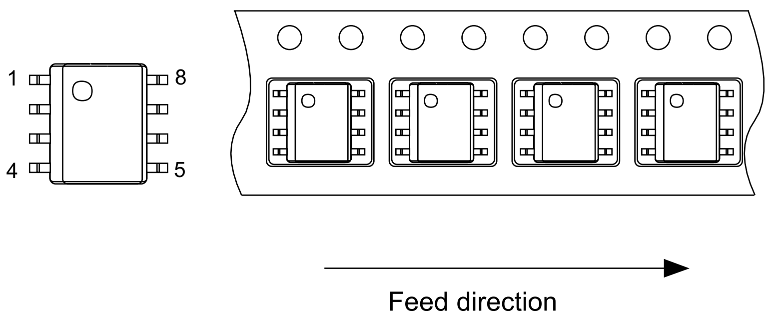
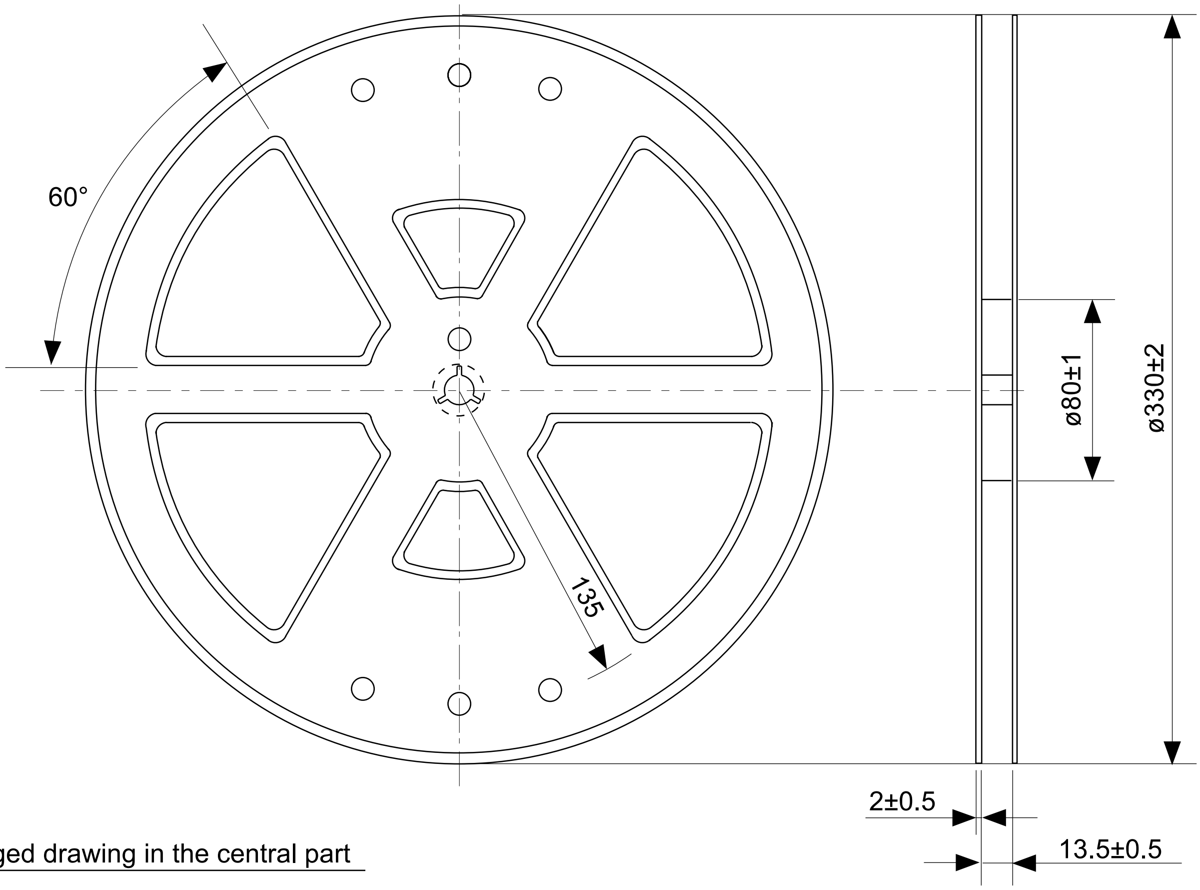
UNIT	mm
Seiko Instruments Inc.	



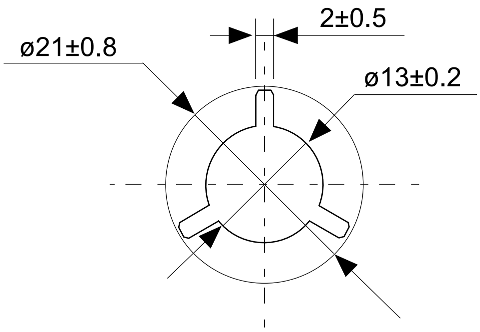


No. FJ008-D-C-SD-1.1

TITLE	SOP8J-D-Carrier Tape
No.	FJ008-D-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FJ008-D-R-S1-1.0

TITLE	SOP8J-D-Reel		
No.	FJ008-D-R-S1-1.0		
SCALE		QTY.	4,000
UNIT	mm		
Seiko Instruments Inc.			