S-8474 Series

WIRELESS POWER TRANSMITTER CONTROL IC

The S-8474 Series is Wireless Power Transmitter Control IC, which is configured with an ON time control circuit, an OFF time control circuit, a reception detection circuit, a UVLO circuit, a high temperature detection circuit, etc.

■ Features

- Power supply voltage: V_{DD} = 4.5 V to 6.5 V
- Current consumption: During operation: I_{SS1} = 200 μA typ.
  During standby: I_{STB} = 3.0 μA max.
- UVLO detection voltage: V_{UVLO-} = 4.1 V typ.
- t_{ON} time is settable by connecting an external resistor to the RTON pin.
- Power saving is possible by intermittent operation during standby time of a receiver module.
  Active time: t_{ACT} = 5.0 ms typ.
  Sleep time: t_{SLEEP} = 25.0 ms typ.
- TH pin detection voltage is selectable: 0.667 V, 0.577 V, 0.500 V, 0.429 V, 0.370 V
- Built-in reception detection circuit
- Status display function: Available by connecting an external LED to the STATUS pin.
  Continuous operation mode: Lighting
  Intermittent operation mode: Lights-out
  High temperature protection mode: Blinking
- Over temperature protection function: Available by connecting a thermistor to the TH pin.
- Operation temperature range: Ta = −40°C to +85°C
- Lead-free (Sn 100%), halogen-free

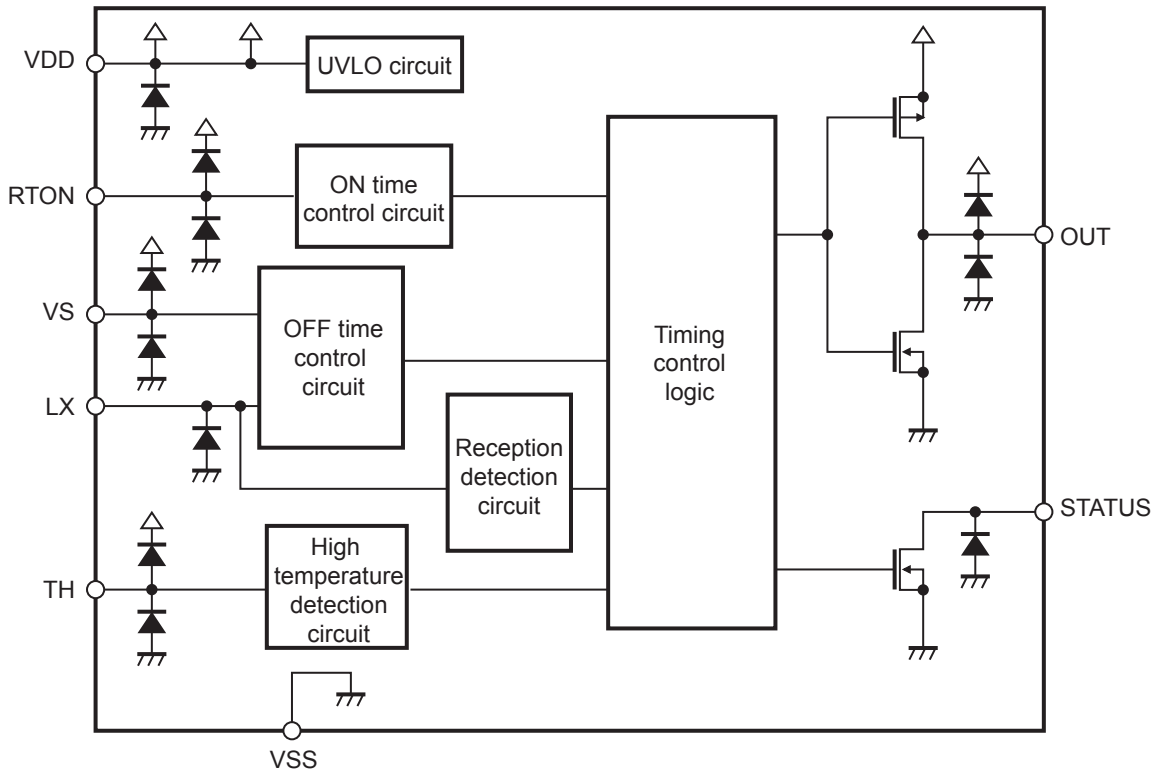
■ Applications

- Device for wireless power
- Small-sized wireless charging system

■ Package

- SNT-8A

■ Block Diagram

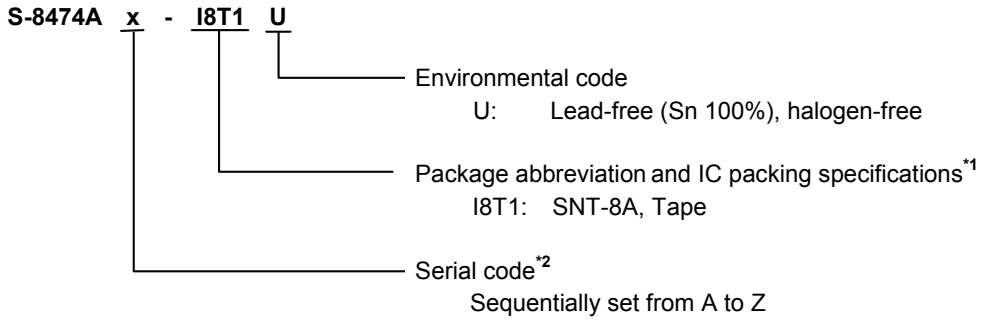


Remark All the diodes shown in the figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

3. Product name list

Table 2

Product Name	TH Pin Detection Voltage*1 [V_{TSD}]
S-8474AC-I8T1U	0.500 V

***1.** TH pin detection voltage is selectable: 0.667 V, 0.577 V, 0.500 V, 0.429 V, 0.370 V

Remark Please contact our sales office for products other than the above.

■ Pin Configuration

1. SNT-8A

Top view

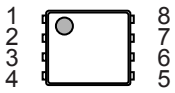


Figure 2

Table 3

Pin No.	Symbol	Description
1	VDD	Power supply voltage pin
2	TH	Thermistor connection pin
3	LX	Input pin for resonance circuit voltage
4	VS	Input pin for resonance circuit power supply voltage
5	STATUS	Output pin for status display
6	RTON	Resistor connection pin for t_{ON} time setting
7	VSS	GND pin
8	OUT	FET gate drive pin for resonance

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DD}	VDD	V_{SS} − 0.3 to V_{SS} + 7.0	V
Input pin voltage	V_{IN}	TH, LX, VS, RTON	V_{SS} − 0.3 to V_{DD} + 0.3	V
Output pin voltage	V_{OUT}	STATUS, OUT	V_{SS} − 0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	−	450[*1]	mW
Operation ambient temperature	T_{opr}	−	−40 to +85	°C
Storage temperature	T_{stg}	−	−40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

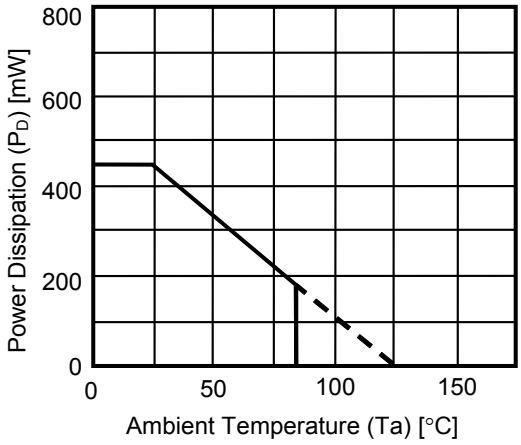


Figure 3 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 5

(V_{DD} = 5.0 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	–	4.5	–	6.5	V
Current consumption during operation	I_{SS1}	–	–	200	300	μA
Current consumption during standby	I_{STB}	V_{DD} = 4.0 V	–	1.0	3.0	μA
UVLO detection voltage	V_{UVLO-}	–	4.0	4.1	4.2	V
UVLO release voltage	V_{UVLO+}	–	4.2	4.3	4.4	V
OUT pin sink current	I_{OUTN}	V_{OUT} = 0.5 V	120	–	–	mA
OUT pin source current	I_{OUTP}	V_{OUT} = V_{DD} – 0.5 V	–	–	–120	mA
STATUS pin Nch driver ON resistance	R_{ONN}	–	–	20	30	Ω
STATUS pin leakage current	I_{LEAKN}	V_{STATUS} = V_{DD}	–	0.1	1.0	μA
LX pin input current "H"	I_{SH_LX}	–	–0.1	–	0.1	μA
LX pin input current "L"	I_{SL_LX}	–	–0.1	–	0.1	μA
VS pin input current "H"	I_{SH_VS}	–	–0.1	–	0.1	μA
VS pin input current "L"	I_{SL_VS}	–	–0.1	–	0.1	μA
TH pin internal resistance	R_{LIN}	–	54.9	61.0	67.1	kΩ
TH pin detection voltage	V_{TSD}	–	V_{TSD} – 0.015	V_{TSD}	V_{TSD} + 0.015	V
t_{ON} time	t_{ON}	R_{TON} = 1.1 MΩ	4.166	4.386	4.606	μs
Active time	t_{ACT}	–	4.5	5.0	5.5	ms
Sleep time	t_{SLEEP}	–	22.5	25.0	27.5	ms
STATUS pin blinking cycle	t_{SW}	–	54	60	66	ms
STATUS pin blinking duty	D_{SW}	–	47.5	50.0	52.5	%

■ Test Circuit

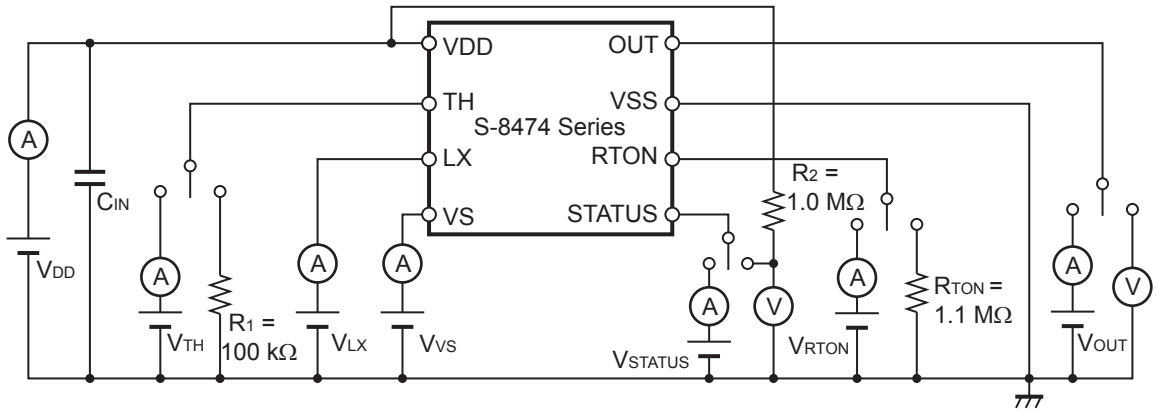


Figure 4

■ Operation

Remark Refer to "■ **Standard Circuit**".

1. Basic operation

1. 1 OUT pin output

(1) After power-on, the power supply voltage (V_{DD}) becomes the UVLO release voltage (V_{UVLO+}) or higher, and a certain period of time elapses. And then, V_{DD} ("H") is output from the OUT pin and an oscillation is started.
(2) V_{DD} output from the OUT pin is maintained only for t_{ON} time (t_{ON}) determined by the resistance connected to the RTON pin.
(3) After the elapse of t_{ON}, V_{SS} ("L") is output from the OUT pin.
The IC holds the period from when V_{SS} is output to when the LX pin voltage exceeds the VS pin voltage (t_m). After that, the OUT pin maintains V_{SS} from when the LX pin voltage drops below the VS pin voltage to when t_m finishes.
(4) After t_m finishes, V_{DD} is output from the OUT pin.
(5) The operations of (2) to (4) are repeated.

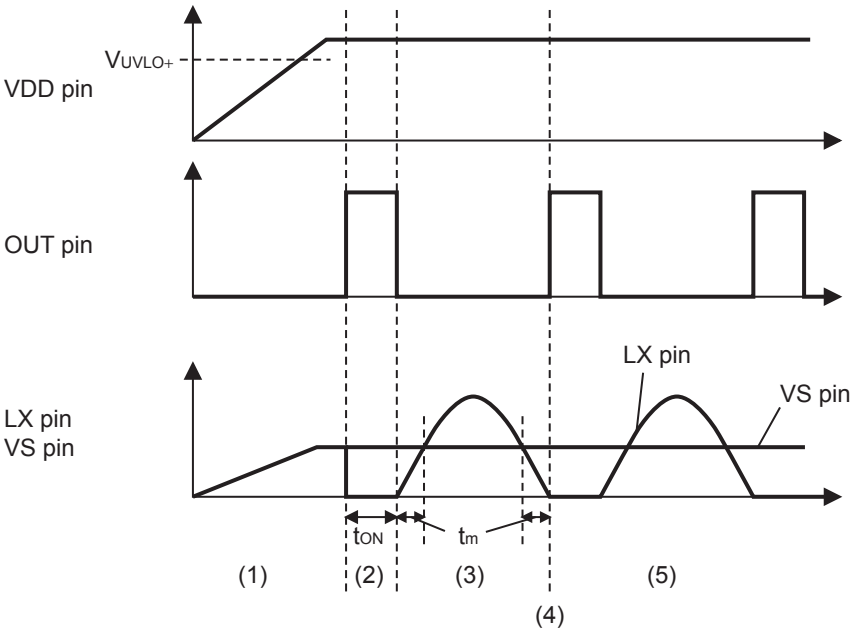


Figure 5

1. 2 Operation modes

The S-8474 Series has two operation modes: continuous operation mode and intermittent operation mode.
As shown in **Figure 6**, the active time (t_{ACT}) and the sleep time (t_{SLEEP}) are repeated alternately.
In the continuous operation mode, the OUT pin output oscillates during both t_{ACT} and t_{SLEEP}.
In the intermittent operation mode, the OUT pin output oscillates during t_{ACT}, and V_{SS} is output during t_{SLEEP}.

Transition of the two operation modes is realized by a reception detection circuit. The reception detection circuit compares peak values of the LX pin voltage waveform and detects a change for approximately 3 ms to 5 ms after t_{ACT} initiation. When there is no change in the peak values of the LX pin voltage waveform, the reception detection circuit changes to a non-detection status, and the mode transitions to the intermittent operation mode. When there is a change, the reception detection circuit changes to a detection status, and the mode transitions to the continuous operation mode.

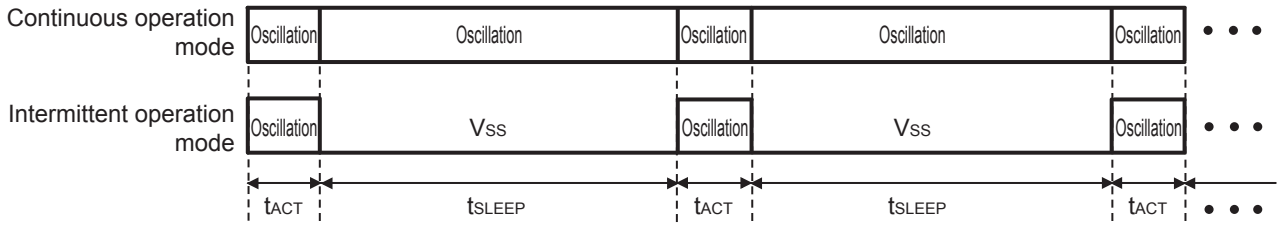


Figure 6

2. UVLO function

The S-8474 Series has a UVLO (under voltage lock out) circuit for avoiding IC malfunctions due to a transient status at power-on or instantaneous power supply voltage drop. If V_{DD} decreases to the UVLO detection voltage (V_{UVLO-}), the S-8474 Series becomes a standby status. In the standby status, the operations of all internal circuits other than the UVLO circuit are stopped, reducing the current consumption. V_{SS} is output from the OUT pin and the STATUS pin changes to "High-Z".
Also, between V_{UVLO+} and V_{UVLO-}, there is a hysteresis width for avoiding malfunctions due to generation of noise etc. in the input voltage.

3. t_{ON} time setting

t_{ON} time can be set to any given value by connecting an external resistor between the RTON pin and the VSS pin. The resistance of the external resistor (R_{TON}) is calculated by the following equation. Set R_{TON} in the range of 500 kΩ to 2.0 MΩ.

$$t_{ON}\ [\mu s] = 3.86 \times R_{TON}\ [M\Omega] + 0.14$$

4. Over temperature protection function

By connecting an external thermistor to the TH pin, a potential over temperature status (due to external component heat generation) can be prevented. When the resistance of the thermistor decreases to the resistance calculated by the following equation (R_{TH}) due to external component heat generation, an over temperature protection function begins to operate, and then the mode changes to a high temperature protection mode. In the high temperature protection mode, the OUT pin output is latched to V_{SS}. However, the other internal circuits operate during the period unlike the standby status, so caution should be exercised. The IC is reset by decreasing V_{DD} to V_{UVLO-} or lower.

$$R_{TH}\ [k\Omega] = \frac{R_{LIN}\ [k\Omega] \times V_{TSD}\ [V]}{(2.5 - V_{TSD}\ [V])}$$

Connect a thermistor between the TH pin and the VSS pin. An NTC thermistor of R = 100 kΩ at Ta = +25°C (R_{25}) is recommended. For example, if an NTC thermistor of R_{25} and $B_{25/50}$ (B constant (25°C/50°C)) = 4250 K is used, the over temperature protection function begins to operate at approximately +70°C when V_{TSD} = 0.500 V. When not using the over temperature protection function, set the TH pin open or connect a resistor of 100 kΩ or greater.

5. Status display function

The S-8474 Series can display the operation status by connecting an external LED to the STATUS pin.
In a continuous operation mode, an Nch driver of the STATUS pin is turned on, "L" is output from the STATUS pin, and the external LED is lighted on. In an intermittent operation mode, the Nch driver of the STATUS pin is turned off, the STATUS pin changes to "High-Z", and the external LED is lighted off.
In a high temperature protection mode, the Nch driver of the STATUS pin is turned on and off repeatedly. Also, "L" and "High-Z" are output from the STATUS pin, the operation is repeated with the STATUS pin blinking cycle (t_{SW}), and the external LED is blinked. When not using the status display function, set the STATUS pin open.

■ Standard Circuit

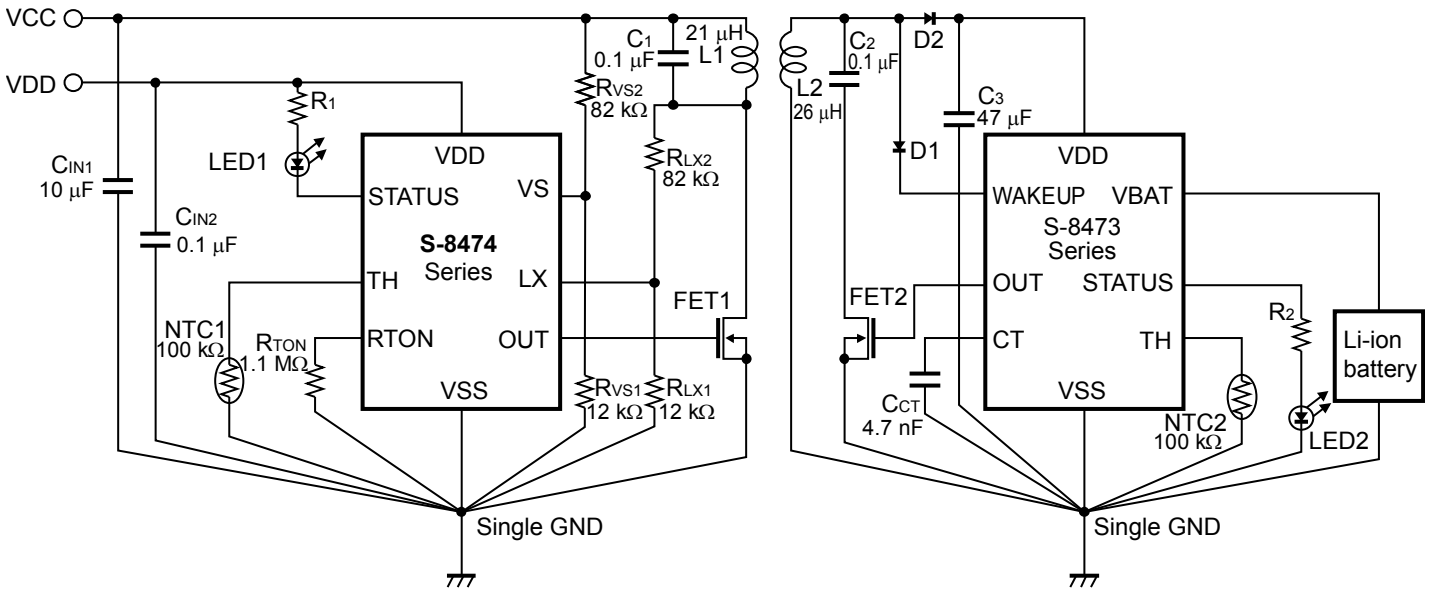


Figure 7

Caution **The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.**

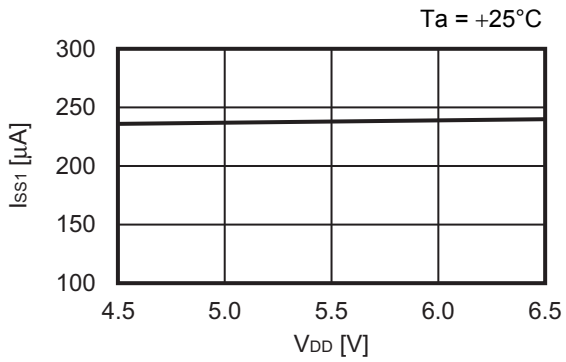
■ Precautions

- For VCC, do not use a power supply which might cause frequency component amplitude of 1 kHz to 110 kHz (LC resonant frequency). It may result in a malfunction.
- To protect from overheat, be sure to connect an NTC thermistor to the TH pin for its use.
- Mount an external resistor, an Nch power MOS FET, etc. as close as possible to the IC so as to make the single GND.
- When the wiring impedance is high, the operation may be unstable due to the resonance circuit or the noise caused by switching of the output pin, so mount the input capacitor (C_{IN2}) as close as possible to the IC.
- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

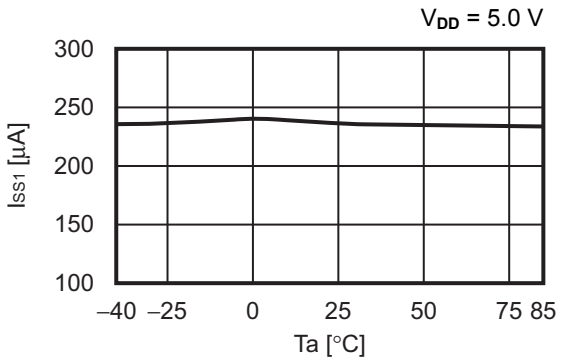
■ Characteristics (Typical Data)

1. Current consumption

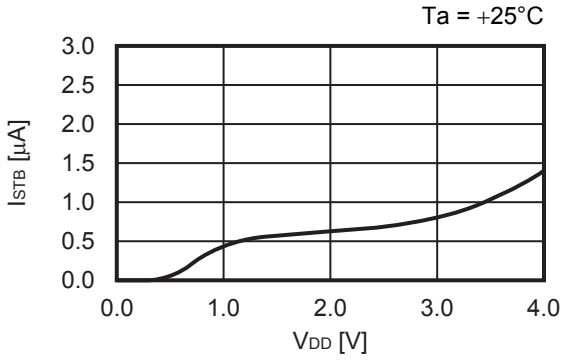
1. 1 I_{SS1} vs. V_{DD}



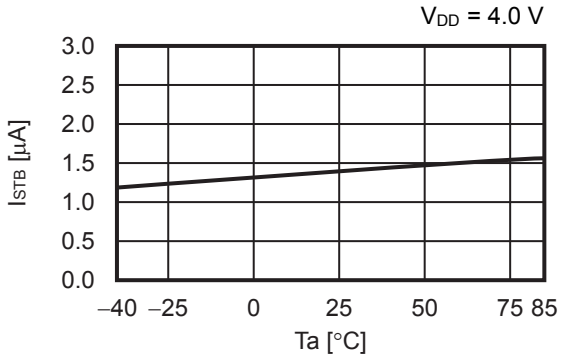
1. 2 I_{SS1} vs. Ta



1. 3 I_{STB} vs. V_{DD}

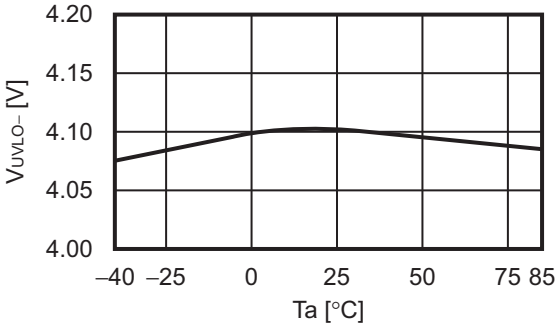


1. 4 I_{STB} vs. Ta

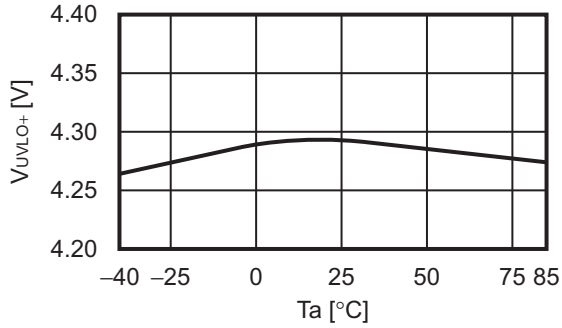


2. UVLO detection voltage, UVLO release voltage

2. 1 V_{UVLO-} vs. Ta

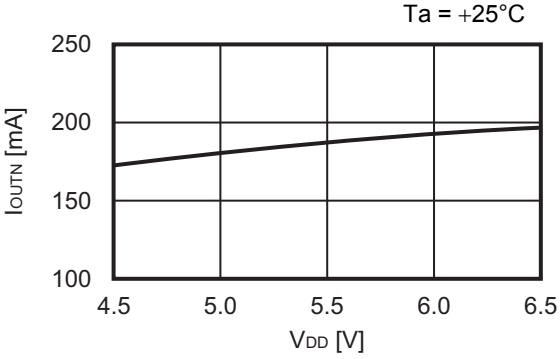


2. 2 V_{UVLO+} vs. Ta

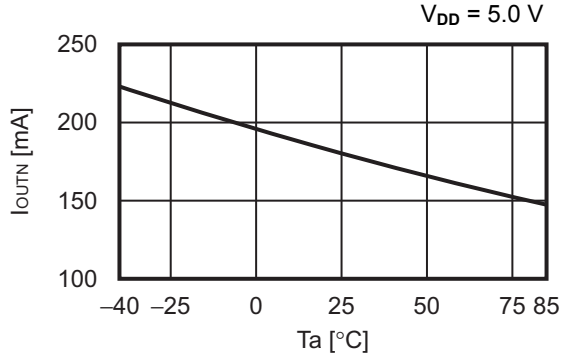


3. Out pin sink current, OUT pin source current, Nch driver ON resistance for STATUS pin

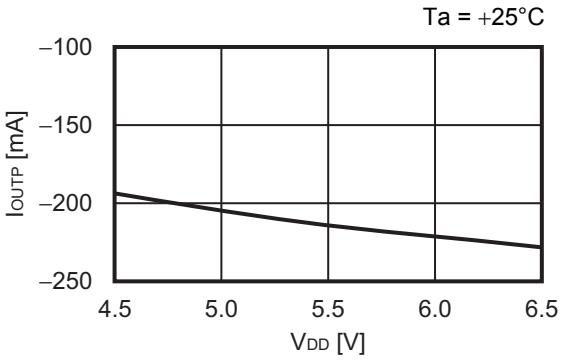
3. 1 I_{OUTN} vs. V_{DD}



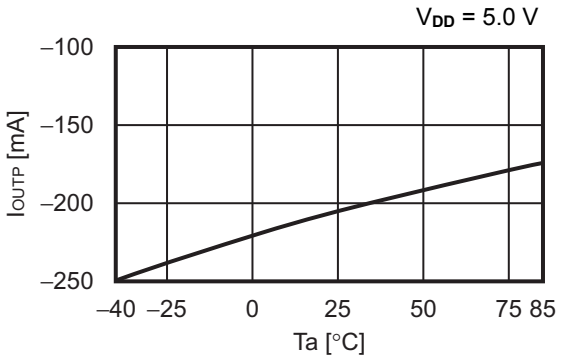
3. 2 I_{OUTN} vs. Ta



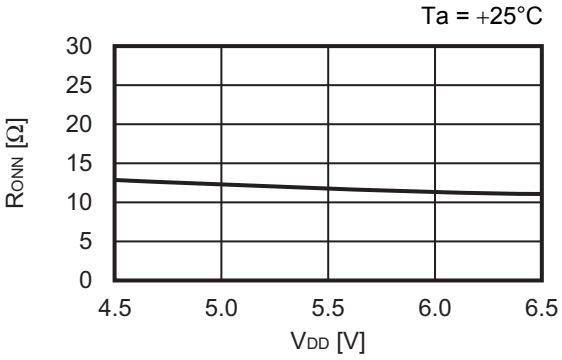
3. 3 I_{OUTP} vs. V_{DD}



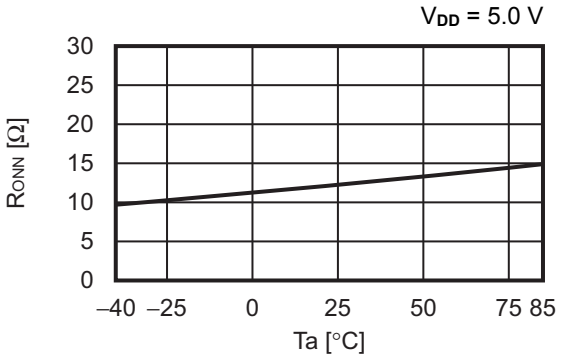
3. 4 I_{OUTP} vs. Ta



3. 5 R_{ONN} vs. V_{DD}

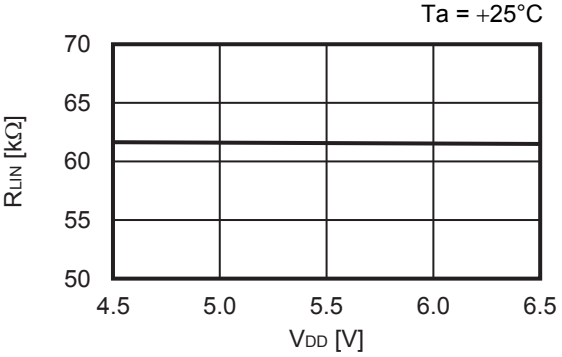


3. 6 R_{ONN} vs. Ta

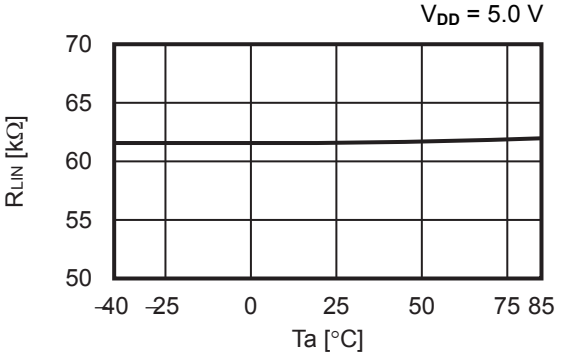


4. TH pin internal resistance, TH pin detection voltage

4. 1 R_{LIN} vs. V_{DD}

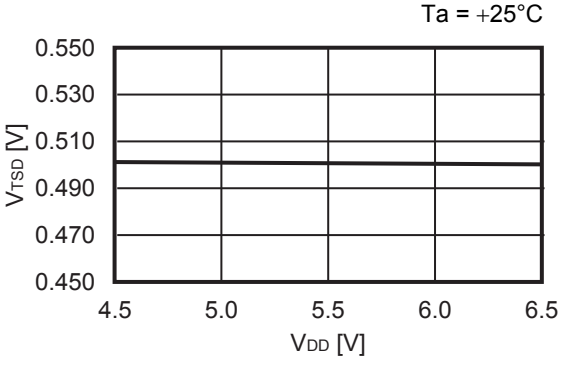


4. 2 R_{LIN} vs. Ta



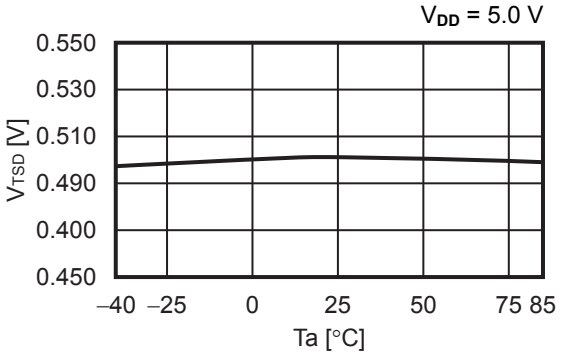
4. 3 V_{TSD} vs. V_{DD}

S-8474AC



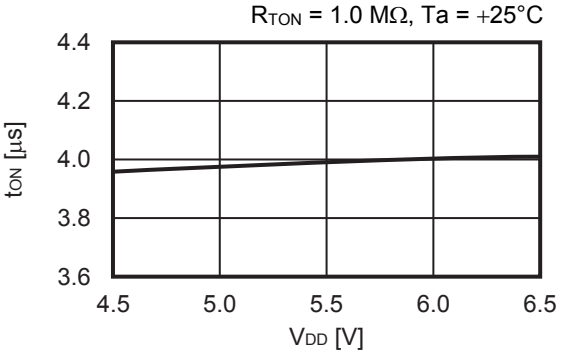
4. 4 V_{TSD} vs. Ta

S-8474AC

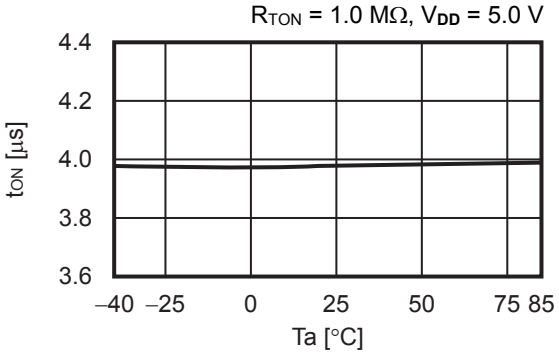


5. t_{ON} time, active time, sleep time, STATUS pin blinking cycle

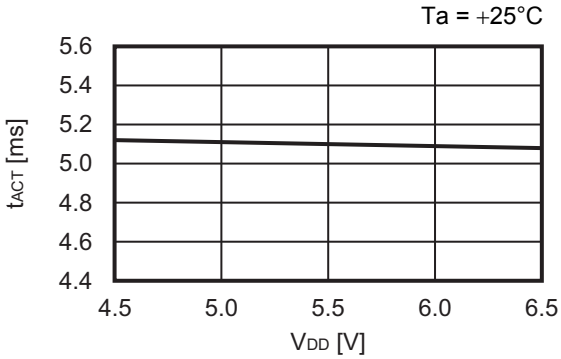
5. 1 t_{ON} vs. V_{DD}



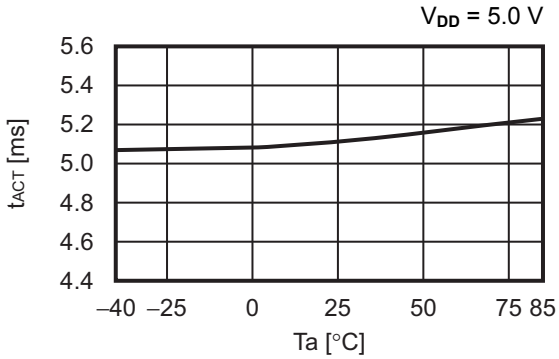
5. 2 t_{ON} vs. Ta



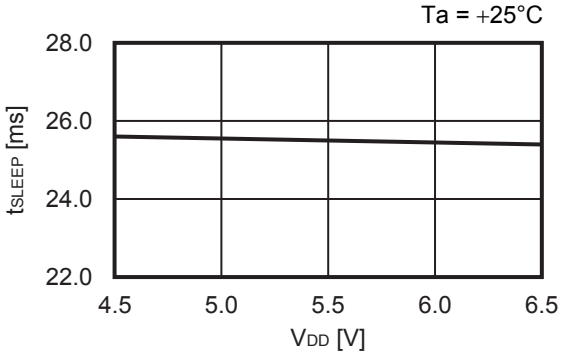
5. 3 t_{ACT} vs. V_{DD}



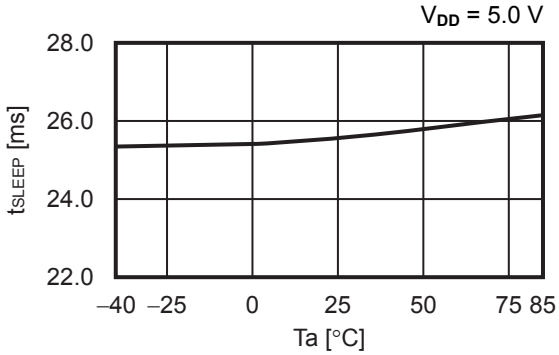
5. 4 t_{ACT} vs. Ta



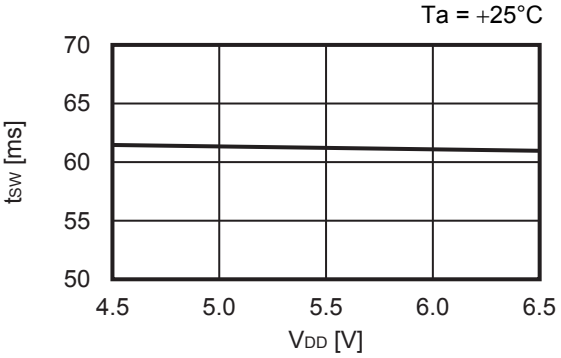
5. 5 t_{SLEEP} vs. V_{DD}



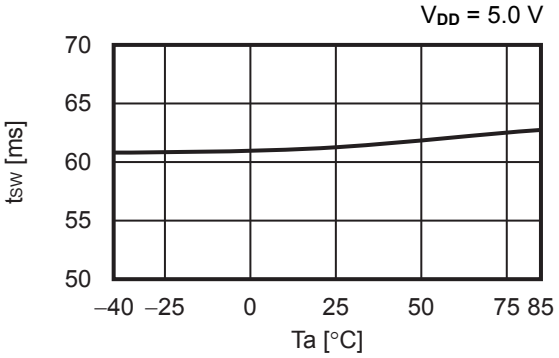
5. 6 t_{SLEEP} vs. Ta

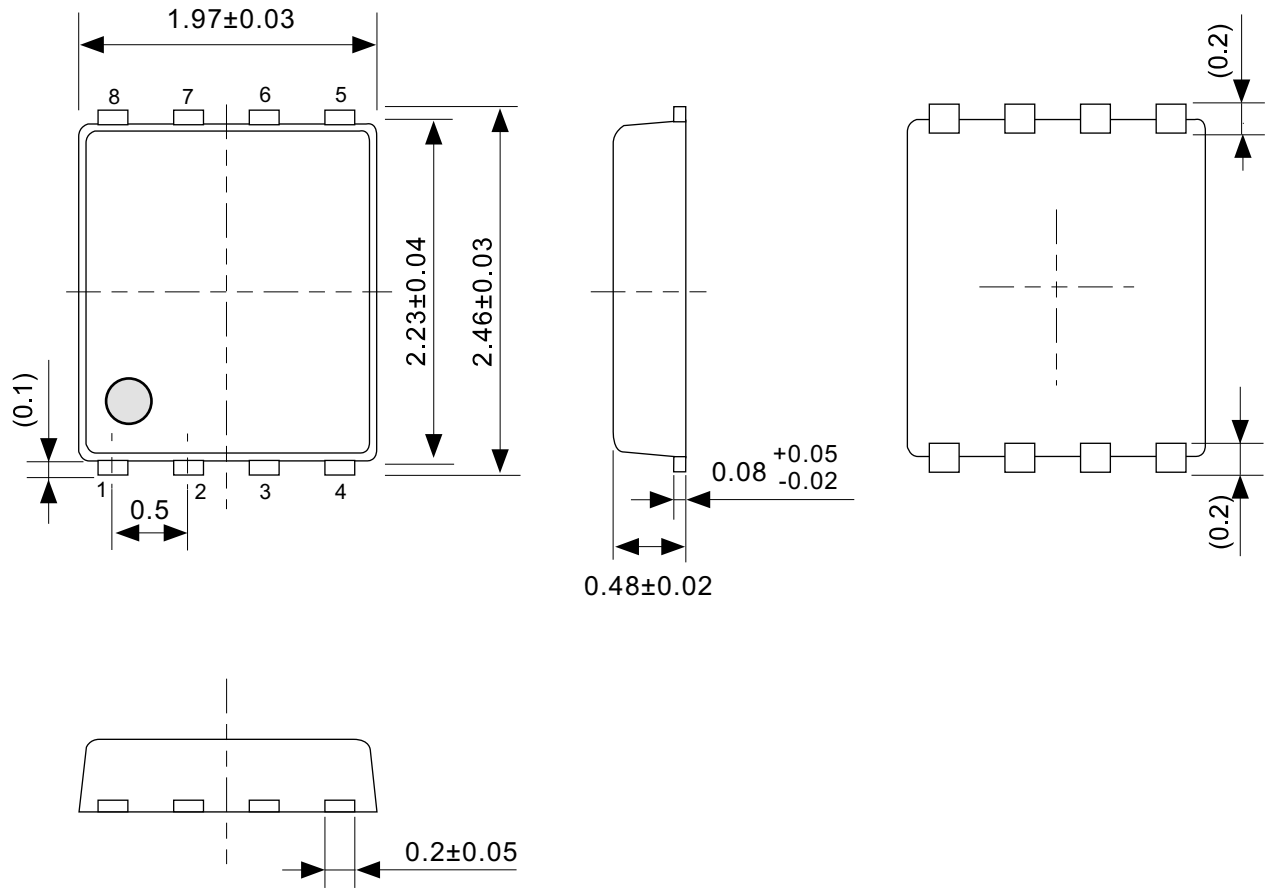


5. 7 t_{SW} vs. V_{DD}



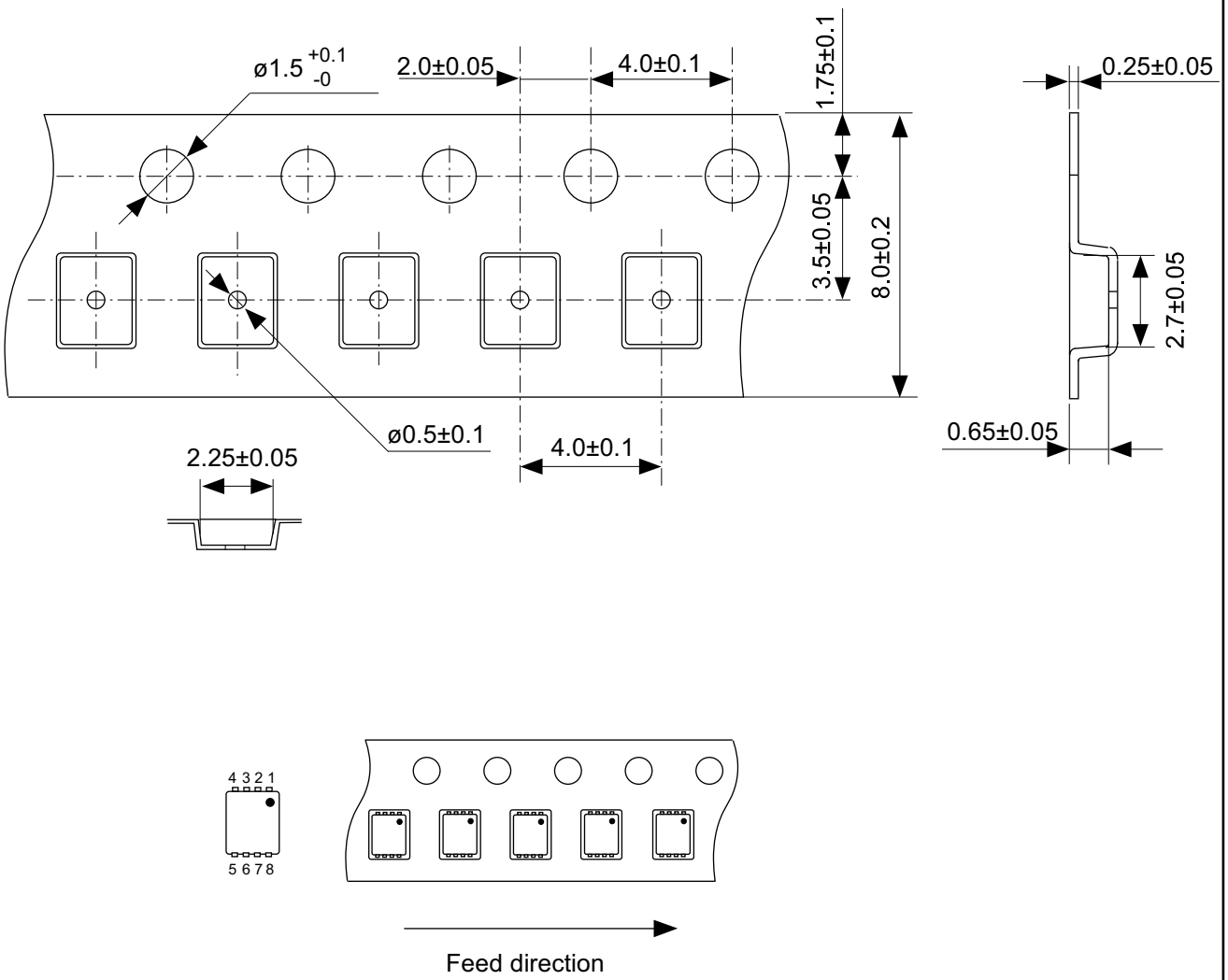
5. 8 t_{SW} vs. Ta





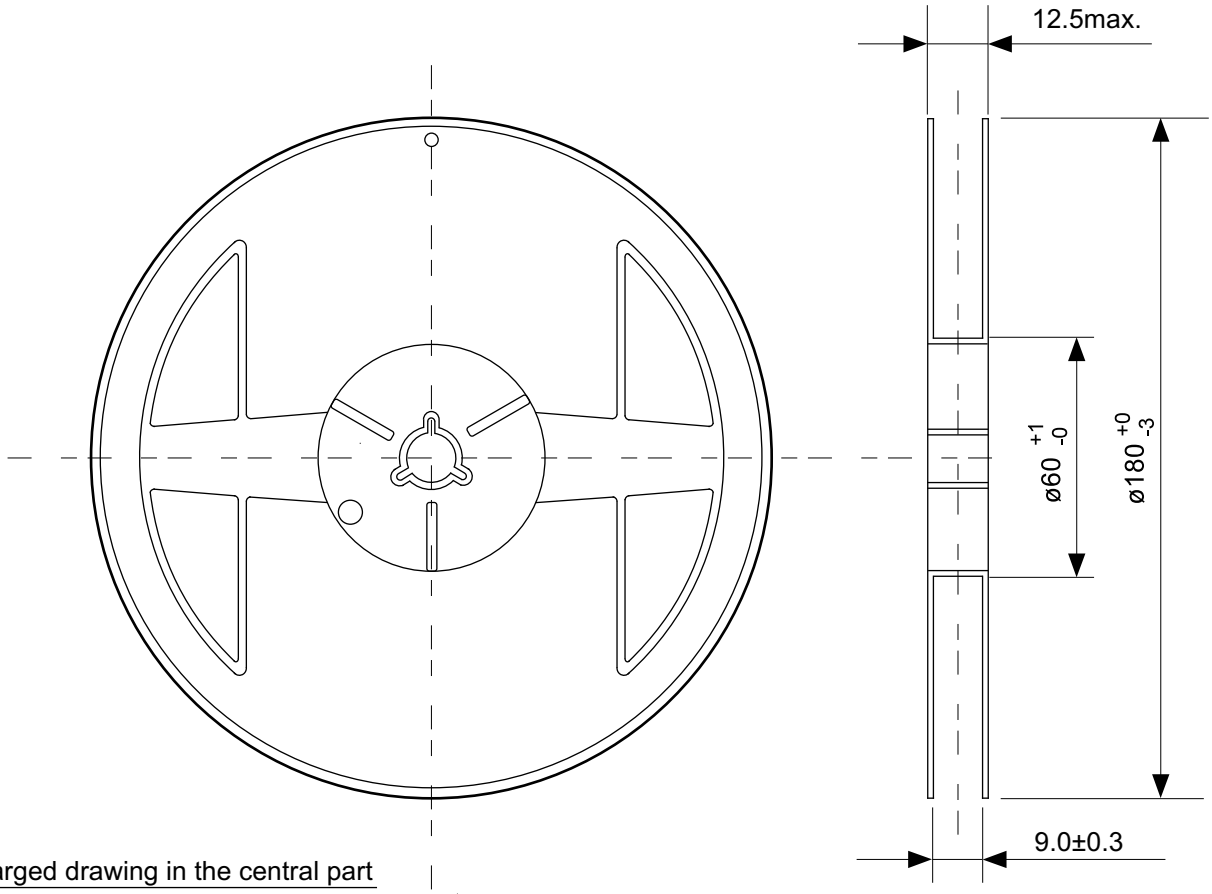
No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

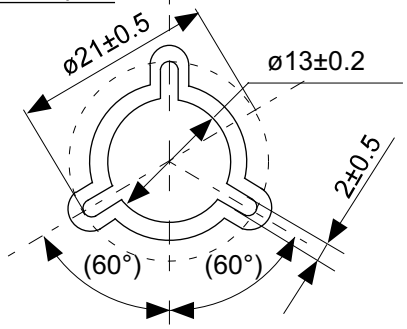


No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

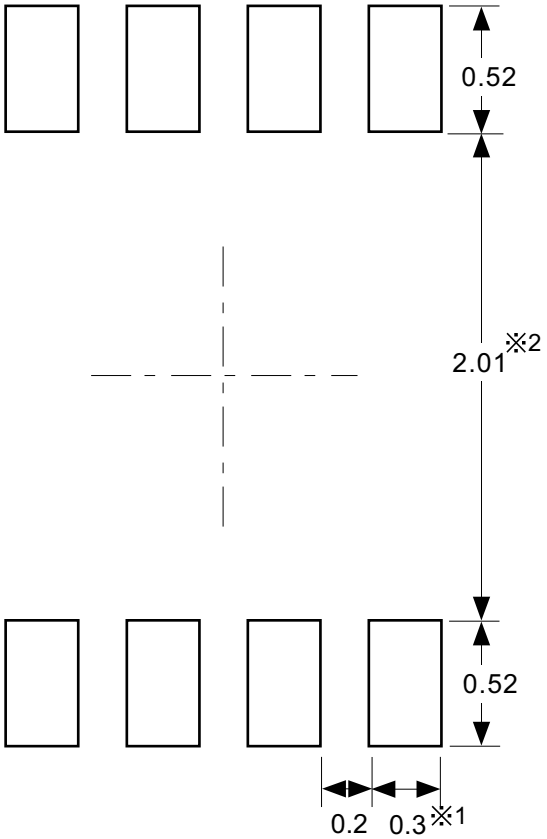


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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