ABLIC

S-82F9 Series

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BATTERY MONITORING IC

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This IC is a battery monitoring IC developed using CMOS technology. Compared with conventional CMOS voltage detectors, this IC is ideal for the applications that require high-withstand voltage due to its maximum operation voltage as high as 24 ٧.

This IC is capable of confirming the voltage in stages since it detects five voltage values.

The S-82F9A Series has an EN pin, allowing for reduction of current consumption by using an external signal to turn off this IC.

The S-82F9B Series has a SENSE pin, and the SENSE pin and external components enable battery monitoring equal to or higher than the rated voltage of the IC.

■ Features

• Detection voltage accuracy: ±1.0%

 $V_{HYS1(S)}$ to $V_{HYS5(S)} = 0$ mV, 50 mV, 300 mV, 400 mV, 500 mV • Hysteresis characteristics:

During operation: $I_{DD1} = 10 \mu A \text{ max}$. • Current consumption:

During power-off: $I_{DD2} = 0.1 \mu A \text{ max}$.

• Operation voltage range: $V_{DD} = 3.6 \text{ V to } 24 \text{ V}$

 $V_{DET1(S)}$ to $V_{DET5(S)} = 7.5 \text{ V}$ to 21.5 V (0.1 V step) • Detection voltage:

• Output form: Nch open-drain output

 Output logic*1: Full charge all on, Individual step voltage on

• SENSE pin power-off voltage: V_{SENSE} < 0.3 V (S-82F9B Series) • Voltage detection pin: S-82F9A Series: VDD pin S-82F9B Series: SENSE pin

• Operation temperature range: Ta = -40°C to +85°C

• Lead-free (Sn 100%), halogen-free

Full charge all on: The multiple output pins become V_{SS} output depending on the input voltage.

When the input voltage is equal to or higher than each of the five detection voltage values,

 $V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = V_{SS}$.

Individual step voltage on: According to the input voltage, only one output pin is a Vss output.

Set the detection voltage to $V_{DET1} > V_{DET2} > V_{DET3} > V_{DET4} > V_{DET5}$ and

 $V_{DETn} > V_{DETn+1} + V_{HYSn+1}$.

 $V_{OUT1} = V_{SS}$ and $V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = High-Z$ when the input voltage is equal

to or higher than detection voltage 1 (VDET1).

■ Application

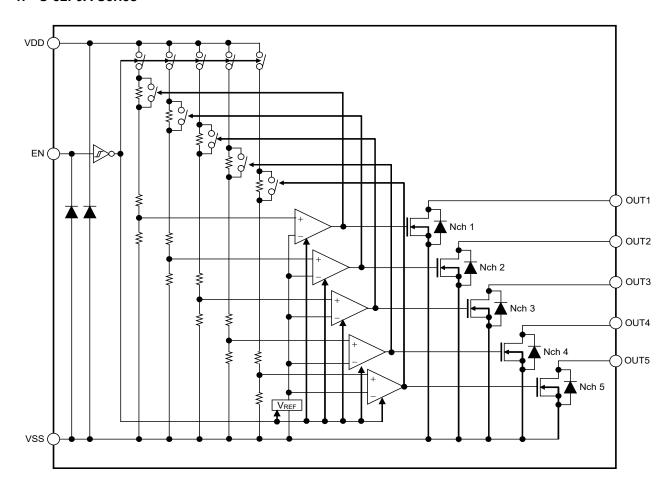
Rechargeable lithium-ion battery pack

Package

• HTMSOP-8

■ Block Diagram

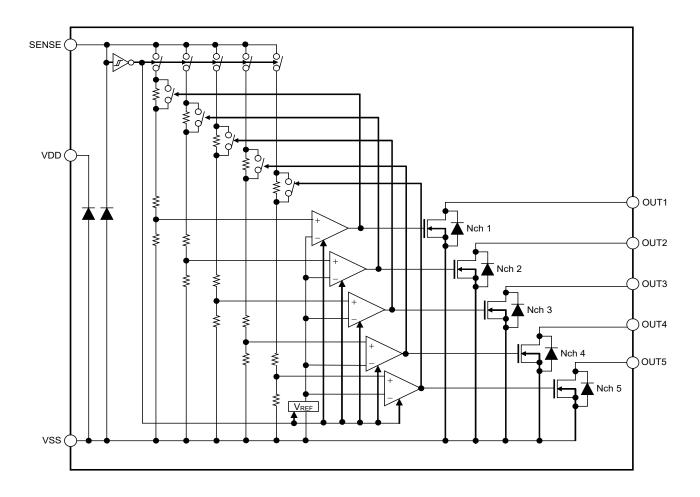
1. S-82F9A Series



Remark Diodes in the figure are parasitic diodes.

Figure 1

2. S-82F9B Series

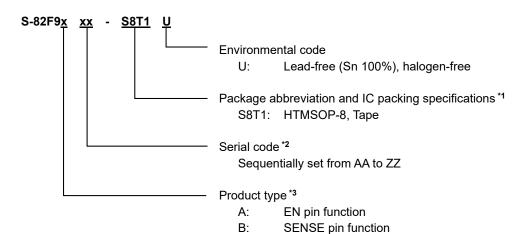


Remark Diodes in the figure are parasitic diodes.

Figure 2

■ Product Name Structure

1. Product name



- *1. Refer to the tape drawing.
- *2. Refer to "3. Product name list".
- ***3.** EN pin function: The EN pin can control the state of the IC. SENSE pin function: The SENSE pin can monitor the battery voltage.

2. Package

Table 1 Package Drawing Codes

Package Name	Package Name Dimension		Reel	Land	
HTMSOP-8	FP008-A-P-SD	FP008-A-C-SD	FP008-A-R-SD	FP008-A-L-SD	

3. Product name list

3. 1 S-82F9A Series

Table 2 (1 / 2)

	Detection	Detection	Detection	Detection	Detection
Product Name	Voltage 1	Voltage 2	Voltage 3	Voltage 4	Voltage 5
	[V _{DET1(S)}]	[V _{DET2(S)}]	[V _{DET3(S)}]	[V _{DET4(S)}]	[V _{DET5(S)}]
S-82F9AAA-S8T1U	21.5 V	18.0 V	14.5 V	11.0 V	7.5 V

Table 2 (2 / 2)

	Hysteresis	Hysteresis	Hysteresis	Hysteresis	Hysteresis	
Product Name	Width 1	Width 2	Width 3	Width 4	Width 5	Output Logic*1
	[V _{HYS1(S)}]	[V _{HYS2(S)}]	[V _{HYS3(S)}]	[V _{HYS4(S)}]	[V _{HYS5(S)}]	
S-82F9AAA-S8T1U	50 mV	Full charge all on				

3. 2 S-82F9B Series

Table 3 (1 / 2)

	Detection	Detection	Detection	Detection	Detection
Product Name	Voltage 1	Voltage 2	Voltage 3	Voltage 4	Voltage 5
	[V _{DET1(S)}]	[V _{DET2(S)}]	[V _{DET3(S)}]	[V _{DET4(S)}]	[V _{DET5(S)}]
S-82F9BAA-S8T1U	21.5 V	18.0 V	14.5 V	11.0 V	7.5 V

Table 3 (2 / 2)

	Hysteresis	Hysteresis	Hysteresis	Hysteresis	Hysteresis	
Product Name	Width 1	Width 2	Width 3	Width 4	Width 5	Output Logic*1
	[V _{HYS1(S)}]	[V _{HYS2(S)}]	[V _{HYS3(S)}]	[V _{HYS4(S)}]	[V _{HYS5(S)}]	
S-82F9BAA-S8T1U	50 mV	Full charge all on				

^{*1.} Output Logic: Full charge all on, Individual step voltage on

Remark Please contact our sales representatives for products other than the above.

■ Pin Configurations

1. HTMSOP-8

Bottom view

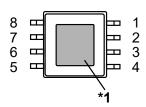


Figure 3

Table 4 S-82F9A Series

Pin No.	Symbol	Description
1	OUT1	Voltage detection output pin 1
2	OUT2	Voltage detection output pin 2
3	OUT3	Voltage detection output pin 3
4	OUT4	Voltage detection output pin 4
5	OUT5	Voltage detection output pin 5
6	VSS	GND pin
7	EN	EN signal input pin
8	VDD	Positive power supply input pin

Table 5 S-82F9B Series

Pin No.	Symbol	Description
1	OUT1	Voltage detection output pin 1
2	OUT2	Voltage detection output pin 2
3	OUT3	Voltage detection output pin 3
4	OUT4	Voltage detection output pin 4
5	OUT5	Voltage detection output pin 5
6	VSS	GND pin
7	SENSE	Detection voltage input pin
8	VDD	Positive power supply input pin

^{*1.} Connect the heat sink of backside at shadowed area to the board and set electric potential open or V_{DD} . However, do not use it as the function of electrode.

■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DD}	V _{SS} - 0.3 to V _{SS} + 28	V
EN pin input voltage (S-82F9A Series)	V _{EN}	Vss - 0.3 to Vss + 28	V
SENSE pin input voltage (S-82F9B Series)	V _{SENSE}	Vss - 0.3 to V _{DD} + 0.3	V
Output voltage n	Voutn	Vss - 0.3 to Vss + 28	V
Operation ambient temperature	Topr	-40 to +85	°C
Storage temperature	T _{stg}	-40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

Remark n = 1 to 5

■ Thermal Resistance Value

Table 7

Item	Symbol	Condition		Min.	Тур.	Max.	Unit
Junction-to-ambient thermal resistance*1		HTMSOP-8	Board A	-	159	-	°C/W
			Board B	-	113	-	°C/W
	θЈΑ		Board C	-	39	-	°C/W
			Board D	-	40	-	°C/W
			Board E	-	30	-	°C/W

^{*1.} Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to ■ Power Dissipation" and "Test Board" for details.

■ Electrical Characteristics

Table 8

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Test Circuit
Common							
Detection voltage n*1	V _{DETn}	-	V _{DETn(S)} × 0.99	V _{DETn(S)}	V _{DETn(S)} × 1.01	V	1
	.,	300 mV ≤ V _{HYSn(S)} ≤ 500 mV	V _{HYSn(S)} × 0.8	V _{HYSn(S)}	V _{HYSn(S)} × 1.2	٧	1
Hysteresis width n*2	V _H YSn	0 V ≤ V _{HYSn(S)} ≤ 50 mV	V _{HYSn(S)} - 0.025	V _{HYSn(S)}	V _{HYSn(S)} + 0.025	V	1
Operation voltage range between VDD pin and VSS pin	V_{DD}	Fixed output pin voltage	3.6	1	24	V	-
Current consumption during operation*3	I _{DD1}	V1 = 23 V, V2 = 23 V	-	-	10	μΑ	1
Current consumption during power-off	I _{DD2}	V1 = 23 V, V2 = 0 V	-	-	0.1	μA	1
		Full charge all on, V1 = 23 V, V2 = 23 V, V3 = 1 V	10	1	-	mA	2
Output sink current n	l _{OUTn}	Individual step voltage on V1 = V2 = V _{DETn} + V _{HYSn} , V3 = 1 V	10	1	-	mA	2
Output leak current n	I _{LEAKn}	V1 = 23 V, V2 = 0 V, V3 = 23 V	-	1	0.1	μΑ	2
S-82F9A Series							
EN pin input voltage "H"	V _{SH}	V1 = 23 V	1.5	ı	ı	V	1
EN pin input voltage "H"	V_{SL}	V1 = 23 V	ı	ı	0.3	V	1
S-82F9B Series							
SENSE pin current	I _{SENSE}	V1 = 23 V, V2 = 23 V	ı	ı	10	μΑ	1
SENSE pin input voltage "H"	V _{SH}	V1 = 23 V	7	-	-	V	1
SENSE pin input Voltage "L"	V_{SL}	V1 = 23 V	-	-	0.3	V	1

^{*1.} V_{DETn} : Actual detection voltage value, $V_{DETn(S)}$: Set detection voltage

Remark n = 1 to 5

^{*2.} V_{HYSn} : Actual hysteresis width, $V_{HYSn(S)}$: Set hysteresis width The relationship between V_{DETn} and V_{HYSn} is as follows.

 $V_{DETn} < V_{DETn} + V_{HYSn}$

^{*3.} Current consumption = I_{VDD} + I_{EN} (S-82F9A Series) Current consumption = I_{VDD} + I_{SENSE} (S-82F9B Series)

■ Test Circuits

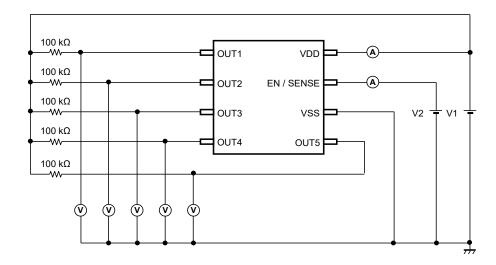


Figure 4 Test Circuit 1

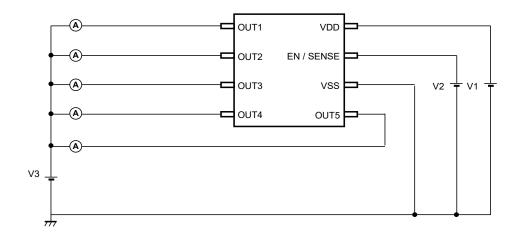


Figure 5 Test Circuit 2

9

■ Standard Circuit

1. S-82F9A Series

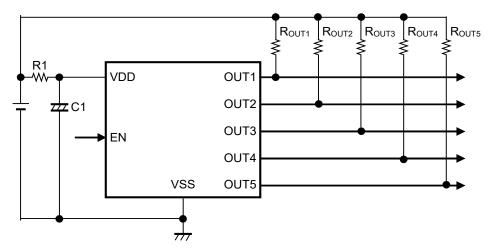


Figure 6

2. S-82F9B Series

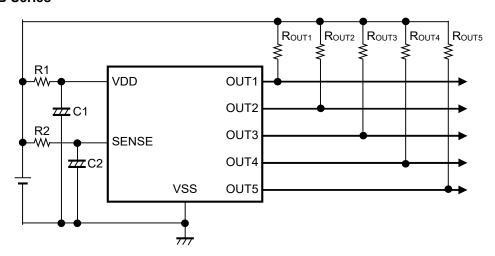


Figure 7

Table 9 Constants for External Components

Symbol	Purpose	Тур.	Remark
R1, R2*1	For power fluctuation	470 Ω	Set the value as small as possible to prevent deterioration of the detection voltage.
C1, C2	For power fluctuation	0.1 µF	-
R _{OUTn} *2	For output pin pull-up	1 kΩ	Make sure the power dissipation of this IC is not exceeded.

^{*1.} Set up R1, R2 as 100 k Ω or less to prevent oscillation.

Caution 1. The constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

Remark n = 1 to 5

^{*2.} Set up each of R_{OUTn} as 620 Ω or more so that the power dissipation is not exceeded.

Operation

1. Basic operation

1. 1 S-82F9A Series

1. 1. 1 When the power supply voltage (VDD) decreases

The OUTn pin becomes detection status if V_{DD} is equal to or lower than the detection voltage (V_{DETn}).

1. 1. 2 When the power supply voltage increases

The OUTn pin becomes release status if VDD is equal to or higher than the release voltage (VDETn + VHYSn).

1. 1. 3 When V_{DD} ≤ minimum operation voltage

The OUTn pin voltage is indefinite.

1. 2 S-82F9B Series

1. 2. 1 When the SENSE pin voltage (VSENSE) decreases

The OUTn pin becomes detection status if V_{SENSE} is equal to or lower than the detection voltage (V_{DETn}).

1. 2. 2 When the SENSE pin voltage increases

The OUTn pin becomes release status if V_{SENSE} is equal to or higher than the release voltage (V_{DETn} + V_{HYSn}).

1. 2. 3 When V_{SENSE} ≤ minimum operation voltage

Even if V_{SENSE} further decreases to the IC's minimum operation voltage or lower, the output from the OUTn pin is stable when V_{DD} is minimum operation voltage or higher.

2. EN pin (S-82F9A Series)

This pin starts and stops this IC.

When $V_{EN} \le V_{SL}$ is set, all internal circuits stop operating, and Nch transistor n (refer to **Figure 1** in **"Block Diagram"**) is turned off, reducing current consumption significantly.

When not using the EN pin, connect it to the VDD pin.

Refer to the circuit diagram in Figure 11 for the circuit connection example.

3. SENSE pin (S-82F9B Series)

This pin starts and stops this IC and monitors the battery voltage.

When $V_{SENSE} \le V_{SL}$ is set, all internal circuits stop operating, and Nch transistor n (refer to **Figure 2** in **Block Diagram**") is turned off, reducing current consumption significantly.

Refer to the circuit diagram in Figure 12 and Figure 13 for the circuit connection example.

Remark n = 1 to 5

■ Timing Charts

1. S-82F9A Series (Full charge all on, V_{EN} ≥ V_{SH})

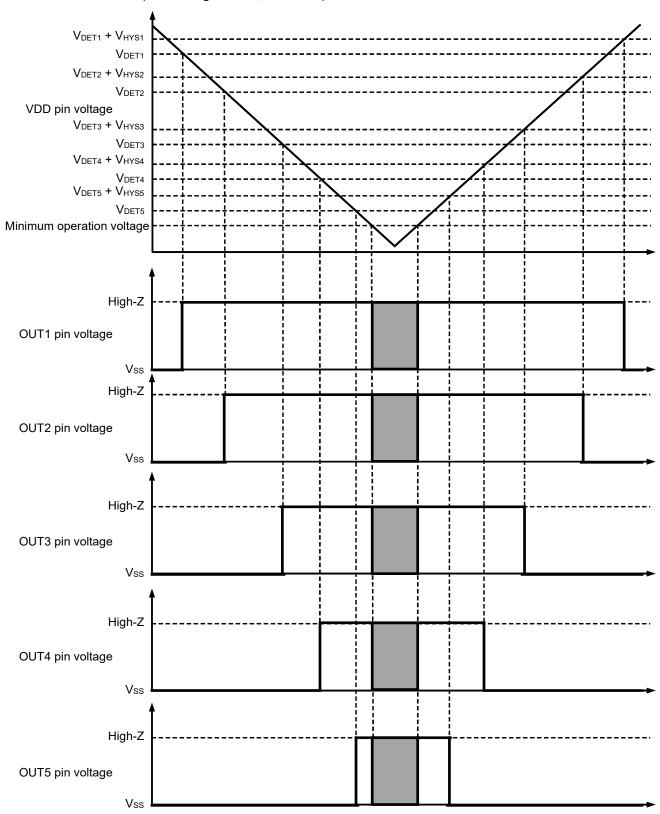
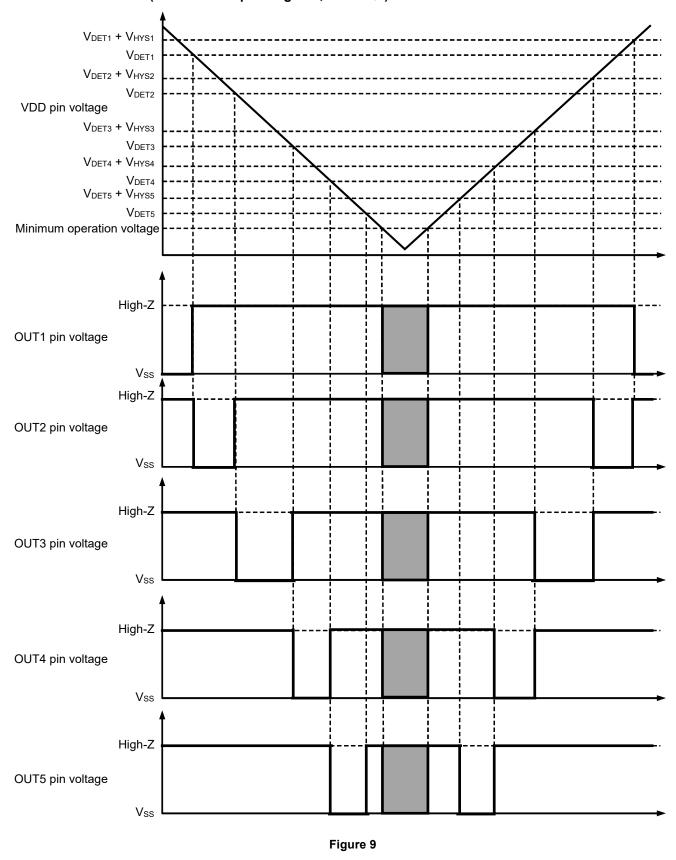


Figure 8

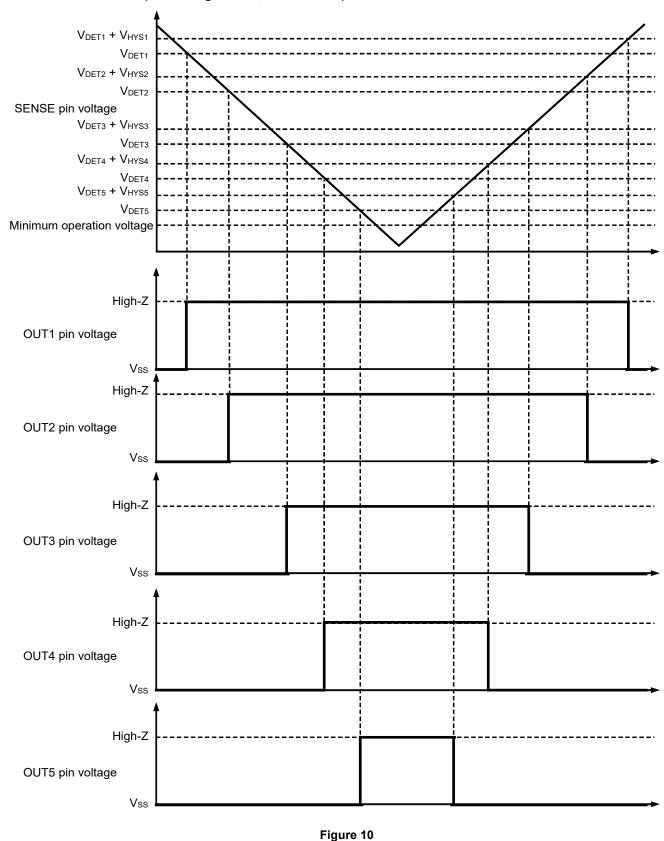
Remark When V_{DD} is equal to or lower than the minimum operation voltage, the output voltage from the OUT1 pin to the OUT5 pin is indefinite in the shaded area.

2. S-82F9A Series (Individual step voltage on, $V_{EN} \ge V_{SH}$)



Remark When V_{DD} is equal to or lower than the minimum operation voltage, the output voltage from the OUT1 pin to the OUT5 pin is indefinite in the shaded area.

3. S-82F9B Series (Full charge all on, V_{SENSE} ≥ V_{SH})



Remark Even if V_{SENSE} is below the minimum operating voltage of the IC, the output voltage from the OUT1 pin to OUT5 pin are stable when V_{DD} is minimum operation voltage or higher.

14

■ Application Circuits

1. LED battery level Indicator

1. 1 S-82F9A Series

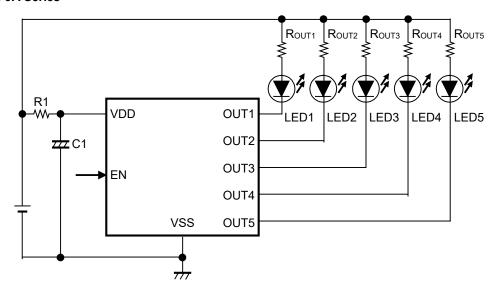


Figure 11

Caution It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

1. 2 S-82F9B Series

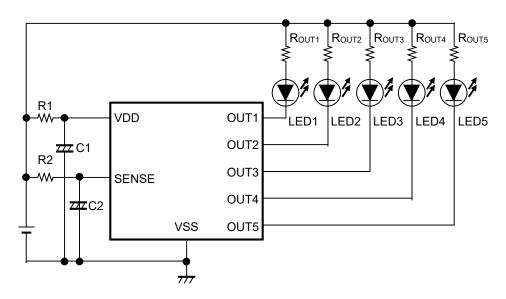


Figure 12

Caution It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

2. Change of detection voltage using S-82F9B Series

This IC can monitor battery voltage equal to or higher than the rated voltage of the IC by making the connection shown in **Figure 13**.

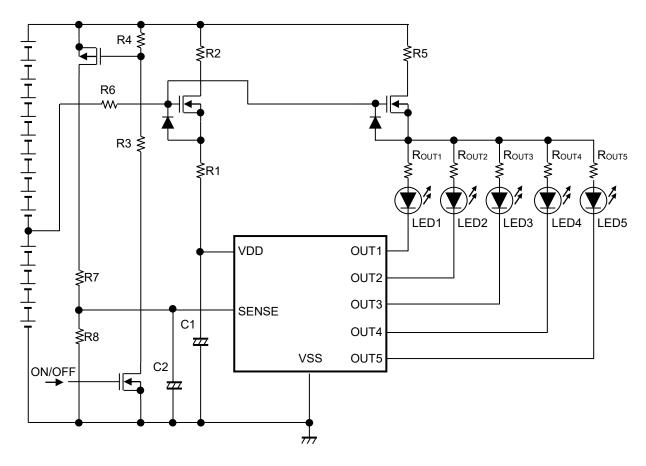


Figure 13

Caution It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

■ Precautions

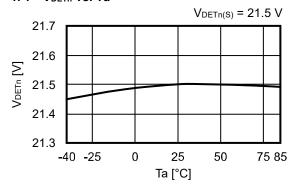
- The application conditions for the input voltage, output voltage, and output pin pull-up resistance should not exceed the package power dissipation.
- Wiring patterns for the VDD pin, the VOUTn pin and the VSS pin should be designed so that the impedance is low.
- Note that the detection voltage may deviate due to the resistance component of output sink current and the VSS pin wiring.
- In applications where a resistor is connected to the input (refer to **Figure 11** in **"■ Application Circuit"**), the feed-through current which is generated when the output switches causes a voltage drop equal to feed-through current × input resistance. After the output switches, the feed-through current stops and its resultant voltage drop disappears, and the output switches. The feed-through current is then generated again, a voltage drop appears. Note that an oscillation may be generated for this reason.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

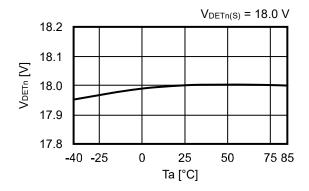
Remark n = 1 to 5

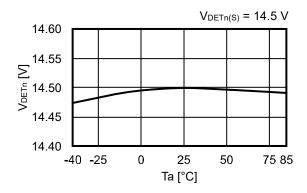
■ Characteristics (Typical Data)

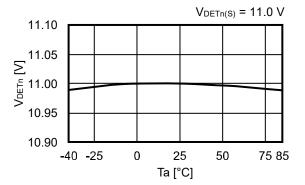
1. Detection voltage

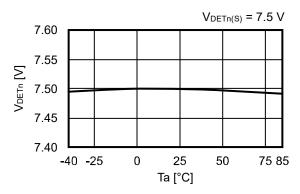
1. 1 VDETn vs. Ta





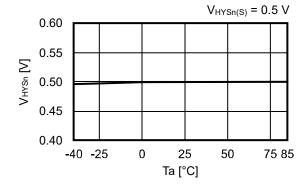


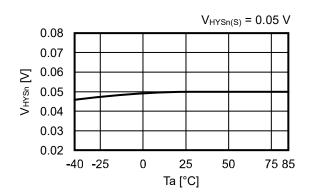




2. Hysteresis width

2. 1 V_{HYSn} vs. Ta

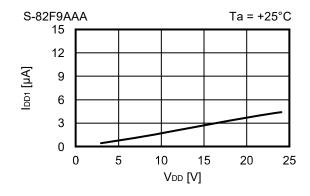




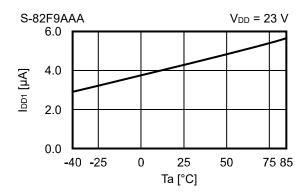
Remark n = 1 to 5

3. Current consumption

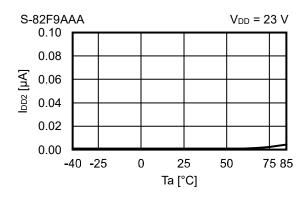
3. 1 IDD1 vs. VDD



3. 2 I_{DD1} vs. Ta

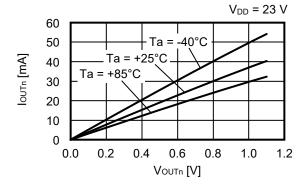


3. 3 IDD2 vs. Ta

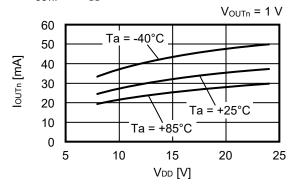


4. Output current

4. 1 Ioutn vs. Voutn



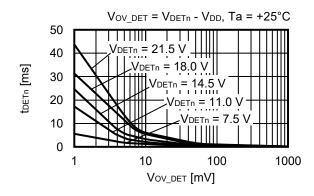
4. 2 I_{OUTn} vs. V_{DD}



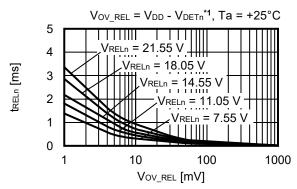
Remark n = 1 to 5

5. Response time

5. 1 tdetn vs. Vov_det



5. 2 treln vs. Vov_REL



*1. $V_{RELn} = V_{DETn} + V_{HYSn}$

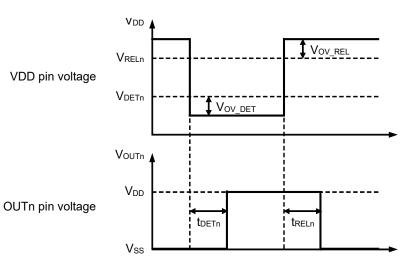


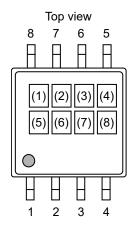
Figure 14 Test Condition of Response Time

Remark 1. Refer to "Figure 4 Test Circuit 1" for the test condition of the response time.

2. n = 1 to 5

■ Marking Specifications

1. HTMSOP-8



(1): Blank

(2) to (4): Product code (Refer to Product name vs. Product code)

(5): Blank(6) to (8): Lot number

Product name vs. Product code

1. 1 S-82F9A Series

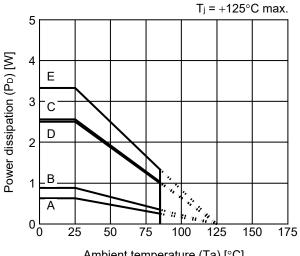
Product Name	Product Code				
Product Name	(2) (3) (4				
S-82F9AAA-S8T1U	9	Υ	В		

1. 2 S-82F9B Series

Product Name	Product Code		
Product Name	(2)	(3)	(4)
S-82F9BAA-S8T1U	9	Υ	D

■ Power Dissipation

HTMSOP-8



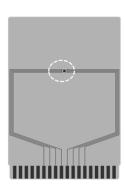
Ambient temperature (Ta) [°C]

Board	Power Dissipation (P _D)
Α	0.63 W
В	0.88 W
С	2.56 W
D	2.50 W
Е	3.33 W

HTMSOP-8 Test Board

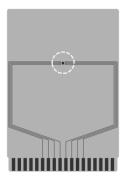
(1) Board A





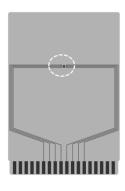
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



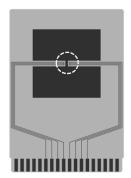
enlarged view

No. HTMSOP8-A-Board-SD-1.0

HTMSOP-8 Test Board

O IC Mount Area

(4) Board D

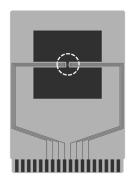


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm ² t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-



enlarged view

(5) Board E

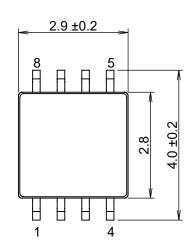


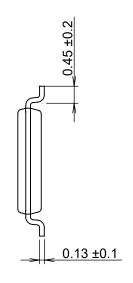
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm ² t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

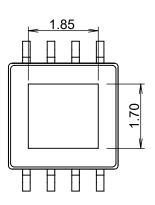


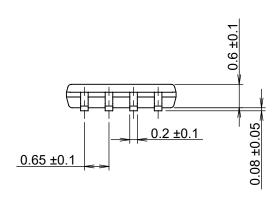
enlarged view

No. HTMSOP8-A-Board-SD-1.0



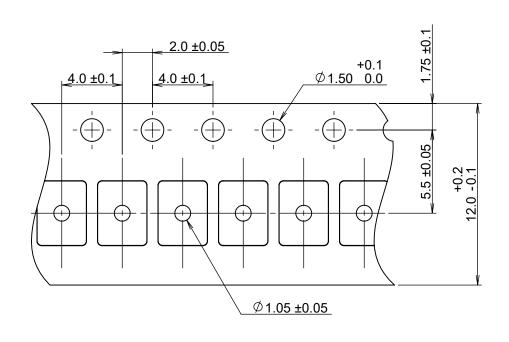


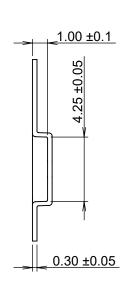


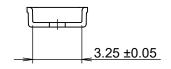


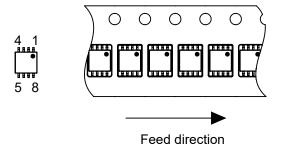
No. FP008-A-P-SD-2.0

TITLE	HTMSOP8-A-PKG Dimensions	
No.	FP008-A-P-SD-2.0	
ANGLE	⊕€-	
UNIT	mm	
ABLIC Inc.		



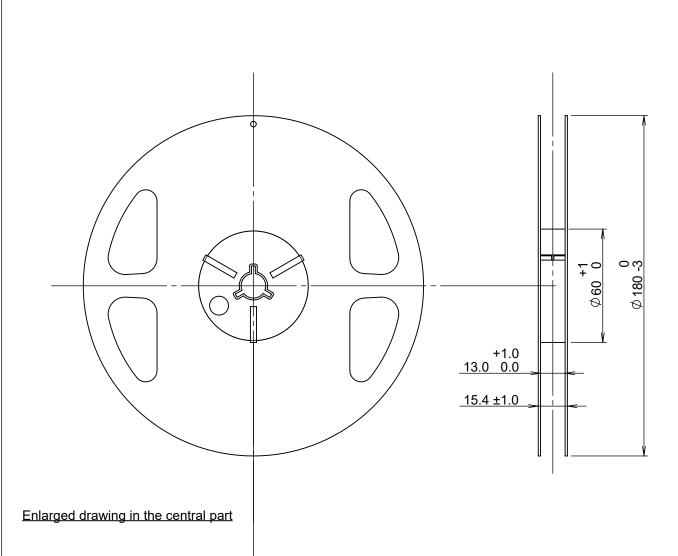


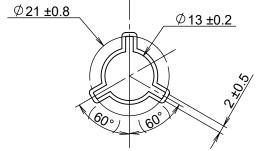




No. FP008-A-C-SD-1.0

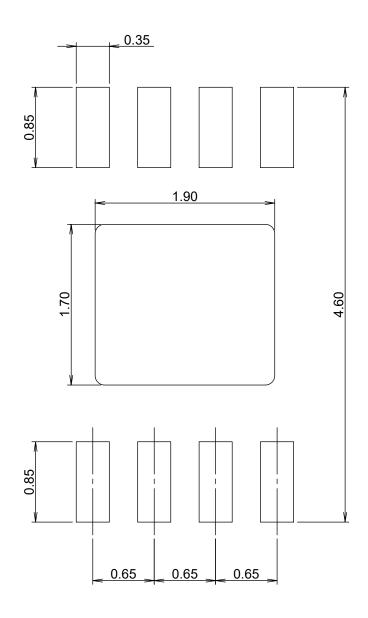
TITLE	HTMSOP8-A-Carrier Tape				
No.	FP008-A-C-SD-1.0				
ANGLE					
UNIT	mm				
ABLIC Inc.					





No. FP008-A-R-SD-2.0

TITLE		HTMS	SOP8-A-	Reel
No.		FP00)8-A-R-S	D-2.0
ANGLE			QTY.	4,000
UNIT	mm			
ABLIC Inc.				



No. FP008-A-L-SD-2.0

TITLE	HTMSOP8-A -Land Recommendation		
No.	FP008-A-L-SD-2.0		
ANGLE			
UNIT	mm		
ABLIC Inc.			

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