S-5719 Series

SUPER LOW CURRENT CONSUMPTION LOW VOLTAGE OPERATION OMNIPOLAR DETECTION TYPE HALL EFFECT SWITCH IC

www.ablic.com

Rev.1.0_00

This IC, developed by CMOS technology, is a high-accuracy Hall effect switch IC that operates with super low current consumption and low voltage.
The output voltage changes when this IC detects the intensity level of magnetic flux density. Using this IC with a magnet makes it possible to detect the open / close in various devices.
High-density mounting is possible by using the super-small SNT-4A package.
Due to its super low current consumption and low voltage, this IC is most suitable for battery-operated portable devices. Also, due to its high-accuracy magnetic characteristics, this IC can make operation's dispersion in the system combined with magnet smaller.

ABLIC Inc. offers a "magnetic simulation service" that provides the ideal combination of magnets and our Hall ICs for customer systems. Our magnetic simulation service will reduce prototype production, development period and development costs. In addition, it will contribute to optimization of parts to realize high cost performance.
For more information regarding our magnetic simulation service, contact our sales representatives.

■ Features

- Pole detection: Detection of omnipolar
- Output logic*1: Active "L"
  Active "H"
- Output form: CMOS output
- Magnetic sensitivity*1: B_{OP} = 1.8 mT typ.
  B_{OP} = 3.0 mT typ.
  B_{OP} = 4.5 mT typ.
- Operating cycle (current consumption)*1: t_{CYCLE} = 531.2 ms typ. (I_{DD} = 0.2 μA typ.)
  t_{CYCLE} = 133.2 ms typ. (I_{DD} = 0.5 μA typ.)
- Power supply voltage range: V_{DD} = 1.3 V to 3.6 V
- Operation temperature range: Ta = -40°C to +85°C
- Lead-free (Sn 100%), halogen-free

***1.** The option can be selected.

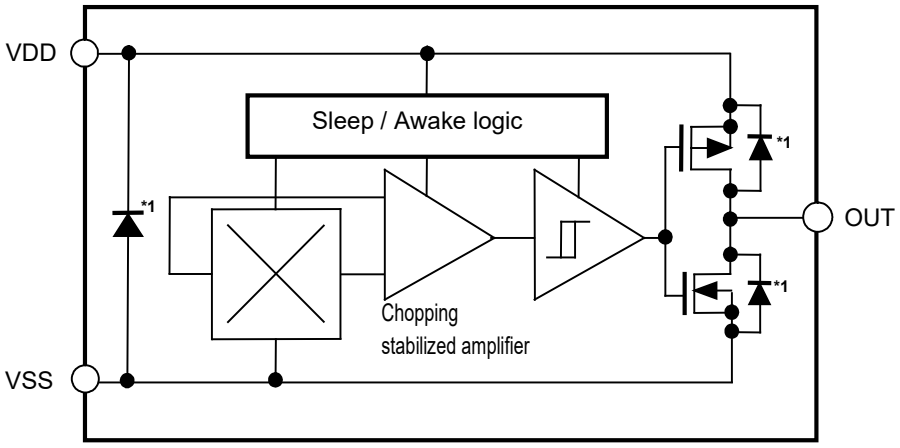
■ Applications

- Home security device (Window/door open/close detection)
- Utility meter
- Battery powered device
- Wearable device

■ Package

- SNT-4A

■ Block Diagram

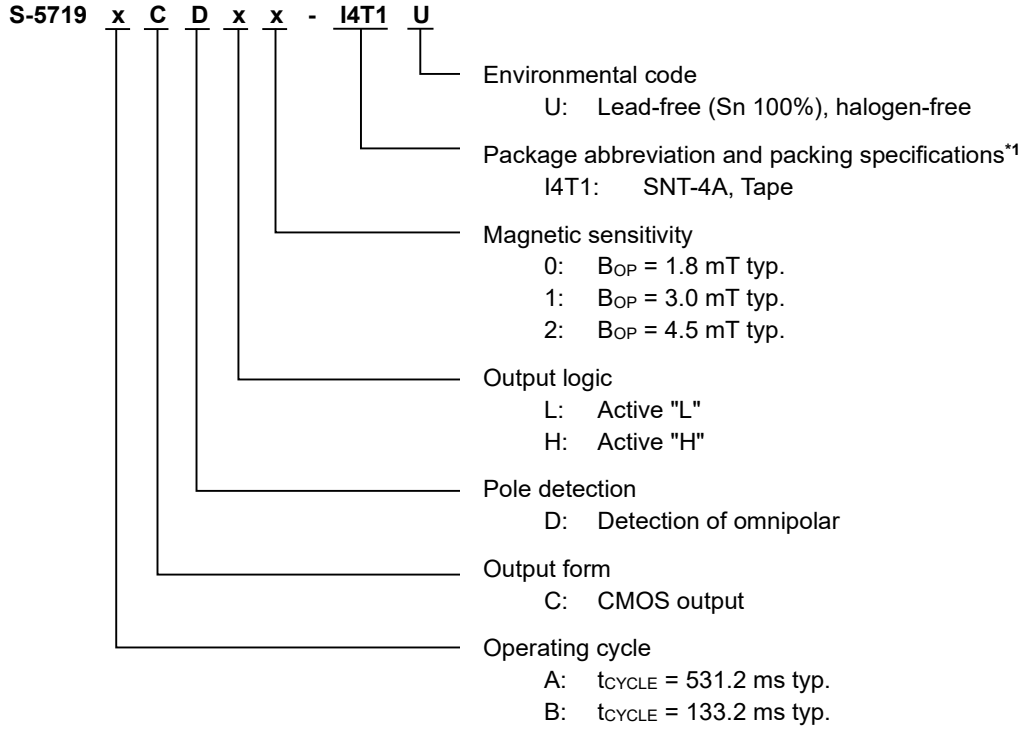


1. Parasitic diode

Figure 1

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SNT-4A	PF004-A-P-SD	PF004-A-C-SD	PF004-A-R-SD	PF004-A-L-SD

3. Product name list

Table 2

Product Name	Operating Cycle (t_{CYCLE})	Output Form	Pole Detection	Output Logic	Magnetic Sensitivity (B_{OP})
S-5719ACDL0-I4T1U	531.2 ms typ.	CMOS output	Omnipolar	Active "L"	1.8 mT typ.
S-5719ACDH0-I4T1U	531.2 ms typ.	CMOS output	Omnipolar	Active "H"	1.8 mT typ.
S-5719ACDL1-I4T1U	531.2 ms typ.	CMOS output	Omnipolar	Active "L"	3.0 mT typ.
S-5719ACDH1-I4T1U	531.2 ms typ.	CMOS output	Omnipolar	Active "H"	3.0 mT typ.
S-5719ACDL2-I4T1U	531.2 ms typ.	CMOS output	Omnipolar	Active "L"	4.5 mT typ.
S-5719ACDH2-I4T1U	531.2 ms typ.	CMOS output	Omnipolar	Active "H"	4.5 mT typ.
S-5719BCDL0-I4T1U	133.2 ms typ.	CMOS output	Omnipolar	Active "L"	1.8 mT typ.
S-5719BCDH0-I4T1U	133.2 ms typ.	CMOS output	Omnipolar	Active "H"	1.8 mT typ.
S-5719BCDL1-I4T1U	133.2 ms typ.	CMOS output	Omnipolar	Active "L"	3.0 mT typ.
S-5719BCDH1-I4T1U	133.2 ms typ.	CMOS output	Omnipolar	Active "H"	3.0 mT typ.
S-5719BCDL2-I4T1U	133.2 ms typ.	CMOS output	Omnipolar	Active "L"	4.5 mT typ.
S-5719BCDH2-I4T1U	133.2 ms typ.	CMOS output	Omnipolar	Active "H"	4.5 mT typ.

Remark Please contact our sales representatives for products other than the above.

■ Pin Configuration

1. SNT-4A

Top view

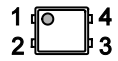


Figure 2

Table 3

Pin No.	Symbol	Pin Description
1	VDD	Power supply pin
2	VSS	GND pin
3	NC*1	No connection
4	OUT	Output pin

*1. The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applicable Pin	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	-	V_{SS} - 0.3 to V_{SS} + 7.0	V
Output current	I_{OUT}	OUT	±1.0	mA
Output voltage	V_{OUT}	OUT	V_{SS} - 0.3 to V_{DD} + 0.3	V
Operation ambient temperature	T_{opr}	-	-40 to +85	°C
Storage temperature	T_{stg}	-	-40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SNT-4A	Board A	-	300	-	°C/W
			Board B	-	242	-	°C/W
			Board C	-	-	-	°C/W
			Board D	-	-	-	°C/W
			Board E	-	-	-	°C/W

*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. S-5719ACDxx

Table 6

(Ta = +25°C, V_{DD} = 1.5 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	-	1.3	1.5	3.6	V	-
Current consumption	I_{DD}	Average value	-	0.2	0.5	μA	1
High level output voltage	V_{OH}	I_{OUT} = -0.5 mA	V_{DD} - 0.4	-	-	V	2
Low level output voltage	V_{OL}	I_{OUT} = 0.5 mA	-	-	0.4	V	3
Awake mode time	t_{AW}	-	-	0.2	-	ms	-
Sleep mode time	t_{SL}	-	-	531.0	-	ms	-
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}	-	531.2	1300.0	ms	-

2. S-5719BCDxx

Table 7

(Ta = +25°C, V_{DD} = 1.5 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	-	1.3	1.5	3.6	V	-
Current consumption	I_{DD}	Average value	-	0.5	0.8	μA	1
High level output voltage	V_{OH}	I_{OUT} = -0.5 mA	V_{DD} - 0.4	-	-	V	2
Low level output voltage	V_{OL}	I_{OUT} = 0.5 mA	-	-	0.4	V	3
Awake mode time	t_{AW}	-	-	0.2	-	ms	-
Sleep mode time	t_{SL}	-	-	133.0	-	ms	-
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}	-	133.2	320.0	ms	-

■ Magnetic Characteristics

1. Product with B_{OP} = 1.8 mT typ.

Table 8

(T_a = +25°C, V_{DD} = 1.5 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	-	0.6	1.8	3.0	mT	4
	N pole	B_{OPN}	-	-3.0	-1.8	-0.6	mT	4
Release point*2	S pole	B_{RPS}	-	0.1	1.1	2.4	mT	4
	N pole	B_{RPN}	-	-2.4	-1.1	-0.1	mT	4
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	-	0.7	-	mT	4
	N pole	B_{HYSN}	$B_{HYSN} = \|B_{OPN} - B_{RPN}\|$	-	0.7	-	mT	4

2. Product with B_{OP} = 3.0 mT typ.

Table 9

(T_a = +25°C, V_{DD} = 1.5 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	-	1.6	3.0	4.0	mT	4
	N pole	B_{OPN}	-	-4.0	-3.0	-1.6	mT	4
Release point*2	S pole	B_{RPS}	-	1.1	2.2	3.7	mT	4
	N pole	B_{RPN}	-	-3.7	-2.2	-1.1	mT	4
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	-	0.8	-	mT	4
	N pole	B_{HYSN}	$B_{HYSN} = \|B_{OPN} - B_{RPN}\|$	-	0.8	-	mT	4

3. Product with B_{OP} = 4.5 mT typ.

Table 10

(T_a = +25°C, V_{DD} = 1.5 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	-	2.5	4.5	6.0	mT	4
	N pole	B_{OPN}	-	-6.0	-4.5	-2.5	mT	4
Release point*2	S pole	B_{RPS}	-	2.0	3.5	5.5	mT	4
	N pole	B_{RPN}	-	-5.5	-3.5	-2.0	mT	4
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	-	1.0	-	mT	4
	N pole	B_{HYSN}	$B_{HYSN} = \|B_{OPN} - B_{RPN}\|$	-	1.0	-	mT	4

1. B_{OPN}, B_{OPS}: Operation points
B_{OPN} and B_{OPS} are the values of magnetic flux density when the output voltage (V_{OUT}) changes after the magnetic flux density applied to this IC by the magnet (N pole or S pole) is increased (by moving the magnet closer).
Even when the magnetic flux density exceeds B_{OPN} or B_{OPS}, V_{OUT} retains the status.

***2.** B_{RPN}, B_{RPS}: Release points
B_{RPN} and B_{RPS} are the values of magnetic flux density when the output voltage (V_{OUT}) changes after the magnetic flux density applied to this IC by the magnet (N pole or S pole) is decreased (the magnet is moved further away).
Even when the magnetic flux density falls below B_{RPN} or B_{RPS}, V_{OUT} retains the status.

***3.** B_{HYSN}, B_{HYSS}: Hysteresis widths
B_{HYSN} and B_{HYSS} are the difference between B_{OPN} and B_{RPN}, and B_{OPS} and B_{RPS}, respectively.

Remark The unit of magnetic density mT can be converted by using the formula 1 mT = 10 Gauss.

■ Test Circuits

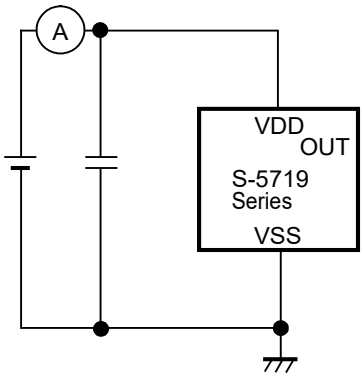


Figure 3 Test Circuit 1

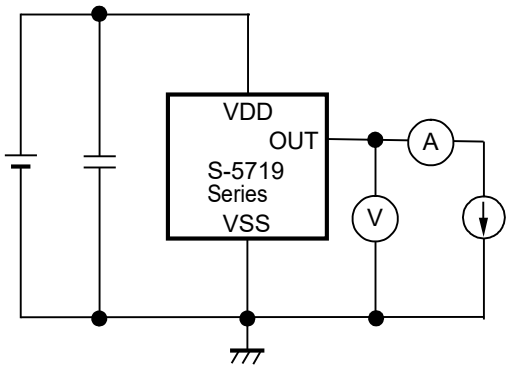


Figure 4 Test Circuit 2

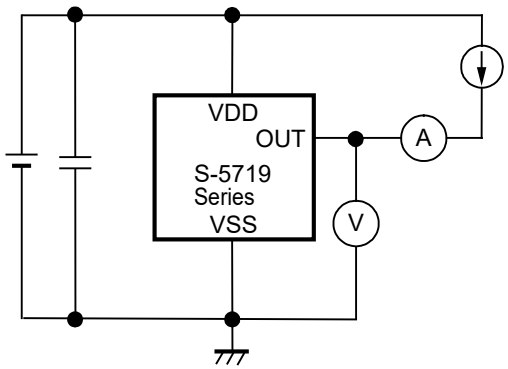


Figure 5 Test Circuit 3

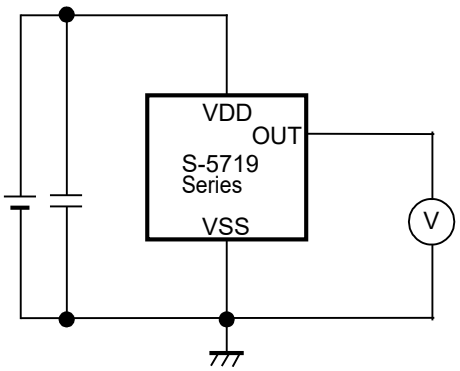


Figure 6 Test Circuit 4

■ Standard Circuit

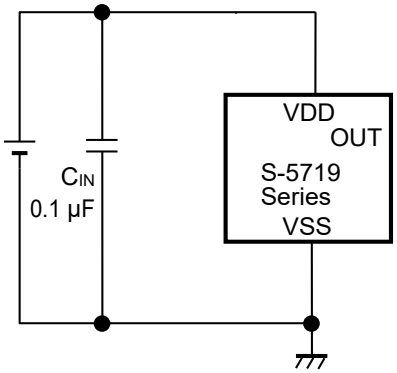


Figure 7

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

■ Operation

1. Direction of applied magnetic flux

This IC detects the flux density which is vertical to the marking surface.
Figure 8 shows the direction in which magnetic flux is being applied.

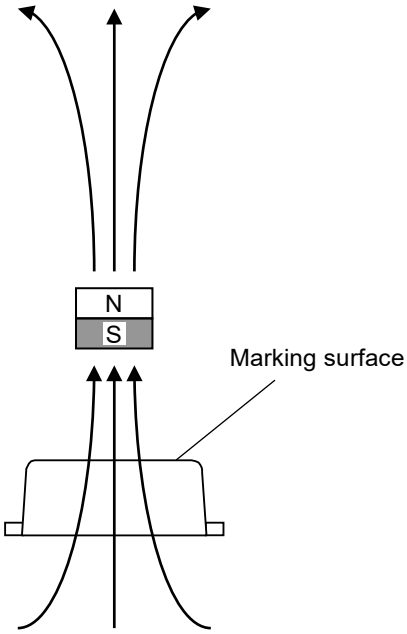


Figure 8

2. Position of Hall sensor

Figure 9 shows the position of Hall sensor.
The center of this Hall sensor is located in the area indicated by a circle, which is in the center of a package as described below.
The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.

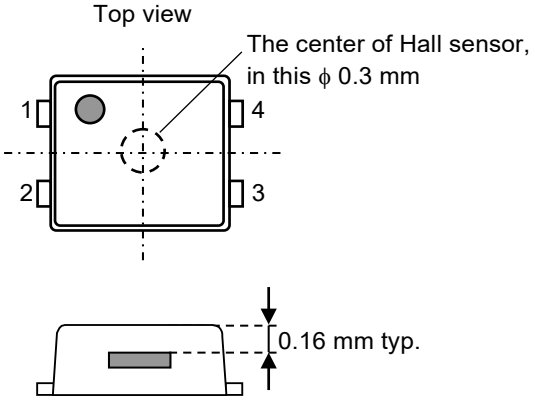


Figure 9

3. Basic operation

This IC changes the output voltage level (V_{OUT}) according to the level of the magnetic flux density (N pole or S pole) applied by a magnet.
The following explains the operation when the output logic is active "L".

When the magnetic flux density vertical to the marking surface exceeds the operation point (B_{OPN} or B_{OPS}) after the N pole or S pole of a magnet is moved closer to the marking surface of this IC, V_{OUT} changes from "H" to "L". When the N pole or S pole of a magnet is moved further away from the marking surface of this IC and the magnetic flux density is lower than the release point (B_{RPN} or B_{RPS}), V_{OUT} changes from "L" to "H".
Figure 10 shows the relationship between the magnetic flux density and V_{OUT}.

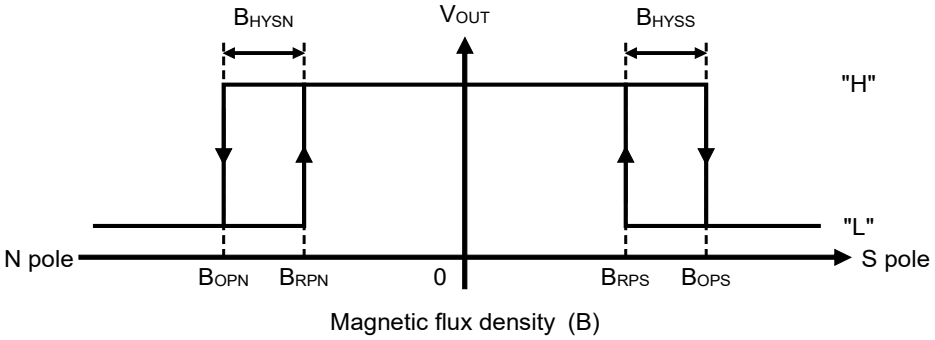


Figure 10

4. Time dependency in the current consumption

This IC performs the intermittent operation, and operates at super low current consumption due to repeating the sleep mode and the awake mode.
Figure 11 shows the time dependency in the current consumption.

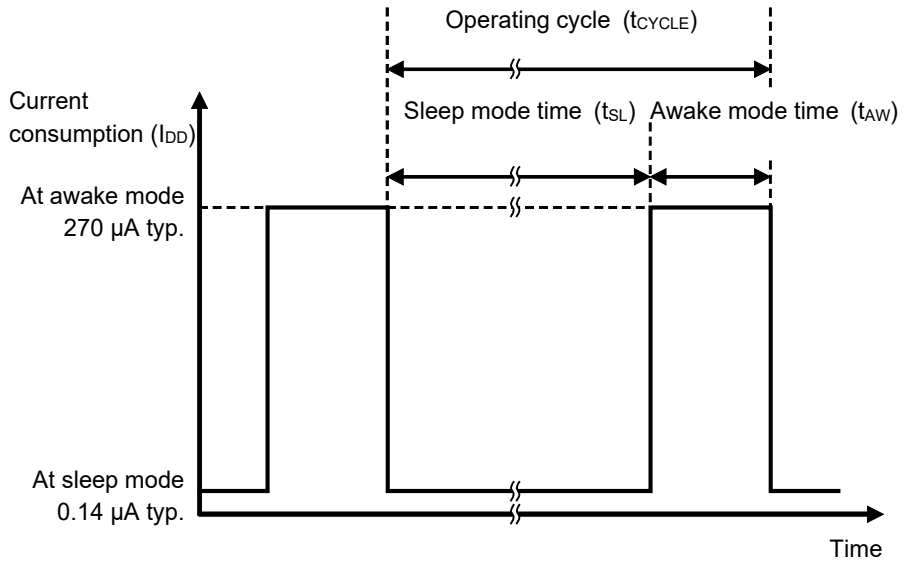


Figure 11

5. Timing chart for magnetic flux density response

Figure 12 shows the operation timing chart for active "L" products.

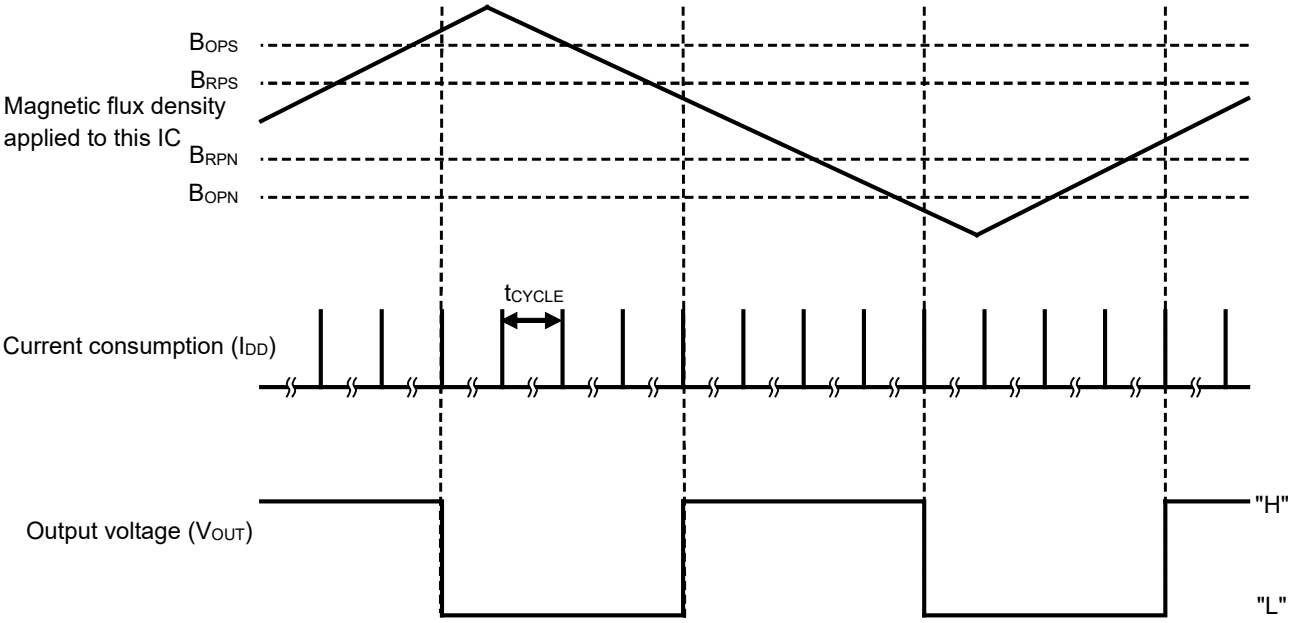


Figure 12

■ Precautions

- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.

- Note that the IC may malfunction if the power supply voltage rapidly changes. When the IC is used under the environment where the power supply voltage rapidly changes, it is recommended to judge the output voltage of the IC by reading it multiple times.

- Note that the IC may malfunction in the following situations.
  When the OUT pin is shorted to VSS pin or VDD pin.
  When the OUT pin is affected by noise.
  When the intermediate potential is applied to the OUT pin.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- Large stress on this IC may affect the magnetic characteristics. Avoid large stress which is caused by the handling during or after mounting the IC on a board.

- Note that the output voltage may change if the intermediate value of magnetic flux density between the operation point and release point is applied to this IC over a long time.

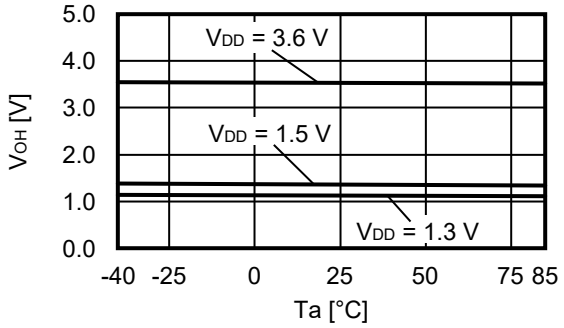
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

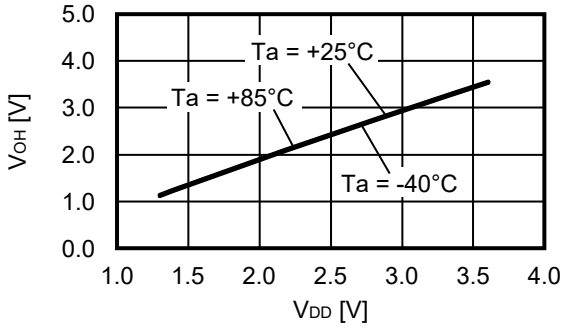
1. Electrical Characteristics

1. 1 Output voltage

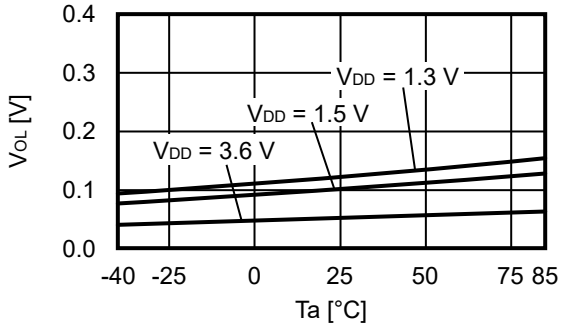
1. 1. 1 High level output voltage (V_{OH}) vs. Temperature (Ta)



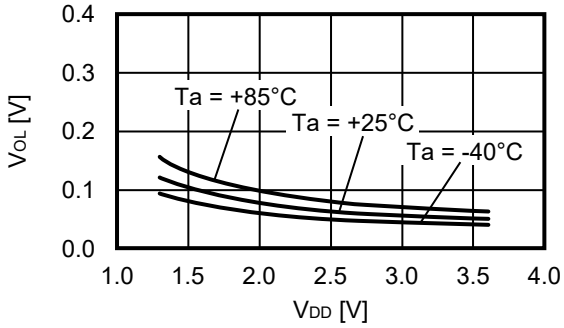
1. 1. 2 High level output voltage (V_{OH}) vs. Power supply voltage (V_{DD})



1. 1. 3 Low level output voltage (V_{OL}) vs. Temperature (Ta)

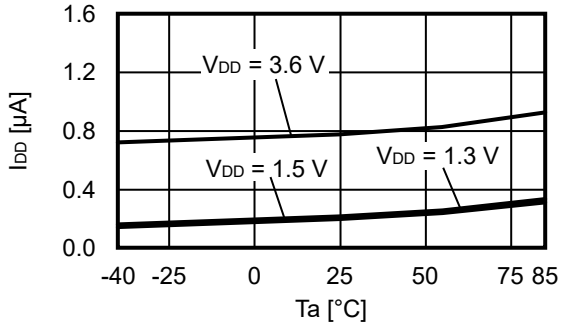


1. 1. 4 Low level output voltage (V_{OL}) vs. Power supply voltage (V_{DD})

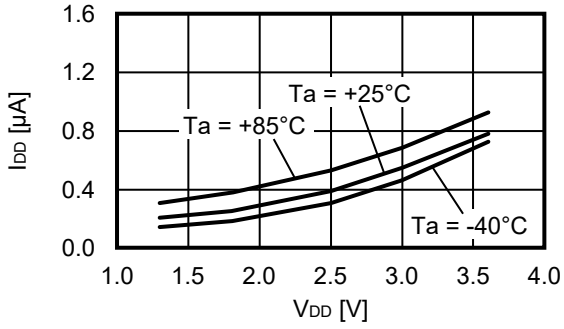


1. 2 S-5719ACDxx

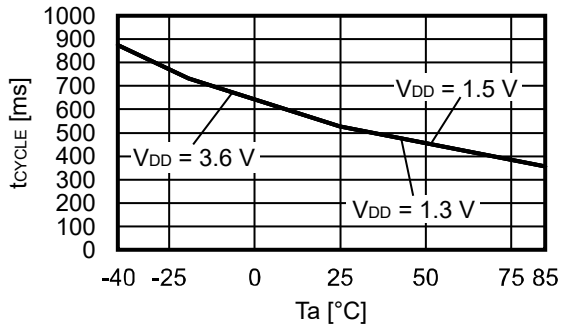
1. 2. 1 Current consumption (I_{DD}) vs Temperature (Ta)



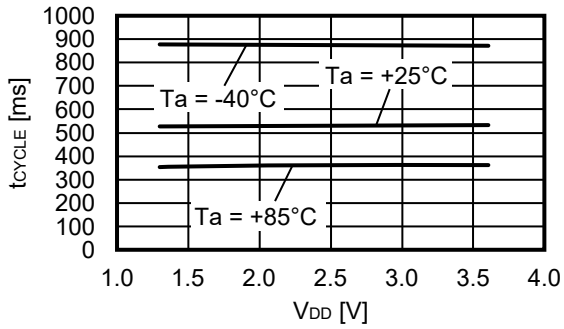
1. 2. 2 Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



1. 2. 3 Operating cycle (t_{CYCLE}) vs. Temperature (Ta)

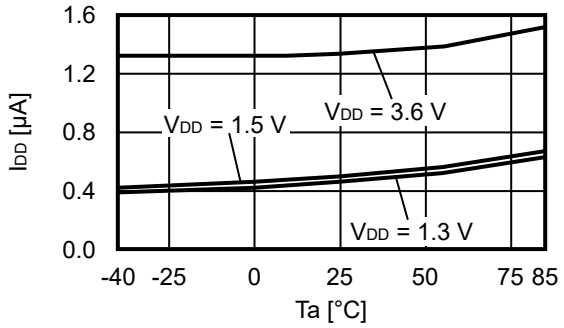


1. 2. 4 Operating cycle (t_{CYCLE}) vs. Power supply voltage (V_{DD})

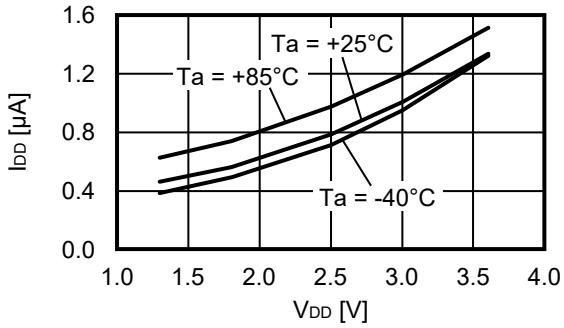


1. 3 S-5719BCDxx

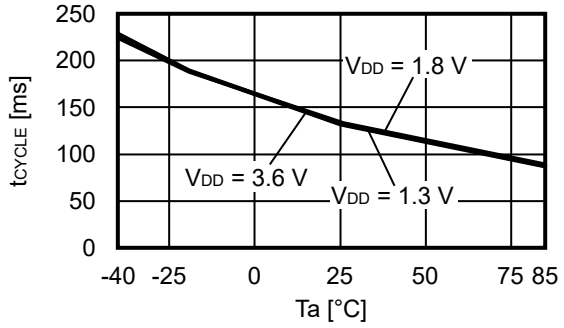
1. 3. 1 Current consumption (I_{DD}) vs. Temperature (Ta)



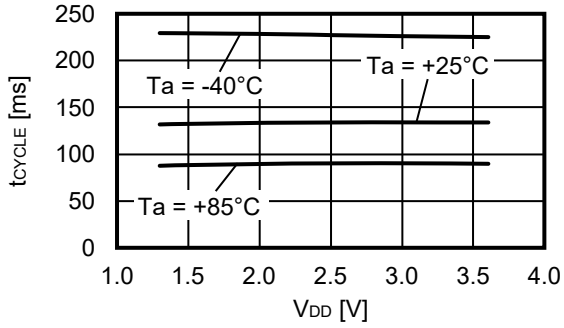
1. 3. 2 Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



1. 3. 3 Operating cycle (t_{CYCLE}) vs. Temperature (Ta)



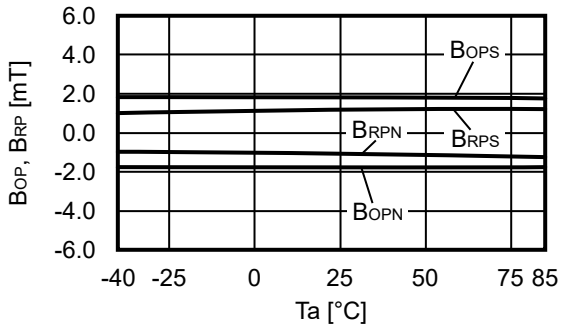
1. 3. 4 Operating cycle (t_{CYCLE}) vs. Power supply voltage (V_{DD})



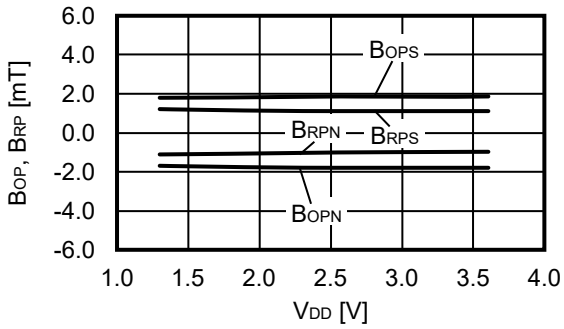
2. Magnetic Characteristics

2. 1 S-5719xCDx0

2. 1. 1 Operation point, Release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

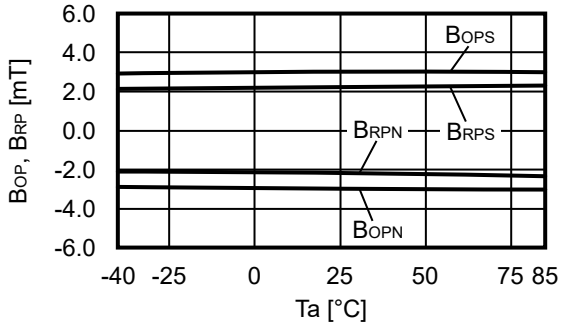


2. 1. 2 Operation point, Release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

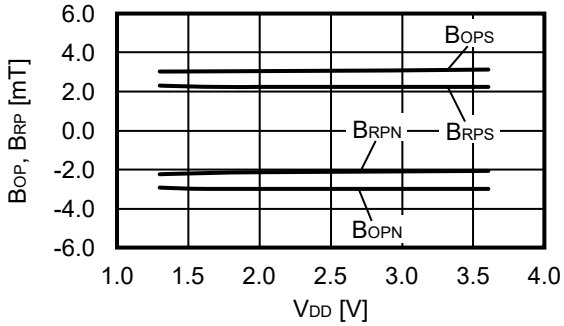


2. 2 S-5719xCDx1

2. 2. 1 Operation point, Release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

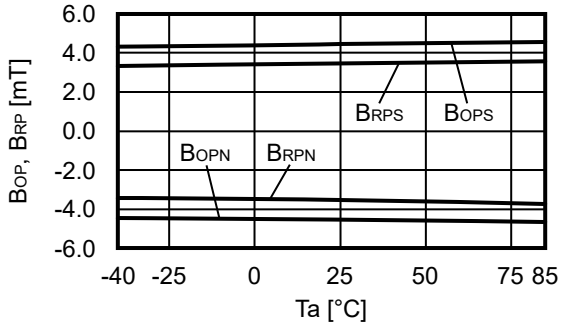


2. 2. 2 Operation point, Release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

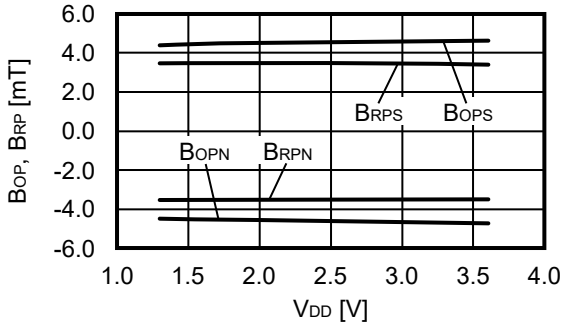


2. 3 S-5719xCDx2

2. 3. 1 Operation point, Release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

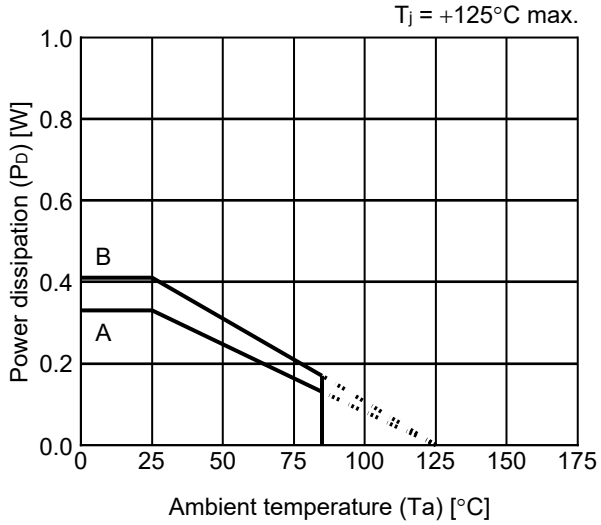


2. 3. 2 Operation point, Release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})



■ Power Dissipation

SNT-4A

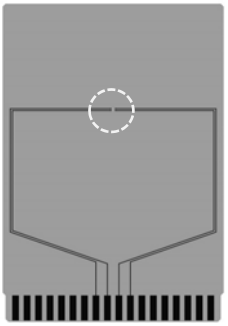


Board	Power Dissipation (P_D)
A	0.33 W
B	0.41 W
C	-
D	-
E	-

SNT-4A Test Board

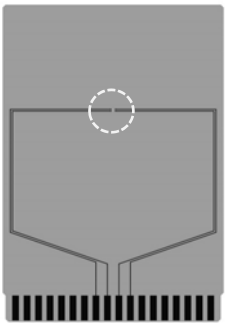
IC Mount Area

(1) Board A



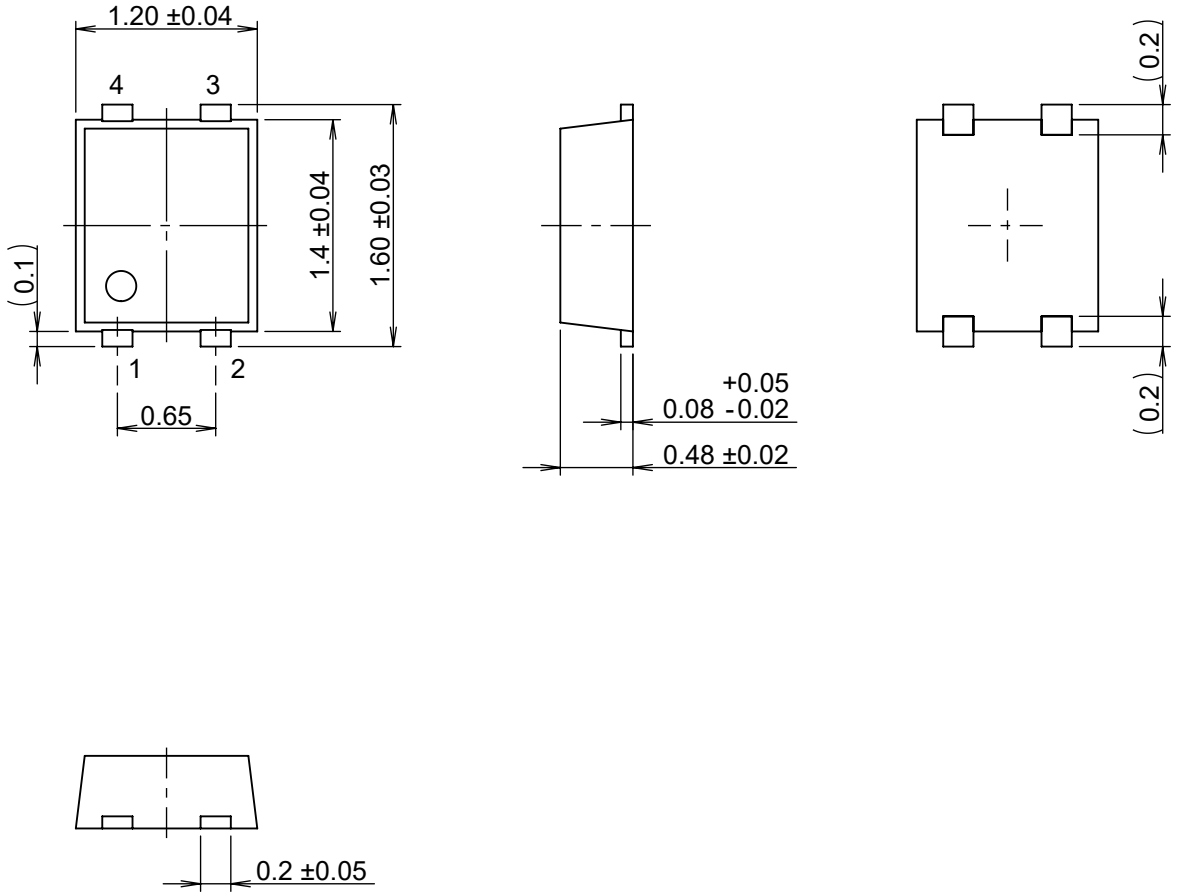
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



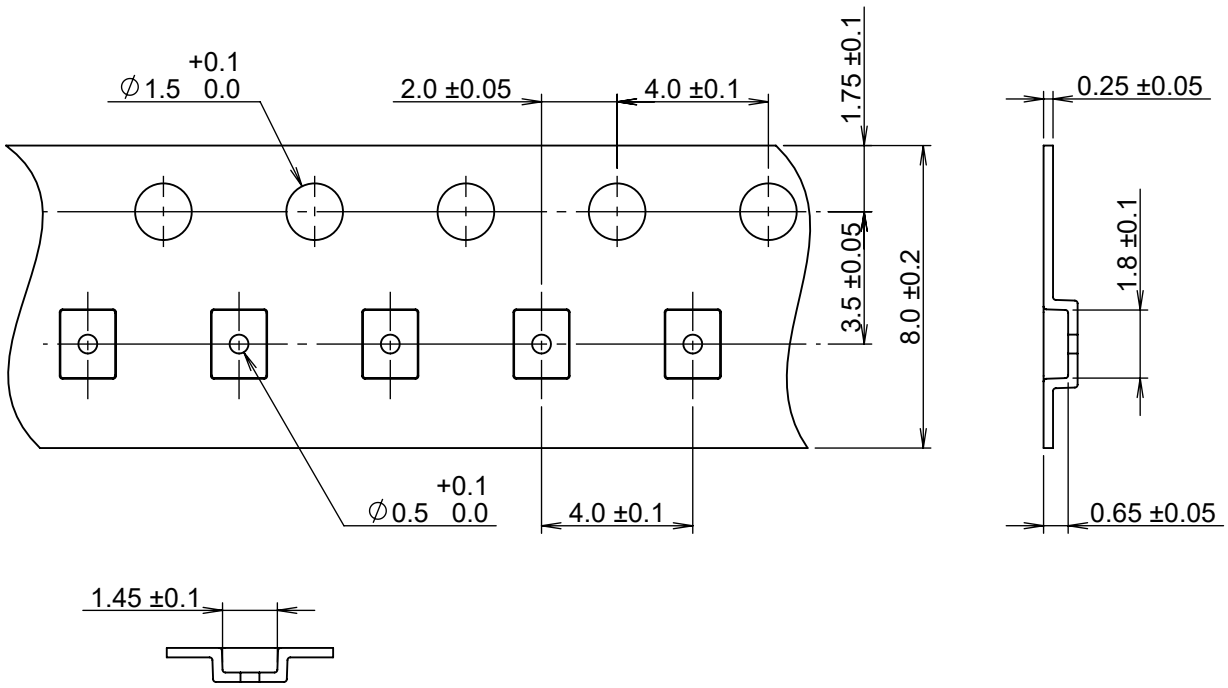
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

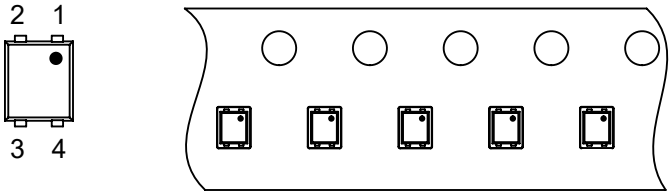
No. SNT4A-A-Board-SD-1.0



No. PF004-A-P-SD-6.0

TITLE	SNT-4A-A-PKG Dimensions
No.	PF004-A-P-SD-6.0
ANGLE	
UNIT	mm
ABLIC Inc.	

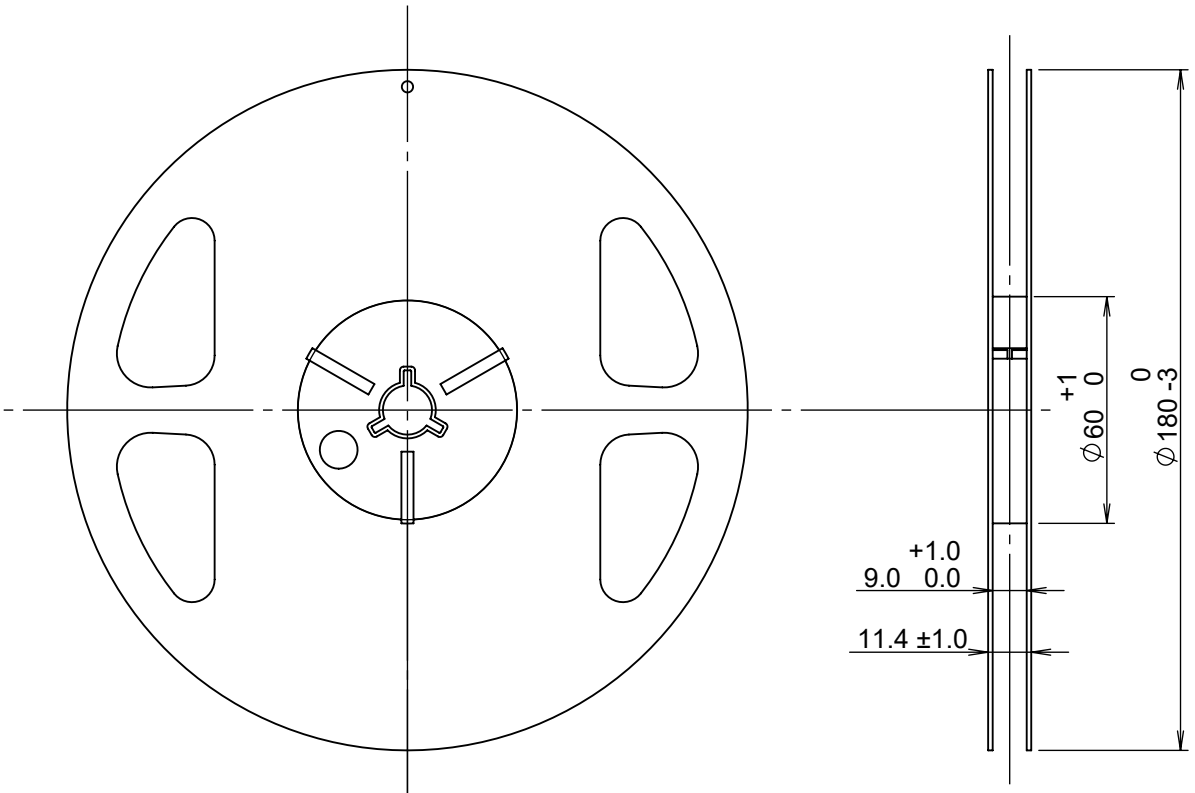




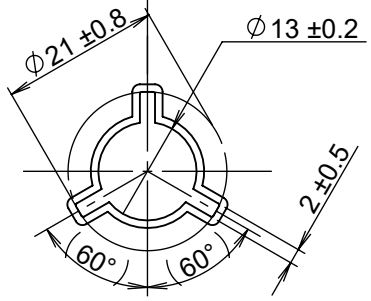
Feed direction

No. PF004-A-C-SD-2.0

TITLE	SNT-4A-A-Carrier Tape
No.	PF004-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

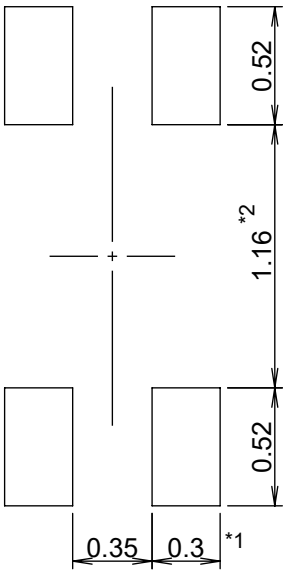


Enlarged drawing in the central part



No. PF004-A-R-SD-2.0

TITLE	SNT-4A-A-Reel		
No.	PF004-A-R-SD-2.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



***1.** ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
***2.** パッケージ中央にランドパターンを広げないでください (1.10 mm ~ 1.20 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は "SNTパッケージ活用の手引き" を参照してください。

***1.** Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
***2.** Do not widen the land pattern to the center of the package (1.10 mm to 1.20 mm).

Caution
1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

***1.** 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
***2.** 请勿向封装中间扩展焊盘模式 (1.10 mm ~ 1.20 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在0.03 mm以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT封装的应用指南"。

No. PF004-A-L-SD-4.1

TITLE	SNT-4A-A -Land Recommendation
No.	PF004-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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