RC4277

Dual Precision Operational Amplifier

Features

- High DC precision
- Very low VOS – 30 μV
- Very low VOS drift – 0.3 μV/°C
- High open-loop gain – 5000 V/mV
- High CMRR – 120 dB
- High PSRR – 120 db
- Low noise – 0.35 μV_{p-p} (0.1 Hz to 10 Hz)
- Low input bias current – 3.0 nA
- Low power consumption – 140 mW

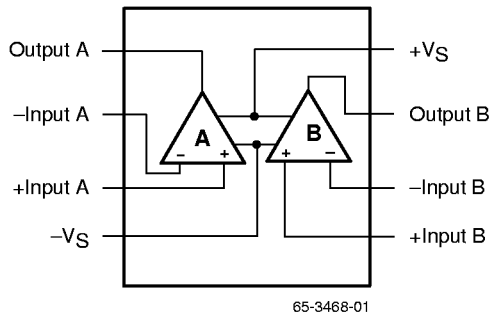
Description

The RC4277 provides the highest precision available in a dual bipolar operational amplifier. A monolithic dual version of the RC4077, the RC4277 is designed to replace OP-07 and OP-77 type amplifiers in applications requiring high PC board layout density. The RC4277 has a well-balanced, mutually supporting set of input specifications. Low V_{OS}, low I_B, high open-loop gain, and excellent matching characteristics combine to raise the performance level of many instrumentation, low-level signal conditioning, and data conversion applications. PSRR, CMRR, V_{OS} drift, and noise levels also support high precision operation.

The high performance of the RC4277 results from two innovative and unconventional manufacturing steps, plus careful circuit layout and design. The key steps are SiCr thin-film resistor deposition and post-package trimming of the input offset voltage characteristic. The low 75 μV max V_{OS} specification is maintained in high-volume production by way of the post-package trim procedure, where internal resistors are trimmed through the device input leads at the final test operation. Devices retain this low offset through the stability and accuracy of the trimmed thin-film resistors.

The RC4277 is available in 8-lead plastic and ceramic DIPs.

Block Diagram



Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±22	V
Input Voltage[2]				±22	V
Differential Input Voltage				30	V
Internal Power Dissipation[3]				500	mW
$P_D T_A$ < 50°C	PDIP			468	mW
	CerDIP			833	
Output Short Circuit Duration		Indefinite			
Junction Temperature	PDIP			125	°C
	CerDIP			175	
Storage Temperature		-65		150	°C
Operating Temperature	RV4277	-25		85	°C
	RC4277	0		70	
Lead Soldering Temperature (60 sec)				300	°C
For T_A > 50°C Derate at	PDIP		6.25		mW/°C
	CerDIP		8.33		

Notes:

1. Functional operation under any of these conditions is NOT implied.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Observe package thermal characteristics.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	CerDIP		45		°C/W
θ_{JA}	Thermal resistance	PDIP		160		°C/W
		CerDIP		150		°C/W

Electrical Characteristics

(V_S = ±15V, and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage[3]			30	75	µV
Input Voltage Offset Match			25	150	µV
Long Term V_{OS} Stability[1]			0.3		µV/Mo
Input Offset Current			0.5	5.0	nA
Input Bias Current			±0.5	±5.0	nA
Input Noise Voltage	0.1 Hz to 10 Hz		0.35		μV_{p-p}
Input Noise Voltage Density	F_O = 10 Hz		10.3		$\frac{nV}{\sqrt{Hz}}$
	F_O = 100 Hz		10		
	F_O = 1000 Hz		9.6		
Input Noise Current Density	F_O = 10 Hz		0.32		$\frac{pA}{\sqrt{Hz}}$
	F_O = 100 Hz		0.14		
	F_O = 1000 Hz		0.12		
Input Voltage Range[2, 4]		±11	±14		V
Common Mode Rejection Ratio	V_{CM} = ±11V	110	132		dB
Power Supply Rejection Ratio	V_S = ±4V to ±16.5V	110	132		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	1300	350		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		
	$R_L \geq 1k\Omega$	±11	±12		
Slew Rate	$R_L \geq 2k\Omega$	0.1	0.3		V/µs
Closed Loop Bandwidth	A_{VCL} = +1.0		0.8		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		60	100	mW
Crosstalk		126	155		dB

Notes:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of VOS vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in VOS during the first 30 operating days are typically 2.5 µV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

Electrical Characteristics

(V_S = ±15V, 0°C ≤ T_A ≤ +70˚C unless otherwise noted)

Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	0°C ≤ T_A ≤ +70°C		50	120	µV
	-25°C ≤ T_A ≤ +85°C		50	135	
Average Input Offset Voltage Drift[2]			0.3	1.0	µV/°C
Input Offset Current			1.5	5.0	nA
Input Bias Current			±1.5	±5.0	nA
Input Voltage Range		±10	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	110	124		dB
Power Supply Rejection Ratio	V_S = ±4V to ±16.5V	110	124		dB
Large Signal Voltage Gain	R_L > 2kΩ, V_{OUT} = ±10V	1300	3000		V/mV
Output Voltage Swing	R_L > 2kΩ	±11	±12.6		V
Power Consumption	R_L = ∞		70	120	mW

Notes:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.

Typical Applications

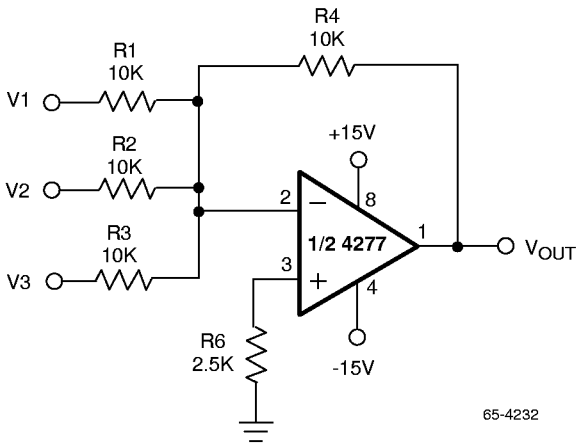


Figure 1. Adjustment-Free Precision Summing Amplifier

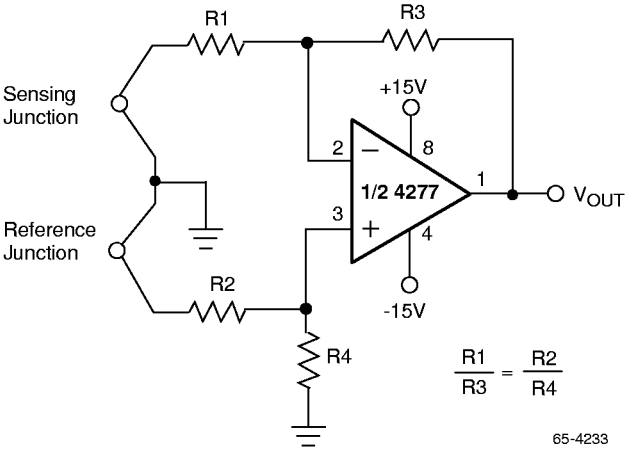


Figure 2. High Stability Thermocouple Amplifier

Typical Applications (continued)

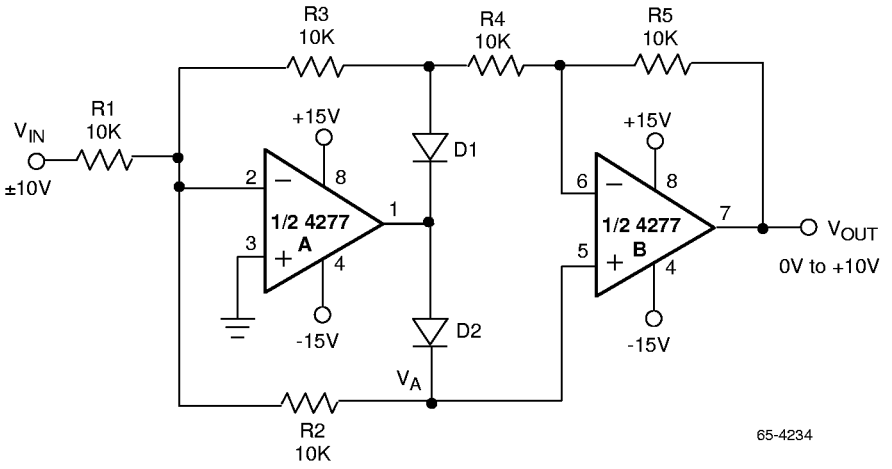
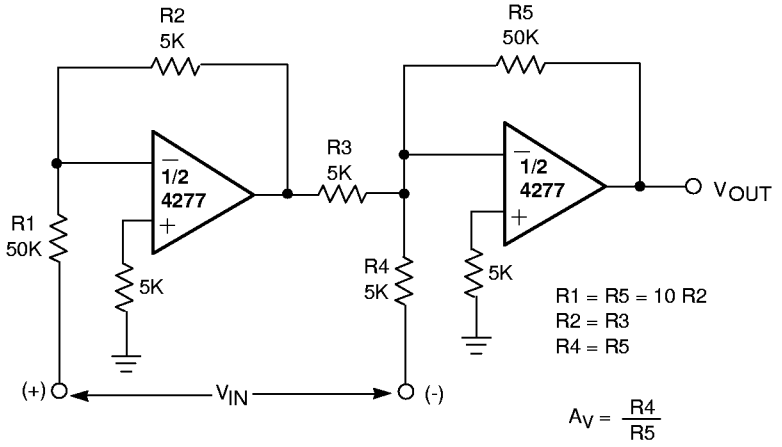


Figure 3. Precision Absolute Value Circuit



Note: This circuit can tolerate input voltages that exceed the 4277's supply voltage rating as long as the slew rate do not exceed the op amp's slew rate.

Figure 4. High Voltage Differential Amplifier

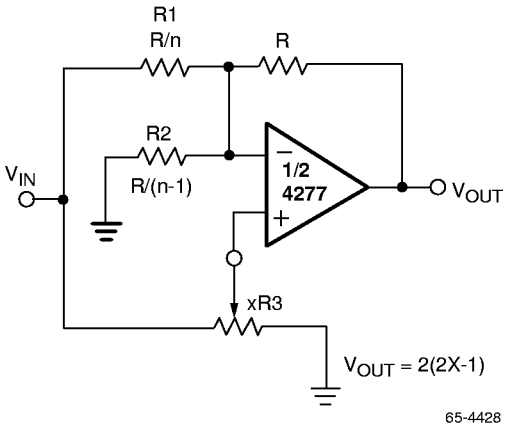


Figure 5. Polarity Changing Gain Controlled Amplifier

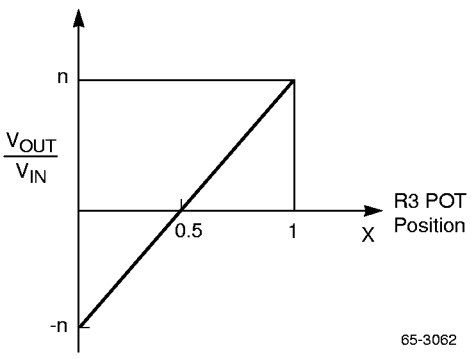


Figure 6. Gain Controlled Amplifier Transfer Function

Typical Applications (continued)

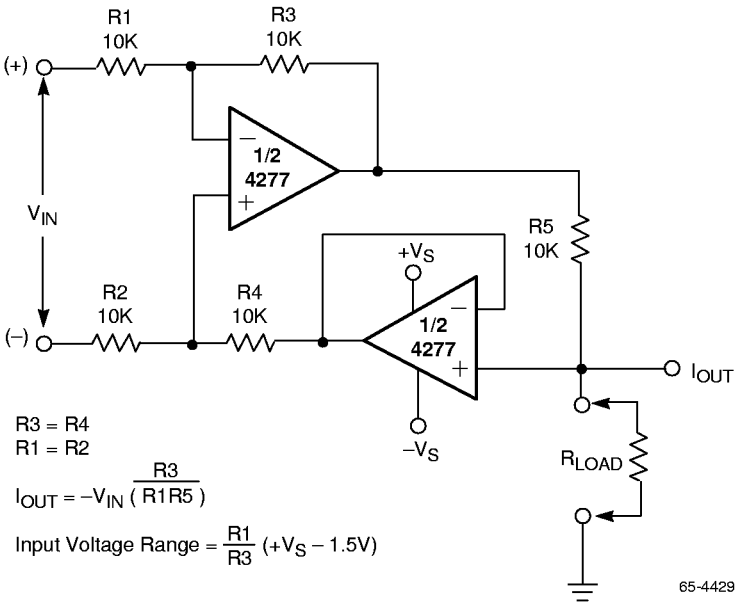


Figure 7. Differential Input Current Source

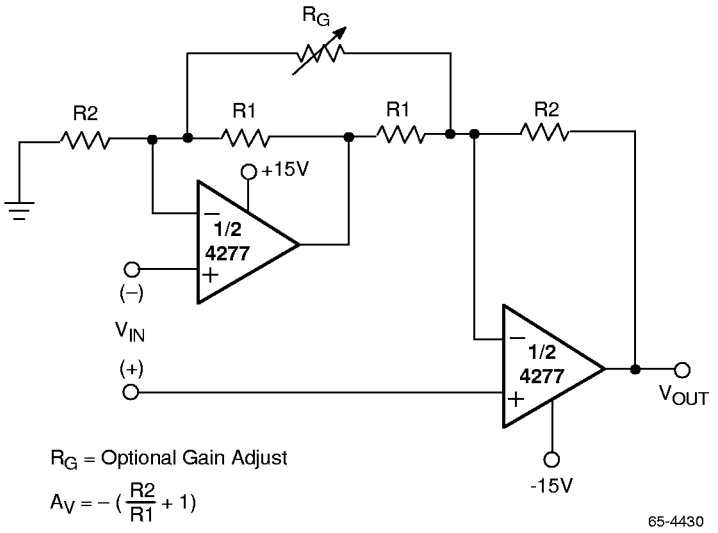


Figure 8. High Input Impedance Subtractor

Typical Applications (continued)

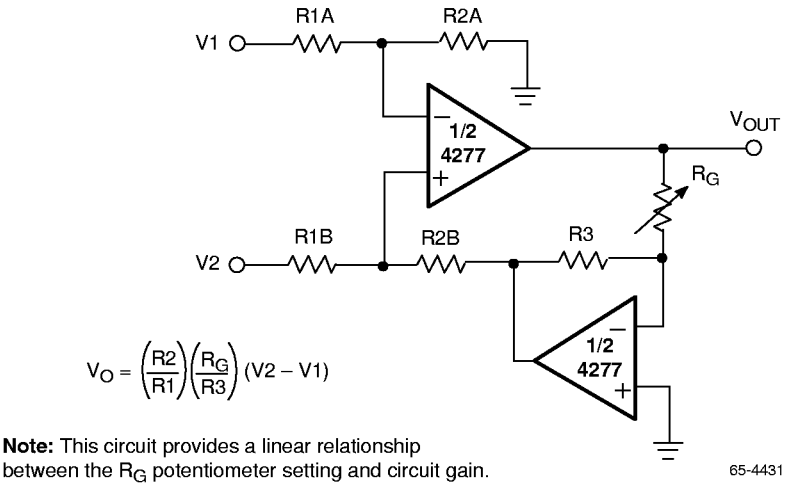


Figure 9. Difference Amplifier with Linear Gain Control

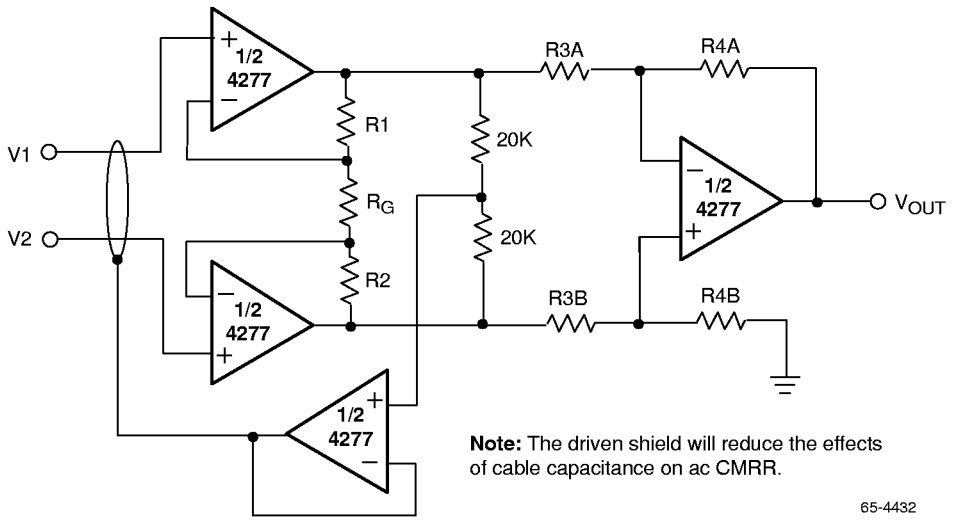
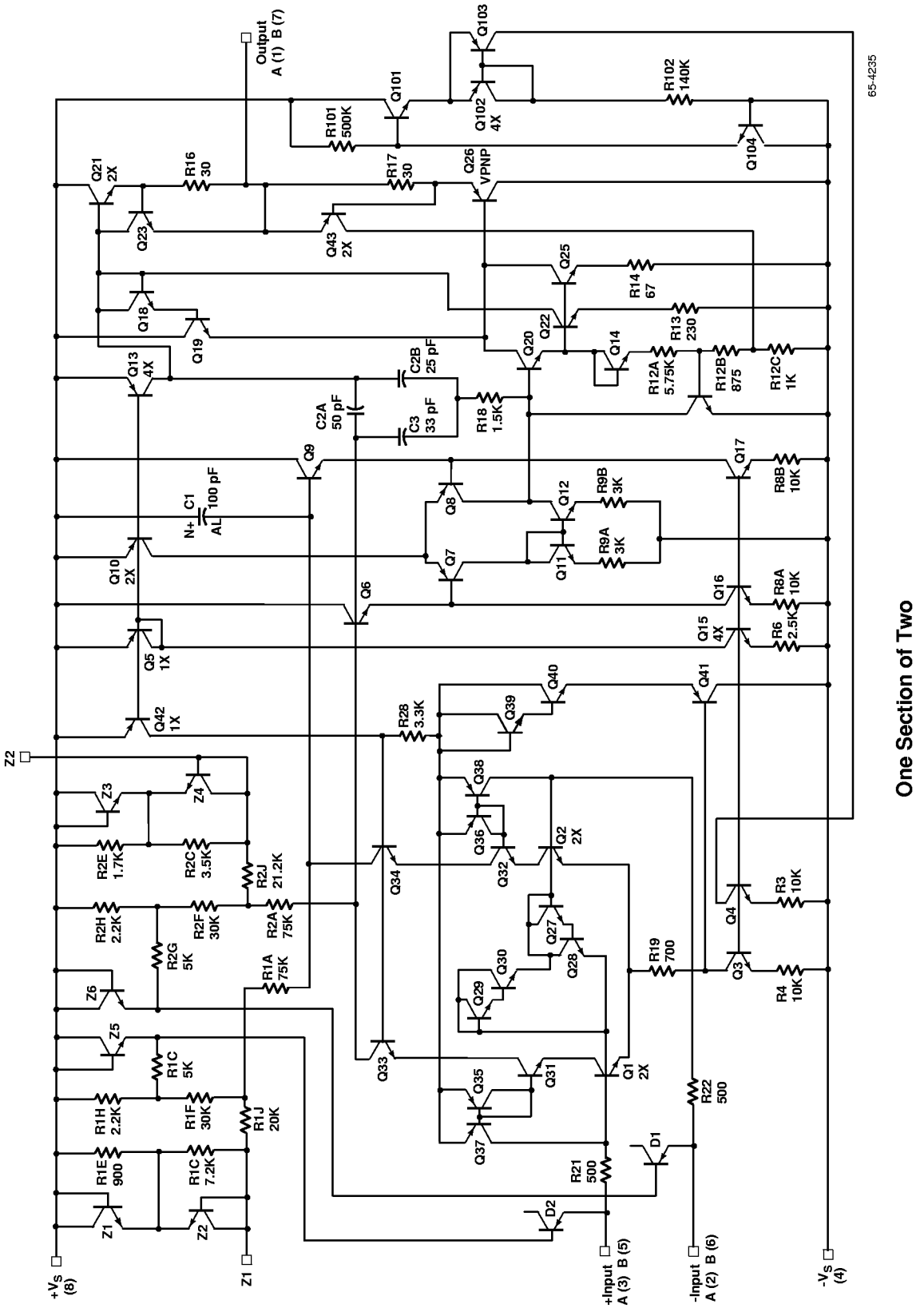


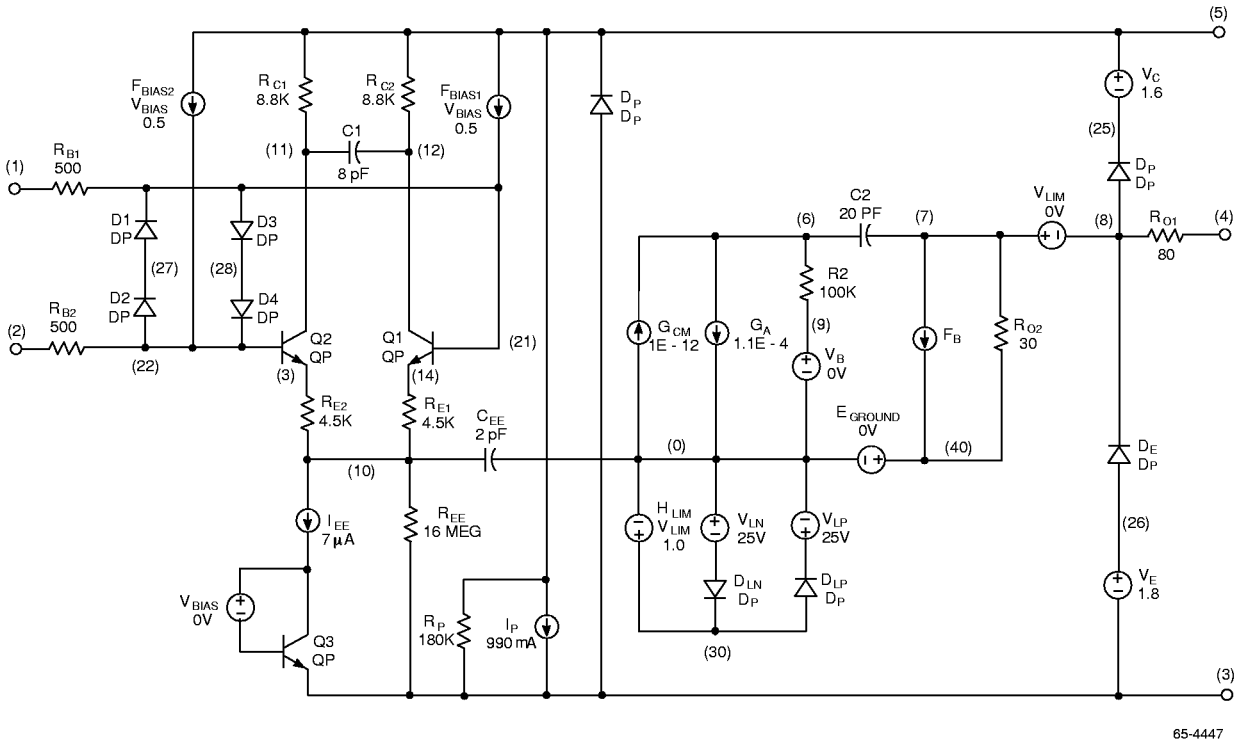
Figure 10. Three Op Amp Instrumentation Amplifier with Driven Shield

Schematic Diagram



RM4277 SPICE Macro Model

This circuit models AC and DC characteristics including slew rate, bandwidth, V_{OS}, I_B, I_{OS}, CMRR, output voltage range, and gain. The circuit produces typical values for these parameters.



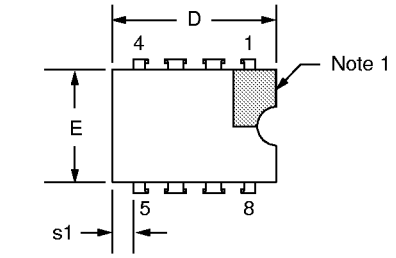
Mechanical Dimensions

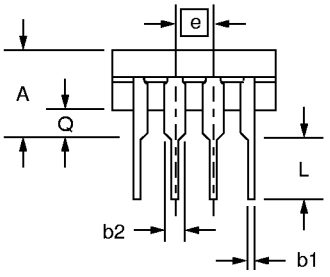
8-Lead Ceramic DIP Package

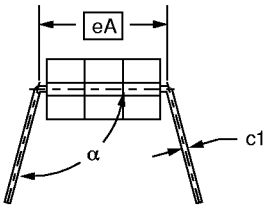
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







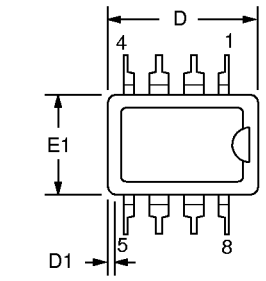
Mechanical Dimensions (continued)

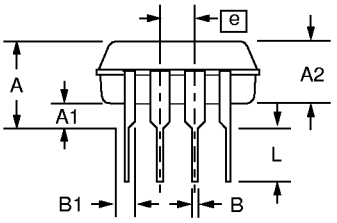
8-Lead Plastic DIP Package

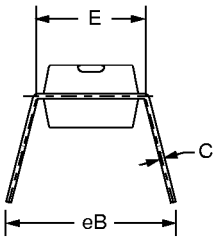
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package
RC4277FN	0°C to +70°C	Commercial	8 Pin Plastic DIP
RV4277FD	0°C to 70°C	Commercial	8 Pin Ceramic DIP

5/20/98 0.0m 001
Stock#DS30004277