8A, 6.5V, 2.1MHz, ACOT® Synchronous Step-Down Converter with I²C Interface

General Description

The RTQ2159 is a high-performance, synchronous step-down DC-DC converter that can deliver up to 8A output current from a 2.85V to 6.5V input supply. The output voltage can be programmed from 0.6V to 1.5V with I²C controlled 7-Bits VID.

The device integrates low $R_{DS(ON)}$ power MOSFETs, accurate reference voltage and an integrated diode of bootstrap circuit to offer a very compact solution.

The RTQ2159 adopts Advanced Constant On-Time (ACOT®) control architecture that provides ultrafast transient response and further reduces the external-component count. In steady states, the ACOT® operates in nearly constant switching frequency over line, load and output voltage ranges and makes the EMI filter design easier. The RTQ2159 operations in Forced-CCM that helps meet tight voltage regulation accuracy requirements.

The device offers independent enable control input pin and power good indicator for easily sequence control. To control the inrush current during the startup, the device provides a programmable soft-start up by an external capacitor connected to the SS pin. Fully protection features are also integrated in the device including the cycle-by-cycle current limit control, UVP, input UVLO and OTP. The RTQ2159 is available in a thermally enhanced WET-WQFN-21L 4x4 (FC) package.

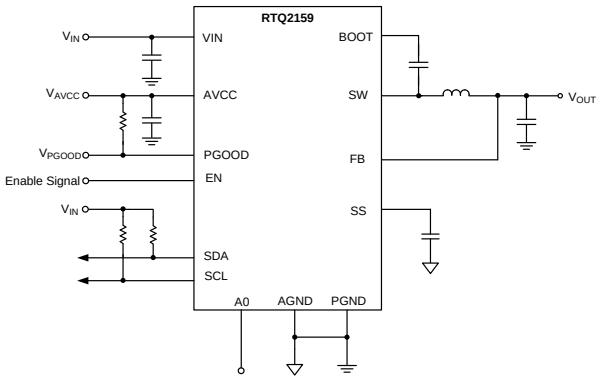
Features

- **AEC-Q100 Grade 1 Qualified**
- **Dramatically Fast Transient Response**
- **Selectable Switching Frequency (0.46MHz / 0.69MHz / 0.92MHz / 2.1MHz)**
- **Extremely High Efficiency 15mΩ/10mΩ MOSFETs**
- **Advanced COT Control Loop**
- **Wide Input Voltage Range from 2.85V to 6.5V**
- **Optimized for Ceramic Output Capacitors**
- **Internal Start-Up into Pre-biased Outputs**
- **Power Good Indicator**
- **Enable Control**
- **Over-Current and Over-Temperature Protections**
- **Under-Voltage Protection with Hiccup Mode**
- **VID Control Range Via I²C Compatible Interface : 0.6V to 1.5V step = 10mV**

Applications

- Automotive Systems
- Infotainment and Cockpit Systems
- Vehicle ADAS ECU
- Connected Car Systems
- High Density DDR Memory
- Broadband Communications and Industrial Systems

Simplified Application Circuit



Ordering Information

RTQ2159□□-QA

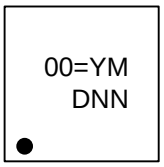
- Grade
  QA : AEC-Q100 Qualified and Screened by High Temperature
- Package Type
  QWTF : WET-WQFN-21L 4x4 (FC) (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

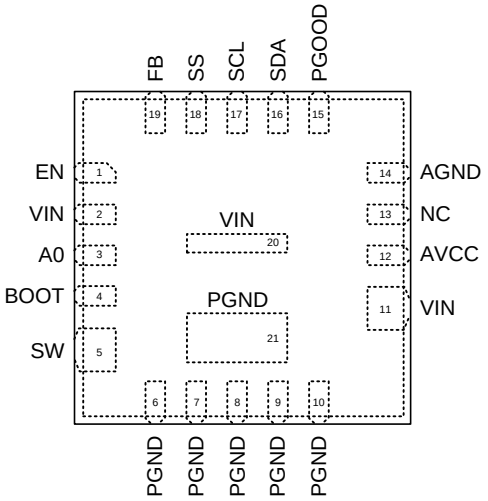
Marking Information



00= : Product Code
YMDNN : Date Code

Pin Configuration

(TOP VIEW)

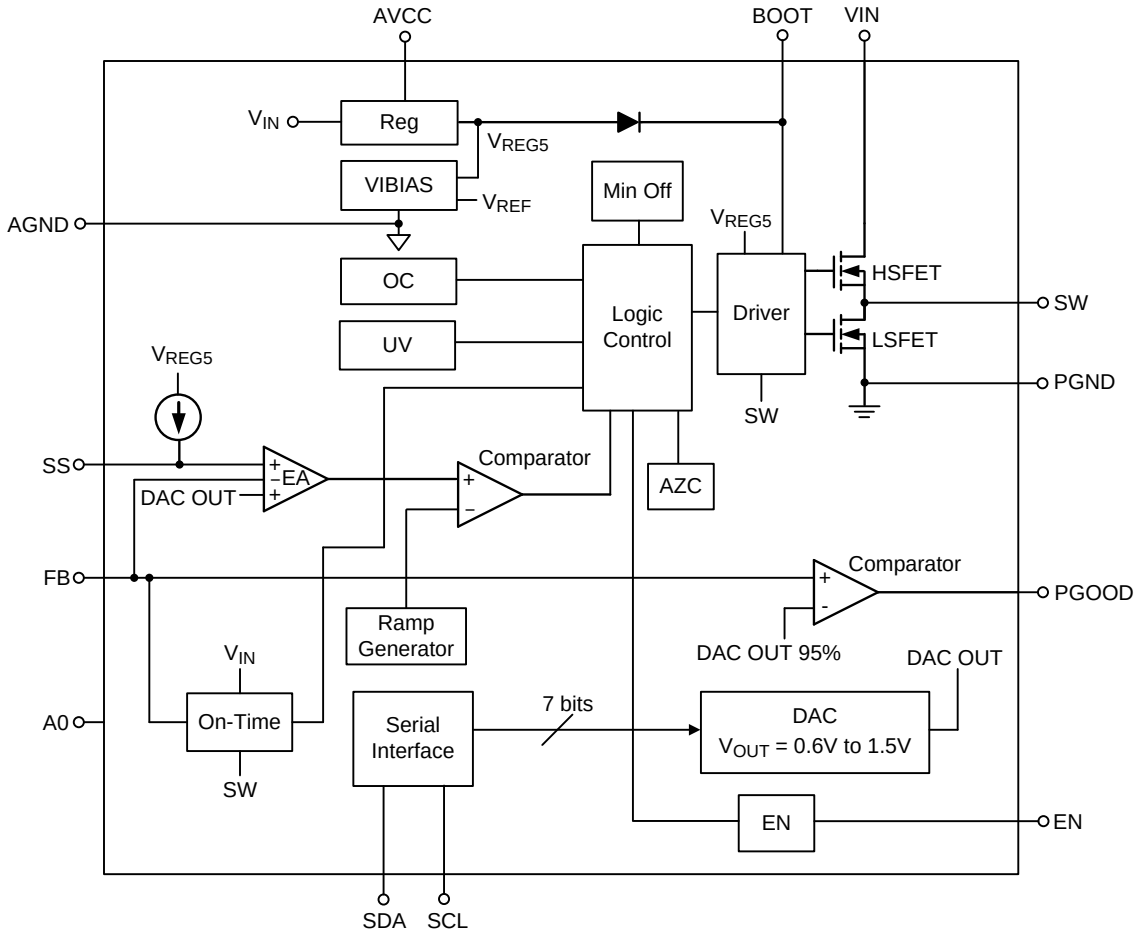


WET-WQFN-21L 4x4 (FC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable control input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode and reduces the supply current.
2, 11, 20	VIN	Input voltage. Support 2.85V to 6.5V input voltage. Connect this pin with a suitable capacitance for noise decoupling. The bypass capacitor should be placed as close to VIN pin as possible.
3	A0	I^2C setting. Device address select pin. High : xxxxx00, Low : xxxxx11, Floating : xxxxx10.
4	BOOT	Bootstrap supply for high-side gate driver. Connect a 0.1μF ceramic capacitor between BOOT and SW pins.
5	SW	Switch node. Connect this pin to an external L-C filter.
6, 7, 8, 9, 10, 21	PGND	System GND. The power GND of the controller circuit. Use wide PCB traces to make the connections.
12	AVCC	LDO output for internal analog power. Connect a 4.7μF capacitor as close to the VCC pin as possible.
13	NC	No internal connection.
14	AGND	Analog GND. AGND and PGND are connected with a short trace and at only one point to reduce circulating currents.
15	PGOOD	Power good indicator output. This pin has an open drain structure. Pull this pin high to a voltage source with a 100kΩ resistor.
16	SDA	I^2C interface, DATA.
17	SCL	I^2C interface, CLK.
18	SS	Soft-start time control pin. Connect a capacitor between the SS pin and AGND to set the soft-start time. The default internal start-up time is 0.833ms without external capacitor.
19	FB	Feedback input. The pin is used to set the output voltage of the converter via a resistor divider. Suggest placing the FB resistor divider as close to FB pin and AGND as possible.

Functional Block Diagram



Operation

The RTQ2159 is a high efficiency synchronous step-down converter utilizes the proprietary Advanced Constant On-Time (ACOT®) control architecture. The ultrafast ACOT® control enables the use of small capacitance to save the PCB size.

During normal operation, the internal high-side power switch (HSFET) is turned on for a fixed interval determined by a one-shot timer at the beginning of each clock cycle. When the HSFET turns off, the low-side power switch (LSFET) turns on. Due to the output capacitor ESR, the voltage ripple on the output has similar shape as the inductor current. Via the feedback resistor network, this voltage ripple compared with the internal reference. When the minimum off-time one-shot (100ns, typ.) has timed out and the inductor current is below the current limit threshold, the one-shot is triggered again if the feedback voltage falls below the feedback reference voltage (1V, typ.). To achieve stable operation with low-ESR ceramic output capacitors, an internal ramp signal is added to the feedback reference voltage to simulate the output voltage ripple. The ACOT® control architecture features ultrafast transient response. When a load is suddenly increased, the output voltage drops quickly, and almost immediately, a new on-time is triggered, and inductor current rises again.

The traditional COT controller implements the on-time to be inversely proportional to input voltage and directly proportional to the output voltage to achieve pseudo-fixed frequency over the input voltage range. But even with defined input and output voltages, a fixed ON time will mean that frequency will have to increase at higher load levels to compensate for the power losses in the MOSFETs and Inductor. The ACOT® control further added a frequency locked loop system, which slowly adjusts the ON time to compensate the power losses, without influencing the fast transient behavior of the COT topology.

Power and Bias Supply

The VIN pins on the RTQ2159 are used to supply voltage to the drain terminal of the internal HSFET. These pins also supply bias voltage for an internal regulator at AVCC. The voltage on AVCC pin is used for internal chip bias and gate drive for the LSFET. The gate drive for the HSFET is supplied by a floating supply (C_{BOOT}) between the BOOT and SW pins, which is charged by an internal synchronous diode from AVCC. In addition, an internal charge pump maintains the C_{BOOT} voltage is sufficient to turn-on the HSFET.

It is important to understand that if there is a discharge path on the AVCC rail that can pull a current higher than the internal LDO's current limit from the AVCC, then the AVCC drops below the UVLO falling threshold and thereby shutting down the output of RTQ2159.

Enable, Start-Up, Shutdown and UVLO

The RTQ2159 implements under-voltage lockout protection (UVLO) to prevent operation without fully turn-on the internal power MOSFETs. The UVLO monitors the internal AVCC regulator voltage. When the AVCC voltage is lower than UVLO threshold voltage, the device is shut off. UVLO is non-latching protection.

The EN pin is provided to control the device turn-on and turn-off. When EN pin voltage is above the turn-on threshold (V_{ENH}), the device starts switching and when the EN pin voltage falls below the turn-off threshold (V_{ENL}) it stops switching.

When appropriate voltages are present on the VIN, AVCC, and EN pins, the RTQ2159 will begin switching and initiate a soft-start ramp of the output voltage. An internal soft-start ramp will limit the ramp rate of the output voltage to prevent excessive input current during start-up. If a longer ramp time is desired, a capacitor can be placed from the SS pin to ground. The 10μA current that is sourced from the SS pin will create a smooth voltage ramp on the capacitor. If this external ramp rate is slower than the internal soft-start, the output voltage will be limited by the ramp rate on the SS pin instead. Once both of the external and internal soft-start ramps have exceeded 1V, the output voltage will be in regulation. The typical external soft start time can be calculated by the equation below.

$$C_{SS}\,(nF) = \frac{t_{SS}\,(ms) \times I_{SS}\,(\mu A)}{V_{REF}\,(V)}$$

where I_{SS} = 10μA, V_{REF} = 1V

When the V_{EN} is lower than V_{ENL}, the SS pin voltage is reset to GND.

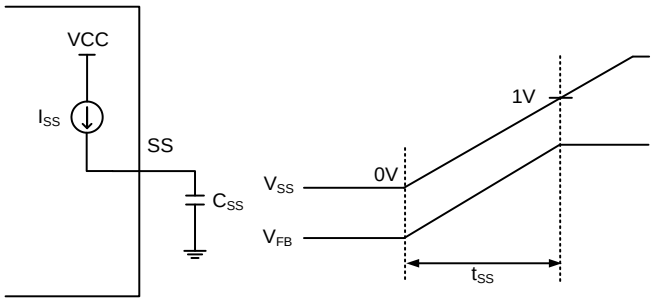


Figure 1. External Soft-Start Time Setting

Pre-Bias

If there is a residual voltage on output voltage before start-up, both of the internal HSFET and LSFET are prohibited switching until the soft start ramp is higher than feedback voltage. When the soft start ramp cross above the feedback voltage, switching will begin and the output voltage will smoothly rise from the pre-biased level to its regulated target.

Switching Frequency, Minimum On-Time and Minimum Off-Time

The RTQ2159 offers four different switching frequencies of 0.46MHz, 0.69MHz, 0.92MHz and 2.1MHz via the I^2C setting. Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and transition losses, but requires larger inductance values and/or capacitance to maintain low output ripple voltage. The RTQ2159 offers default 2.1MHz switching frequency for allowing the use of smaller inductor and capacitor values. An additional constraint on operating frequency is the minimum controllable on-time and off-time. The minimum on-time is the smallest duration of time in which the high-side power MOSFET (HSFET) can be in its “on” state. This time is typically 45ns. In continuous mode operation, the minimum duty cycle can be estimated by ignoring component losses as follows :

$$D_{MIN} = f_{SW} \times t_{ON\_MIN}$$

The minimum off-time, t_{OFF_MIN}, is the smallest amount of time that the RTQ2159 is capable of turning on the low-side power MOSFET (LSFET), tripping the current comparator and turning the power MOSFET back off. This time is 100ns (typ.). The minimum off-time limit imposes a maximum duty cycle of t_{ON} /(t_{ON} + t_{OFF_MIN}).

Current Limit and Output Under-Voltage Protection

The RTQ2159 provides current limits I_{LIM} to support an output continuous current of 8A. The device cycle-by-cycle compares the valley current of the inductor against the current limit threshold. Hence, the output current will be half the ripple current higher than the valley current.

The inductor current level is monitored by measuring the low-side MOSFET voltage between the SW pin and GND, which is proportional to the switch current, during the on-time of LSFET. To improve the current measurement accuracy, temperature compensation is added internally. If the measured drain to source voltage of the LSFET is above the voltage proportional to current limit, the LSFET stays on until the current level becomes lower than the OCL level which reduces the output current available. When the current is limited the output voltage tends to drop because the load demand is higher than what the converter can support.

When the output voltage falls below Output UVP Threshold (V_{UVP}), the UVP comparator detects it and shuts down the device to avoid the excessive heat. If the UVP condition remains for a period of time, a soft-start sequence for auto-recovery will be initiated. It is shown in Figure 2. When the overcurrent condition is removed, the output voltage returns to the regulated value.

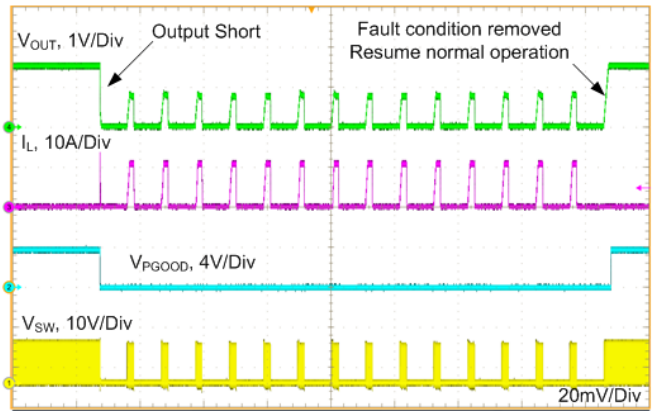


Figure 2. Current Limit and UVP

Similar to the forward overcurrent, the reverse current protection is realized by monitoring the current across the low-side MOSFET. When the LSFET current reaches −10A (typ.), the synchronous rectifier is turned off. This limits the ability of the regulator to actively pull-down on the output.

Power-Good Output

The PGOOD pin is an open-drain power-good indication which is connected to an external voltage source through a pull-up resistor. The power-good function is activated after soft-start is finished and is controlled by the feedback signal V_{FB}. During soft-start, PGOOD is actively held low and only allowed to transition high after soft-start is over. If V_{FB} rises above a power-good threshold V_{TH_PGLH} (typically 95% of the target value), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{FB} drops by a V_{FB} falling hysteresis ΔV_{TH_PGLH} (typically 10% of the target value) or exceeds V_{FB} rising threshold V_{TH_PGHL} typically 110% of the target value), the PGOOD pin will be pulled low. For V_{FB} above V_{FB} falling hysteresis, V_{PGOOD} will be pulled high again when V_{FB} drops back by a power-good hysteresis ΔV_{TH_PGHL} (typically 5% of the target value). Once being started-up, if any protection is triggered (UVP and OTP) or EN is from high to low, PGOOD will be pulled to GND. To prevent unwanted PGOOD glitches during transients or dynamic VOUT changes, the RTQ2159's PGOOD falling edge includes a blanking delay of approximately 10μs.

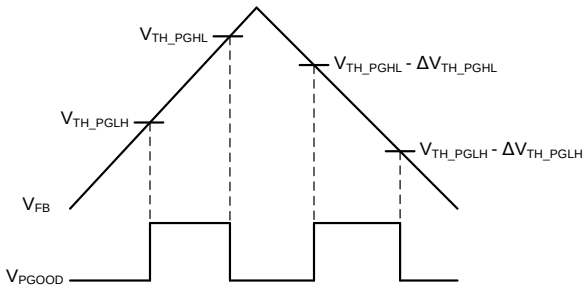


Figure 3. The Logic of PGOOD

Over-Temperature Protection (OTP)

The RTQ2159 monitors the internal die temperature. If this temperature exceeds the thermal shutdown threshold value (T_{SD}, typically 175°C), the RTQ2159 stops switching with SS reset to ground and an internal discharge switch turns on to quickly discharge the output voltage. During start up, if the device temperature is higher than 175°C, the device does not start switching. The device re-starts switching when the temperature drops more than 15°C (typ.).

Output Voltage Discharge

An internal 50Ω discharge switch that discharges the V_{OUT} through SW node during any fault events like UVP, OTP, AVCC voltage below UVLO and when the EN pin voltage (V_{EN}) is below the turn-on threshold.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 7V
- Phase Node Voltage, V_{SW} ---------- –0.3V to 7V
- V_{SW} (t ≤ 10ns) ---------- –3V to 8.5V
- Boot Voltage, V_{BOOT} ---------- –0.3V to 13V
- BOOT to SW (V_{BOOT} – V_{SW}) ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WET-WQFN-21L 4x4 (FC) ---------- 2.55W
- Package Thermal Resistance (Note 2)
  WET-WQFN-21L 4x4 (FC), θ_{JA} ---------- 39.2°C/W
  WET-WQFN-21L 4x4 (FC), θ_{JC} ---------- 3.7°C/W
- Junction Temperature Range ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2 kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 2.85V to 6.5V
- Junction Temperature Range ---------- –40°C to 150°C
- Ambient Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 5V, T_J = –40°C to 125°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Supply Input Voltage VIN	V_{IN}		2.85	--	6.5	V
Supply Current						
Quiescent Current	I_Q	No switching	--	--	500	μA
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V	--	--	30	μA
UVLO						
UVLO Rising Threshold	V_{UVLO_R}	V_{AVCC} rising	--	2.625	2.8	V
UVLO Falling Threshold	V_{UVLO_F}	V_{AVCC} falling	--	2.5	--	V
LDO Output						
LDO Output Voltage	V_{ACC}	V_{IN} = 6.5V to 5V, I_{AVCC} = 500μA	--	5	--	V
LDO Output Current Limit	V_{LIM_LDO}	V_{IN} = 6.5V, VDD < 4.5V	--	40	--	mA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Enable							
EN Input Voltage	Logic-High	V_{ENH}	Measure V_{EN} rising	1.2	--	V_{AVCC}	V
	Logic-Low	V_{ENL}	Measure V_{EN} falling	0	--	0.4	
Input Current		I_{EN}	V_{EN} = 2V	--	1	5	μA
Enable delay Time		T_{EN_DLY}		--	135	--	μs
Thermal Shutdown							
Thermal Shutdown Threshold		T_{SD}		--	175	--	°C
Thermal Recovery Threshold		T_{RC}		--	155	--	°C
Output Voltage and Soft-Start							
Reference Voltage		V_{OUT}	CCM	0.98	1	1.02	V
Soft-Start Time		t_{SS}	V_{OUT} = 1V, leave SS pin floating, 10% to 90%V_{OUT}	--	0.833	--	ms
Soft-Start Charge Current		I_{SS}		--	10	--	μA
$R_{DS(ON)}$							
Switch On-Resistance	High-Side	$R_{DS(ON)\_H}$		--	15	21	mΩ
	Low-Side	$R_{DS(ON)\_L}$		--	10	15	
Current Limit							
Current Limit		I_{LIM}	Valley current	8.1	9.8	11.9	A
Low-Side Switch Negative Current Limit		V_{LIM_NEG}	Valley current	--	–10	--	A
Switching Frequency and Minimum Off-Time							
Switching Frequency		f_{SW}	0x01[1:0] = 10b, V_{OUT} = 1V	1.85	2.1	2.35	MHz
Minimum On-Time		t_{ON_MIN}		--	45	--	ns
Minimum Off-Time		t_{OFF_MIN}		--	100	--	ns
Protections							
UVP Trip Threshold		V_{UVP}		--	70	--	%
UVP Time Delay		t_{UVPDLY}		--	5	--	μs
Power Good							
PGOOD Rising Threshold		V_{TH_PGLH}	V_{FB} rising (Good)	--	95	--	%V_{FB}
		ΔV_{TH_PGLH}	V_{FB} rising (Fault)	--	110	--	
PG Falling Threshold		V_{TH_PGHL}	V_{FB} falling (Fault)	--	90	--	
		ΔV_{TH_PGHL}	V_{FB} falling (Good)	--	105	--	
PGOOD Enable Delay Time				--	10	--	μs
PGOOD Output Low Voltage			I_{PGOOD} = 10mA	--	--	0.4	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PGOOD Output leakage Current		High-Z state, V_{PGOOD} = 5V	--	--	1	μA
Discharge Resistor						
Discharge Resistor	R_{DISCHG}	V_{EN} = 0V, V_{AVCC} = 5V	--	45	55	Ω
Regulation						
Line Regulation	ΔV_{LINE}	CCM	--	0.5	--	%
Load Regulation (Note 5)	ΔV_{LOAD}	CCM	--	0.5	--	%
I^2C						
SDA, SCL Input Voltage		High level	1.2	--	--	V
		Low level	--	--	0.4	
Fast Mode						
SCL Clock Rate	f_{SCL}		--	--	400	kHz
Hold Time for a Repeated START Condition	$t_{HD;STA}$	After this period, the first clock pulse is generated.	0.6	--	--	μs
Low Period of the SCL Clock	t_{LOW}		1.3	--	--	μs
High Period of the SCL Clock	t_{HIGH}		0.6	--	--	μs
Set up Time for a Repeated START Condition	$t_{SU;STA}$		0.6	--	--	μs
Data Hold Time	$t_{HD;DAT}$		0	--	0.9	μs
Data Set Up Time	$t_{SU;DAT}$		100	--	--	μs
Set Up Time for STOP Condition	$t_{SU;STO}$		0.6	--	--	μs
Bus Free Time between a STOP and a START Condition	t_{BUF}		1.3	--	--	μs
Rising Time of Both SDA/SCL Signals	t_R		20	--	300	μs
Falling Time of Both SDA/SCL Signals	t_F		20	--	300	μs
SDA/SCL Output Low Sink Current	I_{OL}	SDA voltage = 0.4V	2	--	--	μs

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

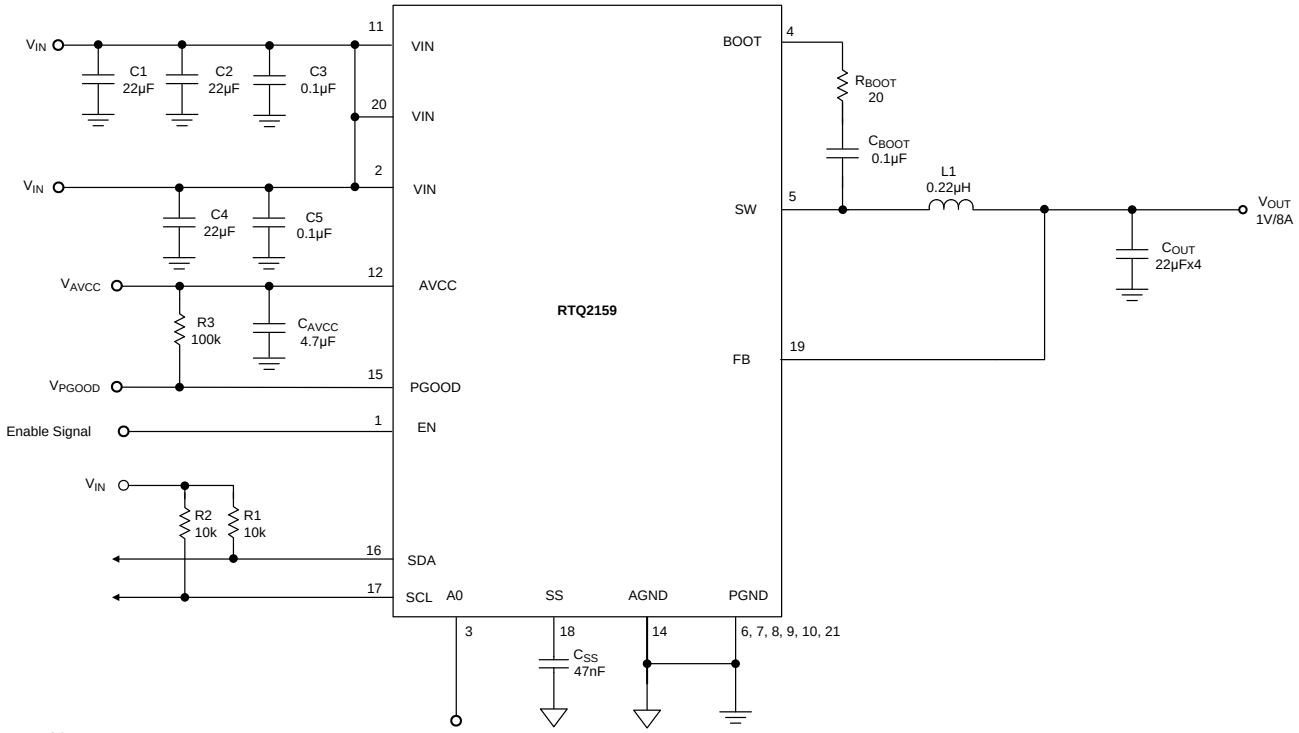
Note 2. Θ_{JA} is measured under natural convection at T_A = 25°C on a Four-layer Richtek Evaluation Board. θ_{JC} is measured at the top of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

Typical Application Circuit



Note :
All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any derating effect, like a DC bias.

Table 1. Suggested Component Values

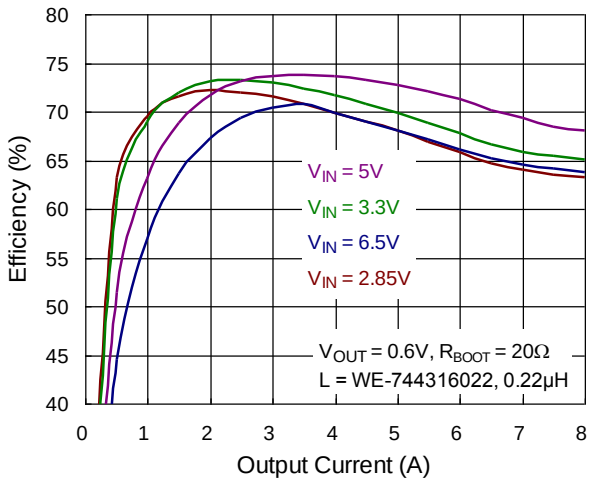
V_{OUT} (V)	L (µH)	C_{OUT} (µF)
1	0.22	88
1.2	0.22	88
1.5	0.22	88

Table 2. Suggested Component Selections

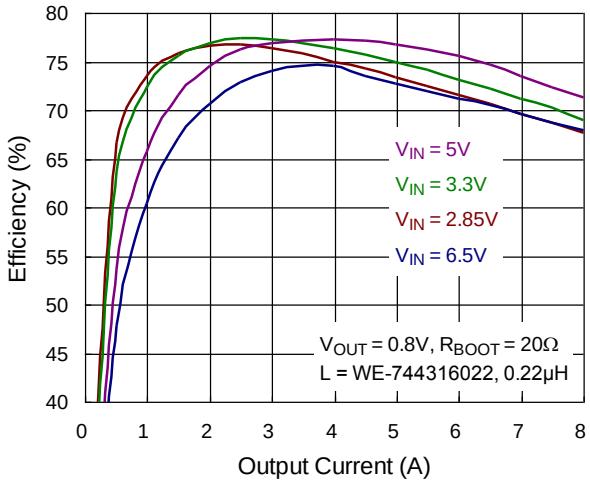
Component	Description	Case Size	Part No.	Component Supplier
L1	0.22µH	5040	744316022	WE-HCI
C3, C5, C_{BOOT}	0.1µF	0603	GRM188R71C104KA01D	Murata
C_{SS}	47nF	0603	0603B473K500CT	WALSIN
C_{AVCC}	4.7µF	0603	GRM188Z71C475KE21	Murata
C1, C2, C4, C_{OUT}	22µF	0603	GRM187R61A226ME15	Murata

Typical Operating Characteristics

Efficiency vs. Output Current



Efficiency vs. Output Current



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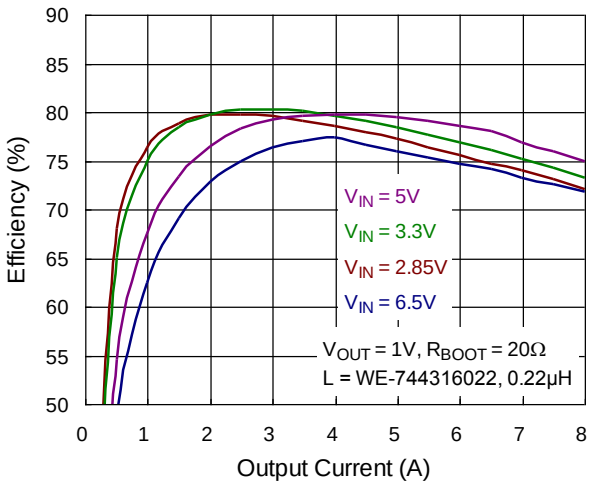
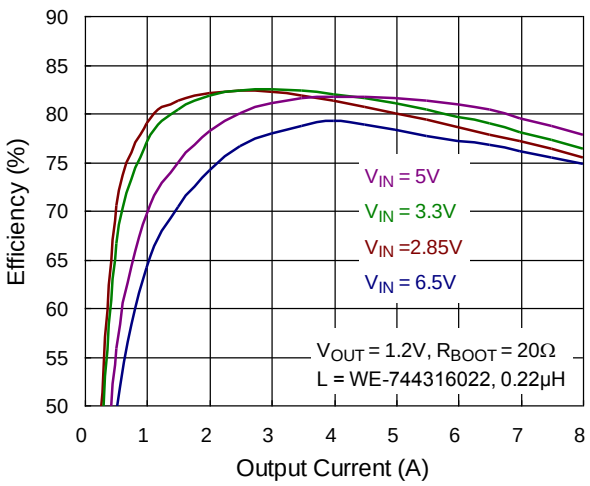
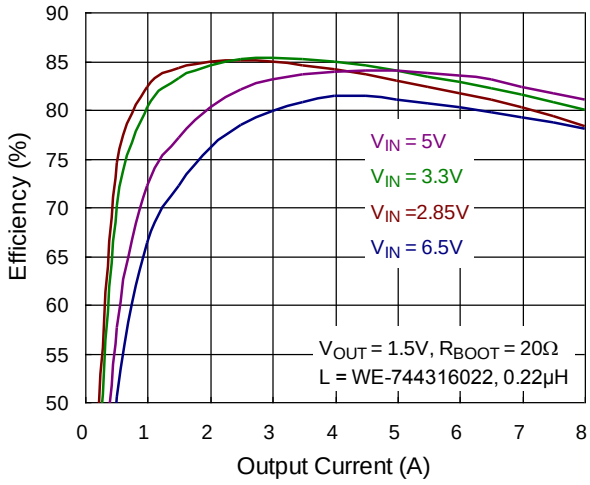


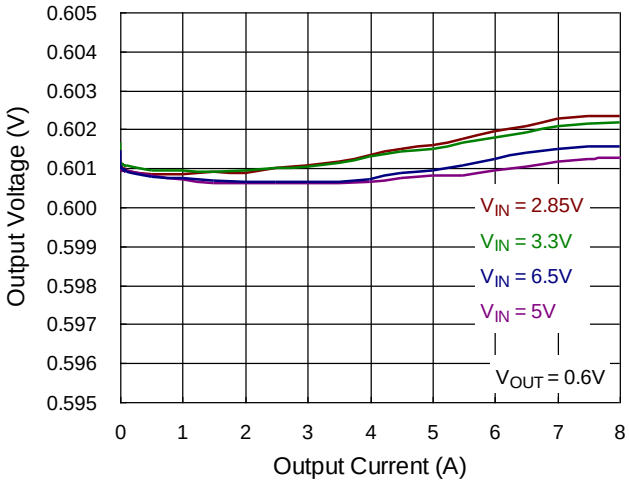
Efficiency vs. Output Current

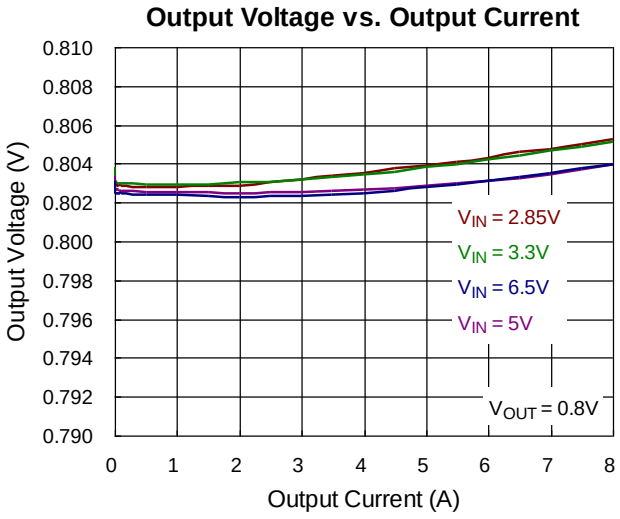


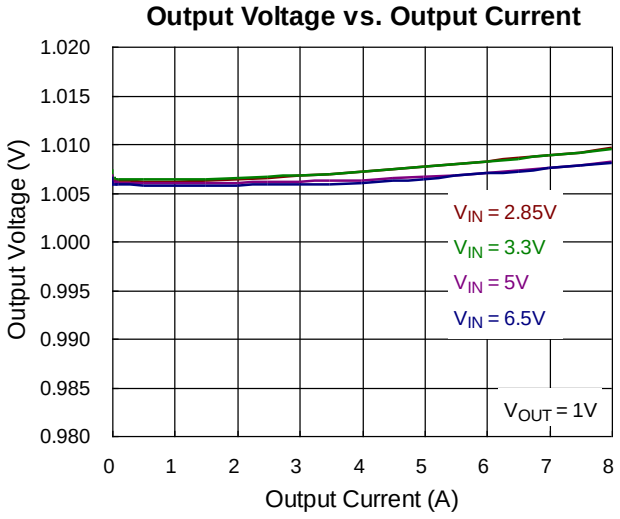
Efficiency vs. Output Current

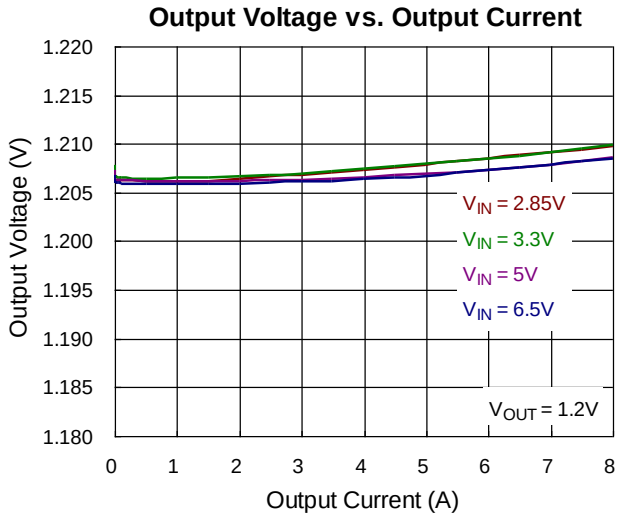


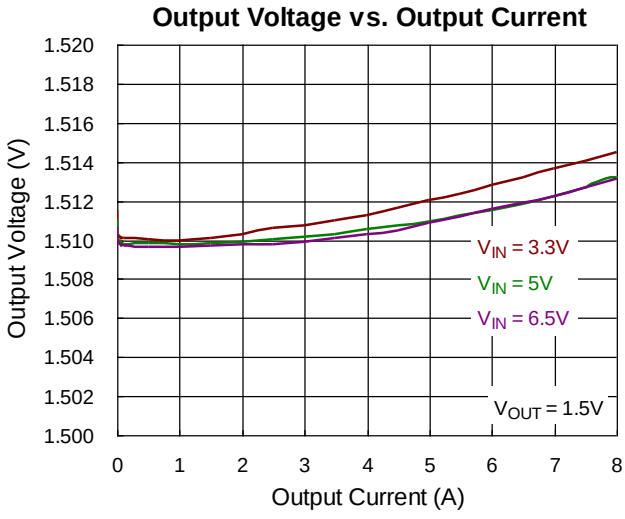
Output Voltage vs. Output Current

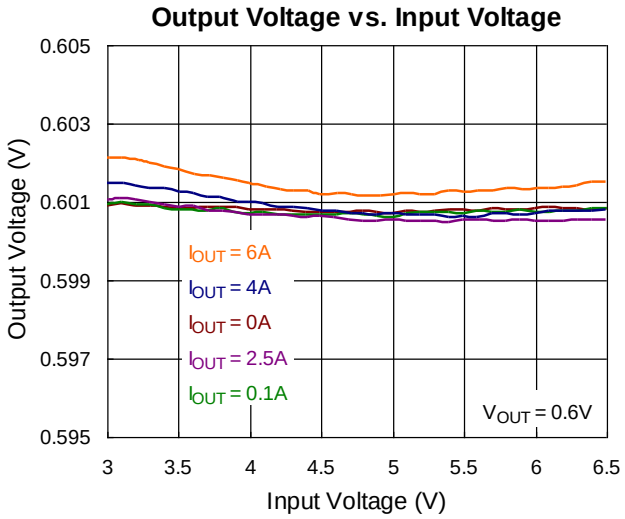


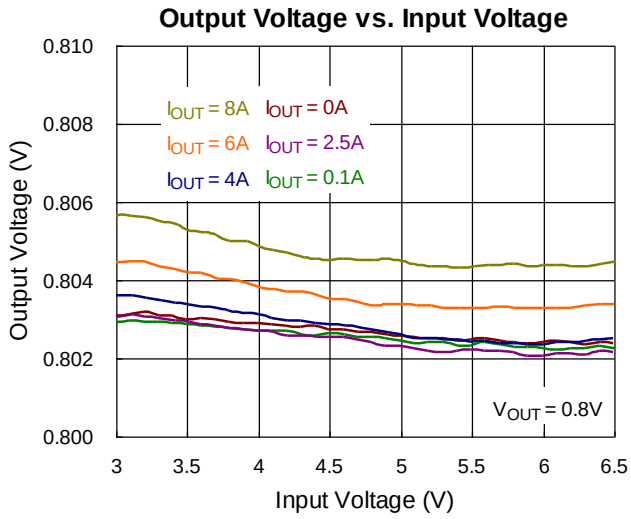




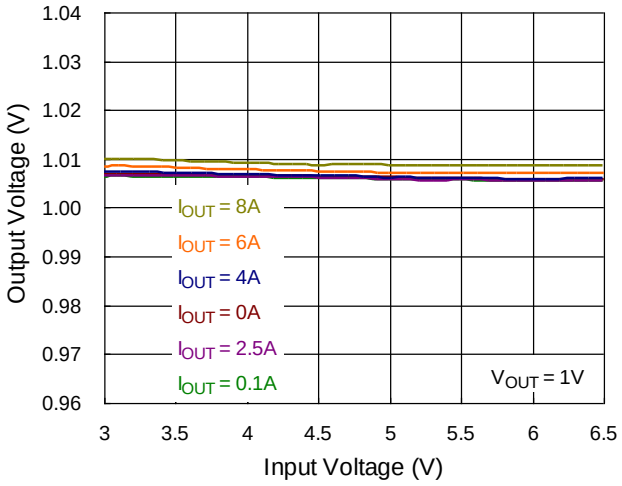




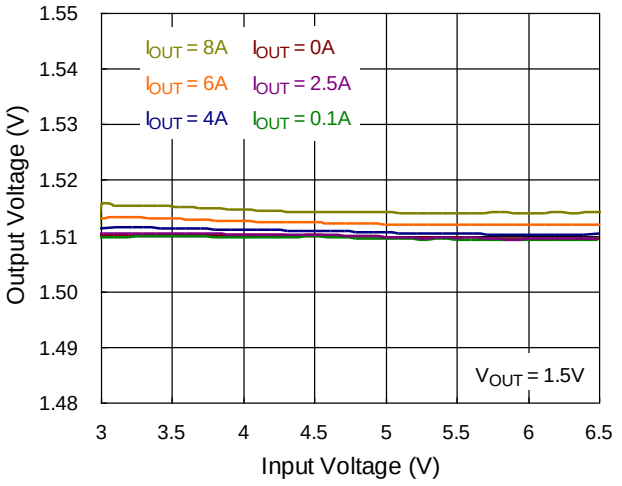




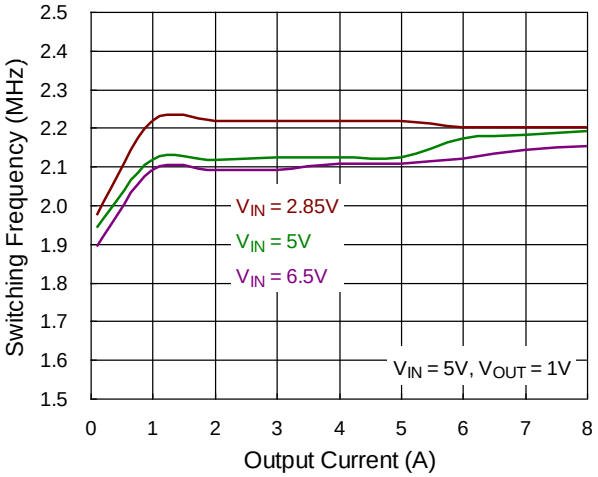
Output Voltage vs. Input Voltage



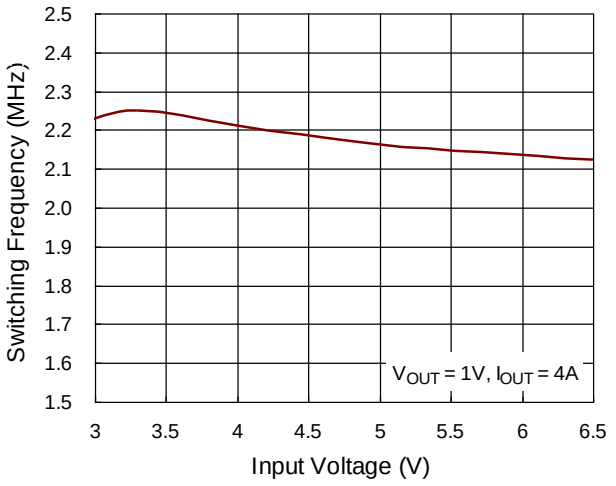
Output Voltage vs. Input Voltage



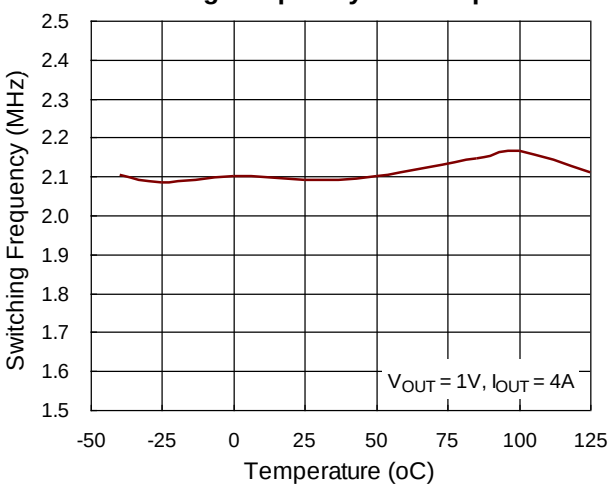
Switching Frequency vs. Output Current



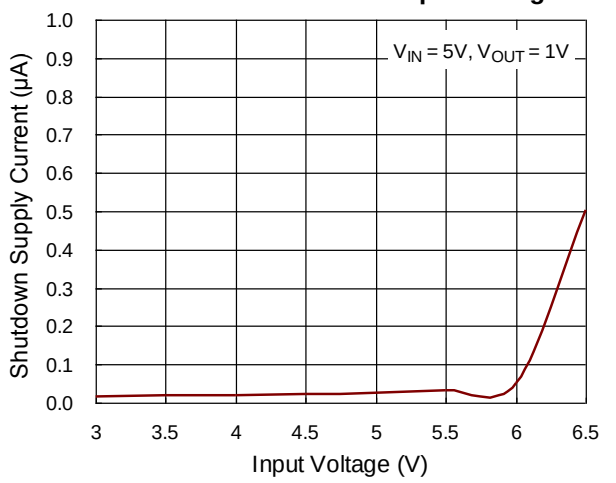
Switching Frequency vs. Input Voltage



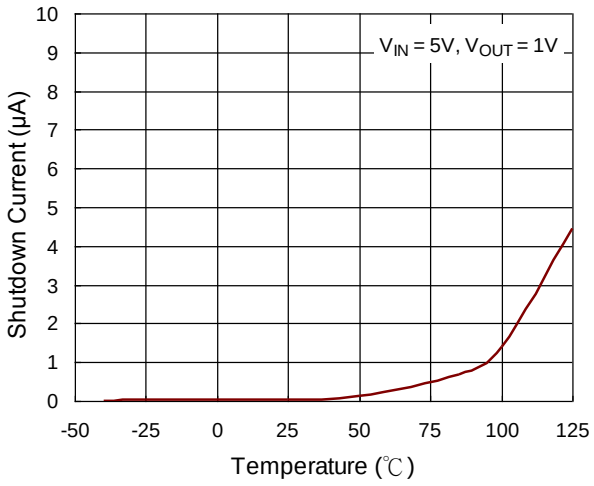
Switching Frequency vs. Temperature



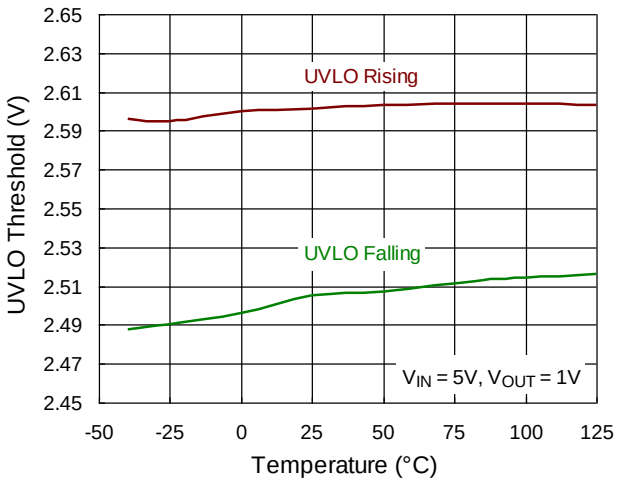
Shutdown Current vs. Input Voltage



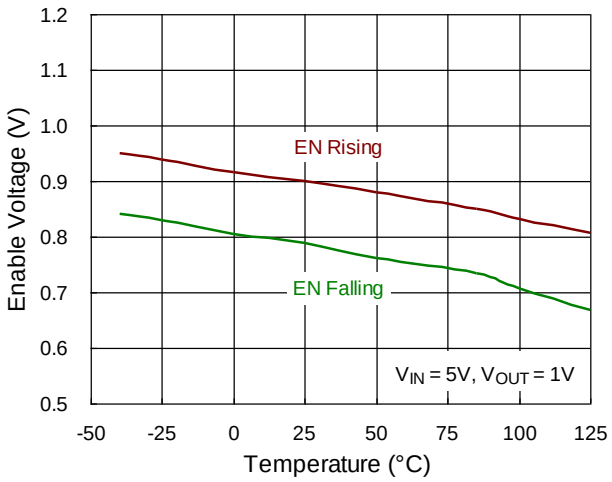
Shutdown Current vs. Temperature



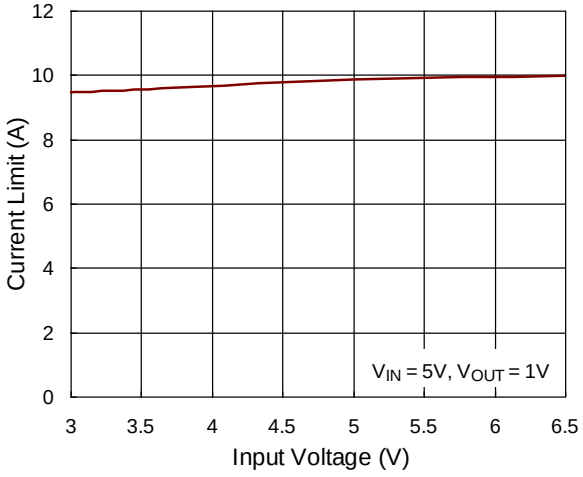
UVLO Threshold vs. Temperature



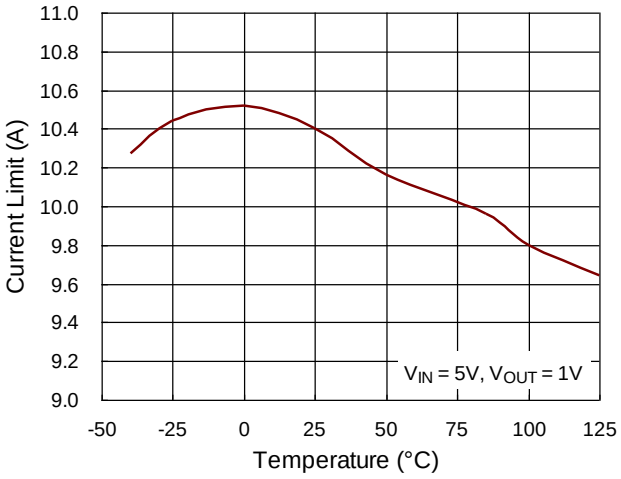
Enable Threshold vs. Temperature



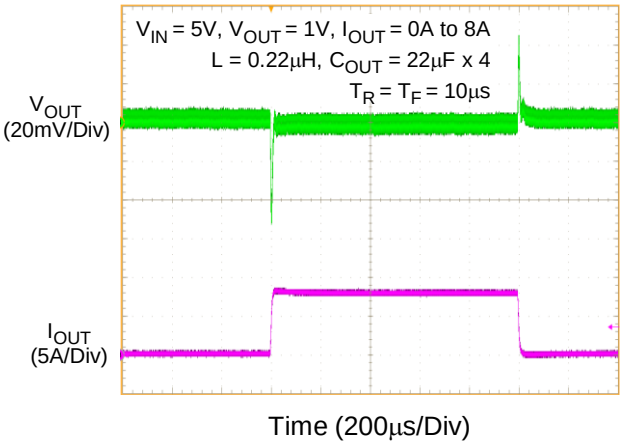
Current Limit Threshold vs. Input Voltage



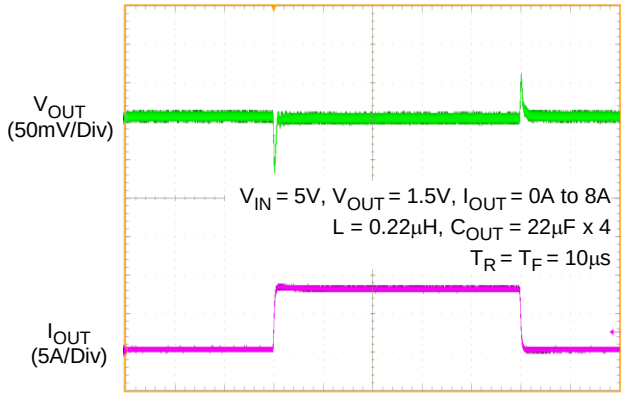
Current Limit Threshold vs. Temperature



Load Transient Response

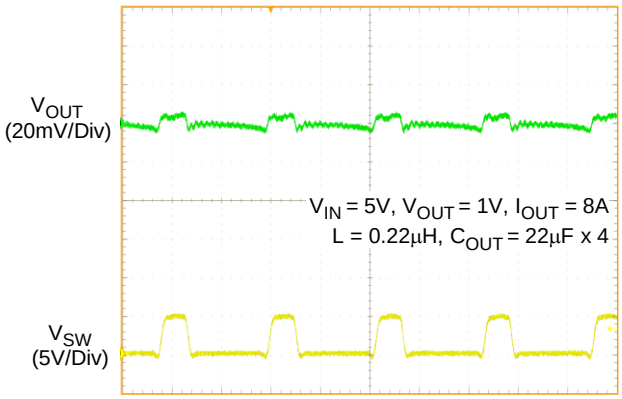


Load Transient Response



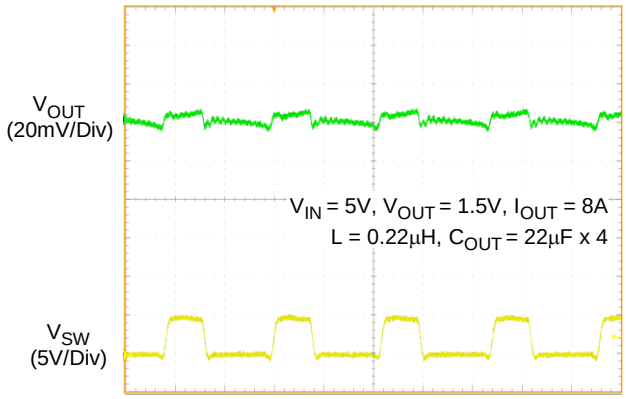
Time (200µs/Div)

Output Ripple Voltage



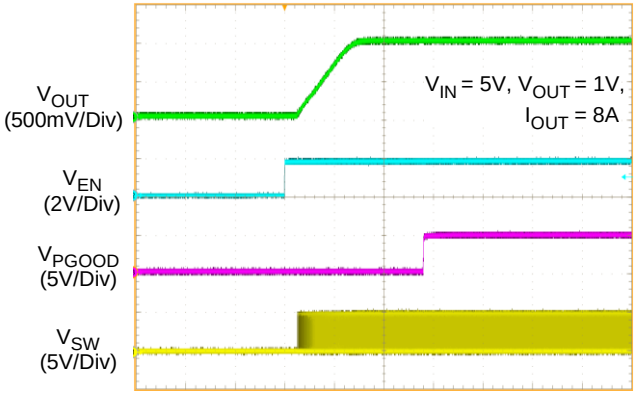
Time (200ns/Div)

Output Ripple Voltage



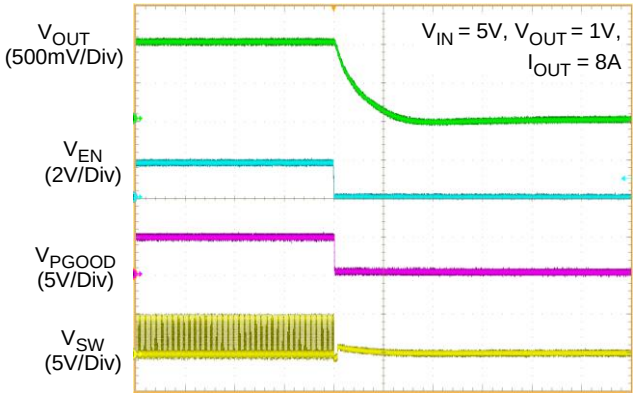
Time (200ns/Div)

Power On from EN



Time (500µs/Div)

Power Off from EN



Time (20µs/Div)

Functional Register Table

Table 3. RTQ2159 Register Summary

Name	Type	Register Reset	Address Offset
MANUFACTURER_ID	R	0x82h	0x00
FREQ_REG	RW	0x0Ah	0x01
SEL_REG	RW	0x00h	0x02
DCDCCTRL_REG	RW	0x0Ah	0x03
STATUS_REG	R	0x00h	0x04
DCDC_SET	RW	0xA4h	0x05

Table 4. MANUFACTURER_ID

Address : 0x00
Description : Manufacturer ID number register

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MANUFACTURER_ID							
Reset Value	0x82h							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
7 : 0	MANUFACTURER_ID	Return the manufacturer ID number : 0x82h

Table 5. FREQ_REG

Address : 0x01
Description : Configure register
Set VID change slew rate and PWM frequency.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved				TSTEP		FREQ	
Reset Value	0	0	0	0	1	0	1	0
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Bits	Name	Description
7 : 4	Reserved	Reserved bit
3 : 2	TSTEP	TSTEP[3:2] = 00b : 20mV/μs TSTEP[3:2] = 01b : 15mV/μs TSTEP[3:2] = 10b : 10mV/μs (default) TSTEP[3:2] = 11b : 5mV/μs
1 : 0	FREQ	FREQ[1:0] = 00b, 0.46MHz FREQ[1:0] = 01b, 0.69MHz FREQ[1:0] = 10b, 2.1MHz (default) FREQ[1:0] = 11b, 0.92MHz

Table 6. SEL_REG

Address : 0x02 **Description :** VID setting register								
Bits	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Name	Reserved	SEL						
Reset Value	0	0	1	0	1	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	**Name**	**Description**
7	Reserved	Reserved bit
6 : 0	SEL	Supply voltage : SEL[6:0] = 0000000b : 0.6V SEL[6:0] = 0000001b : 0.61V SEL[6:0] = 0000010b : 0.62V SEL[6:0] = 0000011b : 0.63V SEL[6:0] = 0000100b : 0.64V SEL[6:0] = 0000101b : 0.65V SEL[6:0] = 0000110b : 0.66V SEL[6:0] = 0000111b : 0.67V SEL[6:0] = 0001000b : 0.68V SEL[6:0] = 0001001b : 0.69V SEL[6:0] = 0001010b : 0.7V SEL[6:0] = 0001011b : 0.71V SEL[6:0] = 0001100b : 0.72V SEL[6:0] = 0001101b : 0.73V SEL[6:0] = 0001110b : 0.74V SEL[6:0] = 0001111b : 0.75V SEL[6:0] = 0010000b : 0.76V SEL[6:0] = 0010001b : 0.77V SEL[6:0] = 0010010b : 0.78V SEL[6:0] = 0010011b : 0.79V SEL[6:0] = 0010100b : 0.8V SEL[6:0] = 0010101b : 0.81V SEL[6:0] = 0010110b : 0.82V SEL[6:0] = 0010111b : 0.83V SEL[6:0] = 0011000b : 0.84V SEL[6:0] = 0011001b : 0.85V SEL[6:0] = 0011010b : 0.86V SEL[6:0] = 0011011b : 0.87V SEL[6:0] = 0011100b : 0.88V SEL[6:0] = 0011101b : 0.89V SEL[6:0] = 0011110b : 0.9V SEL[6:0] = 0011111b : 0.91V SEL[6:0] = 0100000b : 0.92V SEL[6:0] = 0100001b : 0.93V SEL[6:0] = 0100010b : 0.94V SEL[6:0] = 0100011b : 0.95V SEL[6:0] = 0100100b : 0.96V SEL[6:0] = 0100101b : 0.97V SEL[6:0] = 0100110b : 0.98V SEL[6:0] = 0100111b : 0.99V

6 : 0	SEL	SEL[6:0] = 0101000b : 1V SEL[6:0] = 0101001b : 1.01V SEL[6:0] = 0101010b : 1.02V SEL[6:0] = 0101011b : 1.03V SEL[6:0] = 0101100b : 1.04V SEL[6:0] = 0101101b : 1.05V SEL[6:0] = 0101110b : 1.06V SEL[6:0] = 0101111b : 1.07V SEL[6:0] = 0110000b : 1.08V SEL[6:0] = 0110001b : 1.09V SEL[6:0] = 0110010b : 1.1V SEL[6:0] = 0110011b : 1.11V SEL[6:0] = 0110100b : 1.12V SEL[6:0] = 0110101b : 1.13V SEL[6:0] = 0110110b : 1.14V SEL[6:0] = 0110111b : 1.15V SEL[6:0] = 0111000b : 1.16V SEL[6:0] = 0111001b : 1.17V SEL[6:0] = 0111010b : 1.18V SEL[6:0] = 0111011b : 1.19V SEL[6:0] = 0111100b : 1.2V SEL[6:0] = 0111101b : 1.21V SEL[6:0] = 0111110b : 1.22V SEL[6:0] = 0111111b : 1.23V SEL[6:0] = 1000000b : 1.24V SEL[6:0] = 1000001b : 1.25V SEL[6:0] = 1000010b : 1.26V SEL[6:0] = 1000011b : 1.27V SEL[6:0] = 1000100b : 1.28V SEL[6:0] = 1000101b : 1.29V SEL[6:0] = 1000110b : 1.3V SEL[6:0] = 1000111b : 1.31V SEL[6:0] = 1001000b : 1.32V SEL[6:0] = 1001001b : 1.33V SEL[6:0] = 1001010b : 1.34V SEL[6:0] = 1001011b : 1.35V SEL[6:0] = 1001100b : 1.36V SEL[6:0] = 1001101b : 1.37V SEL[6:0] = 1001110b : 1.38V SEL[6:0] = 1001111b : 1.39V SEL[6:0] = 1010000b : 1.4V SEL[6:0] = 1010001b : 1.41V SEL[6:0] = 1010010b : 1.42V SEL[6:0] = 1010011b : 1.43V SEL[6:0] = 1010100b : 1.44V SEL[6:0] = 1010101b : 1.45V SEL[6:0] = 1010110b : 1.46V SEL[6:0] = 1010111b : 1.47V SEL[6:0] = 1011000b : 1.48V SEL[6:0] = 1011001b : 1.49V SEL[6:0] = 1011010b to 1111111b : 1.5V

Table 7. DCDCCTRL_REG

Address : 0x03 **Description :** discharge resistor enable, and internal enable registers								
Bits	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Name	Reserved				Discharge	Reserved	Enable	Reserved
Reset Value	0	0	0	0	1	0	1	0
Read/Write	R	R	R	R	R/W	R/W	R/W	R

Bits	Name	Description
7 : 4	Reserved	Reserved bit
3	Discharge	Discharge[3] = 0b : disable discharge resistor (Only OT/UVLO = 1, disable discharge; EN = 0, enable discharge) Discharge[3] = 1b : enable discharge resistor (default)
2	Reserved	Reserved bit
1	Enable	Enable[1] = 0b : disable Enable[1] = 1b : enable (default)
0	Reserved	Reserved bit

Table 8. STATUS_REG

Address : 0x04 **Description :** indication of status								
Bits	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Name	Reserved						OT	UV
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
7 : 3	Reserved	Reserved bit
2	Reserved	Reserved bit
1	OT	OT[1] = 0b : no OT OT[1] = 1b : OT
0	UV	UV[0] = 0b : no UV UV[0] = 1b : UV

Table 9. DCDC_SET

Address : 0x05 **Description :** current limit, thermal shutdown threshold, PG enable delay time, VID								
Bits	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Name	Reserved		OTSET		PGDSET		Reserved	
Reset Value	0	0	1	0	0	1	0	0
Read/Write	R	R	R	R/W	R/W	R/W	R	R

Bits	**Name**	**Description**
7 : 6	Reserved	Reserved bit
5 : 4	OTSET	OTSET[5:4] = 00b : no OT OTSET[5:4] = 01b : 170°C OTSET[5:4] = 10b : 175°C (default) OTSET[5:4] = 11b : 180°C
3 : 2	PGDSET	PGDSET[3:2] = 00b : PG enable delay time = 0μs PGDSET[3:2] = 01b : PG enable delay time = 10μs (default) PGDSET[3:2] = 10b : PG enable delay time = 20μs PGDSET[3:2] = 11b : PG enable delay time = 40μs
1 : 0	Reserved	Reserved bit

Application Information

A general RTQ2159 application circuit is shown in typical application circuit section. External component selection is largely driven by the load requirement and begins with the operating frequency. Next, the inductor L is chosen and then the input capacitor C_{IN}, the output capacitor C_{OUT}, the internal regulator capacitor C_{AVCC}, and the bootstrap capacitor C_{BOOT}, can be selected. Next, feedback resistors are selected to set the desired output voltage. Finally, the remaining optional external components can be selected for functions such as the EN and UVLO threshold, external soft-start time, and PGOOD.

Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current ΔI_L to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current limit threshold and increases the AC losses in the inductor. To enhance the efficiency, choose a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines not only the ripple current but also the load-current value at which DCM/CCM switchover occurs.

The inductor selected should have a saturation current rating greater than the peak current limit of the device. The core must be large enough not to saturate at the peak inductor current (I_{L_PEAK}) :

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2}\Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The peak-to-peak voltage ripple on input capacitor can be estimated as equation below :

$$\Delta V_{CIN} = D \times I_{OUT} \times \left(ESR + \frac{1-D}{C_{IN} \times f_{SW}} \right)$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple which is caused by ESR can be ignored, and the minimum input capacitance can be estimated as equation below :

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

where ΔV_{CIN_MAX} = 50mV.

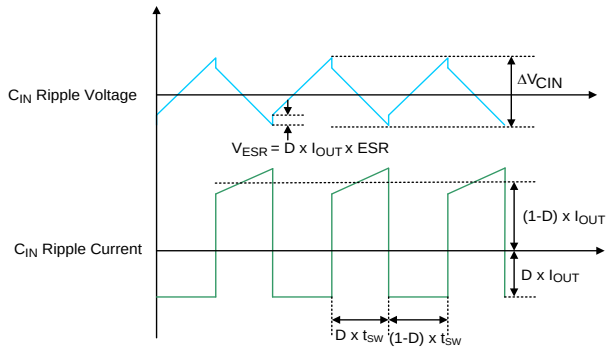


Figure 4. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current of :

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is commonly to use the worse $I_{RMS} \cong I_{OUT}/2$ at $V_{IN} = 2V_{OUT}$ for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for witching regulator applications due to its small size, robustness and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RTQ2159 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pins, with a low inductance connection to the PGND of the IC. In addition to a larger bulk capacitor, two small ceramic capacitors of 0.1μF should be placed close to the part; one at the VIN11/PGND pins and the second at VIN2/PGND pins. These capacitors should be 0402 or 0603 in size.

Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple, the transient loads and to ensure that control loop is stable. Loop stability can be checked by viewing the load transient response. The peak-to-peak output ripple, ΔV_{OUT}, is characterized by two components, which are ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C}, can be expressed as below :

$$\Delta V_{OUT} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

where the ΔI_L is the peak-to-peak inductor ripple current and R_{ESR} is the equivalent series resistance of C_{OUT}. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding to the transient loads, the V_{SAG} and V_{SOAR} requirement should be taken into consideration for choosing the output capacitance value. The amount of output sag is a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The worst-case output sag voltage can be determined by :

$$\Delta V_{OUT\_SAG} = \frac{L \times (I_{L\_PEAK})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

The amount of overshoot due to stored inductor energy when the load is removed can be calculated as :

$$\Delta V_{OUT\_SOAR} = \frac{L \times (I_{L\_PEAK})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Internal AVCC Regulator

Good bypassing at AVCC pin is necessary to supply the high transient currents required by the power MOSFET gate drivers. Place a low ESR MLCC capacitor with capacitance ≥ 4.7μF (or effective capacitance ≥ 1.5μF) as close as possible to AVCC pin, the rated voltage of C_{AVCC} should be higher than 10V with 0805 or 0603 in size.

Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Do not connect AVCC to provide power to other devices or loads.

HSFET Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between BOOT pin and SW pin is used to create a voltage rail above the applied input voltage, VIN. Specifically, the bootstrap capacitor is charged through an internal MOSFET switch to a voltage equal to approximately V_{AVCC} each time the LSFET is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle.

The selection of C_{BOOT} considers the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BOOT} such that the available gate-drive voltage is not significantly degraded when determining C_{BOOT}. A typical range of ΔV_{BOOT} is 100mV to 300mV. The bootstrap capacitor should be a low-ESR ceramic capacitor. For most applications a 0.1μF ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

EMI issue is worse when the switch is turned on rapidly due to high di/dt noises induced. In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small (< 47Ω) resistor between the BOOT pin and the external bootstrap capacitor. This will slow down the rates of the high-side switch turn-on and the rise of V_{SW}. The recommended application circuit is shown in Figure 5, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} being placed between the BOOT pin and the capacitor/diode connection.

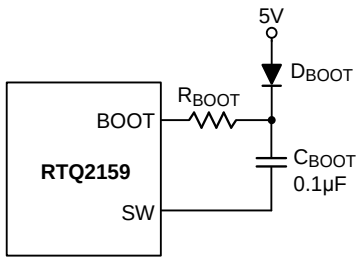


Figure 5. External Bootstrap Diode and Resistor at the BOOT Pin

Enable Control

The EN pin controls the turn-on and turn-off of the device. When EN pin voltage is above the turn-on threshold (V_{ENH}), the device starts switching, and it stops switching when the EN pin voltage falls below the turn-off threshold (V_{ENL}). The EN pin of RTQ2159 has internally pull-up with current source. However, the RTQ2159 internally week pull-down the EN pin. Figure 6 shows example if an enable time delay is required :

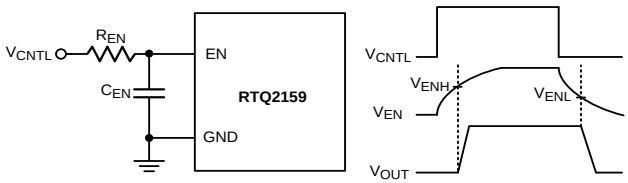


Figure 6. Enable Timing Control

Figure 7 shows examples of configurations for driving the EN pin from logic.

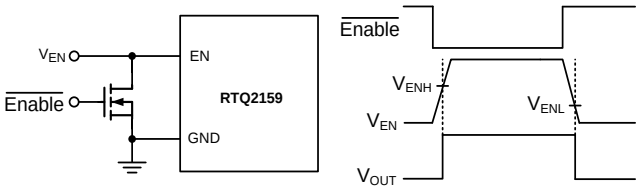
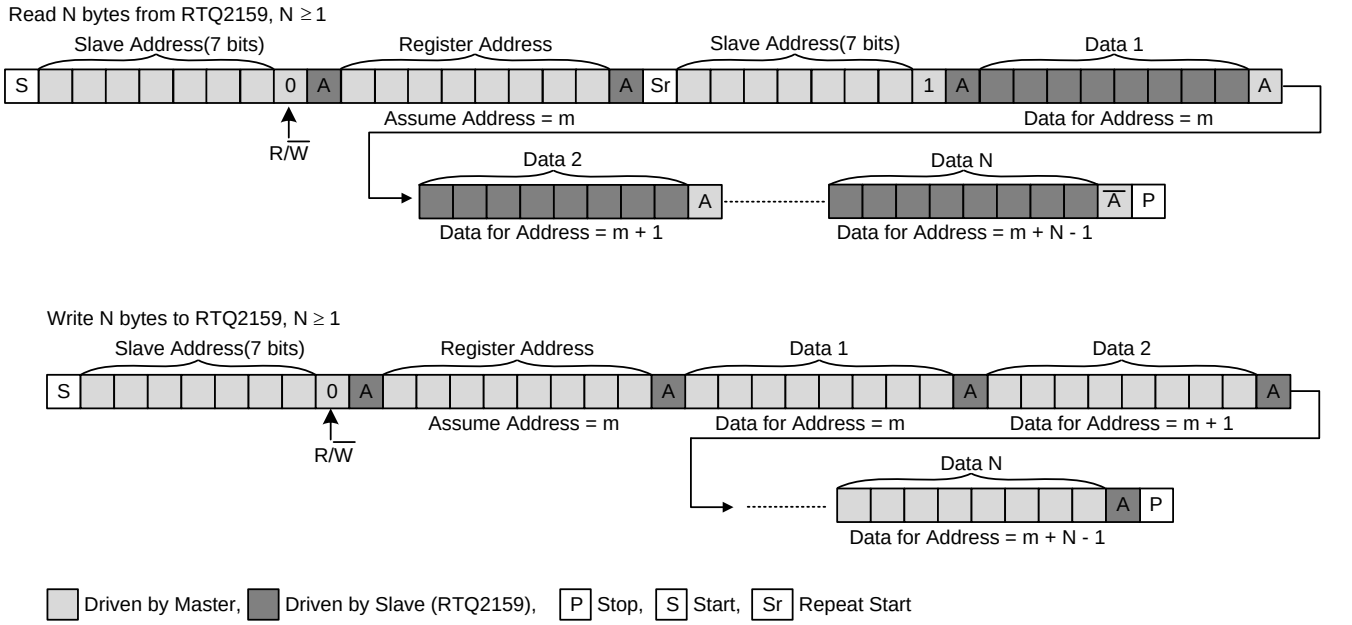


Figure 7. Logic Control for the EN Pin

I²C Interface

A general-purpose serial interface to control and monitor the configuration registers is provided in the RTQ2159 and the I²C slave address of the RTQ2159 are 0x60 (A0 pin = High Level), 0x62 (A0 pin floating), or 0x63 (A0 pin = Low Level). This I²C interface supports standard slave mode (100kbps) and fast mode (400kbps). A multiple bytes reading or writing over the I²C interface can also be done through the RTQ2159 (see Figure 8).



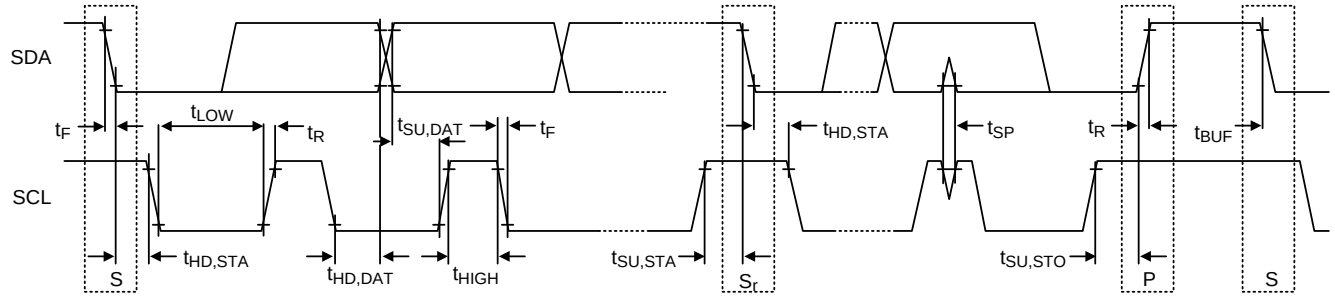


Figure 8. I²C Read/Write Stream and Timing Diagram

Thermal Consideration

In many applications, the RTQ2159 does not generate much heat due to its high efficiency and low thermal resistance of its thermally enhanced WET-WQFN-21L 4x4 (FC) package. However, in applications which the RTQ2159 is running at a high ambient temperature, high input voltage and high switching frequency, the generated heat may exceed the maximum junction temperature of the part.

The junction temperature should never exceed the absolute maximum junction temperature listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 175°C, RTQ2159 stop switching the power MOSFETs until the temperature drops about 15°C cooler.

The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA(EFFECTIVE)}$

- $T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 125°C.
- T_A is the ambient operating temperature.
- $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The device thermal resistance depends strongly on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

Table 10 shows the simulated thermal resistance of RTQ2159 which is mounted on PCB with difference tack-up and copper thickness. The layout of thermal model refers to the RTQ2159 evaluation board.

Table 10. Simulated Thermal Resistance with Difference Tack-Up and Copper Thickness

Simulated θ_{JA}	$\theta_{JA(EFFECTIVE)}$ (°C/W)
4 Layer with 2oz copper	39.2
4 Layer with 1oz copper	57
2 Layer with 1oz copper	75

As an example, consider the case when the RTQ2159 is used in applications where V_{IN} = 5V, I_{OUT} = 8A, V_{OUT} = 1V.

The efficiency at 1V, 8A is 75% by using WE-744316022 (0.22μH, 1.25mΩ DCR) as the inductor and measured at room temperature. The core loss 0.094W can be obtained from its website. In this case, the power dissipation of RTQ2159 is

$$P_{D,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I_O^2 \times DCR + P_{CORE}\right) = 2.49W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 39.2°C/W by using RTQ2159 evaluation board with 4 layers PCB and 2oz copper thickness, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately :

$$T_J = 2.49 \times 39.2 \frac{°C}{W} + 25°C = 122°C$$

Layout Guidelines

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RTQ2159 :

- Four-layer or six-layer PCB with maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- VIN pins should place input capacitors on each side of IC. Place these input capacitors as close to VIN pins as possible.
- Place the AVCC decoupling capacitor, C_{AVCC}, as close to AVCC pin as possible.

- Place bootstrap capacitor, C_{BOOT}, as close to IC as possible. Routing the trace with width of 20mil or wider.
- Place multiple vias under the device near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the RTQ2159 to additional ground planes within the circuit board and on the bottom side.
- The high frequency switching nodes, SW and BOOT, should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Connect the feedback sense network behind via of output capacitor.

Figure 9 is the layout example which uses (70mm x100mm), four-layer PCB with 2oz copper.

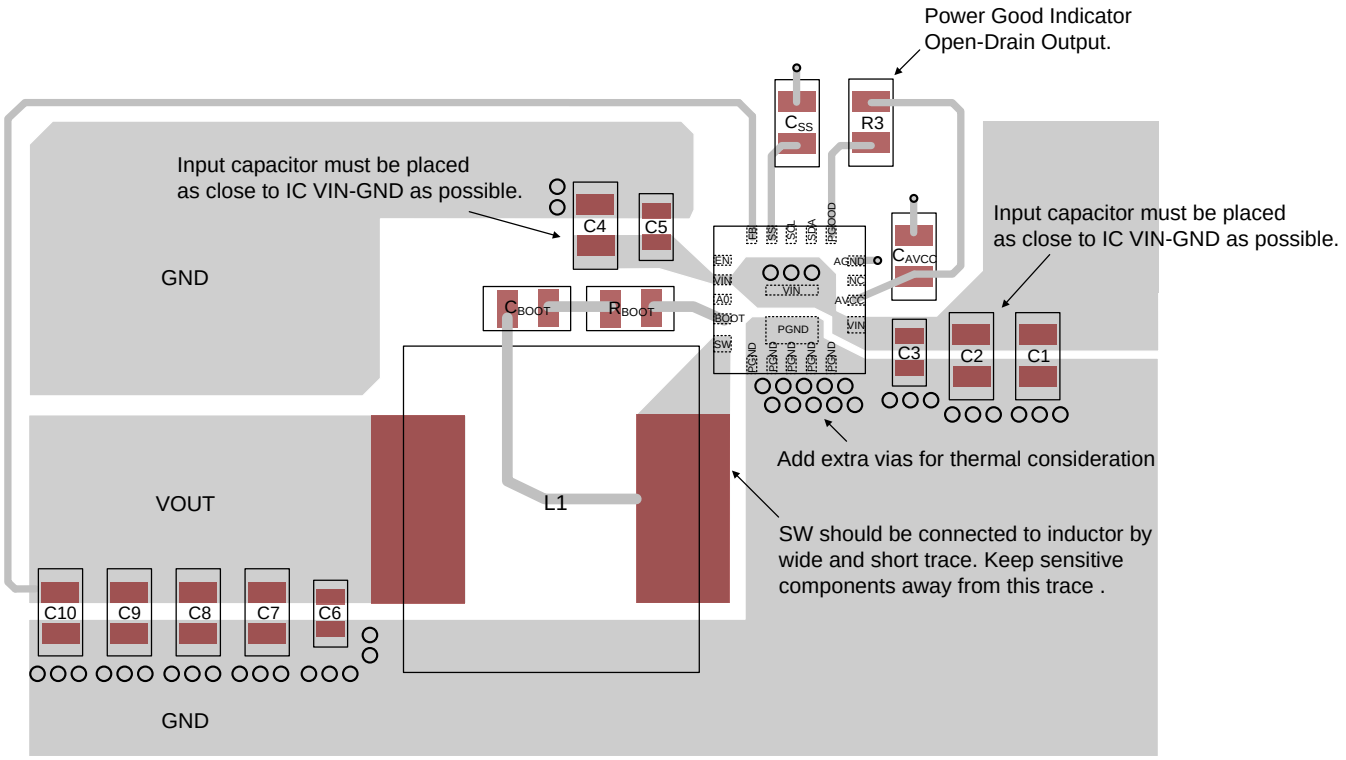
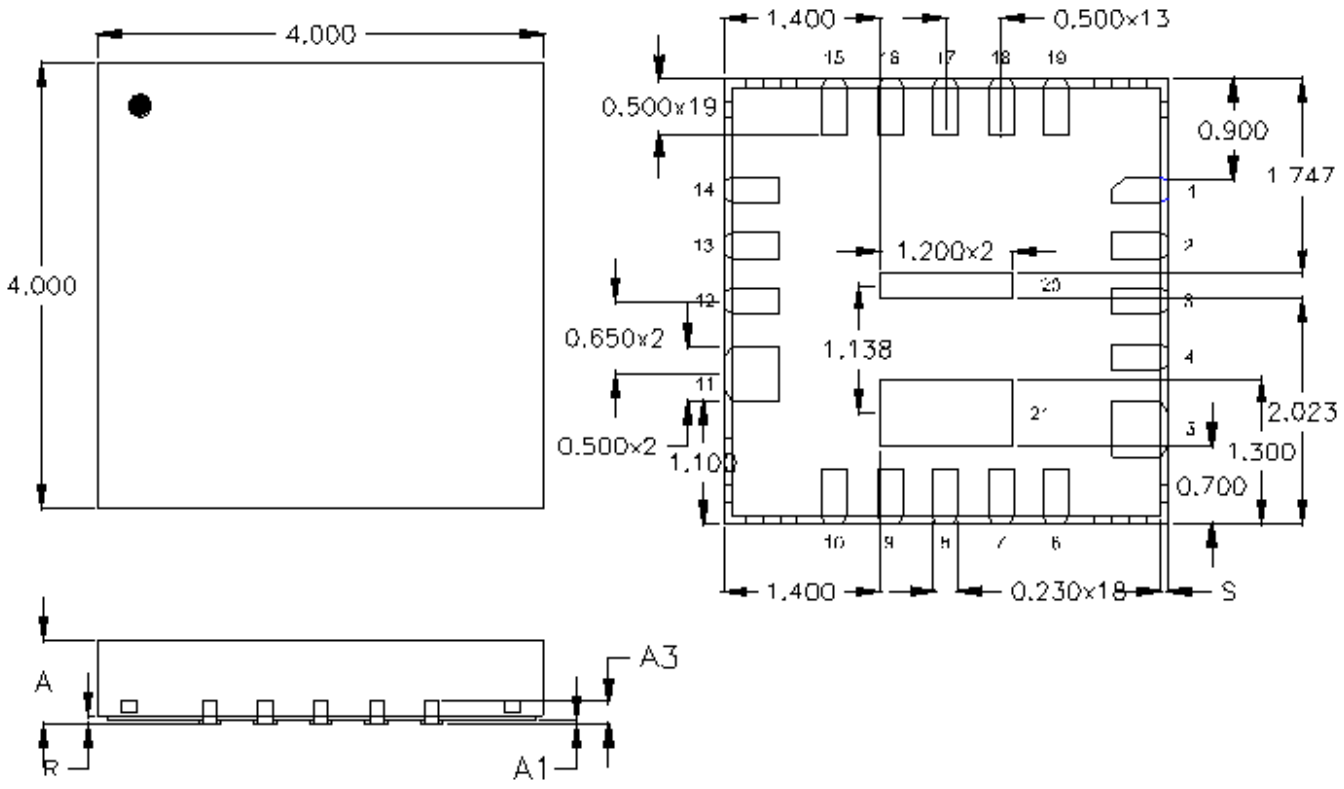


Figure 9. PCB Layout Guide

Outline Dimension

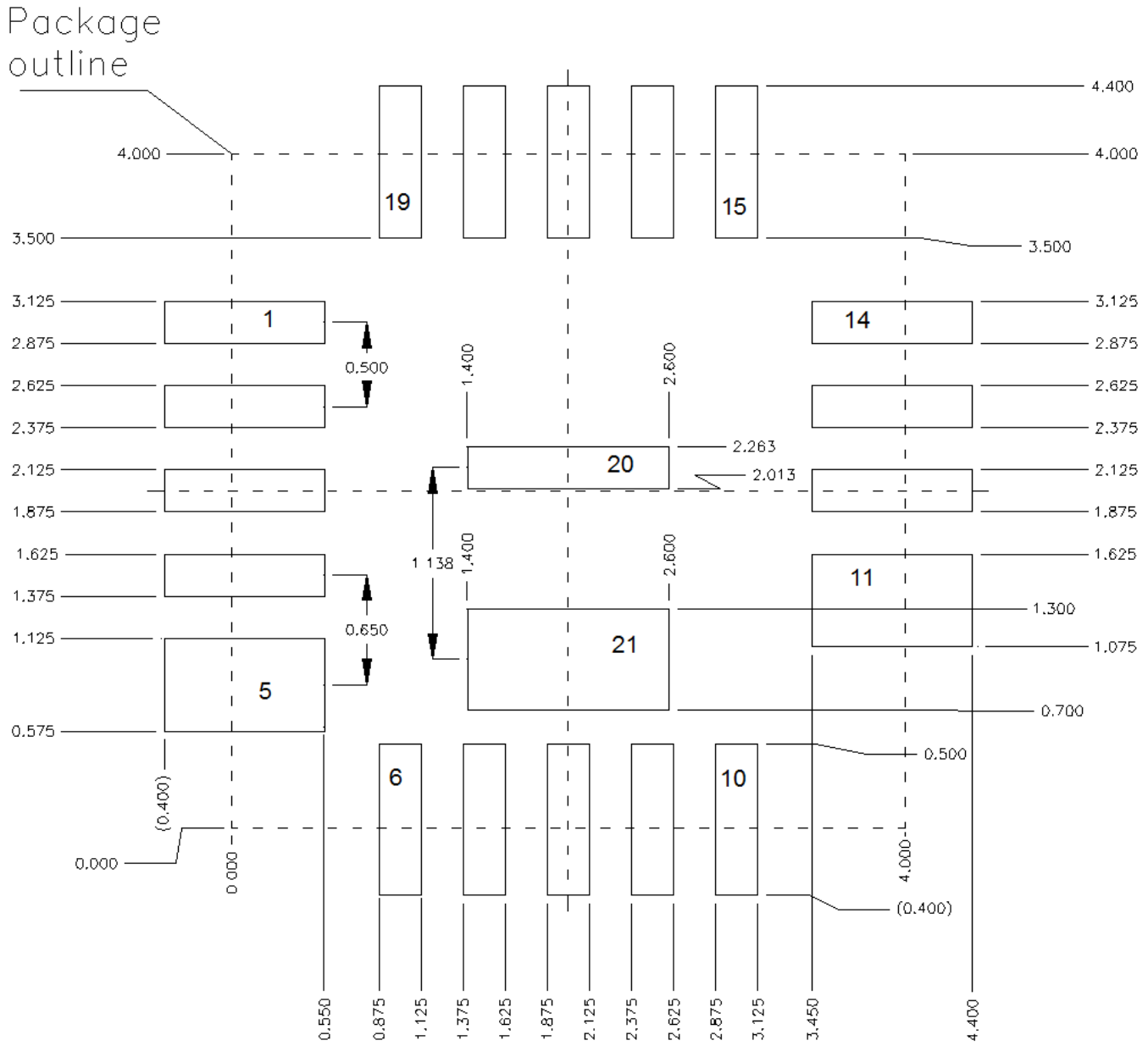


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
R	0.050	0.150	0.002	0.006
S	0.001	0.090	0.000	0.004

Tolerance
±0.050

WET W-Type 21L QFN 4x4 (FC) Package

Footprint Information



Package	Number of Pin	Tolerance
WET-V/W/U/XQFN4x4-21(FC)	21	±0.05

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