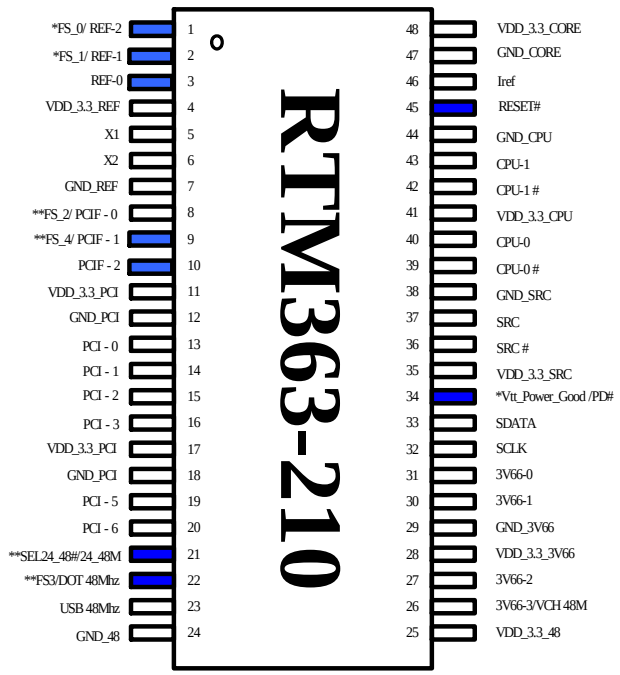
REALTEK SINGLE CHIP CLOCK GENERATOR RTM363-210

1. General Description

RTM363-210 is a 48-pin package, single-chip frequency generator that meets INTEL® CK409 clock synthesizer/driver specification. This chip provides a standard serial bus for programmable clock functions. Through this interface, spread spectrum technology can be enabled to reduce EMI.

2. Features

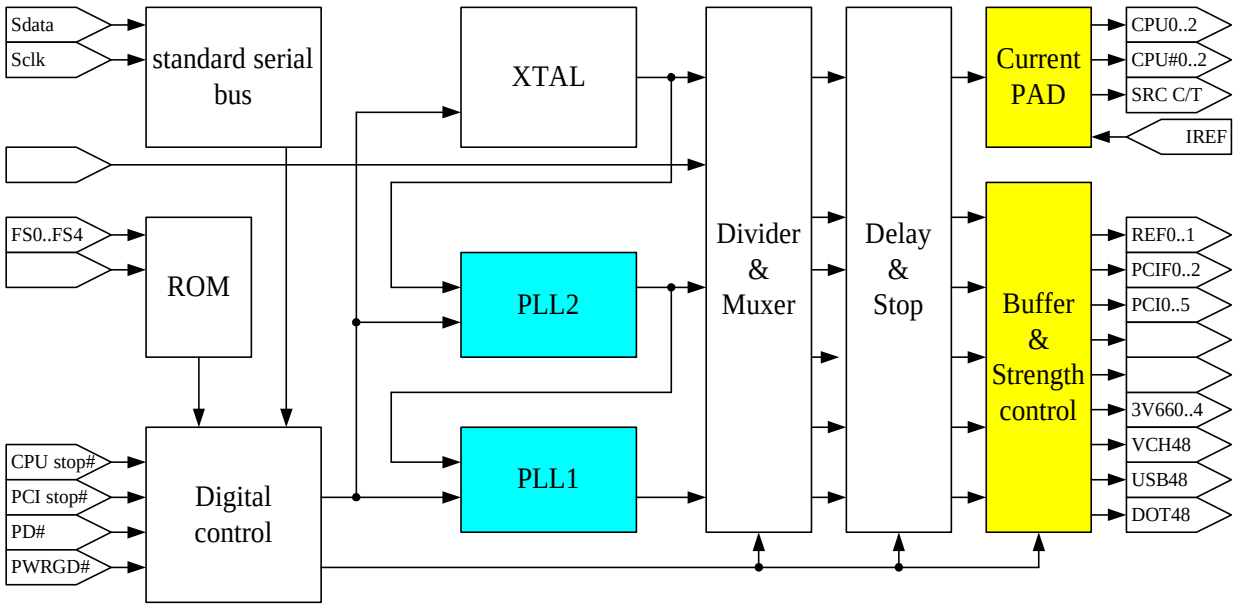
- CPU frequency ratio supports up to 400MHz
- Power down feature.
- Programmable spread spectrum depth.
- Programmable spread spectrum model.
- Programmable driving strength.
- Programmable skew delay.
- Programmable PLL frequency.
- Programmable SRC/AGP/PCI fixed mode.
- Programmable loop filter.
- Programmable smooth-divider.
- Programmable current Iref.
- Programmable watchdog & smooth reset.
- DOS,WIN9x/WIN2000/WINNT/XP apps



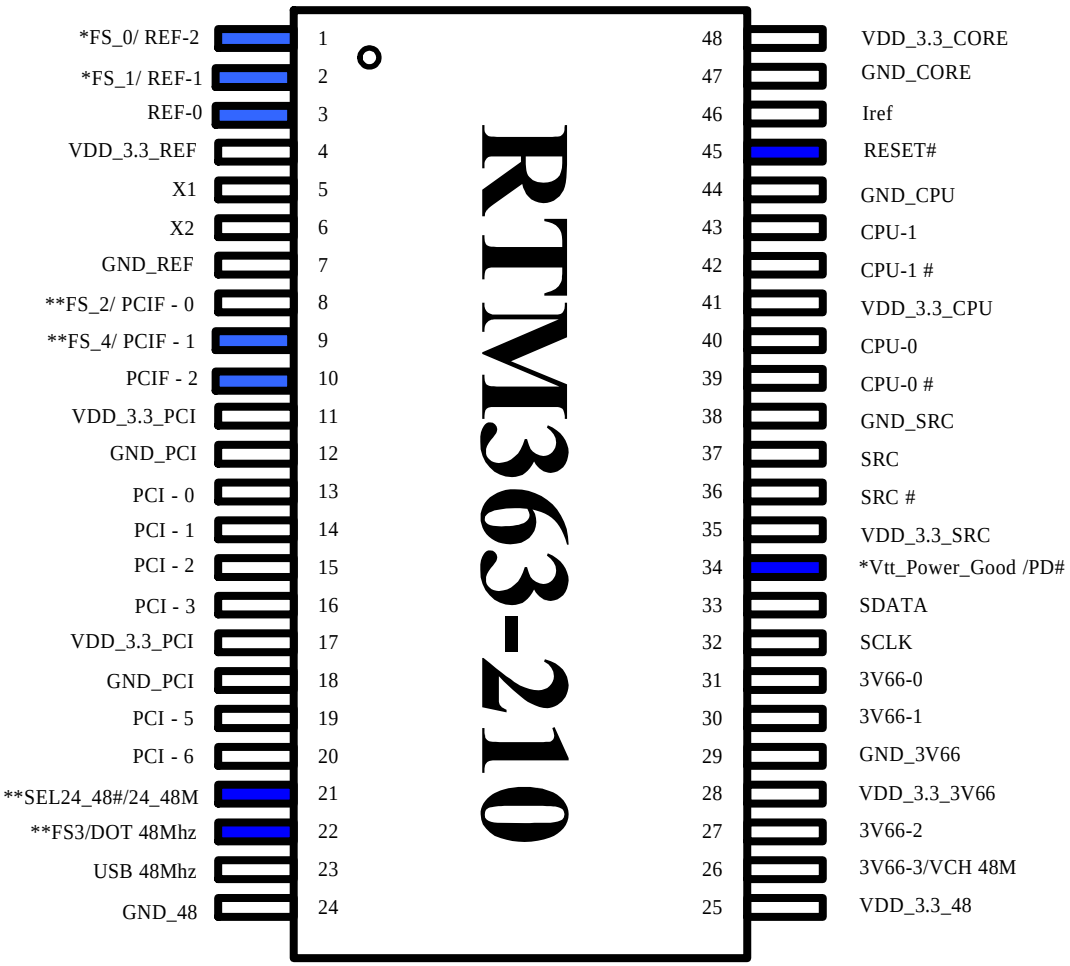
3. Revision History

Rev. No.	Description	Date
0.5	l Initial release spec.	Oct.16 2003

4. Block Diagram



5. Pin Assignment



6. Pin Description

In order to reduce pin counts, and therefore package size and cost, some pins have multiple functions. In those cases, the functions are separated with a "/" symbol. Refer to the 'Pin Assignment' diagram for a graphical representation.

Pin Name	Pin No.	Type	Description
*FS_0 / REF-2	1	I/O	**Frequency Selection 0:** FS_0 latched input for frequency selection. This pin serves as the power-on select strap to determine device's operating frequency as described in frequency Table. **Reference Clock:** 3.3V 14.318 MHz clock output.
*FS_1 / REF-1	2	I/O	**Frequency Selection 1:** FS_1 latched input for frequency selection. This pin serves as the power-on select strap to determine device's operating frequency as described in frequency Table. **Reference Clock:** 3.3V 14.318 MHz clock output.
REF-0	3	O	**Reference Clock:** 3.3V 14.318 MHz clock output.
X1	5	I	**Crystal Input:** This pin has dual functions. It can be used as an external 14.318MHz crystal connection or as an external reference frequency input.
X2	6	O	**Crystal Output:** An output connection for an external 14.318MHz crystal connection. If using an external reference, this pin must be left unconnected.
**FS_2 / PCIF-0	8	I/O	**Frequency Selection 2 :** FS_2 latched input for frequency selection. This pin serves as the power-on select strap to determine device's operating frequency as described in frequency Table **PCIF Clock 0 :** 3.3V 33 MHz free-running PCI clock outputs.
**FS_4 / PCIF-1	9	I/O	**Frequency Selection 4 :** FS_4 latched input for frequency selection. This pin serves as the power-on select strap to determine device's operating frequency as described in frequency Table **PCIF Clock 1 :** 3.3V 33 MHz free-running PCI clock outputs.
PCIF-2	10	O	**PCIF Clock 2:** 3.3V 33 MHz PCI clock outputs.
PCI [0:3], PCI[5:6]	13, 14, 15, 16, 19, 20	O	**PCI Clock 0 through 5:** 3.3V 33 MHz PCI clock outputs.
RESET#	45	O	**RESET# open drain output**: Watchdog & smooth reset output.
**SEL24_48# / 24_48M	21	I	****SEL24_48#**: Latched input for frequency selection.
		O	**24/48# MHz Clock Output**: 3.3V fixed 24/48# MHz, non-spread spectrum clock output.
**FS_3/ DOT 48MHz	22	I/O	**Frequency Selection 3:** FS_3 latched input for frequency selection. This pin serves as the power-on select strap to determine device's operating frequency as described in frequency Table. **48 MHz Clock Output**: 3.3V fixed 48 MHz, non-spread spectrum clock output.
USB 48MHz	23	O	**48 MHz Clock Output**: 3.3V fixed 48 MHz, non-spread spectrum clock output.
3V66_3 / VCH 48M	26	O	**66 MHz Clock Output / 48Mhz Clock Output:** 3.3V output clocks. The operating frequency is controlled by registers.
3V66[0:2]	31, 30,27	O	**66 MHz Clock Output:** 3.3V 66MHz output clocks.
SDATA	33	I/O	Data pin for serial interface.
SCLK	32	I	Clock input pin for serial interface.
Vtt_Power_Good/ PD#	34	I	**Vtt Power Good:** LVTTL compatible input that is a level sensitive strobe used to determine when FS[0:4] inputs are valid and OK to be sampled. One-shot function.
		I	**Power Down Control**: LVTTL compatible input that places the device in power down mode when held low.
SRC & SRC#	37,36	O/C	**Serial Reference Clock:** Serial-ATA reference clock as current-mode differential pair output. Output frequencies depending on the configuration of FS[0:4].
CPU & CPU# [0:1]	39,40,42,43	O/C	**CPU Clock Outputs:** Current-mode differential outputs. Output frequencies depending on the configuration of FS[0:4].
Iref	46	I	**Iref:** A precision resistor is attached to this pin which is connected to the internal current reference .
VDD	4, 11, 17, 25, 28, 35, 41	P	**3.3V Power Connection:** Power supply for REF output buffers, PCI output buffers, 48M output buffers ,3V66MHz output buffers ,and CPU output buffers . Connect to 3.3V.
GND	7, 12, 18, 24, 29, 38, 44	G	**Ground Connections:** Connect all ground pins to the common system ground plane.
GND_CORE	47	G	**Ground Connections:** Ground for internal core logical circuit . Connect all ground pins to the common system ground plane.
VDD_CORE	48	P	**3.3V Core Power :** Power supply for internal core logical circuit . Connect to 3.3V.

Note: Internal 150K pull-up or pull-down resistors that is presented on input pins are marked with (*) and (**) respectively. Design should not rely solely on internal pull-up or pull-down resistors to set I/O pins high or low respectively.

(*):a input pin with internal 150K ohm pull-up resistor.
(**):a input pin with internal 150K ohm pull-down resistor.

FS4	FS3	FS2	FS1/FB	FS0/FA	CPU	SRC	3V66	PCI	SSC
0	0	0	0	0	100.00	100.00	66.67	33.33	No Spread
0	0	0	0	1	133.33	100.00	66.67	33.33	No Spread
0	0	0	1	0	200.00	100.00	66.67	33.33	No Spread
0	0	0	1	1	166.66	100.00	66.66	33.33	No Spread
0	0	1	0	0	200.00	100.00	66.67	33.33	No Spread
0	0	1	0	1	266.66	100.00	66.67	33.33	No Spread
0	0	1	1	0	400.00	100.00	66.67	33.33	No Spread
0	0	1	1	1	333.33	100.00	66.67	33.33	No Spread
0	1	0	0	0	105.00	100.00	70.00	35.00	No Spread
0	1	0	0	1	140.00	100.00	70.00	35.00	No Spread
0	1	0	1	0	210.00	100.00	70.00	35.00	No Spread
0	1	0	1	1	174.99	100.00	70.00	35.00	No Spread
0	**1**	**1**	**0**	**0**	**100.90**	**100.00**	**67.27**	**33.63**	No Spread
0	**1**	**1**	**0**	**1**	**133.90**	**100.00**	**66.95**	**33.48**	No Spread
0	**1**	**1**	**1**	**0**	**200.90**	**100.00**	**66.97**	**33.48**	No Spread
0	**1**	**1**	**1**	**1**	**166.90**	**100.00**	**66.76**	**33.38**	No Spread
1	0	0	0	0	100.00	100.00	66.67	33.34	+/-0.25% center spread
1	0	0	0	1	133.33	100.00	66.67	33.34	+/-0.25% center spread
1	0	0	1	0	200.00	100.00	66.67	33.34	+/-0.25% center spread
1	0	0	1	1	166.66	100.00	66.66	33.33	+/-0.25% center spread
1	0	1	0	0	100.00	100.00	66.67	33.34	-0.5% down spread
1	0	1	0	1	133.33	100.00	66.67	33.34	-0.5% down spread
1	0	1	1	0	200.00	100.00	66.67	33.34	-0.5% down spread
1	0	1	1	1	166.66	100.00	66.66	33.33	-0.5% down spread
1	1	0	0	0	105.00	100.00	70.00	35.00	+/-0.25% center spread
1	1	0	0	1	140.00	100.00	70.00	35.00	+/-0.25% center spread
1	1	0	1	0	210.00	100.00	70.00	35.00	+/-0.25% center spread
1	1	0	1	1	174.99	100.00	70.00	35.00	+/-0.25% center spread
1	1	1	0	0	**100.90**	**100.00**	**67.27**	**33.64**	+/-0.25% center spread
1	1	1	0	1	**133.90**	**100.00**	**66.96**	**33.48**	+/-0.25% center spread
1	1	1	1	0	**200.90**	**100.00**	**66.97**	**33.49**	+/-0.25% center spread
1	1	1	1	1	**166.90**	**100.00**	**66.77**	**33.38**	+/-0.25% center spread

Frequency Table

CPU	SRC	3V66/AGP	PCI
+ /2	+ /4		+ 3V66(AGP)/2(+2.5ns)
+ /3	+ /5	+ /10	+ /20(+2.5ns)
+ /4	+ /6	+ /12	+ /24(+2.5ns)
+ /5	+ /8	+ /15	+ /30(+2.5ns)
+ /6	+ /10	Fix 66.6	Fix 33.3(+2.5ns)
+ /8	Fix 100	Fix 75.0	Fix 37.5(+2.5ns)
+ /10		Fix 85.7	Fix 42.8(+2.5ns)

Phase Table

7. Register Description

Address CR 00h [0]

Bit	Description	Pin	Type	Default
Bit7	Reserved		R/W	1
Bit6	Reserved		R/W	1
Bit5	0 = 24_48 Mhz select 48Mhz 1 = 24_48 Mhz select 24Mhz	21	R/W	Latched
Bit4	**FS4 power-on latched	9	R	Latched
Bit3	**FS3 power-on latched	22	R	Latched
Bit2	**FS2 power-on latched	8	R	Latched
Bit1	**FS1 power-on latched	2	R	Latched
Bit0	**FS0 power-on latched	1	R	Latched

Address CR 01h [1]

Bit	Description	Pin	Type	Default
Bit7	0 = SRC & SRC# clock can not be stopped by PCI_Stop# (CR03[7]) 1 = SRC & SRC# clock can be stopped by PCI_Stop# (CR03[7])	36, 37	R/W	0
Bit6	0 = SRC & SRC# clock output disable (tristate) 1 = SRC & SRC# clock output enable	36, 37	R/W	1
Bit5	Reserved		R/W	1
Bit4	0 = CPU-1 & CPU-1# clock can not be stopped by CPU_Stop# (CR03[6]) 1 = CPU-1 & CPU-1# clock can be stopped by CPU_Stop# (CR03[6])	42, 43	R/W	1
Bit3	0 = CPU-0 & CPU-0# clock can not be stopped by CPU_Stop# (CR03[6]) 1 = CPU-0 & CPU-0# clock can be stopped by CPU_Stop# (CR03[6])	39, 40	R/W	1
Bit2	Reserved		R/W	1
Bit1	0 = CPU-1 & CPU-1# clock output disable (tristate) 1 = CPU-1 & CPU-1# clock output enable	42, 43	R/W	1
Bit0	0 = CPU-0 & CPU-0# clock output disable (tristate) 1 = CPU-0 & CPU-0# clock output enable	39, 40	R/W	1

Address CR 02h [2]

Bit	Description	Pin	Type	Default
Bit7	0 = Drive SRC & SRC# when PD# is asserted 1 = Float SRC & SRC# when PD# is asserted	36, 37	R/W	0
Bit6	0 = Drive SRC & SRC# when PCI_STOP# (CR03[7]) is asserted 1 = Float SRC & SRC# when PCI _STOP# (CR03[7]) is asserted	36, 37	R/W	0
Bit5	Reserved		R/W	0
Bit4	0 = Drive CPU-1 & CPU-1# when PD# is asserted 1 = Float CPU-1 & CPU-1# when PD# is asserted	42, 43	R/W	0
Bit3	0 = Drive CPU-0 & CPU-0# when PD# is asserted 1 = Float CPU-0 & CPU-0# when PD# is asserted	39, 40	R/W	0
Bit2	Reserved		R/W	0
Bit1	0 = Drive CPU-1 & CPU-1# when CPU_STOP# (CR03[6]) is asserted 1 = Float CPU-1 & CPU-1# when CPU_STOP# (CR03[6]) is asserted	42, 43	R/W	0
Bit0	0 = Drive CPU-0 & CPU-0# when CPU_STOP# (CR03[6]) is asserted 1 = Float CPU-0 & CPU-0# when CPU_STOP# (CR03[6]) is asserted	39, 40	R/W	0

Address CR 03h [3]

Bit	Description	Pin	Type	Default
Bit7	Internal PCI_Stop# 0 = internal PCI_Stop# asserted 1 = internal PCI_Stop# de-asserted	8, 9, 10, 13, 14, 15, 16, 19, 20	R/W	1
Bit6	Internal CPU_Stop# 0 = internal CPU_Stop# asserted 1 = internal CPU_Stop# de-asserted	39,40,42,43	R/W	1
Bit5	0 = PCI-5 disable 1 = PCI-5 enable	20	R/W	1
Bit4	0 = PCI-4 disable (Only for RTM363-212) 1 = PCI-4 enable	19	R/W	1
Bit3	0 = PCI-3 disable 1 = PCI-3 enable	16	R/W	1
Bit2	0 = PCI-2 disable 1 = PCI-2 enable	15	R/W	1
Bit1	0 = PCI-1 disable 1 = PCI-1 enable	14	R/W	1
Bit0	0 = PCI-0 disable 1 = PCI-0 enable	13	R/W	1

Address CR 04h [4]

Bit	Description	Pin	Type	Default
Bit7	0 = USB 48Mhz 2.0X driving strength(RTM363-210 Only!) 1 = USB 48Mhz 1.0X driving strength	23	R/W	0
Bit6	0 = USB 48Mhz disable(RTM363-210 Only!) 1 = USB 48Mhz enable	23	R/W	1
Bit5	0 = PCIF_2 can not be stopped by PCI_Stop# (CR03[7]) 1 = PCIF_2 can be stopped by PCI_Stop# (CR03[7])	10	R/W	0
Bit4	0 = PCIF_1 can not be stopped by PCI_Stop# (CR03[7]) 1 = PCIF_1 can be stopped by PCI_Stop# (CR03[7])	9	R/W	0
Bit3	0 = PCIF_0 can not be stopped by PCI_Stop# (CR03[7]) 1 = PCIF_0 can be stopped by PCI_Stop# (CR03[7])	8	R/W	0
Bit2	0 = PCIF-2 disable 1 = PCIF-2 enable	10	R/W	1
Bit1	0 = PCIF-1 disable 1 = PCIF-1 enable	9	R/W	1
Bit0	0 = PCIF-0 disable 1 = PCIF-0 enable	8	R/W	1

1.> CR04h[7]: USB o/p pad driving strength setting.
2.> USB driving strength has 4 levels (set by CR17h[5:4]).
3.> USB o/p pad driving strength setting is an 'OR' operation on inversed CR04h[7] and the logic level of CR17h[5]
4.> CR04h[7] follows Intel's spec: "0" as 2X driving strength and "1" as normal. Setting for "2X" is used when two 48MHz devices are driven.
5.> To get the final setting of USB o/p driving strength, CR04h[7] is inversed first , then 'OR' combined with CR17h[5].
6.> For example, if CR17h[5:4] = [00], this would set the USB driving strength as 1.0X(normal). When CR04h[7]=0 ,the inversed logic is"1", and then 'OR' combined with CR17h[5]. So, the final USB driving strength setting becomes [10], as 1.5x driving strength.

Address CR 05h [5]

Bit	Description	Pin	Type	Default
Bit7	0 = DOT 48Mhz disable 1 = DOT 48Mhz enable	22	R/W	1
Bit6	0 = REF2 disable 1 = REF2 enable	1	R/W	1
Bit5	0 = 3V66-3/VCH_48 select 66Mhz 1 = 3V66-3/VCH_48 select 48Mhz	26	R/W	0
Bit4	0 = 3V66-3 / VCH_48 Mhz disable 1 = 3V66-3 / VCH_48 Mhz enable	26	R/W	1
Bit3	0 = 24_48MHz disable 1 = 24_48MHz enable	21	R/W	1
Bit2	0 = 3V66-2 disable 1 = 3V66-2 enable	27	R/W	1
Bit1	0 = 3V66-1 disable 1 = 3V66-1 enable	30	R/W	1
Bit0	0 = 3V66-0 disable 1 = 3V66-0 enable	31	R/W	1

Address CR 06h [6]

Bit	Description	Pin	Type	Default
Bit7	RESERVED		R/W	0
Bit6	RESERVED		R/W	0
Bit5	0 = PCI-7 disable (Only for RTM363-212) 1 = PCI-7 enable		R/W	1
Bit4	0 = PCI-6 disable (Only for RTM363-212) 1 = PCI-6 enable		R/W	1
Bit3	RESERVED		R/W	1
Bit2	0 = spread spectrum disable 1 = spread spectrum enable		R/W	Latched
Bit1	0 = REF-1 output disable 1 = REF-1 output enable	2	R/W	1
Bit0	0 = REF-0 output disable (Only for RTM363-210) 1 = REF-0 output enable	3	R/W	1

Address CR 07h [7]

Bit	Description	Type	Default
Bit7	Revision Code	R	**1**
Bit6	Revision Code	R	**0**
Bit5	Revision Code	R	**0**
Bit4	Revision Code	R	**0**
Bit3	Vender Code	R	1
Bit2	Vender Code	R	1
Bit1	Vender Code	R	1
Bit0	Vender Code	R	0

REALTEK Vender ID = 0Eh

Address CR 08h [8]

Bit	Description	Default
Bit7	0 = frequency is selected by latched input FS[4:0] 1 = frequency is selected by CR08h[5:0]	0
Bit6	Reserved	0
Bit5	Reserved	0

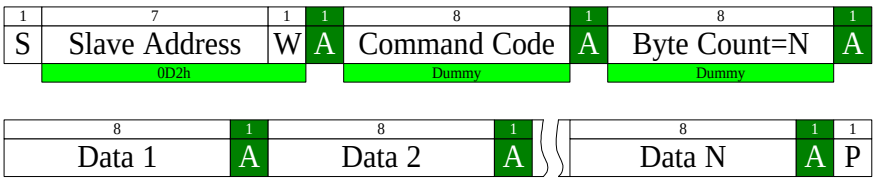
Bit4	Bit3	Bit2	Bit1	Bit0	CPU	SRC	3V66	PCI	SSC
0	0	0	0	0	100.00	100.00	66.67	33.33	No Spread
0	0	0	0	1	133.33	100.00	66.67	33.33	No Spread
0	0	0	1	0	200.00	100.00	66.67	33.33	No Spread
0	0	0	1	1	166.66	100.00	66.66	33.33	No Spread
0	0	1	0	0	200.00	100.00	66.67	33.33	No Spread
0	0	1	0	1	266.66	100.00	66.67	33.33	No Spread
0	0	1	1	0	400.00	100.00	66.67	33.33	No Spread
0	0	1	1	1	333.33	100.00	66.67	33.33	No Spread
0	1	0	0	0	105.00	100.00	70.00	35.00	No Spread
0	1	0	0	1	140.00	100.00	70.00	35.00	No Spread
0	1	0	1	0	210.00	100.00	70.00	35.00	No Spread
0	1	0	1	1	174.99	100.00	70.00	35.00	No Spread
0	1	1	0	0	**100.90**	**100.00**	**67.27**	**33.63**	No Spread
0	1	1	0	1	**133.90**	**100.00**	**66.95**	**33.48**	No Spread
0	1	1	1	0	**200.90**	**100.00**	**66.97**	**33.48**	No Spread
0	1	1	1	1	**166.90**	**100.00**	**66.76**	**33.38**	No Spread
1	0	0	0	0	100.00	100.00	66.67	33.34	+/-0.25% center spread
1	0	0	0	1	133.33	100.00	66.67	33.34	+/-0.25% center spread
1	0	0	1	0	200.00	100.00	66.67	33.34	+/-0.25% center spread
1	0	0	1	1	166.66	100.00	66.66	33.33	+/-0.25% center spread
1	0	1	0	0	100.00	100.00	66.67	33.34	-0.5% down spread
1	0	1	0	1	133.33	100.00	66.67	33.34	-0.5% down spread
1	0	1	1	0	200.00	100.00	66.67	33.34	-0.5% down spread
1	0	1	1	1	166.66	100.00	66.66	33.33	-0.5% down spread
1	1	0	0	0	105.00	100.00	70.00	35.00	+/-0.25% center spread
1	1	0	0	1	140.00	100.00	70.00	35.00	+/-0.25% center spread
1	1	0	1	0	210.00	100.00	70.00	35.00	+/-0.25% center spread
1	1	0	1	1	174.99	100.00	70.00	35.00	+/-0.25% center spread
1	1	1	0	0	**100.90**	**100.00**	**67.27**	**33.64**	+/-0.25% center spread
1	1	1	0	1	**133.90**	**100.00**	**66.96**	**33.48**	+/-0.25% center spread
1	1	1	1	0	**200.90**	**100.00**	**66.97**	**33.49**	+/-0.25% center spread
1	1	1	1	1	**166.90**	**100.00**	**66.77**	**33.38**	+/-0.25% center spread

Bit	Default
Bit4	0
Bit3	0
Bit2	0
Bit1	0
Bit0	0

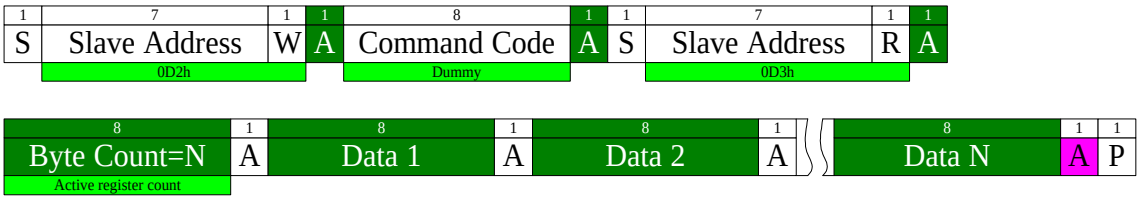
8. Functionality

Standard Serial Bus Control:
Support standard serial bus block-mode and direct word-mode.
Byte Count = 020h
Direct-word-mode index = 1xxx-xxxx Binary (MSB=1)

8.1 Block Mode

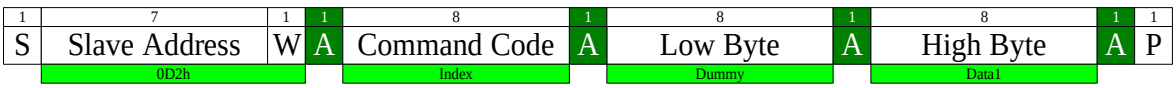


Block Write

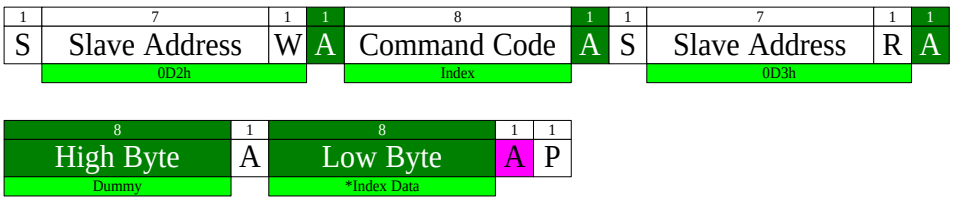


Block Read

8.2 Word Mode



Write Word



Read Word

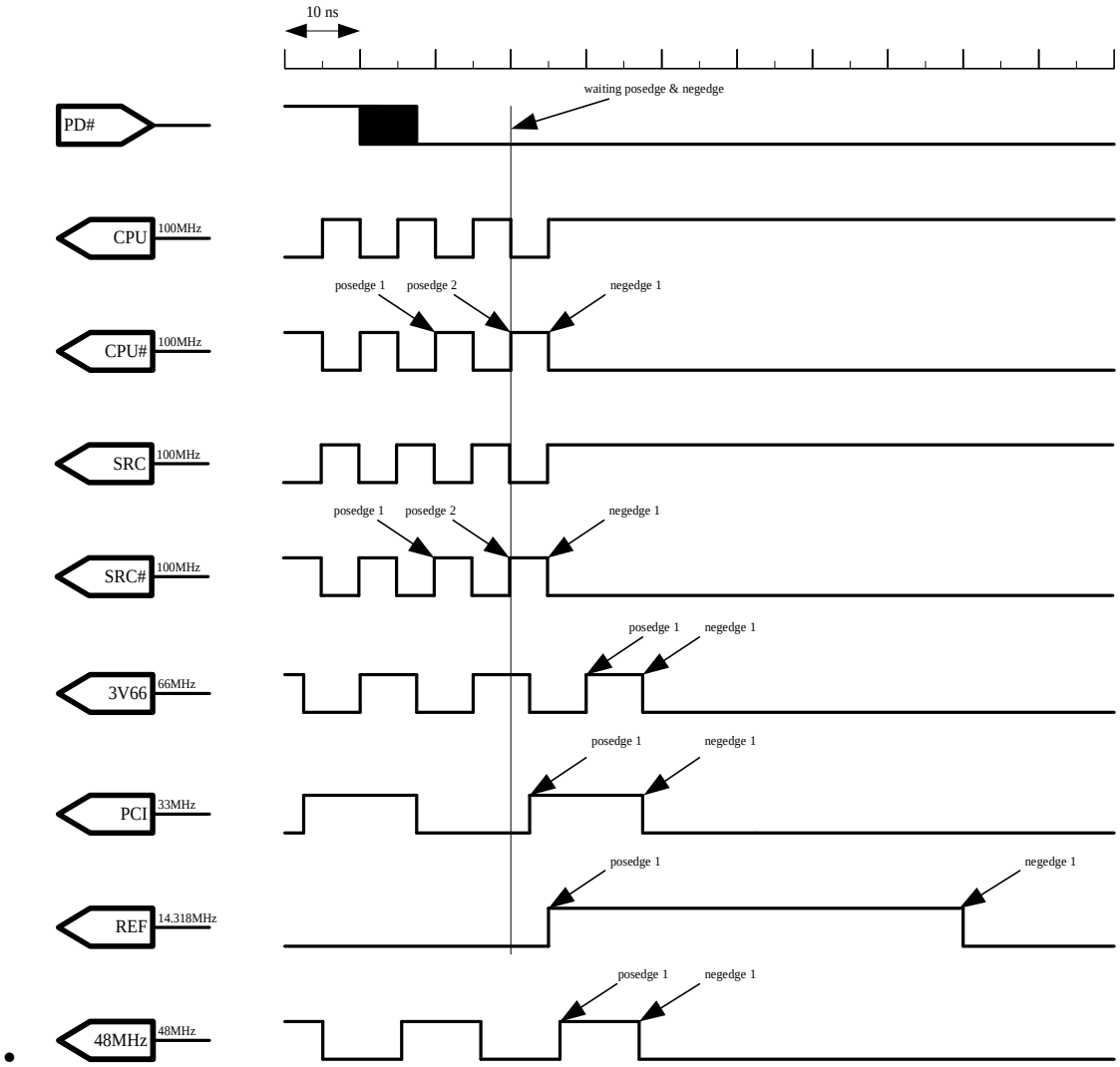
Note: slave address is D2h.

8.3 Power Down

- After *PD# is sampled active (Low) for 2 consecutive rising edges of CPUCLK#, all the output clocks are driven Low on their next High to Low transition

Power-up latency <1.8ms

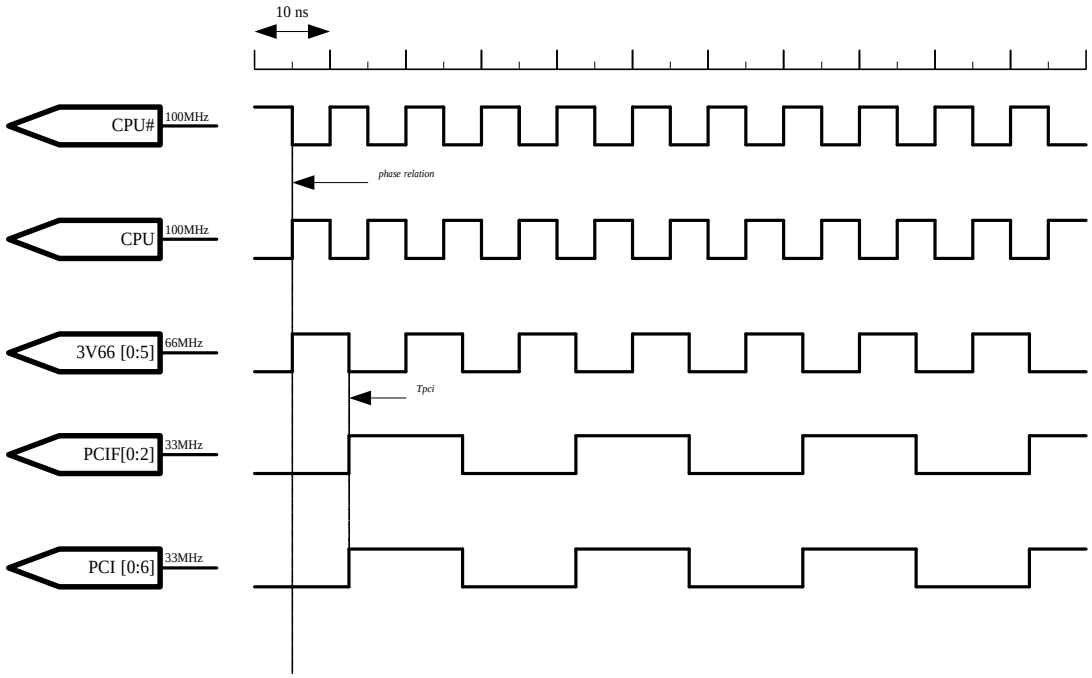
*PD#	CPU	CPU#	SRC	SRC#	3V66	PCI	REF	USB	DOT	Osc	VCOs	Itotal
0	Iref*2	Low	Iref*2	Low	Low	Low	Low	Low	Low	Off	Off	35 mA
0	float	float	float	float	Low	Low	Low	Low	Low	Off	Off	12 mA
1	On	On	On	On	On	On	On	On	On	On	On	350 mA



Power Down Waveform

8.4 Group Skew

Group	Symbol	Conditions	Minimum	Typical	Maximum	Units
CPU [0:3]	Group skew	CPU @ 0.35V	0		100	ps
3V66 [0:4]	Group skew	3V66 @ 1.5V	0		250	ps
PCIF [0:2] & PCI [0:6]	Group skew	PCI @ 1.5V	0		500	ps
USB/DOT/VCH 48	Group skew	48MHz@ 1.5V(USB48 180 Degrees phase offset)	0		1	ns
REF[0:1]	Group skew	REF@ 1.5V	0		500	ps
3V66 to PCI	3V66-PCI skew	3V66@ 1.5V, PCI @ 1.5V	1.5		3.5	ns



Group Skew Waveform

8.5 Host Swing Select

CR1eh,bit1	Z	Rref	Iref	Output current	Voh@Z
0	50	221 1%	5.00 mA	4*Iref	1.0V@50
1	50	475 1%	2.32 mA	6*Iref	0.7V@50

Iref=1.1/Rref

9. Electrical Characteristics

9.1 DC Specifications

Symbol	Parameter	Minimum	Maximum	Units	Notes
Absolute VDD A	3.3V core supply Voltage	-0.5	4.6	V	
Absolute VDD I/O	3.3V I/O supply Voltage	-0.5	4.6	V	
Ts	Storage Temperature	-65	150	°C	
Ta	Ambient Temperature	0	70	°C	
Absolute Vih	3.3V input high voltage	-0.5	4.6	V	
Absolute Vil	3.3V input low voltage	-0.5		V	
ESD	Input ESD protection	2000		V	Human body mode
Operating Vdd A	3.3V core supply Voltage	3.135	3.465	V	
Operating Vdd I/O	3.3V I/O supply Voltage	3.135	3.465	V	
Operating Vih	3.3V input high voltage	2.0	Vdd+0.3	V	
Operating Vil	3.3V input low voltage	Vss-0.3	0.8	V	
Operating Iil	Input leakage current	-5	+5	uA	
Operating Voh	3.3V output high voltage	2.4		V	Ioh=-1mA
Operating Vol	3.3V output low voltage		0.4	V	Iol=1mA
Cin	Input pin capacitance	3	5	pF	
Cxtal	XTAL pin capacitance	3	5	pF	17..20 pF
Cout	Output pin capacitance		6	pF	
Lpin	Pin inductance		7	nH	

9.2 AC Specifications

9.2.1 CPU 0.7V

T_A = 0 - 70C, CPU V_{out} =0.7 V, Vol=0.14V, Voh=0.56V, Test load Rs=33.2 Rp=49.9

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Frequency		100/133/166/200/233/266/333/400 Mhz	100		400	MHz
Output Impedance				50		Ω
Overshoot Voltage					VH+0.3	V
Undershoot Voltage			-0.3			V
Rising edge ring back					0.2	V
Falling edge ring back					0.2	V
Output High Current				6*Iref		mA
Output Low Current				0		mA
V high			660	710	850	mV
V low			-150	0		mV
V cross			2500		550	mV
V cross rising Variation					Calc	mV
V cross all Variation					140	mV
Rise Time		Vol=0.175V, Voh=0.525V	175		700	ps
Fall Time		Vol=0.175V, Voh=0.525V	175		700	ps
Rise Time Variation		Vol=0.175V, Voh=0.525V			125	ps
Fall Time Variation		Vol=0.175V, Voh=0.525V			125	ps
Rise/Fall matching		2*(Trise-Tfall)/ (Trise+Tfall)			20	%
Duty Cycle			45	50	55	%
Skew					100	ps
Jitter					125	ps

9.2.2 SRC 0.7V

T_A = 0 - 70C, SRC V_{out} =0.7 V, Vol=0.175V, Voh=0.525V, Test load Rs=33.2 Rp=49.9

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Frequency		100/133/166/200 Mhz	100		200	MHz
Output Impedance				50		Ω
Overshoot Voltage					VH+0.3	V
Undershoot Voltage			-0.3			V
Rising edge ring back					0.2	V
Falling edge ring back					0.2	V
Output High Current				6*Iref		mA
Output Low Current				0		mA
V high			660	710	850	mV
V low			-150	0		mV
V cross			2500		550	mV
V cross rising Variation					Calc	mV
V cross all Variation					140	mV
Rise Time		Vol=0.175V, Voh=0.525V	175		700	ps
Fall Time		Vol=0.175V, Voh=0.525V	175		700	ps
Rise Time Variation		Vol=0.175V, Voh=0.525V			125	ps
Fall Time Variation		Vol=0.175V, Voh=0.525V			125	ps
Rise/Fall matching		2*(Trise-Tfall)/ (Trise+Tfall)			20	%
Duty Cycle			45	50	55	%
Skew						ps
Jitter					125	ps

9.2.3 3V66/AGP

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 30 pF (unless otherwise stated)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Frequency						MHz
Output Impedance		VO = VDD*(0.5)	12		55	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.55	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 3.153V	-29		-23	mA
Output Low Current		VOL @MIN= 2.0V , VOL@ MAX= 0.4V	27		29	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	0.5		2	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	0.5		2	ns
Duty Cycle		VT = 1.5 V	45	50	55	%
Skew		VT = 1.5 V			500	ps
Jitter		VT = 1.5 V			250	ps

9.2.4 PCI

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 30 pF (unless otherwise stated)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Frequency				33		MHz
Output Impedance		VO = VDD*(0.5)	12		55	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 3.153V	-29		-23	mA
Output Low Current		VOL @MIN= 2.0V , VOL@ MAX= 0.4V	27		29	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	0.5		2	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	0.5		2	ns
Duty Cycle		VT = 1.5 V	45	50	55	%
Skew		VT = 1.5 V			500	ps
Jitter		VT = 1.5 V			500	ps

9.2.5 REF

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 30 pF (unless otherwise stated)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Frequency				14.318		MHz
Output Impedance		VO = VDD*(0.5)	10		55	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 3.153V	-33		-33	mA
Output Low Current		VOL @MIN= 2.0V , VOL@ MAX= 0.4V	30		38	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	1		4	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	1		4	ns
Duty Cycle		VT = 1.5 V	45	50	55	%
Skew		VT = 1.5 V				ps
Jitter		VT = 1.5 V			1000	ps

9.2.6 DOT 48MHz

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 5 - 10 pF (unless otherwise stated)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Frequency				48		MHz
Output Impedance		VO = VDD*(0.5)	20		60	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 3.153V	-29		-23	mA
Output Low Current		VOL @MIN= 2.0V , VOL@ MAX= 0.4V	27		29	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	0.5		2	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	0.5		2	ns
Duty Cycle		VT = 1. 5 V	45	50	55	%
Skew		VT = 1.5 V			250	ps
Long term jitter		10us period jitter @VT = 1.5 V			2	ns
Jitter		VT = 1.5 V			500	ps

9.2.7 USB 48MHz

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 20 pF (unless otherwise stated)

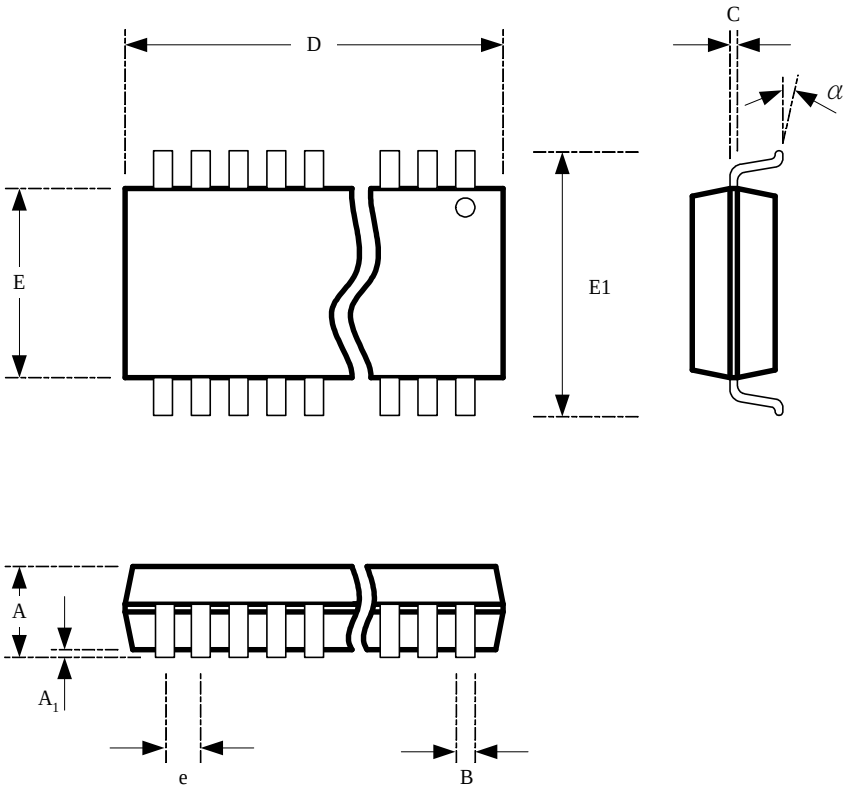
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Frequency				48		MHz
Output Impedance		VO = VDD*(0.5)	20		60	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 3.153V	-29		-23	mA
Output Low Current		VOL @MIN= 2.0V , VOL@ MAX= 0.4V	27		29	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	0.5		2	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	0.5		2	ns
Duty Cycle		VT = 1. 5 V	45	50	55	%
Skew		VT = 1.5 V			250	ps
Long term jitter		125us period jitter @VT = 1.5 V			6	ns
Jitter		VT = 1.5 V			500	ps

9.2.8 VCH 48MHz

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 20 pF (unless otherwise stated)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Frequency				48		MHz
Output Impedance		VO = VDD*(0.5)	20		60	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 3.153V	-29		-23	mA
Output Low Current		VOL @MIN= 2.0V , VOL@ MAX= 0.4V	27		29	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	0.5		2	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	0.5		2	ns
Duty Cycle		VT = 1. 5 V	45	50	55	%
Skew		VT = 1.5 V			250	ps
Long term jitter		125us period jitter @VT = 1.5 V			6	ns
Jitter		VT = 1.5 V			500	ps

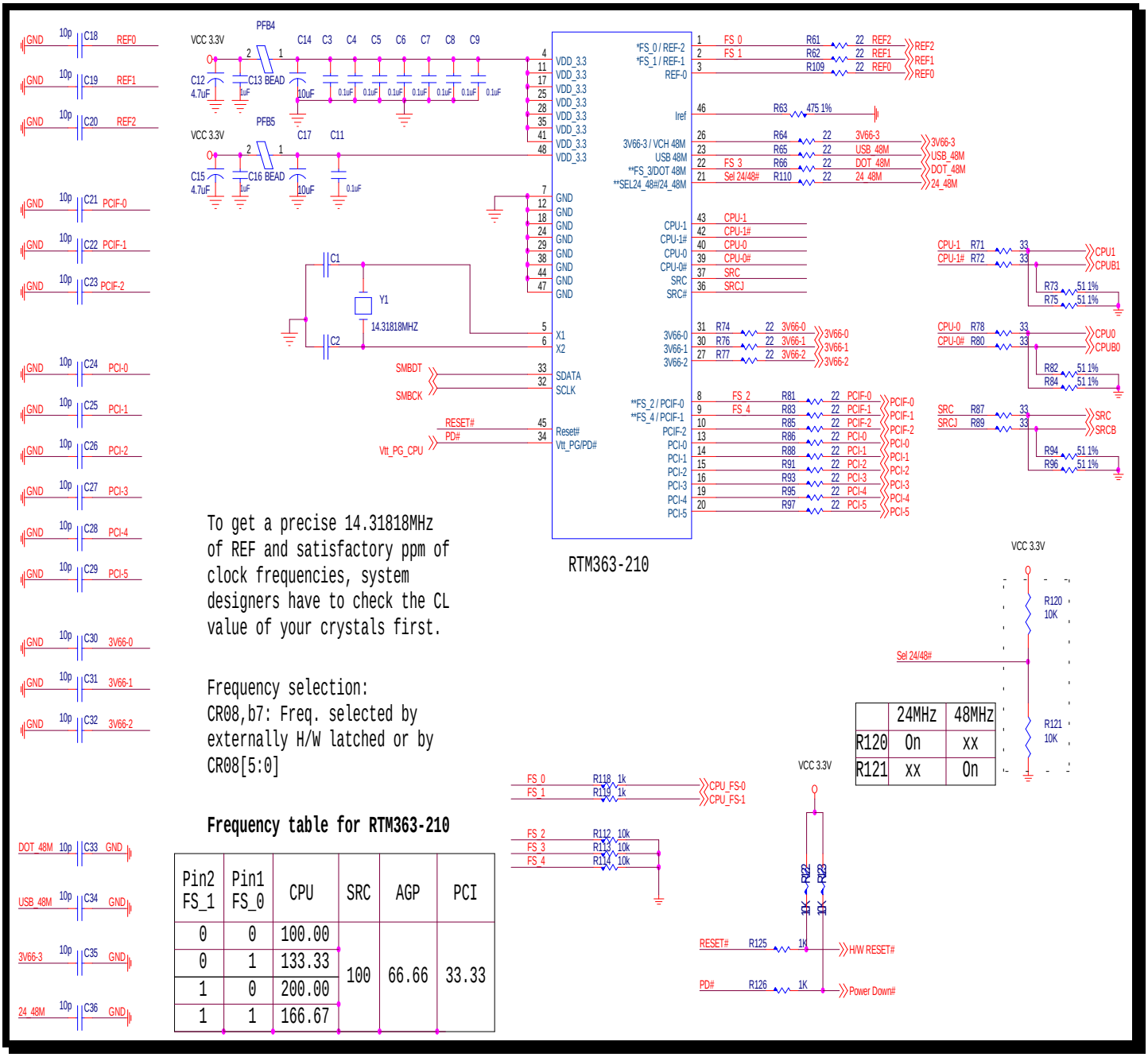
10. Mechanical Dimensions



SSOP Package:(unit using inches)

Symbol	Common Dimensions			Variations	D			N
	Minimum	Typical	Maximum		Minimum	Typical	Maximum	
A	0.095	0.101	0.110	AC	0.620	0.625	0.630	48
A1	0.008	0.012	0.016	AD	0.720	0.725	0.730	56
B	0.008	0.010	0.0135					
C	0.005	0.0075	0.010					
D	See Variations							
E	0.292	0.296	0.299					
E1	0.395	0.415	0.420					
e	0.025BSC							
α	0°	5°	10°					

11. Demo Board Circuit



1.> Please refer to the main board design guide.
2.> Please refer to section 12 for values of C1 & C2

12. Quartz Crystal Requirements

12.1 Frequency and Oscillation Circuits

RTM363 series are designed to work from a crystal with 14.31818MHz.

Fig-1 shows the equivalent circuits of crystal and oscillation circuits within RTM363 series.

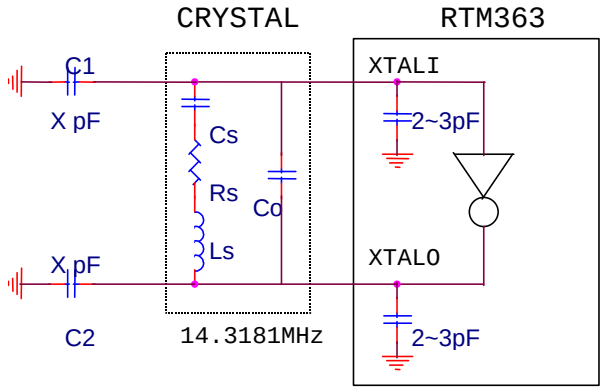


Fig-1 oscillation circuits

$$Fs \cong \frac{1}{2p\sqrt{Ls * Cs}}$$

The series resonant frequency, and parallel resonant frequency:

$$Fp \cong \frac{1}{2p\sqrt{\frac{Ls * Cs * Co}{Cs + Co}}}$$

The oscillated frequency between *Fs* and *Fp*

$$Fo = Fs * \sqrt{1 + \frac{Cs}{Co + CL}}$$

where C_L=[(C1+2pF)*(C2+2pF)] / [(C1+2pF)+(C2+2pF)]

12.2 Crystal Requirements

General Specifications	Requirements
Holder Type	HC-49 U/S
Crystal Freq.	14.31818 MHz
Oscillation Mode	Fundamental
Load Cap. (CL)	10 ~32 pF
Freq. Tolerance(25°C)	+/- 30 ppm
Effective Series Resistance (Rs)	40 ohm max
Effective Shunt Capacitance (Co)	7 pF
Drive Level	< 0.1 mW
Insulation Resistance	500 Mohm min. at DC 100V

Table-1 Crystal General Specification

12.3 Load Capacitance (C_L)

To operate between Fs and Fp requires external load capacitance. So C1 and C2 must be used.

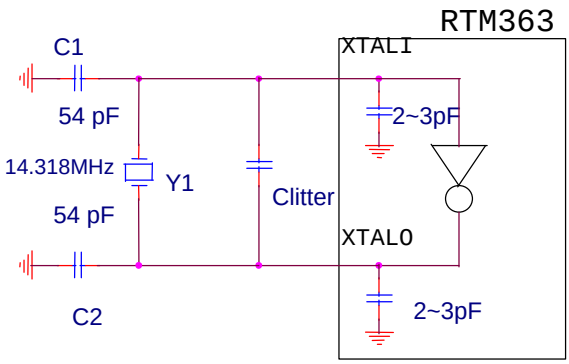


Fig-2 Clitter due to PCB Trace

In ideal case, ignore the C_{litter} at suggested C1=C2=54pF, the equivalent load capacitance is:

$$C_L = ((54pF + 2pF) * (54pF + 2pF)) / ((54pF + 2pF) + (54pF + 2pF)) = 28pF$$

According to Table-1, the crystal with C_L=28pF is adapted. But in most case, the litter capacitor (C_{litter}) generated by PCB trace is existent. So the real C_L is

$$C_L = (C1 + 2pF) // (C2 + 2pF) + C_{litter}$$

Consider the litter capacitance , crystal with C_L=28pF is allowable.

12.4 Reference Table

C_L (pF)	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
C_1=C_2 (pF)	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48	50	52	54	56	58	60	62

Table-2 Crystal C_L General Specification

For detail application about the selection of C1 & C2, please refer to crystal design guide.

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