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RTL8156BG(S)-CG

INTEGRATED 10/100/1000M/2.5G ETHERNET CONTROLLER FOR USB 3.0 APPLICATIONS

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2020/04/24	First release.
1.1	2020/05/26	Revised Table 20 EEPROM Interface, page 19. Revised 6.24 Configuration Sequence, page 28.

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1. General Description

The Realtek RTL8156BG-CG/RTL8156BGS-CG (hereafter referred to as the RTL8156BG(S) (except where differences exist) 10/100/1000M/2.5G Ethernet controller combines a four-speed IEEE 802.3 compatible Media Access Controller (MAC) with a four-speed Ethernet transceiver, USB 3.0 bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8156BG(S) offers high-speed transmission over CAT 5e UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, MDI swap, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, RFI protection, thermal management, loopback diagnostic capability, and error correction are implemented to provide robust transmission and reception capabilities. The RTL8156BG(S) features embedded One-Time-Programmable (OTP) memory that can replace the external EEPROM (93C46/93C56/93C66).

Only the RTL8156BGS provides a built-in switching regulator.

The RTL8156BG(S) features USB 3.0 to provide higher bandwidth and improved protocols for data exchange between the host and the device. USB 3.0 also offers more advanced power management features for energy saving. The RTL8156BG(S) is compatible with the IEEE 802.3u specification for 10/100Mbps Ethernet, the IEEE 802.3ab specification for 1000Mbps Ethernet, and the IEEE 802.3bz specification for 2500Mbps Ethernet.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. In addition to the ACPI feature, remote wake-up (including AMD Magic Packet and Microsoft Wake-Up Frame) is supported in both ACPI and APM (Advanced Power Management) environments.

The RTL8156BG(S) supports Microsoft Wake Packet Detection (WPD) to provide Wake-Up Frame information to the OS, e.g., PatternID, OriginalPacketSize, SavedPacketSize, SavedPacketOffset, etc. WPD helps prevent unwanted/unauthorized wake-up of a sleeping computer.

The RTL8156BG(S) supports ‘RealWoW!’ technology to enable remote wake-up of a sleeping PC through the Internet. This feature allows PCs to reduce power consumption by remaining in low power sleeping state until needed.

Note: The ‘RealWoW!’ service requires registration on first time use.

The RTL8156BG(S) supports Protocol offload. It offloads some of the most common protocols to NIC hardware in order to prevent spurious wake-up and further reduce power consumption. The RTL8156BG(S) can offload ARP (IPv4) and NS (IPv6) protocols while in the D3 power saving state.

The RTL8156BG(S) supports the ECMA (European Computer Manufacturers Association) proxy for sleeping hosts standard. The standard specifies maintenance of network connectivity and presence via proxies in order to extend the sleep duration of higher-powered hosts. It handles some network tasks on behalf of the host, allowing the host to remain in sleep mode for longer periods. Required and optional behavior of an operating proxy includes generating reply packets, ignoring packets, and waking the host.

The RTL8156BG(S) supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE). IEEE 802.3az-2010 operates with the IEEE 802.3 Media Access Control (MAC) Sublayer to support operation in Low Power Idle mode. When the Ethernet network is in low link utilization, EEE allows systems on both sides of the link to save power.

The RTL8156BG(S) is compatible with Microsoft NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum and Segmentation Task-offload (Large send and Giant send) features, and supports IEEE 802.1P Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The maximum supported jumbo frame length of the RTL8156BG(S) is 16384 bytes.

The RTL8156BG(S) is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, docking station, and embedded applications.

2. Features

Hardware

- Integrated 10M BASE-Te and 100/1000M/2.5G transceiver
- Supports 2.5G and 1G Lite mode
- Auto-Negotiation with Extended Next Page (XNP) capability
- Compatible with NBASE-T™ Alliance PHY Specification
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Configurable MDI port ordering (MDI swap) for easy PCB layout
- Supports USB 3.0 and 2.0
- Supports CDC-ECM
- Supports CDC-NCM
- Supports LPM (Link Power Management), U1/U2/U3 at SuperSpeed, and L1/L2 at HighSpeed
- Embedded OTP memory
- Supports hardware CRC (Cyclic Redundancy Check) function
- Transmit/Receive on-chip buffer support
- Supports 25MHz Crystal or external Oscillator
- Built-in switching regulator (RTL8156BGS only)
- Generate reference clock from Crystal
- Supports power down/link down power saving
- Supports Customizable LEDs
- Controllable LED Blinking Frequency and Duty Cycle
- Self-Loopback diagnostic capability
- Thermal management
- 56-pin QFN 'Green' package
- LAN disable/Link state with GPIO pin
- Supports ECMA-393 ProxZzzy Standard for sleeping hosts (see Note 1)
- Wake-On-LAN and 'RealWoW!' Technology (remote wake-up) support (see Note 1)
- EEPROM Interface
- SPI Flash Interface – supports auto-install driver
- Supports WakeUp pin in on-board system

  Note 1: Select between RealWoW! or ECMA; only one feature can be active at a time

- TWSI Interface

IEEE

- Compatible with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Supports IEEE 802.3az (Energy Efficient Ethernet)
- Supports IEEE 802.3bz (2.5GBASE-T)
- Supports Full Duplex flow control (IEEE 802.3x)

Software Offload

- Microsoft NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send v1 and Large send v2) support
- Supports jumbo frame to 16K bytes
- Supports Protocol Offload (ARP & NS)

Microsoft AOAC (Always On Always Connected)/Modern Standby

- Supports 32-set 128-byte Wake-Up Frame pattern exact matching
- Supports link change wake up
- Supports Microsoft WPD (Wake Packet Detection)

Intel CPPM (Converged Platform Power Management)

- Supports L1 with 3ms BESL (USB 2.0)
- Dynamic LTM messaging (USB 3.0)
- Supports U1/U2/U3 (USB 3.0)
- Supports selective suspend

Realtek Dragon Software

- Smart Auto Adjust Bandwidth Control
- Visual User Friendly UI
- Visual Network Usage Statistics
- Optimized Default Setting for Game, Browser, and Streaming Modes
- User Customized Priority Control

3. System Applications

USB 10/100/1000M/2.5G Ethernet on Motherboard, Notebook, or Embedded systems

4. Pin Assignments

4.1. RTL8156BGS Pin Assignments

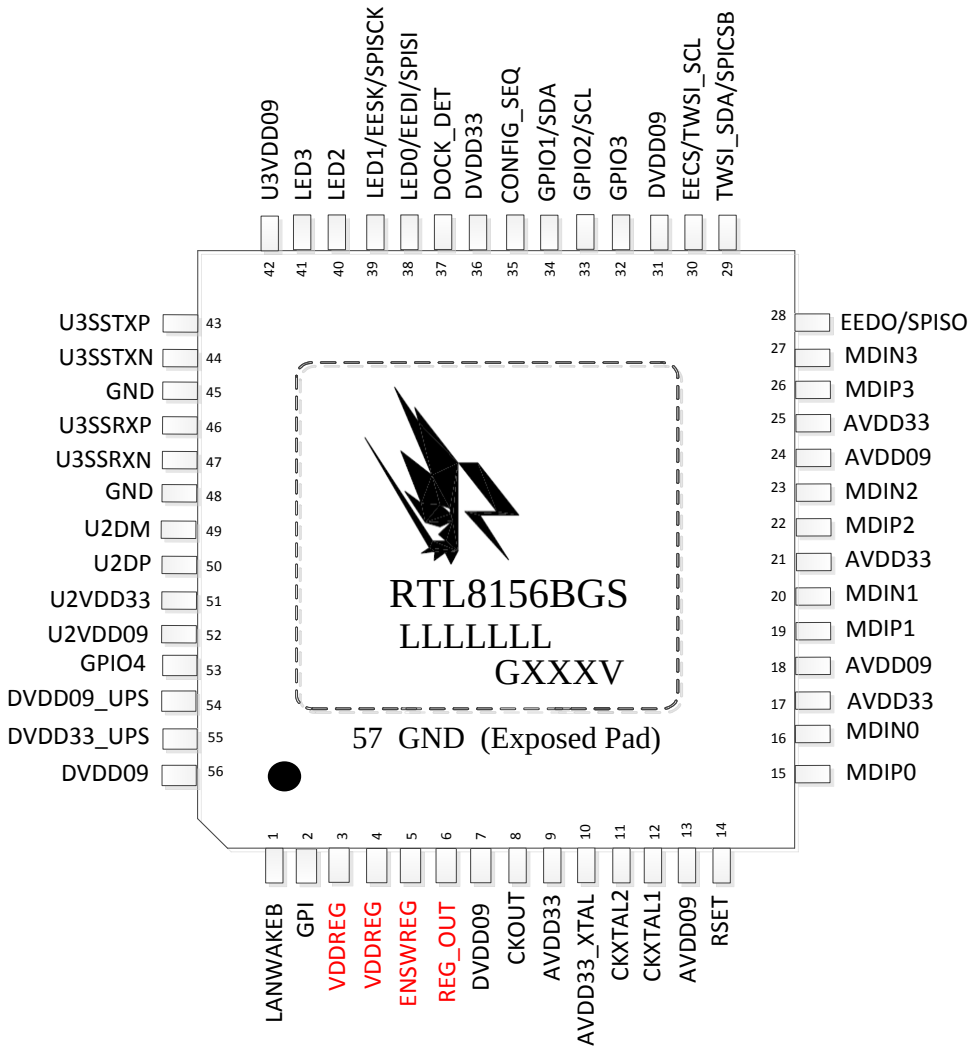


Figure 1. RTL8156BGS Pin Assignments

4.2. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 1). The letter in the 'V' location indicates the IC version; a blank is used for version A.

4.3. RTL8156BG Pin Assignments

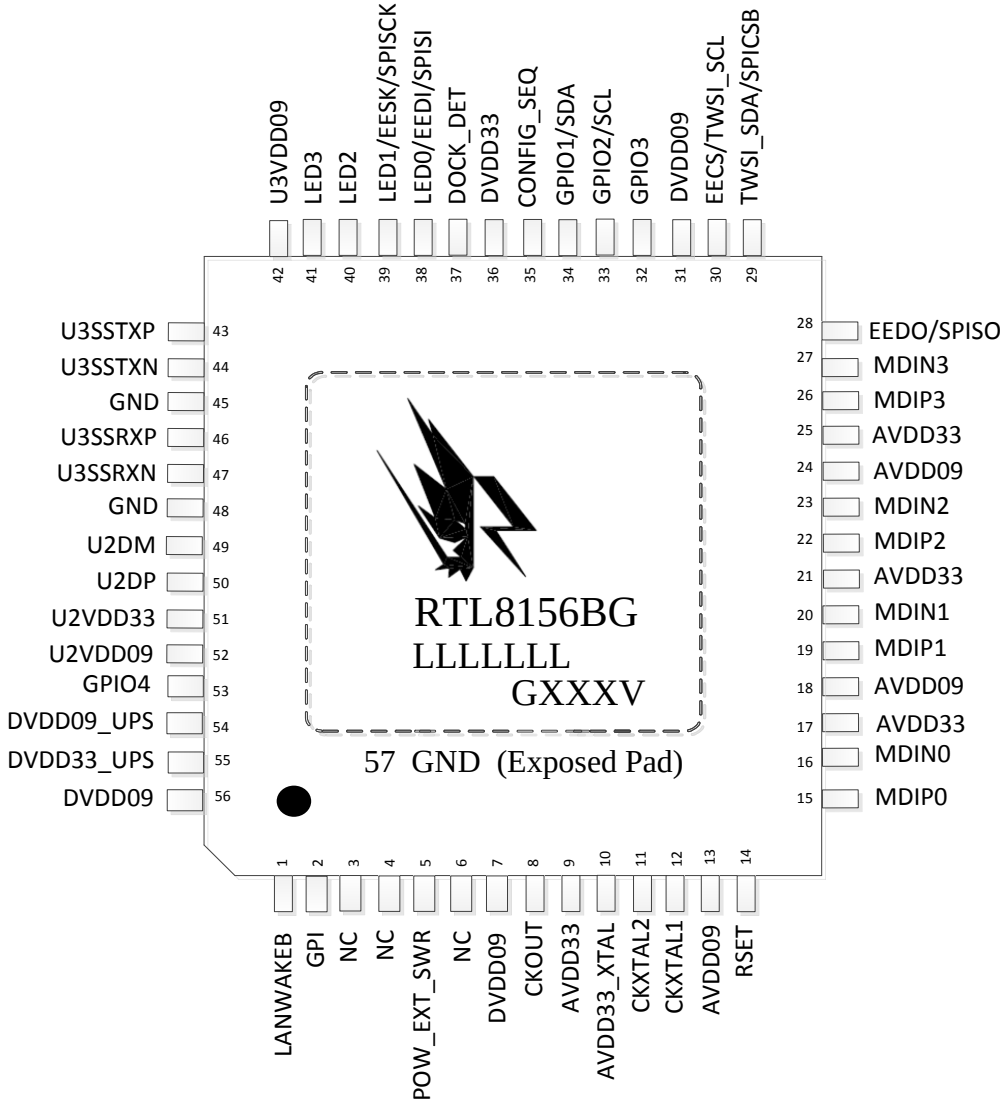


Figure 2. RTL8156BG Pin Assignments

4.4. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 2). The letter in the 'V' location indicates the IC version; a blank is used for version A.

5. Pin Descriptions

The signal type codes below are used in the following tables:

I: Input

O: Output

P: Power

D: Open drain

5.1. Power Management Pin

Table 1. Power Management Pin

Symbol	Type	Pin No	Description
LANWAKEB	D	1	Power Management Event Output Pin (Open drain, active low).

5.2. SPI (Serial Peripheral Interface) Flash Pins

Table 2. SPI Flash Pins

Symbol	Type	Pin No	Description
SPICSB	O	29	SPI Flash Chip Select.
SPISO	I	28	Input from SPI Flash Serial Data Output Pin.
SPISI	O	38	Output to SPI Flash Serial Data Input Pin.
SPISCK	O	39	SPI Flash Serial Data Clock.

Note 1. Pin 29 is a shared pin with TWSI_SDA
Note 2. Pin 28 is a shared pin with EEDO
Note 3. Pin 38 is a shared pin with LED0/EEDI
Note 4. Pin 39 is a shared pin with LED1/EESK

5.3. EEPROM Pins

Table 3. EEPROM Pins

Symbol	Type	Pin No	Description
EESK	O	39	Serial Data Clock.
EEDI	IO	38	EEDI: Output to serial data input pin of EEPROM.
EEDO	I	28	Input from Serial Data Output Pin of EEPROM.
EECS/TWSI_SCL	O	30	EECS: EEPROM Chip Select. SCL: Clock interface for EEPROM.

Note 1. Pin 39 is a shared pin with LED1/SPISCK
Note 2. Pin 38 is a shared pin with LED0/SPISI
Note 3. Pin 28 is a shared pin with SPISO
Note 4. Pin 30 is a shared pin with TWSI_SCL

5.4. TWSI Interface Pins

Table 4. TWSI Pins

Symbol	Type	Pin No	Description
TWSI_SCL	O	30	Serial Data Clock for TWSI.
TWSI_SDA	IO	29	SDA: Data interface for TWSI.

Note 1. Pin 29 is a shared pin with SPICSB
Note 2. Pin 30 is a shared pin with EECS

5.5. I2C Interface Pins

Table 5. I2C Pins

Symbol	Type	Pin No	Description
SDA	IO	34	Data interface.
SCL	I	33	Clock interface.

Note 1. Only Slave Mode is supported.
Note 2. Pin 34 is a shared pin with GPIO1
Note 3. Pin 33 is a shared pin with GPIO2

5.6. Transceiver Interface Pins

Table 6. Transceiver Interface Pins

Symbol	Type	Pin No	Description
MDIP0	IO	15	In MDI mode, this is the first pair in 2.5GBASE-T, 1000BASE-T, i.e., the BI_DA+/- pair, and is the transmit pair in 10BASE-Te and 100BASE-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10BASE-Te and 100BASE-TX. If MDI swap is set, this pair is BI_DD+/- in MDI mode and is BI_DC+/- in MDI crossover mode.
MDIN0	IO	16	
MDIP1	IO	19	In MDI mode, this is the second pair in 2.5GBASE-T, 1000BASE-T, i.e., the BI_DB+/- pair, and is the receive pair in 10BASE-Te and 100BASE-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10BASE-Te and 100BASE-TX. If MDI swap is set, this pair is BI_DC+/- in MDI mode and is BI_DD+/- in MDI crossover mode.
MDIN1	IO	20	
MDIP2	IO	22	In MDI mode, this is the third pair in 2.5GBASE-T, 1000BASE-T, i.e., the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair. If MDI swap is set, this pair is BI_DB+/- in MDI mode and is BI_DA+/- in MDI crossover mode.
MDIN2	IO	23	
MDIP3	IO	26	In MDI mode, this is the fourth pair in 2.5GBASE-T, 1000BASE-T, i.e., the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair. If MDI swap is set, this pair is BI_DA+/- in MDI mode and is BI_DB+/- in MDI crossover mode.
MDIN3	IO	27	

Note: BI_DA+/-, BI_DB+/-, BI_DC+/-, BI_DD+/- means the logical wire-pairs as described in IEEE 802.3 standard. The MDI swap register option should be set in accordance with ICM/XFMR pin definition.

5.7. Clock Pins

Table 7. Clock Pins

Symbol	Type	Pin No	Description
CKXTAL1	I	12	Input of 25MHz Clock Reference. If a 25MHz oscillator is used, connect CKXTAL1 pin to the oscillator's output.
CKXTAL2	O	11	Output of 25MHz Clock Reference. Keep this pin floating if an external 25MHz oscillator drives the CKXTAL1 pin.

5.8. Regulator and Reference Pins

Table 8. Regulator and Reference Pins

Symbol	Type	Pin No	Description
REG_OUT	O	6	For RTL8156BGS Built-in Switching Regulator 0.95V Output
VDDREG	P	3,4	For RTL8156BGS Digital 3.3V Power Supply for built-in Switching Regulator
RSET	I	14	Reference (External Resistor Reference).

5.9. LED Pins

Table 9. LED Pins

Symbol	Type	Pin No	Description
LED0	O	38	See Section 6.2 Customizable LED Configuration, page 13 for Details.
LED1	O	39	
LED2	O	40	
LED3	O	41	

Note 1. In prelink suspend state (power-on and USB disconnected), LED pin output voltage depends on both Ethernet connection (link up/link down) and LED setting (high active/low active).
In LAN disabled state, LED pin output voltage is 0V.
Note 2. Pin 38 is a shared pin with EEDI/SPISI;
Note 3. Pin 39 is a shared pin with EESK/SPISCK;

5.10. Power and Ground Pins

Table 10. Power and Ground Pins

Symbol	Type	Pin No	Description
AVDD33	P	9, 17, 21, 25	Analog 3.3V Power Supply.
AVD33_XTAL	P	10	Analog Power 3.3V Supply for XTAL.
AVDD09	P	13, 18, 24	Analog 0.95V Power Supply.
U3VDD09	P	42	USB 3.0 0.95V Power Supply.
U2VDD33	P	51	USB 2.0 3.3V Power Supply.
U2VDD09	P	52	USB 2.0 0.95V Power Supply.
DVDD33	P	36	Digital 3.3V Power Supply.
DVDD09	P	7, 31, 56	Digital 0.95V Power Supply.
DVDD33_UPS	P	55	Digital 3.3V Uninterruptible Power Supply.
DVDD09_UPS	P	54	Internal Power Saving LDO 0.95V to supply internal circuits. Do NOT connect this pin to other 0.95V power domains. Keep it isolated. A decoupling capacitor is required for this pin.
GND	P	45,48,57	Ground. Exposed Pad (57 pin is E-Pad) is Analog and Digital Ground.

Note: Refer to the most updated schematic circuit for correct configuration.

5.11. GPIO Pins

Table 11. GPIO Pins

Symbol	Type	Pin No	Description
GPI	IO	2	General Purpose Input/Output Pin (3.3V compatible input, 3.3V output only). 1. Power Saving Feature: Output pin (Active Low) 2. Link OK Feature: Output pin (Active High) 3. LAN Disable mode: Input Pin (Active Low)
GPIO4	IO	53	General Purpose Input/Output Pin.
GPIO3	IO	32	General Purpose Input/Output Pin.
GPIO2	IO	33	General Purpose Input/Output Pin.
GPIO1	IO	34	General Purpose Input/Output Pin.

Note 1. Pin 34 is a shared pin with SDA;
Note 2. Pin 33 is a shared pin with SCL;

5.12. USB Interface Pins

Table 12. USB Interface Pins

Symbol	Type	Pin No	Description
U3SSRXP	I	46	USB 3.0 Super-Speed Receive Differential Pair.
U3SSRXN	I	47	USB 3.0 Super-Speed Receive Differential Pair.
U3SSTXP	O	43	USB 3.0 Super-Speed Transmit Differential Pair.
U3SSTXN	O	44	USB 3.0 Super-Speed Transmit Differential Pair.
U2DP	IO	50	USB 2.0 Differential Signal Pair.
U2DM	IO	49	USB 2.0 Differential Signal Pair.

5.13. Other Pins

Table 13. Other Pins

Symbol	Type	Pin No	Description
POW_EXT_SWR	O	5	For RTL8156BG Enable external switch regulator to generate power of 0.95V. **1: Enable 0: Disable.**
ENSWREG	I	5	For RTL8156BGS Enable built-in switch regulator to generate power of 0.95V. **1: Enable 0: Disable.**
NC		3, 4, 6	Not Connected Pin (only RTL8156BG)
DOCK_DET	I	37	Monitor connection of DOCK and Platform (High: Connected, Low: Disconnected).
CONFIG_SEQ	I	35	Modified USB Configuration Sequence High: Set configuration = 1 RTK Set configuration = 2 CDC-NCM Set configuration = 3 CDC-ECM Low: Set configuration = 1 CDC-NCM Set configuration = 2 CDC-ECM Set configuration = 3 RTK

Note 1. Pins 3, 4, and 6 are NC pins when IC package is RTL8156BG.

6. Functional Description

6.1. USB Interface

The SIE (Serial Interface Engine) employs a robust hardwired USB protocol implementation so that the entire USB interface operation can be done without firmware intervention. For all three types of End Points (Bulk-In, Bulk-Out, and Interrupt-In), appropriate responses and handshake signals are generated by the SIE. The SIE analog transceiver complies fully with driver and receiver characteristics defined in USB Specification Rev. 3.2 Gen1.

6.1.1. USB Configurations

The RTL8156BG(S) supports three networking configurations; ECM (Ethernet Control Model) configuration, NCM (Network Control Model) configuration and in-house configuration. The ECM configuration is compatible with CDC-ECM, and is a general Ethernet networking model that enables network communication without installing additional vendor specific drivers. The NCM configuration is compatible with CDC-NCM, and supports high-speed network transmission without installing additional vendor specific drivers. The in-house configuration requires a vendor specific driver to support enhanced features and optimized performance.

6.1.2. Endpoint 0

All USB devices support a common access mechanism for accessing information through this control pipe. Associated with the control pipe at endpoint 0 is the information required to completely describe the USB device. This pipe also provides the register read and write to the RTL8156BG(S).

6.1.3. Endpoint 1 Bulk-In

The RTL8156BG(S) transfers Ethernet Rx packets to the host via this endpoint. The maximum Bulk-In packet size is 1024 bytes. If the Ethernet packet is larger than 1024 bytes, the RTL8156BG(S) splits the Ethernet packet into multiple USB packets.

6.1.4. Endpoint 2 Bulk-Out

The host sends Ethernet Tx packets to the RTL8156BG(S) via this endpoint. The maximum Bulk-Out packet size is 1024 bytes. If the Ethernet packet is larger than 1024 bytes, the host will send the Ethernet packet in multiple USB packets.

6.1.5. Endpoint 3 Interrupt-In

The Interrupt Endpoint (EP3) can be used to poll the current ALDPS state, EEE capability, TX/RX flow control enable, Connection Speed, Duplex mode, and link status of the RTL8156BG(S).

6.2. Customizable LED Configuration

The RTL8156BG(S) supports customizable LED operation modes via control registers. An individual control register for each LED, and a global feature control register are provided to support customized LED signals, which are described in Table 14 & Table 15.

Table 14. Customized LEDs

LEDSEL	LINK				ACT/Full	High/Low Active Control
	Link 10M	Link 100M	Link 1000M	Link 2500M		
LED 0	LED0-Bit 0	LED0-Bit 1	LED0-Bit 3	LED0-Bit 5	LED0-Bit 9	LED0-Bit 12
LED 1	LED1-Bit 0	LED1-Bit 1	LED1-Bit 3	LED1-Bit 5	LED1-Bit 9	LED1-Bit 12
LED 2	LED2-Bit 0	LED2-Bit 1	LED2-Bit 3	LED2-Bit 5	LED2-Bit 9	LED2-Bit 12
LED 3	LED3-Bit 0	LED3-Bit 1	LED3-Bit 3	LED3-Bit 5	LED3-Bit 9	LED3-Bit 12

Table 15. LED Feature Control

Feature Control	LED0-Bit 12	LED1-Bit 12	LED2-Bit 12	LED3-Bit 12	LED Option Table
0	LED0 Low Active	LED1 Low Active	LED2 Low Active	LED3 Low Active	Indicates Option 1 of Table 18 is selected
1	LED0 High Active	LED1 High Active	LED2 High Active	LED3 High Active	Indicates Option 2 of Table 18 is selected

The RTL8156BG(S) supports two special modes: LED OFF Mode and Fixed LED Mode. In LED OFF Mode all LED pins output become floating (power saving). The Fixed LED Mode is shown in see Table 16.

Table 16. Fixed LED Mode

LED0	LED1	LED2
ACT	LINK	Full Duplex + Collision
Transmit	LINK	Receive

The normal mode is set as shown in Table 17 and Table 18.

Table 17. LED Feature Control-2

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Option 1 (see Table 18): Selected Speed LINK+ Selected Speed ACT Option 2 (see Table 18): Selected Speed LINK+ All Speed ACT

Table 18. LED Option 1 & Option 2 Settings

Link Bit				Active Bit	Description		
10	100	1000	2500		Link	Option 1 LED Activity	Option 2 LED Activity
0	0	0	0	0	LED Off		
0	0	0	0	1	-	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}	Act_{10}+Act_{100}+ Act_{1000}+Act_{2500}
0	0	0	1	0	$Link_{2500}$	-	-
0	0	0	1	1	$Link_{2500}$	Act_{2500}	Act_{10}+Act_{100}+ Act_{1000}+Act_{2500}
0	0	1	0	0	$Link_{1000}$	-	-
0	0	1	0	1	$Link_{1000}$	Act_{1000}	Act_{10}+Act_{100}+ Act_{1000}+Act_{2500}
0	0	1	1	0	$Link_{1000}$+$Link_{2500}$	-	-
0	0	1	1	1	$Link_{1000}$+$Link_{2500}$	Act_{1000}+Act_{2500}	Act_{10}+Act_{100}+ Act_{1000}+Act_{2500}
0	1	0	0	0	$Link_{100}$	-	-
0	1	0	0	1	$Link_{100}$	Act_{100}	Act_{10}+Act_{100}+ Act_{1000}+Act_{2500}
0	1	0	1	0	$Link_{100}$+$Link_{2500}$	-	-
0	1	0	1	1	$Link_{100}$+$Link_{2500}$	Act_{100}+Act_{2500}	Act_{10}+Act_{100}+Act_{1000} +Act_{2500}
0	1	1	0	0	$Link_{100}$+$Link_{1000}$	-	-
0	1	1	0	1	$Link_{100}$+$Link_{1000}$	Act_{100}+Act_{1000}	Act_{10}+Act_{100}+Act_{1000} +Act_{2500}
0	1	1	1	0	$Link_{100}$+$Link_{1000}$+ $Link_{2500}$	-	-
0	1	1	1	1	$Link_{100}$+$Link_{1000}$+ $Link_{2500}$	Act_{100}+Act_{1000}+Act_{2500}	Act_{10}+Act_{100}+Act_{1000} +Act_{2500}
1	0	0	0	0	$Link_{10}$	-	-
1	0	0	0	1	$Link_{10}$	Act_{10}	Act_{10}+Act_{100}+Act_{1000} +Act_{2500}
1	0	0	1	0	$Link_{10}$+$Link_{2500}$	-	-
1	0	0	1	1	$Link_{10}$+$Link_{2500}$	Act_{10}+Act_{2500}	Act_{10}+Act_{100}+Act_{1000} +Act_{2500}
1	0	1	0	0	$Link_{10}$+$Link_{1000}$	-	-
1	0	1	0	1	$Link_{10}$+$Link_{1000}$	Act_{10}+Act_{1000}	Act_{10}+Act_{100}+Act_{1000} +Act_{2500}
1	0	1	1	0	$Link_{10}$+$Link_{1000}$+ $Link_{2500}$	-	-
1	0	1	1	1	$Link_{10}$+$Link_{1000}$+ $Link_{2500}$	Act_{10}+Act_{1000}+Act_{2500}	Act_{10}+Act_{100}+Act_{1000} +Act_{2500}
1	1	0	0	0	$Link_{10}$+$Link_{100}$	-	-
1	1	0	0	1	$Link_{10}$+$Link_{100}$	Act_{10}+Act_{100}	Act_{10}+Act_{100}+Act_{1000} +Act_{2500}
1	1	0	1	0	$Link_{10}$+$Link_{100}$+ $Link_{2500}$	-	-

Link Bit				Active Bit	Description		
10	100	1000	2500		Link	Option 1 LED Activity	Option 2 LED Activity
1	1	0	1	1	$Link_{10}$+$Link_{100}$+ $Link_{2500}$	Act_{10}+Act_{100}+Act_{2500}	Act_{10}+Act_{100}+Act_{1000} +Act_{2500}
1	1	1	0	0	$Link_{10}$+$Link_{100}$+ $Link_{1000}$	-	-
1	1	1	0	1	$Link_{10}$+$Link_{100}$+ $Link_{1000}$	Act_{10}+Act_{100}+Act_{1000}	Act_{10}+Act_{100}+Act_{1000} +Act_{2500}
1	1	1	1	0	$Link_{10}$+$Link_{100}$+ $Link_{1000}$+$Link_{2500}$	-	-
1	1	1	1	1	$Link_{10}$+$Link_{100}$+ $Link_{1000}$+$Link_{2500}$	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}	Act_{10}+Act_{100}+Act_{1000} +Act_{2500}

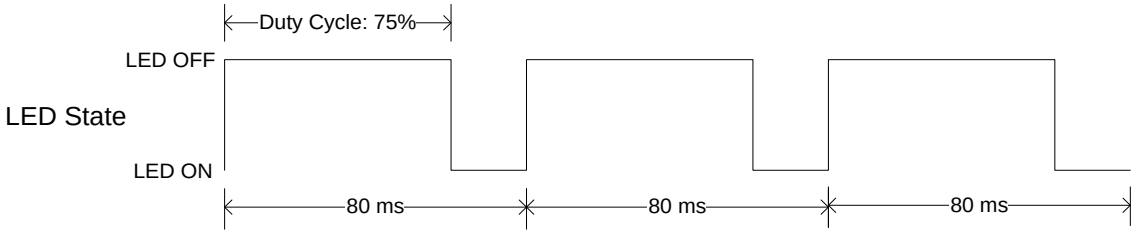
Note:
Act_{10} = LED blinking when Ethernet packets transmitted/received at 10Mbps.
Act_{100} = LED blinking when Ethernet packets transmitted/received at 100Mbps.
Act_{1000} = LED blinking when Ethernet packets transmitted/received at 1000Mbps.
Act_{2500} = LED blinking when Ethernet packets transmitted/received at 2500Mbps.
$Link_{10}$ = LED lit when Ethernet connection established at 10Mbps.
$Link_{100}$ = LED lit when Ethernet connection established at 100Mbps.
$Link_{1000}$ = LED lit when Ethernet connection established at 1000Mbps.
$Link_{2500}$ = LED lit when Ethernet connection established at 2500Mbps.

6.2.1. LED Blinking Frequency Control

The RTL8156BG(S) supports LED blinking frequency control via OCP address DD88h to control the user's LED blinking frequency and duty cycle (see Table 19). If the b_freq[1:0] set as 0x2 and the b_duty_cycle[1:0] set as 0x3, the LED blinking frequency is 80ms and the duty cycle is 75%. The LED State is shown in Figure 3.

Table 19. LED Blinking Frequency Control (OCP Register Offset 0xDD88)

Bit	RW	Description
b_freq[1:0]	RW	LED Blinking Frequency 0: 240ms 1: 160ms (Default) 2: 80ms 3: Link Speed Dependent
b_duty_cycle[1:0]	RW	LED Blinking Duty Cycle 0: 12.5% 1: 25% 2: 50% (Default) 3: 75%



Note: Assume the LED is in low active.

Figure 3. LED Blinking Frequency Example

6.3. PHY Transceiver

6.3.1. PHY Transmitter

XGMII (2500Mbps) Mode

The RTL8156BG(S)'s PCS layer receives data bytes from the MAC through the XGMII interface and performs LDPC encoding to enhance error correction performance. After LDPC framing, each 4 bits are grouped to a PAM16 symbol though a gray code mapping scheme. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT.5e cable at 200MBaud/s through a D/A converter.

GMII (1000Mbps) Mode

The RTL8156BG(S)'s PCS layer receives data bytes from the MAC through the GMII interface and performs the generation of continuous code-groups through 4D-PAM5 coding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. The NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

MII (10Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

6.3.2. PHY Receiver

XGMII (2500Mbps) Mode

Received bits from the media are first passed through the on-chip sophisticated hybrid circuit to eliminate the transmitted signal interference from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, such as adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, RFI cancellation, deskew, and PAM16 decoding. Each 2048-bit-wide data is passed through a LDPC decoder and is sent to the XGMII interface. The Rx MAC retrieves the packet data and sends it to the Rx Buffer Manager.

GMII (1000Mbps) Mode

Input signals from the media pass through the sophisticated on-chip hybrid circuit to separate the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the receive MII/GMII interface and sends it to the RX Buffer Manager.

MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

6.3.3. Link-Down Power Saving Mode

The RTL8156BG(S) implements link-down power saving; greatly cutting power consumption when the network cable is disconnected. The RTL8156BG(S) automatically enters link down power saving mode 3 seconds after the cable is disconnected from it. Once it enters link down power saving mode, it transmits normal link pulses on its TX pins and continues to monitor the RX pins to detect incoming signals. After it detects an incoming signal, it wakes up from link down power saving mode and operates in normal mode according to the result of the connection.

6.3.4. Next Page

If 1000BASE-T mode is advertised, three additional Next Pages (1000BASE-T Message Page, Unformatted Page 1, and Unformatted Page 2) are automatically exchanged between the two link partners. Users can set PHY MMD7.0x10.15 to 1 to manually exchange extra Next Pages via MMD7.0x16 and MMD7.0x19 as defined in IEEE 802.3 standard.

To advertise 2.5GBASE-T capability, both link partners, sharing the same link medium, should engage in XNP (Extended Next Page) exchange. NBASE-T OUI tagged page exchange would be further needed if NBASE-T capability is to be advertised. Users can set PHY MMD7.0x0.13 to 1 to manually exchange extra Extended Next Pages via MMD7.0x16 ~MMD7.0x1B as defined in the IEEE 802.3 standard.

6.4. EEPROM/TWSI Interface

Both 3-wire and TWSI EEPROM interfaces are supported. The 3-wire interface utilizes a 93C46/93C56/93C66, which is a 1K-bit/2K-bit/4K-bit, respectively, EEPROM. The EEPROM interface permits the RTL8156BG(S) to read from, and write data to, an external serial EEPROM device.

Use the PG tool to write eFUSE commands to select the EEPROM 93C46/93C56/93C66 or TWSI function.

The RTL8156BG(S) will auto-load values from the eFUSE or EEPROM. If the EEPROM is not present and eFUSE auto-load is bypassed, the RTL8156BG(S) initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using bit-bang accesses via the 9346CR Register. The 3-Wire EEPROM interface consists of EESK, EECS, EEDO, and EEDI. The correct EEPROM (i.e., 93C46/93C56/93C66) must be used in order to ensure proper LAN function. The RTL8156BG(S) eFUSE supports at least 512 bytes.

Table 20. EEPROM Interface

EEPROM	Description
EECS	93C46/93C56/93C66 Chip Select
EESK	Serial Data Clock for EEPROM
EEDI	Output to Serial Data Input Pin of EEPROM
EEDO	Input from Serial Data Output Pin of EEPROM

Table 20. TWSI Interface

EEPROM	Description
TWSI_SCL	Serial Data Clock for TWSI
TWSI_SDA	SDA: Data interface for TWSI

Table 21. eFUSE Autoload for TWSI/EEPROM

eFUSE Autoload Command	EEPROM Mode
0x20 0xDC 0x00 0x00 0x20 0xDC 0x06 0x01	3-wire EEPROM 93C56/93C66
0x20 0xDC 0x00 0x00 0x20 0xDC 0x06 0x00	3-wire EEPROM 93C46
0x20 0xDC 0x00 0x01	TWSI Mode

Note: [eFUSE Autoload Command] means using the PG Tool to write the \eFUSE command to change the mode.

6.5. SPI (Serial Peripheral Interface) Flash

The RTL8156BG(S) supports the attachment of 32MB (maximum) external Serial Peripheral Interface (SPI) Flash. The SPI flash provides 32MB bytes of serial reprogrammable flash memory.

SPI Flash is enabled by the RTL8156BG(S) through the Chip Select pin, and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). The SPI flash utilizes an 8-bit instruction register. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low transition.

Compared to a parallel bus interface, the Serial Peripheral Interface provides simpler wiring and much less interaction (crosstalk) among the conductors in the cable. This minimizes the number of conductors, pins, and the IC package size, reducing the cost of making, assembling, and testing the electronics.

Table 22. SPI Flash Interface

SPI Flash	Description
SPISO	Input Data Bus.
SPISI	Output Data Bus.
SPISCK	SPI Flash Serial Data Clock.
SPICSB	SPI Flash Chip Select.

Note: For more technical information, refer to the SPI Flash application note.

6.6. I2C Interface

The RTL8156BG(S) supports the standard I2C interface. The I2C bus uses two wires: serial data (SDA) and serial clock (SCL). All I2C master and slave devices are connected with only those two wires. Each device can be a transmitter, a receiver or both. In order to communicate with specific device, each slave device must have an address which is unique on the bus. I2C master devices (usually microcontrollers) don't need an address since no other (slave) device sends commands to the master.

The RTL8156BG(S) works as a slave device, which listens to the bus and is addressed by the master. The master device generates clock, starts communication, sends I2C commands, and stops communication.

Table 23. I2C Interface

I2C	Description
SDA	Serial data line.
SCL	Serial clock line.

The RTL8156BG(S)'s MACID can be modified via the I2C function using a special protocol called 'OTP code'. The 'OTP code' includes a Slave address and is a 36Bytes command (Figure 4).

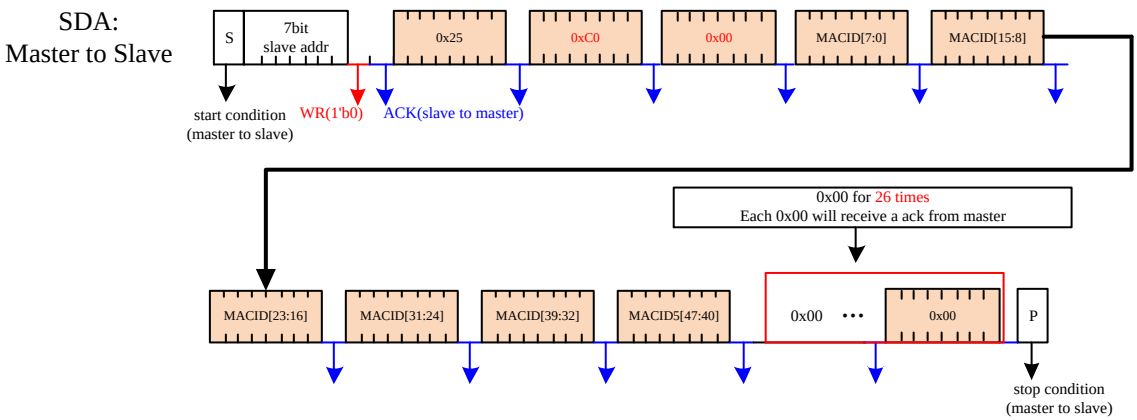


Figure 4. MACID Modified via the I2C Function

6.7. Power Management

The RTL8156BG(S) is compatible with ACPI (Rev 1.0, 1.0b, 2.0), Network Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-directed Power Management (OSPM) environment.

The RTL8156BG(S) can monitor the network for a Wake-Up Frame or a Magic Packet, and notify the system via the USB interface when such a packet or event occurs. The system is then restored to a normal state to process incoming jobs.

When the RTL8156BG(S) is in power saving mode:

- The RTL8156BG(S) monitors the network for wake-up events such as a Magic Packet and Wake-Up Frame in order to wake-up the system
- The RTL8156BG(S) will not receive any packets into the RX on-chip buffer
- USB transactions are stopped

Magic Packet Wake-Up occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8156BG(S), e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8156BG(S) adapter.
- The received Magic Packet does not contain a CRC error.
- The Magic Packet pattern matches, i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wake-Up Frame event occurs only when the following conditions are met:

- The destination address of the received Wake-Up Frame is acceptable to the RTL8156BG(S), e.g., a broadcast, multicast, or unicast address to the current RTL8156BG(S) adapter.
- The received Wake-Up Frame does not contain a CRC error.
- The received Wake-Up Frame matches the Wake-Up Frame pattern given by the local machine's OS. Or, the RTL8156BG(S) is configured to allow direct packet wake-up, e.g., a broadcast, multicast, or unicast network packet.

Note: The RTL8156BG(S) supports 32-set wake-up frames.

6.8. Link Power Management (LPM)

The RTL8156BG(S) supports full USB Link Power Management (LPM). It provides an efficient way for the host to manage power consumption. The four power management states are L0, L1, L2 in USB 2.0.

USB 3.0 also defines four power management states: U0, U1, U2, and U3. If host and hub support LPM, the host/hub can put the device into a low power state. The RTL8156BG(S) will deactivate some of its circuits to reduce power consumption in the low power state, and go back to full functionality in active state.

Refer to http://www.usb.org/developers/docs/

6.9. Wake Packet Detection (WPD)

The RTL8156BG(S) supports Microsoft Wake Packet Detection (WPD) to provide Wake-Up Frame information to the OS, e.g., PatternID, OriginalPacketSize, SavedPacketSize, SavedPacketOffset, etc. WPD helps prevent unwanted/unauthorized wake-up of a sleeping computer.

Refer to the Microsoft Wake Packet Detection (WPD) Interface Specification for details (http://msdn.microsoft.com/en-us/library/hh440160(v=vs.85).aspx).

6.10. 'RealWoW!' (Wake-On-WAN) Technology

The RTL8156BG(S) supports Realtek 'RealWoW!' technology that allows the RTL8156BG(S) to send keep-alive packets to the Wake Server when the PC is in sleeping mode. Realtek 'RealWoW!' can pass wake-up packets through a NAT (Network Address Translation) device. This feature allows PCs to reduce power consumption by remaining in low power sleeping state until needed.

Users can login into the Wake Server via the Internet to wake the selected sleeping PC. Registration of Account information to the Wake Server is required on first time use.

6.11. Energy Efficient Ethernet (EEE)

The RTL8156BG(S) supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps, 100Mbps, and 1000Mbps, and IEEE 802.3bz-2016 EEE at 2.5GBASE-T. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode most of the circuits are disabled, however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported and to select the best set of parameters common to both devices.

Refer to http://www.ieee802.org/3/az/index.html for more details.

6.12. Radio Frequency Interference (RFI)

Among the many possible causes of interference when connecting two PHYs, Radio Frequency Interference (RFI) is the most common. The RTL8156BG(S) is equipped with RFI cancellation ability. This allows the RTL8156BG(S) to maintain data transmission in noisy environments and makes it immune to RFI strikes.

6.13. Fast Retrain (FR)

The RTL8156BG(S) supports IEEE 802.3 Fast Retrain in 2.5GBASE-T. It provides a protocol to quickly converge a Tx/Rx equalizer at both ends of the link when it is needed. If local Rx SNR is bad, or the link partner requests FR, FR is launched and it attempts to train the Tx/Rx equalizer before the link goes down. This protocol can reduce link up/link down wait time and provide better upper layer protocols and applications. This protocol is especially useful when the RTL8156BG(S) is used in noisy environments or a when short time RFI happens to strike the link.

The RTL8156BG(S) supports CISCO Negotiated Fast Retrain, which aims for the same target as IEEE FR but extends some timing specifications to allow better weak link recovery.

6.14. Thermal Detect

When the RTL8156BG(S) operates in 2.5G and 2.5G Lite mode, built-in smart thermal management can sense the IC temperature, regardless of the surrounding environment temperature. To prevent damage, the RTL8156BG(S) depends on the current link speed to mask 2.5G or 2.5G Lite capability and notify the system when an over temperature event occurs. With the aid of this thermal detect mechanism, the RTL8156BG(S) can provide smart power management. The goal of smart power management is to give a balance between power consumption and Ethernet transceiver performance. This feature is especially useful when the RTL8156BG(S) is deployed in thermally constrained environments.

6.15. MDI Swap

Different ICM (Integrated Combo Magnetics) might have opposite PHY sides to the cable side definition. To accommodate this, the RTL8156BG(S) supports MDI swap to prevent PCB trace routing from crossing.

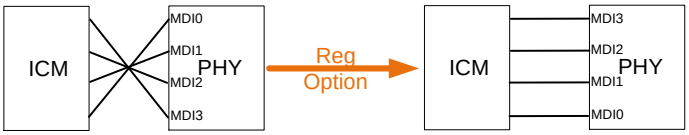


Figure 5. MDI Reverse

6.16. LAN Disable Mode

The RTL8156BG(S) supports the 'LAN Disable Mode' that can use an external signal to control whether the NIC is enabled or disabled. When the RTL8156BG(S) is in LAN disable mode, the RTL8156BG(S) enters power saving state.

6.17. Always On Always Connected/Modern Standby

The RTL8156BG(S) supports Microsoft's AOAC (Always On Always Connected)/Modern Standby model. The AOAC/Modern Standby platform can enter the system state 'Connected Standby/Modern Standby' and allow the RTL8156BG(S) to enter a low-power state. The RTL8156BG(S) will maintain Layer 2 connectivity and generate a wake signal when one of the following conditions is satisfied:

- Link status becomes 'connected'
- Link status becomes 'disconnected'
- Receives a magic packet
- Receives a wakeup frame (pattern match)

6.18. Lite Mode

6.18.1. Giga Lite

The RTL8156BG(S) supports Giga Lite (500M) mode that allows two link partners that both support 1000BASE-T and Giga Lite mode to transmit at 500Mbps data rate if only two pairs (AB pairs) can be detected in the CAT.5 UTP cable. This feature is a Realtek proprietary feature and it conforms to the 802.3az-2010 (EEE) specification.

6.18.2. 2.5G Lite

The RTL8156BG(S) supports 2.5G Lite (1000M) mode that allows two link partners that both support 2.5GBASE-T and 2.5G Lite mode to transmit at 1000Mbps data rate if only two pairs (AB pairs) can be detected in the CAT.5e UTP cable. This feature is a Realtek proprietary feature and it conforms to the 802.3az-2010 (EEE) specification.

6.19. Green Ethernet (1000M/100Mbps Mode Only)

6.19.1. Cable Length Power Saving

In 1000M/100Mbps mode the RTL8156BG(S) provides dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides intermediate performance with minimum power consumption.

6.20. Crossover Detection and Auto-Correction

Ethernet needs a crossover mechanism between both link partners to cross the transmit signal to the receiver when the medium is twisted-pair cable. Crossover Detection & Auto-Correction Configuration eliminates the need for crossover cables between devices, such as two computers connected to each other with an Ethernet cable. The basic concept is to assume the initial default setting is MDI mode, and then check the link status. If no link is established after a certain time, change to MDI Crossover mode and repeat the process until a link is established. An 11-bit pseudo-random timer is applied to decide the mode change time interval.

Crossover Detection & Auto-Correction is not a part of the Auto-Negotiation process, but it utilizes the process to exchange the MDI/MDI Crossover configuration. If the RTL8156BG(S) is configured to only operate in 100BASE-TX or only in 10BASE-Te mode, then Auto-Negotiation is disabled only if the Crossover Detection & Auto-Correction function is also disabled. If Crossover Detection & Auto-Correction are enabled, then Auto-Negotiation is enabled and the RTL8156BG(S) advertises only 100BASE-TX mode or 10BASE-Te mode. If the speed of operation is configured manually and Auto-Negotiation is still enabled because the Crossover Detection & Auto-Correction function is enabled, then the duplex advertised is as follows:

1. If it is set to half duplex, then only half duplex is advertised.

2. If it is set to full duplex, then both full and half duplex are advertised.

6.21. Polarity Correction

The RTL8156BG(S) automatically corrects polarity errors on the receive pairs in 2.5GBASE-T, 1000BASE-T and 10BASE-Te modes. In 100BASE-TX mode polarity is irrelevant. In 1000BASE-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. Users may manually do polarity correction via the register option if polarity is known beforehand. The polarity becomes unlocked only when the receiver loses lock.

In 10BASE-Te mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10BASE-Te link is up. The polarity becomes unlocked when the link is down.

6.22. Driver Auto-Install Mode

Realtek's auto-install mode solves the problem of a lack of network connection or CD-ROM hardware on some recent computer platforms making driver installation difficult. With auto-install mode configured, attach the driver-less RTL8156BG(S) to a system. The RTL8156BG(S) will disconnect, switch to auto-install mode, and reconnect as a USB CD-ROM with a programmed driver installer. The driver will install itself and the RTL8156BG(S) will switch back to USB NIC mode after installation.

The mechanism for identifying driver existence has inherent limitations due to the USB protocol. The general USB enumeration flow consists of Set Address and Set Configuration control transfer. The Set Address is done by the operating system; the Set Configuration is done by the device driver (see note1).

The RTL8156BG(S) detects the driver existence by starting the auto-install mode timer when it receives Set Address. If the driver exists, the driver will do Set Configuration within a short time (millisecond scale after the driver has loaded). The timer will stop upon receipt of Set Configuration. If a driver is not present, the device will not receive Set Configuration and the timer will timeout (default timeout value is 8 seconds).

Note 1: For Linux and OSX, the USB SetConfig is handled by the system USB framework (USB host controller driver and/or USB bus driver); this behavior cannot trigger RTL8156BG(S) switching to auto-install mode. As a result, the RTL8156BG(S) supports auto-install mode in Windows only.
For Linux, Realtek supports a built-in in-house/ECM/NCM driver.
For OSX, Realtek supports a built-in ECM/NCM driver; users can also install an in-house driver.

Note 2: For more technical information, refer to the auto-install mode application note.

6.23. Dock Detect

The Dock detect pin permits the RTL8156BG(S) to connect to the dock platform to monitor the VBUS. The RTL8156BG(S) can Self-Reset through the Dock Detect function to ensure compatibility with those dock platforms that monitor the connection of dock and platform.

6.24. Configuration Sequence

This pin can control a device's bConfigurationValue sequence from a Configuration descriptor when the NIC device is enumerating with a host.

High: RTK's bConfigurationValue=1, NCM's bConfigurationValue=2, ECM's bConfigurationValue=3

Low: NCM's bConfigurationValue=1, ECM's bConfigurationValue=2, RTK's bConfigurationValue=3

This function allows users to use the PG Tool to enable the configuration sequence.

Table 24. Configuration Sequence

GPIO_Config_Seq_Enable	Configuration Sequence	
CONFIG_SEQ: High	Set configuration = 1 Set configuration = 2 Set configuration = 3	RTK CDC-NCM CDC-ECM
CONFIG_SEQ :Low	Set configuration = 1 Set configuration = 2 Set configuration = 3	CDC-NCM CDC-ECM RTK

7. Switching Regulator (RTL8156BGS Only)

The RTL8156BGS incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. Note that the switching regulator 0.95V output pin (REG_OUT) must be connected only to DVDD09, AVDD09, U3VDD09, and U2VDD09 (do not provide this power source to other devices).

Note: Refer to the separate RTL8156BGS layout guide for details.

8. Power Sequence

8.1. Power Sequence Parameters

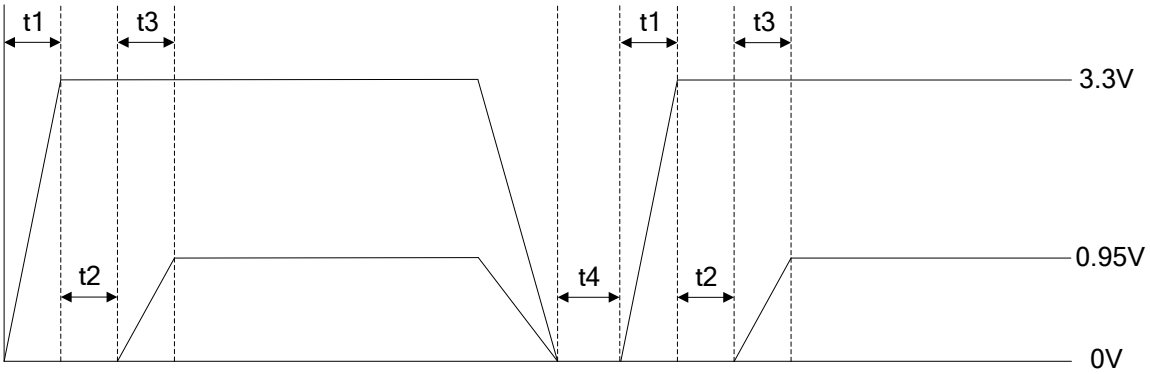


Figure 6. Power Sequence

Table 25. Power Sequence Parameters

Symbol	Description	Min	Typical	Max	Unit
t1	3.3V Rise Time	0.5	1	10	ms
t2	SWR Enable Interval	(Note 1)	-	-	ms
t3	0.95V Rise Time for RTL8156BG	0.5	-	2.2	ms
	0.95V Rise Time for RTL8156BGS	-	-	2.2	ms
t4	On/Off Interval	50	-	-	ms

Note 1: t2 should be well controlled by the RTL8156BG(S)

Note 2: The loosest counting of t1 would be the rising time required for the power rail to output from 0V to 90% of target voltage.

9. Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 26. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
AVDD33, AVDD33_XTAL, DVDD33, DVDD33_UPS, U2VDD33	Supply Voltage 3.3V	-0.3	3.63	V
AVDD09, DVDD09, U2VDD09, U3VDD09	Supply Voltage 0.95V	-0.2	1.05	V
N/A	Storage Temperature	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

9.2. Recommended Operating Conditions

Table 27. Recommended Operating Conditions

Description	Supply Voltage	Minimum	Typical	Maximum	Unit
Supply Voltage	3.3	3.14	3.3	3.46	V
	0.95	0.92	0.95	0.98	V
Ambient Operating Temperature T_A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

9.3. Electrostatic Discharge Performance

Table 28. Electrostatic Discharge Performance

Test Item	Results
HBM ESD	All Pins: ｜3.5KV｜
MM ESD	All Pins: ｜100V｜
CDM ESD	All Pins: ｜200V｜
Latch Up	I/O Pin: 100mA Power Pin: 1.5xVDD

9.4. Crystal Requirements

Table 29. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F_{ref} Tolerance (Note 1)	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=0°C~70°C.	-50	-	+50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	70	Ω
DL	Drive Level.	-	-	0.5	mW
V_{ih}_CKXTAL	Crystal Output High Level	1.4	-	-	V
V_{il}_CKXTAL	Crystal Output Low Level	-	-	0.4	V
Operating Temperature Range	-	-40	-	85	°C
Package (Note 2)	-	-	SMD	-	-

Note 1: F_{ref} Tolerance +/- 50ppm including effects of aging of the first year, external crystal capacitors, and PCB layout.
Note 2: An SMD type crystal MUST be used for the RTL215B/RTL8125BS.
Note 3: An SMD type crystal MUST be used for the RTL8156BG(S).

9.5. Oscillator Requirements

Table 30. Oscillator Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25	-	MHz
Frequency Tolerance	Ta=0°C~70°C	-50	-	50	ppm
Duty Cycle	-	40	-	60	%
RMS Jitter [1]	10kHz~20MHz	-	-	2	ps
V_{ih}	-	1.4		-	V
V_{il}	-	-	-	0.4	V
Rise Time (10%~90%)	-	-	-	11	ns
Fall Time (10%~90%)	-	-	-	11	ns
Operating Temperature Range	-	-40	-	125	°C

Note: Frequency Tolerance +/- 50ppm including effects of aging of the first year, external crystal capacitors, and PCB layout. The phase noise of 25MHz clock input should be at least that as shown in Figure 7.

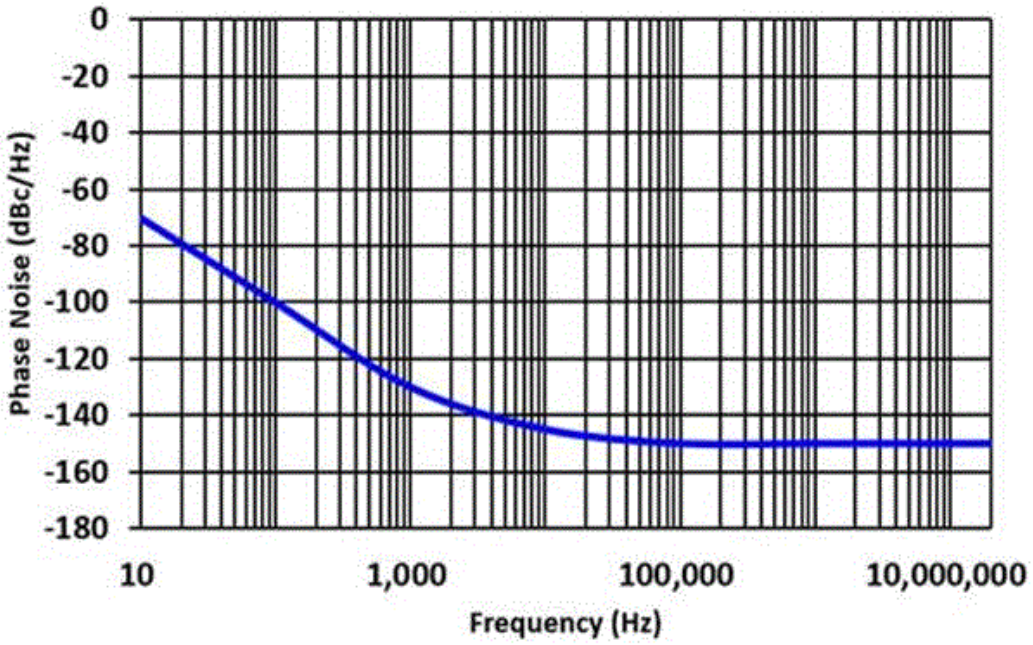


Figure 7. Phase Noise

9.6. Environmental Characteristics

Table 31. Environmental Characteristics

Parameter	Range	Units
Storage Temperature	-55 ~ +125	°C
Ambient Operating Temperature	0 ~ 70	°C
Moisture Sensitivity Level (MSL)	Level 3	N/A

9.7. DC Characteristics

Table 32. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
AVDD33, AVDD33_XTAL, DVDD33, DVDD33_UPS, U2VDD33	3.3V Supply Voltage	-	3.14	3.3	3.46	V
AVDD09, DVDD09, U2VDD09, U3VDD09	0.95V Supply Voltage	-	0.92	0.95	0.98	V
Voh	Minimum High Level Output Voltage	3.3V domain	2.4	3.3	VDD33 + 0.3	V
Vol	Maximum Low Level Output Voltage	3.3V domain	-0.3	0	0.4	V
Vih	Minimum High Level Input Voltage	3.3V domain	2.0	3.3	-	V
Vil	Maximum Low Level Input Voltage	3.3V domain	-	0	0.8	V
Iin	Input Current	Vin=VDD33 or GND	0	-	0.5	µA
Icc	Maximum Operating Supply Current *(Note 2)*	3.3V domain	-	88	92	mA
		0.95V domain	-	364	650	

Note 1: Pins not mentioned above remain at 3.3V.

Note 2: The Maximum Operating Supply Current was measured under the specific conditions of 100 meter Cat5e, +5% of all power rails and Ta = 85°C. This will help the PCB designer have a better understanding of each power rail budget.

9.8. Reflow Profile Recommendations

Table 33. Reflow Profile Recommendations

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Minimum Preheat Temperature (T_{smin})	100°C	150°C
Maximum Preheat Temperature (T_{smax})	150°C	200°C
Preheat Time (t_S) from T_{smin} to T_{smax}	60~120 seconds	60~120 seconds
Ramp-Up Rate (T_L to T_p)	3°C/second max.	3°C/second max.
Liquidus Temperature (T_L)	183°C	217°C
Time (t_L) Maintained above T_L	60~150 seconds	60~150 seconds
Peak Package Body Temperature (T_p)	235°C	260°C
Time $(t_p)^2$ within 5°C of Peak T_P	20 seconds	20 seconds
Ramp-Down Rate (T_p to T_L)	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature (T_p)	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to the topside of the package, measured on the package body surface.

Note 2: Tolerance for Tp is defined as a supplier's minimum and a user's maximum.

Note 3: Reference document: IPC/JEDEC J-STD-020D.1.

9.9. AC Characteristics

9.9.1. TWSI EEPROM Interface Timing

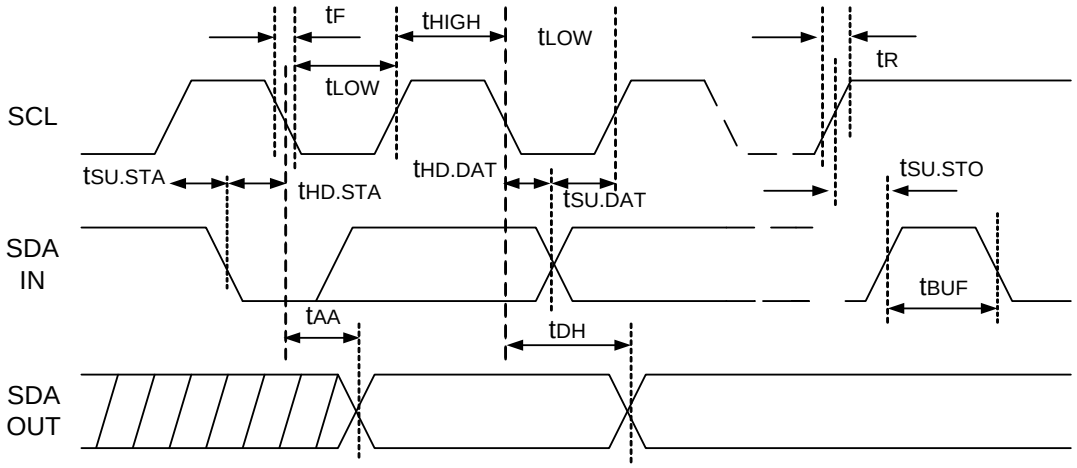


Figure 8. TWSI EEPROM Interface Timing-1

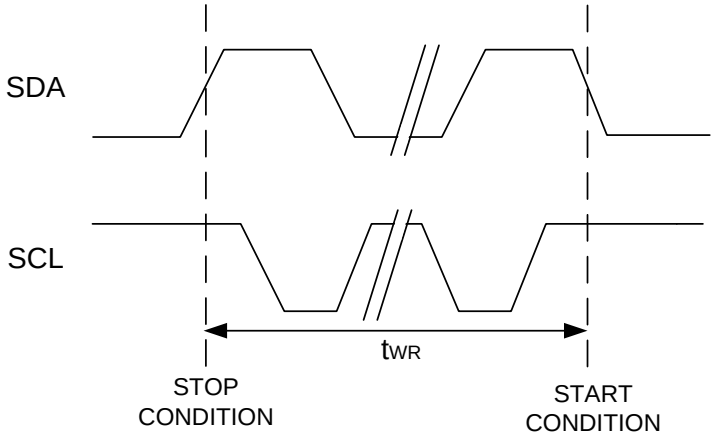


Figure 9. TWSI EEPROM Interface Timing-2

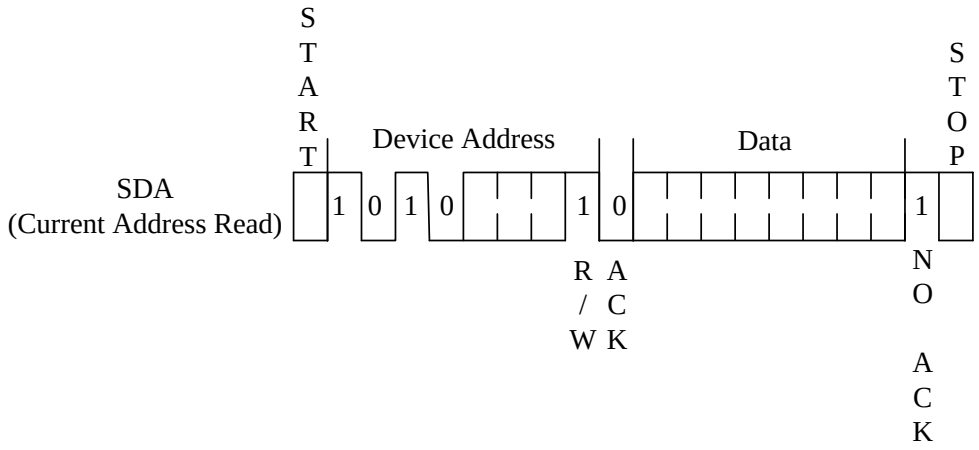


Figure 10. TWSI EEPROM Interface Timing-3

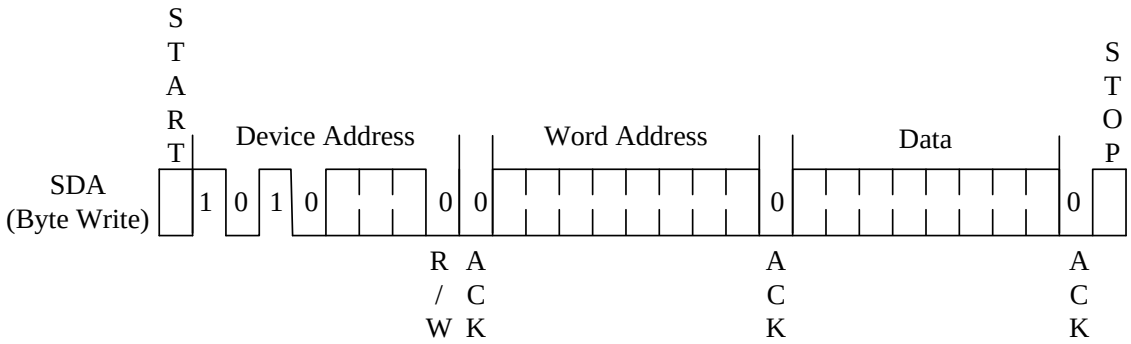


Figure 11. TWSI EEPROM Interface Timing-4

Table 34. TWSI EEPROM Access Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
t_{LOW}	Clock Pulse Width Low	512	-	8192	ns
t_{HIGH}	Clock Pulse Width High	512	-	8192	ns
t_{AA}	Clock Low to DO Valid	-	504	514	ns
t_{BUF}	Time the Bus Must be Free before a New Transmission Can Start	-	-	-	ns
$t_{HD.STA}$	Start Hold Time	247	252	257	ns
$t_{SU.STA}$	Start Setup Time	247	252	257	ns
$t_{HD.DAT}$	DI Hold Time	247	252	257	ns
$t_{SU.DAT}$	DI Setup Time	247	252	257	ns
t_R	Input Rise Time	-	-	-	ns
t_F	Input Fall Time	-	-	-	ns
$t_{SU.STO}$	Stop Setup Time	494	504	514	ns
t_{DH}	DO Hold Time	494	504	514	ns
t_{WR}	Write Cycle Time	5.88	6	6.12	ms

9.9.2. 3-Wire EEPROM Interface Timing

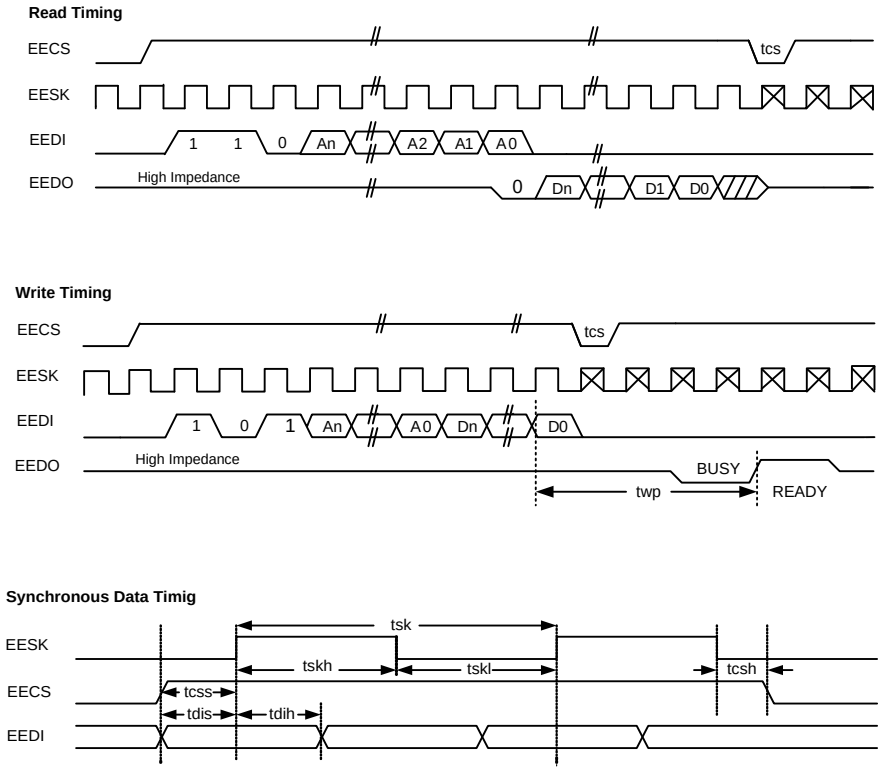


Figure 12. 3-Wire EEPROM Interface Timing

Table 35. 3-Wire EEPROM Access Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
tcs	Minimum CS Low Time	1024	4096	-	ns
tcss	CS Setup Time	512	512	-	ns
tcsh	CS Hold Time	-	0	-	ns
tskh	SK High Time	512	512	8192	ns
tskl	SK Low Time	512	512	8192	ns
tsk	SK Clock Cycle Time	1024	1024	16384	ns
tdis	DI Setup Time	512	512	-	ns
tdih	DI Hold Time	512	512	-	ns
twp	Write Cycle Time	-	6	10	ms

9.9.3. SPI Flash Commands

9.9.3.1 SPI Flash Commands

Table 36. SPI Flash Commands

Command	Operation Code	Action
WREN	06h	Write Enable
WRDI	04h	Write Disable
RDID	9Fh	Read Manufacturer and Product ID
RDSR	05h	Read Status Register
WRSR	01h	Write Status Register
Read	03h	Read
Page Program	02h	Page Program
Sector Erase (4K)	20h	Erase The Selected Sector
Block Erase (64K)	D8h	Erase The Selected Block
Chip Erase	60h or C7h	Erase Whole Chip

9.9.3.2 SPI Flash Command Sequence

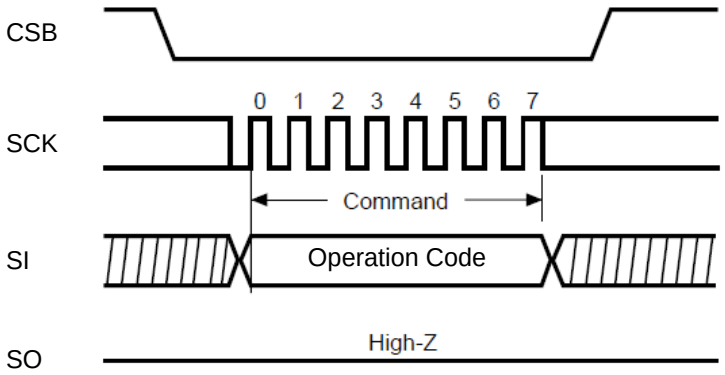


Figure 13. WREN/WRDI Command Sequence

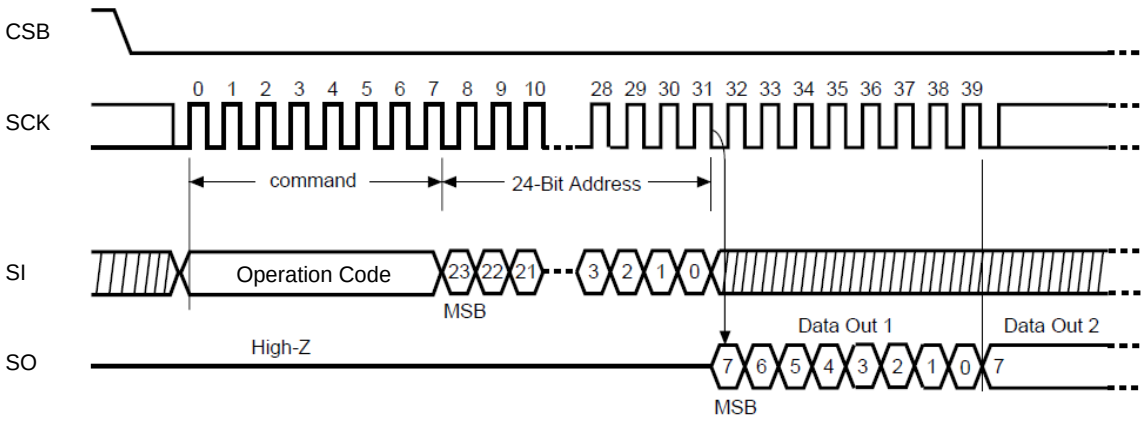


Figure 14. Read Command Sequence

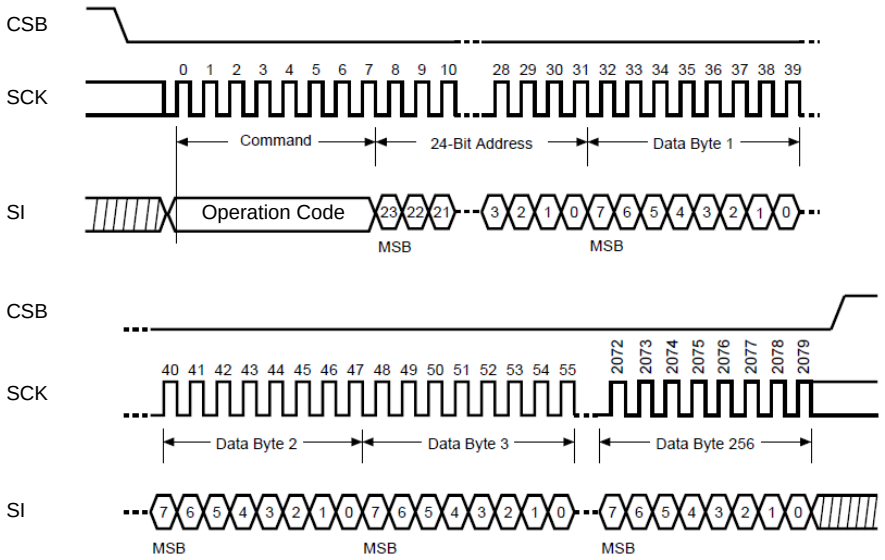


Figure 15. Page Program Command Sequence

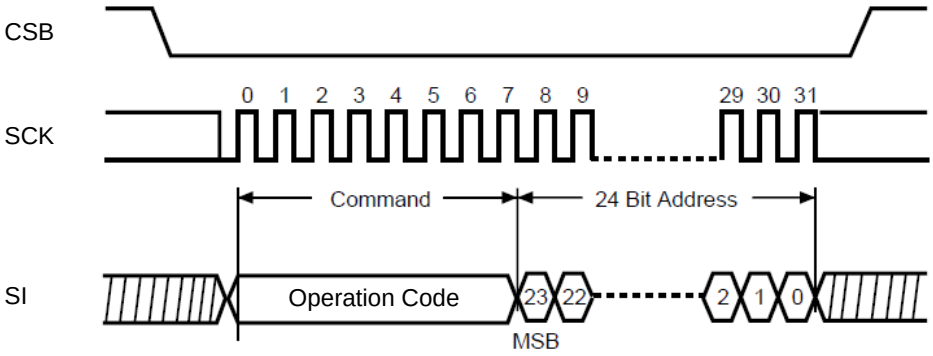


Figure 16. Sector/Block Erase Command Sequence

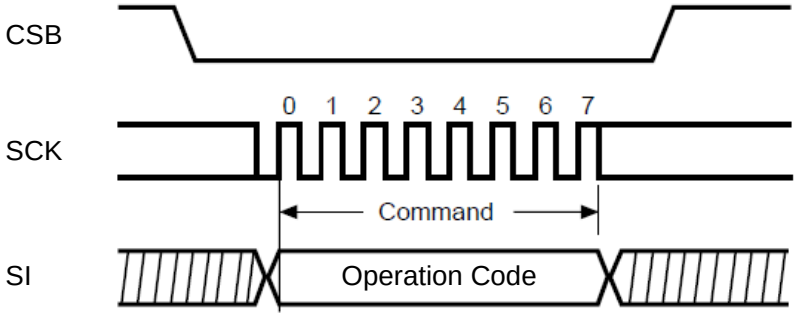
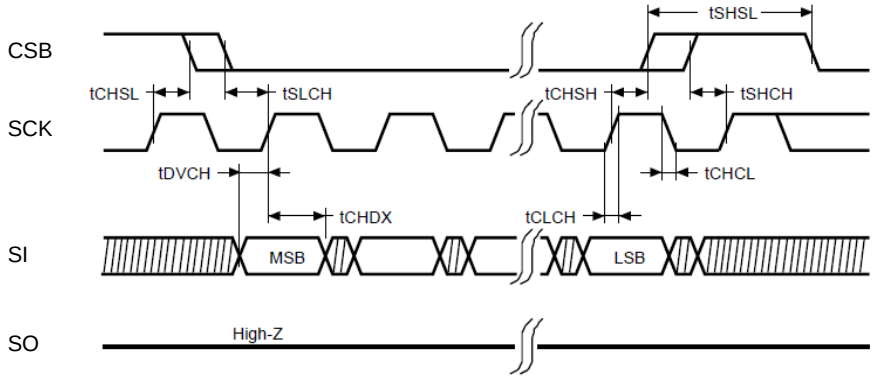


Figure 17. Chip Erase Command Sequence

9.9.4. SPI Flash Interface Timing

Write Timing



Read Timing

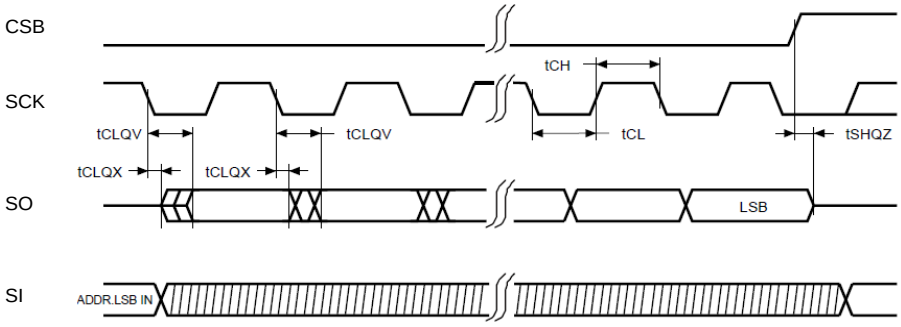


Figure 18. SPI Flash Interface Timing

Table 37. SPI Flash Access Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
fSCK	Clock Frequency for all instructions except Read data (fC)	DC	-	6	MHz
fRSCK	Clock Frequency for the READ instructions (fR)	DC	-	32	MHz
tCH	Clock High Time (fC)	128	-	-	ns
	Clock High Time (fR)	-	16	-	ns
tCL	Clock Low Time (fC)	40	-	-	ns
	Clock Low Time (fR)	-	16	-	ns
tCLCH	Clock Rise Time	0.1	-	-	V/ns
tCHCL	Clock Fall Time	0.1	-	-	V/ns
tDVCH	SI Setup Time	32	-	-	ns
tCHDX	SI Hold Time	96	-	-	ns
tSHQZ	SO Disable Time	-	-	-	ns
tCLQV	Clock Low to SO Valid	-	-	10	ns
tCLQX	SO Hold Time	0	-	-	ns

9.10. Thermal Characteristics

Table 38. Thermal Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
θ_{JA}	Junction-to-ambient thermal resistance $\theta_{JA} = (T_J - T_A)/P_H$	No air flow	-	19.06	-	°C/W
Ψ_{JT}	Junction-to-top-center thermal characterization parameter $\Psi_{JT} = (T_J - T_T)/P_H$	No air flow	-	0.28	-	°C/W

Note: T_J = junction temperature (°C), T_A = ambient temperature (°C), T_T = temperature on the top-center of the package (°C), P_H = total power dissipation (W).

The above thermal characteristics are based on customized PCB information, as shown in Table 39.

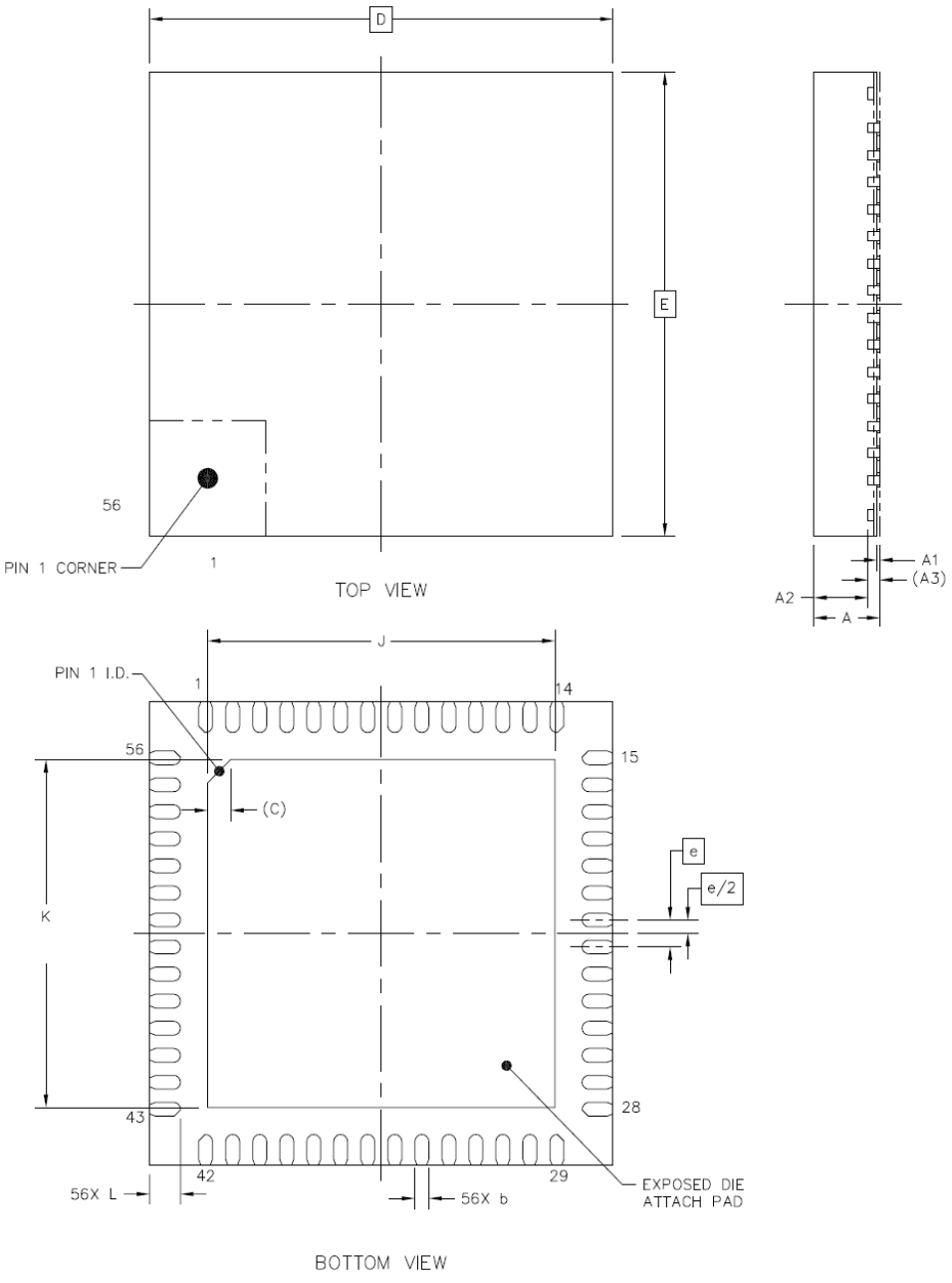
Table 39. PCB Information

PCB type	Customized PCB
PCB layers	4
PCB dimensions	119.9 mm X 56 mm
Cu coverage (%)	L1: 61% L2: 85% L3: 83% L4: 80%
External heat sink	No

Ψ_{JT} is better than θ_{JA} and θ_{JC} (Junction-to-case thermal resistance) on the estimation of the junction temperature (T_J). The temperature on the top-center of the package (T_T) is effected by not only the ambient temperature (T_A), but also the PCB conditions.

P_H includes the power dissipation from the top, bottom and sides of the package, but θ_{JC} assumes that all the power is dissipated only from the top of the package. Thus, θ_{JC} is appropriate for the package attached with the external heat sink. In actual environment, Ψ_{JT} brings a closer value to the actual T_J by measuring T_T.

10. Mechanical Dimensions



10.1. Mechanical Dimensions Notes

Table 40. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.800	0.850	0.900	0.031	0.033	0.035
A_1	0.000	0.035	0.050	0.000	0.001	0.002
A_2	---	0.700	---	---	0.028	---
A_3		0.152REF			0.006REF	
b	0.130	0.180	0.230	0.005	0.007	0.009
D/E	5.90	6.00	6.10	0.232	0.236	0.240
J	4.400	4.500	4.600	0.173	0.177	0.181
K	4.400	4.500	4.600	0.173	0.177	0.181
e		0.350 BSC			0.0138 BSC	
c		0.3REF			0.012 REF	
L	0.350	0.400	0.450	0.0138	0.016	0.018
Tolerance Of Form And Position						
aaa		0.100			0.004	
bbb		0.100			0.004	
ccc		0.080			0.003	
ddd		0.100			0.004	
eee		0.100			0.004	

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: The Max/Min for REF and BSC are +/- 0.1 MILLIMETER (mm).

11. Ordering Information

Table 41. Ordering Information

Part Number	Package
RTL8156BG-CG	56-Pin QFN 'Green' Package
RTL8156BGS-CG	56-Pin QFN 'Green' Package (with Built-in switching regulator)

Note: See page 5 and page 6 for package ID information.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com