RTD2674S

LCD TV Controller

Revision 0.02

August 31, 2009

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Feature

Analog TV IF demodulator

- ✓ Support NTSC / PAL /SECAM IF demodulator

Analog TV Video decoder

- ✓ Support NTSC/PAL/SECAM decode :
  - NTSC-M, NTSC-443.
  - PAL-BDGHI, PAL-M, PAL-N, PAL-60, PAL-CN
  - SECAM.
- ✓ 3D comb filter for NTSC / PAL
- ✓ 2D/1D comb filter for NTSC/PAL and SECAM

Analog VBI Decoder

- ✓ CC : CC1, 2, 3 and4, Text 1, 2, 3 and 4, XDS (eXtension Data Service), V Chip
- ✓ CGMS : ETSI EN 300 294, ITU-R BT.119 method, IEC-61880 method, CC-XDS method
- ✓ WSS : ETSI EN 300 294, ITU-R BT.119 method, IEC-61880 method, CC-XDS method
- ✓ TT: Teletext 1.5/2.5 ETSI EN 300 706

ATV audio-in standard

- ✓ Supports multi-standard TV broadcasting includes : BTSC-Stereo, EIA-J(FM-FM) and FM Stereo A2 System
- ✓ NICAM 728 digital sound for B/G/L/I/D/K system

Analog RGB/YPbPr Input Interface

- ✓ Total 3x Analog inputs for YpbPr and VGA
- ✓ YPbPr input up to 1080p which is shared with VGA RGB input up to WUXGA
- ✓ Support Sync-On-Green(SOG) and Composite-Sync(CS) mode

Digital Video Input Interface

- ✓ 1x video-10 input is supported

HDMI 1.3 Compliant Digital Input Interface

- ✓ 2 x HDMI/DVI RX port with D-switch is supported
- ✓ Operation up to 3.4GHz
- ✓ High-Bandwidth Digital Content Protection (HDCP) 1.3
- ✓ Support CEC

Digital Video Output Interface

- ✓ Integrated 10-bit LVDS transmitter for VESA & JEIDA
- ✓ Support up to WUXGA 1920x1080p Full HD panel

Audio IO

- ✓ Two channel (Stereo) DAC support 32KHz, 44.1KHz, 48KHz, 88.2KHz, 96KHz, 176.4KHz, 192KHz sample rate
- ✓ Support 16-bit, 20-bit, 24-bit PCM data
- ✓ Support S/PDIF input/output for stereo PCM & non-PCM data
- ✓ 48KHz baseband ADC Sample rate
- ✓ SRS / BBE software post processing is supported

High-Quality Video Processor

- ✓ Color-Recover™III for video cross color reduction
- ✓ Clean-Picture™ III for spatial/temporal and Mosquito noise reduction
- ✓ Pixel-Composer™III for following feature:
  - Support 1080i / 480i / 576i de-interlacing
  - Inverse 3:2/2:2 pull-down for Film Mode detection
  - 3D Motion Adaptive De-interlace
  - Low Angel interpolation processing

Vivid-Color™

- ✓ Support YUV/YCrCb/YPrPb to RGB and sRGB matrix color-space conversion
- ✓ Support DLTI/DCTI video-quality improvement
- ✓ ICM for Color Manager
- ✓ Support Black/White Level Expansion
- ✓ Support 2D Y peaking filter and coring
- ✓ Support ACC
- ✓ sRGB compliance
- ✓ xvYCC support

Peripheral IO

- ✓ USB 2.0 Host ports with embedded PHY
- ✓ Support two 16550 UARTs, each has 16-byte FIFO.
- ✓ Support one IrDA Rx interface, which complies with NEC, SHARP, Sony SIRC protocol I, Philips RC-5 and 48-bit Panasonic protocol.
- ✓ Support 2 x I2C master/slave interfaces

Audio Decompression

- ✓ Support MPEG1 layer 1/2/3, LPCM and other formats

Picture Format

- ✓ HD JPEG decoding with unlimited resolution

MemoryInterface

- ✓ Support 1 x 16bit DDR SDRAM
- ✓ Support DDR memory up to 64M bytes
- ✓ memory access speed up to DDR SDRAM@250MHz
- ✓ Support external SPI flash up to 32MB

Power & Technology

- ✓ 3.3V/1.2V power supplier; 2.5V for DDR I/O interface
- ✓ LQFP216 package
- ✓ 27MHz crystal clock with embedded PLL

1.1 System Block Diagram

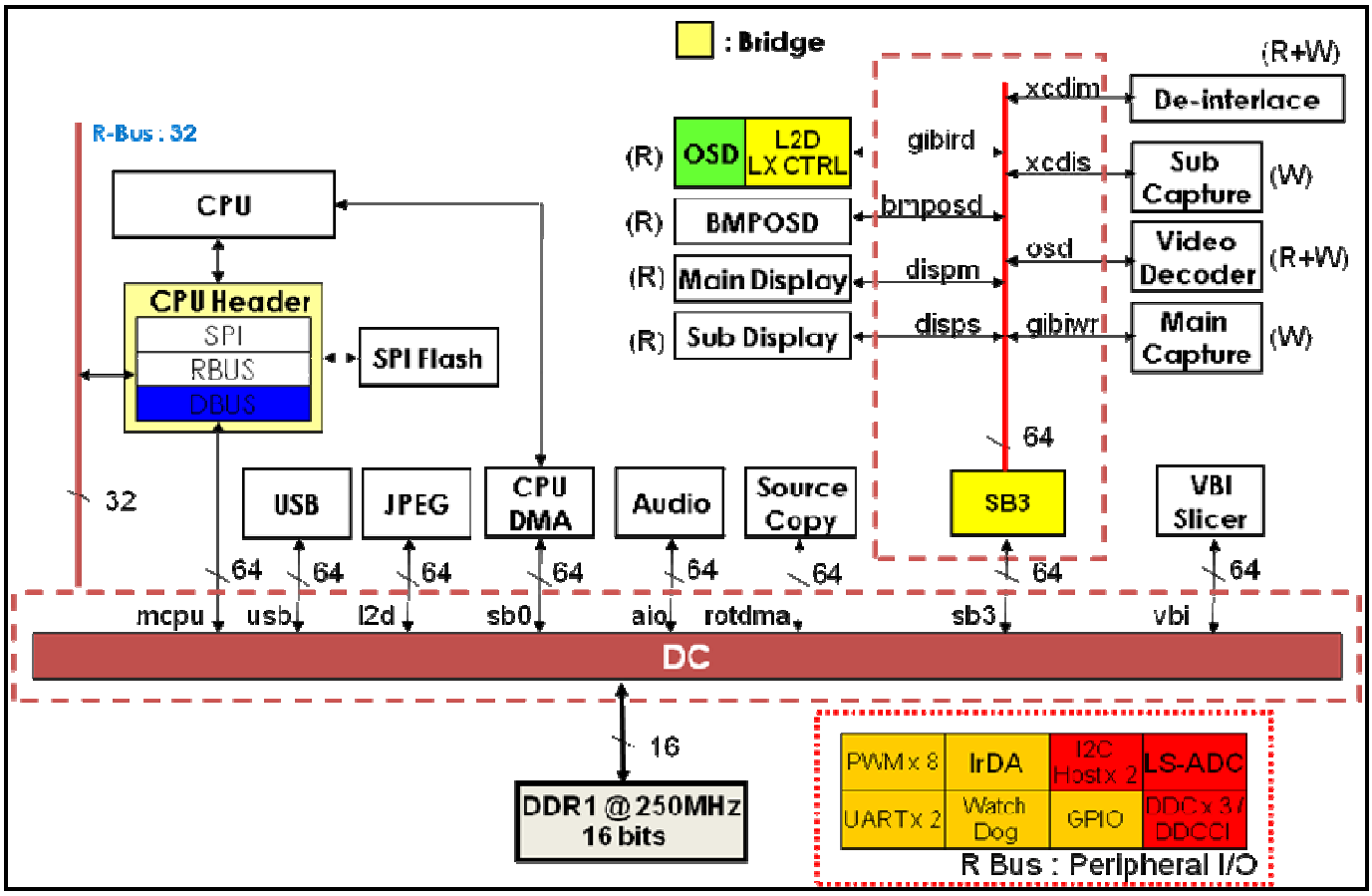
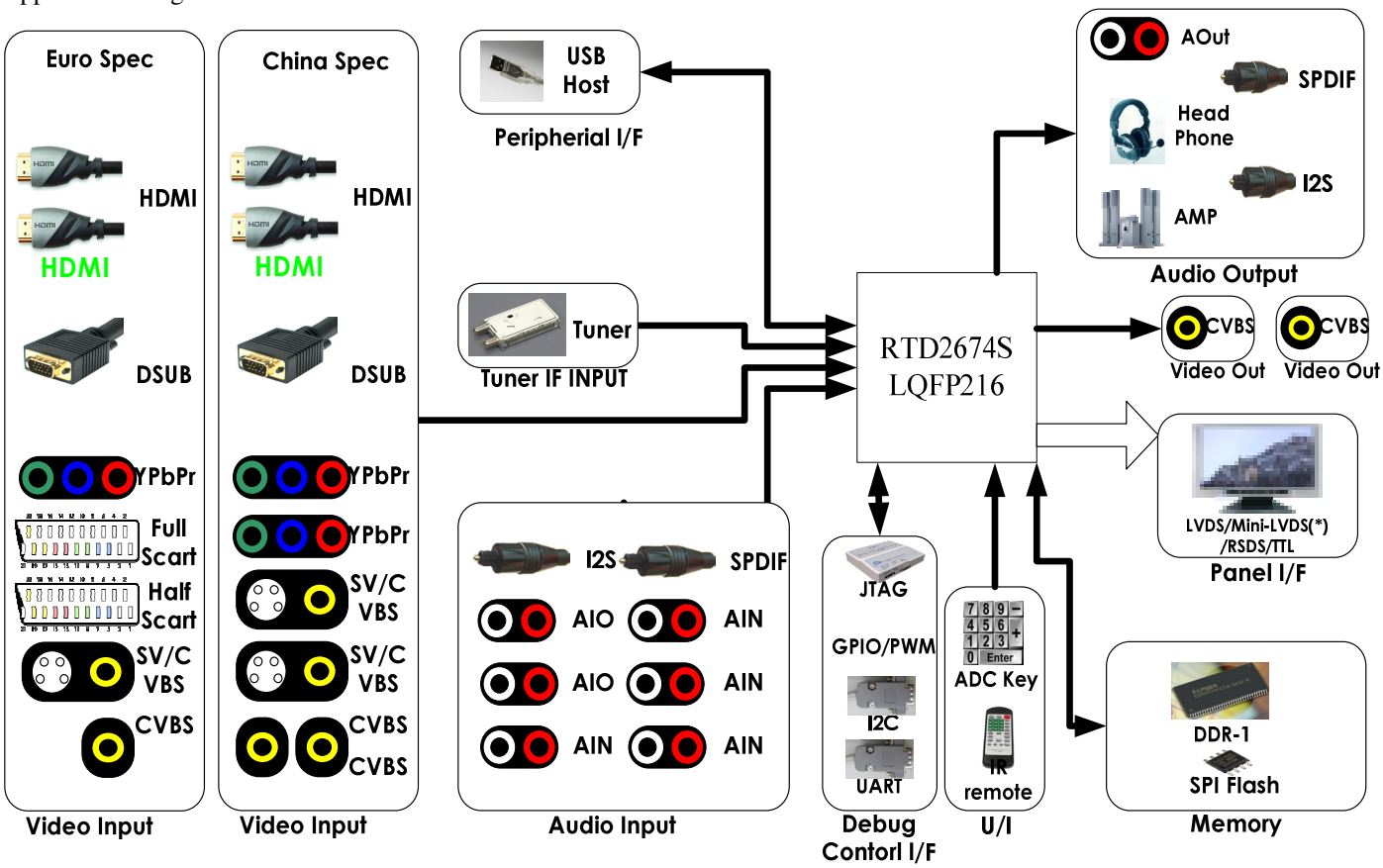


Figure 1 System Architecture

1.2 Application Diagram



(*) Need to Confirm with Panel Spec

1.3 Pin List

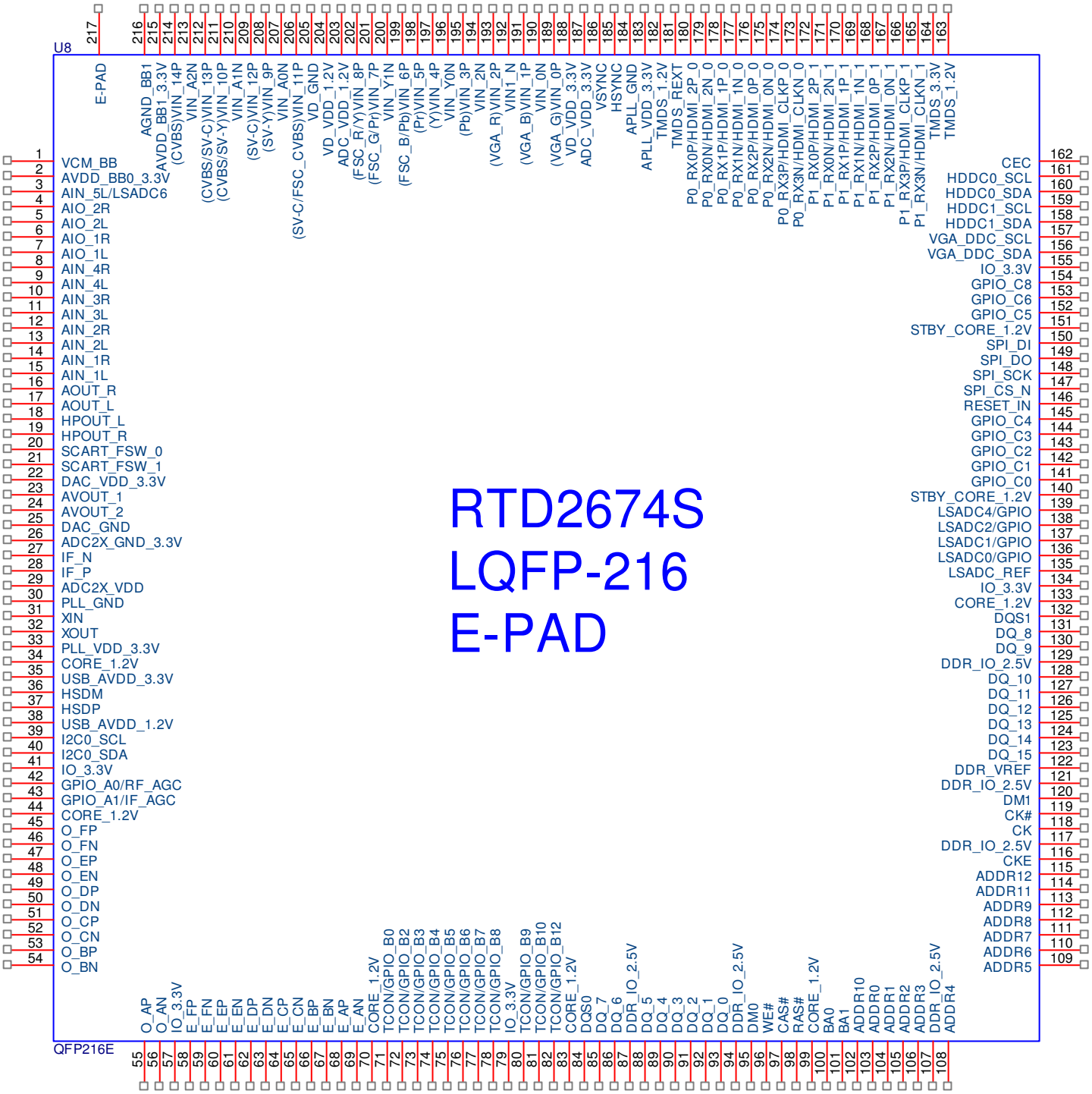


Table 1-1. RTD2674S Pin Assignments – Pin detail description

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

Pin No	Pin Name	Type	Description	Note
1	VCM_BB	AP	Analog Audio Common Voltage Reference	Connect 1uF to GND
2	AVDD_BB0	AP	Analog Baseband Power 3.3V	Analog 3.3V
3	AIN_5L/LSADC6	AI	Low Speed ADC input 6	
4	AIO_2R	AIO	Analog Audio input/output 2 (Right Channel)	
5	AIO_2L	AIO	Analog Audio input/output 2 (Left Channel)	
6	AIO_1R	AIO	Analog Audio input/output 1 (Right Channel)	
7	AIO_1L	AIO	Analog Audio input/output 1 (Left Channel)	
8	AIN_4R	AI	Analog Audio input 4 (Right Channel)	
9	AIN_4L	AI	Analog Audio input 4 (Left Channel)	
10	AIN_3R	AI	Analog Audio input 3 (Right Channel)	
11	AIN_3L	AI	Analog Audio input 3 (Left Channel)	
12	AIN_2R	AI	Analog Audio input 2 (Right Channel)	
13	AIN_2L	AI	Analog Audio input 2 (Left Channel)	
14	AIN_1R	AI	Analog Audio input 1 (Right Channel)	
15	AIN_1L	AI	Analog Audio input 1 (Left Channel)	
16	AOUT_R	AO	Analog Baseband Audio Out (Right Channel)	
17	AOUT_L	AO	Analog Baseband Audio Out (Left Channel)	
18	HPOUT_L	AO	Head Phone DAC output (Left Channel)	
19	HPOUT_R	AO	Head Phone DAC output (Right Channel)	
20	Scart_FSW_0	AIO	SCART RGB Fast Switch Input 0	
21	Scart_FSW_1	AIO	SCART RGB Fast Switch Input 1	
22	DAC_VDD_0	AP	Video DAC Power 3.3V	Analog 3.3V
23	AVOUT_1	AP	CVBS DAC output1	
24	AVOUT_2	AP	CVBS DAC output2	
25	DAC_GND_0	AP	Video DAC GND	
26	ADC2X_GND_1	AP	IFADC GND	
27	IF_N	AP	IF demod Negative input	
28	IF_P	AP	IF demod Postive input	
29	ADC2X_VDD_0	AP	IFADC power 3.3V	Analog 3.3V
30	PLL_GND_1	AP	XTAL PLL GND	
31	XIN	AP	27MHz Crystal Input	
32	XOUT	AP	27MHz Crystal Output	
33	PLL_VDD_0	AP	XTAL PLL power 3.3V	Analog 3.3V
34	Core_1.2V	DP	Core Power 1.2V	Digital 1.2V, Power Down@ Power saving
35	AVDD_1	AP	USB Power 3.3V	Analog 3.3V
36	HSDM_1	AP	USB HOST0 Data Negative	
37	HSDP_1	AP	USB HOST0 Data Postive	
38	LV_USB_1	AP	USB Power 1.2V	Analog 1.2V
39	I2C0_SCL	DIO	Tuner I2C clock	5V tolerance even when power-off
40	I2C0_SDA	DIO	Tuner I2C data	5V tolerance even when power-off

41	VCC3_0	P	PAD I/O Power 3.3V	Digital I/O 3.3V
42	GPIO_A0	DIO	GPIO_A0	5V tolerance even when power-off
43	GPIO_A1	DIO	GPIO_A1	5V tolerance even when power-off
44	Core_1.2V	P	Core Power 1.2V	Digital 1.2V, Power Down@ Power saving
45	B_FP	AO	LVDS_Port_B_F_Pair_P	
46	B_FN	AO	LVDS_Port_B_F_Pair_N	
47	B_EP	AO	LVDS_Port_B_E_Pair_P	
48	B_EN	AO	LVDS_Port_B_E_Pair_N	
49	B_DP	AO	LVDS_Port_B_D_Pair_P	
50	B_DN	AO	LVDS_Port_B_D_Pair_N	
51	B_CP	AO	LVDS_Port_B_C_Pair_P	
52	B_CN	AO	LVDS_Port_B_C_Pair_N	
53	B_BP	AO	LVDS_Port_B_B_Pair_P	
54	B_BN	AO	LVDS_Port_B_B_Pair_N	
55	B_AP	AO	LVDS_Port_B_A_Pair_P	
56	B_AN	AO	LVDS_Port_B_A_Pair_N	
57	LVDSV	P	LVDS Power 3.3V	
58	A_FP	AO	LVDS_Port_A_F_Pair_P	
59	A_FN	AO	LVDS_Port_A_F_Pair_N	
60	A_EP	AO	LVDS_Port_A_E_Pair_P	
61	A_EN	AO	LVDS_Port_A_E_Pair_N	
62	A_DP	AO	LVDS_Port_A_D_Pair_P	
63	A_DN	AO	LVDS_Port_A_D_Pair_N	
64	A_CP	AO	LVDS_Port_A_C_Pair_P	
65	A_CN	AO	LVDS_Port_A_C_Pair_N	
66	A_BP	AO	LVDS_Port_A_B_Pair_P	
67	A_BN	AO	LVDS_Port_A_B_Pair_N	
68	A_AP	AO	LVDS_Port_A_A_Pair_P	
69	A_AN	AO	LVDS_Port_A_A_Pair_N	
70	Core_1.2V	P	Core Power 1.2V	Digital 1.2V, Power Down@ Power saving
71	GPIO_B0	DIO	GPIO_B0	5V tolerance even when power-off
72	GPIO_B2	DIO	GPIO_B2	5V tolerance even when power-off
73	GPIO_B3	DIO	GPIO_B3	5V tolerance even when power-off
74	GPIO_B4	DIO	GPIO_B4	5V tolerance even when power-off
75	GPIO_B5	DIO	GPIO_B5	5V tolerance even when power-off
76	GPIO_B6	DIO	GPIO_B6	5V tolerance even when power-off
77	GPIO_B7	DIO	GPIO_B7	5V tolerance even when power-off
78	GPIO_B8	DIO	GPIO_B8	5V tolerance even when power-off
79	VCC3_2	P	PAD I/O Power 3.3V	

80	GPIO_B9	DIO	GPIO_B9	5V tolerance even when power-off
81	GPIO_B10	DIO	GPIO_B10	5V tolerance even when power-off
82	GPIO_B12	DIO	GPIO_B12	5V tolerance even when power-off
83	Core_1.2V	P	Core Power 1.2V	Digital 1.2V, Power Down@ Power saving
84	DQS0	DO	DDR_DQS0	
85	DQ_7	DIO	DDR_Data7	
86	DQ_6	DIO	DDR_Data6	
87	SVCC25	P	DDR I/O Power 2.5V	
88	DQ_5	DIO	DDR_Data5	
89	DQ_4	DIO	DDR_Data4	
90	DQ_3	DIO	DDR_Data3	
91	DQ_2	DIO	DDR_Data2	
92	DQ_1	DIO	DDR_Data1	
93	DQ_0	DIO	DDR_Data0	
94	SVCC25	P	DDR I/O Power 2.5V	
95	DM0	DO	DDR_Data_Mask0	
96	WE#	DO	DDR Write Enable (Low Enable)	
97	CAS#	DO	DDR CAS (Low Enable)	
98	RAS#	DO	DDR RAS (Low Enable)	
99	Core_1.2V	P	Core Power 1.2V	Digital 1.2V, Power Down@ Power saving
100	BA0	DO	DDR Bank Address0	
101	BA1	DO	DDR Bank Address1	
102	ADDR10	DO	DDR Address10	
103	ADDR0	DO	DDR Address0	
104	ADDR1	DO	DDR Address1	
105	ADDR2	DO	DDR Address2	
106	ADDR3	DO	DDR Address3	
107	SVCC25	P	DDR I/O Power 2.5V	
108	ADDR4	DO	DDR Address4	
109	ADDR5	DO	DDR Address5	
110	ADDR6	DO	DDR Address6	
111	ADDR7	DO	DDR Address7	
112	ADDR8	DO	DDR Address8	
113	ADDR9	DO	DDR Address9	
114	ADDR11	DO	DDR Address11	
115	ADDR12	DO	DDR Address12	
116	CKE	DO	DDR Clock Enable	
117	SVCC25	P	DDR I/O Power 2.5V	
118	CK	DO	DDR Clock Differential(+)	
119	CK#	DO	DDR Clock Differential(-)	
120	DM1	DO	DDR Data Mask1	
121	SVCC25	P	DDR I/O Power 2.5V	
122	VREF	AI	DDR Reference Voltage Input	1.25V Ref input

123	DQ_15	DIO	DDR_Data15	
124	DQ_14	DIO	DDR_Data14	
125	DQ_13	DIO	DDR_Data13	
126	DQ_12	DIO	DDR_Data12	
127	DQ_11	DIO	DDR_Data11	
128	DQ_10	DIO	DDR_Data10	
129	SVCC25	P	DDR I/O Power 2.5V	
130	DQ_9	DIO	DDR_Data9	
131	DQ_8	DIO	DDR_Data8	
132	DQS1	DO	DDR_DQS1	
133	Core_1.2V	P	Core Power 1.2V	Digital 1.2V, Power Down@ Power saving
134	V33_IO	P	PAD I/O Power 3.3V	
135	lsadc_ref	AI	LSADC reference	Connect 10K to GND
136	lsadc0	AI	LSADC0	
137	lsadc1	AI	LSADC1	
138	lsadc2	AI	LSADC2	
139	lsadc4	AI	LSADC4	
140	STBY_Core_1.2V	P	Standby ON Core Power 1.2V	Digital 1.2V, Always On@ Power saving
141	GPIO_C0	DIO	GPIO_C0	5V tolerance even when power-off
142	GPIO_C1	DIO	GPIO_C1	5V tolerance even when power-off
143	GPIO_C2	DIO	GPIO_C2	5V tolerance even when power-off
144	GPIO_C3	DIO	GPIO_C3	5V tolerance even when power-off
145	GPIO_C4	DIO	GPIO_C4	5V tolerance even when power-off
146	RSTI	DI	Chip Reset Input	Low Active
147	SPI_CSn	DO	SPI Flash CS Output	
148	SPI_SCLK	DO	SPI Flash Clock Output	
149	SPI_SDO	DO	SPI Flash Data Output	
150	SPI_SDI	DI	SPI Flash Data Input	
151	STBY_Core_1.2V	P	Standby ON Core Power 1.2V	Digital 1.2V, Always On@ Power saving
152	GPIO_C5	DIO	GPIO_C5	5V tolerance even when power-off
153	GPIO_C6	DIO	GPIO_C6	5V tolerance even when power-off
154	GPIO_C8	DIO	GPIO_C8	5V tolerance even when power-off
155	VCC3_4	P	PAD I/O Power 3.3V	
156	VDDC_SDA	DIO	VGA DDC Data	5V tolerance even when power-off
157	VDDC_SCL	DIO	VGA DDC Clock	5V tolerance even when power-off
158	HDDC1_SDA	DIO	HDMI DDC Data 1	5V tolerance even when power-off
159	HDDC1_SCL	DIO	HDMI DDC Clock 1	5V tolerance even when power-off

160	HDDC0_SDA	DIO	HDMI DDC Data 0	5V tolerance even when power-off
161	HDDC0_SCL	DIO	HDMI DDC Clock 0	5V tolerance even when power-off
162	CEC	DIO	HDMI CEC function	5V tolerance even when power-off
163	RX_V12	AP	HDMI GDI Power 1.2V	
164	RX_V33	AP	HDMI GDI Power 3.3V	
165	HDMI_1_CLKN	AI	HDMI_RX_Port1_CLK_Pair_Negative	
166	HDMI_1_CLKP	AI	HDMI_RX_Port1_CLK_Pair_Positive	
167	HDMI_1_0N	AI	HDMI_RX_Port1_Pair0_Negative	
168	HDMI_1_0P	AI	HDMI_RX_Port1_Pair0_Positive	
169	HDMI_1_1N	AI	HDMI_RX_Port1_Pair1_Negative	
170	HDMI_1_1P	AI	HDMI_RX_Port1_Pair1_Positive	
171	HDMI_1_2N	AI	HDMI_RX_Port1_Pair2_Negative	
172	HDMI_1_2P	AI	HDMI_RX_Port1_Pair2_Positive	
173	HDMI_0_CLKN	AI	HDMI_RX_Port0_CLK_Pair_Negative	
174	HDMI_0_CLKP	AI	HDMI_RX_Port0_CLK_Pair_Positive	
175	HDMI_0_0N	AI	HDMI_RX_Port0_Pair0_Negative	
176	HDMI_0_0P	AI	HDMI_RX_Port0_Pair0_Positive	
177	HDMI_0_1N	AI	HDMI_RX_Port0_Pair1_Negative	
178	HDMI_0_1P	AI	HDMI_RX_Port0_Pair1_Positive	
179	HDMI_0_2N	AI	HDMI_RX_Port0_Pair2_Negative	
180	HDMI_0_2P	AI	HDMI_RX_Port0_Pair2_Positive	
181	TMDS_REXT	AI	TMDS External Resistor Input	Connect 6.2K to GND
182	RX_V12	AP	HDMI GDI Power 1.2V	
183	APLL_VDD	AP	APLL Power 3.3V	
184	APLL_GND	AP	APLL GND	
185	HSYNC	AI	Hsync input	
186	VSYNC	AI	Vsync input	
187	ADC_VDD33	AP	ADC Power 3.3V	
188	ADC_VDC_VDD33	AP	ADC Power 3.3V	
189	VIN_0P	AI	ADC Blue Input 1 Positive	
190	VIN_BN	AI	ADC Blue Input 1 Negative	
191	VIN_1P	AI	ADC Green Input 1 Positive	
192	VIN_GN	AI	ADC Green Input 1 Negative	
193	VIN_2P	AI	ADC Red Input 1 Positive	
194	VIN_RN	AI	ADC Red Input 1 Negative	
195	VIN_3P	AI	YPbPr Blue Input	
196	VIN_Y0N	AI	Common GND for YPbPr	
197	VIN_4P	AI	YPbPr Green Input	
198	VIN_5P	AI	YPbPr Red Input	
199	VIN_6P	AI	YPbPr Blue Input/Scart Blue	
200	VIN_Y1N	AI	Common GND for YPbPr/Scart	
201	VIN_7P	AI	YPbPr Green Input/Scart Green	
202	VIN_8P	AI	YPbPr Red Input/Scart Red/Scart C	
203	ADC_VDD12	AP	ADC Power 1.2V	

204	ADC_VDC_VDD12	AP	ADC Power 1.2V	
205	ADC_GND_OFF	AP	ADC GND	
206	VIN_11P	AI	S-Video C/Scart C Input	
207	VIN_A0N	AI	Common GND for Scart/SV	
208	VIN_9P	AI	S-Video Y/Scart Y Input	
209	VIN_12P	AI	S-Video C Input	
210	VIN_A1N	AI	Common GND for SV	
211	VIN_10P	AI	S-Video Y Input	
212	VIN_13P	AI	CVBS Input	
213	VIN_A2N	AI	Common GND for CVBS	
214	VIN_14P	AI	CVBS Input	
215	AVDD_BB1	AP	Analog Baseband Power 3.3V	
216	AGND_BB1	AP	Analog Baseband GND	
Note	1. AP : Analog Power/Ground 2. AI : Analog Input 3. AO : Analog Output 4. AIO : Analog Input/Output 5. DP : Digital Power/Ground 6. I : Digital Input 7. O: Digital Output 8. IO : Digital Input/Output			

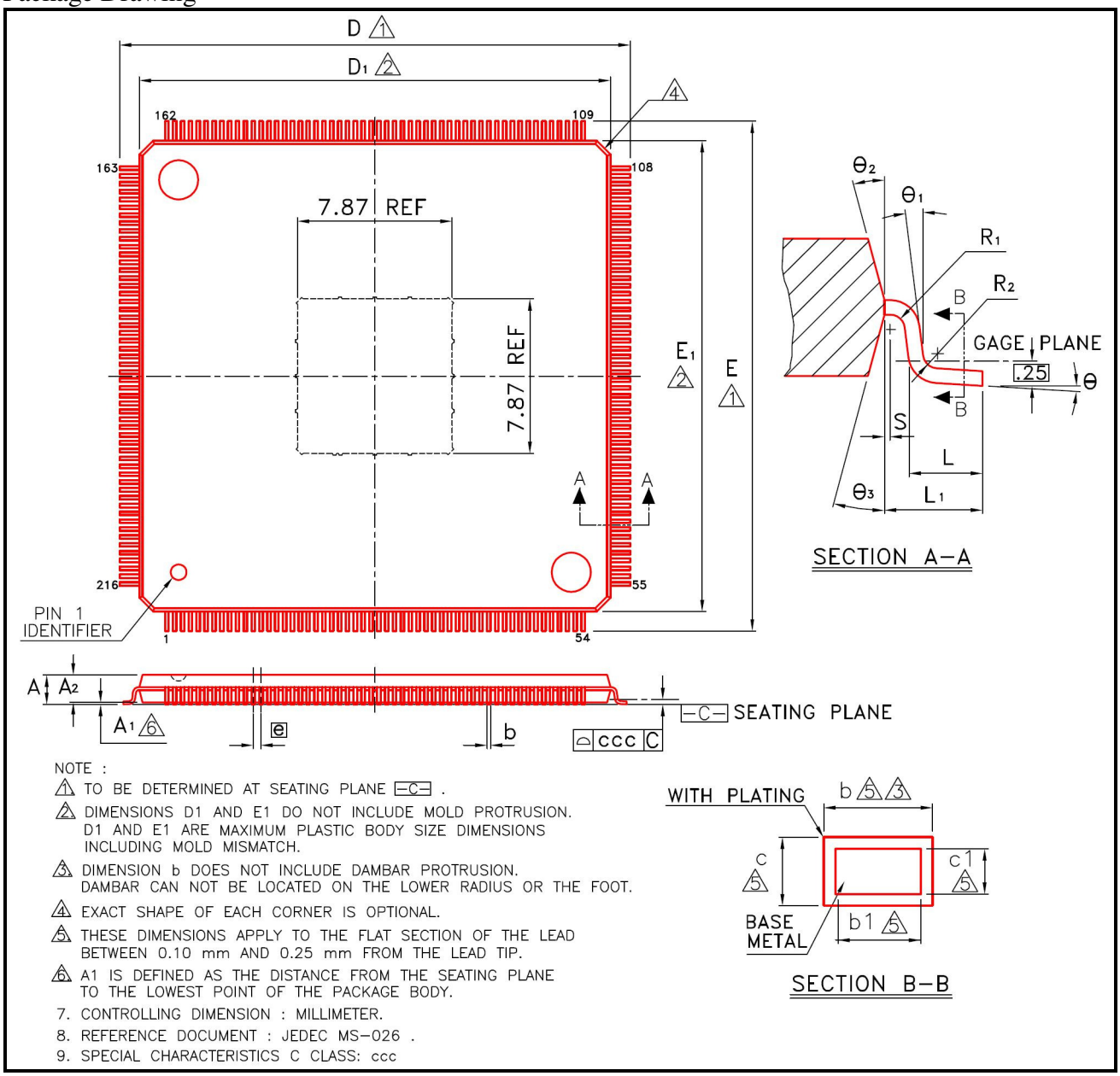
The Package selected for RTD2674S LCD TV Controller is a 216 pin E-PAD LQFP. Table 1-2 is the pin count summary table for the device.

Table 1-2. RTD2674S Pin Assignments – Pin Count

Catagory	Description	Pin Name	Pin Count
Audio	Audio Common Voltage Reference	VCM_BB	1
	Analog Baseband Power 3.3V	AVDD_BB0/1	2
	Analog Baseband GND	AGND_BB1	1
	Analog Audio input	AIN_4R/L , AIN_3R/L , AIN_2R/L , AIN_1R/L	8
	Analog Audio input/output	AIO_1R/L , AIO_2R/L	4
	Analog Audio Out	AOUT_R/L	2
	Head Phone DAC output	HPOUT_R/L	2
DAC	SCART RGB Fast Switch Input	Scart_FSW_0/1	2
	Video DAC Power 3.3V	DAC_VDD_0	1
	CVBS DAC output	AVOUT_1/2	2
	Video DAC GND	DAC_GND_0	1
IF ADC	IFADC GND	ADC2X_GND_1	1
	IF demod differential input	IF_N/P	2
	IFADC power 3.3V	ADC2X_VDD_0	1
XTAL/PLL	XTAL PLL GND	PLL_GND_1	1
	27MHz Crystal Input	XIN	1
	27MHz Crystal Output	XOUT	1
	XTAL PLL power 3.3V	PLL_VDD_0	1
Power	Core Power 1.2V	CORE_1.2V	6
	Standby Power 1.2V	STBY_CORE_1.2V	2
	PAD I/O Power 3.3V	VCC3_0 / VCC3_2 / V33_IO / VCC3_4	4
USB	USB Power 3.3V	AVDD_1	1
	USB HOST0 Data Differential	HSDM_1/HSDP_1	2
	USB Power 1.2V	LV_USB_1	1
Digital I/O	Tuner I2C	I2C0_SCL / SDA	2
	GPIO_A Group	GPIO_A0 / A1	2
	GPIO_B Group	GPIO_B0/2/3/4/5/6 GPIO_B7/8/9/10/12	11
	GPIO_C Group	GPIO_C 0/1/2/3/4/5/6/8	8
	SPI Flash Controller Signal	SPI_CSn /SCLK / SDO/SDI	4
	VGA DDC	VDDC_SDA / SCL	2
	HDMI DDC	HDDC1_SDA / SCL HDDC0_SDA / SCL	4
	CEC	CEC	1
	Reset Input	RESET	1
LVDS	LVDS_Differential	B_FP/FN, B_EP/EN, B_DP/DN, B_CP/CN, B_BP/BN, B_AP/AN, A_FP/FN, A_EP/EN, A_DP/DN, A_CP/CN, A_BP/BN, A_AP/AN	24
	LVDS Power 3.3V	LVDSV	1
GND	Digital GND	E-PAD	E-PAD
DDR	DDR_DQS	DQS0 / DQS1	2
	DDR_Data (LSB)	DQ_[7:0]	8
	DDR_Data (MSB)	DQ_[15:8]	8
	DDR I/O Power 2.5V	DDR_IO_2.5V	6
	DDR_Data_Mask	DDR_DM0 / DDR_DM1	2
	DDR Write Enable (Low Enable)	DDR_WE#	1
	DDR CAS (Low Enable)	DDR_CAS#	1

	DDR RAS (Low Enable)	DDR_RAS#	1
	DDR Bank Address	DDR_BA0 / DDR_BA1	2
	DDR Address	DDR_ADDR[12:0]	13
	DDR Clock Enable	DDR_CKE	1
	DDR Clock Differential	DDR_CK / DDR_CK#	2
	DDR Reference Voltage Input	DDR_VREF	1
LSADC	LSADC reference	lsadc_ref	1
	LSADC	lsadc0 / 1 / 2 / 4 / 6	5
HDMI	HDMI GDI Power 1.2V	RX_V12	2
	HDMI GDI Power 3.3V	RX_V33	1
	HDMI_RX Differential Signal	HDMI_1_CLKN / P, HDMI_1_0N / P HDMI_1_1N / P, HDMI_1_2N / P HDMI_0_CLKN / P, HDMI_0_0N / P HDMI_0_1N / P, HDMI_1_2N / P	16
	TMDS External Resistor Input	TMDS_REXT	1
APLL	APLL Power 3.3V	APLL_VDD	1
	APLL GND	APLL_GND	1
Sync Detect	Hsync input	HSYNC	1
	Vsync input	VSYNC	1
ADC	ADC Power 3.3V	ADC_VDD33 ADC_VDC_VD33	2
	ADC Input (Positive)	VIN_0P / 1P / 2P (for VGA) VIN_3P / 4P / 5P (for YPbPr) VIN_6P / 7P / 8P (for YPbPr/Scart RGB) VIN_11P / 9P (for Scart / SV) VIN_10P / 12P (for SV/CVBS) VIN_13P / 14P (for CVBS)	15
	ADC Input (Negative)	VIN_BN/GN/RN (VGA) V_INY0N/Y1N (YPbPr/Scart) VIN_A0N/A1N/A2N (Scart/CVBS)	8
	ADC Power 1.2V	ADC_VDD12 ADC_VDC_VDD12	2
	ADC GND	ADC_GND_OFF	1
Total Numbers of Pin Count			216

1.4 Package Drawing



NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 .
9. SPECIAL CHARACTERISTICS C CLASS: ccc

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	0.14	0.20	0.004	0.006	0.008
c_1	0.09	0.12	0.16	0.004	0.005	0.006
D	25.85	26.00	26.15	1.018	1.024	1.030
D_1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E_1	23.90	24.00	24.10	0.941	0.945	0.949
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	—	0.003	—	—
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

For RLE only